A Novel Low-Swing Voltage Driver Design And The Analysis Of Its Robustness To The Effects Of Process Variation And External Disturbances

A Thesis presented to

Newcastle University by

Nor Muzlifah Mahyuddin

In Partial Fulfilment

of the Requirement for the Degree of

Doctor of Philosophy in Electrical and Computer Engineering

School of Electrical, Electronics and Computer Engineering

Newcastle University

ACKNOWLDEGEMENT

This research project would not have been possible without the support of many people. First of all I would like to thank my advisor, Dr Saeid Nooshabadi for introducing and sharing this research idea with me.

I wish to express my gratitude to my supervisor, Dr. Gordon Russell who was abundantly helpful and offered invaluable assistance, support and guidance. I would be struggling if it was not for him, his help and concerns motivated me to complete my research successfully. Deepest gratitude is also due to the members of the supervisory and progress committee, Prof. Alex Yakovlev, Dr. Graeme Chester and Dr Fei Xia without whose knowledge and assistance this study would not have been successful. Special thanks also to all my research group members and all my course mates, for sharing the literature and invaluable assistance.

Final and importantly I wish to express my love and gratitude to my beloved families; for their understanding and endless love, throughout the duration of my studies. Especially to my beloved parents, whose invaluable support on financial and emotional fronts made this journey worth the experience. It is their unconditional love and hope which drives me to go further, to push me towards the boundary of success.

ABSTRACT

Market forces are continually demanding devices with increased functionality/unit area; these demands have been satisfied through aggressive technology scaling which, unfortunately, has impacted adversely on the global interconnect delay subsequently reducing system performance. Line drivers have been used to mitigate the problems with delay; however, these have a large power consumption. A solution to reducing the power dissipation of the drivers is to use lower supply voltages. However, by adopting a lower power supply voltage, the performance of the line drivers for global interconnects is impaired unless low-swing signalling techniques are implemented. Low-swing signalling techniques can provide high speed signalling with low power consumption and hence can be used to drive global on-chip interconnect. Most of the proposed low-swing signalling schemes are immune to noise as they have a good *SNR*. However, they tend to have a large penalty in area and complexity as they require additional circuitry such as voltage generators and *low-Vth* devices. Most of the schemes also incorporate multiple *Vdd* and reference voltages which increase the overall circuit complexity. A diode-connected driver circuit has the best attributes over other low-swing signalling techniques in terms of low power, low delay, good *SNR* and low area overhead. By incorporating a diode-connected configuration at the output, it can provide high speed signalling due to its high driving capability. However, this configuration also has its limitations as it has issues with its adaptability to process variations, as well as an issue with leakage currents. To address these limitations, two novel driver schemes have been designed, namely, nLVSD and mLVSD, which, additionally, have improvements in performance and power consumption. Comparisons between the proposed schemes with the existing diode-connected driver circuits (MJ and DDC) showed that the nLVSD and mLVSD drivers have approximately 46% and 50% less delay. The name MJ originates from the driver's designer called Juan A. Montiel-Nelson, while DDC stands for dynamic diode-connected. In terms of power consumption, the nLVSD and mLVSD drivers also produce 43% and 7% improvement. Additionally, the mLVSD driver scheme is the most robust as its *SNR* is 14 to 44% higher compared to other diode-connected driver circuits. On the other hand, the nLVSD driver has 6% lower *SNR* compared to the MJ driver, even though it is 19% more robust than the DDC driver. However, since its *SNR* is still above 1, its improved performance and reduced power consumption, as well other advantages it has over other diode-connected driver circuits can compensate for this limitation. Regarding the robustness to external disturbances, the proposed driver circuits are more robust to crosstalk effects as the nLVSD and mLVSD drivers are approximately 35% and 7% more robust than other diode-connected drivers. Furthermore, the mLVSD driver is 5%, 33% and 47% more tolerant to *SEU*s compared to the nLVSD, MJ and DDC driver circuits respectively, whilst the MJ and DDC drivers are 26% and 40% less tolerant to *SEU*s

compared to the nLVSD circuit. A comparison between the four schemes was also undertaken in the presence of ±3σ process and voltage (*PV*) variations. The analysis indicated that both proposed driver schemes are more robust than other diode-connected driver schemes, namely, the MJ and DDC driver circuits. The MJ driver scheme deviates approximately 18% and 35% more in delay and power consumption compared to the proposed schemes. The DDC driver has approximately 20% and 57% more variations in delay and power consumption in comparison to the proposed schemes. In order to further improve the robustness of the proposed driver circuits against process variation and environmental disturbances, they were further analysed to identify which process variables had the most impact on circuit delay and power consumption, as well as identifying several design techniques to mitigate problems with environmental disturbances. The most significant process parameters to have impact on circuit delay and power consumption were identified to be *Vdd*, *tox*, *Vth*, *s*, *w* and *t*. The impact of *SEU*s on the circuit can be reduced by increasing the bias currents whilst design methods such as increasing the interconnect spacing can help improve the circuit robustness against crosstalk. Overall it is considered that the proposed nLVSD and mLVSD circuits advance the state of the art in driver design for on-chip signalling applications.

Table of Contents

List of Figures

List of Tables

Chapter 1

INTRODUCTION

1.1. Background

Advances in semiconductor technology have resulted in the manufacture of smaller and subsequently faster switching devices. However, the potential for further performance improvements is being limited by the adverse effects that dimension scaling has on interconnectivity, which dominates an IC layout. As the line width of the interconnect decreases its resistance increases necessitating in the use of circuits with a high drive capability for global on-chip signalling. Many different driver circuits have been designed to address this issue; however the main problem that still exists are long propagation delay times and high energy consumption. One cannot reduce the propagation delay without increasing the energy consumption and vice versa. However, low swing drivers [1-6] have emerged to be the answer to this problem. With the ability to symmetrically lower the voltage swing on the interconnect shorter delay times and low power dissipation are able to achieved, but with one major consequence, which is reduced noise margin. Consequently, this will greatly affect the overall performance. Additionally, process variation also adds up to the problems in the performance. Effects such as noise, process variability and single event upsets (*SEU*), whose frequency of occurrence is increasing as device dimensions are reduced, should be considered in the design of low swing driver circuits to ascertain their robustness in driving long global interconnect.

This chapter continues with a general introduction to the background development of integrated circuits (*IC*) from their initial conception until present time. Subsequently, the impact of technology scaling on devices and interconnects is briefly reviewed. This is followed by brief introduction to interconnect structures; materials and interconnectivity analysis that are generally used to evaluate on-chip interconnect performance. Additionally, wire delay models and power dissipation equations are briefly introduced together with the techniques currently used to drive on-chip interconnects. As technology advances further into the deep submicron regions, process variations affect device and interconnect parameters and subsequent issues will also briefly be discussed.

1.2. History Of Integrated Circuits

Semiconductor technology started with the development of the first transistor by Bardeen, Brattain and Shockley at Bell Labs, late in 1947 [7]. As shown in Figure 1.1 IC technology started in 1958, and by the early 60s the first commercially available digital ICs were introduced by Fairchild and Texas Instruments.

In 1965, Intel's co-founder Gordon Moore had a vision of the long-term trends in the future of computing hardware. He stated, "The integrated circuit complexity will exponentially increase at a rate of roughly a factor of 2 per year"[8]. This vision is popularly known as Moore's Law. Intel has kept that pace for over 40 years, as can be seen in Figure 1.1. In 1971, Intel developed its first microprocessor, the 4004 using a P-channel silicon gate technology [9]. Subsequently, N-channel technology was developed in 1974, which had an improved performance over P-channel devices due to higher mobility of electrons compared to holes. Thus, the N-channel technology was chosen by Intel to produce the 8080, which was 10 times faster than the 8008, the processor introduced after the 4004 [9], subsequently followed by 8088, 8086 and 80286 processors. Intel made a further development in its microprocessor products when in 1985, the 80386 was introduced which was Intel is first *CMOS* processor [9].

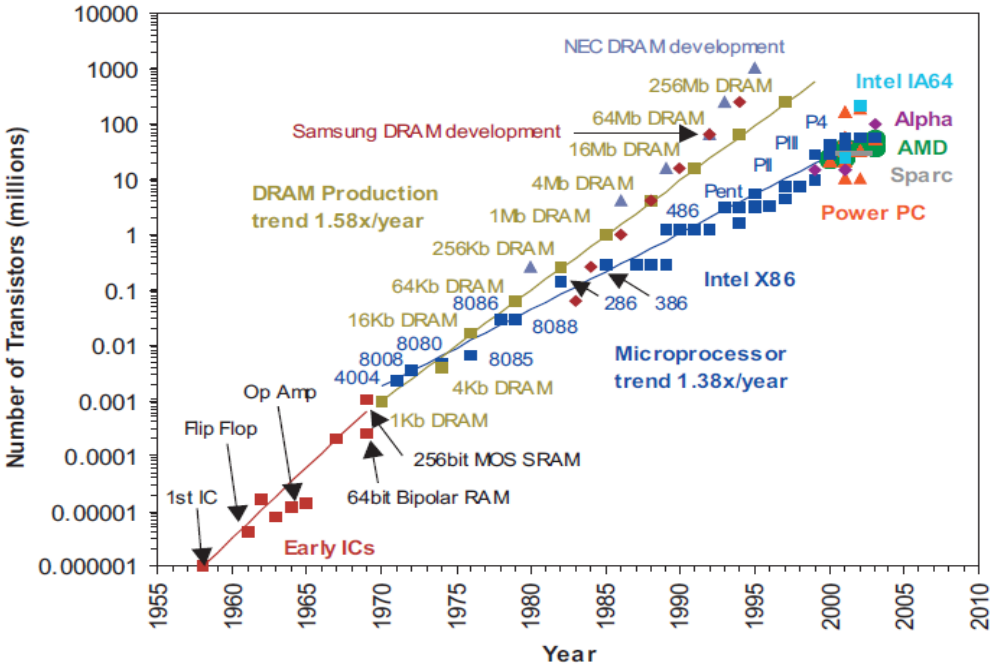


Figure 1.1: Technology advances in semiconductor industry [10].

The 90s showed the birth of the Intel Pentium, the first processor capable of executing more than 1 instruction per clock cycle. The introduction of the Pentium in 1993 was subsequently followed by the Pentium Pro in 1995, Pentium II in 1997 and Pentium III in 1999. The monopoly of the semiconductor industry by Intel became very apparent from the beginning of 2000 until today, with the implementation of Pentium 4 with 180nm technology, followed by 130nm, 90nm and 65nm versions. In 2007, Intel's 45nm technology was debuted as the first high-k gate silicon technology with dual metal gates, which dramatically increases the processor's energy efficiency. This technology is used in the implementation of recent Intel Core 2 Duo processor.

The number of transistors recorded for every generation of integration in Intel is shown in Table 1.1. The Intel Core 2 Duo processor contains 1.7 billion transistors [11]. It is categorized as the Ultra Large Scale Integration (*ULSI*) chip. The most recent examples of advancement in integration are System on Chip (*SoC*) and the 3D ICs. SoC comprises of multiple function systems on a single silicon chip, which cuts development cycle while increasing product functionality, performance and quality. A 3D IC is a chip with two or more stacked layers of electronic components, integrated or interconnected vertically into a single module [12], which is noted for its increased density, speed and power maintenance but also offers unique security advantages such as mitigating the problem with reverse engineering through its stacking process, which will conceal almost all of the circuitry.

Table 1.1: Number of transistors for different generations of Intel processor [8].

Microprocessor	Year	Number of Transistors
Intel 4004	1971	2,300
Intel 8086	1978	29,000
Intel 80,486	1989	1,200,000
Intel Pentium	1993	3,100,000
Intel Pentium II	1997	7,500,000
Intel Pentium III	1999	9,500,000
Intel Pentium 4	2000	42,000,000
Intel Itanium 2	2003	220,000,000
Intel Dual Core Itanium 2	2007	1,700,000,000

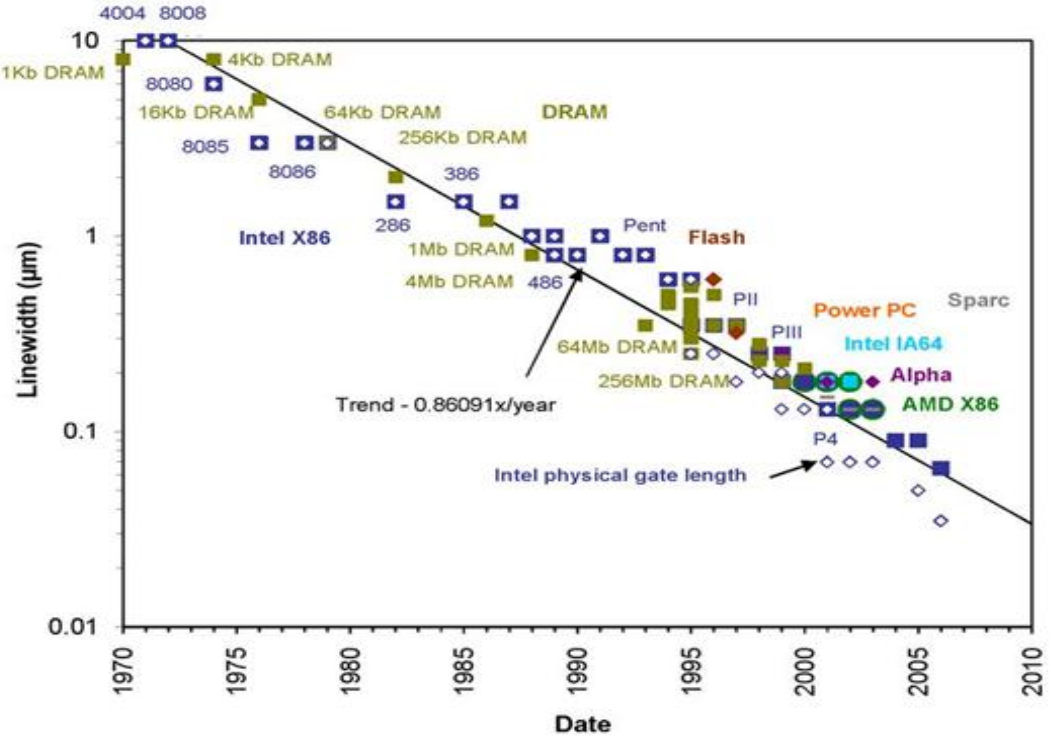


Figure 1.2: The linewidths for different generation of IC technology [13].

As pointed out by the Moore's Law, the transistor count doubled every 2 years and this is mostly due to the significant reduction in linewidth as can be seen in Figure 1.2. The shrinking linewidth enables more components to fit onto an IC. However, there are a number of consequences related to the shrinkage in linewidth. The reduction in linewidth not only affects overall circuit performance, but also requires several modifications to be made in the manufacturing process, which leads to the increase in complexity of the processes being used. This means the equipment has to have greater precision, resulting in the need for more costly equipment as linewidth shrinks in size.

1.3. Devices

1.3.1. *MOSFET* structure and operation

The *MOSFET* is a four-terminal device, where the current flows between the source and drain region when the voltage is applied to the gate terminal. The fourth terminal is represented by the body which serves to modulate the device characteristics and parameters [14]. There are three main *MOSFET* technology families; *PMOS*, *NMOS* and *CMOS*. *PMOS* device is made by diffusing p-type dopants into an n-type silicon substrate to form the source

and the drain. In this type of transistor, current is carried by positively charged carriers, which are holes, moving through a p-type channel. *NMOS* is similar to *PMOS* but uses N-type dopants to make n-channel transistors in p-type silicon substrate. The current flows through n-type channel between source and drain, which is carried by the negatively charged carriers, i.e. electrons. *CMOS* is a combination of both p-channel and n-channel devices on the same silicon substrate. The structure of *CMOS* device is shown in Figure 1.3.

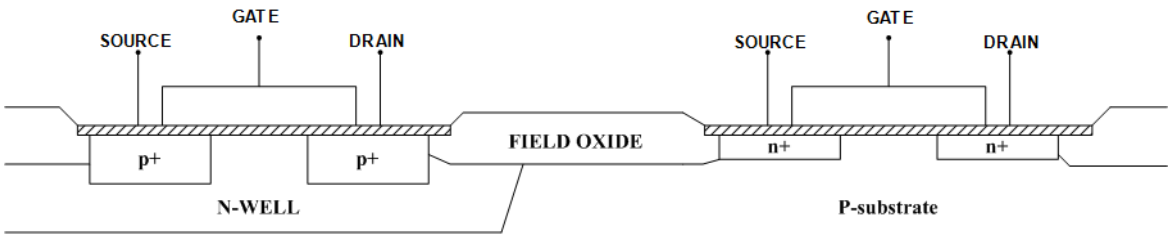


Figure 1.3: Cross-section of *CMOS* device [15].

The operation of a *MOSFET* device involves flow of current between the drain and source terminals by applying voltage to the gate terminal. A thin layer of silicon dioxide (S_iO_2) is situated below the gate terminal. For proper operation, a voltage terminal is also applied to the bulk or silicon substrate. Considering an *NMOS* transistor as an example, when the gate voltage is increased above certain threshold voltage (*Vth*), a conducting channel of electrons is formed in the p-type silicon substrate between the n-type source and drain. The conductivity of the channel is modulated by the gate voltage which means the larger the voltage difference between the gate and the source, the smaller the resistance of the conducting channel and larger the current. When the voltage is lower than *Vth*, no channel exists and the transistor is considered to be open. This behaviour makes transistor a suitable switching device in digital circuits.

1.3.2. Power dissipation of *CMOS* circuits

CMOS circuits can be in two distinct states; a static state during highs and lows of the signals or clocks, and a dynamic state during the transitions. The total device power can be broken down to static and dynamic components, and is made of dynamic power and power due to the static state of the signals.

Dynamic power dissipation is a function of switching factor (α), total load capacitance, supply voltage and switching frequency, which is shown in Equ.1.1 [16];

$$P_{dyn} = \alpha C_L V_{DD}^2 f. \quad (1.1)$$

Static power dissipation is expressed as a product of static current and supply voltage. It can be calculated by Equ.1.2;

$$P_{stat} = I_{stat}.V_{DD} \quad (1.2)$$

$$I_{stat} = I_s\left(e^{qV/kT} - 1\right) \quad (1.3)$$

The static current flows between the supply rails in the absence of switching activity, which should be equal to 0 as *PMOS* and *NMOS* devices are never on simultaneously in the static state. However, this is not the case as there is a leakage current flowing between source or drain and the substrate. This leakage current can be described using a model in Figure 1.4 where it describes the parasitic diodes of a CMOS inverter. The leakage current is described by Equ.1.3, where I_s is a reverse saturation current; *V*, a diode voltage; *k*, a Boltzmann's constant; *q*, an electronic charge and *T* is for temperature. This is called sub-threshold current and it becomes more apparent as the technology scales down. Circuit designers are beginning to consider static power just as important as dynamic power in power analysis.

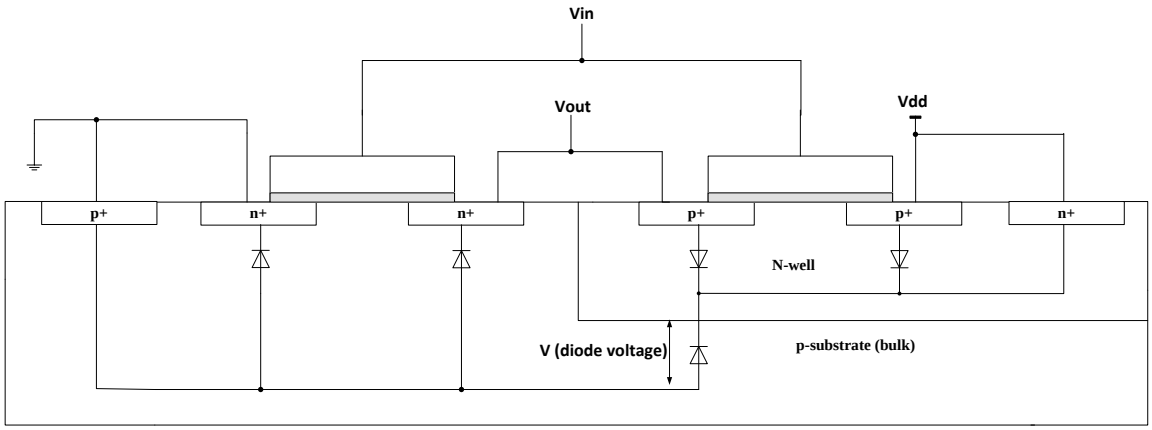


Figure 1.4: Model containing presence of parasitic diodes in CMOS inverter.

1.3.3. Device Scaling

As discussed previously in Section 1.2, the reduction line widths have a significant impact on die sizes and yields, the reduction in feature sizes also influences the properties of the *MOS* transistor as well as indirectly affecting the design metrics such as the switching frequency.

There are two basic types of device scaling; full scaling and fixed-voltage scaling. Full scaling is also known as constant electric field scaling where voltages and dimensions are scaled by the same factor *S*. Full scaling keeps electric fields constant, which ensures the

physical integrity of the devices and avoids breakdown or other secondary effects. This type of scaling results in higher performance, reduced power consumption and greater device density. The effects of full scaling on the device and circuit parameters are shown in Table 1.2.

Table 1.2: Scaling for short-channel devices [14].

Parameter	**Relation**	**Full Scaling**	**Fixed-Voltage Scaling**
W, L, t_{ox}		$1/S$	$1/S$
V_{DD}, V_T		$1/S$	1
$Area_{device}$	WL	$1/S^2$	$1/S^2$
C_{ox}	$1/ t_{ox}$	S	S
C_{gate}	$C_{ox}WL$	$1/S$	$1/S$
I_{sat}	$C_{ox}WV$	$1/S$	1
Current Density	$I_{sat}/Area$	S	S^2
R_{on}	V/ I_{sat}	1	1
Intrinsic Delay	$R_{on} C_{gate}$	$1/S$	$1/S$
P	$I_{sat}V$	$1/S^2$	1
Power Density	$P/Area$	1	S^2

The intrinsic delay is the product of the gate capacitance and the on-resistance of a transistor and is a constant, due to the simultaneous scaling of voltage supply and current levels. Therefore, the improved performance is mainly due to the reduced scaling of the gate capacitance. Power consumption is the product voltage supply and current where both scale down significantly, resulting in a quadratic reduction in power.

Fixed-voltage scaling is proposed as a better alternative to full scaling. This is because full scaling is not feasible in reality since the voltage cannot be scaled aberrantly for the new devices to be compatible with existing components. Therefore, the device dimensions are reduced by a factor of S while the voltage remains constant. However, in a velocity-saturated device, keeping the voltage constant while scaling the device dimensions increases the drain current and power density by a factor of S^2, as shown in Table 1.2. Additionally, this will lead to serious reliability problems such as hot-carrier degradation, oxide-breakdown [17].

To summarize the discussion on device scaling, some of the main characteristics on the recent *CMOS* processes and future predictions are shown in Table 1.3. The effective drive current remains approximately constant. In order to maintain this level of drive current with a continuously reduced supply voltage, aggressive down-scaling of the threshold voltage is

required. This however causes a rapid increase in the gate leakage and sub-threshold leakage current.

Table 1.3: Scaling trends for device and interconnect [18].

Year of Production		2005	2007	2010	2013
Technology DRAM 1/2 Pitch(nm)	*L*	*80*	*65*	*45*	*32*
No of metal levels		*11*	*11*	*12*	*13*
Power supply voltage(V)	V_{dd}	*1.1*	*1.1*	*1*	*0.9*
Effective NMOS drive current(μA/μm)	I_{dd}	*1020*	*1211*	*1807*	*2109*
Effective parasitic series source/drain (kΩ-μm)	R_{sd}	*0.18*	*0.2*	*0.18*	*0.17*
Total gate capacitance(fF/μm)	Cg_{total}	*1.63*	*0.71*	*0.84*	*0.658*
Intrinsic delay of MOSFET, CV/I (ps)	*Di*	*0.87*	*0.64*	*0.46*	*0.28*
Maximum On-chip Frequency(GHz)	*Freq*	*5.20*	*4.70*	*5.88*	*7.34*
*Minimum Clock Period = 15 FO4 = 212.5 * CV/I (ps)*	*T*	*184.88*	*136.00*	*97.75*	*59.50*
Saturation Threshold Voltage (mV)	V_{TH}	*195*	*134*	*103*	*93*
Gate leakage (A/cm²) x10²		*1.88*	*8.00*	*1.56*	*2.23*
Subthreshold Leakage (μA/μm)	I_{lkg}	*0.06*	*0.2*	*0.28*	*0.29*
Minimum Global wiring pitch(μm)	*w+s*	*0.3*	*0.21*	*0.135*	*0.096*
Average Global wiring dual damascene, AR	*t/w*	*2.2*	*2.3*	*2.4*	*2.5*
Interconnect delay RC for 1mm Cu min pitch global wire(ps)	*τ*	*111*	*227*	*542*	*1129*
Conductor effective resistivity for minimum width global wires, nΩ-m (with skin effect)	*ρ*	*25.3*	*27.3*	*31*	*35.2*
Capacitance per unit length for global wires(pF/cm)	C_w	*2.2*	*2.15*	*1.9*	*1.85*
Interlevel metal insulator permittivity	*k*	*3.25*	*3.1*	*2.75*	*2.6*

1.4. On-Chip Interconnectivity

Interconnect is one of the most important components in on-chip signalling. This is apparent since the interconnect parameters have great influence on the overall circuit performance, especially on longer wires.

1.4.1. Structure and materials

There are two types of on-chip interconnectivity namely local and global. Local interconnects, which are relatively short, are between gates within a functional block for example an *ALU*; global interconnects, which are much longer, are used to transport signals

between functional blocks and are usually configured in a bus structure, with the exception of the clock signal. The global interconnects are usually routed on the upper low resistance metallisation layers on a chip. The length of the interconnect not only creates larger signal delays but also has a relatively large coupling capacitance which renders the signal transported along the lines more susceptible to noise effects. Furthermore the adverse effects of technology scaling, as discussed later, impacts heavily on the performance of the global interconnects and is a major challenge to circuit designers.

As shown in Figure 1.5, circuit interconnectivity creates a very complex structure comprising many layers of 'wires' separated by a dielectric insulation, namely SiO_2.

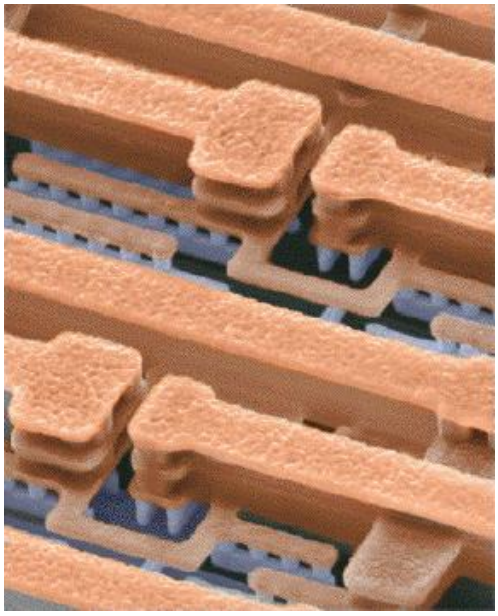


Figure 1.5: A three dimensional view of interconnect structure [19].

Currently the materials used for conductors are Aluminium (*Al*) and Copper (*Cu*). Aluminium-based alloys are used for mature process while Copper-based alloys are used, for example, in modern high performance microprocessors. The formation of aluminium interconnects is achieved using either a physical vapour deposition (*PVD*) or chemical vapour deposition (*CVD*) process to cover the entire chip area; the actual interconnect pattern is subsequently delineated using a photolithographic procedure followed by an etching process.

Copper has a narrower line width than Aluminium but with the same resistivity which results in a denser interconnect system. Copper material is deposited by an electrochemical or vapour deposition process. The etching process for Copper is harder than Aluminium since

dual damascene process [20] is used which involves the deposition of Copper on previously etched oxide trenches and later to be removed using chemical mechanical planarization (*CMP*) process. Copper-based alloy is more expensive than Aluminium-based alloy but can be compensated by better performance.

The dielectric material is Silicon Dioxide (S_iO_2), which has good dielectric properties and is compatible with the rest of the IC processing steps. The dielectric constant for SiO_2 is 3.9 which is considered to be a high-k dielectric material. The dielectric material influences the value of capacitance between conductors through its dielectric constant. As the dielectric constant increases, the interconnect capacitance also increases which leads to longer delays and the increased potential for crosstalk interference between the interconnect wires. Recently, low-k dielectric materials have been introduced and are implemented on most circuits as the requirement for high speed signalling [21].

1.4.2. Parasitic components

Interconnect is composed of three parasitic components; capacitance (*C*), resistance (*R*) and inductance (*L*). These components are used to model the wire which is extremely useful in timing analysis, especially in estimating the interconnect delay. However, most designers prefer to implement *RC* model compared to *RLC* model, because their ability to link interconnect performance easily with physical layout definitions such as line widths, line separation.

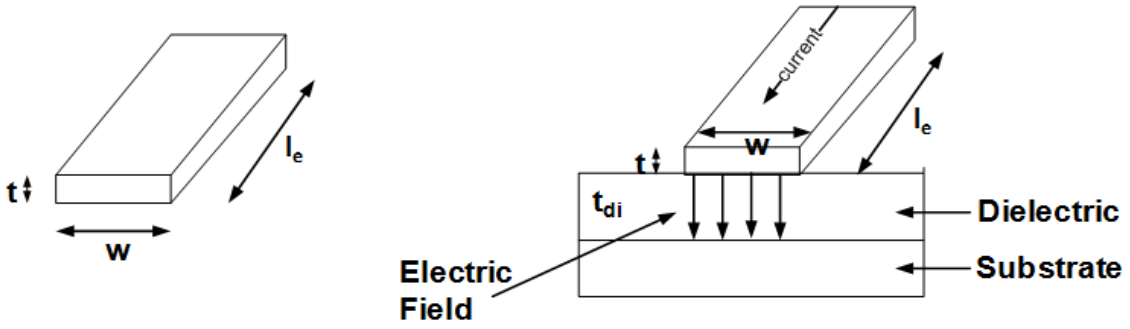
Inductance effects are increasingly important for most on-chip interconnects but the *RC* model is still sufficiently accurate to model local and intermediate wires lengths. Even for global interconnects, *RC* model is still preferable over the *RLC* model due to its simplicity and efficiency and is still being frequently implemented in the majority of interconnect timing and crosstalk noise estimations [22]. Therefore for this thesis, only the *RC* model is considered, i.e. the parasitic components to be discussed will only cover resistance and capacitance.

On-chip interconnect structures are composed of a metal line with rectangular cross-section as shown in Figure 1.6(a). With a uniform metal line of width (*w*) and thickness (*t*), interconnect resistance (*R*) can be calculated as,

$$R = \frac{\rho l_e}{wt}\,, \tag{1.4}$$

where l_e is the interconnect length and ρ is the resistivity of the metal.

In addition to metal lines, vias, which connect multiple layers vertically, contribute to interconnect resistance as well. As the number of metal layers steadily increases and the via size continues to shrink, the effect of via resistance can contribute as much as an additional 10% to the total critical path delay [23]. Wire delay is strongly influenced by the interconnect resistance as it causes Ohmic (*IR*) drop along the wires, which significantly reduces the noise margin, especially if the current density is high.



(a) (b)

Figure 1.6: Structures of interconnect (a) resistance and (b) capacitance.

Interconnect capacitance is known as the coupling of electrical field between the lines. It is a function of the dimensions, distance to surrounding wires and distance to the substrate, as shown in Figure 1.6(b). The value of capacitance is calculated as follows

$$C = \frac{\varepsilon_{di}}{t_{di}} w l_e\,, \tag{1.5}$$

where w and l_e are the width and length of the interconnect, and t_{di} and ε_{di} represent the thickness and permittivity of the dielectric layer respectively.

1.4.3. Interconnectivity Analysis

The implementation of an interconnectivity scheme is analysed in terms of the wire delay, energy consumption and signal integrity which comprises components such as slew rate, crosstalk noise and overshoot.

1.4.3.1. First order wire delay model

One of the most important factors describing the performance of a wire is its delay or latency, which is usually, measured at the 50% V_{DD} points, from the input of the driver to the end of the line (the input of the receiver). Delay is a function of driver strength and wire loading.

When analysing interconnect delay a first order wire delay model known as Elmore delay model [14] is frequently used. Elmore states that the first order time constant at one node is the sum of the *RC* components at that particular node. Therefore, every segment of the wire can contribute to the delay. Based on Elmore model analysis, the delay for distributed model line is as shown in Figure 1.7 and expressed as follows,

Figure 1.7: Elmore delay model [14].

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j \qquad (1.6)$$

The distributed model is commonly used to represent a wire, especially longer wires. The larger the number of segments for distributed model, the more accurate the wire delay is. However in the *SPICE* circuit simulator, the large number of segments is represented by the π model [22] as it is a reasonable approximation of distributed *RC* model.

1.4.3.2. Energy consumption

Due to technology scaling and larger chip sizes, on-chip signals must be transported across more resistive and longer interconnects within shrinking delay budgets [24]. Longer interconnects will lead to a larger total capacitance and thus to more energy consumption. The ever increasing energy consumption of an integrated circuit is mainly due to the interconnect wires and the associated driver and receiver circuits with 40% [14] of it dominated by the interconnect wires. Designers are starting to consider trading off speed for power as circuit techniques such as low swing signalling [1-6] and bit encoding [25-27] have been developed at the cost of reduced noise immunity, routing density and delay penalty.

1.4.3.3. Signal integrity

Signal integrity of the global interconnects deteriorates in the nano-meter regime. This is the result of technology scaling where the on-chip interconnect has a smaller pitch in the advanced technology nodes. The interconnect pitch is scaled down in order to support the increasing device density. In addition, in order to mitigate the delay problem, the scaling of the cross-sectional area of metal wires is required. This results in narrower and taller metal wires, which leads to larger aspect ratio. This improves the interconnect delay problem but causes stronger coupling between neighbouring lines, which will lead to crosstalk noise [22]. Crosstalk noise affects the performance of a circuit by distorting the original switching waveforms which leads to a significant delay variation.

In addition to crosstalk noise, another issue that needs to be considered in designing on-chip interconnect is the slew rate. The slew rate or rise time is defined as the time required for the signals to change from 10% to 90% of its final value. In reality, the slew rate is finite which delays signal stabilization, especially if the driver strength is limited and the interconnect line is lossy.

1.4.4. Interconnect Scaling

Section 1.3.3 described the types of scaling for devices and its impact on the characteristics of a *MOS* transistor and its performance. The improvement in performance is very much associated with the scaling of the device dimensions. Therefore, as the device dimensions are scaled down, the interconnect dimensions must also be reduced to take full advantage of the scaling process.

The interconnect scaling used is called ideal scaling. It is similar to full scaling of devices as all dimensions of the wire are scaled by the same factor *S*. The length of local interconnects scale in the same way as the devices but global interconnects scale differently. Global interconnects provide interconnectivity between large blocks and the input-output circuitry. The average length of long wires is proportional to the die size of the circuit. As the feature size of a device has continued to shrink over the past decades, the die size is gradually increased [13]. Due to these circumstances, scaling between local and global interconnects needs to be differentiated.

The effects of interconnect scaling are shown in Table 1.4, where the dimensions of local wires are scaled with a factor *S*. The scaling of global wires is different and more

complicated, which results in a significant increase in the delay of the global wires. This is a great contrast to the gate delay, which reduces from year to year, and is the reason why interconnect delay is becoming an important factor in integrated circuit design.

Table 1.4: Ideal scaling of interconnect [14]

Parameter	Relation	Local Wire	Global Wire
W, H, t		*1/S*	*1/S*
l		*1/S*	$1/S_C$
C	*lW/T*	*1/S*	$1/S_C$
R	*l/WH*	*S*	S^2/S^C
CR	L^2/Ht	*1*	$S^2/S_C{}^2$

Table 1.3 clearly shows that there is a rapid increase in global interconnect delay. As stated in [18] a 0.7X reverse interconnect scaling trend and 14% increase in die size, have created a challenge for on-chip global interconnect in high performance microprocessors in achieving low propagation delay and high signalling bandwidth [4]. The *RC* time constant increases with each technology node due to a significant increase in resistance despite a small decrease in capacitance, which also leads to a greater deviation in the line edge rate.

The scaling in interconnect is not just due to the critical scaling of its dimension but also relates to its manufacture. Due to yield and manufacturing limitations in scaling with the interconnect thickness, the aspect ratio (*AR*) also continues to increase as shown in Table 1.3. The requirement to minimize dishing on patterned metal line structures and the need to minimize the variations in the sheet resistance, caused by the extensive copper dishing and erosion due to the Chemical Mechanical Planarization (*CMP*) process, are among the factors that influence the increase in AR. These factors also cause a similar increase in the inter-level dielectric (*ILD*) thickness, which will have significant impact on interconnect capacitance.

1.5. Techniques For Driving On-Chip Interconnect

Main problems with long interconnect signalling is caused by the large *RC* time constant, which varies as the square of the length. The large *RC* time constant can degrade the processor performance. Several solutions to this problem have been introduced and are briefly described below.

1.5.1. Repeater insertion

Figure 1.8 shows interconnection between a driver and a receiver with and without repeater insertion. Almost 50% of the total path delay is monopolised by the interconnect delay. The propagation delay over long interconnect can be minimized by using repeater insertion technique.

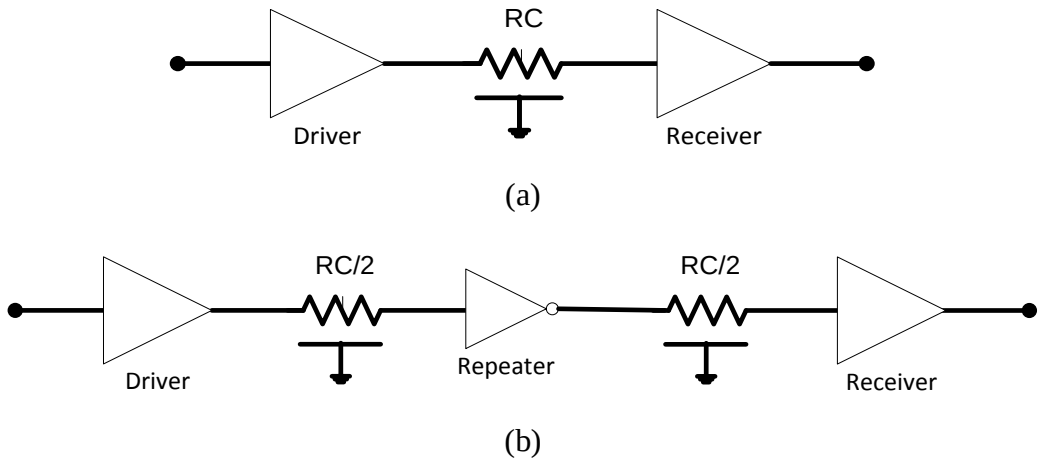


Figure 1.8: The models of (a) normal interconnect and (b) interconnect with a repeater.

The repeater insertion involves dividing a long interconnect into smaller segments and a repeater is inserted to drive each of these segments. By inserting repeaters along the interconnect wire length, the total delay can be reduced, however, there are few disadvantages associated with this method. This technique increases the power dissipation of bus due to large buffers needed to drive the bus. In nano-meter technologies, the leakage power dissipation in these buffers can account for more than 20% of total power consumption [28]. In addition, the delay associated with repeaters themselves also contribute to delay performance of global interconnects.

1.5.2. Low voltage swing signalling

Although low voltage swing signalling technique is usually implemented for power reduction, this technique can also be used for high speed signalling. There are two types of low voltage swing signalling namely, differential and single-ended signalling. Both techniques incorporate reduced voltage swing on the interconnect wire but differ in the number of wires used. For example differential signalling requires 2 wires, which transmit the signal data across the entire length of interconnect. A sense amplifier at the receiving end will detect the voltage difference and convert the received signal back to its normal level.

However, this type of signalling is exposed to the possibility of jitter variation and additional delay by the amplifier. This is mainly due to the use of 2 wires with different signal transitions on each wire. Single-ended signalling will not suffer from these factors but is prone to noise. Recently, there have been several designs proposed which incorporate either single-ended or differential signalling. These new low swing techniques improve on their delay and noise immunity as well as their energy efficiency [1], [3], [6], [29], and will be discussed in more details in Chapter 2.

1.6. The Impact Of Process Variation On On-Chip Signalling

Process variations are categorized as either die-to-die (*D2D*) or within die (*WD*) variations. WD variations, also known as intra-die variations are focus of this study. These variations are random and can be classified into two categories, which are device variations and interconnect variations. Device variations and interconnect variations can also be categorized as intrinsic variation as they are mostly caused by the fabrication process. They can be further categorized as systematic or random.

1.6.1. Device variations

Manufacturing process parameter variation becomes a major bottleneck to the reliable design of *VLSI* systems in nanometer region [30,31]. The imperfections in the process parameters due to sub-wavelength lithography and device variations in small geometry devices such as random dopant fluctuations and line edge roughness, cause great variations in the circuit parameters, such as *Vth*, oxide thickness (*tox*), mobility (μo), device width and effective gate length (L_{eff}).

Vth variability is caused by variability in oxide thickness and dopant fluctuations. Statistical variation in device parameters leads to a statistical distribution of *Vth*. Since *Vth* corresponds to the circuit delay, this will also lead to statistical distribution of the circuit delay. Leakage power has exponential dependence on *Vth*. Therefore, small variations in *Vth* will cause large variability in leakage power [32]. It is expected that high performance microprocessors will be exposed to 30% variation in maximum allowable operating frequency and 20X variation in the leakage power [30] due to variation in transistor parameters.

The main source of circuit performance variability is channel length variation, which is due to D2D and WD variations. Since each variation can cause increase in variability of one or more key design parameters, the variation in channel length will affect the switching speed and static leakage current. This is due to the strong connection of *Vth* to the channel length. Channel length variability results from wafer non-uniformity or line edge roughness. Meanwhile, device width variation is caused by polishing or lithography issues.

1.6.2. Interconnect variations

Most of the work regarding process variation focuses on the impact of within die variation in devices without considering variations in the interconnect. This will result in an inaccurate yield estimation and circuit optimization for current and future technologies. In DSM technologies, interconnect variation becomes increasingly important especially on signal delays.

The interconnect variation results from uncertainties of physical parts of line, for example, interconnect width, inter-wire spacing, ILD thickness and the aspect ratios. Some of which are introduced by CMP processes to planarize the IC surface. The CMP processes cause surface imperfections in the wires due to dishing and erosion. This is important source of timing variability [33]. The variations in the wire dimensions greatly affect the interconnect resistance. It is considered that interconnect resistance is more sensitive to process variation than interconnect capacitance due to the narrow line effects.

1.7. Main Contributions Of This Research

Market forces are continually demanding devices with increased functionality per unit area which have been satisfied through aggressive technology scaling, adversely affecting on the global interconnect delay thus reducing system performance. Line drivers can be used to mitigate the delay problem but its main problem is its high dynamic power consumption. One solution is to reduce *Vdd* but this can impair the performance of the line drivers for global interconnect unless low swing techniques are implemented. Although they can provide high speed signalling with low power consumption, most of the low swing techniques suffer from large area penalty and increases in circuit complexity. In addition, most of the techniques require additional circuitry such as voltage generators and low-Vth devices, as well as

incorporating multiple Vdd and reference voltage sources. Subsequently, they also show the non-adaptability towards process variation and leakage currents.

In order to address these limitations, two novel driver schemes have been designed, namely, nLVSD and mLVSD, which show vast improvements in terms of delay and power consumption, as well as noise immunity and leakage current. These improvements will be shown in the later sections. Therefore, the main contributions of this research to the low swing signalling applications are as follows:

a) Improved delay performance
b) Improved power dissipation
c) Occupies smaller footprint
d) Developed new leakage control circuits
e) Analysed robustness to process variations and external disturbances
f) Identified which process variables have the most impact on delay and power consumption
g) Developed design techniques to mitigate the effect of process variations
h) Developed design techniques to mitigate the effects of SEU and crosstalk

1.8. Publications

a) N. M. Mahyuddin, G. Russell, and E. G. Chester, "Design and analysis of a low-swing driver scheme for long interconnects," *Microelectronics Journal*, vol. 42, no. 9, pp. 1039-1048, 2011.

1.9. Outlines And Scope Of Thesis

Having briefly introduced the advances in semiconductor technology over the past fifty years, the subsequent issues resulting from the reduction in the physical dimensions of devices and interconnects and the contributions of this research towards low swing signalling application; the subsequent chapters will described the work carried out in this research programme to address the power and performance issues related to scaling effects on interconnects. Chapter 2 reviews low voltage swing techniques for line driver implementation as these methods are considered to be the most efficient regarding power dissipation and have less impact on performance. Chapter 3 introduces advancement to the state of the art in low voltage swing driver design. Building on the work outlined in Chapter

3 a complete on-chip signalling system comprises, driver, interconnect and receiver, represented by a level converter is also presented. As device geometries shrink circuit packaging densities increase and circuit application become more susceptible to temporary faults such as crosstalk and SEUs, thus it is important to consider the effect of these faults on the low-swing signalling schemes, as discusses in Chapter 4. Subsequently, as technology nodes become smaller the effects of process variations on circuit performance become more evident; consequently Chapter 5 outlines the analyses of the effect of process variation on the performance of the proposed signalling system. The final chapter comprises the discussion of the performance and variability analyses carried out in previous chapter and followed by the overall conclusions resulting from the investigation, and suggestions for future works, respectfully.

References

[1] J. C. Garcia, J. A. Montiel-Nelson, and S. Nooshabadi, "Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects," *IEEE International Symposium on Circuits and Systems, ISCAS 2007*, pp. 881-884, 2007.

[2] J. C. Garcia, J. A. Montiel-Nelson, and S. Nooshabadi, "Bootstrapped full-swing CMOS driver for low supply voltage operation," *Design, Automation and Test in Europe 2006. DATE '06*, vol. 1, pp. 410-411, 2006.

[3] H. Zhang, V. George, and J. M. Rabaey, "Low-swing on-chip signaling techniques: effectiveness and robustness," *IEEE Trans. Very Large Scale Integrated System*, vol. 8, no. 3, pp. 264-272, 2000.

[4] L. Zhang, J. Wilson, R. Bashirullah, L. Luo, J. Xu, and P. Franzon, "Driver pre-emphasis techniques for on-chip global buses," in *Proceedings of the 2005 International Symposium on Low Power Electronics and Design, ISLPED '05*, 2005, pp. 186-191.

[5] M. Ferretti and P. A. Beerel, "Low swing signaling using a dynamic diode-connected driver," *Proceedings of the 27th European Solid-State Circuits Conference. ESSCIRC 2001*, pp. 369-372, 2001.

[6] A. Narasimhan, M. Kasotiya, and R. Sridhar, "A low-swing differential signalling scheme for on-chip global interconnects," *18th International Conference on VLSI Design*, pp. 634-639, 2005.

[7] D. P. Bob Donlan, "Pushing the Limits: Looking Forward..Looking Back," *Microelectronic Design*, vol. 1, 1987.

[8] "Moore's Law: Raising the Bar," *http://download.intel.com/museum/Moores_Law/Printed_Materials/Moores_Law_Backgrounder.pdf*, 2005.

[9] "History of the Integrated Circuit," *cited Sept. 2010: Available from http://www.icknowledge.com/history.html*.

[10] S. W. Jones, "Introduction to Integrated Circuit Technology," *cited Sept. 2010: Available from http://www.icknowledge.com*, vol. September.

[11] Intel, "New Dual-Core Intel Itanium 2 Processor Doubles Performance, Reduces Power Consumption," *cited Sept. 2010: Available from http://www.intel.com/pressroom/archive/releases/2006/20060718comp.htm*, vol. September, 2006.

[12] E. Beyne, "3D System Integration Technologies," *International Symposium VLSI Technology, Systems and Applications*, pp. 1-9, 2006.

[13] S. W. Jones, "Exponential Trends in the Integrated Circuit Industry," no. 2010. 2008.

[14] A. C. J. M. Rabaey Borivoje Nikolic, *Digital Integrated Circuits*, 2nd ed. Prentice Hall, 2003.

[15] STMicroelectronics, "Introduction to semiconductor technology," *AN900 Application Note*. 2000.

[16] C. Piguet, "Low-Power Electronics Design," in *Computer Engineering*, 1st ed., V. Oklobdzija, Ed. Switzerland: CRC Press, 2005, pp. 159-161.

[17] S. K. and Y. Leblebici, "CMOS Digital Integrated Circuits." 1999.

[18] "International Technology Roadmap for Semiconductors," *www.itrs.net accessed January 2010*.

[19] "Materials and Devices website for Scientists and Engineers," *http://materials.usask.ca/images/photos/SEMof3LevelCuInterconP98.GIF accessed on February 2011*, 1997.

[20] J. Healey, "Current Technical Trends: Dual Damascene and Low-k Dielectrics." Threshold Systems, pp. 1-6, 2002.

[21] F. Moll, *Interconnection noise in VLSI circuits*. Springer, 2004.

[22] B. P. Wong Mittal Anurag, Cao, Y., Starr, G., *Nano-CMOS circuit and physical design*. John Wiley & Sons, 2005.

[23] C. Visweswariah, "Death, taxes and failing chips," *IEEE Design Automation Conference*. pp. 343-347, 2003.

[24] D. Sylvester Kaul, H., "Power Driven Challenges in Nanometer Design," *IEEE Design and Test of Computers*, vol. 13, pp. 12-21, 2001.

[25] N. K. Samala, D. Radhakrishnan, and B. Izadi, "A novel deep sub-micron bus coding for low energy," *Proceedings of the International Conference on Embedded Systems and Applications*, pp. 25-30, 2004.

[26] A. R. Brahmbhatt, J. Zhang, Q. Wu, and Q. Qiu, "Low-power bus encoding using an adaptive hybrid algorithm," *Proceedings of the 43rd annual Design Automation Conference, DAC '06*, pp. 987-990, 2006.

[27] A. Acquaviva and R. Scarsi, "A spatially-adaptive bus interface for low-switching communication," *Proceedings of the 2000 International Symposium on Low Power Electronics and Design, 2000. ISLPED '00.*, pp. 238-240, 2000.

[28] K. Banerjee Mehnotra, A., "A power optimal repeater insertion methodology for global interconnects in nanometer designs," *IEEE Trans. Electron Devices*, vol. 49, pp. 2001-2007, 2002.

[29] J. C. Garcia, J. A. Montiel-Nelson, J. Sosa, and H. Navarro, "A Direct Bootstrapped CMOS Large Capacitive-Load Driver Circuit," *Design, Automation and Test in Europe. DATE'04*, vol. 1, pp. 680-681, 2004.

[30] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter variations and impact on circuits and microarchitecture," in *Proceedings of the 40th annual Design Automation Conference*, 2003, pp. 338-342.

[31] K. A. Bowman, S. G. Duvall, and J. D. Meindl, "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 2, pp. 183-190, 2002.

[32] R. Rao, "Parametric yield estimation considering leakage variability," *DAC 2004*, pp. 442-447, 2004.

[33] C. Hernandez, F. Silla, and J. Duato, "A methodology for the characterization of process variation in NoC links," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2010*, 2010, pp. 685-690.

Chapter 2

POWER REDUCTION TECHNIQUES FOR ON-CHIP SIGNALLING

2.1. Background

The trend of decreasing device size and increasing chip densities involving several hundreds of millions of transistors per chip has resulted in tremendous increase in design complexity [1,2]. Additionally this trend of reducing the feature size along with increasing the clock frequency has made reliability a huge challenge for the designers [3]. Furthermore, market forces are continually demanding devices with increased functionality/unit area; these demands have been satisfied through aggressive technology scaling which, unfortunately, has impacted adversely on the global interconnect delay subsequently reducing system performance. Subsequently, high power line drivers have been used to mitigate the problems with delay; however, these have large power consumption. The need to address these problems of global on-chip interconnect is evident from the increased interest in the development of low-power and high-speed on-chip signalling schemes. In this chapter, the different approaches and techniques used to mitigate the problems of power consumption as well as maintaining high speed signalling are briefly reviewed, pointing out their strengths and weaknesses. The review starts off with the description of the general model and the parameters associated with power consumption in digital integrated circuits. This is followed by addressing several power reduction techniques that can be divided into full-swing and low-swing signalling schemes. The full-swing signalling methods comprises bootstrapping techniques and parallelism or multiplexing techniques [4-6], while the low-swing signalling method consists of single-ended and differential signalling schemes. Subsequently, the low-swing signalling techniques will be focused on due to their capabilities of providing low power and high speed signalling with minimum area consumption and complexity. The chapter concludes with a qualitative comparison between the low-power high-speed signalling schemes.

2.2. Power Consumption In Digital Integrated Circuits

A general model of power consumption was introduced in the previous chapter. Power consumption comprises of dynamic and static power, with the dynamic power being dominant and is the result of charging and discharging of the load capacitance. Static power consumption, as previously mentioned, is caused by the leakage currents. The leakage current has increasingly become important as the technology scales down, especially at 45nm and beyond. At 45nm and beyond, the gate-oxide tunnelling leakage current becomes more dominant than the sub-threshold leakage current due to the oxide thickness. Thinner oxide will lead to high electric field across the gate oxide, even if *Vdd* is scaled lower than 0.7V. The direct consequence of thinner oxide and high electric field is an occurrence of quantum mechanical tunnelling and a sizeable current can flow from/to the gate terminal [7]. As the contributions of leakage power consumption is considered relatively small for conventional on-chip signalling, especially for 90nm technology, the power consumption can be considered to comprise mainly of the dynamic power consumption [8]. However, for low-swing signalling applications, the leakage current could be quite significant and may present drawbacks to the performance of several low-swing signalling schemes. Therefore, for this thesis, the leakage current will be considered in the analysis carried out for all the circuits designed using a 90nm technology.

2.2.1. Dynamic power consumption

Dynamic power consumption is due to capacitance charging/discharging and consumes most of the power used by *CMOS* circuits. Consider a situation where an inverter is used and the total load capacitance is represented at the output by the capacitor, C_L as shown in Figure 2.1. For the input transition from high to low, the *NMOS* pull-down network (*PDN*) is cut off and *PMOS* pull-up network (*PUN*) is activated, charging the load capacitance, C_L up to *Vdd*. This process draws energy equal to $C_L Vdd^2$ from the power supply. Half of this is dissipated immediately in the *PMOS* transistor, while the other half is stored on the load capacitance. The process is reversed as the input returns to *Vdd* and C_L is discharged, the energy of $C_L Vdd^2$ is dissipated in the *NMOS PDN*.

The derivation of the energy dissipated in the capacitor is as follows:

In a parallel plate capacitor there is a uniform electric field;

$$W = \frac{\varepsilon_o}{2} \vec{E}^2 \int_v^\infty dv^3, \tag{2.1}$$

where W is energy and $\vec{E}$ is electric field.

The volume of the plate capacitor is,

$$V = \int_v^\infty dv^3 = A.d, \tag{2.2}$$

where A is the surface area and d is the length of the plate capacitor, and the magnitude of the electric field is,

$$\vec{E} = \frac{V}{d} \tag{2.3}$$

By adding equations 2.2 and 2.3 into Eq.2.1, the equation for the energy dissipated in the capacitor is obtained,

$$W = \frac{\varepsilon_o}{2} \left(\frac{V}{d}\right)^2 A.d = \frac{1}{2} V^2 \varepsilon_o \frac{A}{d} = \frac{1}{2} CV^2, \tag{2.4}$$

where $C = {\varepsilon_o A}/{d}$.

It can be concluded that the dynamic power consumption is dependent on the switching activity of the signals, which can be defined as expected number of rising and falling transitions per data cycle. Coupled with the average data rate, *f*, which can be the clock frequency in a synchronous system, the dynamic power consumption, as shown in Equ.1.1, is proportional to the activity factor (α) which is used to model the average switching activity in the circuit, the total load capacitance (C_L), the square of the supply voltage (*Vdd*) and the switching frequency (*f*). It is important to analyze the behaviour of each component of the dynamic power consumption, i.e. *Vdd*, C_L, *f*, and α; in order to identify an effective way of obtaining the power savings.

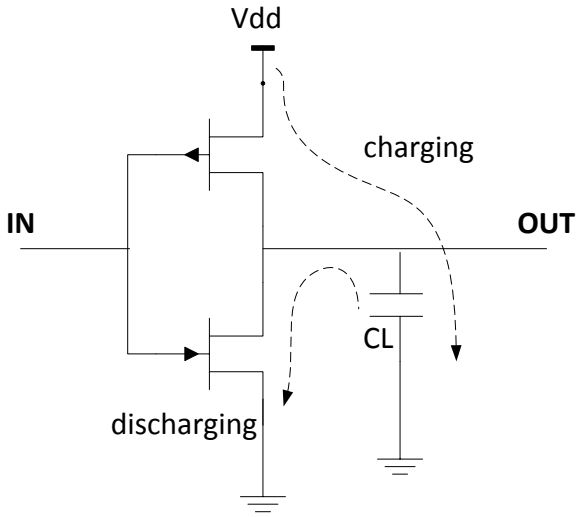


Figure 2.1: The load capacitance charging and discharging paths.

2.2.1.1. Power supply voltage, *Vdd*

Without the need of any special circuitry, voltage reduction offers the most significant means of reducing the power consumption due to its quadratic relationship to power. Unfortunately, the supply voltage cannot be reduced without affecting other performance parameters such as circuit delay, where it influences the delay negatively, leading to reduced system performance. The delay will increase linearly with the decrease in supply voltage for $Vdd >> Vth$. Large reductions in circuit speed, which accompanies the decrease in *Vdd*, can be controlled provided that the *Vdd*/*Vth* ratio is kept constant [9]. In conclusion, *Vdd* reduction is a significant means of lowering the power consumption. The other aspects that remain to be addressed are the issues of minimising the total load capacitance and activity factor in the means to reduce power consumption.

2.2.1.2. Load capacitance

The dynamic power consumption has a linear dependency on the switching of the load capacitance, which comprises the capacitances in the devices and interconnect. The device capacitances used to be larger than the interconnect parasitic capacitances but as the technology has scaled down, the interconnect capacitance has increasingly become more significant. The total load capacitance can be expressed as,

$$C_L = C_{gate} + C_{diffusion} + C_{wire} \quad (2.1)$$

The gate capacitance consists of non-linear components such as the overlap capacitances and their values depend upon the operating region. However, for power estimation of digital circuits, the gate capacitance is approximated as,

$$C_{gate} = C_{ox} W L_{eff} \tag{2.2}$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance per unit area and L_{eff} is the effective channel length.

The diffusion capacitance is made of two components; bottom-plate capacitance and side-wall junction capacitance. The nominal values of these capacitances can be found in Berkeley BSIM4 model [10].

C_{wire} is the parasitic capacitance, which is a very strong function of the geometry. For the configuration of a conductor surrounded by two adjacent wires as shown in Figure 2.2, Sakurai in [11] defines a coupling capacitance as follows:

$$C_g = \varepsilon_k \left[1.15\left(w/h\right) + 2.4\left(t/h\right)^{0.222}\right] l_e \tag{2.3}$$

$$C_c = \varepsilon_k \left[0.003\left(w/h\right) + 0.83\left(t/h\right) - 0.07\left(t/h\right)^{0.222}\right] \left(h/s\right)^{1.34} l_e \tag{2.4}$$

$$C_{wire} = C_g + 2C_c \tag{2.5}$$

where ε_k is dielectric permittivity, h is dielectric height and s is separation between two wires. C_{wire} defines a total capacitance for the middle conductor as the sum of C_g and $2C_c$ assuming that there is no signal transition on the two adjacent wires.

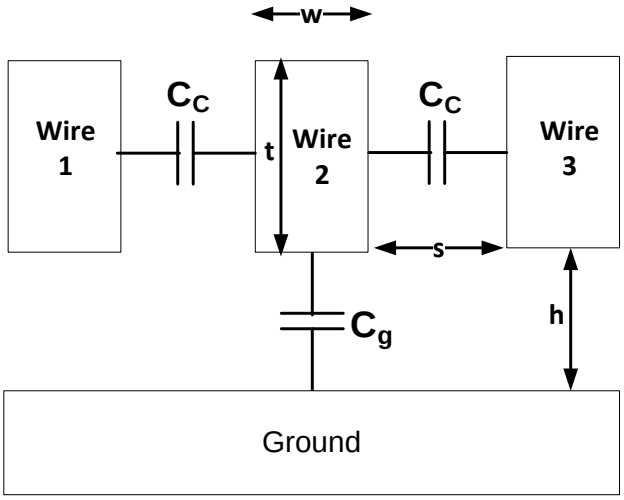


Figure 2.2: Cross-section of wire capacitance [12].

Although minimizing the load capacitance, by using smaller devices and shorter wires offers another technique to minimize power consumption [9], it has, in a similar way to supply voltage reduction, a negative effect on the circuit performance. For example, the load capacitance can be reduced by shrinking the device sizes but this unfortunately will reduce the current drive of the transistors, slowing down the circuit. This loss in performance might prevent *Vdd* from being lowered as much as possible.

2.2.1.3. Switching factor

In addition to the supply voltage and load capacitance, the switching factor also influences the dynamic power consumption. The switching factor is a combination of the activity factor, α, and the switching frequency ($s.f = \propto .f$). Zero dynamic power will be consumed if there is no switching activity. The switching factor can be interpreted as the expected number of data transitions per period clock cycle. It corresponds to the expected number of energy consuming transitions that will be triggered by the arrival of each new data. The value of the switching factor in different situations is crucial for the determination of power consumption. For example, it is known that the maximum activity of a random data signal driven for simple logic circuits is 0.4 to 0.5 [13]. For more complex circuits such as finite state machines, this tends to be lower. It can be concluded that the average switching factor may vary between 0.05 and 0.5 depending upon the situation.

Switching factor can be combined with the load capacitance to form an effective capacitance which describes the average capacitance charged during each data period. There are several techniques for reducing switching activity as a means of saving power such as algorithmic

level techniques [14,15] and multi-level logic optimization [16,17]. However, in order to have inherently lower data activity, the techniques usually employ complex arithmetic or architecture. This is a price to be paid for the reduced data activity in terms of higher physical capacitance.

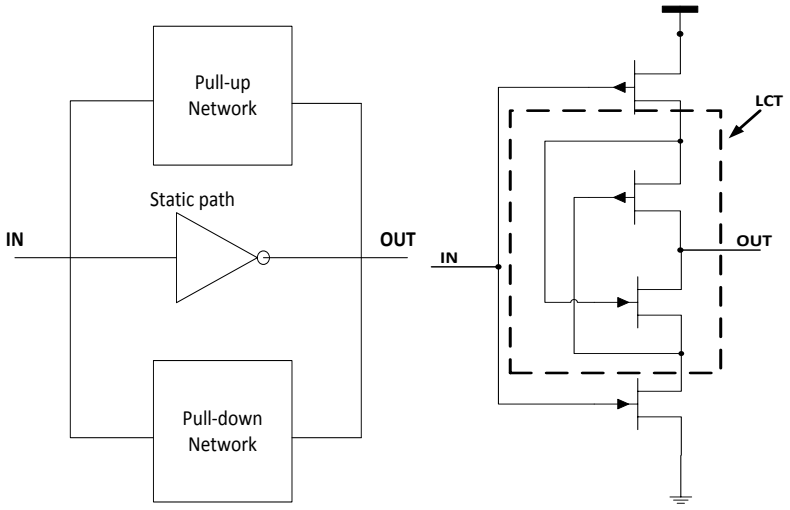
2.2.2. Leakage currents

In nanometer scaled CMOS circuits, beside the dynamic power dissipation, energy dissipation can result from various forms of leakage currents such as gate-oxide tunnelling, sub-threshold leakage and junction tunnelling leakages. For submicron technologies, the dominant leakage mechanism is the sub-threshold leakage current. However, the gate-oxide tunnelling leakage currents become adversely dominant at 45nm technologies and below [7]. Tunnelling is caused by the decrease in the gate-oxide thickness, which is needed to achieve a high current drive capability and to reduce the short-channel effects. The short-channel effect is caused by the decrease in the channel length, which leads to the increase in the depletion regions in the source and drain areas of a device. The short-channel effect produces a reduction of the threshold voltage, which also increases the sub-threshold leakage currents [8]. The circuit designs in this thesis are carried out in 90nm technology and involve using a low value of *Vdd* (*1.0V*), which also indicates a reduction in the threshold voltage accordingly to maintain good driving capabilities. As a result, the leakage current gradually becomes a limiting factor for down-scaling the threshold voltage since it determines the power consumption of a chip in an idle state. Thus at 90nm technology, it is important to consider the sub-threshold leakage current in the analysis as the device behaviour in the sub-threshold regime can be affected, directly influence on the power consumption. The gate-oxide tunnelling leakage current will be neglected in this thesis as its effect is relatively small at 90nm and even at 65nm technology.

The sub-threshold leakage is present only during the OFF state of a transistor, as it is caused by the weak inversion region in the channel for small values of the gate voltage ($V_g << V_{th}$) [18]. In order to overcome this effect, the threshold voltage has been kept high, approximately above 0.5V. However, as technologies are scaled further down into the sub-nanometer regions, maintaining a relatively high threshold voltage has become challenging.

There have been, for example in a driver circuit, several methods adopted to overcome the problems associated with leakage currents such as creating a direct static path between the

input and output of the driver [19], or implementing leakage control transistor (*LCT*) [20]. In order to cancel out the leakage current effects and improve the noise immunity a low speed static path is created, as shown in Figure 2.3(a), which can be as small as a minimum sized inverter. This path is used when the input is stable and there is no transition activity.



(a) (b)

Figure 2.3: The architecture of leakage reduction mechanism: (a) static path [19] and (b) leakage control transistor [20].

Implementation of the LCT method is usually applied to low voltage drivers which accommodate more than one path for the signal propagation during the transition activity. The leakage control transistor, as shown in Figure 2.3(b), is created by the controller in the gate terminal of one transistor by the source of the other. For any input combination, one of the leakage control transistors is always near the cut-off voltage which consequently increases the resistance of the path from *Vdd* to ground, subsequently leading to a decrease in the sub-threshold leakage currents. Both of these methods will be considered in the design of the proposed low-swing signalling scheme for this work, which will be discussed in the next chapter.

2.3. Low Power CMOS Circuits

Power consumption has emerged as a very significant design parameter. Aggressive market driven demands and technology-related limitations have steered researchers to try to invent new design techniques and methodologies to confront the power requirements. In a given *CMOS* technology, in order to achieve a high throughput, more power is consumed due to

proportional relations between the dynamic power dissipation and the switching activity. Thus, conventional *CMOS* signalling such as shown in Figure 2.4 is no longer applicable for on-chip applications. The driver and receiver circuits are both conventional *CMOS* inverters [21]. Conventional *CMOS* signalling reduces the power consumption by reducing the power supply but resulting in circuit speed reduction. Both low power consumption and high speed signalling can be achieved if highly efficient logic circuits with low power-delay-products are implemented. Several low-power high-speed signalling schemes, which have been proposed in the past, will be discussed next. They are divided into two categories, namely, full-swing and low-swing signalling schemes.

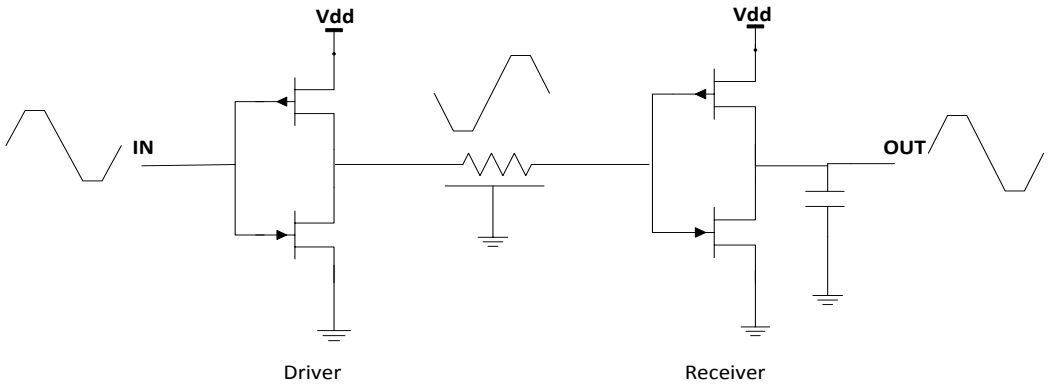


Figure 2.4: The conventional *CMOS* signalling scheme [21].

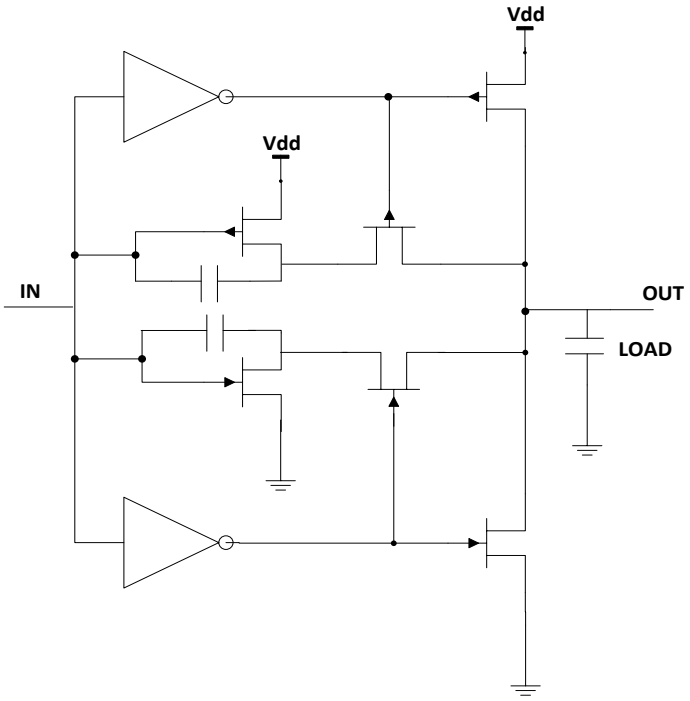
2.3.1. Full-swing on-chip signalling schemes

Two examples of the full-swing signalling schemes are the bootstrapping techniques, which enhance the driving capability of the driver circuits and reduces the power consumption; and the parallelism techniques which incorporate a multiplexing transmitter that reduces the clock load of the pre-amplifier and driver stages, which reduces the power consumption and provides speed improvement.

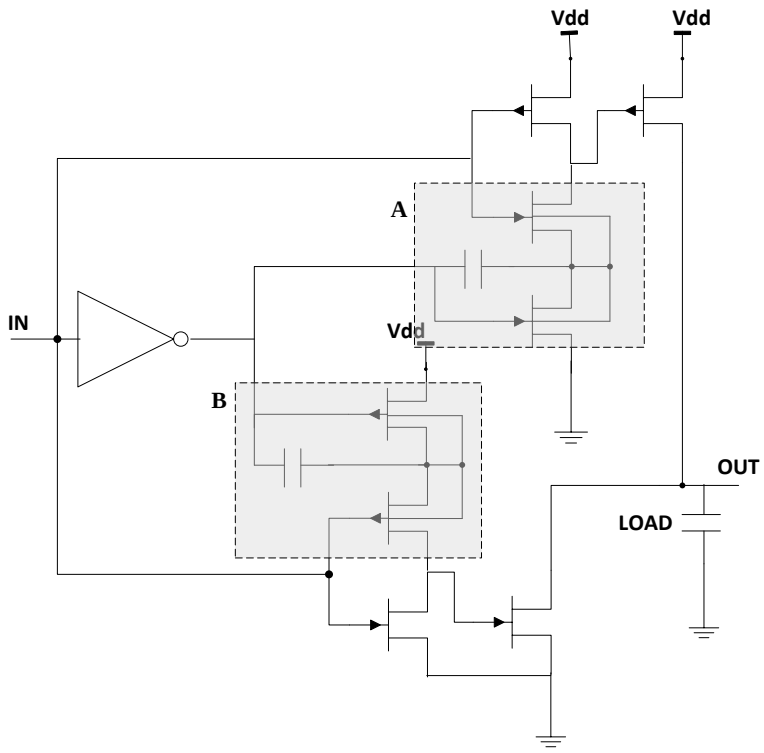
2.3.1.1. The bootstrapping techniques

Bootstrapping techniques can be used in the low voltage *CMOS* dynamic and static logic circuits to enhance speed performance for system-on-chip applications. The techniques are used in a *CMOS* large-load full-swing driver which exploits capacitive coupling to drive a dynamic node to a voltage that exceeds the power supply. Bootstrapping techniques can be divided into two categories, which are direct and indirect methods shown in Figure 2.5. In the direct method extra capacitors are directly connected between the input and output of the

driver through the pass transistors [22,23], whilst in the indirect method two extra capacitors are connected to the gates of the devices (*A and B*) at the output stage of the driver to improve the device driving capability during the switching transition [24]. However since the threshold voltage of the *CMOS* devices do not scale down with the same factor as the power supply, the indirect techniques are not very effective in driving the large capacitive loads. The direct methods, on other hand, directly apply the bootstrapping capacitors to the output node, thereby improving the driver speed.



(a)



(b)

Figure 2.5: The architectures of (a) direct and (b) indirect bootstrapping techniques [19].

Several line drivers that employ direct bootstrapping techniques sometimes use two bootstrapped capacitors. For example, a driver logic circuit such as the M-driver [23] which consists of three stages, namely, the controlling signal circuit, positive and negative pumping circuit and the driving circuit, requires two bootstrap capacitors for low-to-high and high-to-low transitions. Another direct bootstrapping circuit which also requires two capacitors for successful transitions is the *CMOS* bootstrapped dynamic logic circuit (*BDL*) [25]. The BDL circuit comprises a dynamic logic circuit and a bootstrapped circuit, where two bootstrapped capacitors are used for its two periods of operations, that is pre-charge and logic evaluation.

Both the M and BDL driver circuits have improvements in terms of speed, power and active area over other dynamic bootstrapping driver circuits such as the D-driver [22], which requires access to the bulk nodes of *PMOS* and *NMOS* devices. However, both drivers employ two bootstrap capacitors which add to the complexity of the overall circuits due to the increase in the power consumption and area overhead. This is overcome by the F-driver [26], which requires only one bootstrap capacitor to achieve bootstrapping for both switching transitions, resulting in lower area and power consumption.

The main problem with the bootstrapping technique is its tendency to overshoot and undershoot the voltage signal. If the voltage across a device exceeds the power supply by

more than a small amount, permanent damage may occur [19], which is why this technique is seldom used. Even though the enhanced driving capability greatly improves speed performance of a driver circuit its full swing signalling capability and the use of bootstrap capacitor, which can be as large as the internal load capacitance of the driver circuit, results in significant increase in power consumption.

2.3.1.2. The parallelism or multiplexing techniques

The parallelism technique is a technology independent technique which reduces power consumption and maintains the throughput of logic blocks and processors by decreasing the operating frequency and supply voltage [27,28]. At a reduced *Vdd*, this method is used to maintain the throughput of logic devices that are placed on the critical path. Parallelism as shown in Figure 2.6 accommodates *M* parallel units which are clocked at *f/M*. Each unit can compute its results in a time slot *M* times longer and can therefore be supplied at a reduced supply voltage.

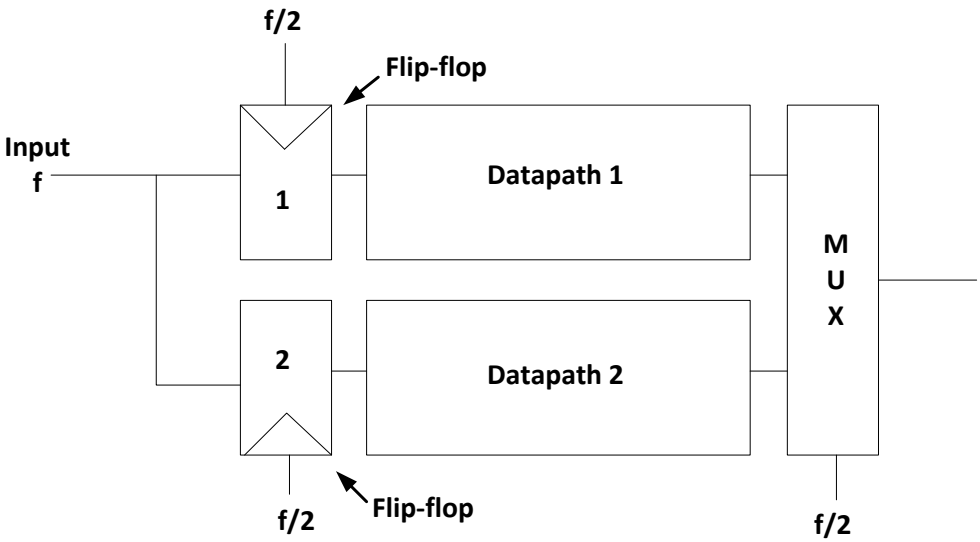


Figure 2.6: The architecture of parallelism technique [8].

Multiple instances are needed if the units used are datapaths or processors which results in an *M* times area increase and switching capacitance. However, if the units used consist of smaller transistors and the operating frequency is reduced, a power reduction can be achieved. In addition, some parallelized logic units do not require M-unit replication such as memories. In parallelized memories, each unit contains *1/M* bits of data or instruction, resulting in the same total area to store the information and the same total switching capacitance. Parallelized circuits such as memories, shift registers and serial-parallel

converters are a few examples that accommodate parallelism at low *Vdd* and incurring a small overhead [29].

The parallelism technique can be applied to on-chip signalling schemes through the use of transceivers. Parallelism in transceivers obviates the need for high frequency clocks to achieve high bit-rates [30,31]. High bit-rates can be supported while both transmitter and receiver operate at a lower frequency. The technique comprises multiple transmitters connected in parallel converting low frequency parallel data streams into a single high frequency stream on the channel through a multiplexer. The parallel receivers will then convert the high frequency data stream back to the low frequency parallel data streams [31]. The parallelism technique lowers the clock frequency needed to support a certain bit-rate and thus provides opportunities for saving power. This is mainly due to the voltage being adaptively scaled down for the lower clock frequency. However, without the voltage scaling, the power reduction cannot be achieved because the power reduction due to the lower frequency is cancelled by the increased switched capacitance.

The parallelism technique with multiplexed transceivers can be divided into two categories, namely, the output and input multiplexed transmitters. The output multiplexed transmitter proposed by Yang [30] has multiple drivers connected in parallel with each driver consisting of two *PMOS* transistors in series, as shown in Figure 2.7. Each driver is only active when the inputs, namely *dclk(n)* and *qclk(n)*, are low. The inputs are aligned with the clock phases that are one phase apart, $\Phi(n)$ and $\Phi(n+1)$. The pre-driver shown in Figure 2.7 controls the input clock frequency depending on the data being transmitted to match the delays between the two inputs. However, there are factors that limit the potential of this driver circuit which is mostly *Vth*-related problems. Increased driver sizing is necessary to support the desired swing at low *Vdd* as *Vdd* approaches *Vth*. However, this reduces the power savings benefits of low voltage operation since increasing the driver size means higher driver current, thus increase in power. In addition, lower *Vdd* will result in a narrower pulse width at the output [30].

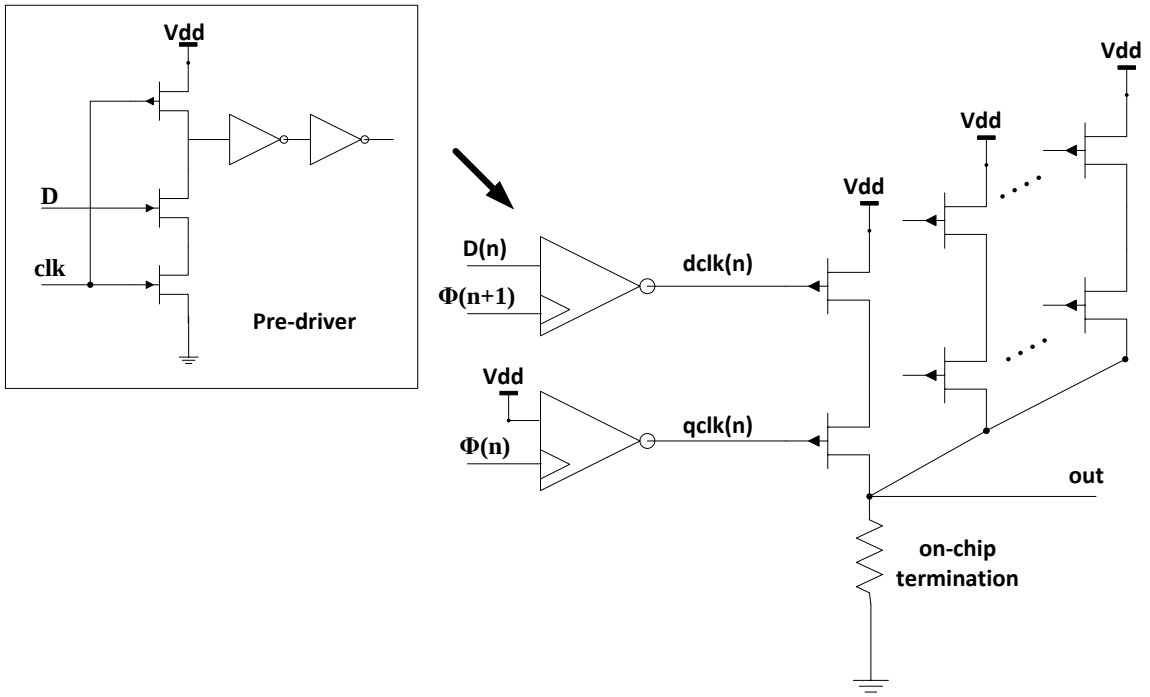


Figure 2.7: The output multiplexed transmitter by Yang et al [30].

Alternatively, the problems with the output multiplexed transmitter shown in Figure 2.7 can be solved by implementing the multiplexed transmitter with the level shifting pre-driver circuit [32]. The level-shifting pre-driver shown in Figure 2.8, shifts the voltage level of input driver down by *Vth* so that the *PMOS* driver inputs swing between *–Vth* and *V-Vth* which subsequently mitigates the previous driver's problem with *Vdd* as the *PMOS* driver behaves as if its *Vth* is 0. In addition, this driver is less sensitive to supply voltage variation because the turn-on and turn-off points of the driver are now independent of *Vdd* [32]. However, the power savings benefit might be compromised by the need for negative pulse generator to assist the *PMOS* driver in switching down to *–Vth* for full output swing. Power saving is achieved with increased data rates without increasing the size of the driver but instead requires additional circuitry, i.e. the negative pulse generator. The power savings benefit of the output multiplexed transmitter scheme with level-shifting pre-driver circuit is significantly affected as the negative pulse generator is required for each driver at every data stream input. Subsequently, this also results in the silicon area overhead.

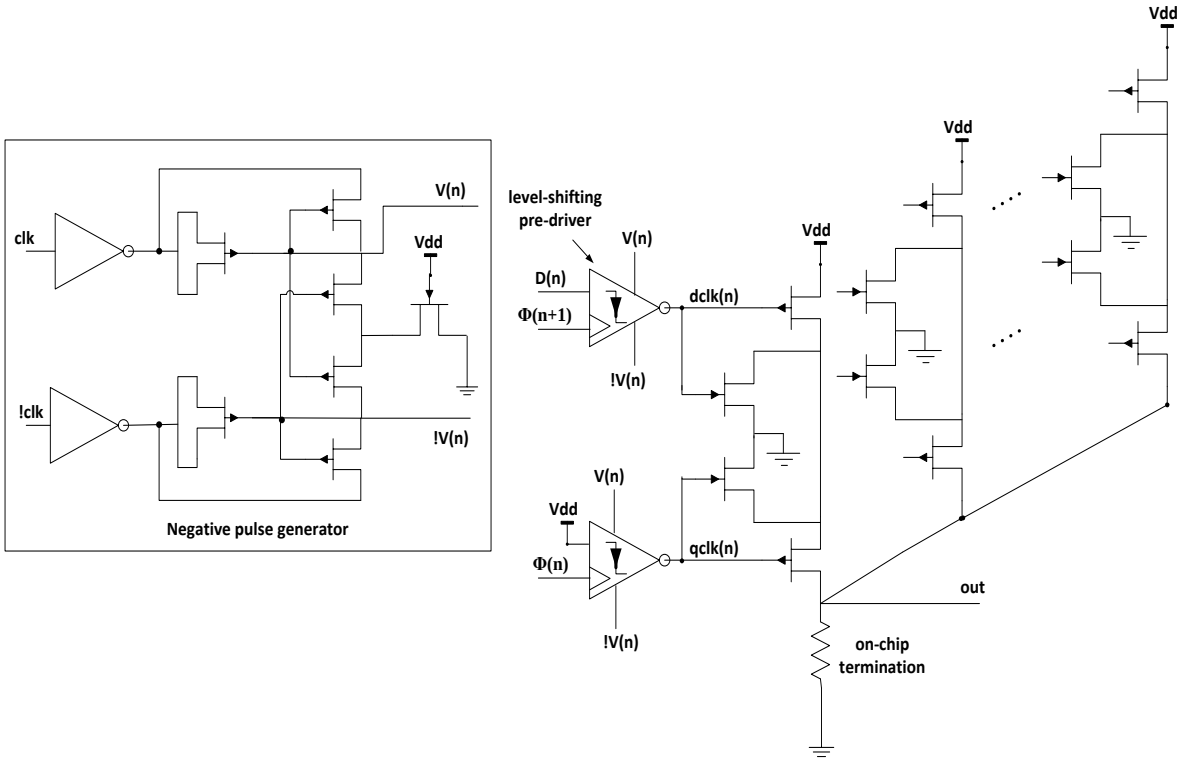


Figure 2.8: The output multiplexed transmitter with level-shifting [32].

The input multiplexed transmitters shown in Figure 2.9 [33] provides speed improvement over the output multiplexed architecture as well as significantly lower power and area overheads. The input multiplexed transmitter reduces the clock load by a significant amount by multiplexing signals before amplification. It also reduces area by requiring only a single copy of the output driver rather than one copy for each multiplexer input. The transmitter comprises a dual pseudo-NMOS multiplexer, a pre-amplifier and an output driver, and also employs a delay-locked loop circuit with regulated supply voltage, which further reduces the power consumption as well as achieving better supply noise rejection [33].

The main problem with the parallelism or multiplexing technique is its stringent matching requirement among the parallel components to avoid degradation of signal quality. To add to its complexity, each multiplexed transmitter is required for every data stream input which may include additional circuitry such as level shifter as in [32]. This leads to increase in power consumption and silicon area overhead. Even though input multiplexed transmitter has several advantages over the output multiplexed transmitter in terms of power, area and speed, its characteristic of having a full swing signalling capability, which is like the bootstrapped techniques, results in the increase in power consumption. In addition, the power saving of the parallelism or multiplexing techniques are strongly dependent on the voltage scaling.

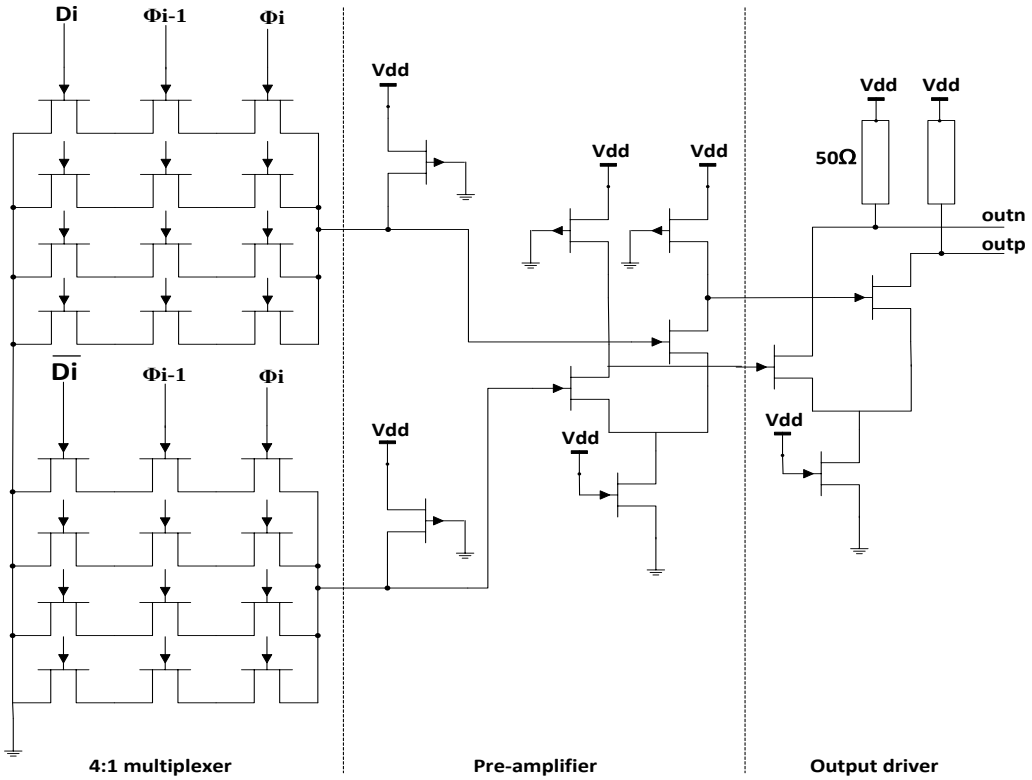


Figure 2.9: The input multiplexed transmitter [33].

Compared to the full-swing signalling schemes such as the bootstrapping technique and the parallelism technique, there are several low-power high-speed on-chip signalling schemes which have better power-delay performance; these are the low-swing on-chip signalling schemes, which will be discussed in the next section.

2.3.2. Low-swing on-chip signalling schemes

This technique aims at power reduction on a large load capacitance through the use of reduced voltage swing on the interconnections. With the load capacitance, operating frequency and supply voltage remain unchanged, on-chip lower power consumption can be achieved using specially designed circuits. These circuits which are placed at each end of the interconnection are used to convert the full rail-to-rail swing to low voltage swing, and vice versa.

In this thesis, the main focus is reducing the power consumption of on-chip interconnects while maintaining the circuit performance. One of the best solutions toward achieving better energy efficiency is by reducing the voltage swing of the signal on the interconnect. Low swing drivers can accommodate either a single-ended or differential signalling schemes. In single-ended signalling, the receiver detects an absolute change in voltage in a single wire

while the receiver detects a relative difference in voltage between two wires in differential signalling. Several low swing signalling schemes such as those that employ multiple voltage supplies, reference voltages, bootstrapping, charge sharing, differential voltage mode, driver pre-emphasis, current mode techniques and diode-connected configuration will be now discussed, highlighting the mechanism, the advantages and disadvantages of each scheme.

2.3.2.1. Multiple voltage techniques

There are two main categories of multiple voltage techniques that is the multi-*Vdd* technique and multi-*Vth* technique. Both methods have the same concept where high supply voltage or high threshold voltage is applied to the critical gates while the rest of the circuits is connected to a lower supply voltage or has transistors with lower threshold voltages.

The multi-*Vdd* technique can be referred as clustered voltage scaling. The circuit is partitioned so that the non-critical gates run at Vdd_L and only critical gates use Vdd_H. the multi-*Vdd* technique is usually applied to effectively reduce power consumption without degrading the operating speed. However, level converters should be inserted to prevent a large static current flow to the low-to-high conversion. A good example of the multi-*Vdd* technique is the conventional low-swing signalling scheme shown in Figure 2.10, which employs both Vdd_L and Vdd_H at the driver and the receiver. Several low-swing circuits that employ multi-*Vdd* technique focus on the effective design of the level converter such as the level converter using pass transistor half latch [34], the *PMOS* cross-coupled level converter [35] and the single supply diode voltage limited level converter [36]. The effective design of the level converter at the receiver end is very important as the performance of the driver circuit is solely dependent on it.

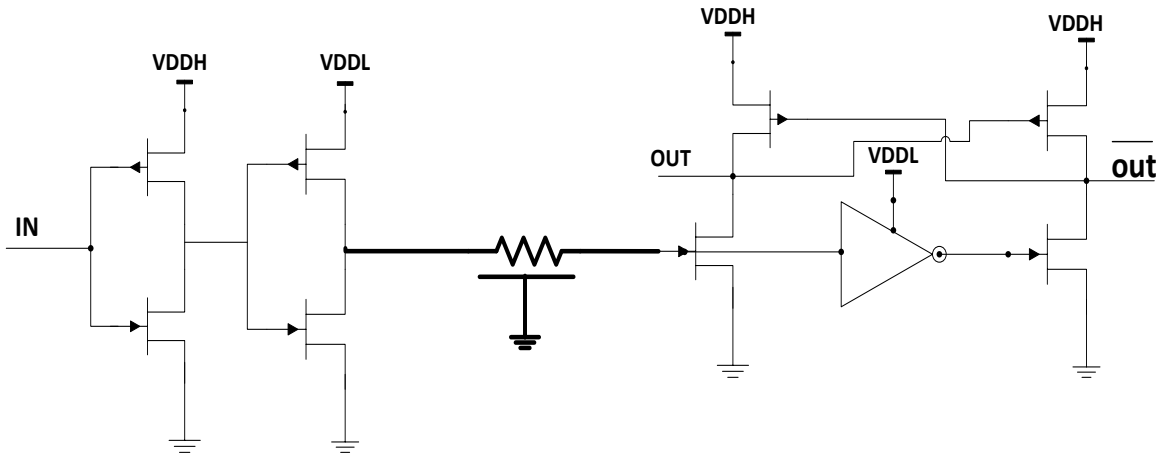
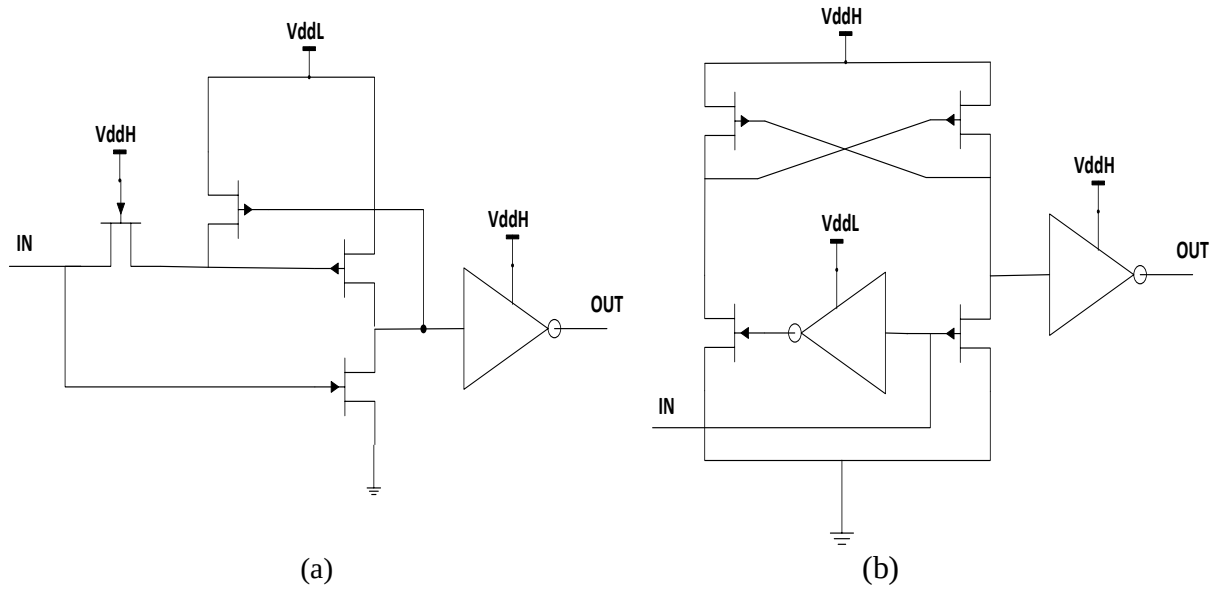


Figure 2.10: The conventional low-swing signalling scheme [37].

Similar to other low-swing signalling schemes, the level converter shown in Figure 2.11(a) using pass transistor half latch provides low power and high speed but since it requires Vdd_L and Vdd_H , the placement and routing are difficult in physical designs [34]. The *PMOS* cross-coupled level converter as shown in Figure 2.11(b) suffers from the same problems regarding the placement and routing which is solved by the single supply diode voltage limited level converter. The placement and routing is made easier by using a single *Vdd* at the level converter [36]. However this technique does not have the best performance compared to the first two techniques, namely the conventional low-swing signalling scheme shown in Figure 2.10, and the low-swing multiple *Vdd* signalling schemes with pass transistor half latch as in Figure 2.11(a).

The main issue with the multi-*Vdd* technique is the timing analysis and layout placement. With a single power supply, timing analysis is simpler as it can be performed for single performance point based on a characterized library. However for multiple power supplies, the timing analysis has to be performed separately for each *Vdd*, making it more complex. In addition, both low and high *Vdd* cells need to be separated because they have different n-well voltages [38], which increase the complexity of the circuit.



(a) (b)

Figure 2.11: The low-swing multiple *Vdd* signalling schemes with (a) pass transistor half latch [34] and (b) PMOS cross-coupled level converter [35].

Another issue with the multi-*Vdd* technique is the increase in static current, which is caused by not feeding the output of the low *Vdd* gates directly to the high *Vdd* gates because the output can never be raised higher than low *Vdd* [38]. Even if the output of low *Vdd* gates is connected to the high *Vdd* circuit, the static current still flows due to the *PMOS* in the high

Vdd circuit never being completely cut-off. A possible solution to the static current problem is to place a level converter between high and low *Vdd* gates. However, this may result in the increase in area and power. The multi-*Vth* technique can overcome the problem with static power consumption.

The multi-*Vth* technique accommodates both high threshold and low threshold transistors in the driver circuit to significantly improve the power delay product through reduced output swing level voltage. A cross-coupled latch is usually used as the receiver which re-converts the reduced swing to a full swing [21]. An example of a line driver circuit employing the multi-*Vth* technique, shown in Figure 2.12, is the Up-Down Low-Swing voltage driver scheme, which accommodates both the low *Vth* and high *Vth* transistors at the driver and the receiver circuits. This architecture is similar to the multi-*Vdd* driver scheme.

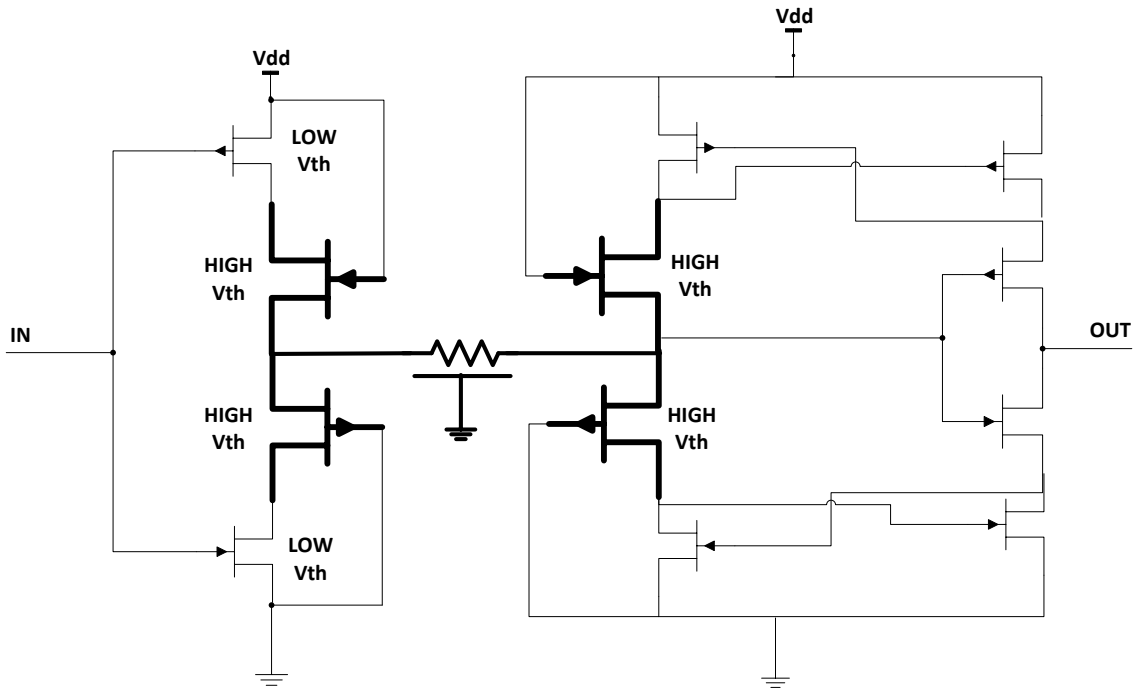


Figure 2.12: Up-Down low-swing voltage driver (*UDLD*) [21].

Unlike the multi-*Vdd* technique which suffers from increased static current, the multi-*Vth* technique is usually used to reduce the static power. If the multi-*Vdd* technique is combined with the multi-*Vth* technique, both the static and dynamic consumption can be reduced [39]. However, the problems regarding placement and routing with the multi-*Vdd* techniques, also apply to the multi-*Vth* technique as two different *Vth* values are used which requires two different technology libraries. Therefore, if both techniques are implemented, the power

savings achieved by these techniques seem insignificant compared to the increase complexity of their physical designs.

2.3.2.2. Static source driver scheme

The static source driver signalling schemes discussed here are the low-swing single-ended voltage mode (*VM*) signalling schemes with the static source driver. The static source drivers are useful for global on-chip signalling as they provide fast signalling. They also provide low power consumption on the interconnect through reduced voltage swing. The first example of the static source driver is the conventional low-swing signalling driver shown previously in Figure 2.10. The conventional low-swing signalling scheme employs a static source driver with two power supplies, Vdd_H and Vdd_L to provide low swing voltage on the interconnect. Even though the signalling scheme provides a low-power and high-speed signalling, the use of multiple power supplies increases the complexity of the circuit.

Another example of the static-source driver scheme that incorporates multiple reference voltages is the symmetric driver and level converter (*SDLC*) shown in Figure 2.13, which comprises a static source-offset driver and a symmetric level converter. The source-offset driver in [40] has a configuration of a *CMOS* inverter. The differences are that the driver operates with the internal supply voltages, *Vsl* and *Vcl*, and the threshold voltages of the *MOSFET*s are lowered so that $\Delta V_{thn} = V_{sl}$ and $\Delta V_{thp} = V_{dd} - V_{sl}$. This way the effective gate voltages are the same as the conventional *CMOS* inverter operating at *Vdd* [40].

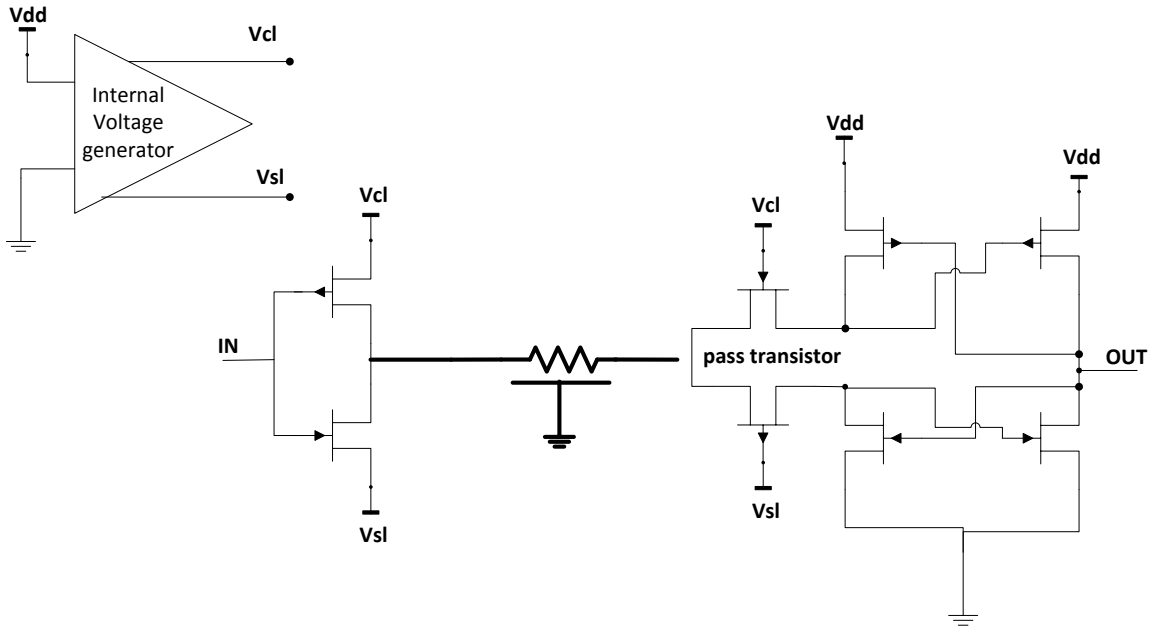


Figure 2.13: The symmetric driver and level converter scheme [40].

The receiver for the SDLC circuit has a similar configuration to the conventional low-swing signalling scheme except that a pair of pass transistors is added and the internal inverter is replaced by the *CMOS* crossed-coupled latch. Two internal supply voltages are used instead of multiple *Vdd*, which are applied to the gates of the pair of pass transistors. The internal supply voltages originate from the internal voltage generator at the driver side. Therefore the earlier problem with the layout placement with conventional low-swing signalling using multiple voltage supplies is mitigated. However, by using low voltage supplies to obtain reduced voltage swing, the driver consumes a significant amount of driving current. This is overcome by using low-*Vth* devices to achieve the required level of voltage swing. However, the use of the internal voltage generator which provides the two extra power rails contributes to the complexity of the scheme as it introduces additional routing to the scheme.

The main issues with the previous method are the use of extra power rails and low-*Vth* devices. The static source driver to be mentioned next, overcomes this problem by utilizing the threshold voltage drop of source followers, and is known as the static source driver level converter (*SSDLC*) signalling scheme. The output of the source-follower in the SSDLC scheme, shown in Figure 2.14 tracks the threshold voltage drop of the input, simplifying the way to limit the interconnect swing without the use of extra reference voltages or circuitry. The source-follower driver also provides a high impedance input and fast signalling. The source-follower is usually used as a level shifter or a buffer to drive large capacitive loads. In this configuration, the driver limits the interconnect swing from |*Vthp*| to *Vdd*-*Vthn* or approximately two threshold values below *Vdd*.

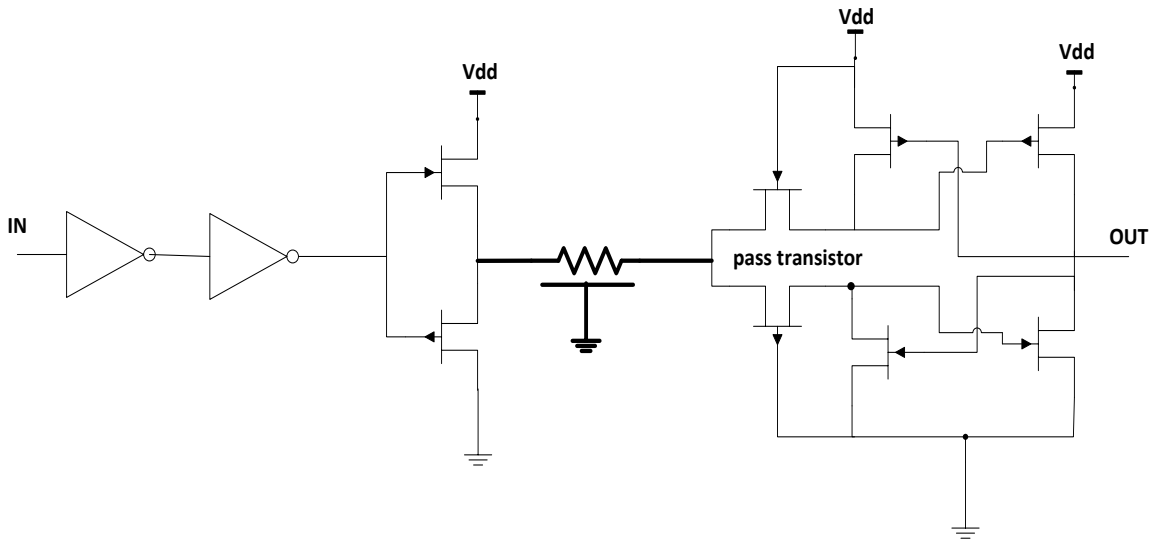


Figure 2.14: The symmetric source driver level converter (*SSDLC*) scheme [37].

The receiver for the SSDLC scheme is similar to the receiver in the SDLC scheme except that the gates of the two pass transistors are biased at *Vdd* and ground respectively. Low-*Vth* devices are not required for this driver scheme due to the characteristic of the source follower. However, as stated in [37], the driver scheme requires a large *Vdd*, greater than *2.8V*, to generate a reasonable voltage swing on the interconnect. This may be the reason why its energy-delay product is almost the same as the conventional low-swing signalling scheme [37]. The advantage that the SSDLC scheme has over the conventional low-swing signalling and other static source driver schemes is improvements in terms of delay and complexity but lacks in the aspect of power saving, which is essential for on-chip signalling applications.

In conclusion, the static source driver scheme is strongly dependent on the level conversion circuitry of the receiver for successful signalling, and most of the driver schemes such as the conventional low-swing signalling and the SDLC schemes require extra power rails or multiple power supplies. Even if multiple power supplies or extra power rails are not used, a relatively large *Vdd* is needed to successfully operate as in the SSDLC scheme.

2.3.2.3. *NMOS* only push-pull driver scheme

The previous two schemes, the SSDLC and ASDLC only manage to provide linear energy reductions since both schemes use standard *Vdd*. An *NMOS* only push-pull driver scheme is an improvement over the source-follower driver scheme in terms of power consumption. The driver scheme does not require any extra power supplies nor implementation of multiple voltage techniques but instead employs a voltage reference to drive the interconnect with reduced swing. The voltage reference could be as low as *0.7V*. Similar to the static source driver scheme, the driver is dependent on the level conversion circuitry of the receiver. The basic structure of the *NMOS* only push-pull driver scheme is shown in Figure 2.15, accommodating differential sense amplifier at the receiver side.

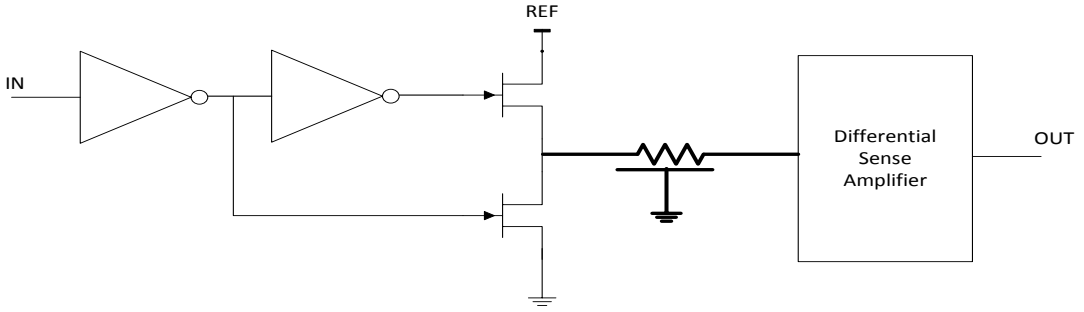


Figure 2.15: *NMOS* only push-pull driver scheme [37].

Several *NMOS* only push-pull driver schemes with different receiver designs [37] will be discussed here. There are four types of level converter used with the *NMOS* only push-pull driver. One of the level converters uses low-*Vth* devices, while another implements a coupling capacitor. There are also level converters that rely on extra timing signals to successfully retrieve the original signal.

The level converter with low-*Vth* devices is similar to the level converter in the conventional low-swing signalling scheme except that, as the name suggests, uses low-Vth devices. The reference voltage is also applied to the level converter which is set to *0.7V* and the *Vthn* and |*Vthp*| of the low-*Vth* devices are set at *0.3V* [37]. The internal inverter in the level converter regenerates a complementary input signal internally, turning the level converter into a differential sense amplifier. The use of low-*Vth* devices will cause excessive leakage currents but since the low-*Vth* devices in this scheme are sized smaller than the driver, it is negligible compared to the total switching power of the driver scheme. In addition, the low-*Vth* devices are essential for this scheme as they help in turning on the *NMOS* or turning off the *PMOS* devices at the receiver output.

Another level converter design for this driver scheme implements a capacitive coupling as an alternative to the low-*Vth* devices. The coupling capacitor is used to boost the low swing signal in order to turn on the *NMOS* transistor at the receiver output. Similar to the previous level converter, a voltage reference is also used for this scheme except that two voltage references are used instead which are set at *0.8V* and *1.2V*. The concept of charge sharing is introduced between the coupling capacitor and the parasitic capacitances. This however requires the coupling capacitor to be large enough for the charge sharing to work. The coupling capacitor is also used to convert a very low swing to a full swing using a bootstrapping technique. By using the coupled capacitance, low-*Vth* devices and extra timing signals are not needed. The level converter is also sensitive [37] to the device variations, especially the uncertainty in *Vth* as it can affect the small noise margin.

Examples of the level converter for the *NMOS* only push-pull driver scheme that use extra timing signals for the receivers to detect the low swing signal more effectively are the level-converting register (*LCR*) and pseudo-differential interconnect (*PDIFF*) schemes. The LCR scheme shown in Figure 2.16 comprises of a cross-coupled inverter pair with one pre-charge transistor and one pass transistor whose gates are controlled by two timing signals, i.e. *PRE* and *EVAL* respectively [37]. The LCR scheme consumes little area overhead but the use of

extra timing signals increases the complexity of the circuit. In addition, the matching of the current drive capabilities at the input of the receiver is sensitive to the receiver's noise margin which is susceptible to supply noise and *Vth* variations. The LCR provides fast signalling only if the *EVAL* signal is applied after the input of the receiver reaches the stable point. The *NMOS* only push-pull driver scheme with LCR is too dependent on the timing signals for reliable operation.

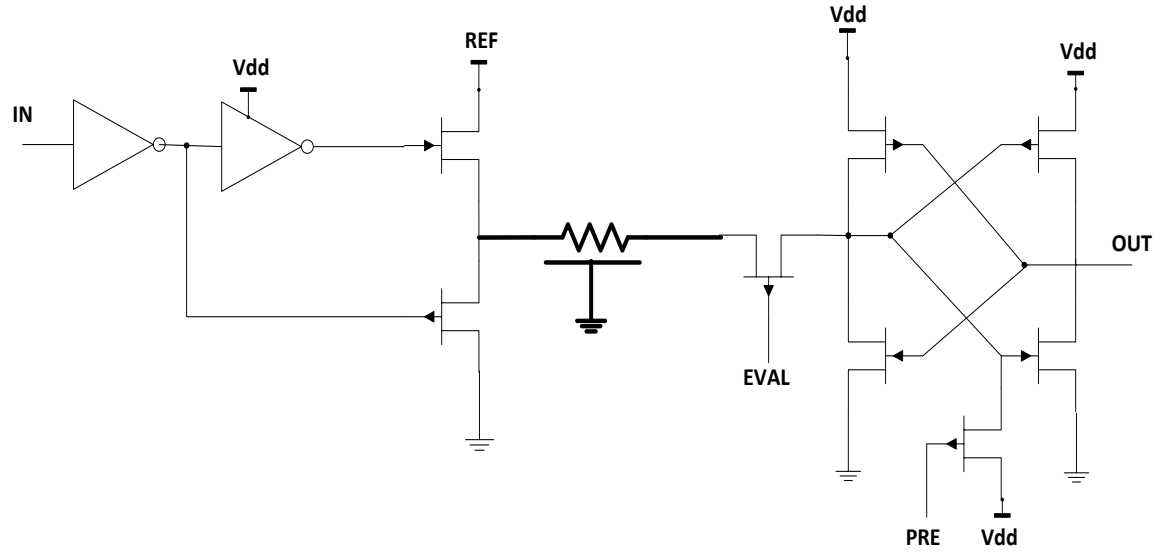


Figure 2.16: The level-converting register (*LCR*) [37].

The pseudo-differential interconnect scheme [37] is a level converter which also requires extra timing signals. The receiver comprises a clocked sense amplifier followed by a static flip flop. Similar to the LCR scheme, one voltage reference is used. The usage of a single wire per bit improves the reliability of this scheme in the aspect of the input offset and circuit sensitivity. However, there is a possible mismatch between the different voltage references of the driver and receiver which contributes to some reliability degradation.

Although the *NMOS* only push-pull driver schemes provides a significant improvement in the energy-delay product compared to the static source driver schemes, the schemes are still susceptible to supply noise and device variations. In addition, the use of reference voltages and extra timing signals increase the complexity of the schemes.

2.3.2.4. Charge sharing bus

The charge sharing technique has been mentioned previously in the *NMOS* only push-pull driver scheme where its voltage level converter utilizes this technique in the coupling

capacitor for reliable level conversion. The charge sharing technique can also be applied to the differential signalling scheme. The technique is also often used between two bus wires to reduce the voltage swing using either a charge inter-shared bus [41] or charge recycling bus [42-44] schemes.

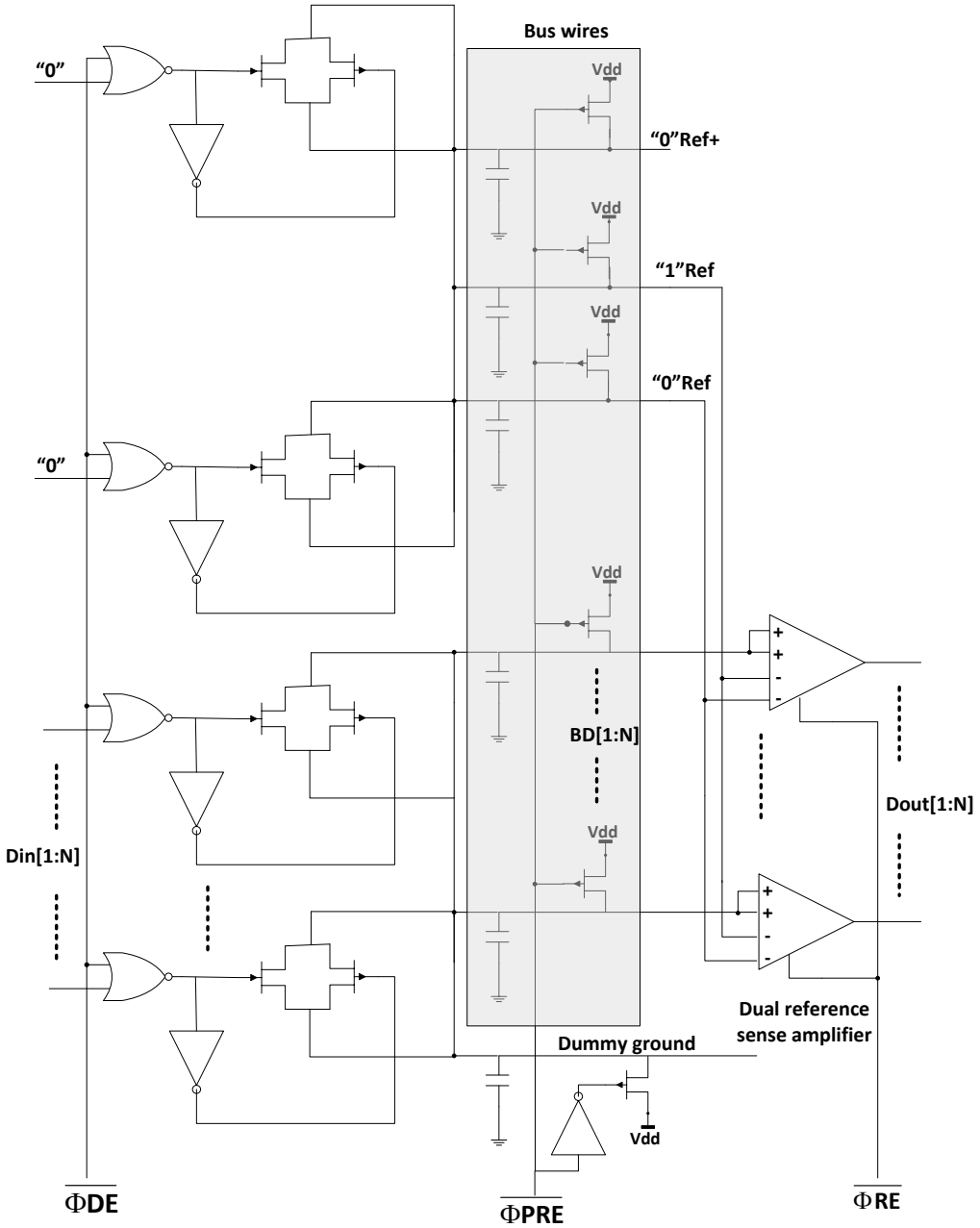


Figure 2.17: The charge inter-shared bus (*CISB*) scheme [41].

An example of the charge inter-shared bus scheme is the CISB shown in Figure 2.17, which is a reduced swing internal bus architecture achieving low power operation with no *DC* power consumption within any of the bus architecture [41]. The reduced swing is obtained by charge sharing between the bus wires and an additional bus wire, referred to as dummy

ground. The dummy ground is initially discharged to the real ground value and then immediately isolated from the ground, followed by the bus wires being discharged to the dummy ground instead of the real ground [41].

Noise could be significant due to the reduced swing but this can be overcome by implementing a differential amplifying scheme at the receiver end. The differential amplifier requires two reference voltages and extra timing signals to operate the dummy ground. Although the differential amplifier at the receiver is useful in overcoming the noise problems, the potential saving of this scheme is also compromised by the use of reference voltages and extra timing signals. Subsequently, the use of reference voltages and extra timing signals increase the complexity of the scheme. The cell area is almost double the cell area of conventional bus scheme due to the increased number of logic gates in the bus driver as well as the receiver.

All charge stored at the output node of a typical *CMOS* circuit is dumped to the ground when the output state changes. A charge recycling circuit can reuse the charge from the previous cycles to reduce the power associated with the nodes involved in charge recycling by half [42]. An example of a charge recycling bus scheme is the low-swing charge recycling (*LSCR*) scheme which uses differential pass transistor logic, as shown in Figure 2.18. The LSCR scheme is used for low-power silicon-on-insulator (*SOI*) applications because in SOI the charge recycling bus scheme is less affected by the body effect and *Vth* variations when the source and drain voltages are raised [43], whilst leading to faster speed since lower *Vthn* in the pass transistor chain speeds up the circuit. Low power consumption is expected but the potential savings are compromised due to the transient leakage current during the clock transition, which is caused by the charge recycling mechanism. In addition, the complexity of the circuit is increased due to the use of clocked latched sense amplifier and differential signalling.

Overall, the main issue of charge sharing bus schemes, whether they are charge inter-shared or charge recycled techniques, is still related to the complexity of the circuit. However as stated in [44], the power savings of the charge sharing bus scheme is more beneficial if it is applied to larger buses applications, where extra timing signals and reference voltages are tolerable.

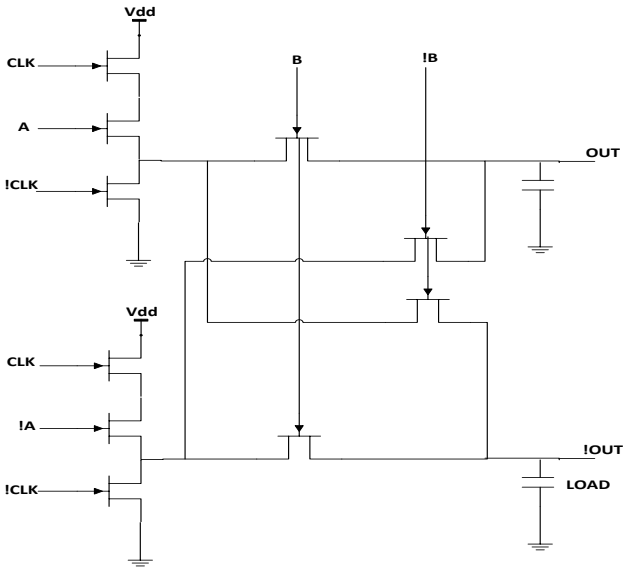
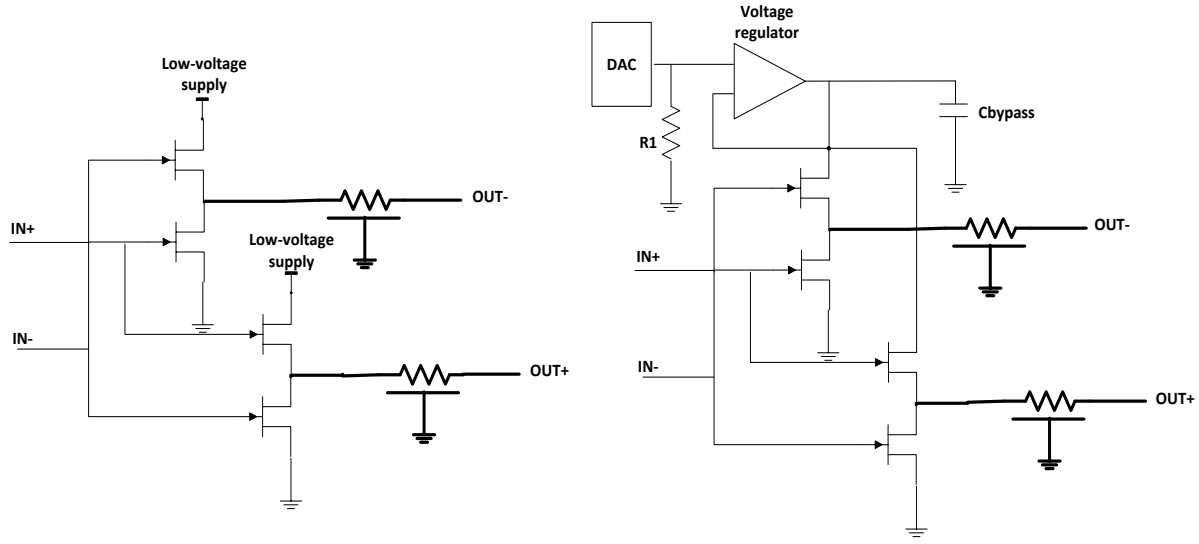


Figure 2.18: Low-swing charge recycling (*LSCR*) scheme [43].

2.3.2.5. Differential voltage mode signalling scheme

The previous low-swing signalling techniques with the exception of the charge sharing bus, implement a single-ended signalling scheme. There are several on-chip signalling schemes that use differential signalling taking advantage of their high noise immunity characteristic. The differential signalling techniques can be implemented in current mode (*CM*) and voltage mode (*VM*) signalling schemes. The difference between CM and VM signalling is that the signal produced on the transmission lines in VM uses the voltage as a signal while CM uses the current. In addition, a VM receiver presents a high impedance capacitive termination [45] while a low impedance termination is presented at the CM receiver which results in reduced signal swing and increased bandwidth.

Differential VM signalling is able to further reduce the signal swing at a very low *Vdd* as used in the low-swing signalling scheme in [46]. The proposed drivers in [46] consume less current and introduce ac-coupling without modifying the design compared to the current-mode drivers. An example of this driver scheme is a voltage mode driver with a low *Vdd*, as shown in Figure 2.19(a), which comprises of two *NMOS* transistors as pull-up and pull-down networks. However this configuration of the driver scheme requires additional external low voltage supply to obtain low swing output voltage since the output voltage swing is determined to be *Vdd*/2. This increases the complexity of the circuit.



(a) (b)

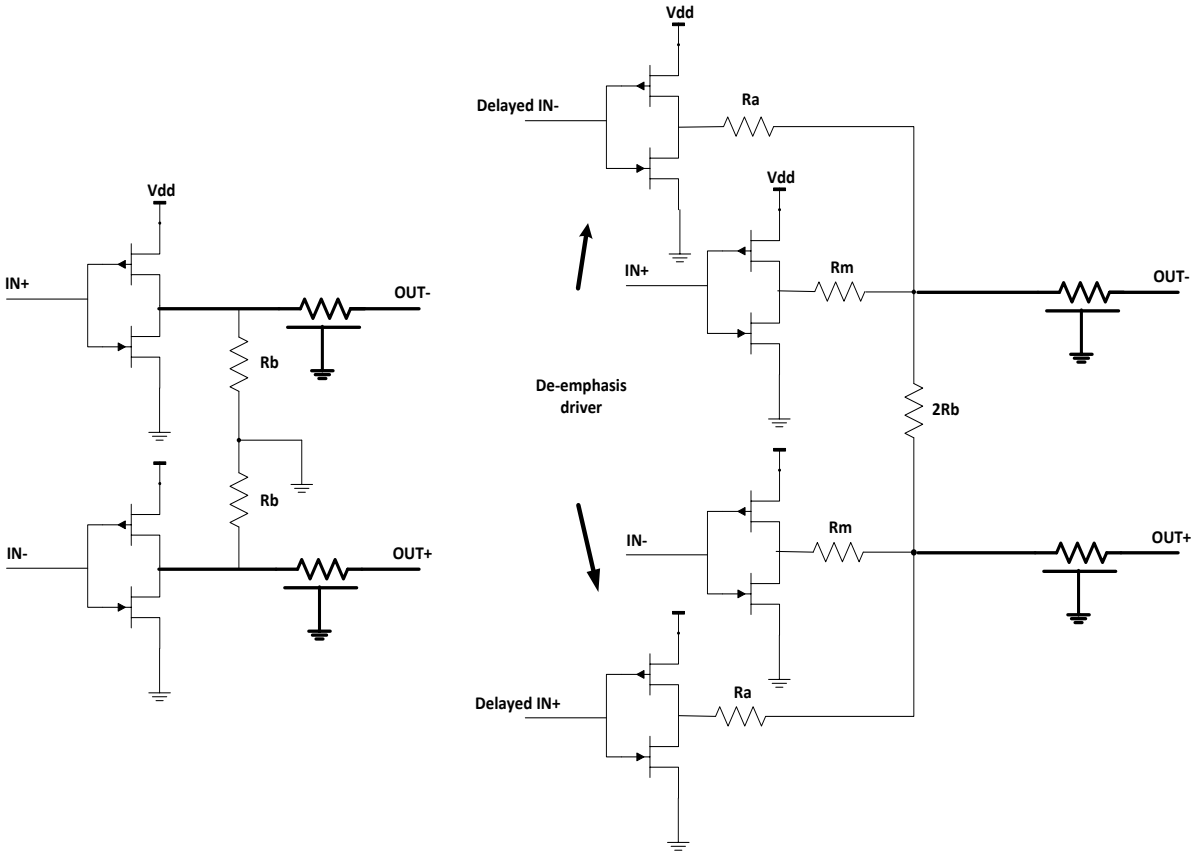
Figure 2.19: The differential VM signalling driver with (a) external low-voltage supply and (b) regulator [46].

The external voltage supply can be replaced with regulated *Vdd* as proposed by the differential VM driver scheme in Figure 2.19(b), where the voltage swing is controlled by a regulator. However, the regulator is known to be a complicated analogue circuit which requires large capacitor, C_{bypass} at the regulated supply output for an ac ground. The solution to this problem leads to another low-swing differential VM driver design as shown in Figure 2.20.

The driver circuit shown in Figure 2.20(a) is called a reduced-swing voltage mode driver, which basically consists of two *CMOS* inverters and incorporates two supplementary resistors, *Rb* between the two inverters to make an additional current path. The resistive current path allows the voltage to be reduced with the increase in resistance between *Vdd* and ground leads to less drawn current with the reduced output voltage swing. A *PMOS* transistor is used as a pull-up resistor since all devices in the driver operate with a shared supply, thus there is no need for an extra low power supply. The driver scheme also employs de-emphasis drivers to compensate the inter-symbol interference due to narrow bandwidth of the channel.

Inter-symbol interference occurs when data on a channel is corrupted by other data travelling on the same channel but at an earlier time. For lossy and on-chip interconnect channels, this happens when the energy stored from data earlier sent sums with the unrelated data. In other words, the inter-symbol interference occurs when the attenuated high frequency signal components are overwhelmed by the un-attenuated low frequency components [47]. This can

be compensated by emphasizing the high frequency signal or attenuating the low frequency components which will equalize the channels.



(a) (b)

Figure 2.20: The configuration of (a) reduced-swing VM driver signalling scheme with (b) de-emphasis driver [46].

Figure 2.20(b) shows the reduced-swing VM driver with de-emphasis drivers. The de-emphasis drivers have weak strength and one clock latency to the main driver. Since the interconnect for this scheme is already doubled due to the nature of differential signalling, additional circuitry such as the de-emphasis driver increases the total area overhead. However, there are more efficient ways incorporating a de-emphasis driver into a differential signalling scheme, these methods will be discussed later in Section 2.3.2.7.

The receiver used for the schemes proposed previously comprised a clocked unbalanced sense amplifier, which charges and discharges every clock cycle, which will slightly increase the power consumption as the activity factor will be high. Another differential voltage mode signalling scheme is proposed in [48] which comprises a receiver circuit based on the symmetric source driver level converter (*SSDLC*) scheme, as mentioned previously in

Section 2.3.2.2. The differential voltage mode driver circuit proposed in [48] is called a self level converter (*SLC*) driver, which consists of a pair of identical level converter circuits fed by the input signal and its complement. There is a pair of diode-connected transistors at the driver output which can be sized accordingly to control the output voltage swing in the desired range. The receiver produces a difference signal which cancels out any coupled and common mode noise that maybe present in the signal [48], thus increasing the robustness and reliability of the scheme. The SLC driver scheme has better delay and power characteristics but has no improvement on the effect of process variation on delay.

The differential voltage mode signalling scheme is advantageous over the single-ended schemes proposed previously, especially in terms of noise immunity and has better delay and power characteristics. However, similar to the single-ended scheme, the differential voltage mode signalling also requires additional circuitry such as a voltage regulator, de-emphasis drivers and additional low power supplies to increase its robustness against noise and process variations; subsequently, its main disadvantage is its overall complexity.

2.3.2.6. Current mode signalling scheme

The low-swing CM signalling scheme has significant advantages over the conventional low-swing VM signalling (Figure 2.10) in terms of power, delay and noise immunity [49]. The scheme is also one of the promising alternatives to the voltage mode buffer insertion scheme for high-speed low-power on-chip signalling. This technique was usually used for off-chip interconnections but several circuit designers [37,50] have explored its potential for on-chip use. The CM signalling can be implemented as a single-ended or differential signalling.

A. Single-ended Current Mode Signalling Scheme

Several repeaterless CM signalling schemes with driver pre-emphasis or dynamic overdriving have been proposed for data transmission over long interconnects [51-53]. The CM signalling schemes with driver pre-emphasis will be discussed later in the next section. Dynamic overdriving means giving a strong drive to the line during the transition of the input and very small drive in steady state. It also involves amplifying high frequency components of the input signal before transmitting. This will lead to the decrease in delay of the interconnect. The scheme can adaptively control the signal swing based on the input. CM signalling schemes with a dynamic overdriving driver are single-ended permitting high-speed data transmission at low static power consumption to be achieved [54].

An example of this scheme is the dynamically overdriving driver with feedback inverter or DOD-FB [51] as shown in Figure 2.21. The scheme consists of a strong driver and a weak driver where the output of the driver is fed back to the feedback inverter at the front. The strong driver is turned off after the line voltage crosses the switching threshold of the feedback inverter [51]. The receiver used for this scheme comprises a low gain amplifier and a controlled current source in the feedback loop of the amplifier. The feedback circuit clamps the interconnect line to *Vdd*/2 and creates a current sensing virtual ground node at the receiver input. A high sensing speed is achieved because the node is always very close to the amplifying inverter threshold voltage. The input level of the amplifier can change very quickly by the small amount needed to swing its output before the feedback becomes active to clamp the input to approximately *Vdd*/2 [51]. However, the main disadvantage of this scheme is with respect to clamping the input voltage to *Vdd*/2 which results in continuous current drain through the interconnect line, thus increasing in the power consumption. The scheme still suffers from static power consumption even though it uses sleep transistors during steady state to control the static current.

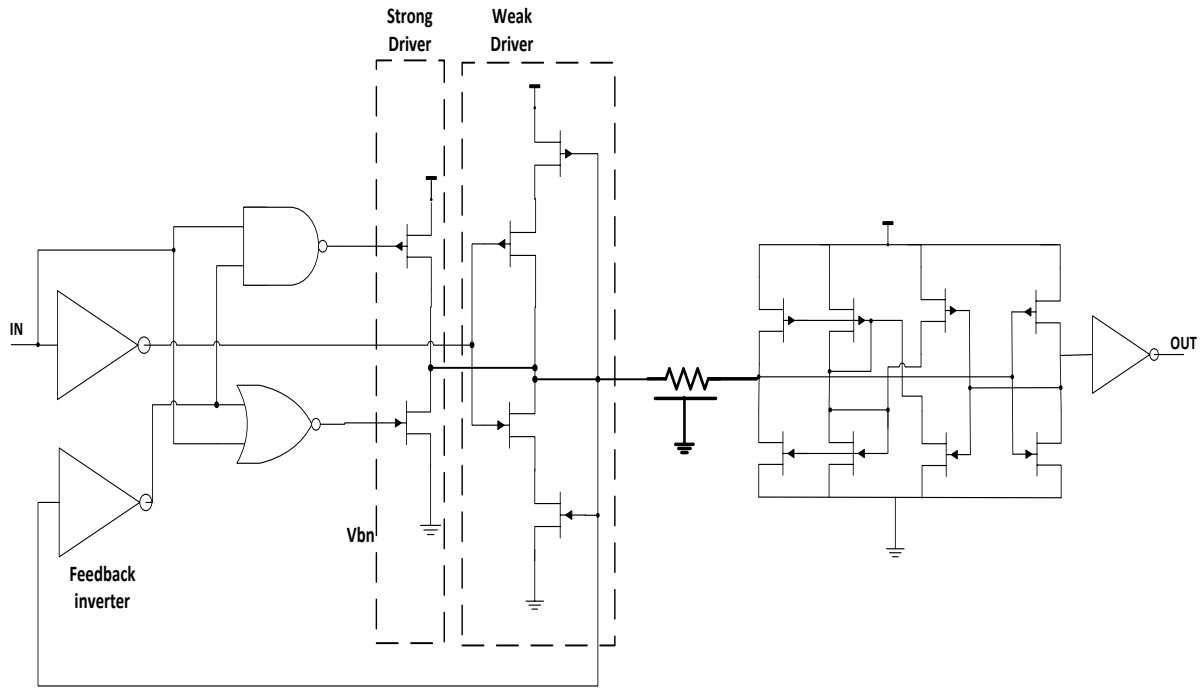


Figure 2.21: Dynamic over-driving driver circuit with feedback inverter scheme.

The DOD-FB scheme is significantly affected by the static current and thus another dynamically overdriving driver scheme is proposed to mitigate this problem. The scheme is known as a pulse-based CM scheme, as shown in Figure 2.22 which is designed to trade off

speed for a smaller static current drain [51]. The scheme implements a pulse generator at the input driver to convert the data stream into pulses. The transmitter is basically an inverter driver but with an output swing which is limited between *Vdd*-|*Vthp*| and ground. The receiver consists of a current mirror which reconstructs the pulses at the receiving end, and a feedback inverter latch. This is followed by a level converter which regenerates the level from pulses to the original data stream. The level converter also includes a delay element. The limited swing from the driver reduces the power consumption and is very critical to the receiver operation as a higher swing would turn off the receiver transistor through the current mirror [51]. The pull-down transistor of the driver has a relatively large width which is essential to provide a low resistance path to the ground. In comparison to the DOD-FB scheme, the static current is reduced but the pulse-based CM scheme is not suitable for high data activity as it trades off high speed for lower static power consumption.

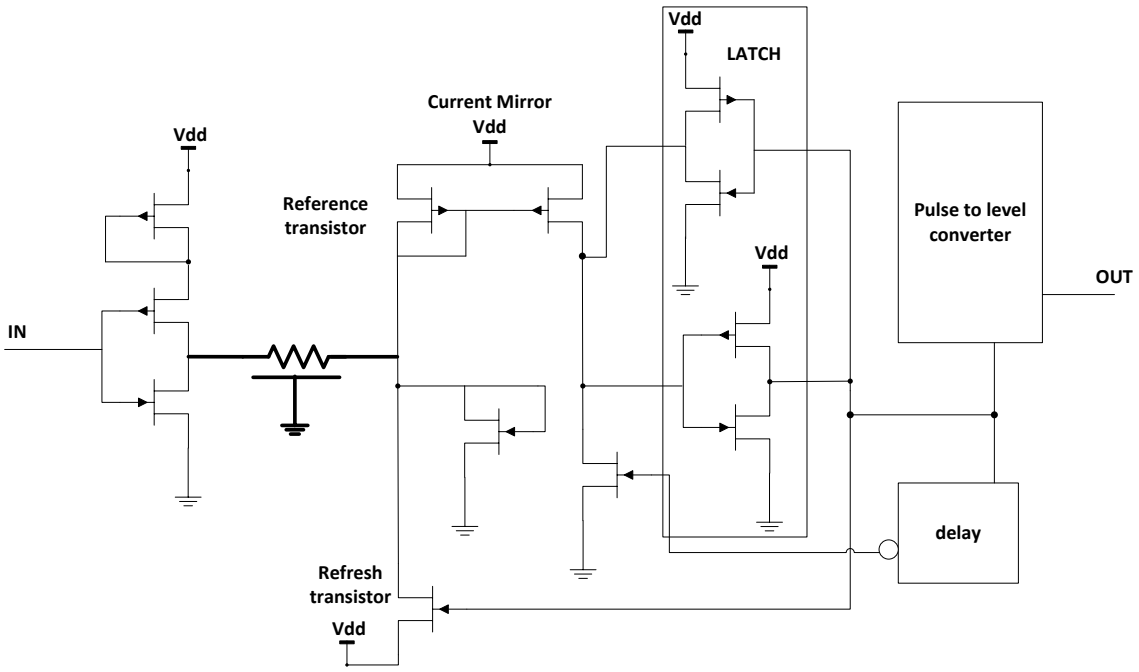


Figure 2.22: Dynamic over-driving driver circuit with pulse-based CM scheme.

Another dynamically overdriving driver scheme has been proposed [54], which is an improvement over the DOD-FB and pulse-based CM scheme in terms of power, delay and area. The scheme is a dynamic overdriving driver scheme with a biasing circuit and is also known as DOD-Bias, as shown in Figure 2.23. Similar to the DOD-FB scheme, strong and weak drivers are employed with the strong driver kept on for a fixed duration of time given by delay element in the driver. The bias voltages of the current sources in the strong and weak drivers are generated by inverters with a shorted input and output. The bias generation

circuit for the *PMOS* current sources consists of a small *PMOS* transistor which functions as a process corner sensor, and a long channel *NMOS* transistor as an internal resistor [54]. The same configuration is also applied for the bias generation circuit for the *NMOS* current sources but substitutes the small *PMOS* transistor with an *NMOS* device, and the long channel *NMOS* transistor with *PMOS* device. The static power consumption is reduced in this scheme as it is distributed to all the lines in the bias generation circuit. The delay element is a chain of 3 inverters while the receiver consists of diode-connected *PMOS* and *NMOS* pair, followed by an inverter.

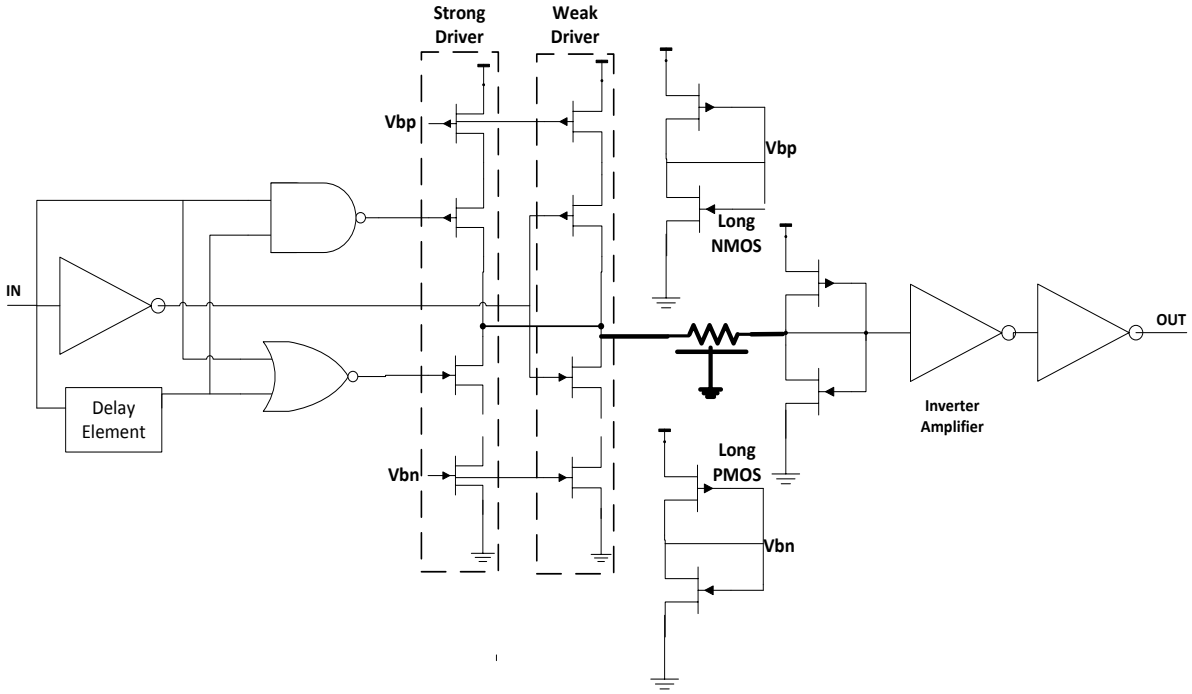


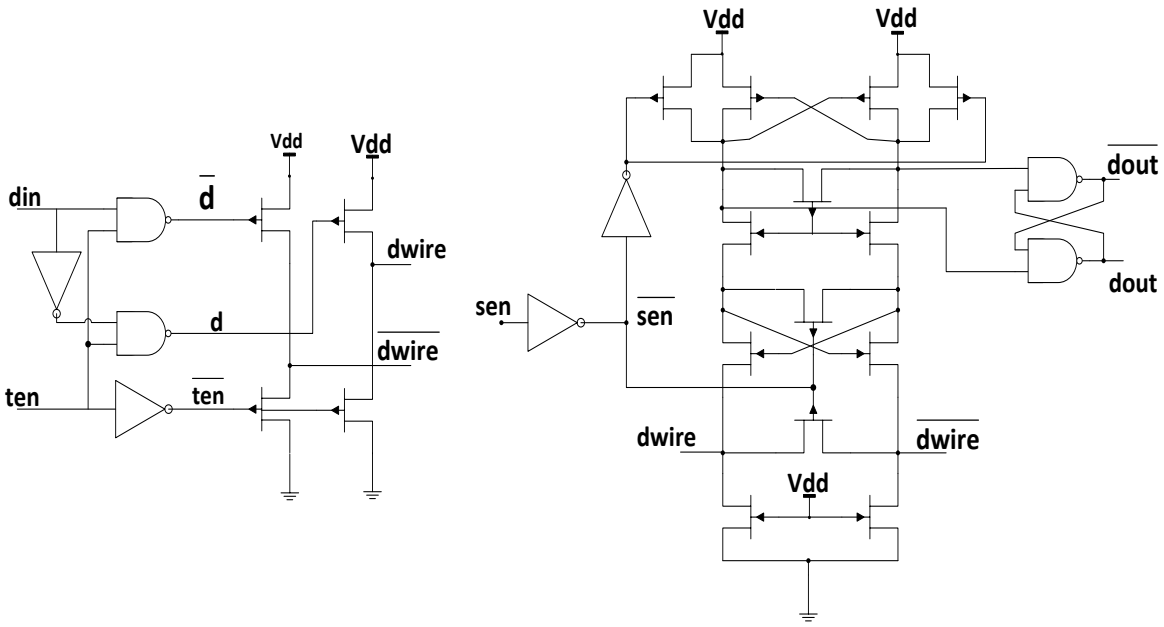
Figure 2.23: The dynamic overdriving driver scheme with a biasing circuit [54].

The DOD-Bias scheme provides significant improvements in terms of power, delay and area over other similar techniques and the conventional low-swing signalling method. However, there are a few flaws with this scheme, especially by incorporating the dynamic overdriving driver. Firstly, the DOD driver used in this low-swing signalling scheme limits the overall speed through the use of long channel transistors in the DOD driver which increase the interconnect delay [54]. Even though the problem regarding the static current is mitigated by the DOD-Bias scheme, the throughput of these CM schemes is still degraded due to the process variations.

B. Differential Current Mode Signalling Scheme

Differential CM signalling has a distinct advantage over the single-ended method in terms of noise immunity and signal integrity, which is important in deep submicron designs. Additionally, it can operate at much higher signalling rates than the conventional single-ended VM signalling schemes. The operation of the transmission line in the differential CM method allows the voltage swing to be reduced without using separate voltage references [48] and also isolates the received signal from power supply noise [49]. The drawback of CM signalling is the static power consumption. However, this can be reduced through differential CM signalling such as the single pFET current source signalling scheme [55].

The single pFET current source signalling (*SiPF*) scheme [55] consists of two current sources and some control logic as shown in Figure 2.24(a). The receiver used for this scheme is shown in Figure 2.24(b). Figure 2.25 shows the architecture of the SiPF scheme, where extra timing signals are required for the pulse generators at the driver and the receiver. There are two control signals, TEN and SEN, from the pulse generator which control the signalling scheme operation. The TEN signal enables the driver while the SEN signal enables the current mode sense amplifier receiver. The receiver converts the current difference into a logic level output. Basically, the current sources are controlled using the logic gates and the interconnect which draws high current during data transfer is actively clamped from the transmitter side. This method is to prevent the current from draining through the interconnect line. The scheme can also be used to connect multiple tri-state transmitters to a single interconnect which is faster than using parallelism or multiplexing techniques and thus saves on the number of wires required. This differential CM scheme with pulse generators is efficient in terms of delay and power, especially for global on-chip signalling as well as providing a reduction in static power consumption.



(a) (b)

Figure 2.24: The architecture of (a) the SiPF transmitter and (b) the CM sense amplifier receiver [55].

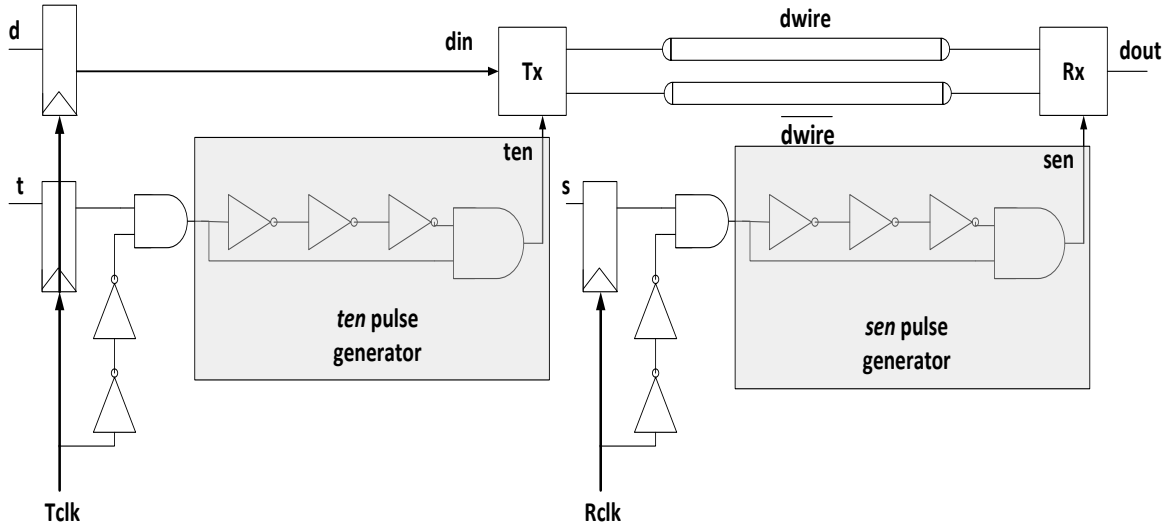


Figure 2.25: The overall architecture of the SiPF scheme [55].

Another example of a differential CM signalling scheme which instead of using pulse generators to control the signalling, a common-mode feedback circuit is used. The differential CM signalling scheme shown in Figure 2.26 is one of the schemes that is able to present a reduced swing signal and output a common-mode voltage by implementing a common-mode feedback circuit [56]. The driver comprises source-coupled logic gates with load resistors. The scheme also includes switching both the source and sink currents at the

output stage, which helps in reducing the total current consumption. The common-mode feedback circuit is applied at the input of the pre-driver buffers which help in driving the large input capacitance at the output of the driver. The buffers control the input common-mode voltage of the output driver very carefully which maintains the correct operation of the transistors at the output stage. The common-mode feedback circuitry provides a common-mode noise rejection which improves the reliability of the driver scheme. In addition, there is an improvement in speed and power.

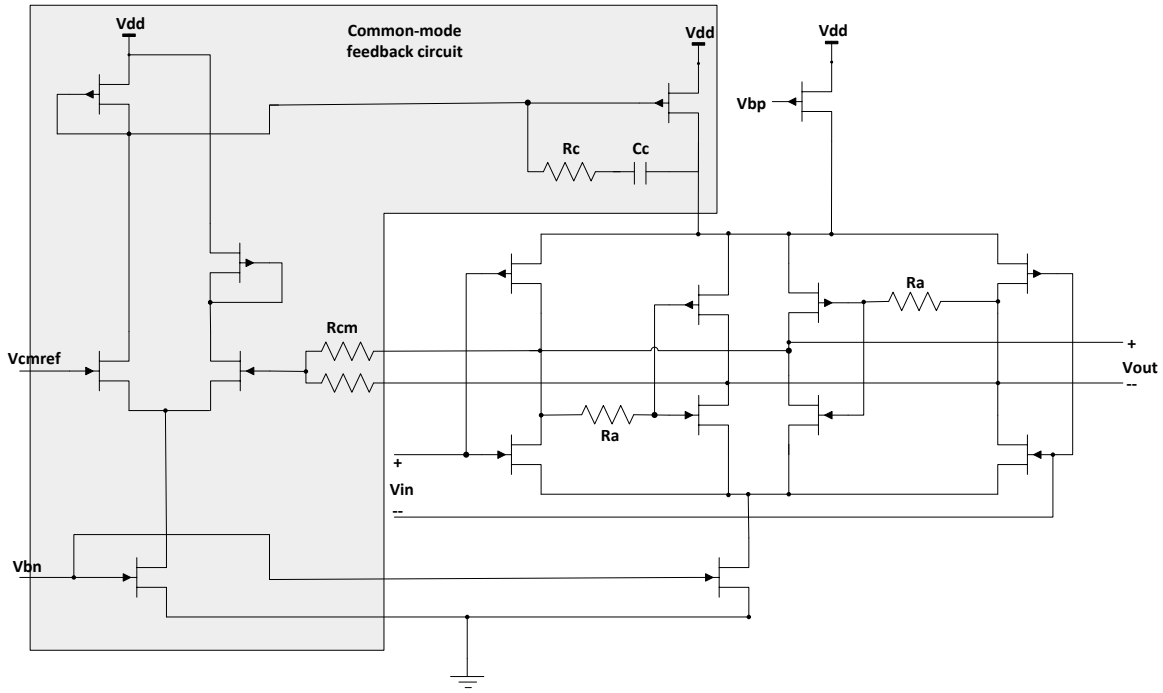


Figure 2.26: Differential CM signalling scheme with common-mode feedback circuit [56].

The SiPF and the differential CM signalling scheme with common-mode feedback circuit, require additional circuitry for the signalling operations. However, a system which does not require a pulse generator or feedback circuitry in order to achieve a high-speed low-power on-chip signalling capability is the low-swing differential CM signalling scheme [57]. As shown in Figure 2.27, the driver consists of a current source, a differential pull-down network and an active *PMOS* load. A reference voltage called *Vload* is fed to the gate of the *NMOS* transistor which functions as a current source; *Vload* is set at *1.8V*. The scheme is based on the current steering approach where the current source will generate a constant current which is steered to one of the circuit paths depending on the inputs to the differential pull-down network. The pair of *PMOS* transistors at the pull-up network acts as a load resistance. This differential CM signalling scheme provides constant energy consumption due to the use of constant current source. The dynamic power consumption is negligible with

respect to the static power [57]. The scheme improves in energy-delay product and area overhead compared to the repeater insertion technique.

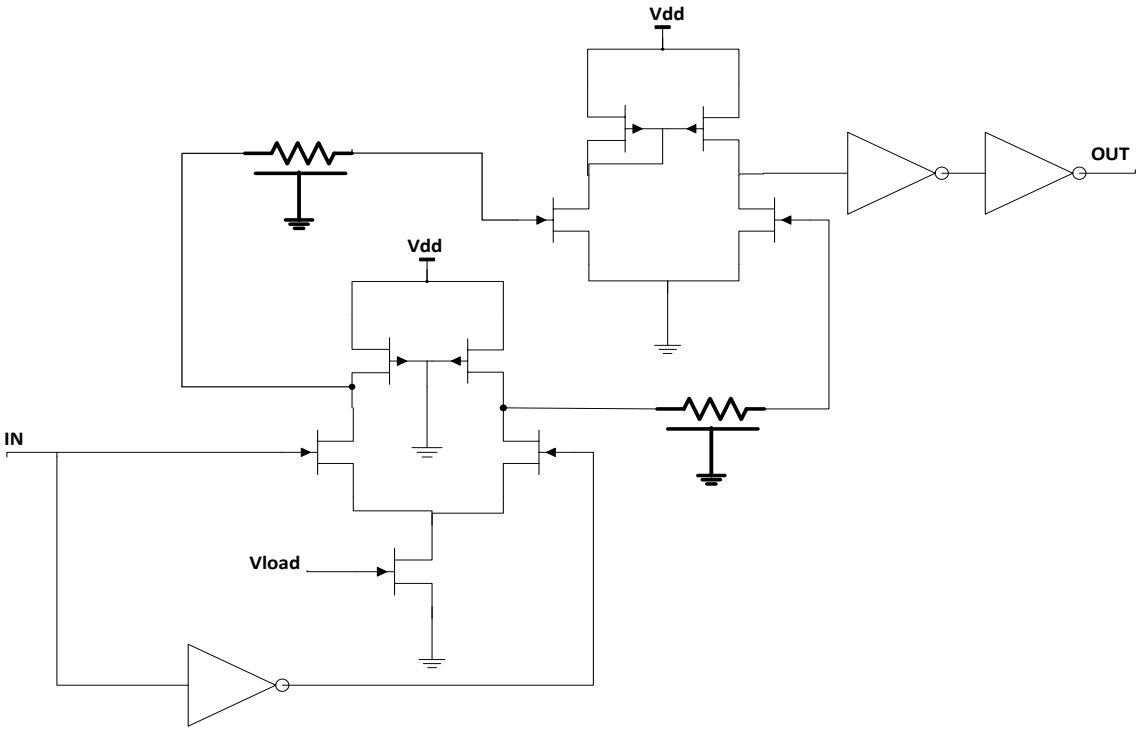


Figure 2.27: Low-swing differential CM signalling scheme [57].

Overall, the differential CM signalling schemes discussed previously come with significant costs because the transmitter and receiver require extensive complex design management such as the pulse generator and feedback circuitry, and may still be vulnerable to clock skew and jitter variations. They also introduce extensive area overhead due to the additional circuitry and extra timings as well as doubling the number of wires due to the nature of differential signalling. These drawbacks increase the complexity of the circuit. Even though the differential CM signalling scheme such as the low-swing differential CM signalling scheme [57] does not implement additional circuitry or extra timing, it does however, require a reference voltage, which is essential in keeping the current source constant for reliable signalling. In addition, for low data activity applications, the differential CM signalling scheme can create larger power dissipation than the conventional single-ended VM signalling schemes [58], due to the static current path of CM signalling which adds to the total power dissipation [59].

2.3.2.7. Driver pre-emphasis techniques

Driver pre-emphasis techniques are often used for low-power applications as they provide low-swing signalling. Unlike most low-swing signalling schemes which often sacrifice noise margin and bandwidth for low power consumption, the driver pre-emphasis techniques improve the bandwidth whilst trading off noise margin due to reduced voltage swing. This technique can be associated with the differential CM [53] and single-ended VM signalling methods [47,53]. The scheme is based on an equalization technique where the frequency dependent attenuation in a lossy transmission line is suppressed to achieve higher data rates. The suppression reduces the voltage swing, which leads to improvements in bandwidth and power consumption. In addition, the scheme also provides an overdrive of the signal at the receiver input which subsequently increases the signalling speed. When the data goes through the driver, it is pre-emphasized, which means it will not introduce any extra delay into the timing. Furthermore the data sequence does not need to be pipelined or delayed before entering the input of the bus.

There are two types of low-swing signalling schemes which incorporate driver pre-emphasis techniques [53]. The first scheme involves a differential CM signalling with driver pre-emphasis technique, and consists of, as shown in Figure 2.28, a single-ended to differential converter circuit, a 1-tap finite impulse response (*FIR*) filter and a simple digital-to-analog converter (*DAC*), where they are used to reduce the driver power overhead.

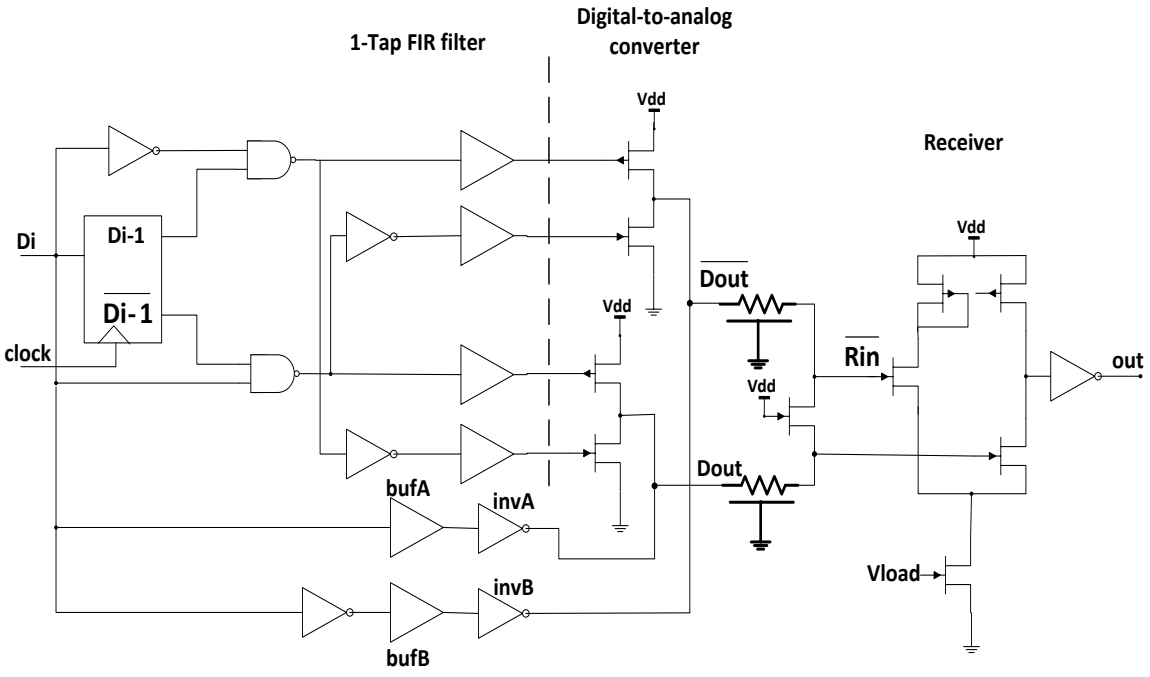


Figure 2.28: Differential CM signalling scheme with driver pre-emphasis techniques [53].

The digital-to-analog converter comprises two tri-state gates which are only turned on when a transition is detected [53]. The input to the 1-tap filter is from the delay element which consists of long-channel transistors. The filter checks whether the current data is different from the previous data sent and determines whether the DAC should be turned on. The receiver consists of an *NMOS* transistor and a differential pair of an active current mirror. The *NMOS* transistor is situated at the input of the receiver and acts as the resistive termination, while the current mirror amplifies the differential signal swing and converts it to a single-ended output. The long-channel transistors are used to compensate for the input offset voltage [53]. This configuration provides effective power savings for high data activity applications. As been analysed in [53], the static current for the differential CM signalling scheme with driver pre-emphasis technique is high for data activity factor less than 0.1.

Another configuration of an on-chip signalling scheme which incorporates the driver pre-emphasis technique is the single-end VM circuit. In current mode signalling, the high frequency signal components are pre-emphasized at the driver whilst in VM signalling the low frequency signal components are de-emphasized [47] which reduces the inter-symbol interference and thus saves power.

The single-ended VM signalling scheme with pre-emphasis driver is shown in Figure 2.29. The DAC circuit employs two stages of tri-state gates where the first stage is a pair of *PMOS/NMOS* transistors forming an un-attenuated driver, which provides a full signal swing at the driver output [53] The second stage consists of two pairs of *PMOS/NMOS* transistors forming an attenuated driver which attenuate all consecutive *1's* or *0's*. The un-attenuated driver is only turned on when there is a transition activity, which provides full signal swing at the driver output. The attenuated driver consists of a normal output driver gate which is connected to diode-connected transistors to provide the low signal swing from *Vth* to *Vdd-Vth* at the receiver input.

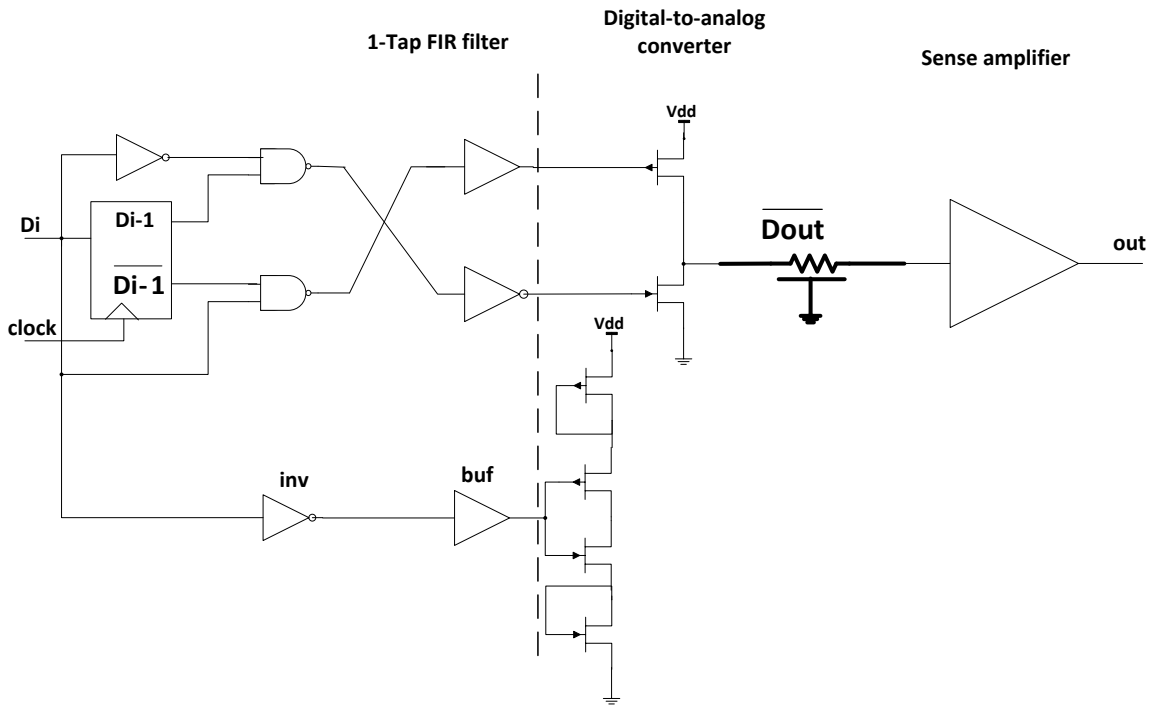


Figure 2.29: Single-ended VM signalling scheme with pre-emphasis driver [47].

The power-delay performance of the driver pre-emphasis technique is significantly improved compared to the repeater insertion technique. The pre-emphasis technique improves the bandwidth while trading off noise margin for a reduced signal swing. The reduced power consumption is achieved by both the CM and VM signalling schemes, with the CM scheme reigning over the VM scheme in terms of reduced static current. However, one important aspect that is needed to be considered is its robustness against process variations. The DC voltage levels at both driver output and the input are dependent on *Vth*, thus any variation in *Vth* will directly affect the performance of the pre-emphasis technique, especially the noise margin.

2.3.2.8. MJ Driver Circuit

MJ driver is a low-swing driver based on the UDLD driver, which provides a symmetrical low swing through the use of diode-connected transistors pairs at the output as shown in Figure 2.30. The driver circuit also provides high driving capability through the use of multipath technique where two separate paths are provided for assisting low-to-high and high-to-low transitions at the output. The upper half of the circuit is in charge of the rising transition whilst the lower half of the circuit is for the falling transition. The combination of these two paths and the feedback path through G6 provides for large output currents and fast switching of the output during transitions. In [60], the MJ driver is compared against another

diode-connected driver called the DDC driver, which shows significant improvements in speed and power consumption. An important advantage of this driver over other low-swing driver circuits discussed so far is its ability to provide high speed signalling with low power consumption without additional circuitry or wires, resulting in small area overhead. Subsequently, the MJ driver provides stable voltage swing, as a result, is less prone to noise especially supply voltage noise.

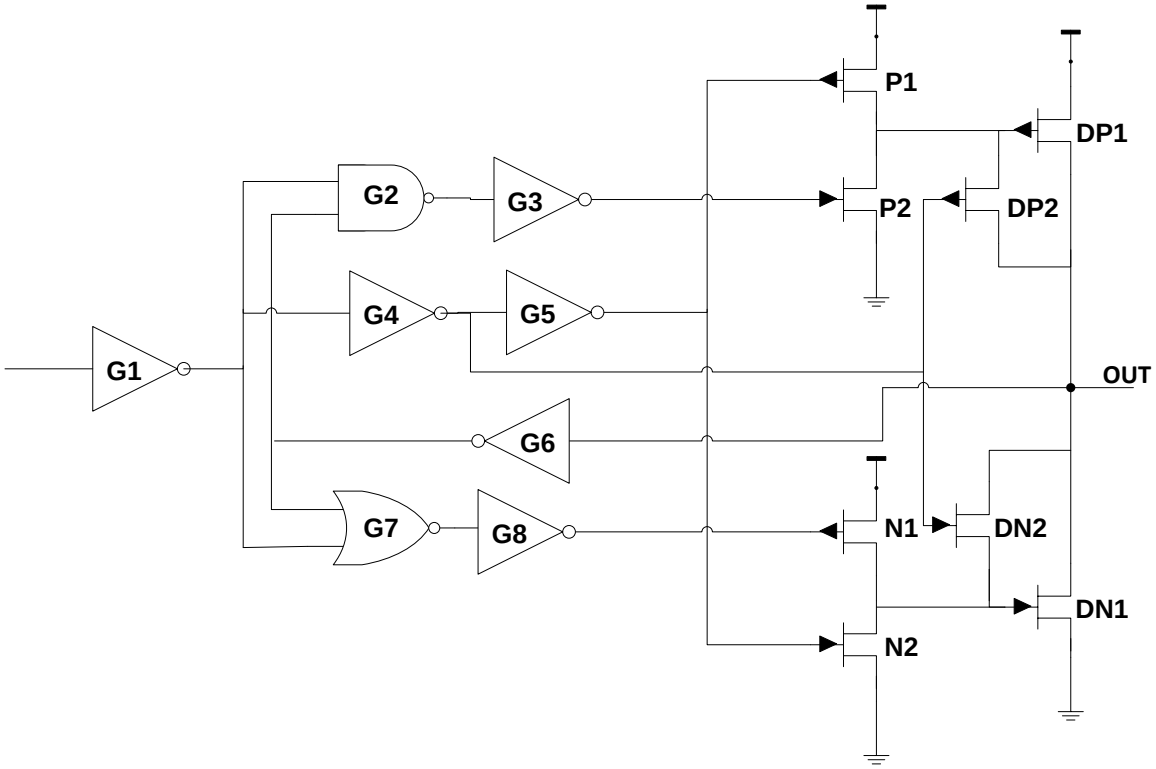


Figure 2.30: The MJ driver circuit with diode-connected configuration [60].

2.4. Summary

Several important aspects of power consumption have been discussed and some related models are introduced to assist in modelling a low-power on-chip signalling circuits for this thesis. Several low-power signalling schemes are introduced and categorized into full-swing and low-swing signalling. All the signalling schemes mentioned in this chapter are described and analysed in order to understand their features and abilities to provide low-power and high-speed signalling. Subsequently, the salient characteristics of the signalling schemes are summarised in Table 2.1, for future use and reference for designing a low-power and high-speed on-chip signalling scheme.

Table 2.1: Qualitative comparison of low-power on-chip signalling schemes.

	A	B	C	D	E	F	G	H	I	J	K
Low swing			X	X	X	X	X	X	X	X	X
Extra Vdd					X	X	X				
Reference voltage				X	X	X					
Multiple *Vdd*			X	X	X	X					
Low power	X	X	X	X	X	X	X	X	X	X	X
Low delay	X		X	X	X		X	X	X	X	X
Good SNR		X	X	X	X		X	X	X	X	X
Area penalty	X	X	X			X	X		X	X	
Low-*Vth* device				X							
Extra timing					X	X					
High leakage current			X			X		X			
Receiver-dependency			X	X	X						
Long-channel Transistor								X		X	
Extra capacitor	X										
Interconnect	Se	Se	Se	Se	Se	Se/Di	Di	Se	Di	Se/Di	Se

Keywords:

A: Bootstrapping technique
B: Parallelism technique
C: Multiple voltage technique
D: Static source driver
E: NMOS only push-pull driver
F: Charge sharing bus
G: Differential voltage mode signalling
H: Single current mode signalling
I: Differential current mode signalling
J: Driver pre-emphasis technique
K: MJ driver
Se: Single-ended signalling
Di: Differential signalling

Most of the signalling schemes summarised in Table 2.1 address low power applications but not all schemes provide high speed signalling such as schemes employing parallelism techniques and charge sharing bus techniques. The full-swing signalling schemes such as

those that employ parallelism and bootstrapping techniques can provide low power implementations but are slightly less efficient compared to power savings ability provided by the low-swing signalling methods. However, the main issue faced by the low-swing signalling schemes is the area penalty. The necessity to accommodate extra *Vdd* supplies, reference voltages, low-Vth devices, extra timing and multiple *Vth* contribute to the increase in area overhead and complexity. Subsequently, several low-swing signalling schemes also incorporate long-channel transistors which can caused increase in delay of overall scheme. The main problem with the differential low-swing signalling schemes are the increase in the number of wires which adds to the area overhead. Even though this issue can be traded off with the noise rejection and significant power reduction, the increase in the number of wires can significantly affect the complexity of the schemes especially if additional circuitry such as multiple *Vdd* supplies and extra timing circuitry are required. The most important aspect that can be highlighted here is that process variation analysis is often not included in their analysis, which is significantly important as process variation can adversely affect the performance of the signalling schemes.

Table 2.1 indicates that the MJ driver circuit (K), has the best attributes compared to the other signalling schemes. This is because the scheme provides low power and high speed signalling without the use of extra circuitry such as extra *Vdd* and reference voltages. In addition, the scheme has a good *SNR* as well as low leakage currents. The MJ driver employs a simple inverter at the receiver end, which also minimises the area overhead. The differential current mode signalling also has similar attributes to the MJ driver, however, suffers from area penalty due to the doubled number of wires. Furthermore, sense amplifiers are usually incorporated in the differential current mode signalling schemes, which increases the area penalty.

Another candidate that is also has comparable attributes with the MJ driver is the driver pre-emphasis technique. Even though extra circuitry such as extra *Vdd* supplies, multiple *Vth* and reference voltages are not required for driver pre-emphasis techniques, which can increase overall complexity, the schemes still suffer from area penalty due to the double number of wires used for differential pre-emphasis driver scheme and the use of a sense amplifier for both single-ended and differential pre-emphasis driver schemes. Subsequently, the use of long-channel transistors may affect the overall throughput of the scheme as the driver pre-emphasis technique significantly dependent on the long-channel transistors.

The low-swing signalling schemes proposed in this work also incorporate diode-connected configuration at the output as they can provide low-power and high-speed signalling due to its high driving capability without the use of a sense amplifier, long-channel transistors and even additional number of wires, similar to the MJ driver circuit. The proposed scheme is able to further reduce the signal swing in order to have significant power reduction whilst still maintaining high speed performance and good SNR.

The most important aspect that can be highlighted here is that process variation analysis is often not included in the analysis, which is significantly important as process variation can affect the performance of the signalling schemes. In addition to process variation, the impact of temporary faults such as crosstalk and single event upset are important issues to consider. Analysis on process variation as well as temporary faults will be discussed in the later chapters, addressing the robustness of the proposed low-swing signalling scheme against variability and external disturbances.

References

[1] S. Borkar, "Design challenges of technology scaling," *Micro, IEEE*, vol. 19, 1999, pp. 23-29.

[2] D. Sylvester Kaul, H., "Power Driven Challenges in Nanometer Design," *IEEE Design and Test of Computers*, vol. 13, 2001, pp. 12-21.

[3] V. De and S. Borkar, "Technology and design challenges for low power and high performance [microprocessors]," *1999 International Symposium on Low Power Electronics and Design Proceedings.*, S. Borkar, ed., 1999, pp. 163-168.

[4] W. Jeong, B.C. Paul, and K. Roy, "Adaptive supply voltage technique for low swing interconnects," *Proceedings of the 2004 Asia and South Pacific Design Automation Conference*, Yokohama, Japan: IEEE Press, 2004, pp. 284-287.

[5] K.S. Yeo Roy, K., *Low-Voltage, Low-Power VLSI Subsystems*, McGraw Hill, 2005.

[6] E. Macii, *Ultra Low Power Electronics and Design*, Kluwer Academic Publishers, 2004.

[7] S.P. Mohanty Ranganathan, N., Kougianos, E., Patra, P., *Low-Power High-Level Synthesis for Nanoscale CMOS Circuits*, Springer, 2008.

[8] C. Piguet, *Low power CMOS circuits: technology, logic design and CAD tools*, Taylor and Francis Group (CRC), 2006.

[9] J. Rabaey, *Low Power Design Methodologies*, Kluwer Academic Publishers, 1995.

[10] U. of C. Berkeley, "BSIM4.3.0 MOSFET Model User's Manual."

[11] K.T. T. Sakurai, "Simple formulas for 2 and 3-D capacitances," *IEEE Trans. Electron Devices*, vol. 30, 1983, pp. 183-185.

[12] B.P. Wong Mittal Anurag, Cao, Y., Starr, G., *Nano-CMOS circuit and physical design*, John Wiley & Sons, 2005.

[13] P. Vanoostende, P. Six, and H.J. DeMan, "Evaluation of the limitations of the simple CMOS power estimation formula: comparison with accurate estimation," *Proceedings of European Workshop on power and timing modelling*, 1992, p. 16.25.

[14] S. Iman Pedram, M., "Multilevel Network Optimization for Low Power," *Proc. 1994 IEEE/ACM Int. Conf. on CAD, ICCAD'94*, 1994, pp. 372-377.

[15] R.V. Menon Chennupati, S., Samala, N.K., Radhakrishnan, D., Izadi, B., "Switching activity minimization in combinational logic design," *Proceedings of 2004 Int. Conf. on Embedded Systems and Applications*, 2004, pp. 45-51.

[16] M. Ito Chinnery, D., Keutzer, K., "Low Power Multiplication Algorithm for Switching Activity Reduction through Operand Decomposition," *Proceedings of 21st Int. Conf. on Computer Design*, 2003, pp. 21-26.

[17] W. Nebel, "System Level Power Optimization," *Euromicro Symposium on Digital System Design*, 2004, pp. 27-34.

[18] A.C. J. M. Rabaey Borivoje Nikolic, *Digital Integrated Circuits*, Prentice Hall, 2003.

[19] B. Kheradmand-Boroujeni and M. Masoumi, "A new large capacitive-load driver circuit for low-voltage CMOS VLSI," *2004 IEEE International Workshop on Biomedical Circuits and Systems*, M. Masoumi, ed., 2004, pp. S1/1-S5-8.

[20] N. Hanchate Ranganathan, N., "LECTOR: A technique for leakage reduction in CMOS circuits," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 12, 2004, pp. 196-205.

[21] A. Rjoub and O. Koufoparlou, "Low power high speed multithreshold voltage CMOS bus architecture," *Computer and Electrical Engineering (CEE)*, vol. 30, 2004, pp. 269-280.

[22] P.C. Chen and J.B. Kuo, "Sub-1V CMOS large capacitive load driver circuit using direct bootstrap technique for low voltage CMOS VLSI," *Electronic Letters*, vol. 38, 2002, pp. 265-266.

[23] J.C. Garcia, J.A. Montiel-Nelson, J. Sosa, and H. Navarro, "A Direct Bootstrapped CMOS Large Capacitive-Load Driver Circuit," *Design, Automation and Test in Europe. DATE'04*, vol. 1, 2004, pp. 680-681.

[24] J.H. Lou and J.B. Kuo, “A 1.5-V full-swing bootstrapped CMOS large capacitive-load driver circuit suitable for low-voltage CMOS VLSI,” *Solid-State Circuits, IEEE Journal of*, vol. 32, 1997, pp. 119-121.

[25] J.B. Kuo, “Evolution of bootstrap techniques in low-voltage CMOS digital VLSI circuits for SOC applications,” *Fifth International Workshop on System-on-Chip for Real-Time Applications, 2005. Proceedings.*, 2005, pp. 143-148.

[26] J.C. Garcia, J.A. Montiel-Nielsen, and S. Noorshabadi, “A single capacitor bootstrapped power efficient CMOS driver,” *48th Midwest Symposium on Circuits and Systems*, vol. 1, 2005, pp. 287-290.

[27] R.W.B. A.P. Chandrakasan S.Sheng, “Low Power CMOS Digital Design,” *IEEE Journal of Solid-State Circuits*, vol. 27, 1992, pp. 473-484.

[28] J.M. W. Nebel, *Low Power Design in Deep Submicron Electronics*, Dordrecht: 1997.

[29] D. Soudris, *Circuit Techniques for Dynamic Power Reduction*, CRC Press, 2006.

[30] C.K. Yang and M. Horowitz, “A 0.8um CMOS 2.5Gb/s Oversampling receiver and transmitter for serial links,” *IEEE Journal of Solid-State Circuits*, vol. 31, 1996, pp. 2015-2023.

[31] K. Lee, “A CMOS serial link for fully duplexed data communication,” *IEEE Journal of Solid-State Circuits*, vol. 30, 1995, pp. 353-364.

[32] J. Kim, “Design of CMOS adaptive supply serial link,” 2002.

[33] M.-J.E. Lee, W.J. Dally, and P. Chiang, “Low power area efficient high speed I/O circuit techniques,” *IEEE Journal of Solid-State Circuits*, vol. 35, 2000, pp. 1591-1599.

[34] F. Ishihara, F. Sheikh, and B. Nikolic, “Level conversion for dual-supply system,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 12, 2004, pp. 185-195.

[35] K. Usami, M. Igarashi, F. Minami, T. Ishikawa, M. Kanazawa, M. Ichida, and K. Nogami, “Automated low power technique exploiting multiple supply voltages applied to a modern processor,” *IEEE Journal of Solid-State Circuits*, vol. 33, 1998, pp. 463-472.

[36] R. Puri, L. Stok, J. Cohn, D. Pan, D. Sylvester, A. Srivastava, and S. Kulkarni, “Pushing ASIC performance in a power envelope,” *Proc. 2003 IEEE/ACM Int. Conf. on CAD, ICCAD’03*, 2003, pp. 788-793.

[37] H. Zhang, V. George, and J.M. Rabaey, “Low-swing on-chip signaling techniques: effectiveness and robustness,” *IEEE Trans. Very Large Scale Integrated System*, vol. 8, 2000, pp. 264-272.

[38] F.S. Q. Zhu P. Chong, “A Placement Technique for Multiple Voltage Design,” 2006.

[39] D. Rittman, “Challenges and solutions in physical design for high performance IC design in VDSM era,” 2004.

[40] Y. Nakagome, K. Itoh, M. Isoda, K. Takeuchi, and M. Aoki, “Sub-1-V swing internal bus architecture for future low-power ULSIs,” *Solid-State Circuits, IEEE Journal of*, vol. 28, 1993, pp. 414-419.

[41] M. Hiraki, H. Kojima, H. Misawa, T. Akazawa, and Y. Hatano, “Data dependent logic swing internal bus architecture for ultra low power LSI’s,” *IEEE Journal of Solid-State Circuits*, vol. 30, 1995, pp. 397-402.

[42] H. Yamauchi, H. Akamatsu, and T. Fujita, “An assymptotically zero power charge recycling bus architecture for battery operated ultrahigh data rate ULSI’s,” *IEEE Journal of Solid-State Circuits*, vol. 30, 1995, pp. 423-431.

[43] A. Inoue, V.G. Oklobdzija, W.W. Walker, M. Kai, and T. Izawa, “A low power SOI adder suing reduced-swing charge recycling circuits,” *IEEE Journal of Solid-State Circuits*, 2001, pp. 316-317.

[44] P. Sotiriadis, T. Konstantakopoulos, and A. Chandrakasan, “Analysis and implementation of charge recycling for deep submicron buses,” *Proceedings of 2001 International Symposium on Low Power Electronics and Design, ISLPED’01*, 2001, pp. 364-369.

[45] R. Bashirullah, W. Liu, and R. Cavin III, “Delay and power model for current-mode signaling in deep submicron global interconnects,” *Proceedings of the IEEE 2002 Custom Integrated Circuits Conference*, 2002, pp. 513-516.

[46] H. Song, S. Kim, and D.-K. Jeong, “A reduced-swing voltage-mode driver for low power multi-Gb/s transmitter,” *Journal of Semiconductor Technology and Science*, vol. 9, 2009, pp. 104-109.

[47] L. Zhang, J.M. Wilson, R. Bashirullah, L. Luo, J. Xu, and P.D. Franzon, “Voltage-Mode Driver Preemphasis Technique For On-Chip Global Buses,” *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 15, 2007, pp. 231-236.

[48] A. Narasimhan, M. Kasotiya, and R. Sridhar, “A low-swing differential signalling scheme for on-chip global interconnects,” *18th International Conference on VLSI Design*, 2005, pp. 634-639.

[49] W.J. Dally and J.W. Poulton, *Digital Systems Engineering*, Cambridge University Press, 1998.

[50] A. Maheswari Burleson, W., “Current Sensing Techniques for Global Interconnects in VDSM CMOS,” *Proceedings of IEEE Computer Society Workshop on VLSI*, 2001, pp. 66-70.

[51] A. Katoch, H. Veendrick, and E. Seevinck, “High speed current mode signal circuit for on-chip interconnects,” *IEEE International Symposium on Circuits and Systems, ISCAS 2005*, vol. 4, 2005, pp. 4138-4141.

[52] M.M. Tabizi, N. Masoumi, and M. Deilami, "High speed current mode signalling for interconnects considering transmission line and crosstalk effects," *50th Midwest Symposium on Circuits and Systems, MWSCAS'07*, 2007, pp. 17-20.

[53] L. Zhang, J. Wilson, R. Bashirullah, L. Luo, J. Xu, and P. Franzon, "Driver pre-emphasis techniques for on-chip global buses," *Proceedings of the 2005 International Symposium on Low Power Electronics and Design, ISLPED '05*, 2005, pp. 186-191.

[54] M.V. Dave, M.S. Baghini, and D. Kuma-Sharma, "A process variation tolerant high speed and low power current mode signalling scheme for on-chip interconnects," *Proceedings of the 19th ACM Great Lakes Symposium on VLSI*, 2009, pp. 389-392.

[55] N. Tzartzanis and W.W. Walker, "Different current mode sensing for efficient on-chip global signalling," *IEEE Journal of Solid-State Circuits*, vol. 40, 2005, pp. 2141-2147.

[56] A. Tajalli and Y. Leblebici, "A power-efficient LVDS driver circuit in 0.18um CMOS technology," *Research in Microelectonics and Electronics Conference, PRIME 2007*, 2007, pp. 145-148.

[57] L. Yang, C. Jue-Ping, H. Yue, and L. Yi, "A low swing differential signalling circuit for on-chip global interconnects," *9th International Conference on Solid-State and Integrated-Circuit Technology, ICSICT 2008*, 2008, pp. 1693-1696.

[58] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A 3Gb/s/ch transceiver for RC-limited on-chip interconnects," *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, 2005, pp. 386-606 Vol. 1.

[59] E. Seevinck Beers, P.V., Ontrop, H., "Current mode techniques for high speed VLSI circuits with application to current sense amplifiers for CMOS SRAMs," *IEEE Journal of Solid-State Circuits*, vol. 26, 1991, pp. 525-536.

[60] J.C. Garcia, J.A. Montiel-Nelson, and S. Nooshabadi, "Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects," *IEEE International Symposium on Circuits and Systems, ISCAS 2007*, 2007, pp. 881-884.

Chapter 3

LOW-SWING SIGNALING SCHEMES INCORPORATING A DIODE-CONNECTED CONFIGURATION

3.1. Background

Delay and power dissipation have been important issues for quite some time due to the aggressive scaling used in integrated circuit design. The ever increasing energy consumption of an integrated circuit is mainly due to the interconnect wires and the associated driver and receiver circuits. The need for high speed on-chip signalling with low power is increasingly in demand. Low swing signalling schemes are known to provide both high speed and low power to global on-chip applications as discussed in Chapter 2. Most of the low-swing signalling schemes are also immune to noise as they have good *SNR*. However, the low-swing signalling schemes discussed in Chapter 2, have a large penalty in area and complexity as they require additional circuitry such as internal voltage generators and *low-Vth* devices. Most of the schemes also incorporate multiple *Vdd* and reference voltages which increase the overall circuit complexity. As shown in Table 2.1, the low-swing signalling circuit called the MJ driver scheme [1] has the best attributes over the other low-swing signalling techniques in terms of low power, low delay, good *SNR* and low area overhead.

The MJ driver is classified as a diode-connected driver, other driver circuits in this category are the UDLD [2] and DDC [3] drivers, which will be discussed in this chapter. The VM pre-emphasis driver scheme [4] introduced in Chapter 2, also incorporates a diode-connected configuration. This configuration is efficient in providing a high speed signalling due to its high driving current capability, especially if placed at the output, as in the case of the MJ driver and the VM pre-emphasis driver described in Chapter 2. Subsequently, this configuration also provides lower voltage swing at the output, which directly leads to lower power consumption. However, the issue with this type of configuration is its adaptability to process variation [3], as well as the issue with leakage currents. Consequently, this means it is of the utmost importance to address these issues when designing a diode-connected driver or any type of low-swing driver, as well as obtaining low power consumption and maintaining high speed signalling.

Therefore in this work, a low-swing signalling scheme which incorporates the diode-connected configuration is proposed. The proposed driver circuits, namely the nLVSD and the mLVSD drivers, which have similar characteristics to the MJ driver, will be discussed in this chapter. The nLVSD and mLVSD circuits will be analysed in terms of power consumption and performance; the common problematic issues, such as noise and leakage power consumption, encountered by other diode-connected driver schemes will also be addressed.

This chapter continues with an overview of the performance metrics of a low-swing signalling scheme in Section 3.2. The structure and components of the low-swing signalling scheme incorporating diode-connected configuration is introduced in Section 3.3 together with its main components (*driver*, *interconnect*, *receiver*) which are detailed in separate sub-sections. The driver subsection will concentrate on the diode-connected configuration, which includes a background review on the structure and circuit operations, which leads to the proposed driver circuits. Brief introductions on the interconnect and the receiver design will also be included. Lastly, an outline of the performance analyses that will be undertaken are described, which includes the comparison between the DDC (dynamic diode-connected), MJ and the proposed driver schemes in terms of power consumption, delay, area overhead and noise immunity. The power consumption and delay of the driver schemes are analysed against several contributing factors such as the load capacitance, supply voltage, operating temperature and frequency.

3.2. Performance Metrics Of Low-Swing Signalling Schemes

The work in this thesis involves a comparison between four diode-connected driver schemes in terms of their performance on long interconnect. Consequently, to make a fair comparison between the schemes, the same interconnect architecture is used. For each of the schemes under test, the following metrics will be considered.

a) Dynamic power consumption

The dynamic switching energy of a wire is a function of wire capacitance, load capacitance, supply voltage and voltage swing, which is shown in Equ.3.1 [5];

$$Energy = (C_L + C_w)V_{dd}V_{swing}. \quad (3.1)$$

While the dynamic power consumption can be calculated by using Equ.3.2, which is a product of energy and switching frequency.

$$P_{dyn} = Energy.f_{req} \quad (3.2)$$

b) Design complexity

The design complexity of a signalling scheme can be measured in terms of its area overhead and the use of additional *Vdd* or *low-Vth* devices.

c) Delay

Delay can be approximated by the Sakurai's equation [6] shown below.

$$Delay = 0.4R_W C_W l_e^2 + 0.7(R_{dr}C_W l_e + R_{dr}C_L + R_W C_L l_e) \quad (3.3)$$

where R_W and C_W are the interconnect resistance and capacitance per unit length, l_e, R_{dr} is the output resistance of the driver, and C_L is the load capacitance. The output resistance of a *MOSFET* is a nonlinear function of the supply voltage. A closed form expression for R_{dr} is given below [7].

$$R_{dr} = \frac{3}{4}\frac{V_{dd}}{I_{dsat}}\left(1 - \frac{7}{9}\lambda V_{dd}\right) \quad (3.4)$$

where,

$$I_{dsat} = k'\frac{W}{L}\left((V_{dd} - V_{th})V_{dsat} - \frac{V_{dsat}^2}{2}\right) \quad (3.5)$$

and

$$k' = {\mu\varepsilon_{ox}}/{t_{ox}} \quad (3.6)$$

Where, I_{dsat} = saturation drive current, V_{dsat} = saturation source drain voltage, *W/L* = transistor aspect ratio, t_{ox} = gate oxide thickness, λ = channel length modulation, proportional to the increase of channel length.

C_L can be calculated through the equation for the driver delay, which is approximately equivalent to $0.7R_{dr}C_L$. The driver delay, t_p, can be determined by using a circuit simulation

package, for example, *SPECTRE*. The delay can also be obtained by measuring from the 50% *Vdd* point of the signal input of the driver to corresponding point on the signal at the end of the line, i.e. the signal input of the receiver, as shown in Figure 3.1.

d) Energy-Delay-Product and Power-Delay-Product

Both metrics can be used to analyse both power and speed performance. Energy-Delay-Product (*EDP*) is a product of total energy consumption and propagation delay while Power-Delay-Product is defined as a product of the average power consumption and propagation delay. These metrics are usually used in determining optimized widths of a device. *EDP* is preferable since it is independent of the operating frequency, which simplifies the optimization process and can be applied at any signal rate.

e) Waveform integrity

Waveform integrity can be measured in terms of slew rate and signal overshoot. An ideal signal is a step function, switching instantaneously between 0 and *Vdd*. However, this model is only an approximation to the actual switching waveforms, which in reality have a non-zero slew rate and possible signal overshoots.

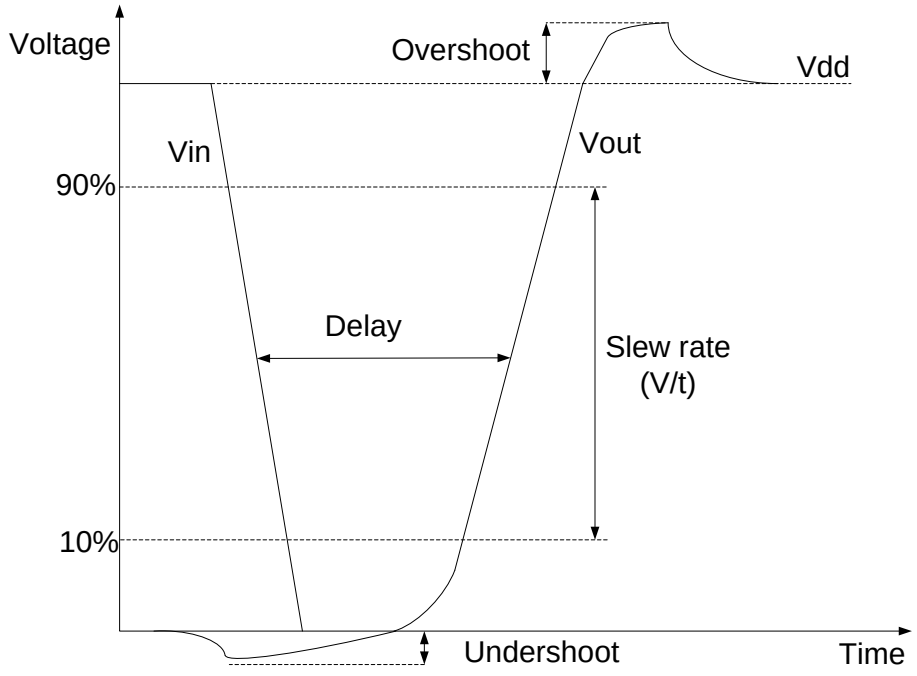


Figure 3.1: Performance metrics for on-chip interconnect analysis [8].

Slew rate is defined as the ratio of voltage to time (V/t) required for the signal to change from 10% to 90% of its final value. Due to limited driver strength and lossy interconnect condition, switching in reality has a finite slew rate, which delays signal stabilization and transportation. As circuit speed increases rapidly, slew rates need to be well controlled. Furthermore, high speeds may also lead to signal overshoot, either above *Vdd* or below ground (*undershoot*), as shown in Figure 3.1.

f) Reliability

Reliability is measured in terms of signal-to-noise (*SNR*) ratio, which is defined as

$$SNR = \frac{0.5V_S}{V_N} \tag{3.7}$$

The worst-case noise analysis for reliability measurement has been summarised in [9]. The overall noise is considered to be generated from two main sources categorized as either proportional noise sources or independent noise sources, as shown below,

$$V_N = K_N V_S + V_{IN} \tag{3.8}$$

The proportional noise sources ($K_N V_S$) are proportional to the magnitude of signal swing such as crosstalk and the signal-induced power supply noise. The signal-induced power supply noise K_{PS} is estimated to be 1% and 5% of the signal swing for differential and single-ended signalling, respectively. The crosstalk coupling coefficient, K_C is a ratio between coupling capacitance and interconnect load capacitance as shown in Equ.3.9, where C_C is the coupling capacitance, C_W is the interconnect capacitance and C_L is the fan-out capacitance. The crosstalk attenuation is estimated to be 0.05 for a static driver circuit. Therefore, when considering the effect of crosstalk noise, $K_N = Attn_C K_C + K_{PS}$ where $Attn_C$ is crosstalk noise attenuation.

$$K_C = \frac{C_C}{C_W + C_C + C_L} \tag{3.9}$$

V_{IN} comprises independent noise sources such as receiver input offset, receiver sensitivity and signal-unrelated power supply noise. The receiver input offset, R_X_O and receiver sensitivity, R_X_S are dependent on the receiver, which involves changes in the receiver's switching threshold voltage in respect to process variations. The signal-unrelated power supply noise, *PS* is assumed to be 5% of the magnitude of the power supply. The power

supply attenuation coefficient, *Attn* is defined as the change in the switching threshold voltage in respect to the supply voltage variation whilst the transmitter offset, T_X_O results from the parameter mismatch between the transmitter and receiver. Equ.3.8 can subsequently be expanded to include these noise parameters, as shown in Equ.3.10.

$$V_{IN} = R_X\_O + R_X\_S + Attn.PS + T_X\_O \qquad (3.10)$$

The power supply attenuation coefficient, *Attn* is measured by the changes in receiver switching threshold voltage due to the change of the supply voltage, as shown in Figure 3.2(a). Receiver input offset, R_X_0 and receiver sensitivity, R_X_S can be measured as shown in Figure 3.2(b) where the worst case difference of the threshold voltage is measured at every simulated process corner.

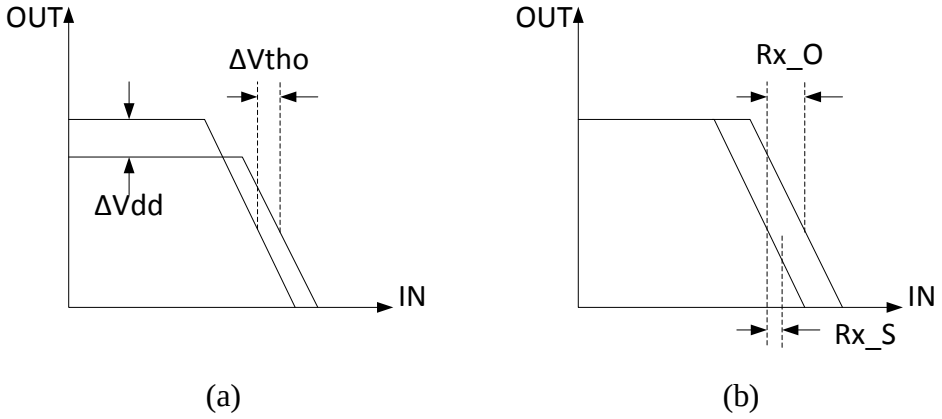


Figure 3.2: The measurement of (a) power supply attenuation coefficient, and (b) receiver input offset and sensitivity [9].

3.3. The Low-Swing Driver Signalling Schemes

Long global interconnects are usually associated with long propagation delay and on-chip power consumption, mainly due to its parasitic components. Most circuits apply low voltage techniques to mitigate problems with power consumption and propagation delay. However, driving large capacitive loads limits the performance of *CMOS* circuits, especially at low voltages. The most effective technique for global interconnects to achieve power reduction and delay efficiency is by reducing the voltage swing of the signal propagating along the wire; however, this will require a fast low voltage swing driver circuits. Low swing signalling schemes consist of a low voltage swing driver and a low power level restorer

(*output buffer*) at the receiver end, as shown in Figure 3.3. Each of the main components (*driver, interconnect, receiver*) of the scheme requires careful detailed design in order to obtain the objective of having a low power and fast signalling scheme for global interconnects. For this work, the design of a diode-connected driver circuit will be focused on, followed by the interconnect model and suitable receiver design.

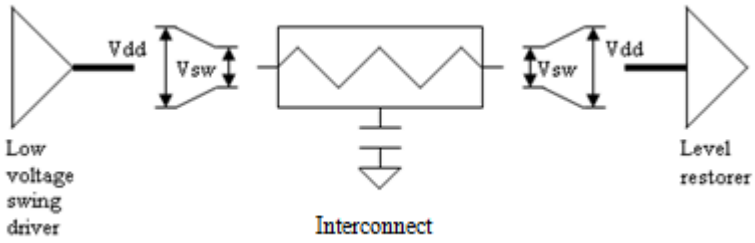


Figure 3.3: The architecture of low swing signalling scheme.

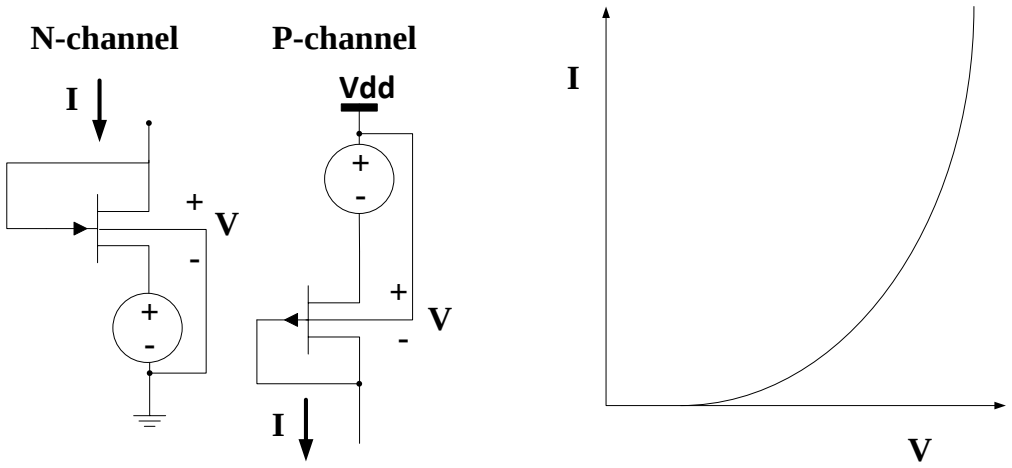
3.3.1. Diode-connected driver structure

Basically, power consumption is a product of switching frequency, load capacitance, supply voltage and voltage swing. The voltage swing should be as low as possible in order to reduce the power consumption. The challenge is in retrieving back the original signal or how to convert the low swing back to the full rail signal swing. In order to retrieve the original swing, an efficient receiver circuit is required which can add to the complexity of the low swing scheme and can occupy a large area overhead. In addition, the reduced voltage swing increases the delay through the long interconnect wires. Therefore, extra strong drivers are needed to drive the high capacitance nodes in order to maintain the required speed. As mentioned before, a strong driver circuit which can produce a low signal swing without the requirement for additional circuitry or a complicated receiver circuit is incorporated in the diode-connected configuration used in the MJ driver circuit. Therefore it is essential to understand the concept of diode-connected configuration first in order to design a new and improved version of the MJ driver.

A. Diode-connected configuration

In the diode-connected configuration the drain terminal of a device is shorted to the gate terminal, subsequently the drain saturation current, I_{dsat}, which flows through the *MOSFET* device increases exponentially with the increase in the output voltage. The diode-connected configuration for both *NMOS* and *PMOS* devices are as shown in Figure 3.4(a) and the I-V

characteristics for n-channel device is shown in Figure 3.4(b). The I-V characteristics for this configuration are qualitatively similar to a p-n junction diode or *MOS* diode, which is mostly used as a component in a current mirror or a means of creating a voltage drop in level translation circuit.



(a) (b)

Figure 3.4: Diagrams of (a) diode-connected configuration for *CMOS* devices and I-V characteristics for n-channel diode-connected configuration [10].

The I-V characteristic of the *MOS* device is described by the large signal equation for drain current in saturation as in Equ.3.11. The connection of the gate to the drain guarantee operation in the saturation region, which means that V_{ds} is in charge of I_D and thus, the channel transconductance becomes a channel conductance.

$$I_D = \left(\frac{k'W}{2L}\right)\left(V_{gs} - V_{th}\right)^2 = \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2 \qquad (3.11)$$

The nature of this configuration is that it is able to control the output to a certain voltage level and not allow that voltage to increase beyond a given limit. Basically it compresses the input voltage into a smaller output voltage; hence a low swing signal is produced. At low voltage levels, I_{dsat} can be reduced significantly to freely change the value of the output voltage with little or no impedance loading [11]. For deep submicron processes, the resistivity of the interconnect is significant and over-driving the interconnect by actively driving the interconnect beyond the low swing limits will help in decreasing the propagation delay [12]. The amount of over-drive is determined by proper transistor sizing.

B. Low-swing driver application

As mentioned previously, the diode-connected configuration is used in current mirror circuits and additionally, due to its nature in limiting voltage output to a certain level, it can also be applied as a high-to-low voltage level converter, which is essential in low-swing driver circuits. The concept of a diode-connected configuration incorporated in the MJ driver, was adapted from an Up-Down Low Swing Voltage Driver (*UDLD*) [2] shown in Figure 3.5, where the output voltage swing is based on the value of the threshold voltage, *Vth*. However in the MJ driver the resulting symmetrical output swing is between *Vthp* and *Vdd–Vthn*.

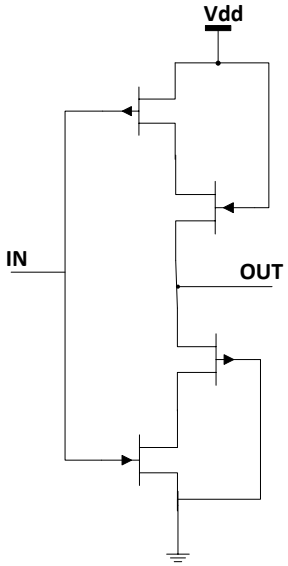


Figure 3.5: Circuit diagram of the UDLD driver [2].

Another adaptation of this driver configuration is a dynamic diode-connected driver which is presented in Figure 3.6. The dynamic diode-connected (*DDC*) driver is similar to the MJ driver in terms of its advantages compared to other low-swing drivers as it does not require any additional circuitry or power supplies to provide efficient power and delay performances. The DDC driver comprises 4 output transistors (*DDC-P, DDC-N*) which switch in three different modes; active, diode-connected and turn-off. When the DDC driver is turned on or in active mode, it provides a high drive capability to quickly charge or discharge the interconnect. When the transistors are switched to diode-connected mode, the voltage swing on the interconnect is limited, which offers lower impedance than the source follower giving improved noise immunity. The DDC driver is compared with a conventional *CMOS* driver in [3] in terms of energy consumption, delay and noise immunity. As expected, the DDC driver excelled in lower energy consumption and delay compared to the conventional *CMOS* driver

but due to its sensitive nature to variations in power supply, device parameters and loading condition, its noise immunity is 36% less compared to the conventional *CMOS* driver.

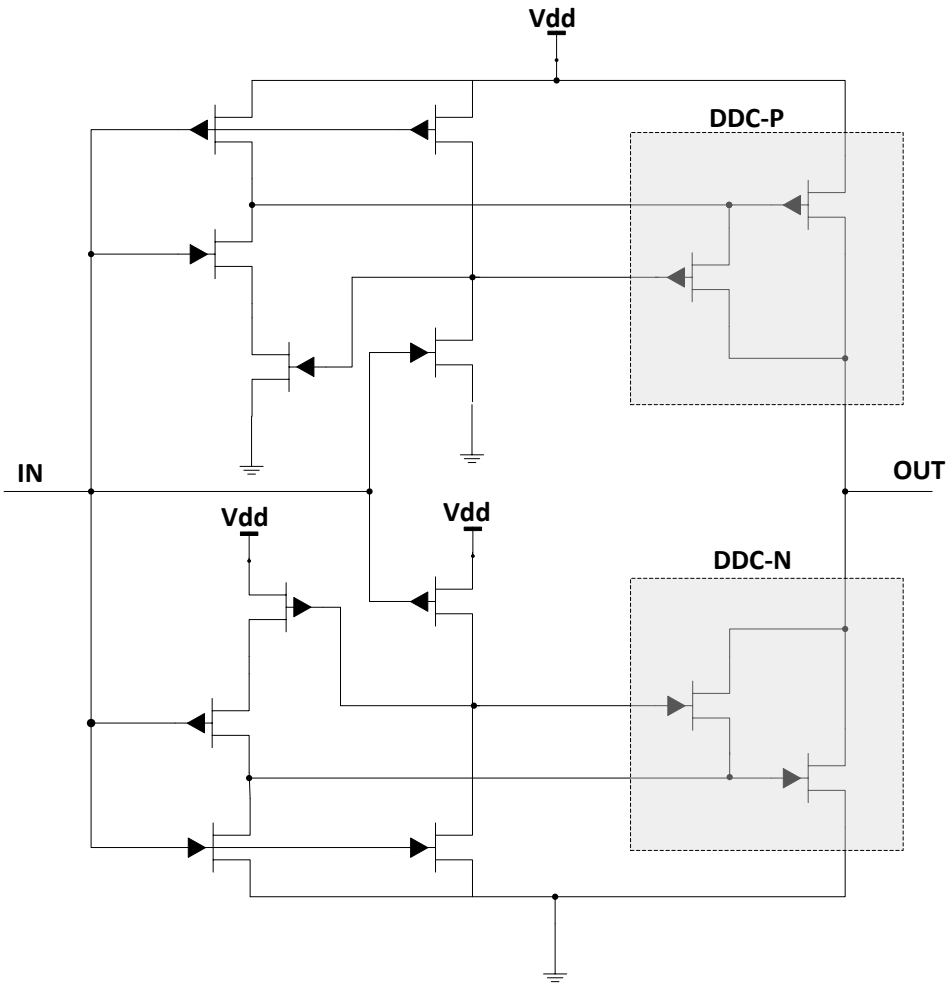


Figure 3.6: Circuit diagram of the DDC driver [3].

As mentioned previously, the MJ-driver also incorporates diode-connected configuration which has several advantages over other low-swing driver circuits [3], [9], [13-16]. The name MJ originates from the driver's designer called Juan A. Montiel-Nelson. The MJ driver is said to have better energy-delay performance compared to the DDC driver as it provides a larger driving current during the logic transitions. It also provides improvement in terms of robustness and sensitivity to power supply variation [1].

The MJ driver shown in Figure 3.7 relies on a multipath technique which includes a feedback inverter, G6, and two feedback paths at gates G2, G3, G7 and G8. The multipath technique involves only one operational path during each transition. This means the upper half of the driver is only operational during the rising transition while the lower half is active during the falling transition. However, with the use of the multipath technique, the MJ driver is

considered to be redundant in terms of area as only half of the circuit is needed to be operational during each rising and falling transition.

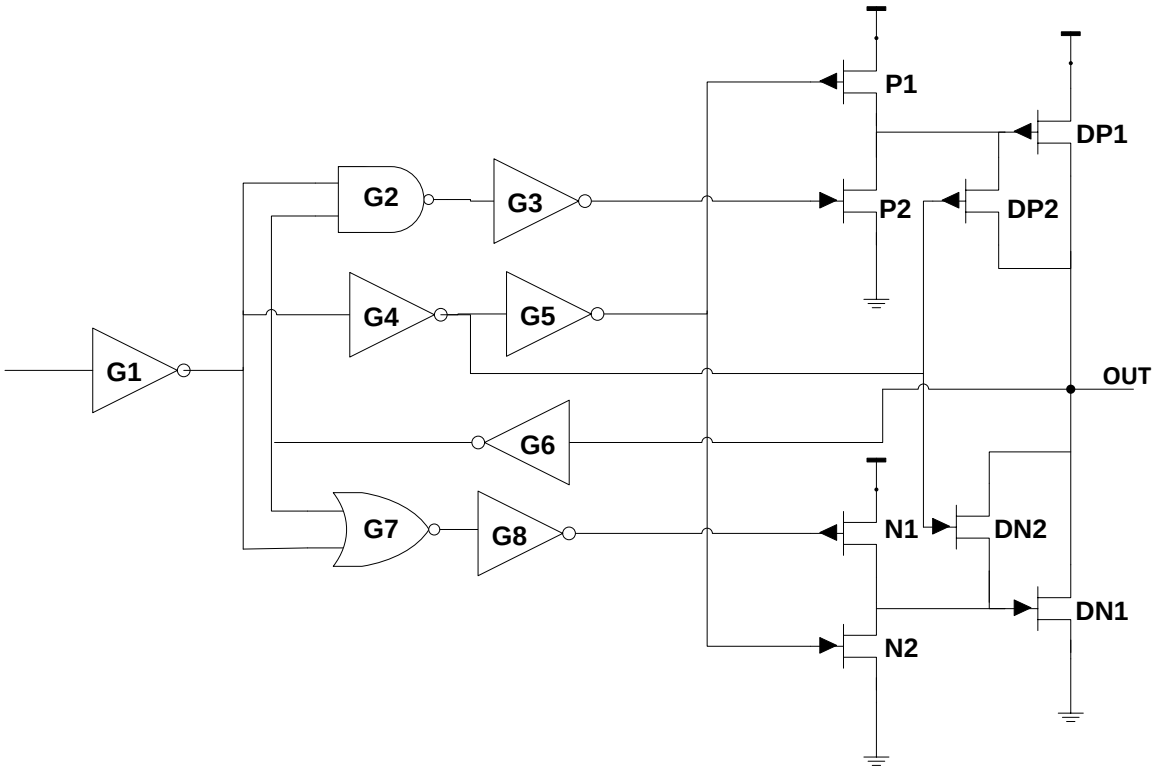


Figure 3.7: Circuit diagram of the MJ driver [1].

Consequently the objectives of any new design, whilst maintaining the low voltage swing capability of the MJ driver must not only eliminate its disadvantages but also reduce the power consumption and propagation delay of the circuit. These objectives can be achieved through the nLVSD driver shown in Figure 3.8, and also the mLVSD driver shown in Figure 3.10. Both names are obtained through designer's initial N and M. Both drivers are similar to the MJ driver in terms of their use of diode-connected configuration but the MJ driver is lacking in some aspects. This is further explored where the nLVSD driver is firstly discussed which is followed by the mLVSD driver.

Although the nLVSD driver design is based on the MJ driver, it differs as seen in Figure 3.7 and Figure 3.8, in its simplicity which results in a smaller footprint. The nLVSD driver employs similar diode-connected transistor pairs at the output but instead of their inputs depending on the output of the feedback inverter and the two feedback paths, the inputs of the diode-connected transistor pairs (*LP2, P2D, LN2, N2D*) in the nLVSD driver are symmetrically switched to be controlled by a set of drivers, INV4 and INV5. INV4 is an

upsized driver while INV5 is a downsized driver, which limits the maximum voltage level at *Vpy* and the minimum voltage level at *Vny*. The values of *Vpy* and *Vny* can be adjusted by changing the size of both drivers. The voltage swing of the MJ driver is measured between *Vdd-Vth* and *Vth* but a lower swing can be achieved by the nLVSD driver through INV4 and INV5 drivers as it swings between *Vpy-Vth* and *Vth-Vny*, where *Vpy* <*Vdd* and *Vny* >*GND*. Subsequently, lower power consumption can be achieved through the nLVSD driver. This circuit also differs from the MJ driver as both paths, i.e. (*INV3, NAND, INV4*) and (*INV3, NOR, INV5*) are active at the same time during both logic transitions. Consequently every component is active or involved for every transition, minimising possible noise as both paths are switching in the same direction; and minimizing leakage power as each component is actively switching to avoid any static power. Additionally, the implementation of the diode-connected transistor pairs at the output provides a larger driving current during the switching transitions, which results in faster signalling and better energy-delay-product.

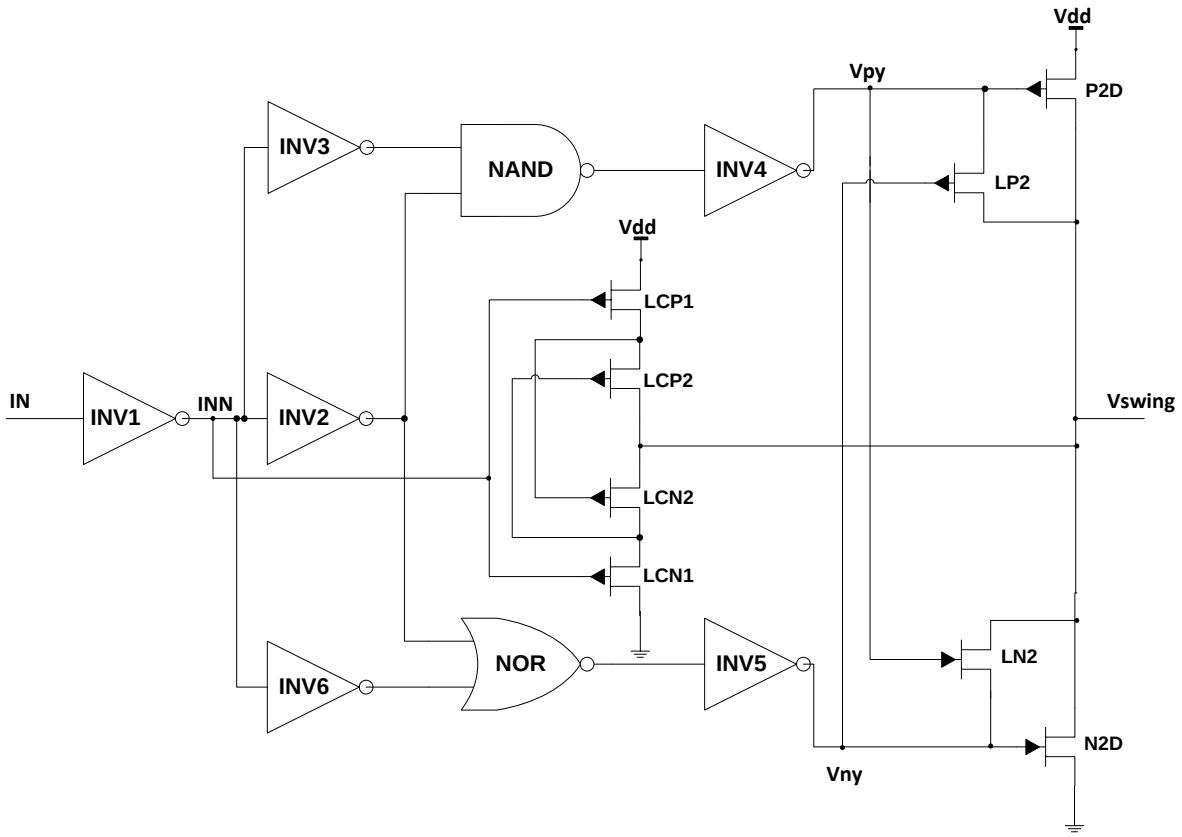


Figure 3.8: Circuit diagram of the nLVSD driver.

In order to cancel out the leakage current effects and improve the noise immunity, a leakage control transistor [17] is placed at the driver output. The leakage control transistors LCP2 and LCN2, function by controlling the gate terminal of one transistor, by the source of the other.

For any input combination, one of the leakage control transistors is always near the cut-off voltage which consequently increases the resistance of the path from *Vdd* to ground, subsequently leading to a decrease in the sub-threshold leakage currents. Transistors LCP1 and LCN1 are used to provide direct static path between the input and output of the driver when the input is stable or no transition activity is detected. These devices (*LCP1, LCP2, LCN1, LCN2*) provide an efficient mechanism to minimise the leakage current without affecting the delay and power consumption. Initially, without the leakage control device, the nLVSD driver has a comparable lower leakage power compared to the dynamic power consumption. Additionally, it can increase robustness and reliability of the driver. This results in the increase in transistor count, which amounts to the same transistor count as the MJ driver. However, since minimum sized transistors are used for the leakage control device, the nLVSD driver has approximately 50% smaller area than the MJ driver. This is shown in Table A1.5, in Appendix I, where the total active areas for all diode-connected drivers, which are to be evaluated, are recorded. The channel widths for transistors in the diode-connected drivers; namely, the nLVSD, mLVSD, DDC and MJ drivers are also recorded in Appendix I. The technology used for the transistors are from UMC CMOS 90nm with BSIM4V4.3.0 (Cadence SPECTRE v.5.0.33) model. The circuit netlist for the nLVSD and mLVSD drivers are also included in Appendix I. The active areas as well as the channel widths for the drivers as well as the receiver have been optimized based on their energy-delay performances, which are calculated for a 10mm interconnect.

The circuit operation of the nLVSD driver is best explained in terms of its signal voltage waveforms as shown in Figure 3.9, where they are obtained through Cadence Virtuoso Analog Design Environment.

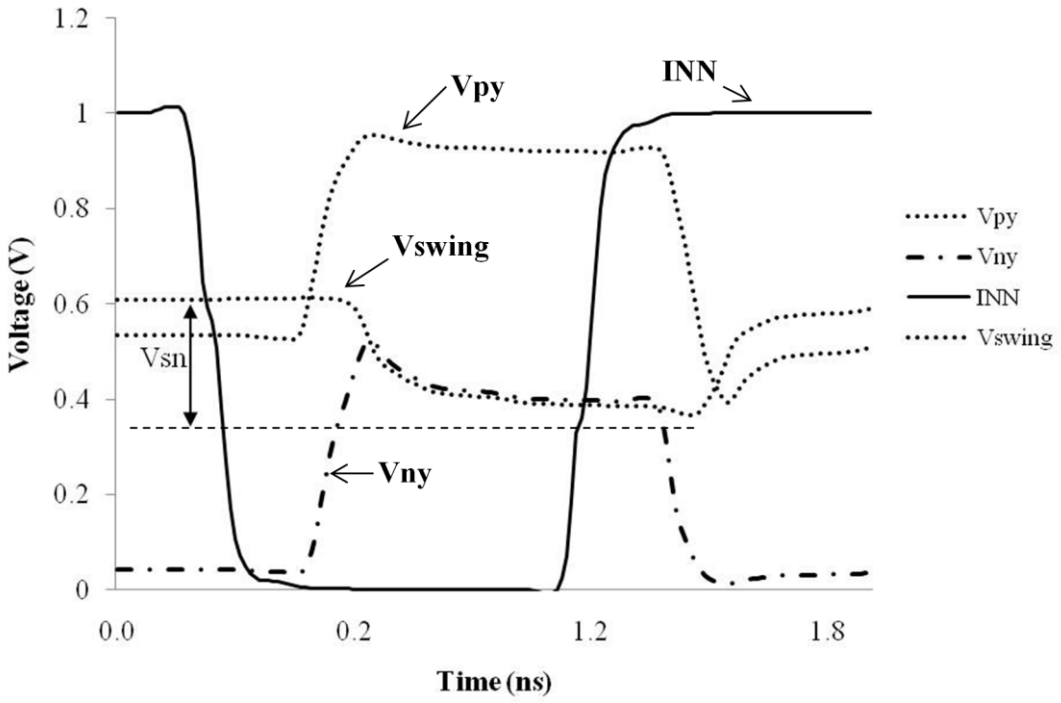


Figure 3.9: Signal waveforms of the nLVSD driver.

As been mentioned before, INV4 and INV5 are sized to provide a maximum voltage of *Vpy* and a minimum voltage of *Vny*. In this case, the sizes of INV4 and INV5 are configured so that *Vpy* swings from *Vdd/2* to *Vdd* and *Vny* from *Gnd* to *Vdd/2*. As INN is set to '1', *Vpy* and Vny are set at *Vdd/2* and *Gnd*. *Vpy* will not fully turn on LN2, making it slowly discharge, however *Vny* will fully turn on LP2, making the output voltage swing to approximately *Vpy*. When INN switches from high to low, *Vpy* and *Vny* rise to *Vdd* and *Vdd/2* respectively. This will turn on LN2 and turn off P2D. As INN approaches '0', LN2 will slowly discharge while N2D holds the charge as *Vny* has not yet reached beyond the threshold voltage in order to activate it, creating a slow discharge at the output. Finally as INN reaches '0', *Vny* reaches beyond the threshold to activate N2D and LN2 is fully activated through *Vpy*, which creates a diode-connected configuration at the output giving the output value of *Vthn*. For a rising input transition, the same sequence is applied where the output swing of $Vsn = Vdd - |Vthp|$ is obtained. During the operation of the nLVSD driver, the leakage control transistors do not play a significant role other than reducing the leakage power, which in this instance is 10% compared to MJ driver.

From Figure 3.9 it is seen that this circuit has the limitation of producing a very low amplitude voltage swing, this can have a significant effect on its noise immunity as most noise components are dependent on the size of the voltage swing. Therefore, a new diode-

connected driver is proposed which improves in terms of the amplitude of the signal swing and provides an efficient energy-delay performance, including low leakage power consumption, and most importantly, with higher noise immunity. The new low-swing driver is known as the mLVSD driver, as shown in Figure 3.10. The mLVSD driver will still incorporate all of the essential components of diode-connected driver as in the nLVSD circuit except for the leakage control transistors, which will be replaced with a pair of pass transistors, connecting the input to the output through the diode-connected transistors pairs. The leakage power consumption for this driver is expected to be as low as the nLVSD driver as the pass transistors also provide a direct connection from the input to the output of the driver. The voltage swing of the mLVSD driver is higher compared to the nLVSD driver (*Vsm* > *Vsn*) since the output voltage swing is no longer dependent on INV4 and INV5, or limited by the value of *Vpy* and *Vny*, but instead follows the changes in the input to the pass transistor pairs. Thus the output swing will no longer range from *Vpy*-*Vth* and *Vth*-*Vny* but encapsulates the same voltage swing range as the typical diode-connected driver, e.g. UDLD circuit, which is from *Vthn* to *Vdd*-|*Vthp*|.

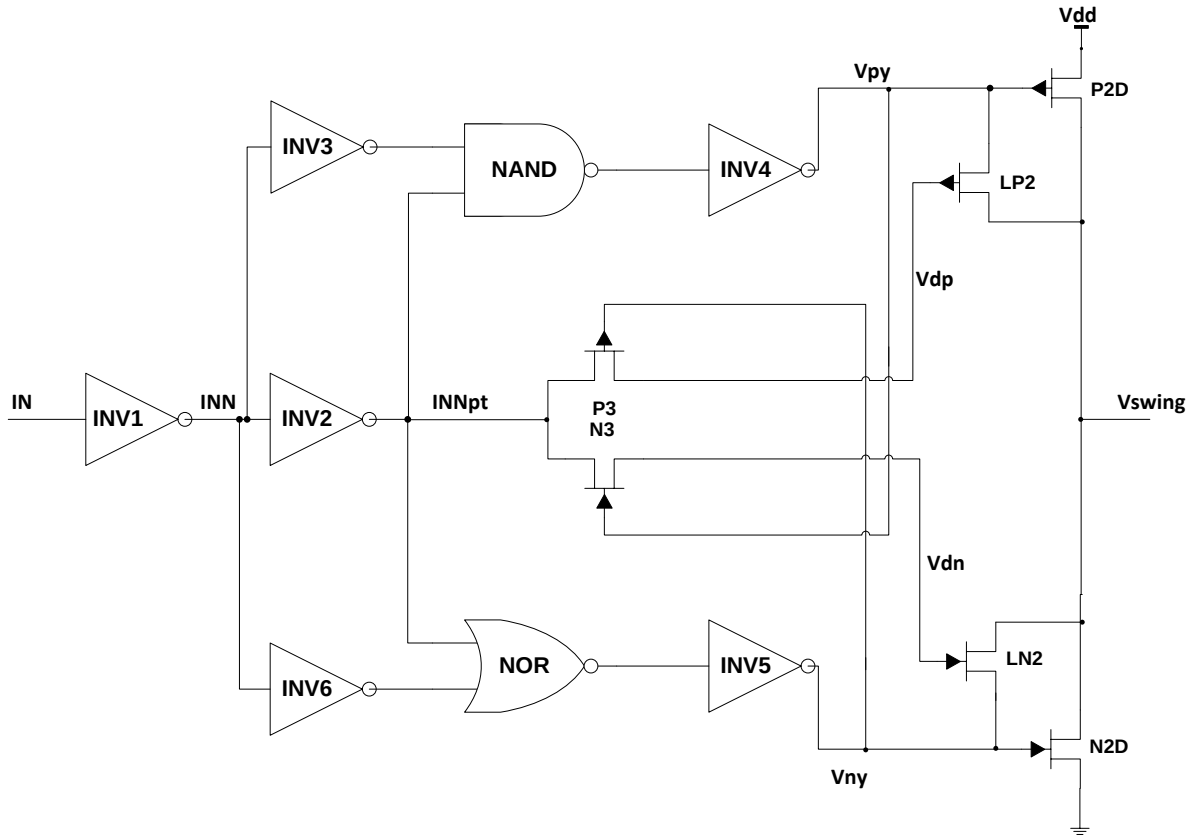


Figure 3.10: Circuit diagram for the mLVSD driver.

Even though the circuit structure of the mLVSD driver is similar to the nLVSD driver especially at the diode-connected transistor pairs, there is an increase in the amplitude of the output voltage swing (*Vsm*) as can be observed from Figure 3.11. The signal waveforms in Figure 3.11 indicate that the output voltage swing is still symmetrical similar to the waveforms of the nLVSD driver but the output transistors will only be diode-connected when INN is '0' giving the voltage swing a magnitude of *Vthn*. The p-channel diode-connected transistor pairs will never be diode-connected as its input will never reached below the threshold voltage, thus resulting in an output signal swing of magnitude *Vdd/2*. Thus, the output swing is smaller than the UDLD and DDC drivers but higher than the nLVSD driver.

In order to fully understand the changes in the circuit operation of the mLVSD driver, signal waveforms in Figure 3.11 are used to highlight the difference between the mLVSD and nLVSD drivers in terms of its voltage swing. These signal waveforms are also obtained through Cadence Virtuoso Analog Design Environment. When INN = 0, *Vny* swings to *Vdd/2* which activates N2D as it is above the threshold value. The n-channel pass transistor is turned on as *Vpy* = *Vdd*, which activates LN2 as *Vdn* = INNpt = 1. Since both LN2 and N2D are activated, the diode-connected configuration is formed at the output, providing an output voltage of *Vthn*. During a rising transition, INNpt approaches 0, which causes *Vny* to change from *Vdd/2* to *Gnd*. This also shows that *Vdn* and *Vdp* decrease with INNpt. When INNpt reaches 0 as INN =1, *Vny* = 0 activate the p-channel pass transistor providing *Vdp* with value of |*Vthp*| while *Vpy* switched from *Vdd* to *Vdd/2*. Both LN2 and N2D are turned off while P2D cannot be completely turned on as *Vpy* is not low enough and will never be fully turned on since *Vpy* only swings from *Vdd/2* to *Vdd*. This results in the output with a magnitude of *Vdd/2* as only LP2 is turned on, and not equal to *Vdd*-|*Vthp*| as the output is not diode-connected.

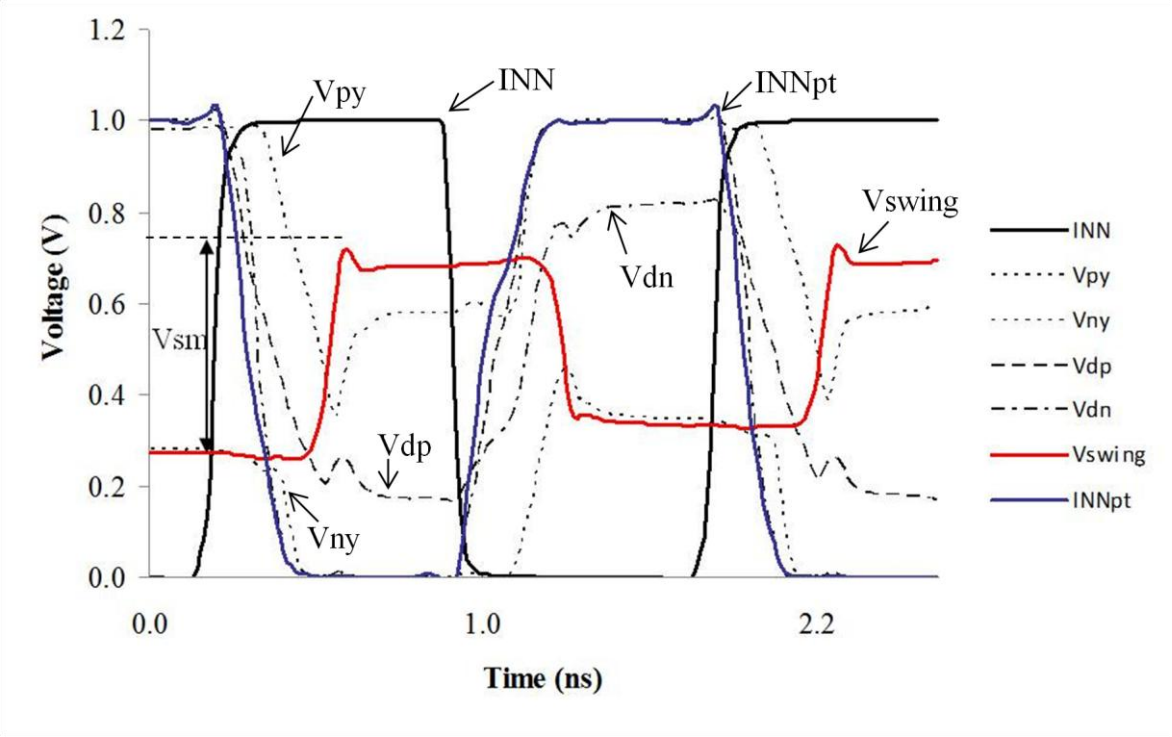


Figure 3.11: Signal waveforms of the mLVSD driver.

3.3.2. The on-chip interconnect model

New diode-connected drivers have been proposed and detail descriptions of their structures have also been discussed. However, the driver alone will not be enough to design a low power and high speed signalling scheme. Additionally, an effective interconnect model is required in order to perform timing and signal integrity analyses; the model needs to encapsulate the electrical parameters of the interconnect layout and technology information such as the width and length of the interconnect, and related dielectric parameters. The electrical parameters are necessary so that they can be combined with other circuit components for overall performance evaluation. In practice these can be obtained through parasitic extraction.

The interconnect can be presented by an *RC* or *RLC* equivalent circuit. Since interconnect inductance is usually negligible at low clock speeds, on-chip interconnect is modelled only with *RC* components. However, as the circuit operation reaches gigahertz range, the inductance effect becomes more significant in signal integrity analysis such as signal overshoot and reduced slew rate. On the other hand, by incorporating interconnect inductance into the model the subsequent computation becomes very expensive. Therefore, it

is important to only include interconnect inductance when it is necessary. The importance of L can be determined by evaluating the following time constants [8]:

1. Driver input signal slew rate, t_r
2. Time of flight for a transmission line, $t_f = Length.\sqrt{LC}$
3. Elmore delay for an RC line, $t_e = RC/2.(Length)^2$

Interconnect should be modelled as an RLC line if it satisfies the following conditions [18], [19]:

1. $t_f > t_e$: In this condition, the inductance effect will lead to a longer signal delay.
2. $t_r < 2t_f$: $2t_f$ is the time required for a signal to travel the round trip from the driver to the end of the line, which implies that when the switching is fast enough, the signalling is affected by the reflected signal.

Although, inductance effects are increasingly significant for modelling on-chip interconnects, the RC equivalent circuit is still sufficiently accurate to model the majority of situations. Thus, for this work, only the RC equivalent circuit is employed in timing and signal integrity analyses in evaluating the performances of diode-connected driver schemes, giving reasonable accuracy and saving on computational time.

The conventional interconnect model usually employs a lumped RC segment however this model lacks the accuracy to model high-performance interconnect significantly with the increase in circuit operating frequency. An alternative to the lumped RC model is a distributed RC model. The distributed resistance and capacitance are approximated with a number of lumped elements, as shown in Figure 3.12. The distributed RC circuit is represented as N distributed RC lumped elements of proportionally less resistance and capacitance. As the number of segments approaches infinity, the lumped approximation will converge with the true distributed circuit.

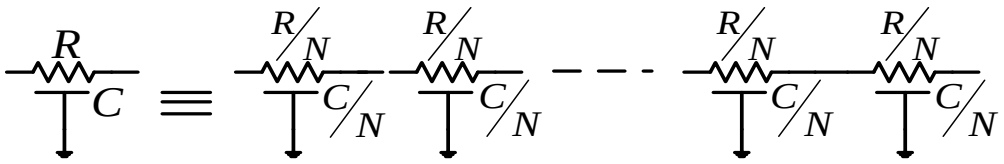


Figure 3.12: An equivalent approximation of N-segment distributed RC circuit [10].

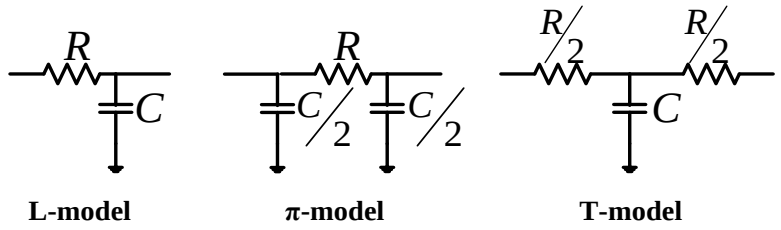


Figure 3.13: Standard approximations of distributed *RC* model [10].

There are three standard approximations to the distributed model, which are the L-model, T-model and π-model, as shown in Figure 3.13. The L-model is a poor model for distributed interconnect as it requires a large number of segments for accurate results. The π-model is preferable compared to the L-model as only a small number of segments as required, for example, three segments are sufficient to obtain approximately 97% accuracy level [6]. The T-model is comparable to the π-model but is only useful for circuits which contain more nodes and requires more time to solve [10]. Thus, it is a common practice to use the π-model for distributed interconnects, as shown in Figure 3.14.

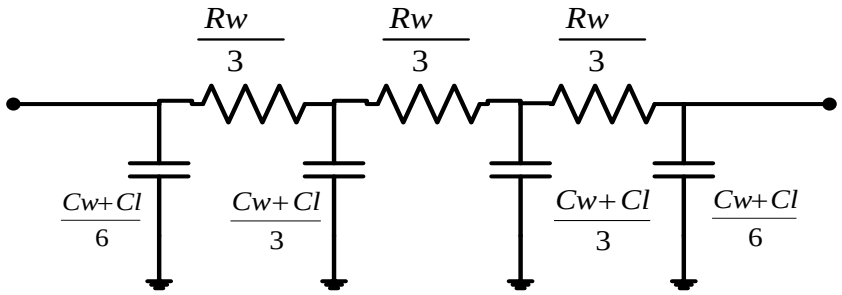


Figure 3.14: The *π3 RC* interconnect model.

The interconnect capacitance, C_w can be calculated using Equation 2.3 to 2.5 in Chapter 2, whilst the resistance can be obtained through Equ.3.12 [8].

$$R_W = \frac{\rho l_e}{wt} \tag{3.12}$$

Where ρ is the metal resistivity, l_e is the interconnect length, while w and t, are the interconnect width and thickness respectively. The interconnect model for this work is calculated to comprise a 480.6Ω resistor and a 1.745pF capacitor to represent an interconnect length of 10mm using nominal values of interconnect parameters recorded in Table 3.1 at 90nm technology. An extra load capacitance, *Cl* of 0.25pF per mm length of interconnect is distributed along the wire to represent the fan-out.

Table 3.1: Nominal values of interconnect parameters.

Parameters	Nominal values
Interconnect width, w	0.56μm
Interconnect thickness, t	0.81μm
Interlayer Dielectric height, h	0.94μm
Metal resistivity, ρ	21.8nΩ.m
Dielectric permittivity, k	3.25

3.3.3. The low-swing level converter receiver

Receivers usually comprise 2 stages; the first stage consists of a signal conditioning or sampling circuit while the second stage provides the gain. The second stage which provides the gain needed by the system is usually carried out by a clocked regenerative amplifier; however simple inverter chain can also be used at this stage.

The low-power high-speed level restorer used for signal conditioning is a device which resembles a Schmitt Trigger, as shown in Figure 3.15. This level converter has the same characteristics as the Schmitt Trigger and provides a fast signal detection speed compared to a standard inverter. The Schmitt Trigger receiver, also known as the ScTr level converter, can turn a slowly varying input signal into a clear digital output signal. It provides a significant improvement in terms of delay and power consumption due to its fast transitions at the output by suppressing the direct-path currents. Even though it consumes slightly more area than a simple inverter, better power and delay performance is readily traded off against a small increase in area. The Schmitt Trigger receiver is followed by a simple inverter chain to provide gain for the scheme. The inverter chain is minimally sized. The receiver inverters are implemented with a channel width $Wn = 0.27\mu m$ and $Wp = 0.81\mu m$.

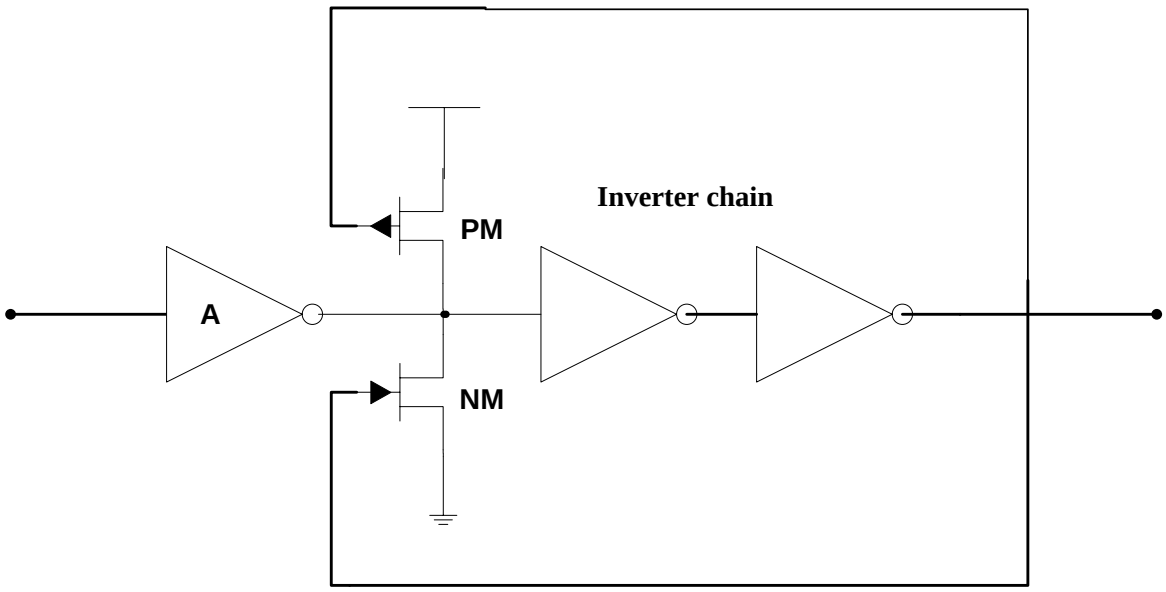


Figure 3.15: The ScTr level-converter configuration.

The input to inverter A is the output of the level converter. When the input equals 0, the feedback loop biases the PMOS transistor (*PM*) in the conductive mode while NMOS transistor (*NM*) is off. The input signal effectively connects to an inverter consisting of a pull-up network of PM and PMOS device of inverter A whilst the pull-down network comprises only the NMOS device of inverter A. This results in changes in the effective ratio of the level converter, where the switching threshold is moved upwards. When the input switches, NM is activated while PM is turned off. The extra pull-down device provided by NM speeds up the transition and thus provides a sharp output signal, thus resembling the operation of a Schmitt Trigger, it is very useful in an noisy environment, thus improving the reliability of the nLVSD driver scheme.

3.4. Performance Analyses To Be Undertaken

In order to address the efficiency of the proposed driver schemes their performances in terms of speed and power consumption, as well as EDP and leakage currents are tested against several design parameters such as the interconnect length, supply voltage, operating temperature and frequency. The noise analysis will be included in order to compare the signal to noise ratio between the driver schemes. These analyses will be undertaken on the DDC, MJ, nLVSD and mLVSD driver schemes. When performing the timing and signal integrity analyses the overall circuit shown in Figure 3.16 is used.

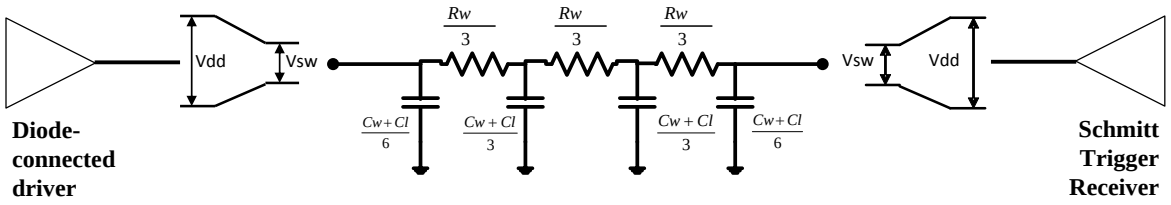


Figure 3.16: An implementation of driver schemes for performance analysis.

3.4.1. The Power and Performance Analysis of the Low-Swing Signalling Schemes

The performance of the driver schemes will be analysed and compared with respect to the main design parameters, namely delay, power consumption, EDP, leakage currents, area overhead and signal to noise ratio. The four schemes will incorporate the same *Vdd*, operating frequency and interconnect structure. It is assumed that *UMC 90nm CMOS* process is used to implement the design. The interconnect is implemented in Metal 1 layer for these analyses.

This analysis will be performed by increasing the length of the interconnect, from 1 to 10mm, between the driver and receiver and repeating the signal delay and power consumption calculations. It is expected that by increasing the interconnect length, the signal delay will also be increased as delay is dependent on the interconnect length as shown in Equ.3.3. The signal delay is also dependent on the driver strength, which is due to the high driving current of the driver. An efficient line driver will be able to propagate a signal at a high speed on long interconnects without increasing the size of the driver.

3.4.2. Comparison Analysis of the Leakage Currents for the Low-Swing Signalling Schemes

For submicron technologies, the dominant leakage mechanism is the sub-threshold leakage current, which needs to be addressed as the low-swing signalling schemes used in this work are implemented using 90nm technology where leakage currents are increasingly becoming more significant. Consequently, circuit temperature is linearly dependent on the power consumption, as it increases when power consumption is high. Since the leakage current increases with the increase in temperature, thus the comparative analysis involving leakage currents is carried out to the effects of temperature. Thus for this analysis, the leakage currents of the low-swing signalling schemes; namely, the nLVSD, mLVSD, DDC and MJ driver schemes are measured for a range of temperatures from 12°C to 55°C.

3.4.3. Noise Analysis Comparison of Low-Swing Signalling Schemes

Noise analysis is important in designing a low-swing signalling scheme as it is expected to have higher noise due to the low noise margin. However, if any mismatch between the driver and the receiver, in terms of process parameters such as the threshold voltage, can be reduced or avoided, better noise immunity can be achieved with high signal to noise ratio. However, increases in power consumption can significantly affect the signal integrity as it causes deviation of a node voltage from its nominal value, increasing the possible mismatch between the driver and receiver.

3.5. Summary

This chapter has introduced the concept of diode-connected configuration which has been applied to several low-swing drivers such as the UDLD, DDC and MJ-drivers. The advantages and disadvantages of these drivers were discussed, leading to the design of the nLVSD and mLVSD drivers. Both of these drivers incorporate diode-connected configurations at the output, in order to achieve low power and high speed performance. Additionally, both proposed drivers also have smaller areas compared to the existing diode-connected drivers even though they incorporate leakage control mechanism in their driver circuits. Leakage control transistors are implemented in the nLVSD driver circuit whilst the mLVSD driver incorporates a pair of pass transistors providing direct static paths between the input and output of the drivers when the input is stable or no transistor activity is detected. The mechanism aids in further reducing the leakage current of the low-swing signalling schemes. Subsequently, the configuration used in the mLVSD driver results in a higher amplitude output signal swing compared to the nLVSD. Due to its lower voltage swing, the nLVSD driver is expected to consume less power than the UDLD, DDC and MJ drivers but negatively affects its noise immunity capability due to the reduced noise margin. Therefore, the mLVSD driver is introduced which has a higher voltage swing compared to the nLVSD driver but lower than that of the UDLD, DDC and MJ drivers.

In order to analyze the performance of these diode-connected drivers, similar interconnect model and receiver design will be used. A distributed π-model for interconnect and a Schmitt Trigger level converter are introduced. Different type of analyses are also introduced in preparation for performance analyses of the DDC, MJ, nLVSD and mLVSD driver schemes

against wire length, supply voltage, operating temperature and frequency, and noise. The overall results will be discussed in Chapter 6 where the proposed driver schemes are expected to have better performance compared to other diode-connected driver schemes.

In this chapter, the effect of crosstalk is not yet considered. In order to design an efficient low-swing interconnect scheme, every aspect of interconnect problems needs to be considered. Therefore, in the next chapter, background review on crosstalk is introduced which includes problems associated with crosstalk and possible methods in mitigating these problems. Chapter 4 will also discuss the effect of crosstalk on the diode-connected driver scheme in on-chip signalling application.

References

[1] J. C. Garcia, J. A. Montiel-Nelson, and S. Nooshabadi, "Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects," *IEEE International Symposium on Circuits and Systems, ISCAS 2007*, pp. 881-884, 2007.

[2] A. Rjoub and O. Koufopavlou, "Efficient drivers, receivers and repeaters for low power CMOS bus architectures," in *The 6th IEEE International Conference on Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99.*, 1999, vol. 2, pp. 789-794 vol.2.

[3] M. Ferretti and P. A. Beerel, "Low swing signaling using a dynamic diode-connected driver," *Proceedings of the 27th European Solid-State Circuits Conference. ESSCIRC 2001*, pp. 369-372, 2001.

[4] L. Zhang, J. M. Wilson, R. Bashirullah, L. Luo, J. Xu, and P. D. Franzon, "Voltage-Mode Driver Preemphasis Technique For On-Chip Global Buses," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 15, no. 2, pp. 231-236, 2007.

[5] C. Piguet, "Low-Power Electronics Design," in *Computer Engineering*, 1st ed., V. Oklobdzija, Ed. Switzerland: CRC Press, 2005, pp. 159-161.

[6] T. Sakurai, "Approximation of wiring delay in MOSFET LSI," *Journal of Solid State Circuit*, vol. 18, no. 4, pp. 418-426, 1983.

[7] A. C. J. M. Rabaey Borivoje Nikolic, *Digital Integrated Circuits*, 2nd ed. Prentice Hall, 2003.

[8] B. P. Wong Mittal Anurag, Cao, Y., Starr, G., *Nano-CMOS circuit and physical design*. John Wiley & Sons, 2005.

[9] H. Zhang, V. George, and J. M. Rabaey, "Low-swing on-chip signaling techniques: effectiveness and robustness," *IEEE Trans. Very Large Scale Integrated System*, vol. 8, no. 3, pp. 264-272, 2000.

[10] N. H. E. Weste Harris, D., *CMOS VLSI Design: A Circuit and Systems Perspective*. 2005.

[11] D. A. Johns and K. Martin, *Analysis Integrated Circuit Design*. John Wiley & Sons, 1997.

[12] C. Kwon, K. M. Rho, and K. Lee, "High Speed and Low Swing Interface Circuits using Dynamic Overdrive and Adaptive Sensing Scheme," *International Conference on VLSI and CAD*, pp. 388-391, 1999.

[13] A. Tajalli and Y. Leblebici, "A power-efficient LVDS driver circuit in 0.18um CMOS technology," *Research in Microelectonics and Electronics Conference, PRIME 2007*, pp. 145-148, 2007.

[14] L. Zhang, J. Wilson, R. Bashirullah, L. Luo, J. Xu, and P. Franzon, "Driver pre-emphasis techniques for on-chip global buses," in *Proceedings of the 2005 International Symposium on Low Power Electronics and Design, ISLPED '05*, 2005, pp. 186-191.

[15] H. Song, S. Kim, and D.-K. Jeong, "A reduced-swing voltage-mode driver for low power multi-Gb/s transmitter," *Journal of Semiconductor Technology and Science*, vol. 9, no. 2, pp. 104-109, 2009.

[16] M. Hiraki, H. Kojima, H. Misawa, T. Akazawa, and Y. Hatano, "Data dependent logic swing internal bus architecture for ultra low power LSI's," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 4, pp. 397-402, 1995.

[17] N. Hanchate Ranganathan, N., "LECTOR: A technique for leakage reduction in CMOS circuits," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 12, no. 2, pp. 196-205, 2004.

[18] A. Deutsch et al., "When are transmission line effects important for on-chip interconnections," *IEEE Trans. Microwave Theory Tech.*, vol. 45, no. 10, pp. 1836-1846, 1997.

[19] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figure of merit to characterize the importance of on-chip inductance," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 7, no. 4, pp. 442-449, 1999.

Chapter 4

ANALYSIS OF THE ROBUSTNESS OF LOW-SWING SIGNALLING SCHEMES TO EXTERNAL DISTURBANCES

4.1. Background

The reliability of electronic system has become a major issue as the advances in semiconductor technology continually reduce devices dimension. As device geometries shrink circuit packing densities increase and circuit application become more susceptible to transient and intermittent faults caused by, for example, crosstalk, noise and the effects of neutron and alpha-particle strikes. Crosstalk problems have increased due to higher packing densities of devices and interconnect, changes in the aspect ratio of interconnects and reduced supply voltages. Increases in the susceptibility to effects of particle strikes (*single event upsets*) have resulted from the reduction in node capacitances. Transient and intermittent faults are classified as non-permanent faults as they are created by temporary changes in environmental conditions; this is in contrast to permanent faults resulting from irreversible physical changes in the structure of a circuit due, for example, to shorted or open interconnect.

Several studies have shown that the non-permanent faults are the pre-dominant cause of malfunctions experienced by present day computer systems [1]. It is considered that these faults may account for 80% or more of the failures in digital systems [2,3]. With the introduction of new technologies in order to achieve low power and high performance with low cost or area, the problem with the non-permanent faults is becoming more significant. Consequently in this work, in order to assess the reliability of low-swing signalling schemes, it is necessary to consider the main factors that can affect the signal integrity of the interconnects. It is important to include the reliability analysis with respect to occurrence of non-permanent faults early in design stage to improve system robustness and explore the subsequent tradeoffs [4].

The chapter begins with a brief introduction to the types of temporary faults which can occur in *VLSI* circuits, namely transient faults and intermittent faults, caused by, for example, *SEU* and crosstalk respectively. The methodology adopted for the analysis of each type of fault is

subsequently discussed followed by the results and discussion of the analysis of the effects of *SEU* and crosstalk on the performance of low-swing signalling schemes.

4.2. Temporary Faults

Faults in *VLSI* circuits can be classified as either permanent faults, which affect the functionality of the circuit permanently such as short or open interconnect; and non-permanent faults, which occur randomly and are temporary. A non-permanent fault is a non-destructive fault and falls into one of two categories [5]:

a) Transient fault, which is caused by environmental conditions such as temperature, voltage fluctuation, cosmic rays and alpha particles.

b) Intermittent fault, caused by non-environmental conditions such as loose connections, critical timing, power supply noise, resistive or capacitive variations or couplings and noise in the system.

Recent studies [6] have shown that the likelihood of the appearance of transient and intermittent faults is growing in systems manufactured using deep submicron technologies. Subsequently, the likelihood of these faults due to process variations is also growing, which is the reason that they are becoming important reliability concerns for future technology nodes. It is known that single event upsets from transient faults have emerged as a key challenge in microprocessor design, resulting from a single particle hit whilst failure from intermittent faults caused by crosstalk is increasingly become a great concern as it can provide functional and timing failure to the *VLSI* circuits. Thus, in order to meet the system reliability requirements, it is necessary to consider these faults in the analysis of the robustness of a circuit.

4.3. Impact Of Transient Faults On Low-Swing Signalling Schemes

The reliability operation of *VLSI* circuits is necessary to avoid catastrophic consequences especially for system operating under adverse environmental conditions. Information in electronic circuits is stored and propagated through a collection of electrical charges [7]. Any event which upsets these charges can cause errors in the circuit output. These errors are

called transient faults, soft errors or single event upsets and arise from energetic particles, such as neutrons from cosmic rays and alpha particles from packaging material generating electron-hole pairs as they pass through a semiconductor device [8]. Higher *VLSI* integration and lower *Vdd* have been contributing factors to higher rates of occurrence of particle induced transients which results in higher soft error rates (*SER*).

Traditionally memories have been the most affected by *SEU* because small transistor sizes are used to increase memory density, resulting in lower capacitance and hence higher *SER*s [9]. However, memories can be protected by error detecting or correcting codes. Due to extensive technology scaling, it has been observed that unprotected combinational logic circuit is becoming more vulnerable to radiation-induced transient faults [10,11].

4.3.1. Single Event Upsets (*SEU*) - Introduction

An *SEU* is a radiation induced fault in an integrated circuit. The effect of an *SEU* is to change the behaviour of the digital circuits in some unexpected manner, often producing incorrect results. Since an *SEU* does not reflect a permanent failure of the device, it is termed soft or transient.

As previously mentioned, the two primary types of radiation causing this effect are alpha particles from packaging and device materials, and neutrons originating from cosmic rays. When an energetic particle strikes a sensitive area such as the area near the reverse biased drain junction in a transistor, electron-hole pairs are generated, such as shown in Figure 4.1. The amount of energy to create the electron-hole pairs is recorded at 3.6eV for silicon, where for an energy of 1MeV, the charge generated by a particle strike is 44.5fC. Since a circuit node in *90nm* technology can store between 1 to 10fC, a particle with an energy of 1MeV can alter the logic value stored on the node. This shows that with every new technology node, circuit susceptibility to the effects of particle strikes increases. The minimum energy of a particle to create a voltage transition of sufficient strength to change logic value on a node is given by Equ.4.1.

$$E_{min} = 3.6 \times Q_{crit}/q \qquad (4.1)$$

where *Qcrit*, critical charge, is the amount of charge necessary to trigger a change in the logical level.

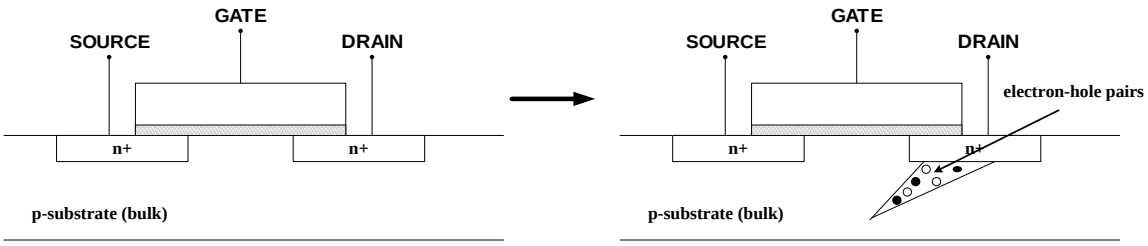


Figure 4.1: An illustration of how alpha particles strike a *MOSFET* device.

From the previous comparative analysis discussed in Chapter 3, low-swing signalling schemes have better or improved performance in terms of delay and power consumption, as well as robustness against noise. In order to ensure that the signal integrity of the low-swing signalling schemes, their reliability against any type of fault needs to be evaluated. Since radiation-induced faults such as an *SEU* have received significant attention in recent years, especially in deep submicron regime, it is important to investigate the performance of the low-swing signalling schemes using circuit design approach.

4.3.2. Measurement and Modelling of an *SEU*

Modelling of an *SEU* at the circuit level is commonly done using a current source at the impacted node and a measurement of *Qcrit*. *Qcrit* is an important parameter in measuring the *SEU* sensitivity of a circuit node [12]. In order to measure *Qcrit*, a current source is used to model the current pulse created by the ion strike. The current source is modelled in the form of double exponential waveform described by Equ.4.2.

$$I(t) = \frac{Qcrit}{(\tau_F - \tau_R)}\left[exp\left(\frac{-t}{\tau_F}\right) - exp\left(\frac{-t}{\tau_R}\right)\right] \quad (4.2)$$

This is the most commonly used model where the two timing parameters (τ_R and τ_F) representing the rising and falling time constants of the exponentials. This model has been widely used in the literature to find not only the *Qcrit* but the *SEU* introduced by ion strikes in combinational logic [13].

For this work, the most sensitive nodes on the low-swing driver need to be located, in order to place the current source, thus all nodes on the low-swing driver were tested against the *SEU*, by observing the changes in the output voltage swing. Preliminary results show that the most sensitive nodes in these circuits are located in the digital part of the low-swing drivers, which are, for example, inside the box area of the mLVSD driver circuit shown in Figure 4.2.

In this instance a current source is placed at node *A*, which is the most sensitive, therefore for other low-swing driver circuits, i.e. the nLVSD, DDC and MJD-driver, current sources are similarly placed.

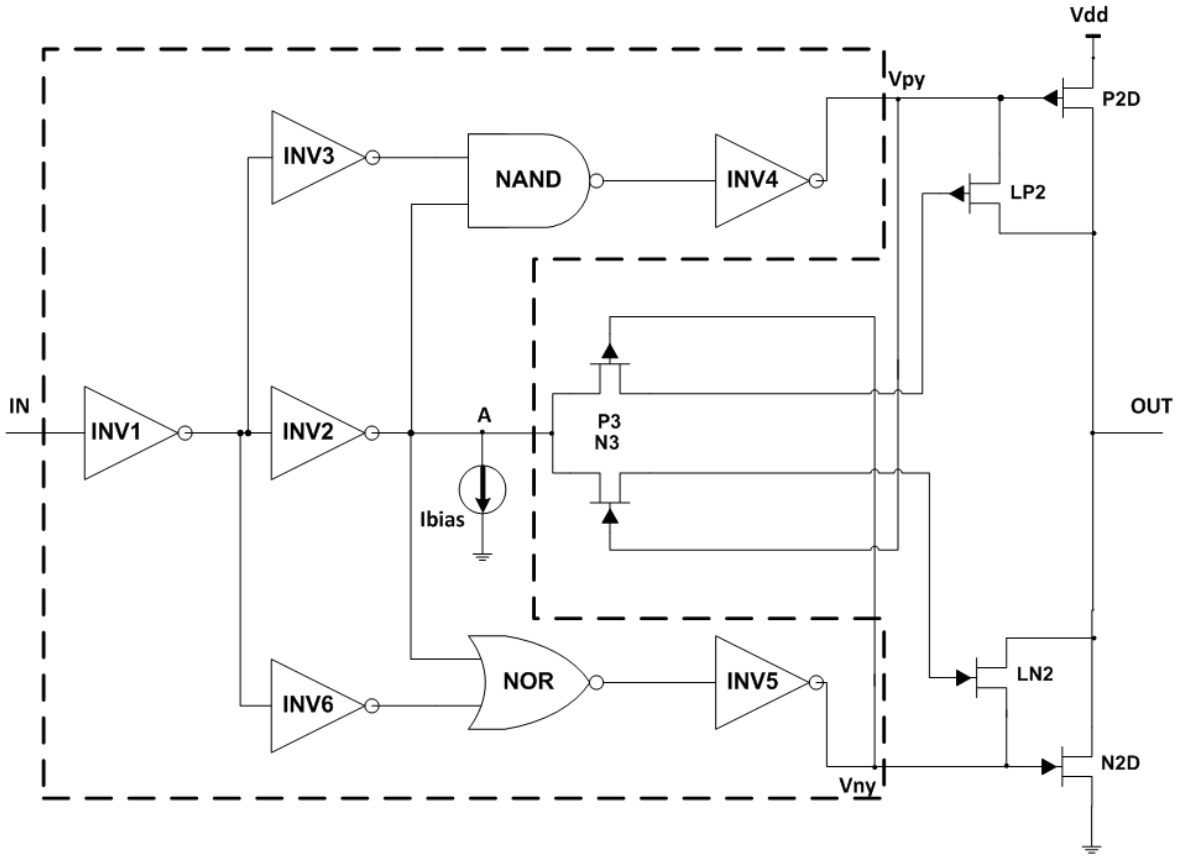


Figure 4.2: Circuit implementation of *SEU* analysis.

In order to analyse the robustness of these low-swing driver circuit against an *SEU*, the circuits are implemented in *90nm UMC* technology with the same *Vdd*, operating temperature and frequency. The sensitivity towards *SEU* is measured in terms of *Qcrit* by varying the bias current. The low-swing driver scheme with the highest critical charge is then analysed to investigate the impact of different parameters such as *Vdd*, operating frequency and bias current on the *SEU* tolerance of the driver scheme.

For different operating frequencies of 0.5, 1 and 2GHz, the output voltage swing is swept from 0.25V to 0.5V. Since for a low-swing driver, the output voltage swing is linearly correlated with the *Vdd*, thus, the voltage swing can be changed indirectly by changing the value of *Vdd*. Therefore, *Vdd* is varied from 0.6V to 1V where 0.6V is chosen as the minimum *Vdd* as to ensure that the signal integrity of the driver is still intact. Subsequently, the bias current is swept from 30µA to 500µA with a constant *Vdd* and operating frequency.

This step is repeated for other values of *Vdd*. Through these analyses, the effects of *Vdd*, bias current (*Ibias*) and operating frequency on *Qcrit* can be observed.

4.3.3. *SEU* Analysis – Results and Discussion

In this work, *SEU* analysis is performed for all low-swing signalling schemes, namely, nLVSD, mLVSD, MJD and DDC driver schemes. However, in order continue with further analysis of the impact of different parameters affecting *SEU* tolerance of the low-swing driver scheme, the low-swing driver with the highest critical charge is chosen as candidate. The result for the comparison analysis is shown in Figure 4.3. These results were obtained using Cadence Virtuoso Analog Design Environment, where a range of bias currents was inserted to the driver circuit such as shown in Figure 4.2 together with the corresponding critical charge calculated using Equ.4.2. This process was repeated for every driver circuit to be tested.

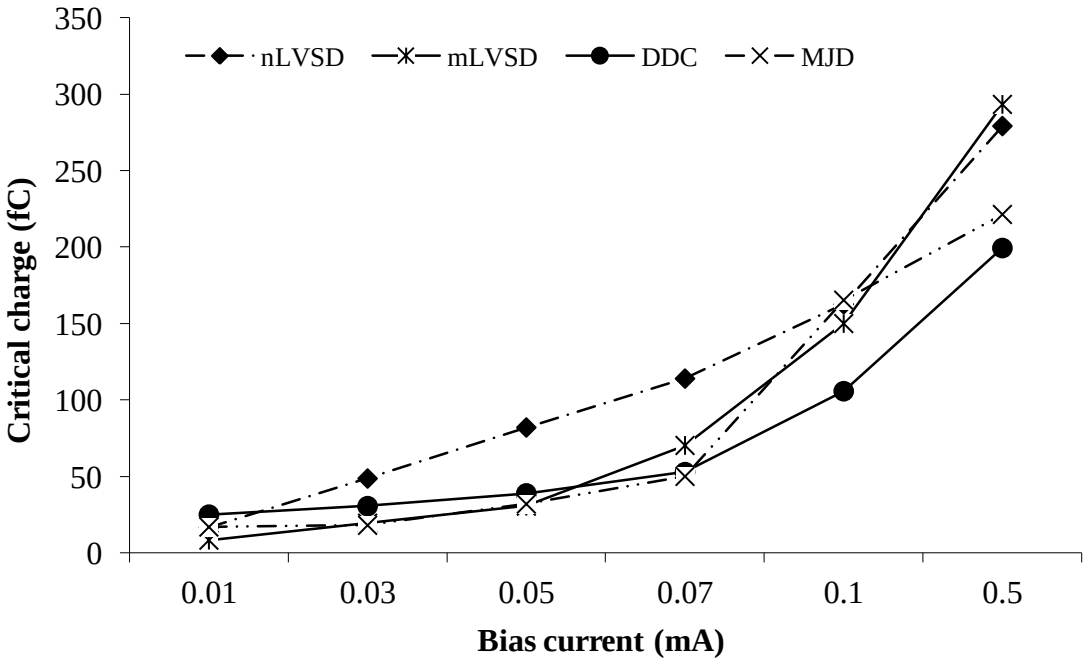
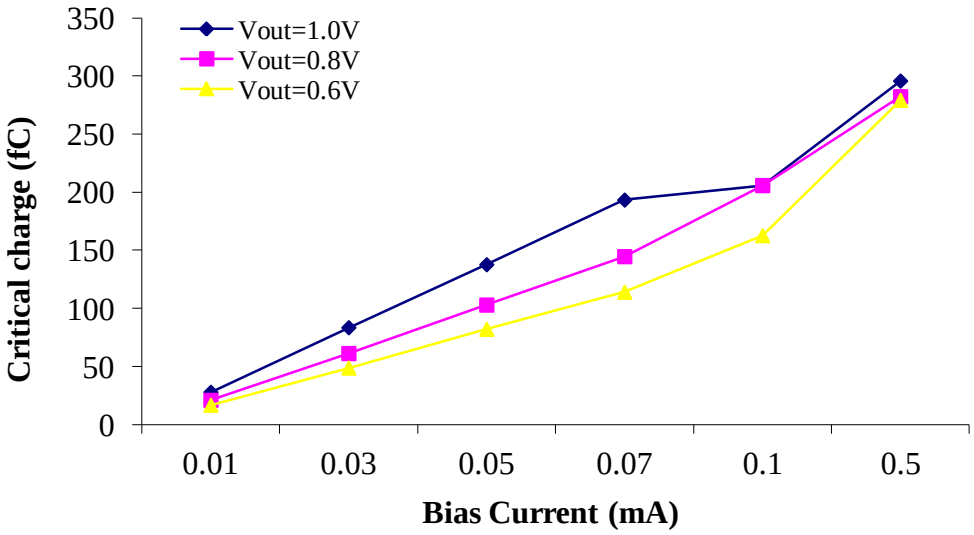


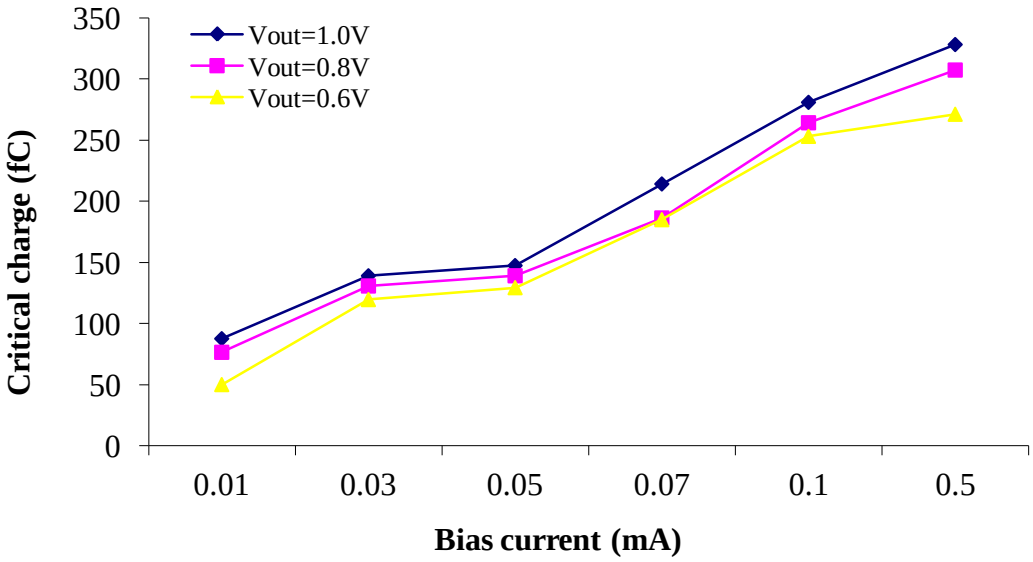
Figure 4.3: Comparison of critical charge between low-swing signalling schemes.

Figure 4.3 indicates that the mLVSD driver is the best candidate to be tested for *SEU* tolerance as it has the highest critical charge compared to other low-swing drivers. Subsequently, the result also shows that the critical charge for the nLVSD driver is almost the same as the mLVSD which indicates that both of the proposed low-swing drivers have better *SEU* tolerance compared to the DDC and MJ drivers. Therefore, the mLVSD driver is

chosen to be the candidate to be tested for this analysis by using Cadence Virtuoso Analog Design Environment. Firstly, the impact of bias current on the *SEU* tolerance of the mLVSD driver is tested at fixed temperature of 25°C, varying Vdd from 0.6V to 1V and operating frequency from 0.5GHz to 1GHz. This is also carried out using Cadence Virtuoso Analog Design Environment. The results are presented in Figure 4.4.



(a)



(b)

Figure 4.4: Critical charge against bias current for different output voltage at (a) 0.5GHz and (b) 1GHz.

Figure 4.4 indicates that by increasing the bias current, there is no effect towards *Qcrit* as the operating frequency is increased from 0.5 to 1GHz. A larger bias current implies larger transistor size and as a result larger capacitances to hold charge and consequently greater

immunity to an *SEU*. In Table 4.1, the amount of increase in *Qcrit* is shown for different values of *Vdd* at an operating frequency of 0.5GHz when moving from 30µA to 500µA. It can be seen that the value of *Qcrit* increases between three and six times as the supply voltage is reduced from 1 to 0.6V.

Table 4.1: *Qcrit* improvement with current bias for different *Vdd* at 0.5GHz

Vout(V)	*Qcrit*(fC) at *Ibias* = 30uA	*Qcrit*(fC) at *Ibias* = 500uA	Increase in *Qcrit*
0.6	48.67	279.21	x5.74
0.8	61.18	282.26	x4.61
1	83.43	295.78	x3.55

It is expected that as the bias current increases, *Qcrit* increases, which implies that the effect of an *SEU* on the circuit can be minimized if larger bias current is applied. However, this might have a significant effect on the power consumption, which increases linearly with the bias current. Since, a key objective of the low-swing driver schemes is reducing power consumption, thus, the trade-off between bias current and power consumption needs to be considered if this method is used.

SEU tolerance can also be improved by increasing the voltage swing or in this case the voltage supply. The improvement in *SEU* tolerance by increasing *Vdd* is shown in Figure 4.5. *Qcrit* increases with *Vdd* due to better margin on the effective voltage (*Vgs* – *Vth*) of the diode-connected transistors at the output. This is similar to increasing noise margin of the circuit. Therefore, with a higher voltage swing, more charge is needed to upset the affected node, or change the output. The improvement in *Qcrit* is shown in Table 4.2 when varying *Vdd* from 0.8V to 1V with constant bias current at an operating frequency of 0.5GHz. Improving the *SEU* tolerance by changing the values of *Vdd* will still increase the power consumption, even though the bias current is constant, but since low-swing application is used, the increase in power consumption is insignificant compared to the improved *SEU* tolerance of the low-swing driver scheme. However, one factor that needs to be considered is the driver size as the increase in *Vdd* with constant bias current will lead to increase in an output resistance of the driver.

Table 4.2: *Qcrit* improvement with Vdd
for different bias currents at 0.5GHz

Bias current (µA)	*Qcrit*(fC) at *Vdd* = 0.8V	*Qcrit*(fC) at *Vdd* = 1V	Increase in *Qcrit*
30	12.51	19.47	X1.56
50	26.42	31.98	X1.21
100	59.79	94.55	X1.58

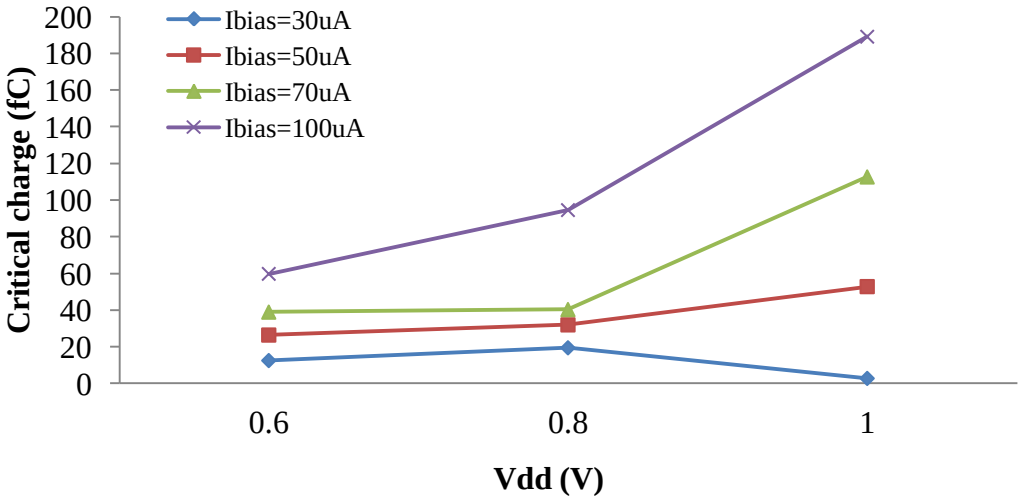


Figure 4.5: Critical charge against supply voltage for different bias currents at 0.5GHz.

Another method in improving *SEU* tolerance is by increasing the operating frequency or data rates. The mLVSD driver is simulated at 0.5, 1 and 2GHz, varying *Vdd* from 0.6 to 1V. At frequency below 1GHz, *Qcrit* is independent of the operating frequency. This means there is enough time for *SEU* to upset a node. At higher frequencies, the ionization time constants are independent of the operating frequency, thus at some points, they will become larger than the operating frequency. Therefore, more energy is required for an *SEU* to have an effect in this short period of time, which makes the circuit less sensitive to radiation at high frequencies. The dependability of *Qcrit* on operating frequency is shown in Figure 4.6.

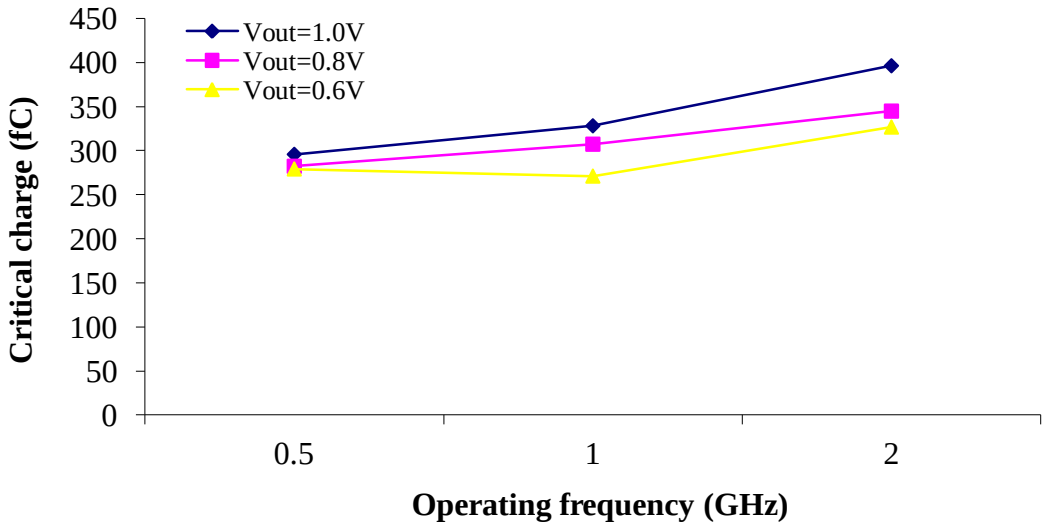


Figure 4.6: Critical charge against operating frequency for different *Vdd* values at bias current of 500µA.

The improvement in *Qcrit* by increasing the operating frequency is shown in Table 4.3. *Qcrit* increases by about 1.2 times when the frequency increases from 1 to 2GHz at a constant *Vdd* of 1V.

Table 4.3: *Qcrit* improvement with operating frequency for different bias currents at 1V.

Ibias(uA)	*Qcrit*(fC) at frequency = 1GHz	*Qcrit*(fC) at frequency = 2GHz	Increase in *Qcrit*
10	87.6	88.99	x1.02
70	214.13	264.18	x1.23
500	328.14	396.27	x1.21

Based on the results obtained, as the bias current increases, the critical charge increases as well, this is due to an increase in transistor sizes. The larger the transistors, the larger their capacitances, which in turn increase the value of the critical charge. The results also show that *Qcrit* can increase up to 6 times as the bias current changes from 30 to 500µA. However, this improvement in *SEU* tolerance is at a cost of an increase in power consumption. Beside from the bias current, *Vdd* is also swept to observe the impact on *Qcrit*. As *Vdd* increases, the output voltage swing increases as well, this in turn increases *Qcrit*, consequently making the node more tolerant to *SEU*. The results also show that *Qcrit* is increased to more than 1.6 times when *Vdd* is increased from 0.8 to 1V at bias currents of 30 and 500µA respectively. Increasing *Qcrit* by increasing *Vdd* adds to the power consumption, even though the bias

current is unchanged. However, by using the low-swing drivers, the increases in power consumption is insignificant to the improvement achieved this technique.

The mLVSD driver scheme was simulated varying the frequency from 0.5 to 2GHz in order to observe the dependability of *Qcrit* on speed. The results indicate that *Qcrit* is independent of operating frequency until it reaches a frequency threshold, which is 1GHz in this case. When this threshold is reached, *Qcrit* increases with the operating frequency, *Qcrit* is almost 1.2 times greater at 2GHz than at 1GHz.

Having analysed and discussed different design methods in mitigating problems with *SEU*s, as well as identifying the robustness of the diode-connected driver circuits against *SEU*s, the next section will explore the impact of intermittent faults, namely, the crosstalk, on the low-swing signalling (nLVSD, mLVSD, MJ and DDC) schemes.

4.4. Effect Of Crosstalk On The Reliability Of Low-Swing Signalling Schemes

As the feature sizes have been shrinking with process technology scaling, the spacing between adjacent interconnect lines keeps decreasing in every process node. While the lateral width of interconnect wires has been scaled down significantly, their vertical height has not been scaled in proportion, which leads to a very rapid increase in the amount of coupling capacitance between the wires. In [14] it was reported that coupling capacitance accounts for more than 85% of the total interconnect capacitance in the 90nm technology node. More aggressive technology scaling will lead to an increase in the overall contribution of the coupling capacitances to the total interconnects capacitance. Subsequently, as technology advances, there will be an increase in chip frequency and a decrease in voltage margin, which will exacerbate the impact of crosstalk noise on interconnect delay. All the above trends consolidate the needs to include crosstalk effect in the reliability analysis of *VLSI* circuits.

Crosstalk is due to capacitive coupling, where the switching characteristics of an interconnect line is affected by the simultaneous switching of lines that are in close physical proximity, as illustrated as in Figure 4.7. When line *A* switches, it tends to bring its neighbouring line *B* along with it on account of capacitive coupling. If line *B* is supposed to switch simultaneously, this may increase or decrease the switching delay. If *B* is not supposed to switch, crosstalk causes noise on line *B*. The impact of crosstalk depends on the ratio of C_C to the total capacitance. Crosstalk is very important in long interconnects as the load capacitance no longer dominates being replaced by the coupling capacitance.

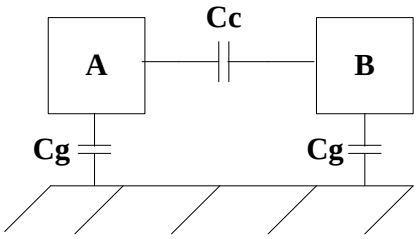


Figure 4.7: Capacitances between adjacent neighbours and ground.

4.4.1. Crosstalk Noise Effects

Crosstalk noise is introduced as line *B* partially switches when line *A* switches, where line *B* is supposed to remain constant. In this case, line *A* is known as the aggressor line while line *B* is the victim. If the victim is floating, the circuit can be modelled as a capacitive voltage divider to compute the victim noise as shown in Figure 4.8(a). Note that ΔVa is normally *Vdd*, and ΔVv is voltage changes across the victim line.

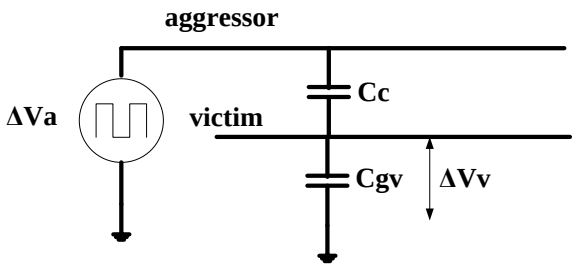
$$\Delta V_V = \frac{C_C}{C_{gv}+C_C}\Delta V_a \tag{4.3}$$

If the victim line is actively driven, the driver will supply current to oppose and reduce the victim noise. The drivers are modelled as resistors as shown in Figure 4.8(b). The peak noise becomes dependent on the time constant ratio, *k* of the aggressor to the victim line [15].

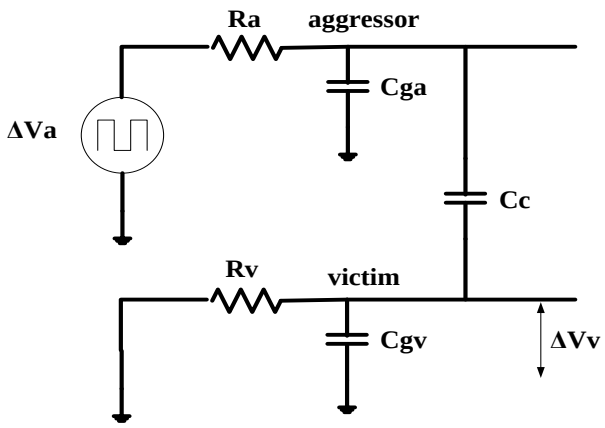
$$\Delta V_V = \frac{C_C}{C_{gv}+C_C}\frac{1}{1+k}\Delta V_a \tag{4.4}$$

where $k = \frac{\tau_a}{\tau_v} = \frac{R_a(C_{ga}+C_C)}{R_v(C_{gv}+C_C)}$.

Larger or faster drivers oppose the coupling effects faster and resulting in a noise voltage that is a smaller percentage of *Vdd*. During the noise event, the victim transistor is in linear region whilst the aggressor is in saturation. For equal sized drivers, this means *Ra* is 2 to 4 times *Rv*, with greater ratios arising from more velocity saturation [15].



(a)



(b)

Figure 4.8: The circuit model when coupling to (a) a floating victim line and (b) driven victim line [16].

When analysing the effects of noise, the term 'noise width' is used as a measure of the length of time that the value of the noise voltage is larger than a given threshold and is generally used to represent the speed of the noise. The capacitive crosstalk noise can be illustrated as in Figure 4.9, where it shows that the peak noise amplitude, *Vpeak* is not the only metric used to characterize noise. Even if *Vpeak* exceeds a certain threshold, the receiver may still be immune to noise in certain cases such as when the noise has a very narrow width and the receiver capacitance is large, which means that the noise is too fast to trigger a low bandwidth receiver.

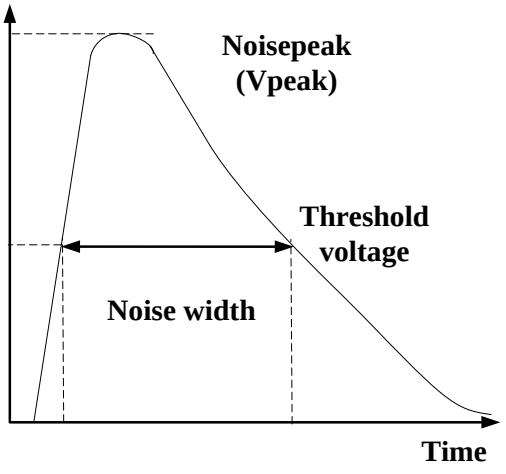


Figure 4.9: Characterizations of crosstalk noise [17].

4.4.2. Crosstalk Delay Effects

If a wire and its neighbour are both switching, the direction of the switching affects the amount of charge that must be delivered. The charge delivered to the coupling capacitor is

$Q=Cc\Delta V$ where ΔV is the change in voltage between lines *A* and *B*, referring back to Figure 4.8. If line *A* switches but line *B* does not, then $\Delta V=Vdd$. The total capacitance effectively seen by *A* is just the capacitance coupling to ground, *Cg* and to line *B*, *Cc*. If lines *A* and *B* switch in the same direction, $\Delta V=0$. Hence no charge is required and *Cc* is effectively absent for delay purposes. If lines *A* and *B* switch in the opposite directions, $\Delta V=2Vdd$, twice as much charge is required. Equivalently, the capacitance can be treated as being effectively twice as large switching through *Vdd* alone.

The effective coupling capacitance can be interpreted in the form of a switching factor (*s.f*). The idea of the switching factor is based on the Miller effect across the coupling capacitance as described previously. In order to approximate *Cc* as a ground capacitance with only one switching node, the effective *Cc* should be calculated as follows [16]:

$$C_{Ceff} = s.f \times C_C \tag{4.5}$$

$$s.f = 1 - \frac{\Delta V_V}{\Delta V_{a1}} \tag{4.6}$$

where ΔV is the voltage change during the overlapping period of voltage switching. According to these equations, *s.f* can be summarised in Table 4.4. Note that ↑,↓ and – denote 0-to-1, 1-to-0 and no transitions respectively.

Table 4.4: Effective crosstalk capacitance for different transitions.

Transitions	↑↑or↓↓	↑-or↓-	↓↑or↑↓
ΔV	0	*Vdd*	2*Vdd*
s.f	0	1	2
Cc_{eff}	0	*Cc*	2*Cc*

If a three wire bus is used such as shown in Figure 4.10, the same analysis can be applied for the second aggressor line. If the crosstalk capacitances between the victim and both aggressor lines are identical, the total effective *Cc* can be calculated as follows:

$$C_{Ceff} = \rho C_C \tag{4.7}$$

$$\rho = s.f_1 + s.f_2 \tag{4.8}$$

where ρ is a coupling factor, a sum of switching factors for both cases.

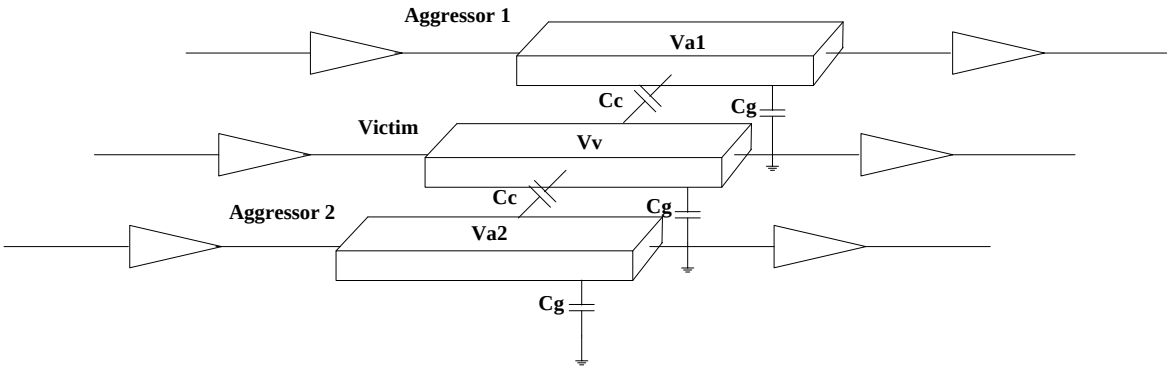


Figure 4.10: Circuit structure for a three-wire bus[18].

4.4.3. Methods of crosstalk mitigation

There are several common methods of mitigating problems with crosstalk and they can be grouped into two categories, i.e. physical design techniques such as driver sizing, interconnect geometry optimization and shielding, and circuit techniques such as repeater insertion. Signal delay is a strong function of the physical interconnect structure such as wire length, width and spacing. In addition, the magnitude of the coupling noise is strongly dependent on how close the wires are placed and the neighbouring transition activity, which is determined by the driver strength and load capacitance.

4.4.3.1. Driver sizing

If the victim driver is large, its effective conductance increases, allowing it to hold a signal on an interconnect line more steadily. On the other hand, if an aggressor driver is larger, the amount of noise it can induce on a victim is increased. Therefore, increasing the driver size has a two-fold impact on crosstalk, which is the noise on the wire with the large driver is decreased but the induced on noise neighbouring lines will increase.

4.4.3.2. Interconnect geometry optimization

The most effective way in reducing the interconnect delay is by increasing the interconnect width as wider lines generally have less delay. This is because when the width is increased, the reduction of resistance occurs faster than the increase in total capacitance, which is dominated by coupling capacitance. The two dominating considerations of capacitive crosstalk are coupling capacitance and neighbouring switching condition which means that the effective way of reducing noise is to increase the spacing between lines.

4.4.3.3. Shielding

The capacitive coupling effects can be avoided if the adjacent lines do not switch. The coupling can be eliminated by shielding critical signals with power or ground wires on one (*half-shielding*) or both sides (*shielding*). Shielding can also be combined with data duplication as shown in Figure 4.11(d). Figure 4.11 shows how shielding technique works in a three wires bus. Aside from eliminating capacitive coupling, this technique can also be used to remove any associated delay uncertainty. The use of power or ground lines as shield wires within high speed buses is the most commonly used design technique to limit signal line coupling but at the cost of an increased routing area.

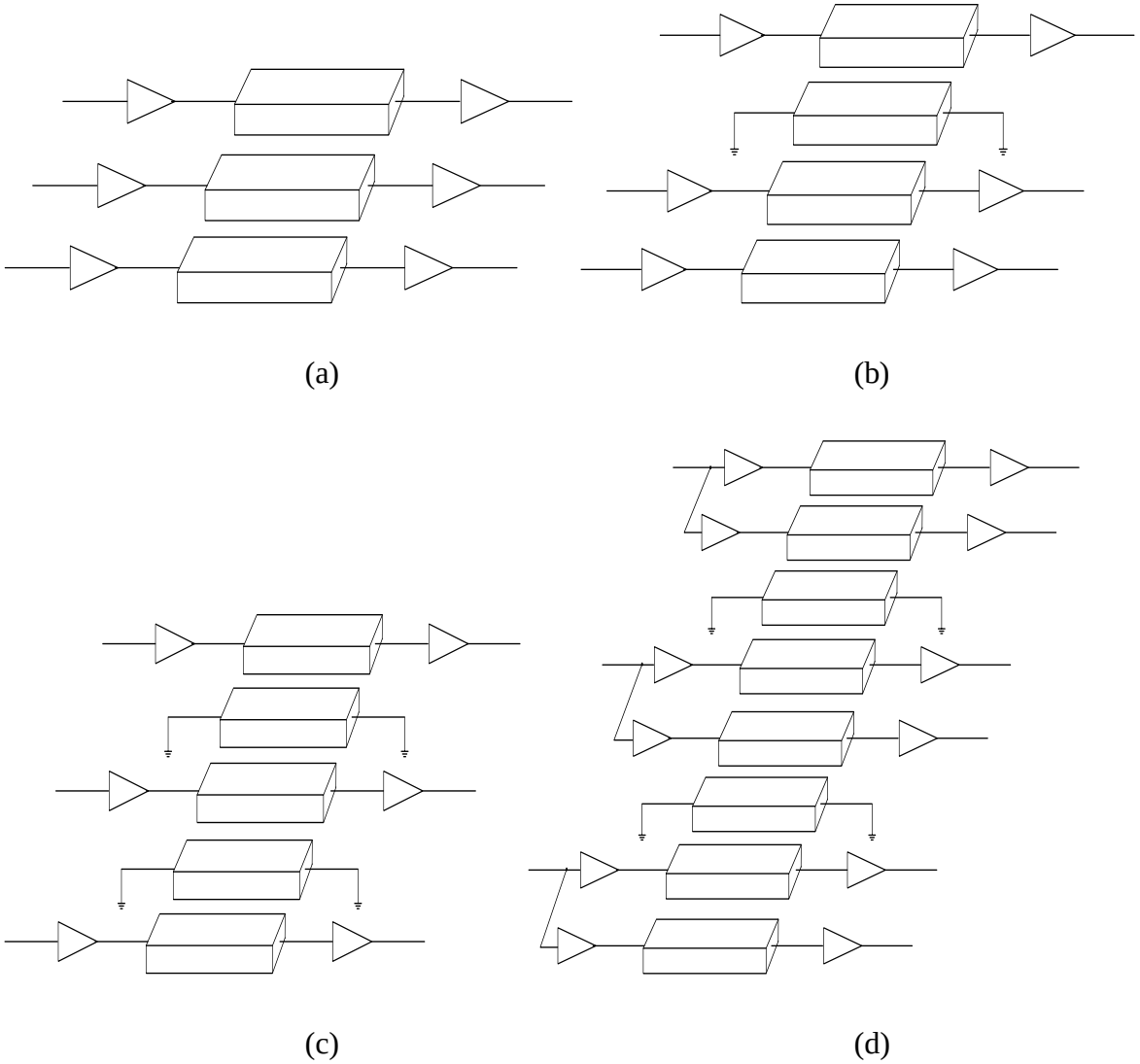


Figure 4.11: Shielding techniques; (a) unshielded lines, (b) half-shielded lines, (c) shielded lines and (d) shielded and duplication lines [17].

4.4.3.4. Repeater insertion

Repeater or buffer insertion is a key solution for reducing the large delay of long interconnects but with the penalty of increased chip area and power consumption. the technique breaks down long interconnects and insert drivers or repeaters in between the resulting segments, essentially reducing the delay dependence on wire length from a quadratic to linear function and thus greatly alleviating the delay problem of long interconnects. Additionally, it improves signal slew rate at the far-end receiver due to the regenerative nature of *CMOS* drivers.

With the exception of the first and last segments of the interconnects, the buffers or repeaters are usually inserted at uniform intervals because in practice the driver and receiver sizes may not be the same as the buffer size. For *RC* interconnects, the most commonly used expression to calculate the optimal number of buffers, *k*, and optimal buffer size, *h*, is that of Bakoglu [19]. The optimal number of buffers is calculated as:

$$k_{opt} = \sqrt{\frac{0.4R_wC_w}{0.7R_{dr}C_{in}}} \tag{4.9}$$

where R_{dr} and C_{in} are the output resistance and input capacitance of a minimum size buffer, whilst R_w and C_w are wire resistance and capacitance. The optimal size of the buffer can be calculated as follows:

$$h_{opt} = \sqrt{\frac{R_{dr}C_w}{R_wC_{in}}} \tag{4.10}$$

Breaking down the interconnect into shorter segments, makes it more immune to noise. This technique reduces the parallel length of interconnects which strongly affects the crosstalk noise. The crosstalk noise is suppressed by the regenerative nature of the buffer.

The placement of the buffer on adjacent lines can be staggered to minimize the impact of coupling capacitance on delay and crosstalk noise as shown in Figure 4.12. The buffers are offset so that each gate is placed in the middle of its neighbouring gates' interconnect loads. The effective switching factor is limited to 1 due to the presence of potential worst-case simultaneous switching or adjacent wires for only half the length of the victim line, while the other half of the victim line will experience the best case neighbouring switching activity due to symmetry. Repeater or buffer insertion is an effective method of reducing crosstalk noise

and delay uncertainty but it does however require an increasingly larger area and power, which are limited in how much they can improve the reliability.

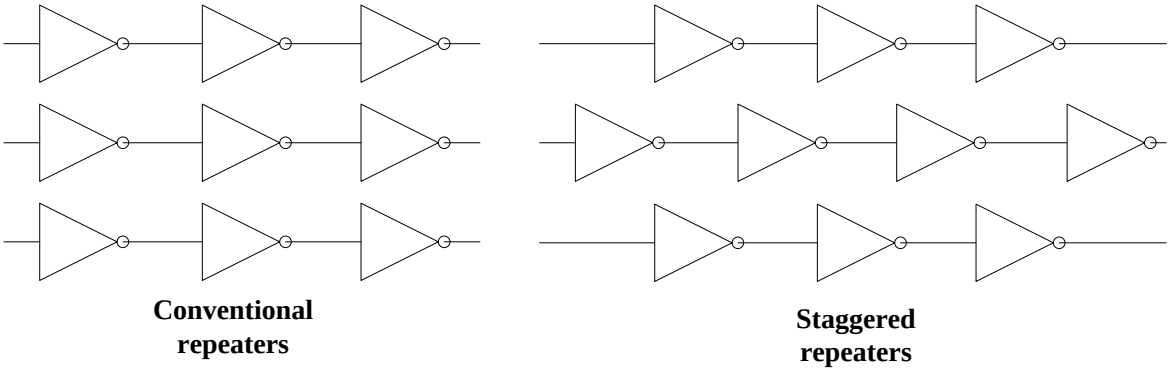


Figure 4.12: Types of repeater insertion [17].

4.4.4. Crosstalk Analysis – Results and Discussion

The impact of crosstalk on delay and the reliability of low-swing signalling scheme for 90nm process technology has been studied using the circuit model shown in Figure 4.10, where the interconnect lines are driven by low-swing drivers and are terminated by low power level restorers as receivers. The aim of this analysis is to investigate the impact of crosstalk on delay and reliability of a low-swing signalling scheme. The mLVSD driver scheme is chosen as a candidate, as this has been proven to have better overall performance from the results obtained previously. Therefore the mLVSD drivers are incorporated into the bus design whilst the Schmitt Trigger receivers are used at the receiver end. In addition to the impact of crosstalk on delay and reliability, the effect of crosstalk on the energy consumption of low-swing signalling scheme was also included; the analysis will include impact of crosstalk avoidance methods discussed previously. In the analysis, a fixed interconnect length of 10mm is used.

Table 4.5 summarises all possible transitions on a 3-wire bus according to their failure characteristics. The transition states are categorized into their types of failure, which are then divided into different crosstalk cases, for both crosstalk delay and noise.

Table 4.5: Data transitions analysed for crosstalk delay and noise[18].

Failure mechanism		Transition	Failure modes
None		000,001,010,011,100,101,110,111,↓00, 00↓,↓01,10↓,↓0↓,11↑,↑11,01↑,↑10, ↑1↑	
Crosstalk delay	Case 1	↑↑↑,↓↓↓	Timing
	Case 2	0↑↑,↑↑0,0↓↓,↓↓0,1↓↓,↓↓1,1↑↑,↑↑1	
	Case 3	↓↑↑,↑↑↓,↑↓↓,↓↓↑, 0↑0,1↑1,0↑1,1↑0, 0↓0,1↓1,0↓1,1↓0	
	Case 4	1↑↓,0↑↓,↑↓1, ↑↓0, 1↓↑,0↓↑,↓↑1, ↓↑0	
	Case 5	↓↑↓,↑↓↑	
Crosstalk noise	Case 1	↓0↑,↓1↑,↑0↓,↑1↓	Functional
	Case 2	↑00, ↑01,10↑,00↑,↓10,01↓,↓11,11↓	
	Case 3	↓1↓,↑0↑	

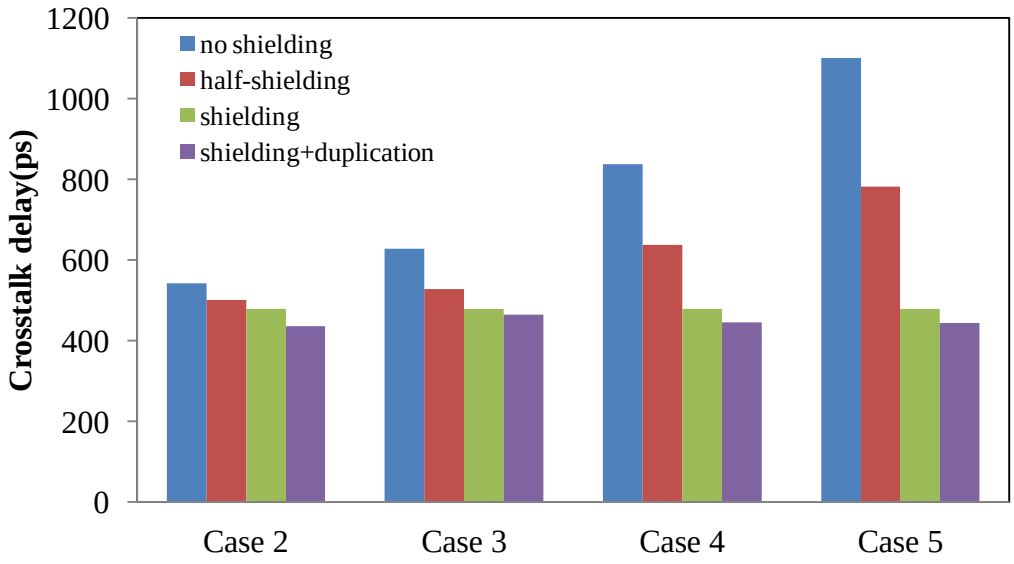
The transitions above are classified into different types of failure modes based on its behaviour. For example in the case of timing failure mode, ↓↑↑ from Case 3, the effective coupling capacitance is calculated to be $3C_c$ where C_c is the coupling capacitance. This is calculated using Table 4.4 where ↓↑ equals to $2C_c$ and ↑↑ equals to C_c where the total equals to $3C_c$, indicating increases in delay as delay is a function of effective capacitance as well as interconnect resistance. In case of functional failure mode, ↓1↓ Case 3 is taken as an example where this is one of the worst cases possible. It shows both transitions on the aggressor wires which can change the value of the victim wire in the middle, causing false data transmission[18].

Timing failure caused by crosstalk delay for Case 5 is expected to be higher compared to Case 2 as it increases with the potential crosstalk activity. The functional failure due to crosstalk noise is measured in terms of peak voltage of the noise, which is expected to increase from Case 1 to Case 3. The impact of cross avoidance methods on crosstalk delay and noise are measured and analysed for each case. The tools used for this analysis is Cadence Virtuoso Analog Design Environment. The analysis is applied for every single transition in each case in order to achieve accuracy in the results.

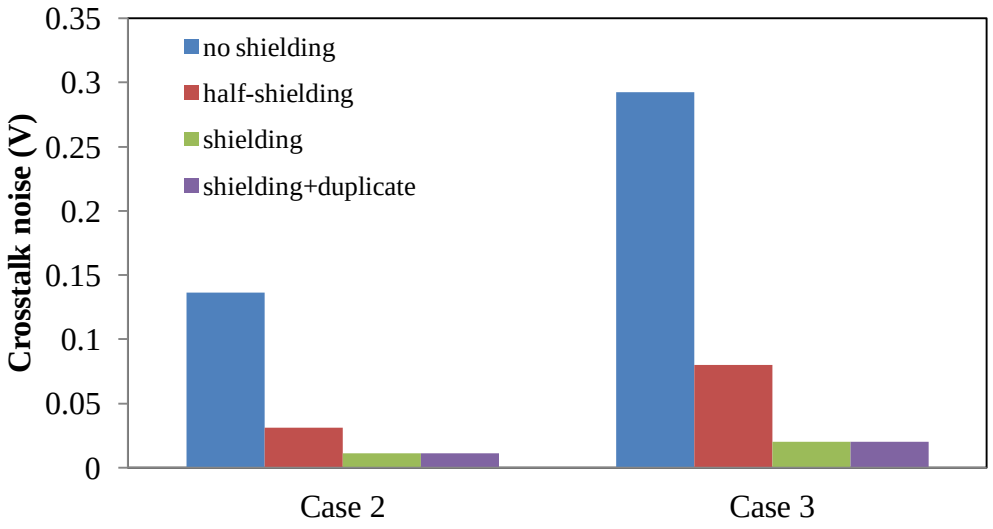
4.4.4.1. The Impact of Shielding

The shielding method can apply either power or ground wires to the existing bus to reduce the impact of crosstalk on delay and reliability of the system. In this analysis, ground wires are used instead and placed as illustrated in Figure 4.11, where different types of shielding methods are implemented, i.e. shielding, half-shielding, shielding and duplication. These shielding methods are applied for each case, as shown in Table 4.5, in analysing the impact of crosstalk delay and noise.

The results in Figure 4.13 show that half-shielding is not very efficient in mitigating the problem with crosstalk, mainly due to its inability to provide complete protection from crosstalk-induced static noise. Duplication and shielding was found to have the best performance as it eradicates static noise induced by capacitive coupling which makes the low-swing bus resilient to functional failures. Subsequently, this method reduces the coupling capacitance, which in turn reduces the crosstalk delay.



(a)

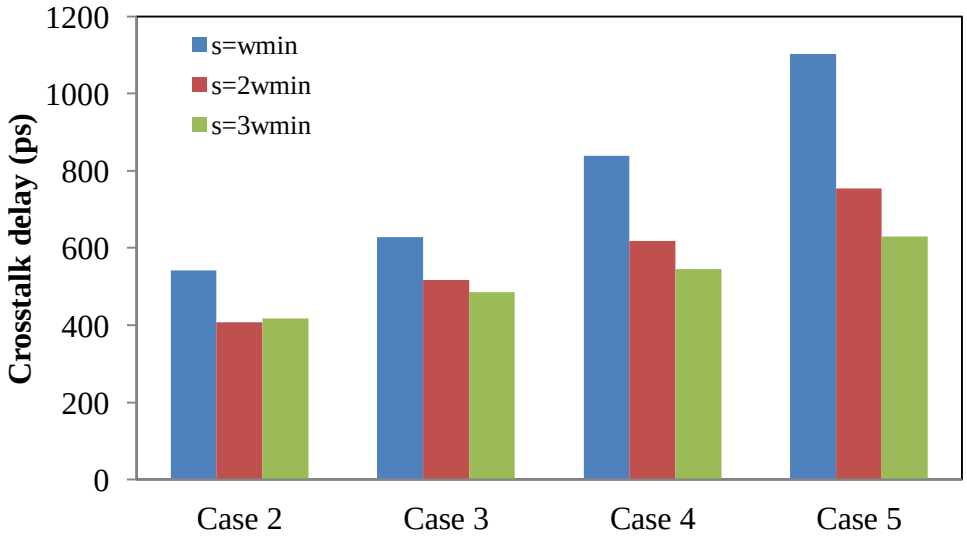


(b)

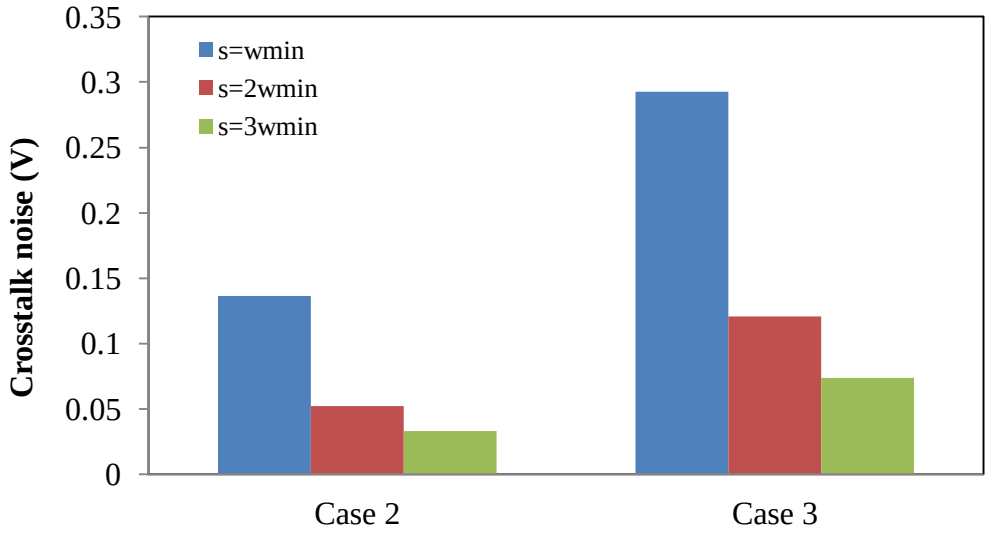
Figure 4.13: Impact of shielding methods on (a) crosstalk delay and (b) crosstalk glitch.

4.4.4.2. The Impact of Wire Spacing

Wire spacing can also be employed to reduce crosstalk delay and noise as shown in Figure 4.14. This is because by increasing the distance between the adjacent wires, will lead to a reduction in its interwire capacitance, i.e. coupling capacitance, which in turn reduces both the delay and the peak voltage of crosstalk glitches.



(a)



(b)

Figure 4.14: Impact of increase wire spacing on (a) crosstalk delay and (b) crosstalk glitch.

4.4.4.3. The Impact of Buffer Insertion

The total length of interconnect used for this analysis is 10mm. Buffer design used incorporates both the low-swing device and level restorer conceived from the mLVSD driver scheme which is then redesigned by removing few unnecessary gates in the digital part of the driver to reduce the area consumption as well as delay. The delay of the buffer, shown in Figure 4.15, is measured at 26.2ps which gives the optimum length of interconnect for minimized delay, calculated using Equ.4.9 and Equ.4.10, to be approximately 2.5mm. Therefore in this analysis, the maximum number of buffers that can be used for the 10mm length of interconnect is 3. A three wire bus shown in Figure 4.10 comprising low-swing signalling schemes is tested against crosstalk effect for three cases; no buffer, 1 buffer and 3 buffer insertions. A uniform buffer insertion method is implemented in this analysis using Cadence Virtuoso Analog Design Environment as measurement tool.

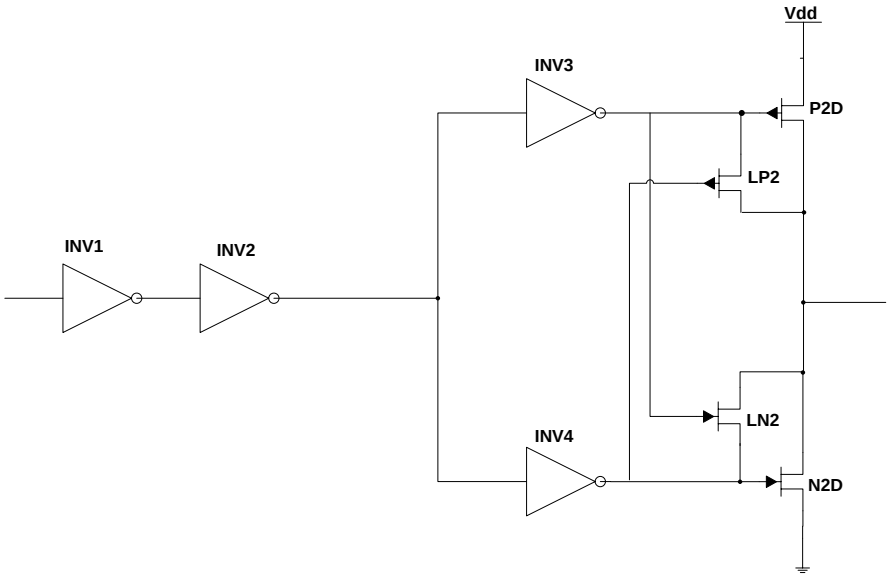
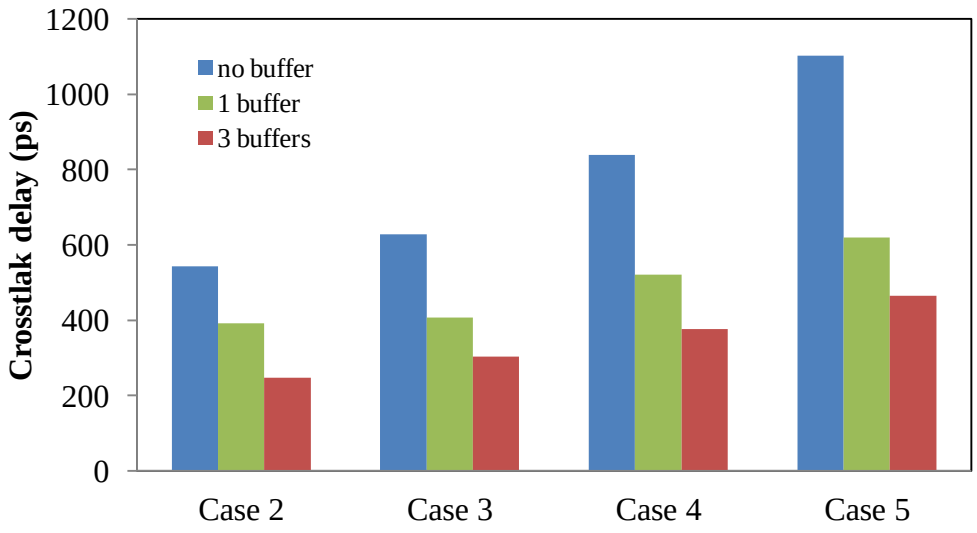
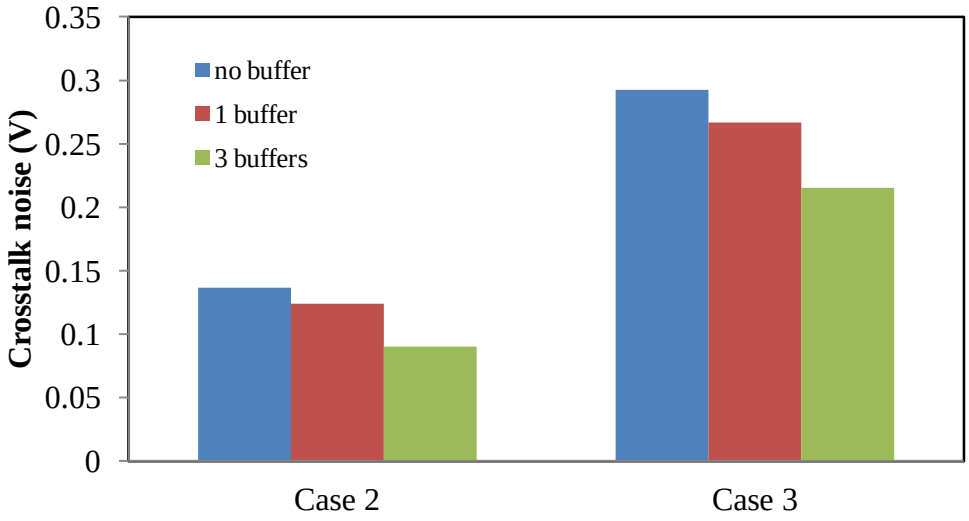


Figure 4.15: Buffer circuit used in the crosstalk analysis.

Buffer insertion proved to be efficient in mitigating problems with crosstalk as shown in Figure 4.16. The method reduces the length of the interconnect which in turns significantly reduces the interconnect delay, due to the reduced dependency of the wire length on wire delay from quadratic to a linear function. Additionally, buffer insertion is also effective in reducing the peak voltage of crosstalk noise due to the reduced parallel length of interconnects and the regenerative nature of the buffer, which suppresses the noise along the interconnect.



(a)

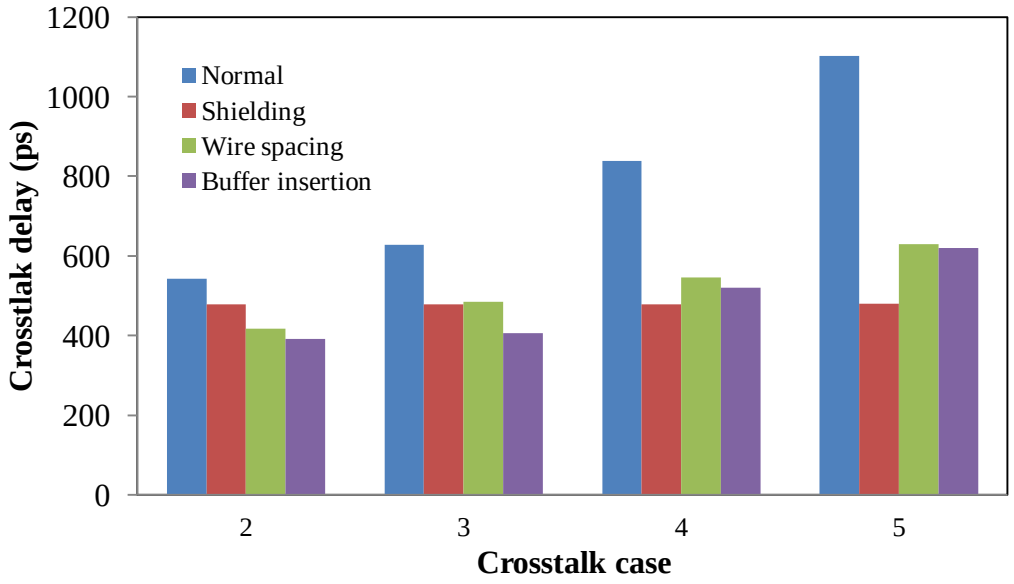


(b)

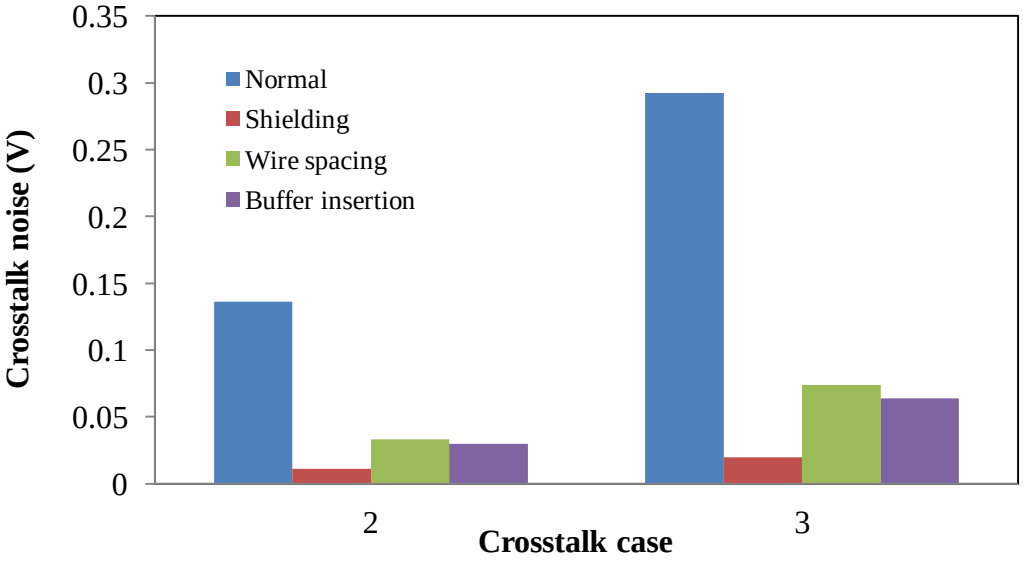
Figure 4.16: Impact of buffer insertion methods on (a) crosstalk delay and (b) crosstalk glitch.

4.4.4.4. Comparative Analysis of Crosstalk Avoidance Techniques

The comparative analysis is necessary in order to observe the impact of different design methods in mitigating the crosstalk effect. The crosstalk delay and noise are compared on the low-swing signalling bus with different design techniques, namely: wire spacing, shielding and buffer insertion. The Cadence Virtuoso Design Environment is again used to assist in this analysis. The results in Figure 4.17 indicate that shielding has the best performance as it achieves less crosstalk delay and glitches. However, when design parameters such as power consumption and area cost need to be considered, shielding is not the best choice in mitigating the problems with crosstalk. As shown in Figure 4.18, low-swing bus with shielding consumes more energy than the normal low-swing bus. This can also be said for buffer insertion method, which, in addition to high energy consumption, also requires larger area. As different applications have different reliability requirements, the best design is the one which can achieve the target performance with the minimum area and power overheads. Since the key objective of the low-swing signalling scheme is to have low power and area cost, the wire spacing method is the best technique as it achieves the reliability objective at minimal area and power cost.



(a)



(b)

Figure 4.17: (a) Crosstalk delay and (b) noise for different crosstalk avoidance methods

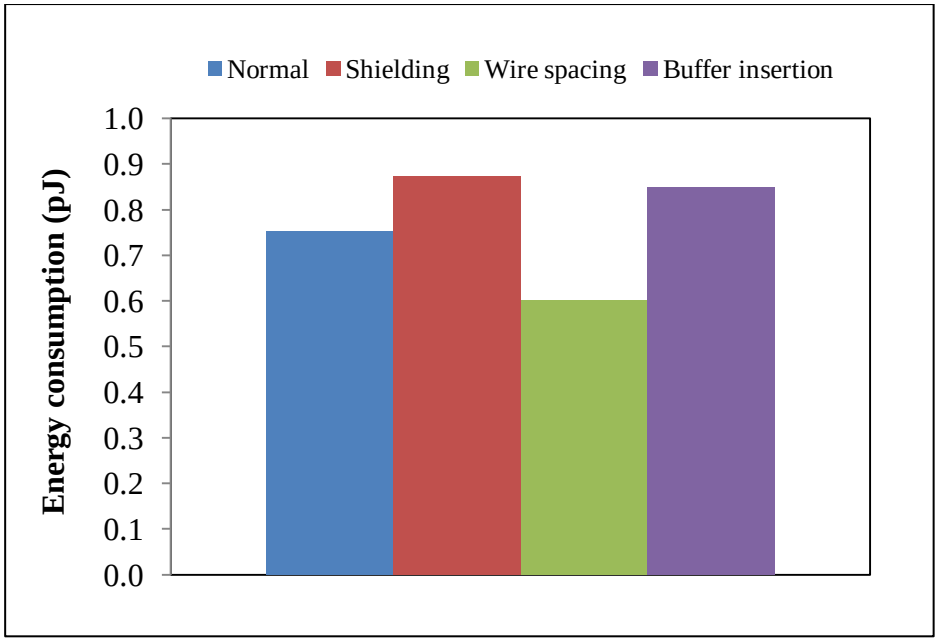


Figure 4.18: Impact of crosstalk avoidance methods on energy consumption.

4.5. Summary

Background reviews on the impact of an *SEU* and crosstalk effects on the performance of low-swing signalling schemes have been introduced. Several important factors such as design methods or parameters that can be implemented into the design scheme for mitigating problems with *SEU* and crosstalk effects have also been discussed. A comparative analysis for all four low-swing signalling schemes, namely: the nLVSD, mLVSD, DDC and MJ driver schemes have been carried out in order to investigate their reliability against *SEU*s and crosstalk effects. The results indicate the proposed low-swing signalling schemes (nLVSD and mLVSD) have better performance and greater immunity to *SEU*s.

In terms of *SEU* tolerance, the results indicate that although by introducing a high bias current into the design which will increase the critical charge and hence improve the reliability towards *SEU*s, the power consumption is significantly increased. Another method in reducing the impact of *SEU* is by increasing *Vdd* or the operating frequency but the improvement is less significant than employing high bias current. Therefore, a good trade-off between the two design parameters need to be found in order to meet reliability target with minimal power overhead.

Several design methods to mitigate the problems with crosstalk, namely: wire spacing, buffer insertion and shielding, have been discussed. The results show that all three methods are

efficient in reducing the crosstalk delay and noise. However, the comparative analysis between these methods indicates that shielding has the best performance overall but at a cost of power and area. Therefore, in order to meet the reliability requirement as well as obtaining minimum power and area cost, wire spacing is found to be the best design solution in this case.

Reliability analysis for the low-swing signalling schemes against non-permanent faults have been performed clarifying that the proposed driver schemes have the best performance overall. However, another important reliability issue which needs to be considered in the analysis is the effects of process variation. Therefore, the reliability of the low-swing signalling schemes against process variation will be investigated in the next chapter.

References

[1] R. K. Iyer, "Experimental Evaluation," *Twenty-Fifth International Symposium on Fault-Tolerant Computing*, pp. 115-132, 1995.

[2] R. K. Iyer and D. Rosetti, "A statistical load dependency of CPU errors at SLAC," *Twenty-Fifth International Symposium on Fault-Tolerant Computing, " Highlights from Twenty-Five Years".*, p. 373, 1995.

[3] H. Ball and F. Hardy, "Effects and detection of intermitten failures in digital system," *Proc. AFIPS Conference*, pp. 329-335, 1969.

[4] D. Atienza et al., "Reliability-aware design for nanometer scale devices," *Proceedings of ASP-DAC*, pp. 549-554, 2008.

[5] A. J. van de Goor, *Testing Semiconductor Memories: Theory and Practice*. Wiley, 1991.

[6] C. Constantinescu, "Impact of deep submicron technology on dependability of VLSI circuits," in *Proceedings International Conference on Dependable Systems and Networks*, 2002, pp. 205-209.

[7] A. Makeshwari, I. Koren, and W. Burleson, "Accurate estimation of soft error rates in VLSI circuits," *Proceedings of 19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, DFT 2004*, pp. 377-385, 2004.

[8] C. Weaver, J. Emer, S. S. Mukherjee, and S. K. Reinhardt, "Techniques to Reduce the Soft Error Rate of a High-Performance Microprocessor," *Proceedings of 31st Annual International Symposium on Computer Architecture*, vol. 32, no. 2, pp. 264-275, Mar. 2004.

[9] T. C. May and M. H. Woods, "Alpha-particle-induced soft errors in dynamic memories," *IEEE Transactions on Electron Devices*, vol. 26, no. 1, pp. 2-9, 1979.

[10] P. Shivakumar, M. Kistler, S. W. Keckler, D. Burger, and L. Alvisi, "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic," *Proceedings International Conference on Dependable Systems and Networks*, vol. 0, pp. 389-398, 2002.

[11] N. Seifert, "Impact of scaling on soft error rate in commercial microprocessors," *IEEE Trans. Nuclear Science*, vol. 49, no. 6, pp. 3100-3106, 2002.

[12] M. Haghi and J. Draper, "The Effect of Design Parameters on SEU Sensitivity of MOS Current Mode Logic," *GLSVLSI '09*, pp. 233-238, 2009.

[13] R. Naseer, Y. Boulghassoul, J. Draper, S. Dasgupta, and A. F. Witulski, "Critical Charge Characteristics for Soft Error Rate Modelling in 90nm SRAM," *IEEE International Symposium on Circuits and Systems, ISCAS 2007*, pp. 1879-1882, 2007.

[14] D. Sinha and H. Zhou, "Statistical timing analysis with coupling," *IEEE Trans ComputerAided Design of Integrated Circuits and Systems*, vol. 25, no. 12, pp. 2965-2975, 2006.

[15] R. Ho, K. Mai, and M. Horowitz, "The future of wires," *Proc. IEEE 2001 Int. Interconnect Tech. Conf.*, pp. 490-504, 2001.

[16] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuit and System Respective*, 3rd ed. Addison-Wesley, 2005.

[17] B. P. Wong Mittal Anurag, Cao, Y., Starr, G., *Nano-CMOS circuit and physical design*. John Wiley & Sons, 2005.

[18] B. Halak, "The Analysis and Optimisation of Performance and Reliability Metrics of Capacitive Links in Deep Submicron Semiconductor Technologies," Newcastle University, 2009.

[19] H. B. Bakoglu, *Circuits, Interconnections and Packaging for VLSI*. Reading: Addison-Wesley, 1990.

Chapter 5

THE EFFECTS OF PROCESS VARIABILITY ON LOW-SWING SIGNALLING SCHEMES

5.1. Background

The salient aspect that can be highlighted from the comparison of the low-swing signalling schemes in Table 2.1 is the absence of a process variation analysis when considering the performance of each scheme, this is a significant omission as process variation can affect the performance of the signalling schemes. Process variations considered in this study are random intra-die variations affecting device and interconnect parameters, for example, fluctuations in threshold voltage, oxide thickness, wire spacing and thickness. These variations are classified as random as they result from the unpredictability of the semiconductor fabrication process; countering their effect is deemed to be the most significant challenge to driver circuit design especially in *VDSM* (*Very Deep Sub-Micron*) technologies. Environmental variations such as supply voltage and temperature are also considered as they are important for power consumption considerations [1].

The chapter begins with an introduction to process variability analysis which highlights the type of variations that are common in the nano-metre regime. The statistical methods which are used in the analyses are introduced comprising corner based analysis, Monte Carlo analysis and the Design of Experiment (*DoE*). These methods are briefly discussed in terms of advantages and disadvantages, which highlights the reason of employing *DoE* in this work. The work flow for analysing the effects of process variability on low-swing signalling schemes is also introduced and is divided into 2 sets of experiments, namely; the single signalling without considering crosstalk effects, and signalling with crosstalk effect; this is followed by the results and a discussion on the outcomes of the analysis.

5.2. Introduction To Variability

The variations in process and design parameters have significantly increased due to the rapid scaling of *CMOS* technology which leads to severe variability in circuit performance and

functionality in the nano-metre regime [2-4]. Variability can be defined as the deviation of parameters from their desired values due to the limited controllability of a process; every process has some level of uncertainty. As device sizes continue to scale down into the deep submicron regime, manufacturing tools are less reliable in their control of design parameters. Process variation usually arises from limitations imposed by the layers of physics, imperfect tools and properties of materials that are not fully understood [5].

5.2.1. Taxonomy of variation

For deep submicron technologies, a combination of device physics, die location dependence, optical proximity effect, micro loading in etching and deposition may lead to heterogeneous and non-monotonic relationship among process parameters [6]. Without detailed understanding of the individual contribution, the resulting process variations might be considered to be completely random and large. However, better understanding of the specific contributions to their distribution reveals that process variations are composed of both systematic and random parts. Variations are said to be systematic when the changes in parameter values are due to known and predictable causes, whilst random variations are due to the inherent unpredictability; for example in the semiconductor fabrication process fluctuations in channel doping, gate oxide thickness and inter-level dielectric (*ILD*) permittivity. As random variations cannot be compensated for and are difficult to minimize, this type of variability may pose the most significant challenge to design an adequate yielding nano-metre scaled integrated circuits [7].

While die-to-die (*D2D*) and wafer-to-wafer variations are more random in nature, within wafer and within die variations are more spatial or location dependent. *D2D* or inter-die variations are the difference in the value of a parameter across nominally identical die and are typically accounted for in circuit design as a shift in the mean of some parameter value equally across all devices or structure on any one chip [6]. Within die (*WD*) or intra-die variations are deviations which occur spatially within any one die. In contrast to *D2D* variations, *WD* variations contribute to the loss of matched behaviour between structures on the same chip. With the *WD* variations, one is concerned with individual transistors, interconnects or any geometric or electrical parameters of the circuit, and how these vary, differentially from their designed or nominal values.

In this work, the robustness of the low-swing driver schemes against variability needs to be tested as it can significantly influence the circuit performance. *WD* variations can affect each transistor differently resulting in for example, devices, within close proximity, having different values of *Vth*. In this case, variability analysis of *WD* variations is chosen for this work as the effects are more closely related to the circuit design.

Several categories of variability have been introduced such as *WD* and *D2D* variations, and systematic and random variations. These categories of variability can further be divided into two sources of variations, which are physical and environmental variations. Environmental factors include *Vdd* and temperature of the chip or across the chip, whilst physical factors include arise in structural device and interconnect variations which are essentially permanent.

5.2.1.1. Physical Variation

Physical variations are caused by processing and masking limitations which results in random or spatially varying deviations from designed parameter values. Physical variations can be categorized as either device and interconnect variations. There are also two forms of variation in both categories as they are further divided into geometric and electrical parameters for the device, and geometric and material parameters for the interconnect.

a) Device geometric variations

This type of variation relates to the physical structure of transistors and other devices such as resistors and capacitors in the circuit. These variations include film thickness and lateral dimensional variations. Film thickness variation includes gate oxide thickness which is critical but usually relatively well controlled. Other intermediate process thickness variations such as poly or spacer thickness can impact on channel length but are rarely modelled. Meanwhile, variations in the lateral dimensions such as length and width of transistors typically arises due to photolithography proximity effects such as systematic pattern dependency and plasma etch dependencies which can affect layout density and aspect ratio.

b) Device electrical parameter variations

Both device geometry and electrical parameter variations are important in variability analysis but one often focuses more on electrical parameter variations. This is because in many cases, the electrical parameters are often directly extracted and modelled. Related examples of the

electrical parameter variations are the threshold voltage and leakage current variations. The most important electrical parameter is the threshold voltage. In addition to geometric sources, mobile charge in the gate oxide can introduce a bias dependent variation which can sometimes be approximated at 10% of the threshold voltage of the smallest device in a given technology. Besides the threshold voltage variation, another electrical parameter that can be significantly affected is the subthreshold leakage current. It may vary substantially and can be impacted by shallow trench isolation structure and stress imperfections due to oxidation and chemical mechanical planarization (*CMP*), which is used to remove the deposited Copper on the etched oxide trenches [8].

c) Interconnect geometry variations

Similar to devices, dimensional as well as material property deviations can be important source of variations in interconnect structures. The main example of interconnect geometric variation parameters are interconnect width and spacing, metal thickness and dielectric thickness. Deviations in the width of the patterned line arise primarily from photolithography and etch dependencies. At the smallest dimension or at a lower metal layer, the importance of the proximity and lithographic effects may be significant. Deviations in line width can directly impact on line resistance, as well as the capacitance, and can also result in difference in line spacing. This can affect the magnitude of line-to-line coupling within the layer which can affect crosstalk and signal integrity.

In conventional metal interconnect, the metal thickness is usually well controlled but can vary from wafer to wafer or across the wafer. However, in dual damascene process [8], dishing and erosion can significantly impact the final thickness of the patterned lines, with 10 to 20% of deviation depending on particular patterns [3]. Another type of thickness that can be affected by variability is the dielectric thickness. The thickness of deposited and polished oxide films can also suffer from substantial deviations. The *CMP* process can introduce larger variations across the die, resulting from the density of raised topography in different regions across the chip [9,10].

d) Interconnect material parameter variations

The most common examples of this type of variation are the contact and via resistance, and metal resistivity and dielectric constant. The contact and via resistance are related to good ohmic contact which can be sensitive to etching and cleaning processes with substantial *D2D*

variations. Meanwhile there is possibility of an occurrence of the metal resistivity variation on *D2D* basis but is usually well controlled. Similarly the dielectric constant is also well controlled although it may vary depending on the deposition process.

5.2.1.2. Environmental Variation

Environmental variations are caused by variations in *Vdd* and temperature, which vary with the operation of the circuit. This type of variation, while possible to model during the design phase is difficult to compensate for, as it is not always present. Therefore, in order to counter these types of variations, circuit designers usually focus on minimizing the variation itself, such as assuring that there is no voltage drop along power line of greater than 10% of *Vdd*, rather than changing the whole circuit. However physical variations are usually treated as a statistical number with the appropriate distribution such as a Gaussian model, this is different from environmental variations which are treated as corners of the operating conditions rather than random parameters.

Environmental variations are acknowledged as important as the physical variations. This is because the environmental variation is potentially a very significant source of performance loss in future technology trends. For example, when *Vdd* is scaled down, the power consumption is reduced which directly increases the delay sensitivities. This in turn may limit the efficacy of *Vdd* scaling for low power applications. *Vdd* will continue to scale modestly by 15%, not by the historic 30% per generation, due to difficulties in scaling *Vth*, and to meet the transistor performance goals [5]. Therefore, the role of *Vdd* should be correctly analysed in variation aware design. Besides *Vdd*, temperature also plays a significant role in meeting performance goals as the physical parameter variations are mostly temperature dependent with higher temperatures causing performance degradation. Thus, this is the reason why the environmental variations are also included in the variability analysis.

5.2.2. Variability Analysis - Methodologies and Work Flow

There are several statistical analysis tools that are used to perform variability analysis on CMOS circuits, or more specifically for this work, on low-swing driver schemes. The most common methods are the corner based analysis, Monte Carlo analysis and the Design of Experiment (*DoE*) method. Brief introductions to these methods are discussed below together with their advantages and disadvantages. This is followed by work flow outline that

is used in this thesis to analyse the robustness of the performance of low-swing driver schemes against variability.

5.2.2.1. The Corner Analysis

Corner based analysis can be assumed as an adaptation of the theory of Design of Experiments to circuit design, assuming that each process variation has a minimum and a maximum value. If there are n variables, there are 2^n possible combinations or corners of their extremes. An example of the structure of this analysis is shown in Figure 5.1, where all eight corners build up a cube with a nominal value is set in the middle of the cube.

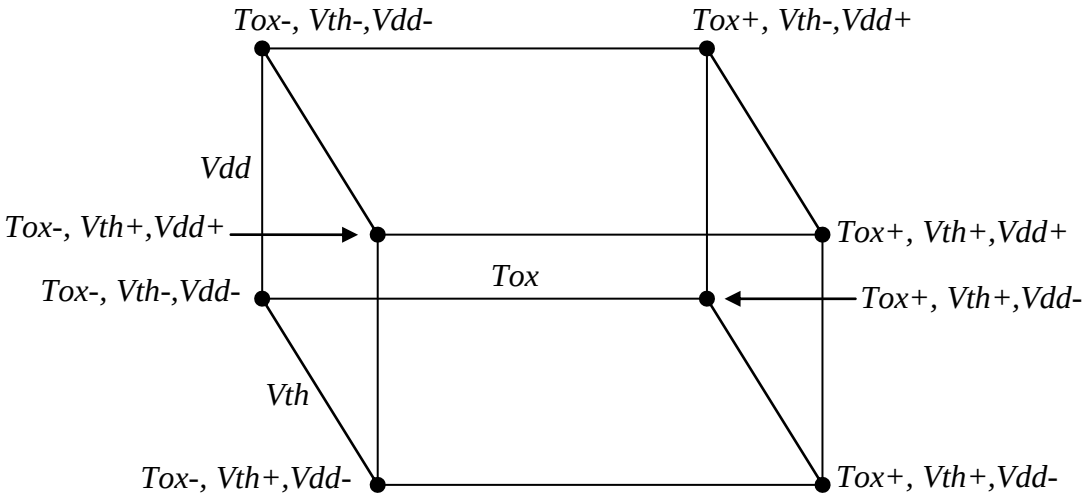


Figure 5.1: Corner based analysis model [11].

Since the cube represents the limits of the process, it is anticipated that any particular die will lie somewhere within this cube as far as the values of these particular process and design variables are concerned. If the design fulfils the specification in all eight corners, it will fulfil the values anywhere in the cube. However, it is important to make the appropriate trade-offs to ensure that this is indeed the case.

The fundamental problem with corner analysis is that it lacks the fuzziness that real processes exhibit. When queried about the possible values of one process parameter in particular process, a statistical distribution will always be presented, not a minimum or maximum value. The statistical information is usually in the form of a probability density function (*Gaussian, Uniform and Poisson*) and its measures of central tendency (*mean,* μ) and dispersion (*standard deviation,* σ). A synthesis tool is required to translate this statistical information about process and design variables to statistical information about design

specifications. However, applying this approach on this analysis method requires an astronomical number of samples. An efficient alternative is to statistically sample the process space with a large number of samples. This is the basis of the Monte Carlo method.

5.2.2.2. The Monte Carlo Analysis

Monte Carlo analysis is a straightforward statistical approach to characterize within die variability. This analysis requires multiple simulations of the test circuit, randomly varying the parameters of interest within their expected distributions with each simulation. For example, in this analysis, a set of *N* random numbers, where each set representing both process and design parameters, is generated on the basis of the statistical properties of each parameter. A simulation is then performed using these random numbers as the values of the process and design variables, and is repeated *N* times. The value of *N* can be small, around 100 or even 1000, however, the higher the value of *N*, the more accurate the analysis will become.

As shown in Figure 5.2, the input for the Monte Carlo analysis is a set of statistical distributions for the process and design parameters whilst the output is a set of statistical distributions for various designs specifications of interest, which are generated using, for example, the *SPICE* circuit simulator. In this example the inputs are gate-oxide thickness and threshold voltage whilst the outputs for these inputs are delay and power consumption. For the analysis carried out in this research, the Monte Carlo tool inside Cadence Virtuoso Analog Design Environment was used where 1000 runs are chosen for improved accuracy.

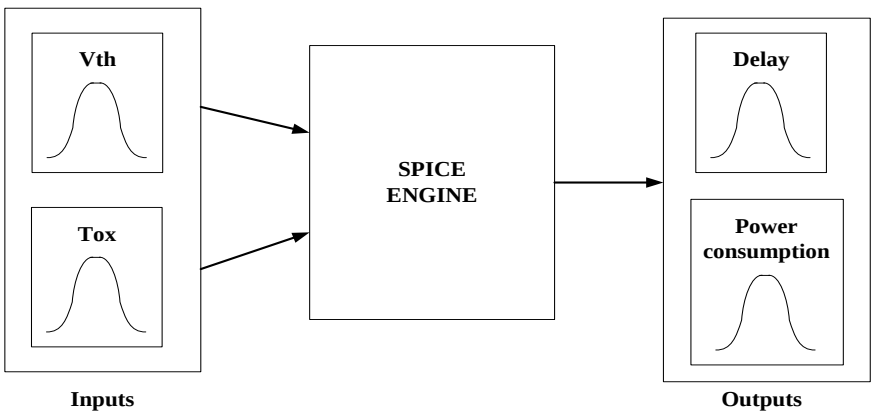


Figure 5.2: Methodology of Monte Carlo analysis to account for performance parameters in respect to the process parameters of interest [11].

Even though the Monte Carlo analysis is statistically efficient in terms of its data accuracy compared to the corner based analysis; it, however, requires larger amounts of computing resources as it is expensive and time consuming to run the simulation, as it usually requires many runs for a given set of input values in order to achieve accurate results. Thus, a more efficient and user friendly statistical analysis tool is required. Therefore, the method of Design of Experiment analysis is adopted in this work due to its computational efficiency over the Monte Carlo analysis.

5.2.2.3. The Design of Experiment (*DoE*) Analysis

The statistical design of experiments (*DoE*) is an efficient procedure for planning experiments so that the data obtained can be analyzed to yield valid and objective conclusions. In an experiment, one or more process variables (*factors*) are changed in order to observe the effect that the changes have on one or more output variables (*responses*). It is widely used in multidisciplinary design to create approximations of the output. This method is much more efficient to run and gives a functional relationship between design factors (*input, x)* and responses (*output, y)*. An experimental design formally represents a sequence of experiments to be performed and expressed in terms of factors or design variables set at specified levels. It is represented mathematically by a matrix *X* where the rows represent the experimental runs and the columns denote the particular setting for each factor for each run [12].

The procedure begins with determining the objectives of an experiment and selecting the process factors for the study. The statistical theory underlying DoE generally begins with the concept of process models.

The best way is to begin with a process model of the box type with several discrete or continuous input factors that can be controlled, and one or more measured output responses as can be seen in Figure 5.3. Experimental designs are used to derive an approximation model linking the outputs and inputs, which generally contain first and second order terms. The experiment often has to account for a number of uncontrolled factors that maybe discrete such as different machine or operators, or continuous such as temperature or humidity.

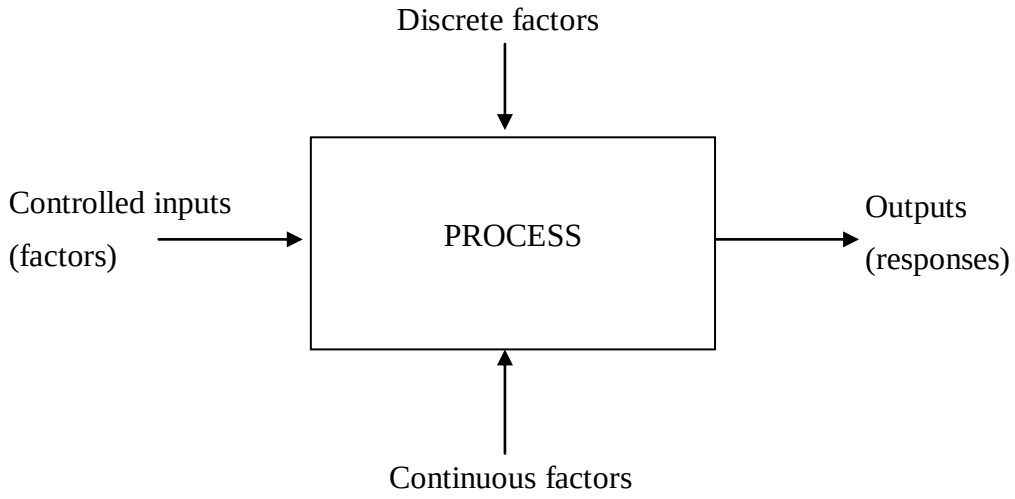


Figure 5.3: A box type example of a process model for *DoE* [13].

The empirical models which fit to the experimental data take either linear or quadratic forms where a linear model with two factors (x_1 *and* x_2) is as shown below:

$$y = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{12} x_1 x_2 + \varepsilon \tag{5.1}$$

Where y is response for given levels of the main effects (x_1 *and* x_2) and ε is the experimental error. The x_1x_2 term is included to account for a possible interaction effect between x_1 and x_2. The constant β_0 is the response of y when both main effects are zero.

A quadratic form is a second order model which adds two more terms to the linear model namely, $\beta_{11}x_1^2$ and $\beta_{22}x_2^2$ to build a model as shown below:

$$y = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{11} x_1^2 + \beta_{22} x_2^2 + \beta_{12} x_1 x_2 + \varepsilon \tag{5.2}$$

This model is typically used in response surface *DoE* with suspected curvature.

Before the type of design of experiment is selected, the design objectives need to be determined. There are four types of design objectives that are mainly used in *DoE*, namely, comparative, screening, response surface method and regression model objectives. The four design objectives are summarised in Table 5.1 with their functions respectively.

Table 5.1: Types of design of experiments with their functions.

Designs	Functions
Comparative	• Choose between alternatives with narrow scope, suitable for initial comparison • Choose between alternatives with broad scope, suitable for confirmary comparison
Screening	• To identify which factors or effects are important • 2 to 4 factors = full factorial • >3 factors, starts with as small design as possible • Trying to extract the most important factors from a large list of initial factors (fractional factorial design)
Response surface modelling	• To achieve one or more of the following objectives: - Hit a target - Maximize or minimize a response - Reduce variation by locating a region where the process is easier to manage - Make a process robust
Regression modelling	• To estimate a precise model , quantifying the dependence of response variables on process inputs

The comparative objective is used when it needs to be decided whether one important factor among the other factors under investigation is significant or whether or not there is a significant change in the response for different levels of that factor. The screening objective is used when it is required to select or screen out important main effects from the many less important ones. The response surface method objective is used to estimate the interaction and quadratic effects of factors to be investigated. The process involves finding optimal process settings, troubleshooting process problems and making a process more robust against external and non-controllable influences. The final design objective is the regression model objective when it is required to model a response as a mathematical function of a few continuous factors and it is used as a guideline to build a good model parameter.

For each design objective, except the regression model objective, several *DoE* methods can be used depending upon the number of factors as shown in Table 5.2. Each of the *DoE* methods is briefly described below.

Table 5.2: Summary of design methods for each type of design objectives.

Number of factors	Comparative objective	Screening objective	Response surface method objective
1	1-factor completely randomized design	-	-
2 – 4	Randomized block design	Full or fractional factorial	Central composite design
5 or more	Randomized block design	Fractional factorial or Plackett-Burman	Screen first to reduce number of factors

For a single factor, the comparative objective is usually used which incorporates 1-factor completely randomized design. For two to four factors, all three objectives can be applied, the randomized block design is used for comparative objective; the full or fractional factorial design for screening purposes and the central composite design (*CCD*) to fulfil response surface method objective. For five or more factors, the same design method is used for comparative objective, whilst fractional factorial or Plackett-Burman design is used for screening. However for response surface method objective, it is required to screen first in order to reduce the number of factors before proceeding with *CCD*. For the research work in this thesis, the response surface method objective is selected with the Plackett-Burman and *CCD* designs incorporated into the design of experiments.

5.2.2.3.1. 1-factor completely randomized design

This design compares the values of a response variable based on the different levels of the main factors. For completely randomized design, the levels of the main factors are randomly assigned to the experimental units.

5.2.2.3.2. Randomized block design

This design involves one factor or variable that is of primary interest but there are also several secondary factors that may affect the measured result but are not of primary interest. An important technique called blocking can be used to reduce or eliminate the contribution to experimental error caused by these factors. Basically, this design involves blocking factors followed by randomization. Blocking is used to remove the effects of a few of the most important secondary variables whilst randomization is then used to reduce the contaminating effects of the remaining secondary variables.

5.2.2.3.3. Full factorial design

The most basic experimental design is full factorial design. The most common designs for the full factorial are the 2^k, which are used to evaluate main effects and interactions, and 3^k designs for evaluating main and quadratic effects and interactions, for k is number of factors, which is equal to 2 and 3 levels respectively. The most common experimental design is the 2-level design because it is ideal for screening design, being simple and economical.

The two-level design uses +1 and -1 notation to denote the high and the low levels respectively for each factor. The use of +1 and -1 for the factor settings is called data coding. This aids in the interpretation of the coefficient fits to any experimental model. The centre point for this design is zero.

5.2.2.3.4. Fractional factorial design

This design is where not all factor level combinations are considered and the designer can choose which combinations are to be excluded. Thus, only an adequately chosen fraction of the treatment combinations is required for the complete factorial experiment is selected to be run. Even if the number of factors in a design is small, the 2^k runs specified for a full factorial can quickly become large. In order to counter this problem, only a fraction of the runs specified by the full factorial design is used. Properly chosen fractional factorial designs for two-level experiments have the desirable properties of being both balanced and orthogonal. A design is said to be balanced when each factor has the same number of levels. The fractional factorial design only focuses on fractions of two-level designs because the two-level fractional designs are the most used in engineering.

5.2.2.3.5. Plackett-Burman design

This design is a two level fractional factorial design used for screening experiments, where only a few specifically chosen runs are performed to investigate just the main effects, assuming all interactions are negligible when compared with few important main effects. The Plackett-Burman designs can be performed efficiently for 25 runs or more. These designs accept up to 47 factors, which sometimes can be narrowed down to 10 factors or less.

In the research work Plackett-Burman design was carried out on 31 device and interconnect parameters associated with the low-swing driver schemes described in Chapter 3. Through

Plackett-Burman screening the main effects or factors has been reduced to 12 as listed in Table 5.3. The device parameters include the threshold voltage, *Vtho*, gate-oxide thickness, *tox* and other parameters such as carrier mobility, μo and effective gate length, *Leff*, whilst the interconnect parameters consists of resistivity, ρ, interconnect dimensions (width, *w*; spacing, *s*; thickness, *t*; interlayer dielectric height, *h*) and the inter-level metal insulator permittivity, ε_k. Environmental factors such as *Vdd* and temperature are also included in the variability analysis. As the main parameters have been identified through the Plackett-Burman design, the next step will involve an implementation of these parameters on the *RSM* design.

Table 5.3: The main parameters of variability.

Device parameters	Interconnect parameters
Vth	ε_k
tox	ρ
Leff	*s*
μo	*w*
Vdd	*t*
Temp	*h*

5.2.2.3.6. Central composite design (CCD)

CCD is a two level factorial or fractional factorial design, augmented by centre points and axial points [13]. The centre points are where all values of the factors are in mid-range whilst the axial points are positioned at mean, $\pm\alpha$ for each factor, where α is the variation in the factor , which gives the estimation of the curvature of the response surface. For *k* input factors, *CCD* requires ($2^k + k + 1$) experimental runs to build a second order model of the output parameters. The desirable features of this design are their orthogonality, where there is minimal variance of the regression coefficients, and rotability, which means equal precision of estimation in all directions.

The experimental design consists of devising a set of experiments in which the range of input parameters can be altered systematically between three levels (*-1, 0, +1*) which represent (*-3σ, 0, +3σ*) variations respectively. The circuit output of interest is measured and calculated at each of the design points to build mathematical models of the output. For the 12 input parameters used for this analysis, *DoE* (*CCD*) technique is computed by using *Minitab*,

indicating 154 experiments is required, where the experiment points for each parameter is recorded in Appendix II.

5.2.2.4. Work Flow for Variability Analysis implementing *DoE* method

The work flow for the variability analysis used in this thesis is summarised below:

a) Modelling the parasitic elements of the circuit

Assuming that the interconnection between driver and receiver in the signalling scheme is implemented using top layer metal to be realised using *UMC 90nm* technology. Two sets of experiments for the variability analysis were carried out, the first set comprised a single line signalling scheme, hence without any crosstalk effects, and the second a three-wire signalling arrangement with crosstalk effects. The parallel line structures are placed between two grounded shields. The resistive and capacitive parasitic elements of the interconnect are calculated using Equation 2.3 to 2.5 and Equ.3.12.

b) Identify sources of variation

In the previous section, the main parameters for the variability analysis have been identified and narrowed down to 12 factors with the aid of the Plackett-Burman analysis. The main factors are shown in Table 5.4 with their 3σ variations, these values are in agreement with those used previously [2,14].

Table 5.4: Parameter values and 3σ variations.

Technology		90nm	
Device parameters	±3σ	Interconnect parameters	±3σ
Vth	30%	ε_k	3%
tox	10%	ρ	30%
Leff	16.7%	*s*	20%
μo	10%	*w*	20%
Vdd	10%	*t*	10%
Temp	(12-70)°C	*h*	10%

c) Design of the statistical experiment

DoE techniques are employed in the variability analysis of the two interconnect schemes in order to build a first order polynomial approximation for the first set of experiment whilst a second order polynomial approximation is used for the design metrics of interest in the second set of experiments. For the first set of experiments, the design metrics are delay and power consumption whilst the second experiment is focused in crosstalk delay and crosstalk glitches. For the 12 input parameters used for this analysis, *DoE* (*CCD*) technique used here requires 154 experiments which are summarised in Appendix II.

d) Record circuit response at each design point

In order to obtain the circuit response for each design point, simulations are carried out using the circuit analyzer (*SPECTRE*) in Cadence Virtuoso Analog Design Environment. The design metrics of interest were measured and calculated in each experiment.

e) Generate polynomial approximations for the circuit output

The polynomial approximations are obtained through statistical software called *Minitab*. There are two types of polynomial approximations, which are coded and uncoded. The input factors in the coded approximation have normalized values of (*-1, 0, +1*) which represent (μ-3σ, 0, μ+3σ), where μ and σ are mean and standard deviations of the input parameters to be tested. The input factors for the uncoded ones have the actual mean values, which can be difficult to analyse. Therefore, the coded polynomial approximation is used instead.

The following sections outline the results obtained from the methodologies used, which were previously discussed, to analyse the impact of variability on the performance of the low-swing signalling schemes. Design models for the low-swing signalling schemes are also discussed for each set of experiments.

5.3. The Impact Of Variability On The Performance Of The Low-Swing Signalling Schemes

As mentioned previously, two set of experiments were undertaken which comprised a single signalling scheme without considering crosstalk effects and the second, a three-wire signalling with crosstalk effects.

5.3.1. Analysis of effect of process variation on the performance of the low-swing driver schemes.

The impact of intra-die process variations on delay and power consumption of low-swing signalling schemes for 90nm process technology has been studied using the circuit model shown in Figure 5.4, where an interconnect line is driven by a low-swing driver and is terminated by a low power level restorer as a receiver. The effect of process variations on the low-swing signalling schemes was determined using a 1000 run Monte Carlo simulation. The parameters to be varied are shown in Table 5.4. In the analysis, a fixed 10mm length of interconnect is used.

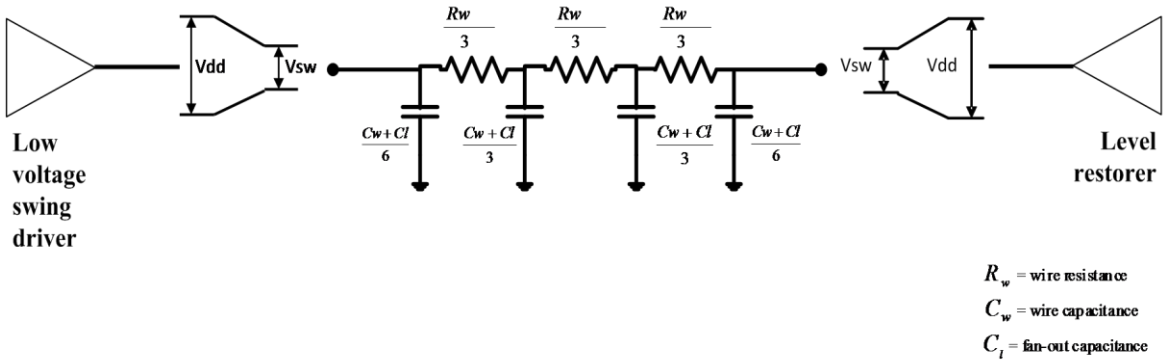
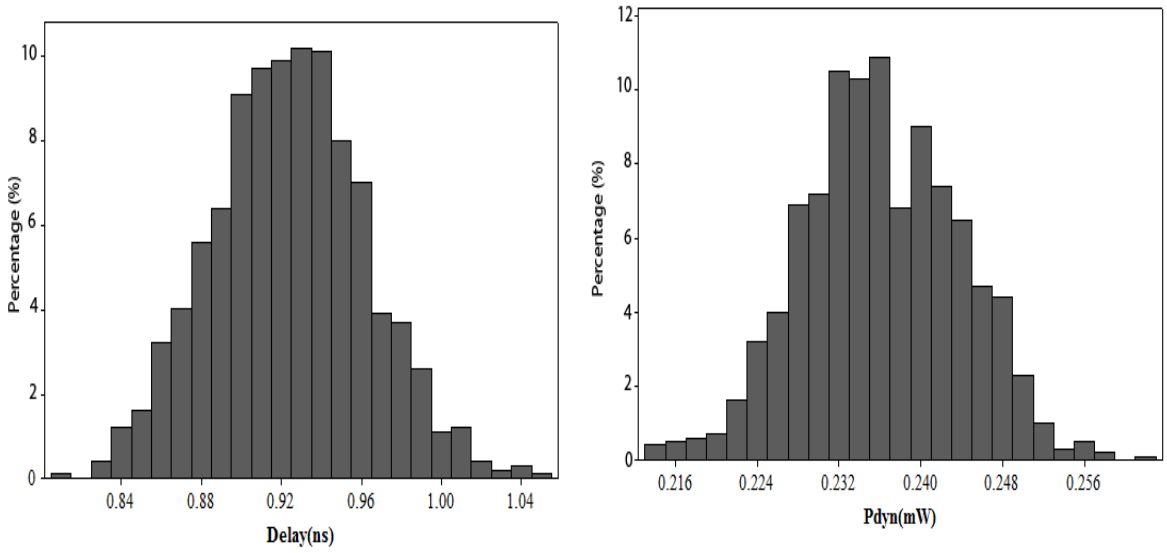


Figure 5.4: Circuit model of low-swing signalling scheme.

In addition to the Monte Carlo analysis, another set of experiments was undertaken to establish individual parameter sensitivities. In this case, all parameters were varied individually in the range of ± 3σ whilst maintaining other parameters at their nominal values. This experiment was carried out using Design of Experiments (*DoE*) techniques [13] to highlight the importance of each variable towards the power and speed performances.

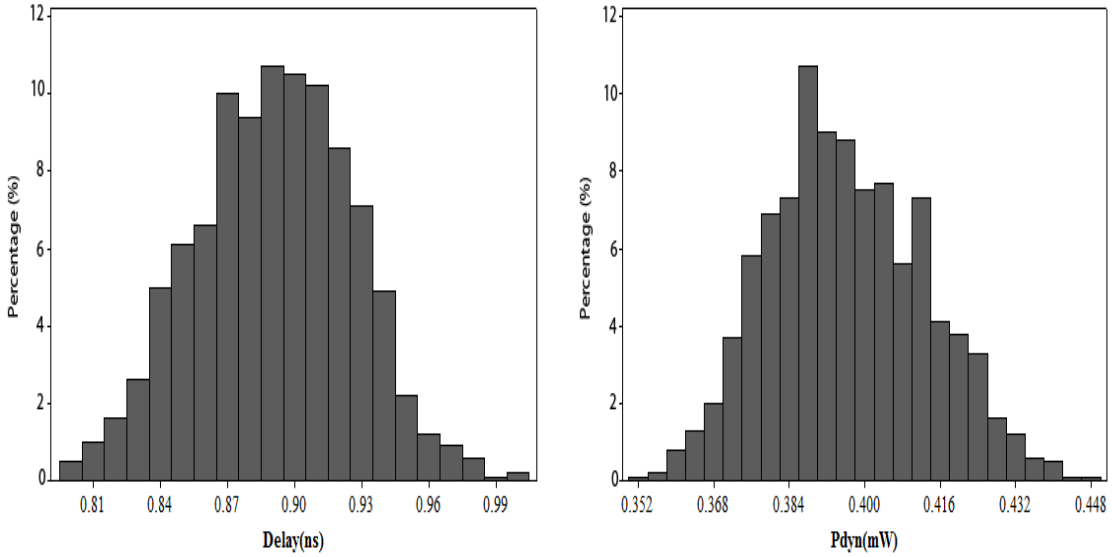
5.3.1.1. Monte Carlo Analysis

Figures 5.5 and 5.6 show, for the nLVSD and mLVSD driver schemes respectively, the distribution of the delay and dynamic power consumption for a 10mm line length in 90nm technology for 1000 Monte Carlo runs. It can be seen that for the nLVSD driver scheme, the delay is normally distributed with the peak at 923.8ps with the distribution of 10.1% over 1000 runs; the dynamic power is normally distributed with a peak of 0.2361mW with the distribution of 10.9% over 1000 runs. The delay and dynamic power variability is 4.17% and 3.26% respectively. Meanwhile, the mLVSD driver scheme also has normal distributions for both the delay and dynamic power with peaks at 890.9ps and 0.3963mW with 10.7% and 8.8% distributions over 1000 runs respectively. The delay and dynamic power variability for the mLVSD driver scheme is 3.96% and 4.23% respectively. A similar analysis was undertaken for the DDC and MJ-driver schemes. Table 5.5 shows the mean and standard deviations of the performance parameters analysed for all four schemes.



(a) (b)

Figure 5.5: Histograms of (a) delay and (b) power consumption of the nLVSD driver scheme.



(a) (b)

Figure 5.6: Histograms of (a) delay and (b) power consumption of the mLVSD driver scheme.

The lowest delay for the 10mm line occurs with the mLVSD scheme which also has the lowest standard deviation; the nLVSD scheme is 3.6% slower than the mLVSD scheme and has a standard deviation which is almost 5% greater than the mLVSD scheme. However the nLVSD scheme has 44% improvement in terms of power consumption and also deviates about 23% less than the mLVSD scheme. This indicates that the mLVSD scheme excels overall in terms of delay but the nLVSD scheme is better overall in terms of power consumption due to its lower swing. However, both proposed schemes are better in performance compared to DDC and MJ-driver schemes as well as more robust when exposed to process variations.

Table 5.5: Performance metrics of low voltage swing signalling schemes.

Technology	90nm							
Driver scheme	nLVSD-driver		mLVSD-driver		MJ-driver		DDC-driver	
	Mean	σ	Mean	σ	Mean	σ	Mean	σ
Delay(ps)	923.8	4.17%	890.9	3.96%	969.1	4.72%	1721	4.8%
Power Consumption (mW)	0.236	3.26%	0.396	4.23%	0.436	5.05%	0.465	5.88%

Both of the proposed driver schemes are more robust compared to the DDC and MJ-driver schemes in terms of delay and dynamic power variations. However, when comparing the nLVSD and mLVSD performances against variability, both schemes complement each other

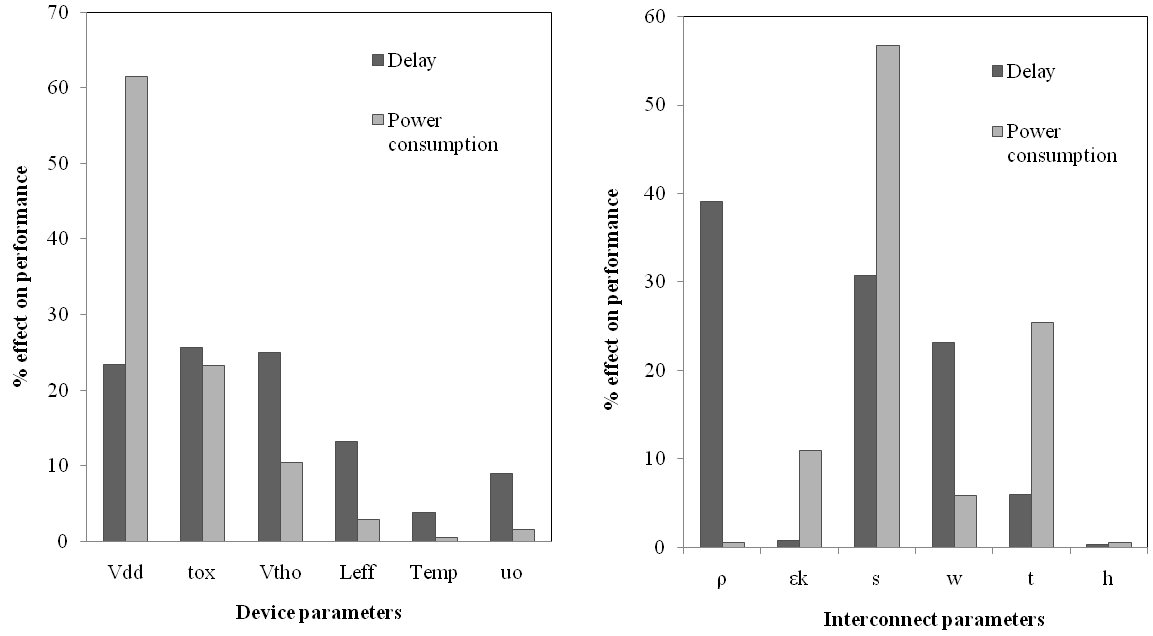
as shown in Table 5.5. Although mLVSD scheme has less deviation in delay compares to nLVSD scheme but in terms of dynamic power variation, it deviates more. In order to distinguish the best driver scheme in terms of robustness against variability, SNR is chosen to be the deciding design metric as it comprises components that associate with process variations such as receiver sensitivity and receiver input offset. The results for all four schemes are shown in Table 5.6, which indicates that the mLVSD driver scheme is the most robust against noise and process variation among all four schemes.

Table 5.6: Noise comparisons between low-swing signalling schemes.

Schemes	Rx_O(V)	Rx_S(V)	Vnoise(V)	SNR
mLVSD	0.04	0.02	0.15	1.58
nLVSD	0.04	0.02	0.13	1.29
MJD	0.05	0.03	0.17	1.41
DDC	0.08	0.05	0.2	1.03

5.3.1.2. Design-of-Experiment (Central Composite Design) Analysis

From the previous Monte Carlo analysis and the power-delay comparison between the four driver schemes, the results obtained indicate that the proposed driver schemes, namely, the mLVSD and nLVSD perform better than DDC and MJ-driver schemes in terms of delay and power consumption, even under process, voltage and temperature variations. To gain a better understanding of which process parameters have the greatest impact on performance, the mLVSD-driver scheme was further analyzed as this had a better performance profile than the other 3 driver schemes. The analysis was performed using Design-of-Experiment method together with Plackett-Burman analysis to distinguish the most significant parameters among the process variations. A statistical tool called Minitab can both perform DoE and Plackett-Burman analysis. Based on the number of known process parameters, statistical models for both analyses were created. With delay and power consumption as the outputs for these analyses, both outcomes are simulated using Cadence Spectre based on the inputs given by the statistical models. These data are then processed by Minitab. For Plackett-Burman analysis, the results from Minitab are presented in Figure 5.7 for both device and interconnect parameters and will be discussed in the following subsections.



(a) (b)

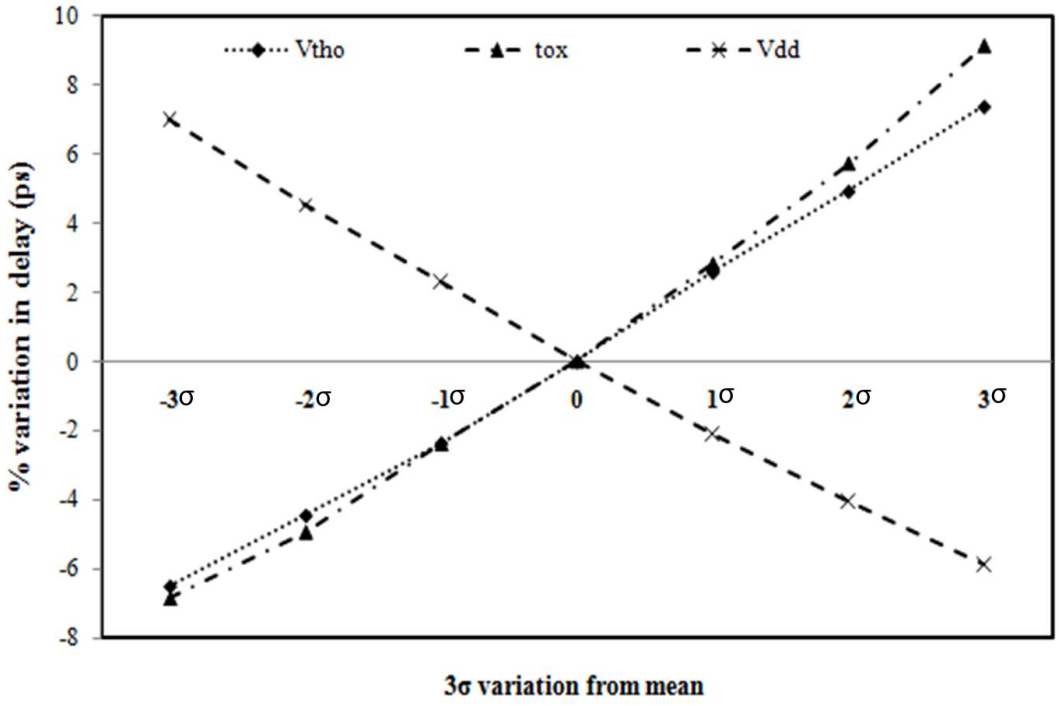
Figure 5.7: The results of Plackett-Burman analysis on (a) device and (b) interconnect parameters.

5.3.1.2.1. The effect of device variation

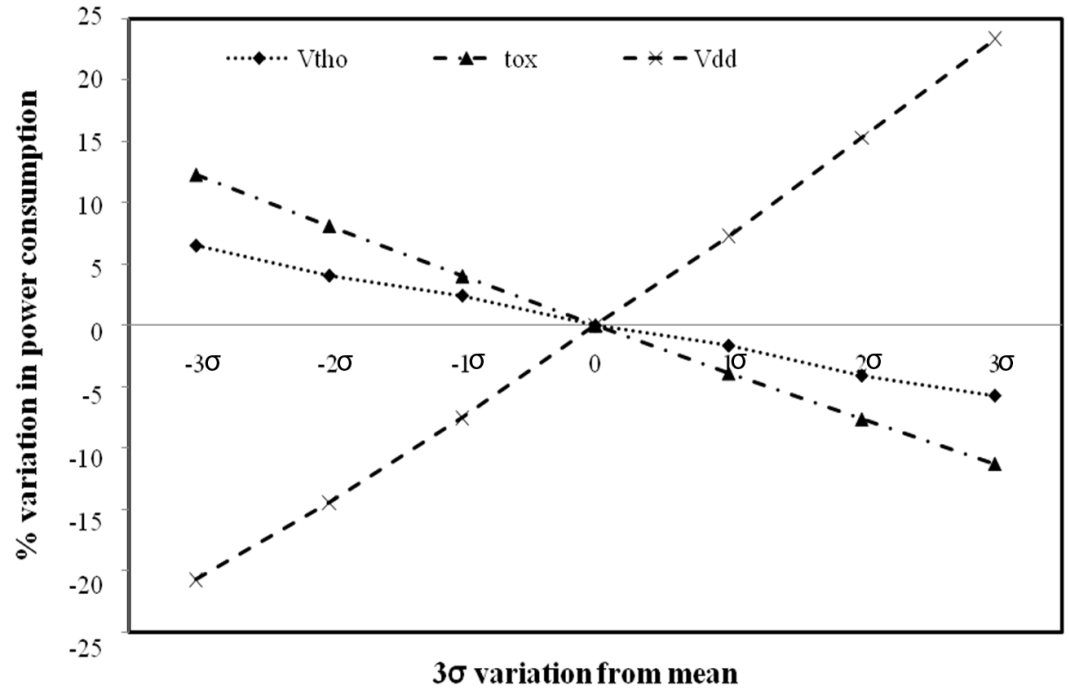
First, an individual parameter sensitivity analysis on the delay and power consumption for a 10mm line was undertaken by varying the device parameters, shown in Table 5.4 along with *Vdd*, individually with the other device parameters at their nominal value. Figure 5.8(a) shows the dependence of delay for a 10mm line at 90nm technology on the threshold voltage (*Vtho*), oxide thickness (*tox*) and supply voltage (*Vdd*). Scaling down the threshold voltage will greatly affect the delay. This can be seen in Figure 5.8(a), where there is a steep decrease in delay as the threshold voltage is reduced. For a *MOSFET* transistor, either operating in a saturated or non-saturated mode, the driving current is directly proportional to *Vgs-Vtho*; thus if the threshold voltage is reduced, the driving current will rise, which leads to faster switching speed.

Furthermore, from Figure 5.8(a) it is seen that the effect of *tox* towards delay is similar to *Vtho*, with a slightly decrease as *tox* is reduced. From a performance point of view, a thinner gate oxide is preferred if the reliability concerns can be met. A thinner gate oxide also leads to shallower junction depth, providing greater control over short channel effects affecting the threshold voltage of the transistor, resulting in smaller gate delay and faster device performance. Gate oxide thickness, *tox*, as well as contact potential, $2\Phi_F$ are the major

influences that contribute to changes in threshold voltage. Therefore, any changes in gate oxide thickness will also change the threshold voltage. This indicates the high correlation between *tox* and *Vtho* towards propagation delay.



(a)



(b)

Figure 5.8: Effect of device variability on (a) delay and (b) power consumption.

The dependence of power consumption for a 10mm line at 90nm technology on *tox*, *Vtho* and *Vdd* is shown by Figure 5.8(b). The trend in power consumption with *tox, Vtho and Vdd* are completely opposite to the trend in delay; in this instance the power consumption has a negative correlation with *tox* and *Vtho*; and the variation in delay according to *tox* and *Vtho*, as shown in Figure 5.8(a), is higher than that of power consumption for ±3σ values. Figure 5.8(b) also shows, as expected, that the power consumption is very sensitive to variation in *Vdd* due to the quadratic relationship. The variation in power consumption due to *Vdd* variability is almost double the variation due to *tox* and *Vtho*. Overall, Figure 5.8 shows the classic delay-power trade-off that is used by designers for the optimization of one parameter by relaxing the other.

5.3.1.2.2. Sensitivity towards interconnect variation

A similar procedure to analyse the effect of process variations on device performance was performed on the interconnect. The interconnect parameters ε_k and ρ will not be included in the analysis, although they contribute significantly to the interconnect values as shown in Figure 5.7(b). This is because both these parameters are usually well controlled [3]. Focussing on the interconnect dimensions, *w*, *s* and *t* which are the most significant parameters that could affect both delay and power consumption. The essential components of interconnect are its resistance, R_W and capacitance, C_W. The effect of variations in *w* and *t* on R_W and C_W is shown in Figure 5.9.

Figure 5.9 describes the variation in wire capacitance and resistance as the width and thickness varies at +20%, while the wiring pitch ($s + w$) remains constant. The direction of the graph indicates the relationship between R_W and C_W with *w* and *t*. When *w* and *t* increase, the interconnect resistance decreases while the interconnect capacitance increases, when *w* and *t* decrease the converse occurs. The significant change in resistance and capacitance variations are reflected in the delay, where the variation in the wire resistance is significantly greater than the wire capacitance. Thus, considering the delay in the form of time constant ($R_W C_W$), the fluctuation in delay is between -16.7% and 9.1% to the ±20% variation in *w* and *t*.

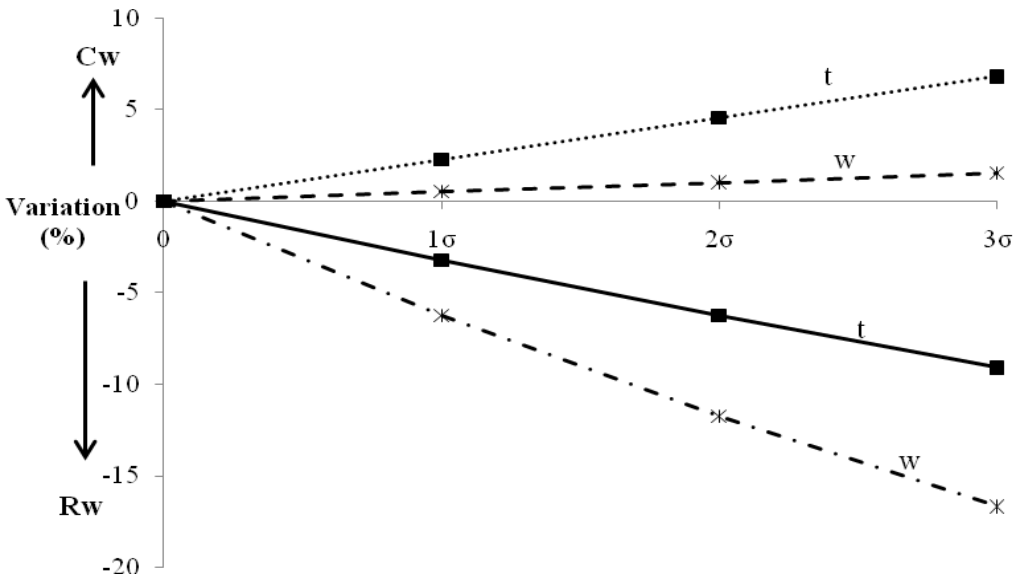


Figure 5.9: The effect of variations in interconnect width and thickness on its resistance and capacitance.

From Figure 5.10, there are 3 cases; s=w, s=2w and s=3w in which the 3σ variation of Cw and delay were measured for each case. The 3σ variation is interpreted as a percentage of variation from the means. For each case, the results were computed using the Monte Carlo tool in Cadence Virtuoso Analog Design Environment where the 3σ variation for the delay and Cw were retrieved from the histograms produced by the tools. Figure 5.10 indicates, as the interconnect spacing increases, the variation of C_W decreases. This indicates that the effect of C_W on delay becomes smaller as the spacing becomes wider. The variation of R_W is independent of the interconnect spacing. When the interconnect spacing becomes wider, the variation of R_W is unchanged while the variation of C_W becomes smaller, which indicates that R_W has more impact on delay than C_W, thus the variation of delay also increases. In the case of $s = w$, when w and t fluctuate between +20% and -20%, delay varies between -10% and 19%, whilst in the case of $s = 6w$, delay varies between -16% and 30%.

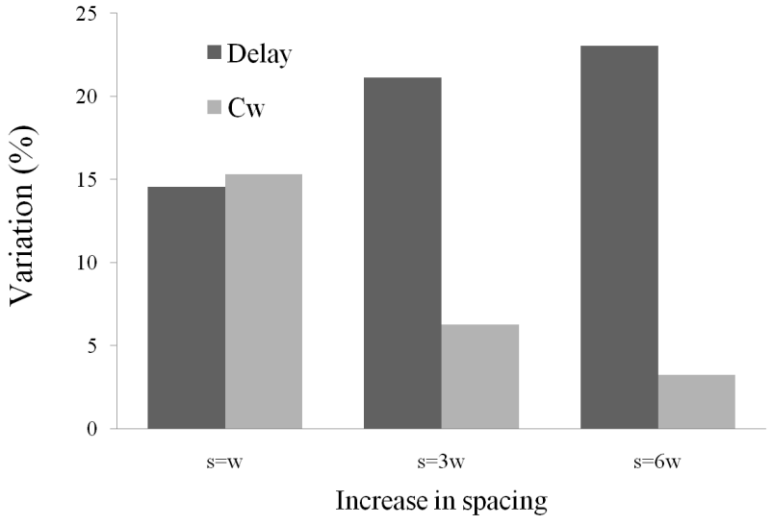
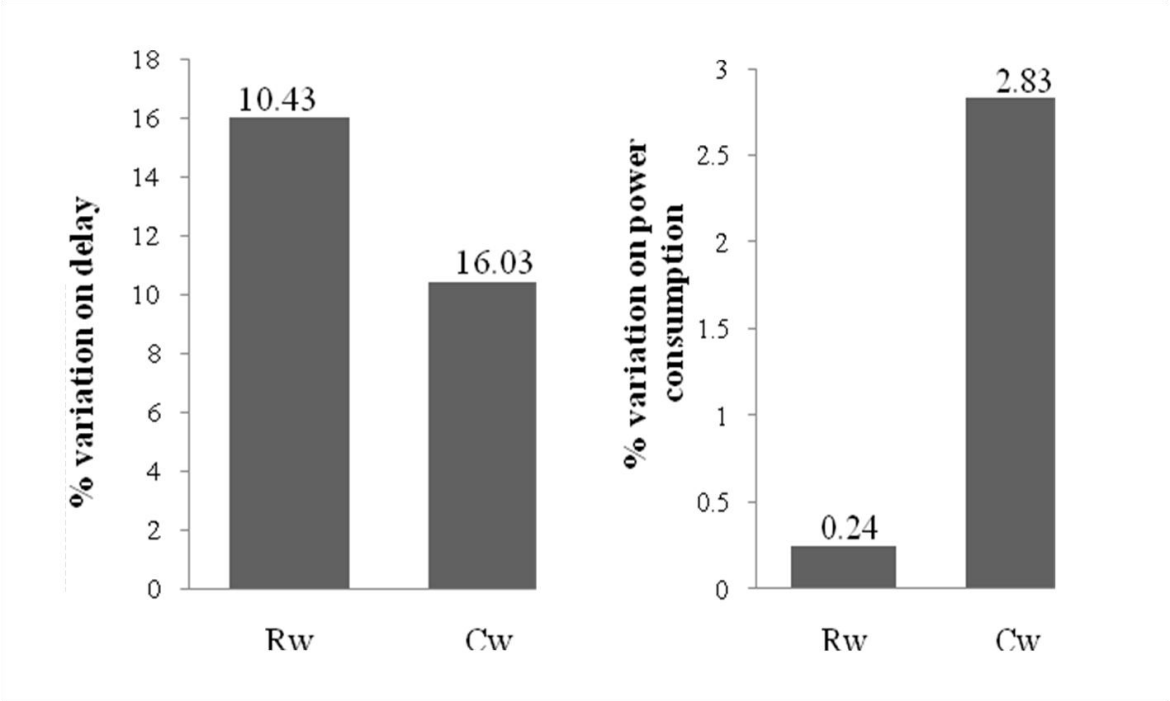


Figure 5.10: Variations in delay and interconnect capacitance to the effects of width and thickness due to the increase in spacing.

The interconnect variation can also influence the power consumption as shown previously in Figure 5.7(b). Although the physical parameters ε_k and ρ have a significant effect on power consumption and delay, they are unlikely to be altered during the fabrication process. Consequently the only interconnect parameters to be subjected to process variation are *s*, *w* and *t*. The variability in wire resistance and capacitance correlate with one another to variations in delay as shown in Figure 5.11(a). However the variation in power consumption has the greatest contribution from changes in wire capacitance as shown in Figure 5.11(b). From Figure 5.12, the analysis on the interconnect variation indicates a high variation of power consumption with regards to interconnect spacing and thickness, as its ±20% variation contributes to about 6% and 5% respectively to the variability in power consumption. However, interconnect width has a small effect on power consumption as it only causes about 1% variability in power consumption.



(a) (b)

Figure 5.11: The variation on (a) delay and (b) power consumption in terms of interconnect parasitic components.

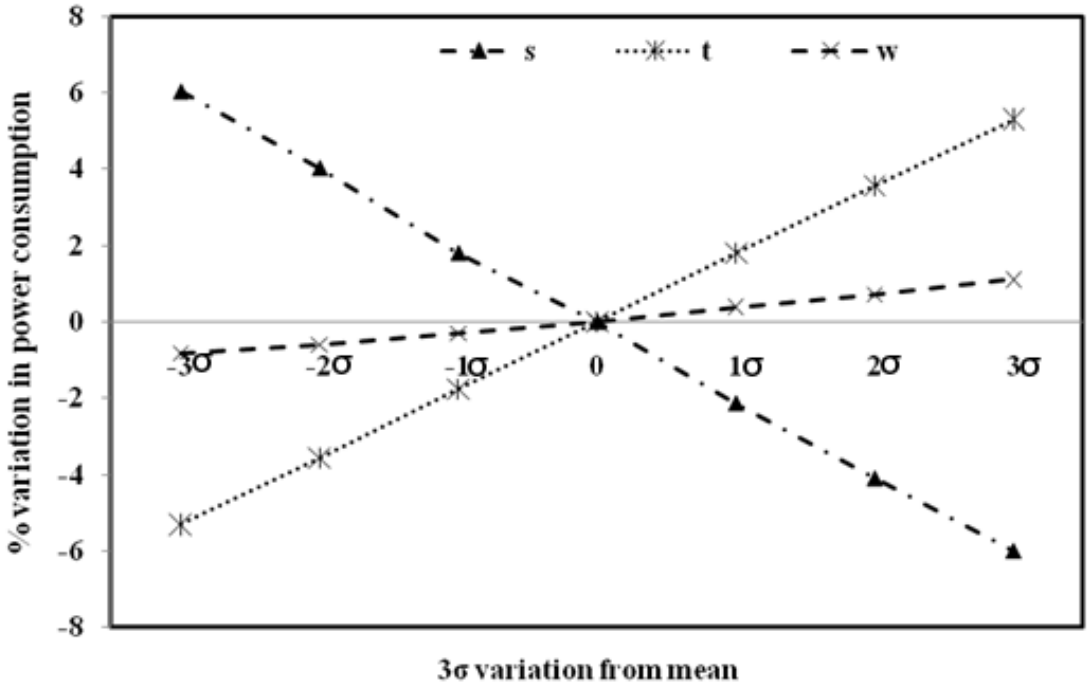


Figure 5.12: Effect of interconnect variability on power consumption.

5.3.2. Analysis and modelling of the crosstalk effects on the mLVSD driver scheme.

For simplicity, in the following analysis, 8 sources of variations were considered, namely, supply voltage, temperature, threshold voltage, effective gate length, metal wire resistivity, wire width, wire thickness and inter-layer dielectric thickness. The wire width and spacing are assumed to be negatively correlated, letting *w* be the independent variable. The same goes for *Vth* as it is used instead to represent both *Vtho* and *tox*. The variables were listed previously in Table 5.4 with their 3σ variations. The wire width used in this analysis is the minimum wire width in 90nm technology.

5.3.2.1. Impact of variability on crosstalk delay

Figure 5.13 shows the interconnect structure used in the analysis of the impact of process variation on crosstalk effects. The *DoE* (*CCD*) method outlined previously is used in this analysis to build a linear model based on Equ.5.1. In this instance the linear model of the delay of the middle (*victim*) line in Figure 5.13 is given by Equ.5.3.

$$D = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \cdots + \beta_i x_i \qquad (5.3)$$

where *x* is a variation parameter, which in this case are *Vdd*, *Temp*, *Leff*, *Vth*, ρ, *w*, *t* and *h*, and β is a regression coefficient.

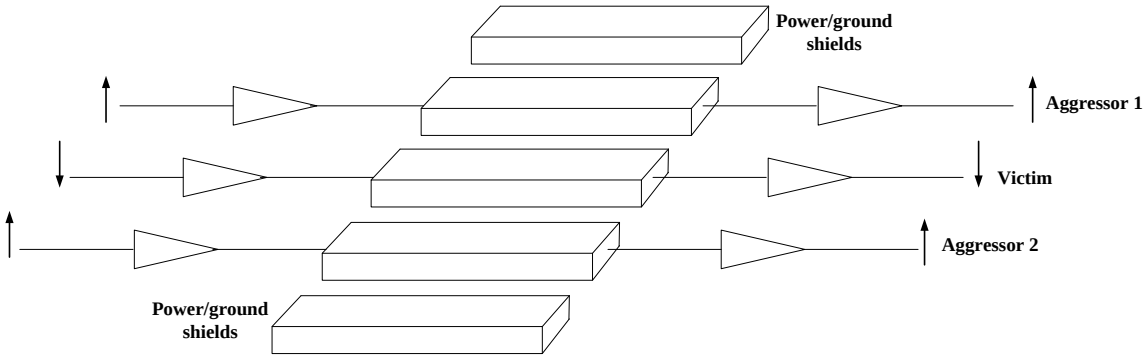


Figure 5.13: Circuit structure for variability analysis on crosstalk effects.

In the previous chapter, several design methods have been discussed in mitigating the problems associated with crosstalk delay. The same methods are also considered in the variability analysis of crosstalk delay, namely, buffer insertion and increased wire spacing.

Subsequently, general models for a 10mm interconnect were generated for the following cases: minimally spaced wire ($s = w_{min}$) with no buffers, minimally spaced wire with 3 buffers and 3 times minimally spaced wires ($s = 3w_{min}$) with no buffers. The accuracy of these models was validated using R^2 fits analysis, which was found to be above 99% for all considered cases. R-squared (R^2) is the percentage of the response variable variation that is explained by its relationship with 1 or more variables. In general, the higher the value of R^2 the better the model fits the data. R^2 is always between 0 and 100%. It is also known as the coefficient of determination or multiple determinations (*in multiple regressions*).

Similar models are also generated for each crosstalk cases as shown in Table 5.7 indicating effective crosstalk capacitances for different crosstalk cases. Notes that ↑, ↓ and – imply 0-to-1, 1-to-0 and no transitions respectively.

Table 5.7: Effective crosstalk capacitance for different Crosstalk cases [15].

Crosstalk case	Transitions	Effective Coupling Capacitance
1	↑↑↑, ↓↓↓	0
2	↑↑–, –↑↑ ↓↓–, –↓↓	1
3	–↑–, –↓– ↓↑↑, ↑↓↓ ↑↑↓, ↓↓↑	2
4	↓↑–, –↓↑ –↑↓, ↑↓–	3
5	↓↑↓, ↑↓↑	4

As expected, delay sensitivity to variation parameters increases from Crosstalk Case 2 to 5 due to the increase in effective crosstalk capacitance. $^{dD}/_{dx}$ in Figure 5.14 till 5.16 represents delay sensitivity over the variation parameters, where the results were obtained through Minitab. From Figure 5.14, the results indicate that both *Vdd* and ρ have the highest impact on crosstalk delay variations as both of these parameters have the most significant association with delay as discussed previously in Section 5.3.1.2. Delay is linearly dependent on the wire resistance as well as being negatively correlated to *Vdd*. Subsequently this result also shows that delay sensitivity to wire parameter variations has a very high data dependency due to the changes in the effective crosstalk capacitance for each different case.

This dependency can be reduced by incorporating 3 buffers as shown in Figure 5.15, by the significant decrease in delay sensitivity to wire parameter variations. By increasing the wire spacing, the dependency of delay sensitivity on wire parameters can also be reduced but not as much as using the buffer insertion method as shown in Figure 5.16; however, this method can be used to reduce the delay sensitivity to device parameters. This is because by increasing the wire spacing, contributing to the decrease in delay by reducing the wire capacitance without affecting its resistance, which causes the contribution of the driver circuitry to the overall delay to be reduced.

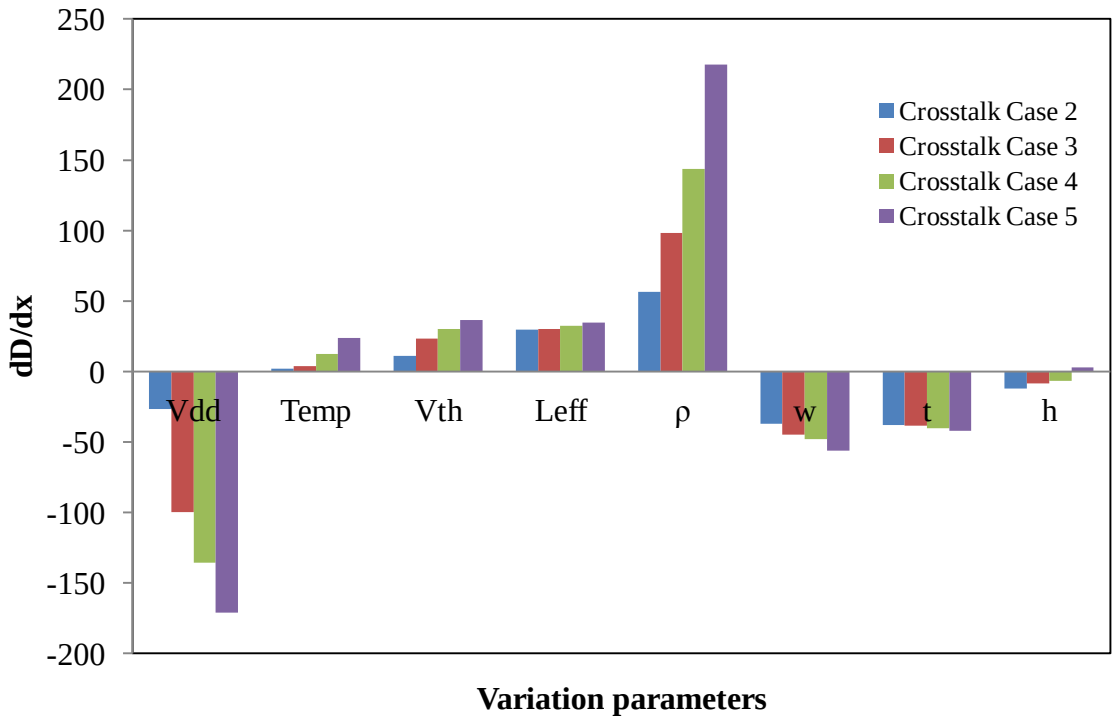


Figure 5.14: Delay sensitivity to variability of minimally spaced wire with no buffer.

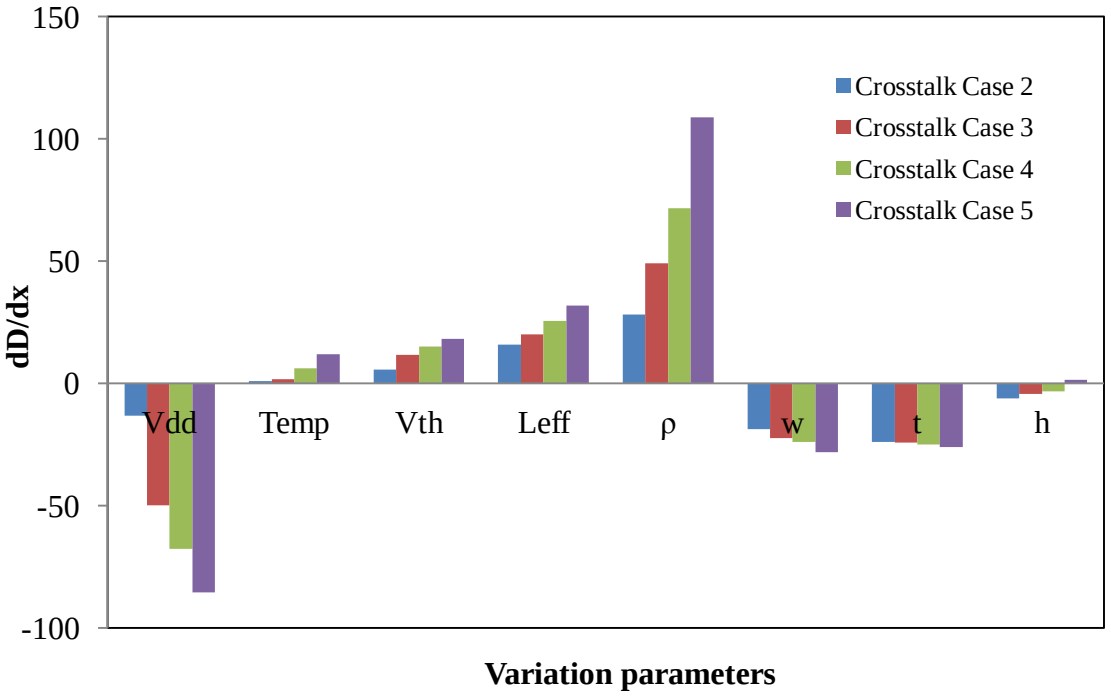


Figure 5.15: Delay sensitivity to variability of minimally spaced wire with 3 buffers.

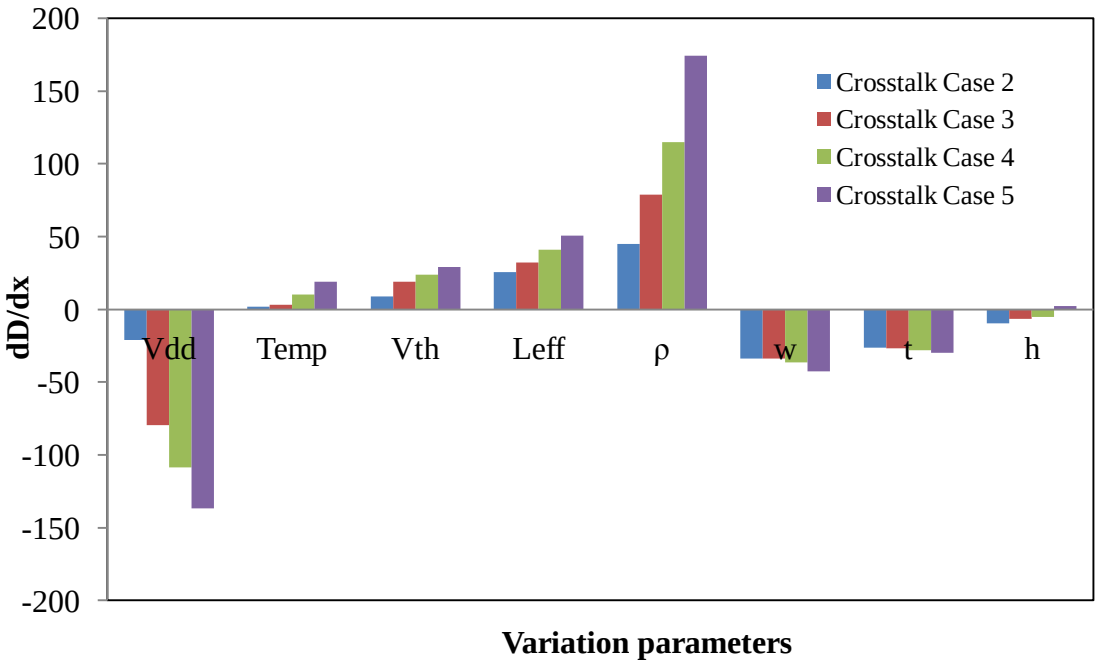


Figure 5.16: Delay sensitivity to variability of a 3 times minimally spaced wire with no buffer.

In addition to the first order or linear model generated, a second order or non-linear model of the crosstalk delay can also be generated. This model comprises interaction and quadratic effects between parametric variations, where its polynomial approximation is as shown in

Equ.5.2. The results obtained through Minitab for the non-linear model are presented in Figures 5.17 to 5.20, where the coefficients indicated in these figures represent regression coefficients (β), referring back to Equ.5.3

A comparison between second order and linear coefficients from Figure 5.14 indicates that the linear coefficients are more significant. Subsequently most of the non-linear effects can be ignored as they have very little impact on the model accuracy. However, as can be seen in Figure 5.17 the quadratic effect of *Vth* is relatively large representing the only significant parameter from the device parameter variations while from the interconnect parameters, the quadratic effects of wire width and dielectric thickness are found to be significantly large. This is because of the dependency of voltage swing on *Vth*, which can affect the delay significantly, and the quadratic effects of w and h contribute to the changes in effective crosstalk capacitance, hence deviations in crosstalk delay. Additionally, the interaction between *Vdd* and ρ also contribute to the large coefficients for delay sensitivity. From Figure 5.14, both *Vdd* and ρ are the most significant parameters to affect delay sensitivity, thus their interaction will have large impact on the delay sensitivity.

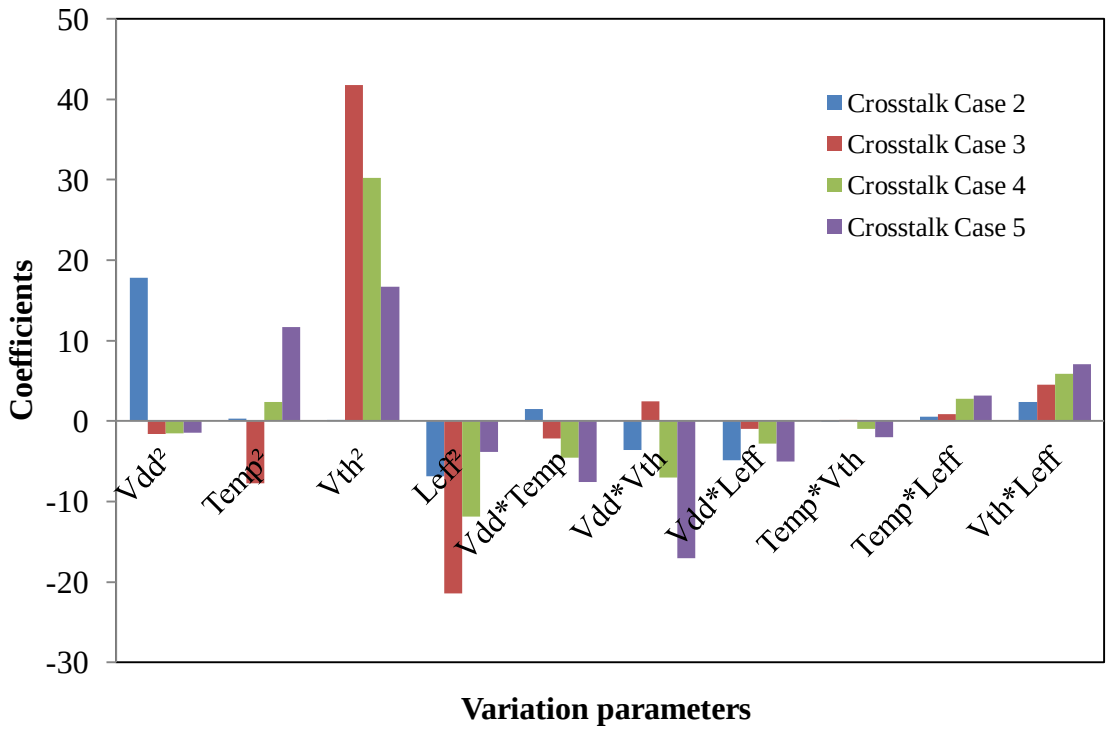


Figure 5.17: Interaction and quadratic coefficients of device and environmental parameter variations.

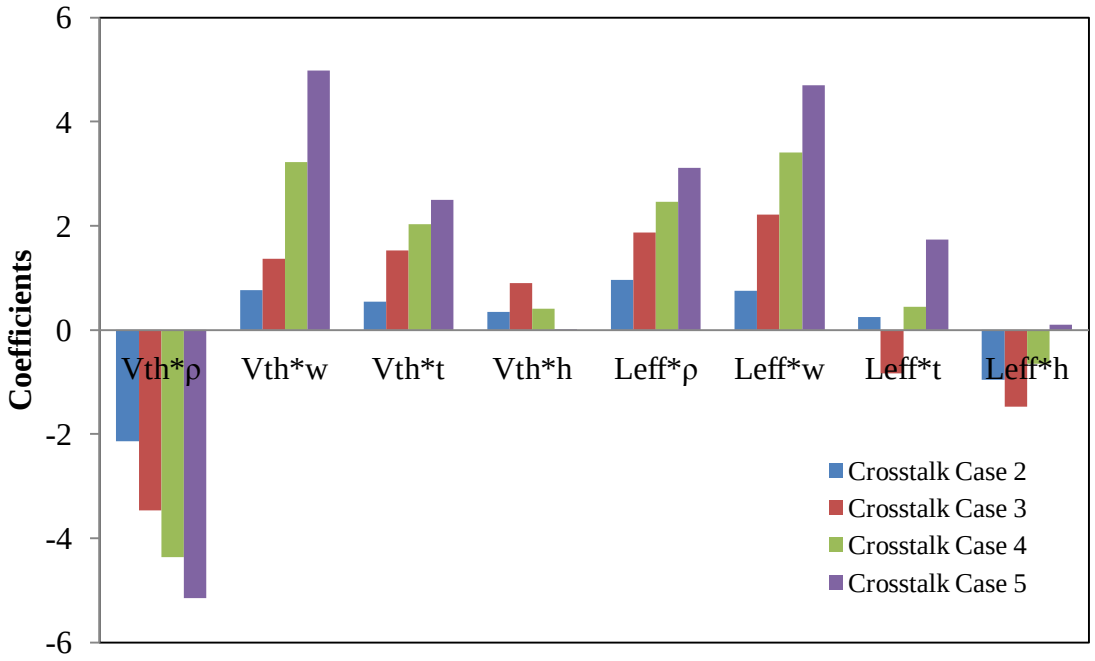


Figure 5.18: Interaction coefficients of device and wire parameter variations.

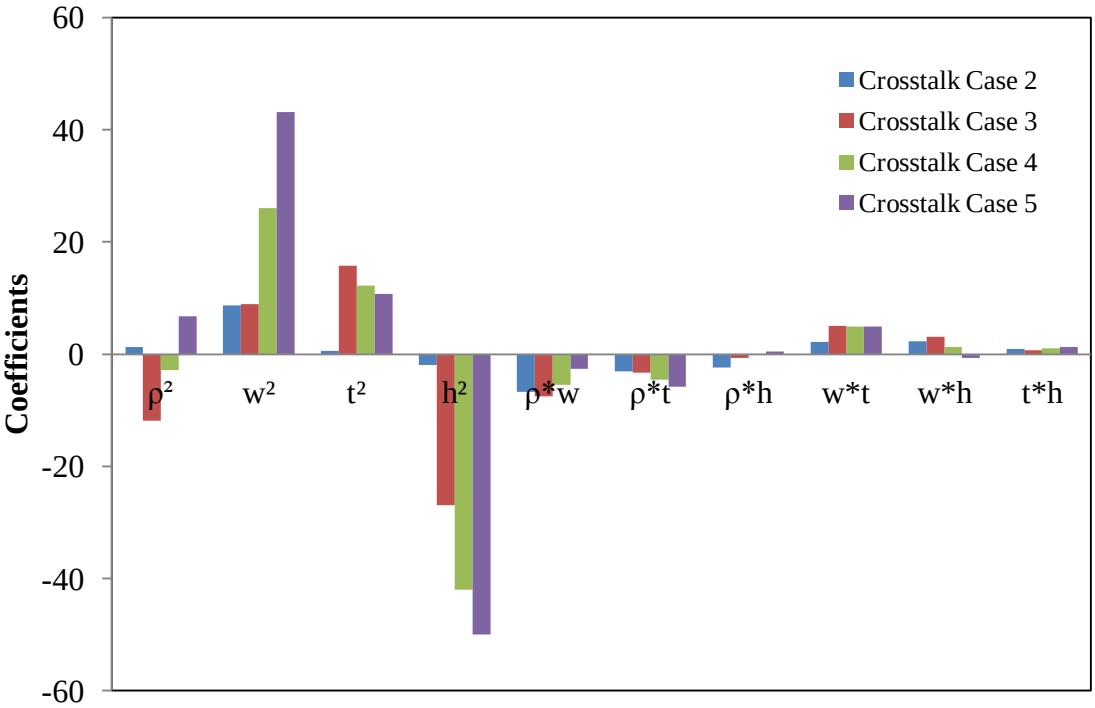


Figure 5.19: Interaction and quadratic coefficients of wire parameter variations.

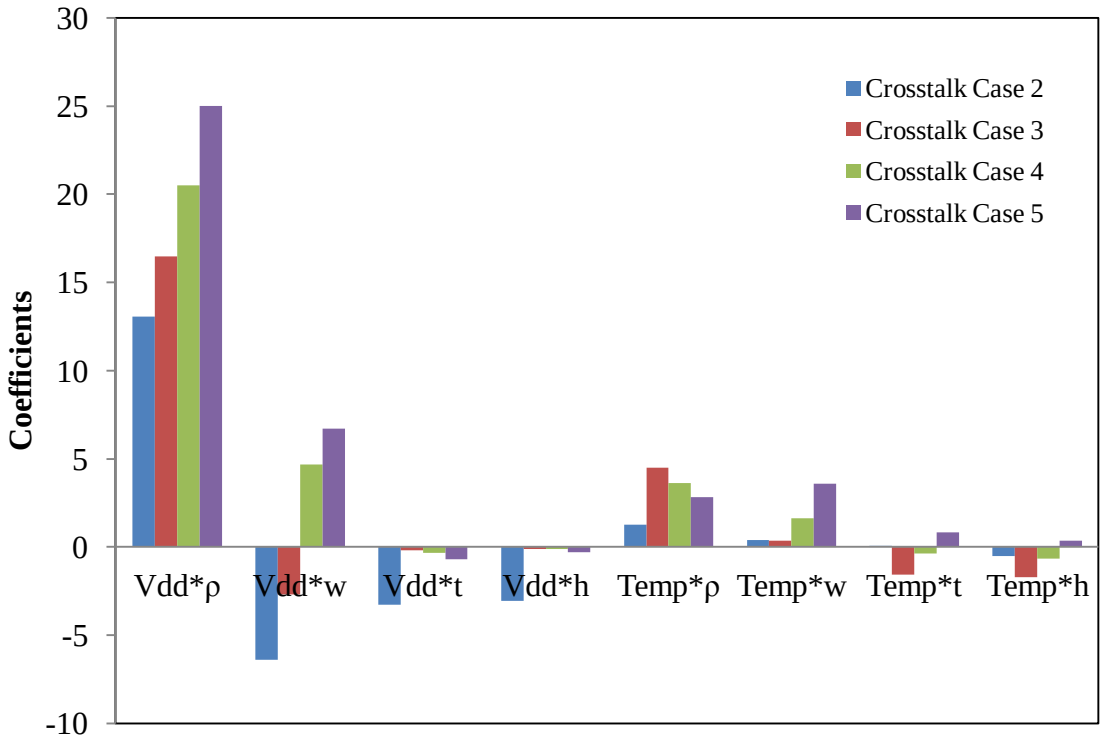


Figure 5.20: Interaction coefficients of wire and environmental parameter variations.

5.3.2.2. Impact of variability on crosstalk glitch

The *DoE* (*CCD*) technique was employed in this analysis to build a polynomial approximation of the crosstalk glitch induced on the middle line in Figure 5.13. There are three types of crosstalk glitches resulting from:

Case 1: the switching of two aggressor wires in different directions

Case 2: the switching of one aggressor wire

Case 3: the switching of two aggressor wires in the same direction

However, the crosstalk glitch resulting from the switching of two aggressor wires in different directions is ignored as its impact is considered insignificant, thus only cases 2 and 3 are considered in this analysis.

In order to investigate the sensitivity of the glitch to parametric variations, linear models of crosstalk glitch in each case are generated for minimally spaced wire with no repeaters. The polynomial approximation of the linear model as shown in Equ.5.1 is used to represent the crosstalk glitch is given by Equ.5.4.

$$G = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \cdots + \beta_i x_i \quad (5.4)$$

where G represents the crosstalk glitch, x_i represents variation parameter which in this case are *Vdd*, *Temp*, *Leff*, *Vth*, ρ, *w*, *t* and *h*, and β_i is regression coefficient for each variation parameter respectively. R^2 was found to be around 99% for all cases.

From Figure 5.21, the results indicate sharp increases in crosstalk glitch sensitivity to all variation parameters in Cases 2 and 3. $^{dG}/_{dx}$ in Figure 5.21 and 5.22 represents glitch sensitivity over the variation parameters, where the results were obtained through Minitab. Crosstalk glitch sensitivity to wire parameter variations has a very high data dependency especially *w*, which is one of the main contributors to effective crosstalk capacitance. However, changes in *Vdd* have also a sizeable contribution to the overall variations. These results are supported by their linear relations to the crosstalk glitch, as shown below [16]:

$$G = V_{peak} = V_{dd} \times \frac{C_C}{t_{aggressor}} \times R_{victim} \quad (5.5)$$

where C_C is the effective crosstalk capacitance, R_{victim} is the wire resistance of the victim line and $t_{aggressor}$ is the switching slew rate of the aggressor line.

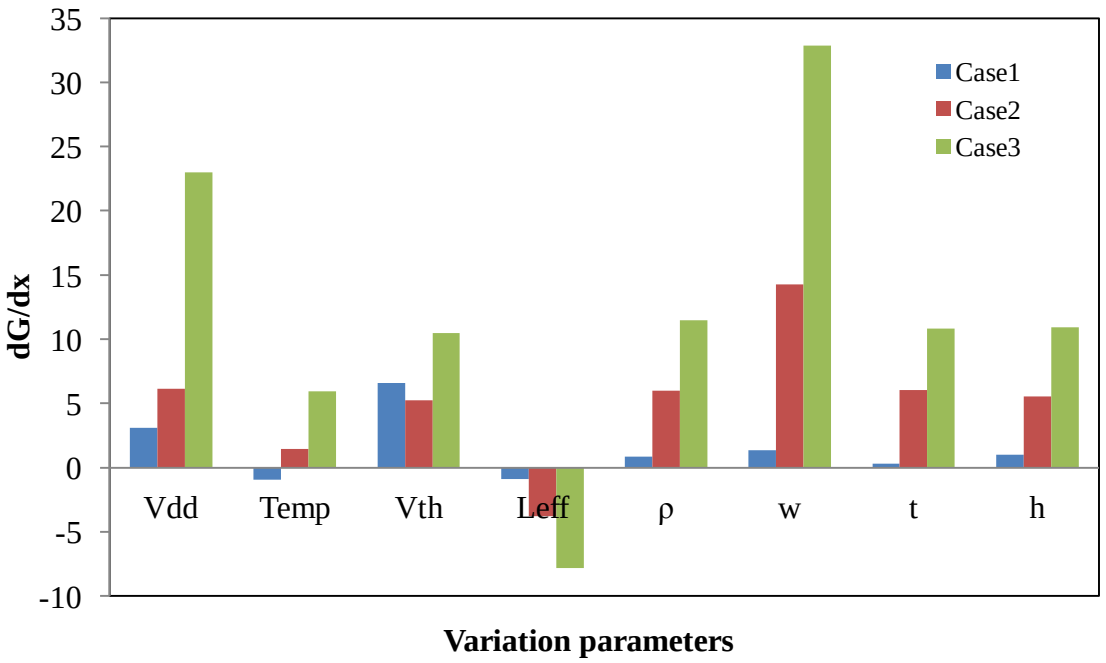


Figure 5.21: Crosstalk glitch sensitivity to variability of a minimally spaced wire with no buffer.

The next step is to investigate the impact of buffer insertion and wire spacing on crosstalk glitch sensitivity to variation parameters. The same linear model is used for the crosstalk glitch of Case 2 with the same interconnect geometry but with $s = 3w_{min}$ for wire spacing analysis, and $s = w_{min}$ with 3 buffers for buffer insertion analysis. A comparison of the results is shown in Figure 5.22. The decrease in the crosstalk glitch sensitivity is more significant through the wire spacing method as it is known to be the most effective way in reducing crosstalk noise. Increasing the distance between the adjacent wires will result in reduction of crosstalk capacitance and thus the crosstalk glitch. With buffer insertion, the crosstalk glitch sensitivity to the wire parameter variations is reduced but there is a slight increase in dependency towards the device parameter variations. This is due to the use of buffers which contribute to the increase in the crosstalk glitch dependency of *Leff*, which is contributed by the driving capability of the low-swing driver and buffers.

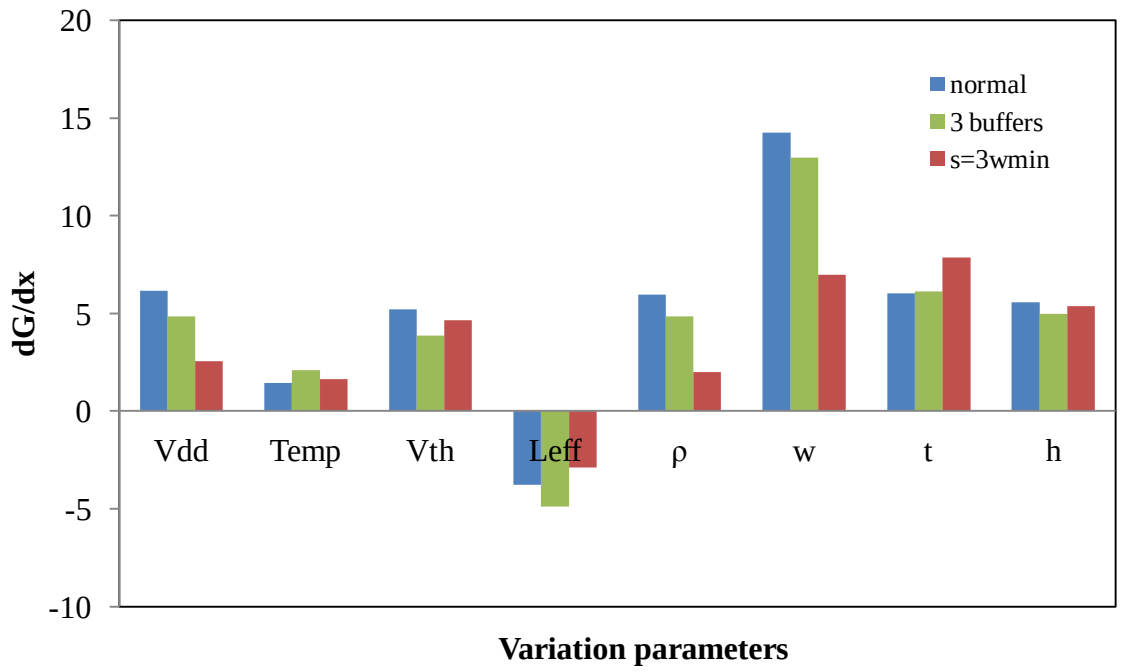


Figure 5.22: The impact of wire spacing and buffer insertion on crosstalk glitch sensitivity to variability.

For cases 2 and 3 second order models for the crosstalk effects on the centre (victim) line in Figure 5.13 were generated using Minitab to observe the interaction and quadratic effects on the crosstalk glitch variations. The accuracy of these models was validated using R^2 fit analysis which was found to be more than 99% for all cases. For this analysis, a 10mm minimally spaced wire with no repeaters was considered. The results are as shown in Figures 5.23 to 5.26. The coefficients stated in Figure 5.23 to 5.26 represent the regression

coefficients (β) for each variation parameters, which in this case are the interaction and quadratic effects of the process parameters. A comparison was made between the second order models and the linear models shown in Figure 5.21. The comparison clearly indicates that the linear coefficients are more significant. The non-linear effects can totally be ignored as they will not have a significant impact on the model accuracy.

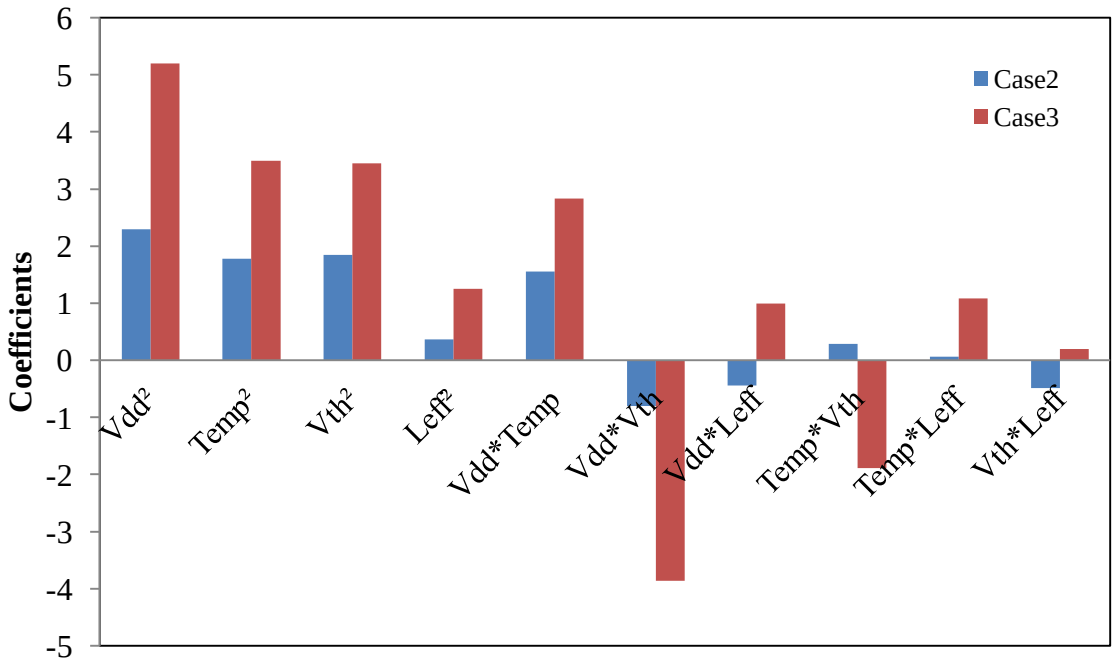


Figure 5.23: Interaction and quadratic coefficients of device and environmental parameter variations.

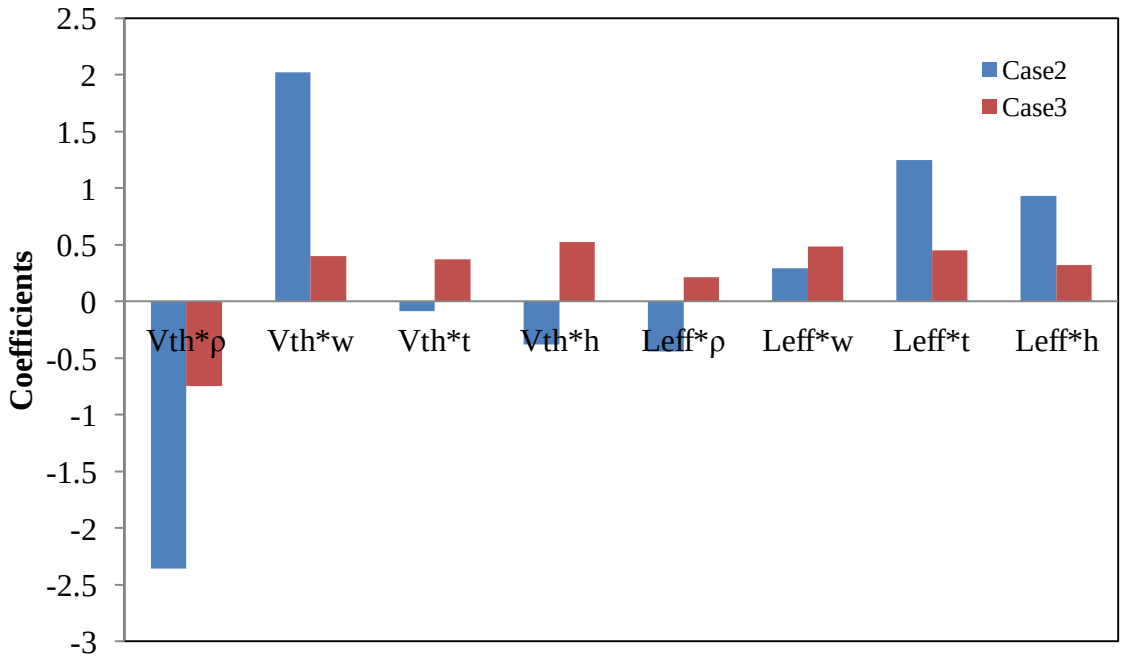


Figure 5.24: Interaction coefficients of device and wire parameter variations.

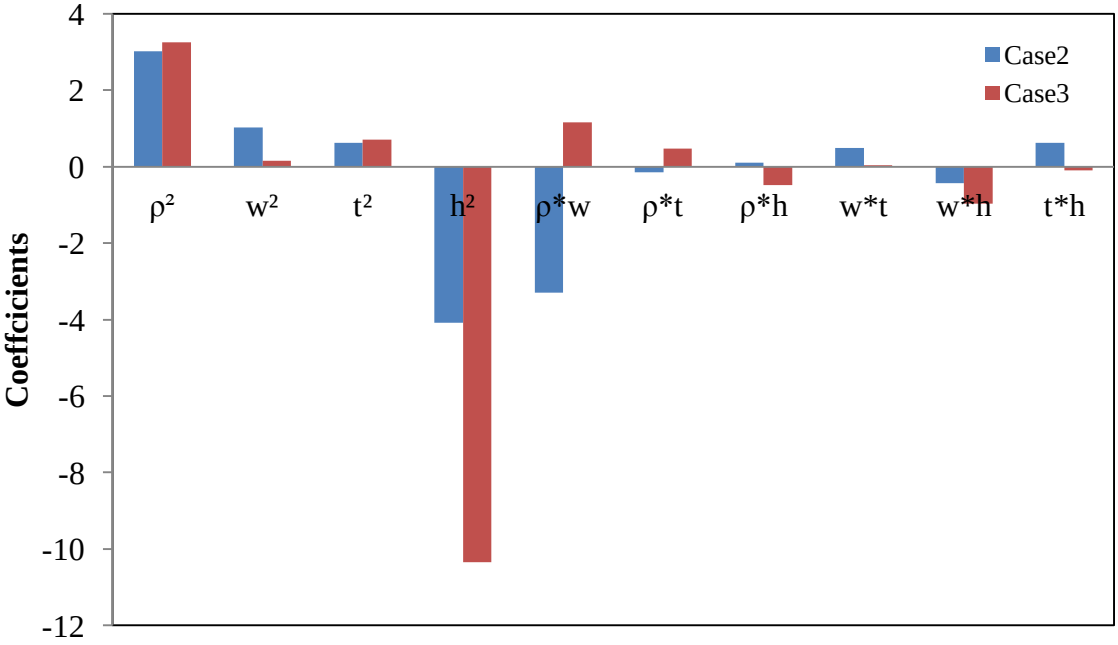


Figure 5.25: Interaction and quadratic coefficients of wire parameter variations.

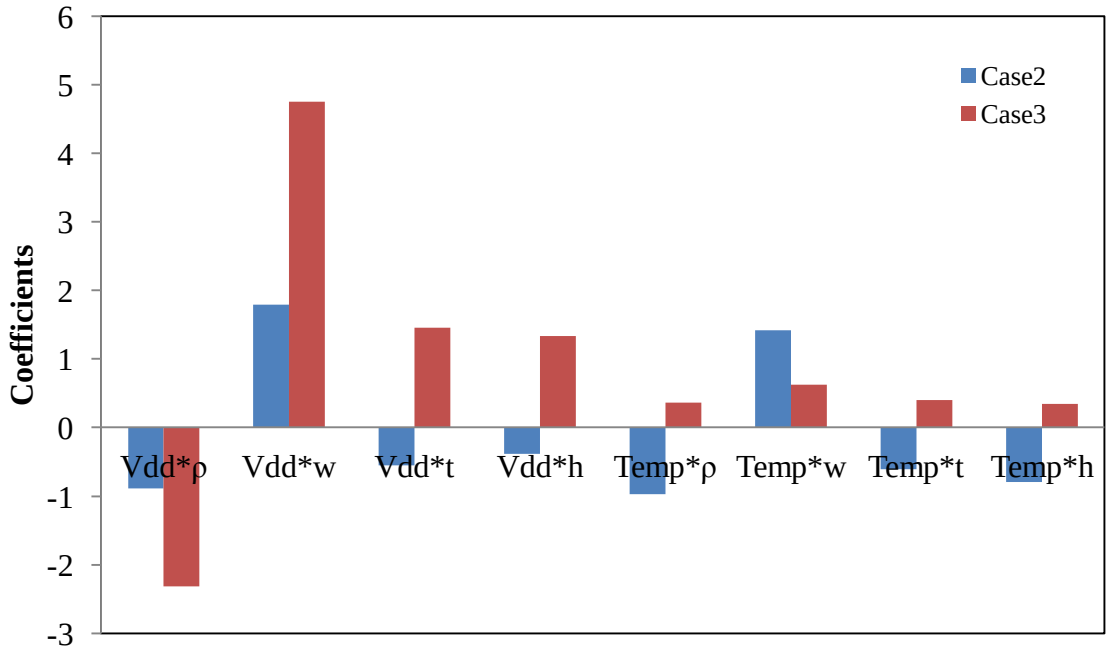


Figure 5.26: Interaction coefficients of wire and environmental parameter variations.

5.4. Summary

In this chapter, a detailed introduction to variability which highlights the type of variations that are common in the nano-metre regime was given. The statistical methods which are used in the process variation analysis are introduced comprising corner based analysis, Monte Carlo analysis and the Design of Experiment (*DoE*). These methods were briefly discussed in terms of advantages and disadvantages, which highlight the reasons for employing *DoE* analysis in this work. The work flow for the *DoE* analysis was also introduced and is divided into 2 sets of experiments, namely; the single signalling without considering crosstalk effects, and signalling with crosstalk effects. The responses for the first set of experiment are delay, power consumption and *SNR* whilst crosstalk delay and glitch are the output responses for the second set.

The first set of experiments involved a Monte Carlo analysis and followed by *DoE*. All four low-swing signalling schemes (mLVSD, nLVSD, MJD and DDC) were used for the Monte Carlo analysis, where the results indicate that the proposed driver schemes, i.e. the mLVSD and nLSVD driver schemes are more robust compared to DDC and MJ-driver schemes. The mLVSD driver scheme has less deviation in delay compared to the nLVSD driver scheme but the nLVSD driver scheme is more robust in terms of power consumption. However, the mLVSD driver scheme has a better performance profile due to its robustness against noise variability.

To gain a better understanding of which process parameters had the greatest impact on performance, the mLVSD-driver scheme was further analyzed as this had a better performance profile among all low-swing signalling schemes tested in this work. In terms of device variations, the most significant parameters are *tox* and *Vtho*, and *Vdd* representing the environmental variation. The trends in power consumption with *tox*, *Vtho* and *Vdd* are completely opposite to the trend in delay. This means that the variations in *tox* and *Vtho* have positive correlations with the delay but negatively correlate with the power consumption. The same scenario also applies for *Vdd* as its variation causes an increase in variability of power consumption but a decrease in delay variation. The positive correlation between *Vdd* and power consumption is due to its quadratic relationship. The negative correlation of *Vdd* with regards to delay is due to the driving current, which decreases when *Vdd* decreases, which results in slower circuit. This has opposite effect on *Vtho* and *tox*, as the driving current increases with the reduction of both these parameters, resulting in faster circuit.

Similar trends can also be seen for interconnect variations. Firstly, the most significant parameters regarding interconnect are *s*, *w* and *t*. As *w* and *t* increase, R_W decreases while C_W increases, which overall causes the delay to decrease. The results also show that the delay variation increases when the spacing becomes wider but the delay itself is decreasing. However, this has an opposite effect on power consumption, as the variation in power consumption increases with *w* and *t*, but decrease with interconnect spacing.

Further analysis was carried out to investigate the impact of variability on crosstalk effects of the mLVSD driver scheme. Both linear and non-linear models were generated for crosstalk delay and glitch. The results indicate that the delay and glitch sensitivities have a high data dependency towards *Vdd* and wire parameter variations. This dependency can be reduced through buffer insertion and wire spacing with latter method being most effective for reducing delay disparity whilst wire spacing is found to be the most effective method in reducing variability in crosstalk glitch production. Results from the second order models indicate that most of the non-linear effects can be ignored as they do not impact significantly on the model accuracy. However, few parameter contributions such as the quadratic effects of *Vth*, *w* and *h* and interactions between *Vdd* and ρ should be considered as they can be regard as significant to the crosstalk delay sensitivity compared to the linear coefficients.

Through this work, both of the proposed driver schemes, namely the mLVSD and nLVSD drivers have proven to be more robust and reliable compared to other diode-connected drivers, namely, the MJ and DDC driver circuits, tested in this work, in terms of low power, high speed and robustness against process variation. The most influential process parameters in device and interconnect variations have also been identified permitting fabrication process choice to be made depending on whether the main design criteria is performance or power consumption. This can also be applied to the variability analysis on the crosstalk effects as the most significant variables as well as their interactions and quadratic coefficients have been identified which aids in distinguishing the right process choice on whether the response of interest is crosstalk delay or glitch.

References

[1] O.S. Unsal, J.W. Tschanz, K. Bowman, V. De, X. Vera, A. Gonzalez, and O. Ergin, "Impact of Parameter Variations on Circuits and Microarchitecture," *IEEE Micro*, vol. 26, 2006, pp. 30-39.

[2] "International Technology Roadmap for Semiconductors," *www.itrs.net accessed January 2010*.

[3] W.J.B. A.P. Chandrakasan F. Fox, *Design of High-Performance Microprocessor Circuits*, New York: IEEE Press, 2001.

[4] K.A. Bowman, S.G. Duvall, and J.D. Meindl, "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration," *IEEE Journal of Solid-State Circuits*, vol. 37, 2002, pp. 183-190.

[5] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter variations and impact on circuits and microarchitecture," *Proceedings of the 40th annual Design Automation Conference*, Anaheim, CA, USA: ACM, 2003, pp. 338-342.

[6] W. Dai and H. Ji, "Timing analysis taking into account interconnect process variation," *6th IEEE International Workshop on Statistical Methodology*, 2001, pp. 51-53.

[7] Y. Cao, P. Gupta, A.B. Kahng, D. Sylvester, and J. Yang, "Design sensitivities to variability: extrapolations and assessments in nanometer VLSI," *15th Annual IEEE International ASIC/SOC Conference, 2002.*, 2002, pp. 411-415.

[8] J. Healey, "Current Technical Trends: Dual Damascene and Low-k Dielectrics," 2002, pp. 1-6.

[9] C. Ouyang, L. Milor, W. Maly, and G. Hill, "An analytical model of multilevel ILD thickness variation induced by the interaction of layout pattern and CMP process," *Ieee International Symposium On Semiconductor Manufacturing Conference Proceedings*, 1999, pp. 221-224.

[10] B. Stine, D. Ouma, R. Divecha, D. Boning, and J. Chung, "A Closed-Form Analytical Model for ILD Thickness Variation," *in CMP Processes", Proc. CMP-MIC*, 1997, pp. 266-273.

[11] S.P. Mohanty Ranganathan, N., Kougianos, E., Patra, P., *Low-Power High-Level Synthesis for Nanoscale CMOS Circuits*, Springer, 2008.

[12] B. Halak Shedable, S., Ramakrishnan, H., Yakovlev, A., Russell, G., "Variability analysis of a high performance strained silicon jamb latch sycnhronizer," *Proceedings of the 19th UK Asynchronous Forum*, 2007, pp. 55-58.

[13] D.C. Montgomery, *Design and Analysis of Experiments*, Wiley, 2005.

[14] B.P. Wong Mittal Anurag, Cao, Y., Starr, G., *Nano-CMOS circuit and physical design*, John Wiley & Sons, 2005.

[15] N.H.E. Weste Harris, D., *CMOS VLSI Design: A Circuit and Systems Perspective*, 2005.

[16] H. Johnson and M. Graham, *High Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, 1993.

Chapter 6

CONCLUDING REMARKS

6.1. Discussions

A major issue in the design of high performance processors is their subsequent power consumption, which is a function of the operating frequency. The cost of packaging a circuit which consumes more than 50W, exceeds the cost of fabricating the circuit. In addition many circuits contain long global interconnects; these necessitate in the use of high power line drivers if their delay is not to compromise the performance of the circuit. Unfortunately, the use of technology scaling to satisfy market demands for increased functionality per unit area aggravates the interconnect delay problem.

Dynamic power consumption of a circuit is proportional to the switching activity of the circuit, load capacitance, the square of the supply voltage and the clock frequency [1]. Techniques adopted to reduce power consumption are thus directed at decreasing one or more of these factors; however since the power consumption is proportional to the square of the supply voltage most techniques are centred on voltage reduction provided high circuit performance is not a major design objective. Unfortunately, using reduced power supply voltages can impair the performance of the line drivers for global interconnect unless low-swing signalling techniques are adopted.

Low power consumption can be achieved while maintaining a high-speed signalling by using a low voltage swing on the interconnections. With the interconnect capacitance, operating frequency and supply voltage remaining the same, lower on-chip power consumption can be achieved using specially designed driver and receiver circuits which are used to convert the full rail-to-rail swing to low voltage swing, and vice versa. These circuits are the essential components of the low-swing signalling scheme.

There are several low-swing signalling schemes that employ a differential signalling method such as those that implement the differential current mode technique [2,3] and driver pre-emphasis technique [4]. There are also several single-ended signalling schemes which offer improvements in terms of both the performance and power consumption. These signalling schemes have been qualitatively compared in Table 2.1, which highlights their

characteristics, advantages and disadvantages. This table is important for future use or reference when designing low-power and high-speed on-chip signalling scheme.

The main problems with the differential signalling method are the area penalty and the complexity of the schemes. Their active area increase is due to the doubling of the number of wires while the increase in their circuit complexity is caused by additional circuitry such as the internal voltage generator for static source driver [5] and voltage regulator for differential voltage mode signalling schemes [6]. The single-ended signalling schemes have the advantage over the differential schemes in terms of the number of wires used but most of the schemes are too dependent on reference voltages and *low-Vth* devices such as the static source driver and *NMOS* only push-pull driver schemes [5]. Both of these methods also require multiple power supplies at both the driver and the receiver ends. The main issue with the multiple power supplies technique is the layout placement and the timing analysis. With a single power supply, timing analysis is simpler as it can be performed for single performance point based on a characterized library. However for multiple power supplies, the timing analysis has to be performed separately for each *Vdd*, which makes it more complex. In addition, both low and high *Vdd* cells need to be separated because the transistors have different n-well voltages [7,8], which increases the complexity of the circuit.

Table 2.1 indicates that the MJ driver scheme (K), has the best attributes compared to the other signalling schemes. This is because the scheme provides low power and high speed signalling without the use of extra circuitry such as extra *Vdd* and reference voltages. In addition, the scheme has a good *SNR* as well as low leakage currents. The MJ driver employs a simple inverter at the receiver end, which also minimises the area overhead. The differential current mode signalling also has similar attributes to the MJ driver, however, suffers from area penalty due to the doubled number of wires. Furthermore, sense amplifiers are usually incorporated in the differential current mode signalling schemes, which increases the area penalty.

Next section will starts off with comparison analyses and discussion between the diode-connected driver schemes, namely, the nLVSD, mLVSD, MJ and DDC driver schemes. The design parameters that are to be compared are area overhead, delay, power consumption, leakage currents and noise immunity. This is followed by the summaries of the reliability analysis against the process variations and environmental disturbances (*SEU* and crosstalk), and concluded with required future works in this area.

6.1.1. The implementation of the proposed driver schemes for the on-chip signalling application

The MJ driver is classified as a diode-connected driver, other low-swing drivers that incorporate this configuration, such as UDLD and DDC were discussed in Chapter 3. The VM pre-emphasis driver scheme [9] introduced in Chapter 2 also incorporates a diode-connected configuration. This configuration is efficient in providing a high-speed signalling due to its high driving current capability, especially if placed at the output, as in the case of the MJ driver and the VM pre-emphasis driver. Subsequently, this configuration also provides lower voltage swing at the output, which directly leads to lower power consumption. However, the issue with this type of configuration is its noise immunity and adaptability to process variation [10], as well as the issue with leakage currents.

From the discussion in Chapter 3, the MJ driver is considered to be redundant in terms of area as only half the circuit is needed to be operational during each rising and falling transition. Consequently the objectives of any new design, whilst maintaining the low voltage swing capability of the MJ driver must not only eliminate its disadvantages but also reduce the power consumption and delay of the circuit. These objectives can be achieved through the nLVSD and mLVSD drivers which are based on the MJ driver but they differ in their simplicity, which results in a smaller footprint. The active area for the MJ driver is measured at 51.34μm^2 whilst both the nLVSD and mLVSD drivers are measured at 25.52μm^2 and 23.4μm^2 respectively. This shows that both the proposed drivers are approximately 50% smaller than the MJ driver. Both proposed drivers have smaller areas compared to the MJ driver even though they incorporate leakage control mechanism in their driver circuit. Leakage control transistors are implemented in the nLVSD driver circuit whilst the mLVSD driver incorporates a pair of pass transistors providing direct static paths between the input and output of the drivers when the input is stable or no transistor activity is detected. The mechanism aids in further reducing the leakage current of the low-swing signalling scheme.

In order to address the efficiency of the proposed driver schemes, their performances in terms of speed and power consumption were analysed and the common problematic issues, such as noise and leakage currents, encountered by other diode-connected driver schemes were addressed. Therefore, comparative analyses were carried out for the nLVSD, mLVSD, DDC

and MJ driver schemes with the Schmitt Trigger level converter is implemented as the receiver.

6.1.2. Comparative analysis of the low-swing signalling schemes

The performance of the low-swing signalling schemes were analysed and compared with respect to the main design parameters, namely delay, power consumption, energy-delay-product and signal to noise ratio. The first design parameter considered was the overall delay of the driver schemes. The analysis was performed by increasing the length of the interconnect, from 1 to 10mm, between driver and receiver and determining the value of signal delay. A plot of the delay against interconnect length is shown in Figure 6.1.

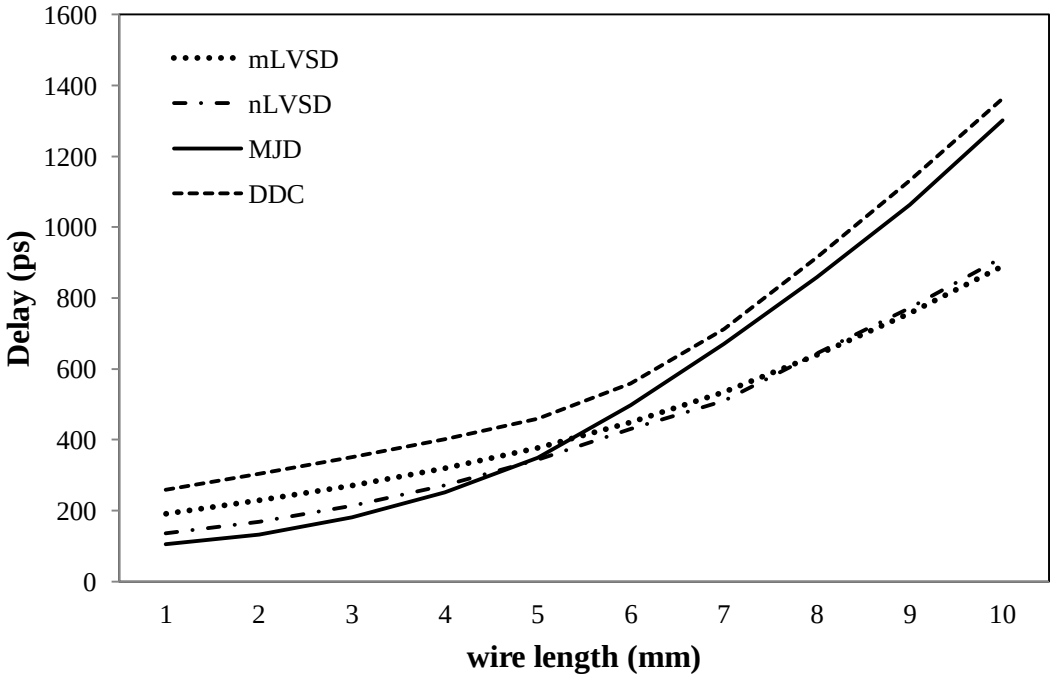


Figure 6.1: The comparison of delay between the low-swing signalling schemes for different range of interconnect length.

The initial rate of increase in delay of all driver schemes is quite similar with the MJ driver scheme showing a slight performance advantage up to 5mm interconnect length. This is followed by the nLVSD, mLVSD and DDC driver schemes. Thereafter the delay curve of the MJ driver scheme crosses over and starts to diverge from the proposed driver schemes and following the curve of the DDC driver scheme, showing a rapid increase in delay. For a 10mm length of interconnect the delay of the MJ and DDC driver schemes are 42% and 49% greater than the nLVSD scheme, whilst the mLVSD driver scheme is 46% and 53% faster than the MJ and DDC driver schemes, respectively. Thus for relatively short interconnect

length (<*6mm*) the MJ driver scheme has better delay characteristics but with only small percentage, thereafter the nLVSD and mLVSD driver schemes show distinct performance advantages as the interconnect length increases, with the mLVSD driver scheme having a slight performance advantage over the nLVSD driver scheme, approximately 3% reduction in delay. This is due to the pair of pass transistors incorporated in the mLVSD driver, which helps in speeding up the switching process.

Regarding the power consumption, Figure 6.2 shows that the nLVSD driver scheme is better than the mLVSD, MJ and DDC driver schemes over the full range of interconnect lengths considered. Thus, the nLVSD driver scheme has significant improvement in power consumption not only for global interconnects but also for shorter wire applications. This is due to its lowest voltage swing compared to other low-swing signalling schemes. This is followed by the mLVSD driver scheme with 34% increase in power consumption compared to the nLVSD driver scheme, and 7% improvement compared to the MJ and DDC driver schemes. At 10mm line length, the nLVSD driver scheme produces 43% improvement in power consumption compared to the MJ and DDC driver schemes.

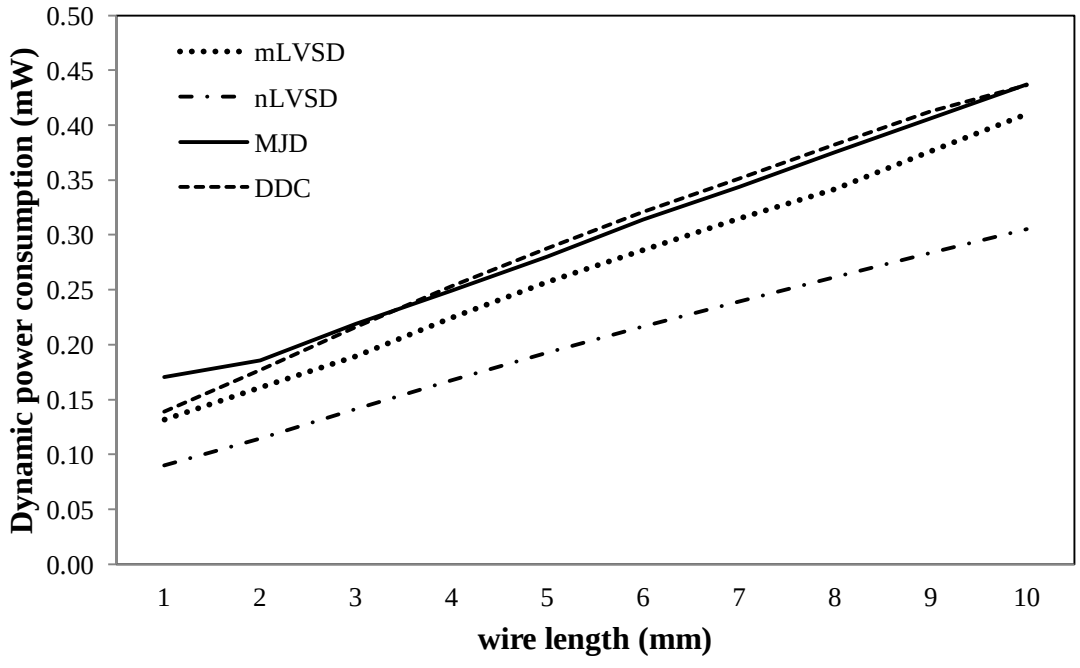


Figure 6.2: The comparison of dynamic power consumption between the low-swing signalling schemes for different range of interconnect length.

In order to analyse both the speed and power consumption for all low-swing signalling schemes at the same time, design metrics such as energy-delay-product (*EDP*) and power-

delay-product (*PDP*) can be used. *EDP* is preferable since it is independent of the operating frequency, which simplifies the optimization process and can be applied at any signal rate. Figure 6.3 indicates that the MJ driver scheme has a similar *EDP* characteristic to the nLVSD driver scheme at an interconnect length of 2mm; thereafter, it increases with the *EDP* curve of the mLVSD driver scheme until it crossover at 5mm and starts to increase rapidly, following the *EDP* curve of the DDC driver scheme, with a slight 10% decrease in *EDP*.

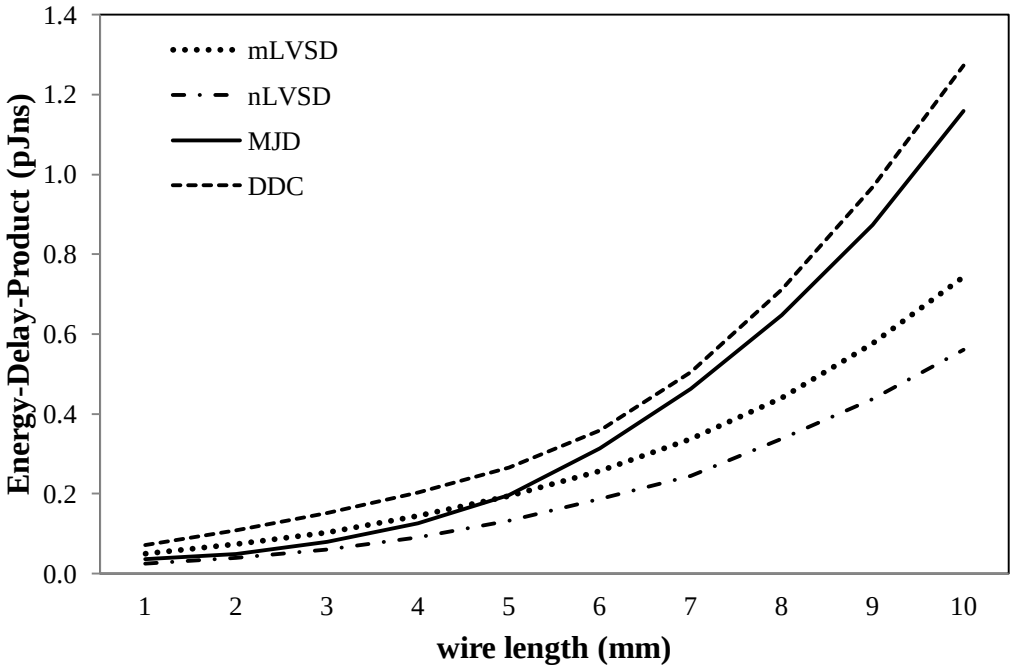


Figure 6.3: The comparison of energy-delay-product between the low-swing signalling schemes for different range of interconnect length.

The nLVSD driver scheme has the best *EDP* characteristic with 33% reduction compared to the mLVSD driver scheme throughout the length of the interconnect. Even though, the mLVSD driver scheme has a higher *EDP* than the nLVSD driver scheme it has a 56% and 71% improvement compared to the MJ and DDC driver schemes, respectively. Conclusively, the proposed driver schemes have the best *EDP* characteristics compared to the MJ and DDC driver schemes. Subsequently, overall, the nLVSD and mLVSD driver schemes produce significant improvements in both power consumption and delay compared to the DDC and MJ driver schemes, again demonstrating its suitability for their use with both long and short interconnects lengths.

Another design metric that need to be analysed for low-swing signalling schemes is the leakage currents. In nanometer scaled *CMOS* circuits, beside the dynamic power dissipation, energy dissipation can result from various forms of leakage currents such as gate-oxide tunnelling, sub-threshold leakage and junction tunnelling leakages. For submicron technologies, the dominant leakage mechanism is the sub-threshold leakage current, which needs to be addressed as the low-swing signalling schemes used in this work are implemented using 90nm technology where leakage currents are increasingly becoming more significant. Consequently, circuit temperature is linearly dependent on the power consumption, as it increases when power consumption is high. Since the leakage current increases with the increase in temperature, thus the comparative analysis involving leakage currents is carried out to the effects of temperature. Thus for this analysis, the leakage currents of the low-swing signalling schemes; namely, the nLVSD, mLVSD, DDC and MJ driver schemes are measured for a range of temperatures from 12°C to 55°C, as shown in Figure 6.4. Note that the result for the DDC driver scheme is not displayed in Figure 6.4, as the leakage currents of the DDC driver scheme has more than four times the increase in the leakage current of all the low-swing signalling schemes shown in Figure 6.4, thus it is discarded in this analysis.

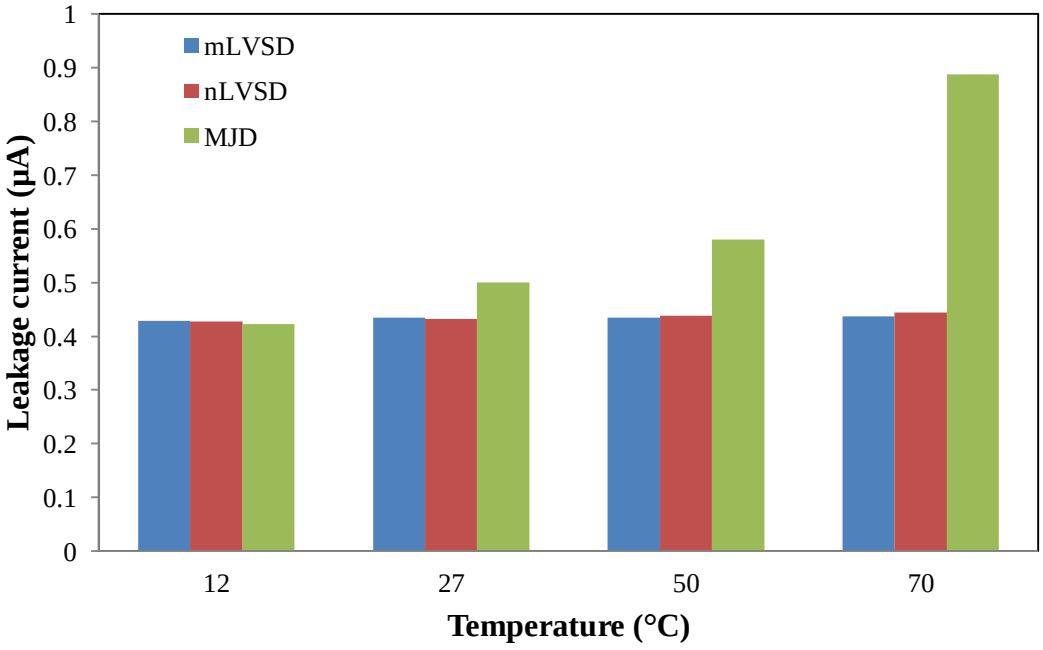


Figure 6.4: Comparison of leakage currents of the mLVSD scheme with the nLVSD and MJ schemes at different temperature range.

The results from Figure 6.4 show that the proposed driver schemes have almost constant leakage currents throughout the temperature range whilst the MJ driver scheme has twice the increase in leakage currents when the temperature increases from 12°C to 70°C. Conclusively, with the use of the leakage control mechanism in the driver, the leakage currents for the proposed driver schemes are considerably reduced and little affected by the changes in temperature.

Even though the proposed driver schemes have been shown to have the best attributes in terms of delay, both dynamic and leakage power consumption, as well as reduced area cost, one important aspect that needs to be addressed is the reliability of the driver schemes. Therefore, the reliability of driver schemes are analysed with respect to their signal to noise ratio using the approach outlined in [5]. The noise margin is affected by changes in the *Vtho* of the devices and their mismatch and the device sizing between driver and receiver in response to process variations. The variability in *Vtho* can adversely affect the noise margin. Mismatch between driver and receiver should be avoided in order to avoid this noise margin penalty. Therefore a reliability analysis has been performed for low-swing signalling schemes, namely, the mLVSD, nLVSD, MJ and DDC driver schemes at an interconnect length of 10mm, in order to highlight this issue, which has been summarised in Table 6.1.

Table 6.1: Noise analysis of low-swing signalling schemes at *Vdd* = 1.0V.

Driver Schemes	*Vs* (V)	$K_N V_S$	R_X_0 (V)	R_X_S (V)	*PS* (V)	*Attn*	T_X_0 (V)	V_N (V)	*SNR*
MJ	0.4913	0.016	0.05	0.03	0.05	0.5	0.05	0.166	1.48
DDC	0.5259	0.018	0.06	0.04	0.05	1.0	0.06	0.225	1.17
nLVSD	0.3444	0.008	0.04	0.02	0.05	0.5	0.03	0.124	1.39
mLVSD	0.4695	0.014	0.04	0.02	0.05	0.5	0.04	0.139	1.69

The K_{PS} (*signal-induced power supply noise*) is estimated to be 5% of the signal swing for single-ended signalling [11]. The crosstalk coupling coefficient, K_C is a ratio between coupling capacitance and interconnect load capacitance as shown in Equ.3.9, where C_C is the coupling capacitance, C_W is the interconnect capacitance and C_L is the fan-out capacitance.

For this work, C_C is calculated at 66.63fF/mm, *Cw* is at 174.47fF/mm whilst C_L is at 250fF/mm using equations 2.3 to 2.5, which gives the value of *Kc* as 0.14.

The crosstalk attenuation, $Attn_c$ is estimated to be 0.05 for a static driver circuit. The voltage swing for all four driver schemes is measured at the interconnect of 10mm. The power supply attenuation coefficient, *Attn* is measured by the changes in receiver switching threshold voltage due to the change of the supply voltage, as shown in Figure 3.2(a). Receiver input offset, R_X_0 and receiver sensitivity, R_X_S can be measured as shown in Figure 3.2(b) where the worst difference of the threshold voltage is measured at every simulated process corners. The noise voltage, V_N can be calculated using Equations 3.8 to 3.10 in Chapter 3.

Table 6.1 indicates that all diode-connected driver schemes tested here have good *SNR* since their *SNR* values exceed 1. Even though all the *SNR* values are above 1, the mLVSD scheme has better performance compared to other driver schemes and including the nLVSD driver scheme, in terms of reliability. The *SNR* of the mLVSD driver scheme is 22% and 14% higher compared to the nLVSD and MJ driver schemes, respectively. Even though the nLVSD driver scheme has the best *EDP* characteristic compared to other low-swing signalling schemes it has smaller *SNR* compared to the mLVSD and MJ driver schemes but with a 19% higher *SNR* than the DDC driver scheme. This is probably due to the lower voltage swing that the nLVSD driver scheme has, which can significantly affect the noise margin.

Based on this comparative analysis, it can be concluded that even though the nLVSD driver scheme has the best attributes in terms of delay, power and leakage consumption, its poor reliability against noise can compromise the signal integrity of its signalling scheme. However, it can be added that both the proposed driver schemes; namely, the nLVSD and mLVSD driver schemes have the best power and performance characteristics compared to the MJ and DDC driver schemes.

Further discussion on the performance of the low-swing signalling schemes with respect to the effect of process variation and environmental disturbances will be continued in the next section. The potential design parameters and methods to improve the reliability of the low-swing signalling schemes against the process variation as well as environmental disturbances are also summarised in the following section.

6.1.3. Impact of external disturbances and process variation on low-swing signalling schemes

As device dimensions are being reduced through the advances in semiconductor technology, the effects of process variations are an important issue which needs to be addressed as it is a salient factor in determining the reliability, performance and functionality of circuits. In addition to process variation, several studies have shown that temporary faults such as those resulting from *SEU* and crosstalk may have been responsible for 80% or more of the failures in digital systems [12,13]. The most important aspect that can be highlighted here is that issues regarding process variation and temporary faults are often not addressed in the reliability analysis, which is significantly important as they can affect the performance of the signalling schemes. Therefore, in this work, in order to assess the reliability of the low-swing signalling schemes, these issues were addressed and discussed in Chapters 4 and 5.

A comparative analysis for all four low-swing signalling schemes, namely, the nLVSD, mLVSD, DDC and MJ driver schemes were carried out in Chapter 4, in order to investigate their reliability against *SEU*s and crosstalk effects. The overall results indicate the proposed low-swing signalling schemes (nLVSD and mLVSD) have better performance and greater immunity to crosstalks and *SEU*s. Comparison analysis on the crosstalk effect were analysed for the low-swing signalling schemes, namely, the nLVSD, mLVSD, MJ and DDC driver schemes. The impact of crosstalk on the reliability of the driver schemes are analysed in the form of K_N (*coupling noise sources*). The results indicate that both proposed driver schemes have smaller K_N, which means more robust to crosstalk effect compared to the MJ and DDC driver schemes. The nLVSD driver scheme has approximately 30% and 39% less K_N compared to the MJ and DDC driver schemes respectively whilst the mLVSD scheme is 4% and 9% more robust in terms of crosstalk than the MJ and DDC driver scheme respectively. Additionally, the nLVSD driver scheme has shown to be 26% more robust than the mLVSD driver scheme. The DDC driver scheme suffers the most from the crosstalk effect as it has 5% more K_N than the MJ driver scheme.

In another aspect of robustness against temporary faults, the impact of *SEU* on the low-swing signalling scheme were also analysed which shows that both proposed driver schemes have better *SEU* tolerance compared to the MJ and DDC driver schemes. *SEU* tolerance was measured in the forms of critical charge; larger the critical charge, the stronger the *SEU* tolerance of a driver scheme is. The mLVSD driver scheme has the highest critical charge

with 5%, 33% and 47% more compared to the nLVSD, MJ and DDC driver schemes. Even though, the nLVSD driver scheme is less tolerance towards *SEU* compared to the mLVSD driver scheme, it is 26% and 40% more robust towards *SEU* effect than the MJ and DDC driver schemes. The DDC driver scheme is the most affected by *SEU* with 11% less critical charge than the MJ driver scheme.

Further analysis was carried out to determine the design strategies that can reduce the impact of *SEU* on the low-swing signalling schemes. The results indicate that the impact of a *SEU* can be reduced significantly by having high bias currents in the circuit design. Although by introducing a high bias current into the design which will increase the critical charge and hence improve the reliability towards *SEU*s, the power consumption is significantly increased. Another method in reducing the impact of *SEU* is by increasing *Vdd* or the operating frequency but the improvement is less significant than employing high bias current. Therefore, a good trade-off between the two design strategies need to be found in order to meet reliability target with minimal power overhead.

Additionally, several design methods to mitigate the problems with crosstalk, namely, wire spacing, buffer insertion and shielding, were also discussed. The results show that all three methods are efficient in reducing the crosstalk delay and noise. However, the comparative analysis between these methods indicates that shielding has the best performance overall but at a cost of power and area. Therefore, in order to meet the reliability requirement as well as obtaining minimum power and area cost, wire spacing is found to be the best design solution in this case.

In addition to the reliability analysis against temporary faults carried out in Chapter 4, the reliability analysis against the effect of process variations were also addressed in Chapter 5. Results from the variability analysis carried out in Chapter 5 have shown that with percentages variation in process parameters as stated in Table 5.4, the lowest delay for the 10mm line occurs with the mLVSD scheme which also has the lowest standard deviation. Meanwhile, the nLVSD scheme is 3.6% slower than the mLVSD scheme and has a standard deviation which is almost 5% greater than the mLVSD scheme. However, the nLVSD scheme has 44% improvement in terms of power consumption and also deviates about 23% less than the mLVSD scheme. This indicates that the mLVSD scheme excels overall in terms of delay but the nLVSD scheme is better overall in terms of power consumption due to its lower voltage swing. However, both proposed schemes have shown to be more robust than

the DDC and MJ driver schemes when exposed to process variations. The results showed that the MJ driver scheme deviates approximately 18% and 35% more in delay and power consumption respectively compared to the proposed schemes. The DDC driver scheme suffered the most from the effect of process variation as it showed that the scheme has approximately 20% and 57% more variations in delay and power consumption compared to the nLVSD and mLVSD driver schemes. From these results, it indicates that the proposed driver schemes are more robust against process variation but the mLVSD driver scheme is found to have the best performance overall when noise factors due to process variations such as the receiver sensitivity and receiver offset are accounted for to determine the most robust low-swing signalling scheme.

To gain a better understanding of which process parameters had the greatest impact on performance of the low-swing signalling scheme, the mLVSD driver scheme was further analyzed as this had a better performance profile among all low-swing signalling schemes tested in this work. In terms of device variations, the most significant parameters are *tox* and *Vtho,* and *Vdd* representing the environmental variation. The trends in power consumption with *tox*, *Vtho* and *Vdd* are completely opposite to the trend in delay. This means that the variations in *tox* and *Vtho* have positive correlations with the delay but negatively correlate with the power consumption. The same scenario also applies for *Vdd* as its variation causes an increase in variability of power consumption but a decrease in delay variation. The positive correlation between *Vdd* and power consumption is due to its quadratic relationship. The negative correlation of *Vdd* with regards to delay is due to the driving current, which decreases when *Vdd* decreases, which results in a slower circuit. The *Vtho* and *tox* have opposite effect on delay as the driving current increases with the reduction of both these parameters, resulting in faster circuit.

Similar trends can also be seen for interconnect variations. Firstly, the most significant parameters regarding interconnect are *s, w* and *t*. As *w* and *t* increase, R_W decreases while C_W increases, which overall causes the delay to decrease. The results also show that the delay variation increases when the spacing becomes wider but the delay itself is decreasing. However, the increase in interconnect spacing has an opposite effect on power consumption, as the variation in power consumption increases with *w* and *t*, but decrease with interconnect spacing.

Further analysis was carried out to investigate the impact of variability on crosstalk effects of the low-swing signalling schemes. Both linear and non-linear models are generated for crosstalk delay and glitch. The results indicate that the delay and glitch sensitivities have a high data dependency towards *Vdd* and wire parameter variations. This dependency can be reduced through buffer insertion and wire spacing with the latter method being the most effective difference in delay whilst wire spacing is found to be the most effective method in reducing variability in crosstalk noise. Results from the second order model indicate that most of the non-linear effects can be ignored as they are insignificant to provide an impact on the model accuracy. However, a few coefficients such as the quadratic effects of *Vth*, *w* and *h* and the interaction between *Vdd* and ρ should be considered as they can be regarded as significant to the crosstalk delay sensitivity compared to the linear coefficients.

6.1.4. Summary

The driver schemes proposed in this work have been shown to be more robust and reliable compared to existing low-swing signalling schemes reviewed in this work, in terms of low power, better signal integrity and robustness against process variations and temporary faults, the mLVSD driver scheme having the best overall attributes. The most effective design parameters or methods that can be implemented in the design of low-swing signalling schemes, in order to improve their robustness against the temporary faults have been identified, which is important for future use in designing low-power and high-speed on-chip signalling schemes to be used in sensitive environments. The most influential process parameters in device and interconnect variations have also been identified permitting fabrication process choices to be made depending on whether the main design criteria is performance or power consumption. This can also be applied to the variability analysis on the crosstalk effects as the most significant variables as well as their interactions and quadratic coefficients have been identified which aids in distinguishing the right process choice on whether the response of interest is crosstalk delay or glitch.

6.2. Conclusions

Due to the aggressive scaling in the integrated circuit design, the global interconnect delay has adversely been affected, which subsequently reduces the system performance. This problem can be mitigated by employing line drivers but with the cost of incurring high power consumption. Consequently, there is a need for a high speed on-chip signalling scheme. Low-swing signalling techniques can provide high speed signalling with low power consumption and hence can be used to driver global on-chip interconnect. Most of the proposed low-swing signalling schemes are immune to noise as they have good *SNR*. However, they tend to have large penalty in area and complexity as they require additional circuitry such as voltage generators and *low-Vth* devices. Most of the schemes also incorporate multiple *Vdd* and reference voltages which increase the overall circuit complexity.

As shown in Table 2.1, the MJ driver scheme, a diode-connected driver circuit, has the best attributes over other low-swing signalling techniques in terms of low power, low delay, good *SNR* and low area overhead. The MJ driver is a low-swing driver which incorporates a diode-connected configuration at the output, providing a high speed signalling due to its high driving capability. However, this configuration also has its limitations; it has issues with its adaptability to process variations, as well as issues with leakage currents. The proposed driver schemes (nLVSD and mLVSD) can overcome these limitations as well as improving performance and achieving lower power consumption. By incorporating diode-connected configuration at the output and leakage control mechanism in the driver circuit, there are vast improvements to be made in power consumption and delay, as well as in leakage current and *SNR*.

Both of the proposed driver schemes have less delay and low power consumption compared to other diode-connected driver schemes. The results indicate that the nLVSD and mLVSD driver schemes are approximately 46% and 50% respectively, faster than other diode-connected driver schemes. In terms of power consumption, the nLVSD and mLVSD driver schemes produce 43% and 7% improvement, respectively, compared to other diode-connected driver schemes. In addition to these results, both proposed driver schemes have low leakage currents compared to both the MJ and DDC drivers having two and four times increase in leakage currents compared to the proposed driver circuits.

The proposed driver schemes have shown to have the best attributes in terms of delay, power consumption, and leakage currents as well as reduced area cost. With regard to the noise immunity, the mLVSD driver scheme is the most robust as its *SNR* is 22%, 44% and 14% higher compared to the nLVSD, DDC and MJ driver schemes, respectively. On the other hand, the nLVSD driver scheme has 6% lower *SNR* compared to the MJ driver scheme, even though it is 19% more robust than the DDC driver scheme. However, since its *SNR* is still above 1, its improved performance and reduced power consumption, as well other advantages it has over other diode-connected driver schemes can compensate for this limitation.

Regarding the robustness to external disturbances, both proposed driver schemes are more robust to crosstalk effects as the nLVSD and mLVSD driver schemes are approximately 35% and 7% more robust than other diode-connected drivers. Furthermore, the mLVSD driver is 5%, 33% and 47% more tolerant to *SEU*s compared to the nLVSD, MJ and DDC drivers respectively, whilst the MJ and DDC drivers are 26% and 40% less tolerant to *SEU*s compared to the nLVSD circuit. This also indicates that the mLVSD is more *SEU* tolerant compared to the nLVSD driver scheme but less robust against crosstalk.

In terms of process variations, both proposed driver schemes are more robust than the MJ and DDC circuits. The MJ driver scheme deviates by approximately 18% and 35% more in delay and power consumption whilst the DDC driver scheme deviates by approximately 20% and 57% more in delay and power consumption in comparison to the proposed schemes. The nLVSD driver scheme has a standard deviation of delay which is almost 5% greater than the mLVSD driver but in terms of power consumption, the nLVSD scheme deviates by about 23% less than the mLVSD scheme.

The above results indicate that the proposed driver schemes have the best attributes compared to other diode-connected drivers showing significant improvements in delay, power consumptions, leakage currents and area overhead as well as robustness against process variations and environmental disturbances. However, in comparing the nLVSD and the mLVSD schemes, each scheme has an advantage over the other, which shows in a way they can compensate for each other based on the required performance goals.

From the above, it is considered that this work has contributed to the state of the art in the design of low-swing signalling circuits. However, as outlined below, further work is required in this area.

6.3. Future Works

There are several ideas or applications in which the low-swing signalling schemes proposed in this work can be used. There are a few suggestions such as increasing bandwidth or incorporating Silicon-on-Insulator technique into the design to further improve the performance and reduce power consumption of the proposed schemes. Subsequently, the proposed driver circuits can be implemented in applications such as multi-level signalling or adaptive signalling schemes to observe their abilities to provide improvements in delay and power consumption as well as reduced leakage currents and increased robustness against external disturbances and process variations, in the existing applications.

6.3.1. Increase bandwidth or operating frequency

The diffusive and dispersive effects of signals travelling over *RC* dominated on-chip interconnects limits both the transmission data rates and propagation latency in long global interconnects within microprocessor circuits [14]. A static driver with a low-impedance current sensing repeater is one of the techniques used to overcome this problem; it has a higher interconnect bandwidth compared to the full-swing voltage sensing schemes, but at the expense of increased power dissipation due to the current mode signalling. The proposed driver schemes in this work have been shown to have a significant improvement in power consumption at a maximum operating frequency of 1GHz. Larger operating frequencies are required to achieve high signal bandwidth.

However, as the operating frequency reaches beyond 1GHz, disruption in signal data can occur, which disrupts the efforts in increasing the signal bandwidth using the proposed drivers. As the demand for high data bandwidth becomes more important in the deep submicron regime, it is essential to modify the proposed driver circuits by incorporating additional mechanisms which enable them to transmit high data bandwidth with low power consumption on the global interconnect lines.

6.3.2. Multi-level signalling application

The multi-level signalling system [15] operates in current mode and consists of a transmitter, receiver and decoder where the transmitter encodes the two signal bits into four current levels and transmits them. The receiver compares the transmitted currents with the reference currents, which converts the four current levels into thermometer codes. The decoder then recovers the original signal. This approach is known to provide high bandwidth and comparable delay to the buffer insertion techniques, it also reduces the number of interconnect wires as with this technique, multiple bits can be transmitted on a single wire. However, this approach does have its limitations as it relies on matching and proper sizing of the driver and receiver transistors and is thus prone to the effects of process variations.

The proposed drivers can be incorporated into this system as they have been shown to be more robust against process variations and matching-related noise, and at the same time, the bandwidth of the proposed driver schemes can be improved with this system. Subsequently, the proposed drivers having a diode-connected configuration at the output can easily be transformed to encapsulate similar functions as current mirrors changing the driver from operating in voltage mode to current mode. Since the system requires constant difference between the current levels produced by the drivers for the system to function properly, the modified part of the proposed drivers can be tuned to achieve this. This can be carried out by changing the size of the diode-connected transistors at the output of the drivers, giving off different current levels for each driver. However, it is important to make the necessary changes in the proposed receiver circuit in order to avoid any mismatch between them.

6.3.3. Implementation of the designs using Silicon on Insulator (SoI) Technology

Silicon-on-Insulator (*SOI*) is a semiconductor fabrication technique which uses pure crystal silicon and silicon oxide for integrated circuits. This technology is useful in the area where there are increased effects of process variation and reduced immunity of *SEU*s. It has attracted attention to be the next force behind technology scaling due to its capability to provide more speed, less power consumption and enhanced scalability as demanded by future *CMOS* generations. Comparing the bulk *CMOS* and *SOI* technologies, *SOI* can work at a 20 to 35% higher speed than standard *CMOS*, as well as having 2 to 4 times less power consumption when running under the same operating conditions. Another advantage of this technology is the suppressed short channel effects, which means that the *SOI* device has a

steeper sub-threshold slope which in turn can be translated into higher driver current and lower source/drain leakage current.

Although driver schemes proposed in this work employ a bulk *CMOS* technology they have shown vast improvements in speed, power consumption, leakage current and robustness to process variations and *SEU*. It is expected that by implementing this in *SOI*, this will result in more speed, less power consumption and leakage current and greater robustness against process variations and *SEU* effects than the current implementation. Subsequently, as *SOI* technology can be used to achieve these advantages, the complexity or area overhead of the proposed driver circuits can be reduced as the circuitry or mechanisms that were incorporated into the circuit design to reduce leakage currents and provide faster signalling can be removed, as they will no longer be necessary.

6.3.4. Adaptive signalling schemes

Previously, the results have shown that a trade-off is required between power consumption and delay, as well as between performance or power consumption and noise immunity for the proposed driver schemes, especially in the case of the nLVSD driver. This is because with the proposed driver schemes, low power consumption can be achieved and high speed signalling can be maintained with the low voltage swing but at the cost of noise immunity, even though it can still be considered as reliable, as the *SNR* is still above 1. However, it is necessary to improve the noise immunity of the proposed drivers especially the nLVSD circuit whilst maintaining low power consumption and high speed signalling. This can be done by employing an adaptive mechanism which varies the voltage swing, as well as an error protection mechanism which adaptively selecting error coding methods such as parity, Hamming and Berger codes, based on the noise levels and detected energy consumption.

Typically, an adaptive signalling scheme is used to dynamically control the driver swing and the corresponding receiver threshold by applying dynamic voltage scaling to the interconnects in order to reduce the power consumption on the interconnect. Subsequently, the variable voltage swing can impact on the speed at which the driver is able to charge and discharge the load capacitance, thus the maximum reliable operating frequency is reduced with lower swings, thus also requiring an adaptive scheme for speed. However, if the proposed driver schemes are implemented, the adaptive scheme for speed can be discarded as

the proposed driver schemes have faster signalling even with lower voltage swings. Therefore, high operating frequency can still be achieved when using low voltage swing.

However, operating with lower voltage swings makes the communication more sensitive to several noise sources. In order to cancel this effect, an error detection encoding at the source and Automatic Repeat Request (*ARQ*) strategy can be implemented [16]. It is known that error detection schemes with retransmission are less costly in terms of energy consumption than error correction schemes. A controller is required which decides on the voltage swing to be used and also to explore the design space for safe operating points. Inputs such as bandwidth requirements and channel reliability are required for controller.

Another adaptive scheme that can be incorporated into the system is adaptive error protection scheme. Different coding methods have different capabilities to detect errors induced by different noise sources. While the coding scheme adopted can be designed for the worst case noise scenario, such an approach will be inefficient in terms of both energy and performance. Therefore it is necessary to design a system with self-embedded intelligence that can vary the coding technique based on the noise behaviour, and switch to the least powerful error detection scheme that can maintain the undetected error rates below specified levels, while energy consumption can be minimized while maintaining required protection levels.

It would be beneficial to consider the two adaptive schemes as complementary and devise schemes that combine voltage scaling and code adaptation. Such a combination is relevant given that a number of different coding schemes can be implemented simultaneously; the number of supply voltages or voltage swing range is typically limited in real systems.

References

[1] C. Piguet, "Low-Power Electronics Design," *Computer Engineering*, V. Oklobdzija, ed., Switzerland: CRC Press, 2005, pp. 159-161.

[2] A. Tajalli and Y. Leblebici, "A power-efficient LVDS driver circuit in 0.18um CMOS technology," *Research in Microelectonics and Electronics Conference, PRIME 2007*, 2007, pp. 145-148.

[3] L. Yang, C. Jue-Ping, H. Yue, and L. Yi, "A low swing differential signalling circuit for on-chip global interconnects," *9th International Conference on Solid-State and Integrated-Circuit Technology, ICSICT 2008*, 2008, pp. 1693-1696.

[4] L. Zhang, J. Wilson, R. Bashirullah, L. Luo, J. Xu, and P. Franzon, "Driver pre-emphasis techniques for on-chip global buses," *Proceedings of the 2005 International Symposium on Low Power Electronics and Design, ISLPED '05*, 2005, pp. 186-191.

[5] H. Zhang, V. George, and J.M. Rabaey, "Low-swing on-chip signaling techniques: effectiveness and robustness," *IEEE Trans. Very Large Scale Integrated System*, vol. 8, 2000, pp. 264-272.

[6] H. Song, S. Kim, and D.-K. Jeong, "A reduced-swing voltage-mode driver for low power multi-Gb/s transmitter," *Journal of Semiconductor Technology and Science*, vol. 9, 2009, pp. 104-109.

[7] F.S. Q. Zhu P. Chong, "A Placement Technique for Multiple Voltage Design," 2006.

[8] U. of C. Berkeley, "BSIM4.3.0 MOSFET Model User's Manual."

[9] L. Zhang, J.M. Wilson, R. Bashirullah, L. Luo, J. Xu, and P.D. Franzon, "Voltage-Mode Driver Preemphasis Technique For On-Chip Global Buses," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 15, 2007, pp. 231-236.

[10] M. Ferretti and P.A. Beerel, "Low swing signaling using a dynamic diode-connected driver," *Proceedings of the 27th European Solid-State Circuits Conference. ESSCIRC 2001*, 2001, pp. 369-372.

[11] W.J. Dally and J.W. Poulton, *Digital Systems Engineering*, Cambridge University Press, 1998.

[12] R.K. Iyer and D. Rosetti, "A statistical load dependency of CPU errors at SLAC," *Twenty-Fifth International Symposium on Fault-Tolerant Computing, " Highlights from Twenty-Five Years".*, 1995, p. 373.

[13] H. Ball and F. Hardy, "Effects and detection of intermitten failures in digital system," *Proc. AFIPS Conference*, 1969, pp. 329-335.

[14] H.B. Bakoglu, *Circuits, Interconnections and Packaging for VLSI*, Reading: Addison-Wesley, 1990.

[15] V. Venkatraman and W. Burleson, "Impact of Process Variations on Multi-Level Signaling for On-Chip Interconnects," *Proceedings of the 18th International Conference on VLSI Design held jointly with 4th International Conference on Embedded Systems Design*, Washington, DC, USA: IEEE Computer Society, 2005, pp. 362-367.

[16] F. Worm, P. Ienne, P. Thiran, and G.A.-de micheli de micheli G., "An adaptive low-power transmission scheme for on-chip networks," *15th International Symposium on System Synthesis, 2002.*, P. Ienne, ed., 2002, pp. 92-100.

APPENDIX I

A1.1 The diode-connected drivers and their transistors sizing

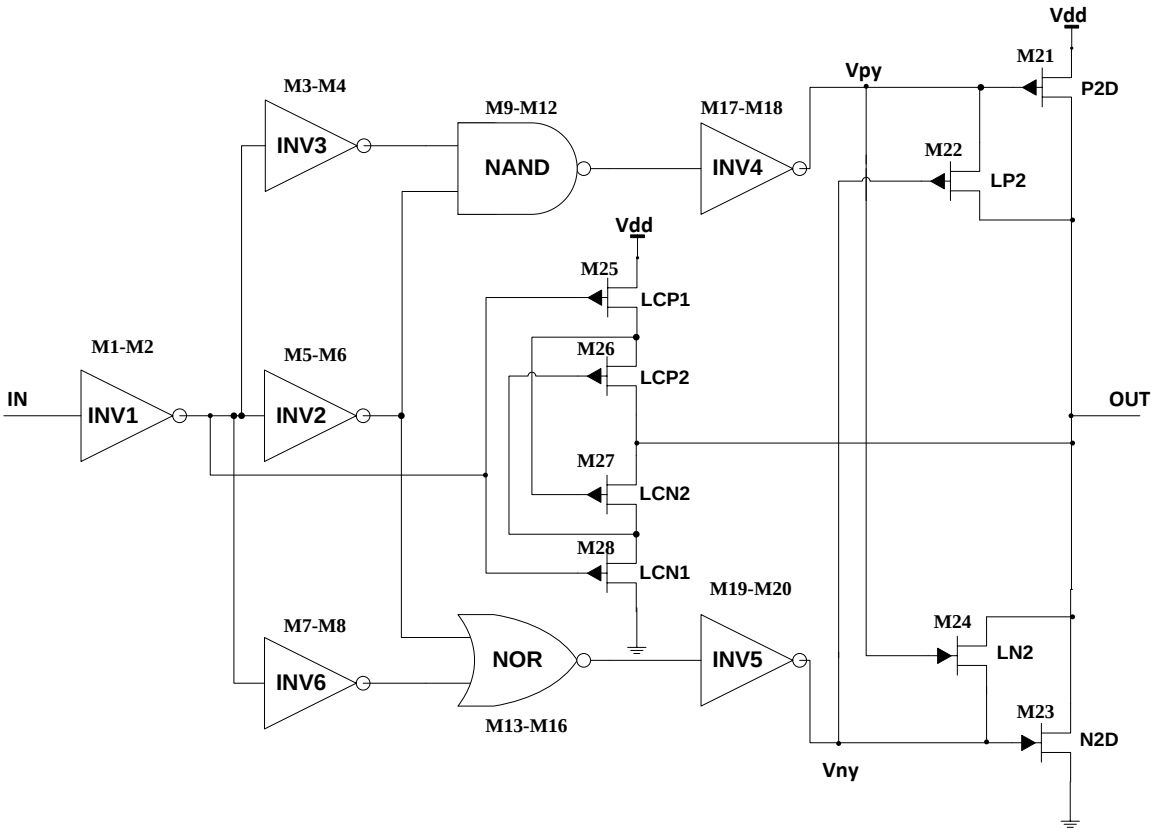


Figure A1.1: The nLVSD driver circuit.

Table A1.1: Channel widths for transistors in the nLVSD driver.

Transistor	Type	Width (µm)	Transistor	Type	Width (µm)
M1	P	12.5	M13/M14	P	3.46
M2	N	4.05	M15/M16	N	2.77
M3/M7	P	1.39	M17/M20	P/N	5.54
M4/M8	N	0.69	M18/M19	N/P	0.2
M5	P	2.77	M21/M23	P/N	20.25
M6	N	1.39	M22/M24	P/N	5.54
M9/M10	P	2.77	M25/M26	P	0.81
M11/M12	N	3.46	M27/M28	N	0.27

nLVSD driver netlist (UMC CMOS 90nm):

```
// Library name: variability_analysis
// Cell name: VA_invx5
// View name: schematic
subckt VA_invx5 ou1 ou2
   X5N (ou2 ou1 0 0) n_10_sp l=L w=195n sa=300n sb=300n nf=1 mis_flag=1 \
      sd=0 as=59.5f ad=59.5f ps=1u pd=1u m=1
   X5P (ou2 ou1 vdd! vdd!) p_10_sp l=L w=5.54u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=1.3296p ad=1.3296p ps=11.56u pd=11.56u m=1
ends VA_invx5
// End of subcircuit definition.

// Library name: variability_analysis
// Cell name: VA_invx6
// View name: schematic
subckt VA_invx6 od1 od2
   X6N (od2 od1 0 0) n_10_sp l=L w=5.54u sa=240n sb=240n nf=1 mis_flag=1 \
      sd=0 as=1.3296p ad=1.3296p ps=11.56u pd=11.56u m=1
   X6P (od2 od1 vdd! vdd!) p_10_sp l=L w=195n sa=300n sb=300n nf=1 \
      mis_flag=1 sd=0 as=59.5f ad=59.5f ps=1u pd=1u m=1
ends VA_invx6
// End of subcircuit definition.

// Library name: variability_analysis
// Cell name: VA_nor
// View name: schematic
subckt VA_nor in inn\-2 od1
   NRN1 (od1 inn\-2 0 0) n_10_sp l=L w=2.77u sa=300n sb=300n nf=1 \
      mis_flag=1 sd=0 as=831f ad=831f ps=6.14u pd=6.14u
m=1
   NRN2 (od1 in 0 0) n_10_sp l=L w=2.77u sa=300n sb=300n nf=1 mis_flag=1 \
      sd=0 as=831f ad=831f ps=6.14u pd=6.14u m=1
   NRP1 (net15 in vdd! vdd!) p_10_sp l=L w=3.46u sa=240n sb=240n nf=1
\
      mis_flag=1 sd=0 as=830.4f ad=830.4f ps=7.4u pd=7.4u
m=1
   NRP2 (od1 inn\-2 net15 vdd!) p_10_sp l=L w=3.46u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=830.4f ad=830.4f ps=7.4u pd=7.4u
m=1
ends VA_nor
// End of subcircuit definition.

// Library name: variability_analysis
// Cell name: VA_invx2
// View name: schematic
subckt VA_invx2 inn\-1 inn\-2
```

```
   X2N (inn\-2 inn\-1 0 0) n_10_sp l=L w=1.385u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=332.4f ad=332.4f ps=3.25u pd=3.25u m=1
   X2P (inn\-2 inn\-1 vdd! vdd!) p_10_sp l=L w=2.77u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=664.8f ad=664.8f ps=6.02u pd=6.02u m=1
ends VA_invx2
// End of subcircuit definition.

// Library name: variability_analysis
// Cell name: VA_invx3
// View name: schematic
subckt VA_invx3 in inn
   X3N (inn in 0 0) n_10_sp l=L w=690n sa=240n sb=240n nf=1 mis_flag=1
\
      sd=0 as=165.6f ad=165.6f ps=1.86u pd=1.86u m=1
   X3P (inn in vdd! vdd!) p_10_sp l=L w=1.385u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=332.4f ad=332.4f ps=3.25u pd=3.25u m=1
ends VA_invx3
// End of subcircuit definition.

// Library name: variability_analysis
// Cell name: VA_nand
// View name: schematic
subckt VA_nand inn inn\-1 ou1
   NDN1 (ou1 inn net4 0) n_10_sp l=L w=3.46u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=830.4f ad=830.4f ps=7.4u pd=7.4u
m=1
   NDN2 (net4 inn\-1 0 0) n_10_sp l=L w=3.46u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=830.4f ad=830.4f ps=7.4u pd=7.4u
m=1
   NDP1 (ou1 inn vdd! vdd!) p_10_sp l=L w=2.77u sa=300n sb=300n nf=1
\
      mis_flag=1 sd=0 as=831f ad=831f ps=6.14u pd=6.14u
m=1
   NDP2 (ou1 inn\-1 vdd! vdd!) p_10_sp l=L w=2.77u sa=300n sb=300n nf=1 \
      mis_flag=1 sd=0 as=831f ad=831f ps=6.14u pd=6.14u
m=1
ends VA_nand
// End of subcircuit definition.

// Library name: variability_analysis
// Cell name: VA_invx1
// View name: schematic
subckt VA_invx1 in inn\-1
   X1N (inn\-1 in 0 0) n_10_sp l=L w=4.05u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=972f ad=972f ps=8.58u pd=8.58u
m=1
   X1P (inn\-1 in vdd! vdd!) p_10_sp l=L w=12.5u sa=240n sb=240n nf=1 \
```

```
    mis_flag=1 sd=0 as=3p ad=3p ps=25.48u pd=25.48u m=1
ends VA_invx1
// End of subcircuit definition.

// Library name: variability_analysis
// Cell name: new_lvsd_driver
// View name: schematic
I115 (net0417 net0169) VA_invx5
I36 (net0318 net0238) VA_invx5
I68 (net0256 net0324) VA_invx5
I116 (net0417 net0175) VA_invx6
I35 (net0318 net0242) VA_invx6
I69 (net0247 net0279) VA_invx6
I79 (net0253 net0249 net0247) VA_nor
I80 (net0126 net0249) VA_invx2
I82 (net0126 net0251) VA_invx3
I81 (net0126 net0253) VA_invx3
I83 (net0251 net0249 net0256)
VA_nand
I113 (net0134 net0126) VA_invx1
V5 (net0134 0) vsource dc=v_amp type=pwl delay=0 edgetype=linear \
    val0=v_amp val1=0 period=2n rise=5.00f fall=5.00f freq=500M \
    ampl=500.0m sinephase=10n sinedc=0 wave=[ 0 1 500.0p 1 500.005p 0 \
    1.059995n 0 1.06n 1 1.5n 1 1.500005n 0 1.999995n 0 2.0n 1 2.56n 1
\
    2.560005n 0 3.059995n 0 3.06n 1 3.56n 1 3.560005n 0 3.999995n 0
\
    4.0n 1 4.5n 1 4.500005n 0 ]
PM42 (net0268 net0415 vdd! vdd!) p_10_sp l=L w=5.4u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=1.296p ad=1.296p ps=11.28u pd=11.28u m=1
PM41 (net0260 net0169 vdd! vdd!) p_10_sp l=L w=20.25u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=4.86p ad=4.86p ps=40.98u pd=40.98u m=1
PM36 (net0260 net0175 net0169 net0169) p_10_sp l=L w=5.54u sa=240n sb=240n
\
    nf=1 mis_flag=1 sd=0 as=1.3296p ad=1.3296p ps=11.56u pd=11.56u m=1
PM35 (net0417 net0268 vdd! vdd!) p_10_sp l=L w=5.4u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=1.296p ad=1.296p ps=11.28u pd=11.28u m=1
PM3 (net0318 net0305 vdd! vdd!) p_10_sp l=L w=5.4u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=1.296p ad=1.296p ps=11.28u pd=11.28u m=1
PM0 (net0313 net0242 net0238 net0238) p_10_sp l=L w=5.54u sa=240n sb=240n \
    nf=1 mis_flag=1 sd=0 as=1.3296p ad=1.3296p ps=11.56u pd=11.56u m=1
PM1 (net0313 net0238 vdd! vdd!) p_10_sp l=L w=20.25u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=4.86p ad=4.86p ps=40.98u pd=40.98u m=1
PM2 (net0305 net0362 vdd! vdd!) p_10_sp l=L w=5.4u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=1.296p ad=1.296p ps=11.28u pd=11.28u m=1
PM32 (net0249 net0279 net0280 net0249) p_10_sp l=L w=2.7u sa=240n sb=240n \
    nf=1 mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u m=1
```

```
PM31 (net0314 net0324 vdd! vdd!) p_10_sp l=L w=20.25u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=4.86p ad=4.86p ps=40.98u pd=40.98u m=1
PM30 (net0314 net0280 net0324 net0324) p_10_sp l=L w=5.54u sa=240n sb=240n
\
      nf=1 mis_flag=1 sd=0 as=1.3296p ad=1.3296p ps=11.56u pd=11.56u m=1
PM40 (net0181 net0177 vdd! vdd!) p_10_sp l=L w=2.7u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u
m=1
PM39 (out net0181 vdd! vdd!) p_10_sp l=L w=5.4u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=1.296p ad=1.296p ps=11.28u pd=11.28u m=1
PM38 (net0177 net0308 vdd! vdd!) p_10_sp l=L w=2.7u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u
m=1
PM37 (net0177 net0177 vdd! vdd!) p_10_sp l=L w=270n sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=64.8f ad=64.8f ps=1.02u pd=1.02u
m=1
NM40 (net0417 net0268 0 0) n_10_sp l=L w=2.7u sa=240n sb=240n nf=1
\
      mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u
m=1
NM39 (net0260 net0169 net0175 net0175) n_10_sp l=L w=5.54u sa=300n sb=300n
\
      nf=1 mis_flag=1 sd=0 as=1.662p ad=1.662p ps=11.68u pd=11.68u
m=1
NM34 (net0260 net0175 0 0) n_10_sp l=L w=20.25u sa=300n sb=300n nf=1 \
      mis_flag=1 sd=0 as=6.075p ad=6.075p ps=41.1u pd=41.1u m=1
NM33 (net0268 net0415 0 0) n_10_sp l=L w=2.7u sa=240n sb=240n nf=1
\
      mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u
m=1
NM2 (net0305 net0362 0 0) n_10_sp l=L w=2.7u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u
m=1
NM0 (net0313 net0242 0 0) n_10_sp l=L w=20.25u sa=300n sb=300n
nf=1 \
      mis_flag=1 sd=0 as=6.075p ad=6.075p ps=41.1u pd=41.1u m=1
NM1 (net0313 net0238 net0242 net0242) n_10_sp l=L w=5.54u sa=300n sb=300n \
      nf=1 mis_flag=1 sd=0 as=1.662p ad=1.662p ps=11.68u pd=11.68u
m=1
NM3 (net0318 net0305 0 0) n_10_sp l=L w=2.7u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u
m=1
NM30 (net0249 net0324 net0325 net0249) n_10_sp l=L w=2.7u sa=240n sb=240n \
      nf=1 mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u m=1
NM29 (net0314 net0325 net0279 net0279) n_10_sp l=L w=5.54u sa=300n sb=300n
\
      nf=1 mis_flag=1 sd=0 as=1.662p ad=1.662p ps=11.68u pd=11.68u
m=1
NM28 (net0314 net0279 0 0) n_10_sp l=L w=20.25u sa=300n sb=300n nf=1 \
```

```
    mis_flag=1 sd=0 as=6.075p ad=6.075p ps=41.1u pd=41.1u m=1
NM38 (out net0181 0 0) n_10_sp l=L w=2.7u sa=240n sb=240n nf=1 mis_flag=1 \
    sd=0 as=648f ad=648f ps=5.88u pd=5.88u m=1
NM37 (net0181 net0177 0 0) n_10_sp l=L w=1.35u sa=240n sb=240n
nf=1 \
    mis_flag=1 sd=0 as=324f ad=324f ps=3.18u pd=3.18u
m=1
NM36 (net0177 net0308 0 0) n_10_sp l=L w=1.35u sa=300n sb=300n
nf=1 \
    mis_flag=1 sd=0 as=405f ad=405f ps=3.3u pd=3.3u m=1
NM35 (net0177 net0177 0 0) n_10_sp l=L w=135n sa=300n sb=300n nf=1
\
    mis_flag=1 sd=0 as=53.5f ad=53.5f ps=1u pd=1u m=1
```

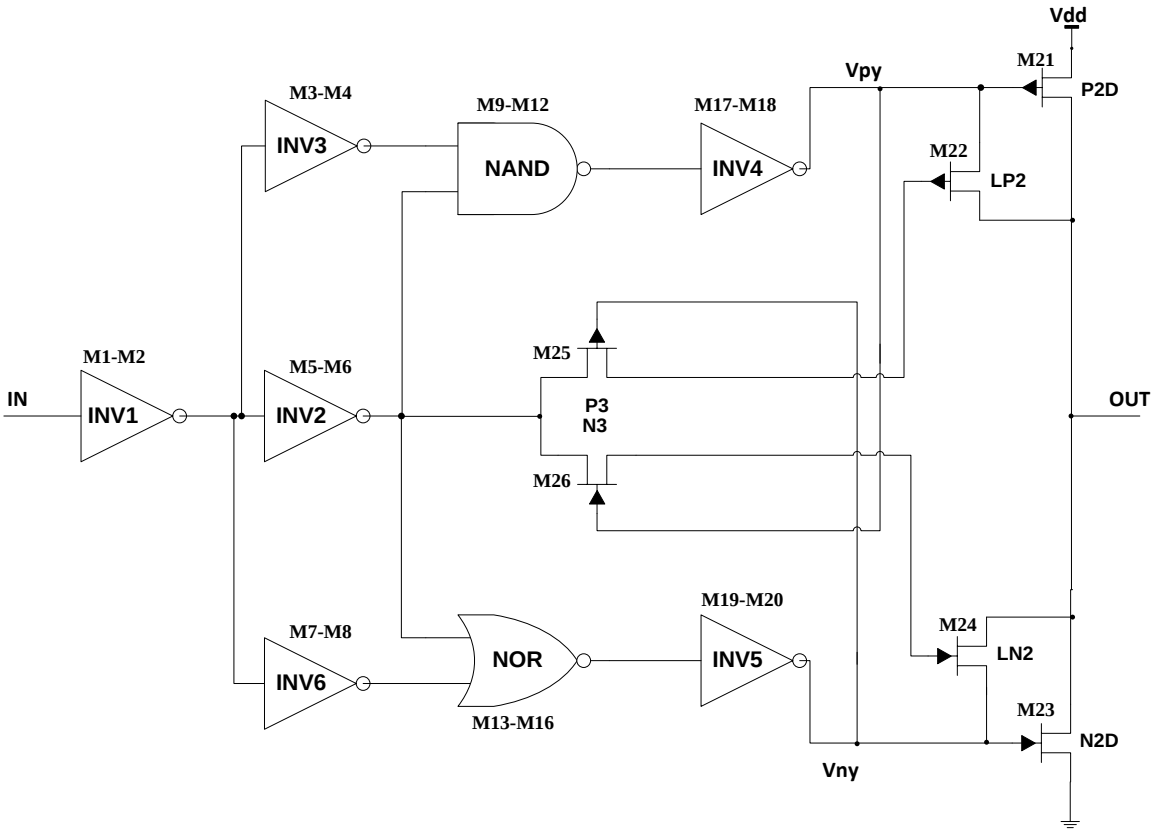


Figure A1.2: The mLVSD driver circuit.

Table A1.2: Channel widths for transistors in the mLVSD driver.

Transistor	Type	Width (µm)	Transistor	Type	Width (µm)
M1	P	12.5	M13/M14	P	3.46
M2	N	4.05	M15/M16	N	2.77
M3/M7	P	1.39	M17/M20	P/N	5.54
M4/M8	N	0.69	M18/M19	N/P	0.2
M5	P	2.77	M21/M23	P/N	20.25
M6	N	1.39	M22/M24	P/N	5.54
M9/M10	P	2.77	M25	P	2.7
M11/M12	N	3.46	M26	N	2.7

mLVSD driver netlist (UMC CMOS 90nm):

```
// Library name: variability_analysis
// Cell name: VA_invx1
// View name: schematic
subckt VA_invx1 in inn\-1
   X1N (inn\-1 in 0 0) n_10_sp l=L w=4.05u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=972f ad=972f ps=8.58u pd=8.58u m=1
   X1P (inn\-1 in vdd! vdd!) p_10_sp l=L w=12.5u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=3p ad=3p ps=25.48u pd=25.48u m=1
ends VA_invx1
// End of subcircuit
definition.

// Library name: variability_analysis
// Cell name: VA_nand
// View name: schematic
subckt VA_nand inn inn\-1 ou1
   NDN1 (ou1 inn net4 0) n_10_sp l=L w=3.46u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=830.4f ad=830.4f ps=7.4u pd=7.4u m=1
   NDN2 (net4 inn\-1 0 0) n_10_sp l=L w=3.46u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=830.4f ad=830.4f ps=7.4u pd=7.4u m=1
   NDP1 (ou1 inn vdd! vdd!) p_10_sp l=L w=2.77u sa=300n sb=300n nf=1 \
      mis_flag=1 sd=0 as=831f ad=831f ps=6.14u pd=6.14u m=1
   NDP2 (ou1 inn\-1 vdd! vdd!) p_10_sp l=L w=2.77u sa=300n sb=300n nf=1 \
      mis_flag=1 sd=0 as=831f ad=831f ps=6.14u pd=6.14u m=1
ends VA_nand
// End of subcircuit
definition.

// Library name: variability_analysis
// Cell name: VA_invx3
// View name: schematic
subckt VA_invx3 in inn
   X3N (inn in 0 0) n_10_sp l=L w=690n sa=240n sb=240n nf=1 mis_flag=1 \
      sd=0 as=165.6f ad=165.6f ps=1.86u pd=1.86u m=1
   X3P (inn in vdd! vdd!) p_10_sp l=L w=1.385u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=332.4f ad=332.4f ps=3.25u pd=3.25u m=1
ends VA_invx3
// End of subcircuit
definition.

// Library name: variability_analysis
// Cell name: VA_invx2
// View name: schematic
subckt VA_invx2 inn\-1 inn\-
2
```

```
   X2N (inn\-2 inn\-1 0 0) n_10_sp l=L w=1.385u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=332.4f ad=332.4f ps=3.25u pd=3.25u m=1
   X2P (inn\-2 inn\-1 vdd! vdd!) p_10_sp l=L w=2.77u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=664.8f ad=664.8f ps=6.02u pd=6.02u m=1
ends VA_invx2
// End of subcircuit
definition.

// Library name: variability_analysis
// Cell name: VA_nor
// View name: schematic
subckt VA_nor in inn\-2 od1
   NRN1 (od1 inn\-2 0 0) n_10_sp l=L w=2.77u sa=300n sb=300n nf=1 \
      mis_flag=1 sd=0 as=831f ad=831f ps=6.14u pd=6.14u m=1
   NRN2 (od1 in 0 0) n_10_sp l=L w=2.77u sa=300n sb=300n nf=1 mis_flag=1 \
      sd=0 as=831f ad=831f ps=6.14u pd=6.14u m=1
   NRP1 (net15 in vdd! vdd!) p_10_sp l=L w=3.46u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=830.4f ad=830.4f ps=7.4u pd=7.4u m=1
   NRP2 (od1 inn\-2 net15 vdd!) p_10_sp l=L w=3.46u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=830.4f ad=830.4f ps=7.4u pd=7.4u m=1
ends VA_nor
// End of subcircuit
definition.

// Library name: variability_analysis
// Cell name: VA_invx6
// View name: schematic
subckt VA_invx6 od1 od2
   X6N (od2 od1 0 0) n_10_sp l=L w=5.54u sa=240n sb=240n nf=1 mis_flag=1 \
      sd=0 as=1.3296p ad=1.3296p ps=11.56u pd=11.56u m=1
   X6P (od2 od1 vdd! vdd!) p_10_sp l=L w=195n sa=300n sb=300n nf=1 \
      mis_flag=1 sd=0 as=59.5f ad=59.5f ps=1u pd=1u m=1
ends VA_invx6
// End of subcircuit
definition.

// Library name: variability_analysis
// Cell name: VA_invx5
// View name: schematic
subckt VA_invx5 ou1 ou2
   X5N (ou2 ou1 0 0) n_10_sp l=L w=195n sa=300n sb=300n nf=1 mis_flag=1 \
      sd=0 as=59.5f ad=59.5f ps=1u pd=1u m=1
   X5P (ou2 ou1 vdd! vdd!) p_10_sp l=L w=5.54u sa=240n sb=240n nf=1 \
      mis_flag=1 sd=0 as=1.3296p ad=1.3296p ps=11.56u pd=11.56u m=1
ends VA_invx5
// End of subcircuit
definition.
```

```
// Library name: variability_analysis
// Cell name: mlvsd
// View name: schematic
C17 (out 0) capacitor c=CL
NM30 (net190 net60 net61 net190) n_10_sp l=L w=2.7u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u m=1
NM29 (net74 net61 net132 net132) n_10_sp l=L w=5.54u sa=300n sb=300n nf=1 \
    mis_flag=1 sd=0 as=1.662p ad=1.662p ps=11.68u pd=11.68u m=1
NM35 (net86 net86 0 0) n_10_sp l=L w=135n sa=300n sb=300n nf=1 mis_flag=1 \
    sd=0 as=53.5f ad=53.5f ps=1u pd=1u m=1
NM36 (net86 net36 0 0) n_10_sp l=L w=1.35u sa=300n sb=300n nf=1 mis_flag=1 \
    sd=0 as=405f ad=405f ps=3.3u pd=3.3u m=1
NM37 (net90 net86 0 0) n_10_sp l=L w=1.35u sa=240n sb=240n nf=1 mis_flag=1 \
    sd=0 as=324f ad=324f ps=3.18u pd=3.18u m=1
NM38 (out net90 0 0) n_10_sp l=L w=2.7u sa=240n sb=240n nf=1 mis_flag=1 \
    sd=0 as=648f ad=648f ps=5.88u pd=5.88u m=1
NM28 (net74 net132 0 0) n_10_sp l=L w=20.25u sa=300n sb=300n nf=1 \
    mis_flag=1 sd=0 as=6.075p ad=6.075p ps=41.1u pd=41.1u m=1
PM32 (net190 net132 net133 net190) p_10_sp l=L w=2.7u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u m=1
PM37 (net86 net86 vdd! vdd!) p_10_sp l=L w=270n sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=64.8f ad=64.8f ps=1.02u pd=1.02u m=1
PM38 (net86 net36 vdd! vdd!) p_10_sp l=L w=2.7u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u m=1
PM39 (out net90 vdd! vdd!) p_10_sp l=L w=5.4u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=1.296p ad=1.296p ps=11.28u pd=11.28u m=1
PM40 (net90 net86 vdd! vdd!) p_10_sp l=L w=2.7u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=648f ad=648f ps=5.88u pd=5.88u m=1
PM30 (net74 net133 net60 net60) p_10_sp l=L w=5.54u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=1.3296p ad=1.3296p ps=11.56u pd=11.56u m=1
PM31 (net74 net60 vdd! vdd!) p_10_sp l=L w=20.25u sa=240n sb=240n nf=1 \
    mis_flag=1 sd=0 as=4.86p ad=4.86p ps=40.98u pd=40.98u m=1
V5 (net170 0) vsource dc=v_amp type=pulse delay=0 edgetype=linear \
    val0=v_amp val1=0 period=1n rise=5.00f fall=5.00f freq=500M \
    ampl=500.0m sinephase=10n sinedc=0 wave=[ 0 1 500.0p 1 500.005p 0 \
    1.059995n 0 1.06n 1 1.5n 1 1.500005n 0 1.999995n 0 2.0n 1 2.56n 1 \
    2.560005n 0 3.059995n 0 3.06n 1 3.56n 1 3.560005n 0 3.999995n 0 \
    4.0n 1 4.5n 1 4.500005n
0 ]
```

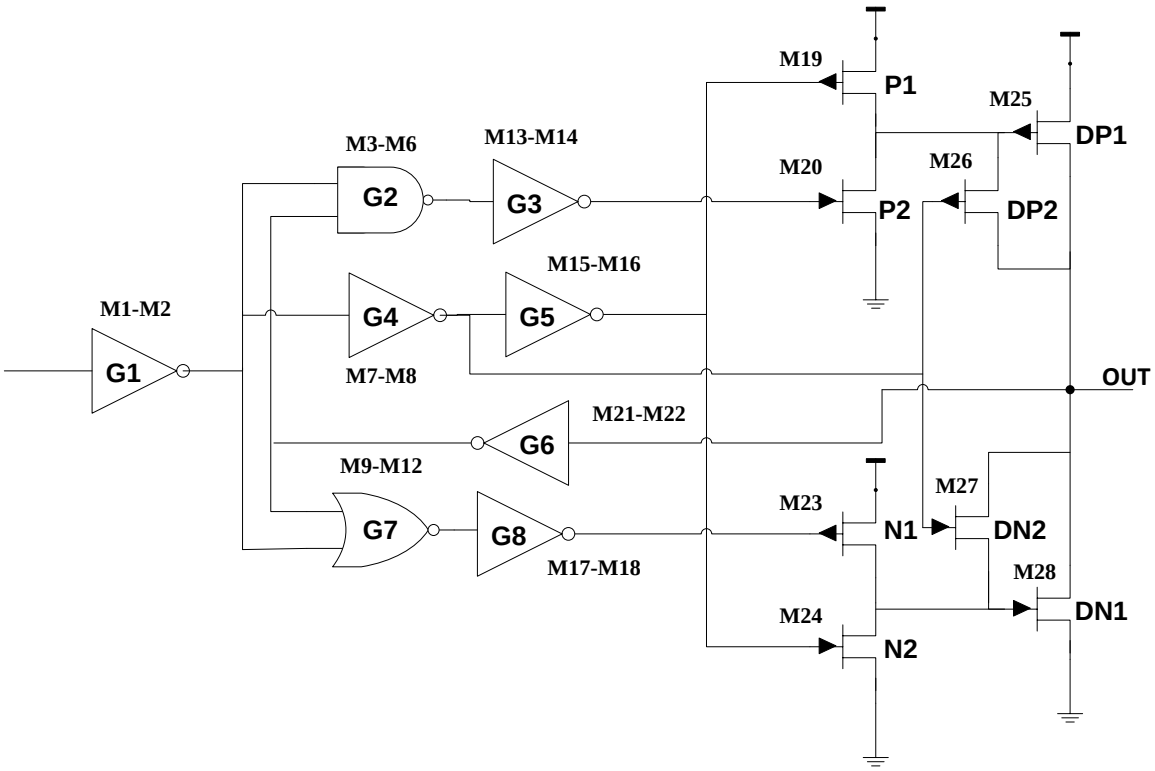


Figure A1.3: The MJ driver circuit.

Table A1.3: Channel widths for transistors in the MJ driver.

Transistor	Type	Width (µm)	Transistor	Type	Width (µm)
M1	P	12.5	M17	P	0.2
M2	N	4.05	M18	N	5.54
M3/M4	P	2.77	M19	P	3.46
M5/M6	N	3.46	M20	N	4.85
M7	P	2.77	M21	P	1.39
M8	N	1.39	M22	N	0.69
M9/M10	P	3.46	M23	P	2.77
M11/M12	N	2.77	M24	N	0.2
M13	P	5.54	M25	P	51.93
M14	N	0.2	M26	P	23.54
M15	P	1.39	M27	N	2.98
M16	N	0.69	M28	N	19.39

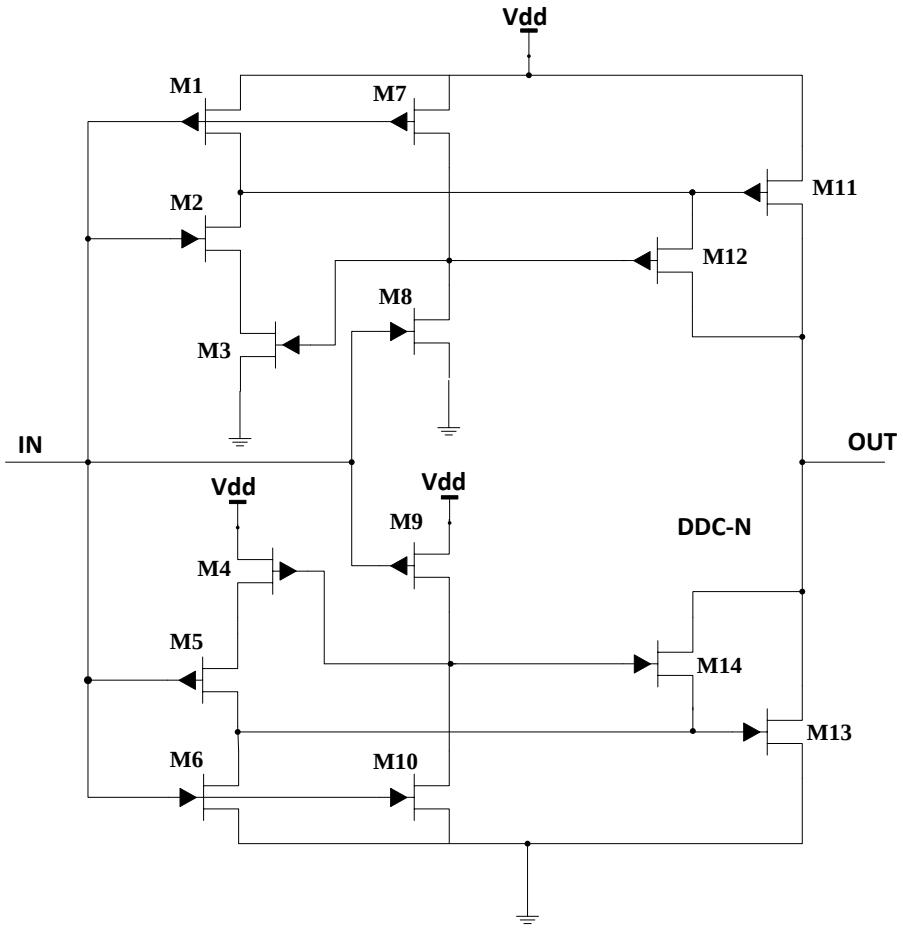


Figure A1.4: The DDC driver circuit.

Table A1.4: Channel widths for transistors in the DDC driver.

Transistor	Type	Width (µm)	Transistor	Type	Width (µm)
M1/M2	P/N	0.27	M7	P	27
M3	N	5.4	M8/M9	N/P	0.5
M4	P	2.7	M10	N	54
M5	P	0.27	M11/M13	P/N	20.25
M6	N	1.35	M12/M14	P/N	5.54

Table A1.5: Total area of the diode-connected drivers.

Drivers	Area
nLVSD	25.5
mLVSD	23.4
MJ	51.3
DDC	36.9

APPENDIX II

A2.1. R-squared

R-squared (R^2) is percentage of response variable variation that is explained by its relationship with 1 or more variables. In general, the higher the R^2, the better the model fits the data. R^2 is always between 0 and 100%. It is also known as the coefficient of determination or multiple determinations (*in multiple regressions*).

Plotting observed values by fitted values graphically illustrates R^2 values for regression models. Theoretically, if a model could explain 100% of the variance, the fitted values would always be equal to the observed values and therefore all the data points would fall on the fitted regression line.

A2.2. Experiment points for *CCD* technique for Statistical Analysis

The table shows the process parameters involved in this analysis where (-1,0,+1) represents (-3σ,0,+3σ). The statistical analysis was carried out using statistical tool called Minitab.

Experiment No.	Vdd	Temp	Vth	Leff	p	w	t	h
1	-1	1	-1	1	-1	-1	1	1
2	1	1	1	1	-1	1	-1	1
3	-1	-1	1	1	-1	1	-1	1
4	1	1	1	-1	1	1	1	-1
5	0	0	0	0	0	-1	0	0
6	-1	1	-1	-1	1	1	1	-1
7	-1	1	-1	-1	-1	-1	-1	1
8	-1	1	1	1	1	-1	1	1
9	1	-1	1	1	1	1	-1	1
10	-1	1	-1	-1	1	-1	1	1
11	1	-1	1	1	1	-1	-1	-1
12	1	0	0	0	0	0	0	0
13	-1	1	-1	-1	1	1	-1	1
14	-1	1	-1	1	1	1	-1	-1
15	-1	-1	1	1	-1	-1	-1	-1
16	-1	1	-1	-1	-1	1	-1	-1
17	1	1	1	-1	1	-1	1	1
18	1	1	1	-1	-1	1	-1	-1
19	1	-1	-1	1	1	-1	1	-1

20	0	0	1	0	0	0	0	0
21	-1	1	1	1	-1	-1	1	-1
22	1	1	-1	-1	1	1	-1	-1
23	1	1	1	-1	-1	-1	-1	1
24	-1	1	1	1	1	1	-1	1
25	1	-1	-1	-1	-1	-1	1	-1
26	0	0	0	0	0	0	0	0
27	0	0	0	0	0	0	0	0
28	1	1	-1	1	-1	-1	-1	1
29	1	-1	1	-1	1	-1	-1	1
30	-1	1	1	1	-1	1	1	1
31	-1	1	1	-1	1	-1	1	-1
32	-1	-1	1	-1	1	1	-1	1
33	-1	-1	-1	1	-1	-1	-1	1
34	-1	1	1	1	1	1	1	-1
35	1	1	-1	1	1	1	1	-1
36	1	1	-1	1	-1	1	1	1
37	-1	1	1	1	1	-1	-1	-1
38	-1	1	-1	1	-1	1	-1	1
39	1	-1	-1	-1	1	1	-1	1
40	1	1	-1	-1	-1	1	1	-1
41	1	1	1	1	-1	-1	1	1
42	0	0	0	0	0	0	0	-1
43	1	1	-1	1	1	-1	-1	-1
44	-1	1	1	-1	-1	1	-1	1
45	1	1	-1	1	-1	-1	1	-1
46	1	-1	-1	-1	1	1	1	-1
47	1	1	1	-1	1	-1	-1	-1
48	-1	-1	1	-1	1	1	1	-1
49	1	-1	1	-1	1	1	-1	-1
50	1	1	1	1	1	1	-1	-1
51	-1	-1	1	1	1	-1	1	-1
52	1	-1	-1	-1	1	-1	-1	-1
53	-1	1	-1	1	1	-1	-1	1
54	-1	-1	1	1	-1	1	1	-1
55	-1	-1	-1	-1	1	1	-1	-1
56	1	-1	1	1	-1	1	1	1
57	1	-1	-1	1	-1	-1	1	1
58	-1	-1	1	1	-1	-1	1	1
59	1	-1	-1	-1	-1	-1	-1	1
60	0	0	0	0	0	0	0	0
61	-1	-1	-1	-1	-1	1	-1	1
62	0	0	0	0	0	0	0	1
63	-1	1	1	1	-1	1	-1	-1
64	1	-1	1	-1	-1	-1	1	1
65	1	-1	1	-1	-1	1	-1	1

66	0	0	0	-1	0	0	0	0
67	1	-1	-1	1	1	-1	-1	1
68	-1	1	1	1	-1	-1	-1	1
69	-1	1	1	-1	-1	-1	-1	-1
70	1	1	1	-1	-1	1	1	1
71	-1	1	-1	1	-1	1	1	-1
72	1	-1	1	-1	1	-1	1	-1
73	-1	-1	1	1	1	1	1	1
74	-1	-1	1	-1	1	-1	-1	-1
75	1	1	1	1	-1	1	1	-1
76	-1	-1	-1	1	1	-1	-1	-1
77	-1	-1	-1	-1	-1	-1	-1	-1
78	0	0	0	0	-1	0	0	0
79	-1	-1	-1	-1	-1	1	1	-1
80	1	1	-1	-1	-1	-1	1	1
81	1	-1	1	1	-1	-1	-1	1
82	0	0	0	0	0	0	0	0
83	-1	-1	1	-1	-1	1	1	1
84	0	0	0	0	0	0	0	0
85	1	-1	1	1	1	1	1	-1
86	-1	1	-1	-1	-1	1	1	1
87	1	1	-1	1	1	1	-1	1
88	0	0	0	0	0	1	0	0
89	-1	-1	-1	1	-1	1	-1	-1
90	0	0	0	0	0	0	0	0
91	-1	-1	-1	-1	-1	-1	1	1
92	-1	1	1	-1	-1	1	1	-1
93	1	-1	-1	-1	-1	1	1	1
94	1	-1	1	1	1	-1	1	1
95	-1	1	1	-1	1	1	-1	-1
96	1	-1	-1	1	1	1	-1	-1
97	1	1	1	1	1	-1	-1	1
98	-1	-1	-1	1	-1	-1	1	-1
99	-1	-1	1	-1	1	-1	1	1
100	-1	1	-1	-1	-1	-1	1	-1
101	1	-1	1	1	-1	-1	1	-1
102	1	-1	1	-1	-1	-1	-1	-1
103	1	1	1	1	1	1	1	1
104	0	0	0	0	1	0	0	0
105	1	1	-1	1	-1	1	-1	-1
106	-1	1	1	-1	1	1	1	1
107	-1	-1	-1	1	-1	1	1	1
108	-1	1	-1	1	1	1	1	1
109	1	-1	1	1	-1	1	-1	-1
110	1	1	1	-1	1	1	-1	1
111	1	1	1	-1	-1	-1	1	-1
112	-1	1	-1	1	-1	-1	-1	-1
113	0	0	0	0	0	0	0	0
114	-1	-1	1	1	1	1	-1	-1
115	1	-1	-1	1	1	1	1	1
116	0	0	0	1	0	0	0	0
117	1	-1	-1	1	-1	1	1	-1

118	1	1	-1	-1	1	-1	-1	1
119	1	-1	1	-1	1	1	1	1
120	-1	1	-1	-1	1	-1	-1	-1
121	-1	1	1	-1	1	-1	-1	1
122	1	1	-1	-1	1	1	1	1
123	-1	-1	-1	-1	1	-1	1	-1
124	0	0	0	0	0	0	0	0
125	-1	-1	1	-1	-1	-1	-1	1
126	-1	-1	-1	-1	1	-1	-1	1
127	1	-1	-1	1	-1	-1	-1	-1
128	-1	-1	1	1	1	-1	-1	1
129	0	0	0	0	0	0	0	0
130	-1	1	1	-1	-1	-1	1	1
131	-1	-1	1	-1	-1	-1	1	-1
132	0	0	0	0	0	0	1	0
133	-1	0	0	0	0	0	0	0
134	1	1	1	1	-1	-1	-1	-1
135	0	0	0	0	0	0	0	0
136	-1	-1	-1	1	1	1	-1	1
137	1	-1	-1	1	-1	1	-1	1
138	1	1	-1	1	1	-1	1	1
139	1	-1	-1	-1	1	-1	1	1
140	1	1	-1	-1	-1	-1	-1	-1
141	0	-1	0	0	0	0	0	0
142	1	-1	-1	-1	-1	1	-1	-1
143	0	0	-1	0	0	0	0	0
144	-1	-1	-1	1	1	1	1	-1
145	-1	-1	-1	-1	1	1	1	1
146	1	-1	1	-1	-1	1	1	-1
147	0	1	0	0	0	0	0	0
148	-1	1	-1	1	1	-1	1	-1
149	-1	-1	1	-1	-1	1	-1	-1
150	1	1	1	1	1	-1	1	-1
151	0	0	0	0	0	0	-1	0
152	1	1	-1	-1	1	-1	1	-1
153	1	1	-1	-1	-1	1	-1	1
154	-1	-1	-1	1	1	-1	1	1