Reconfigurable Time Interval Measurement Circuit Incorporating a Programmable Gain Time Difference Amplifier

A Thesis Submitted for the Degree of Doctor of Philosophy in the Faculty of Engineering

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Abstract

As further advances are made in semiconductor manufacturing technology the performance of circuits is continuously increasing. Unfortunately, as the technology node descends deeper into the nanometre region, achieving the potential performance gain is becoming more of a challenge; due not only to the effects of process variation but also to the reduced timing margins between signals within the circuit creating timing problems. Production Standard Automatic Test Equipment (ATE) is incapable of performing internal timing measurements due, first to the lack of accessibility and second to the overall timing accuracy of the tester which is grossly inadequate. To address these issue 'on-chip' time measurement circuits have been developed in a similar way that built in self-test (BIST) evolved for 'on-chip' logic testing.

This thesis describes the design and analysis of three time amplifier circuits. The analysis undertaken considers the operational aspects related to gain and input dynamic range, together with the robustness of the circuits to the effects of process, voltage and temperature (PVT) variations. The design which had the best overall performance was subsequently compared to a benchmark design, which used the 'buffer delay offset' technique for time amplification, and showed a marked 6.5 times improvement on the dynamic range extending this from 40 ps to 300ps. The new design was also more robust to the effects of PVT variations.

The new time amplifier design was further developed to include an adjustable gain capability which could be varied in steps of approximately 7.5 from 4 to 117. The time amplifier was then connected to a 32-stage tapped delay line to create a reconfigurable time measurement circuit with an adjustable resolution range from 15 down to 0.5 ps and a dynamic range from 480 down to 16 ps depending upon the gain setting. The overall footprint of the measurement circuit, together with its calibration module occupies an area of 0.026 mm^2

The final circuit, overall, satisfied the main design criteria for 'on-chip' time measurement circuitry, namely, it has a wide dynamic range, high resolution, robust to the effects of PVT and has a small area overhead.

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Chapter 1

Introduction

1.1 Background

Recently, Integrated Circuits (ICs) have seen large advances in terms of performance and functionality per unit area to address the demands of market forces. Typically, these advances have been achieved by scaling down the size of the transistors, which also has reduced the cost per transistor, as a large number of scaled-down transistors can occupy a smaller area [1]. In addition, the reduction in transistor size will continue and is expected to reach 10 nm by 2015 [2]. However, as the scaling down of technology has been increased to meet the demands of market forces, the effect of random variations in the fabrication process has also increased, causing a reduction in the robustness and reliability of the designs [3-5].

Process variation is a challenging problem in very deep sub-micro CMOS process technologies. As the device dimensions are scaled down, design parameter variability is producing increasingly unpredictable consequences in circuit performance. As a result, maintaining the correct timing relationships between signals in an IC is becoming problematic and, ultimately, can cause a functional failure. However, it is becoming more difficult to measure the temporal relationship between signals in an IC using Standard Automatic Test Equipment (ATE) due to the lack of measurement resolution and accessibility, resulting in the need for on-chip time measurement circuitry [6, 7], which is the objective of this project as discussed later.

This chapter continues with an overview of manufacturing defects in Section 1.2, while Sections 1.3 describes some timing anomalies which occur in circuits such as jitter, clock skew and metastability which need to be measured. Section 1.4 outlines the design criteria to be satisfied for an effective implementation of an "on-chip" time measurement scheme. The Chapter concludes with the contributions made to this area of research and a road map of the thesis, in sections 1.5 and 1.6.

1.2 Process Variation and Manufacturing Defects

The manufacture of present day ICs is a complex process requiring an excess of 900 steps and 34 masking levels. At any stage a scratch on a mask as a contaminant can result in open or short circuit occurring in the interconnections. In addition, the variability in doping, etching, oxidation, metallisation, and other fabrication steps produces a random variation in transistor and interconnect parameters [8-10]. The effect of random variations in the fabrication process has increased as scaling technology has reached the nanometre regime [3, 4]. For example, the ultra-thin gate oxide layer , in the range of 1–3 nm, in the extremely deep sub-micron CMOS process, has become very sensitive to very small variations in the fabrication process [3]; the effect of process variations on gate oxide has a direct impact on the electrical characteristics of the transistor. As another example, with the reduction in the transistor size the amount of dopant atoms has decreased and the subsequent impact of random dopant fluctuation has been magnified [11]. This variation on the electrical characteristics of the transistors has an influence on the overall circuit performance [12]. Figure 1.1 shows examples of the effect on interconnect resulting from defect in the manufacture process.

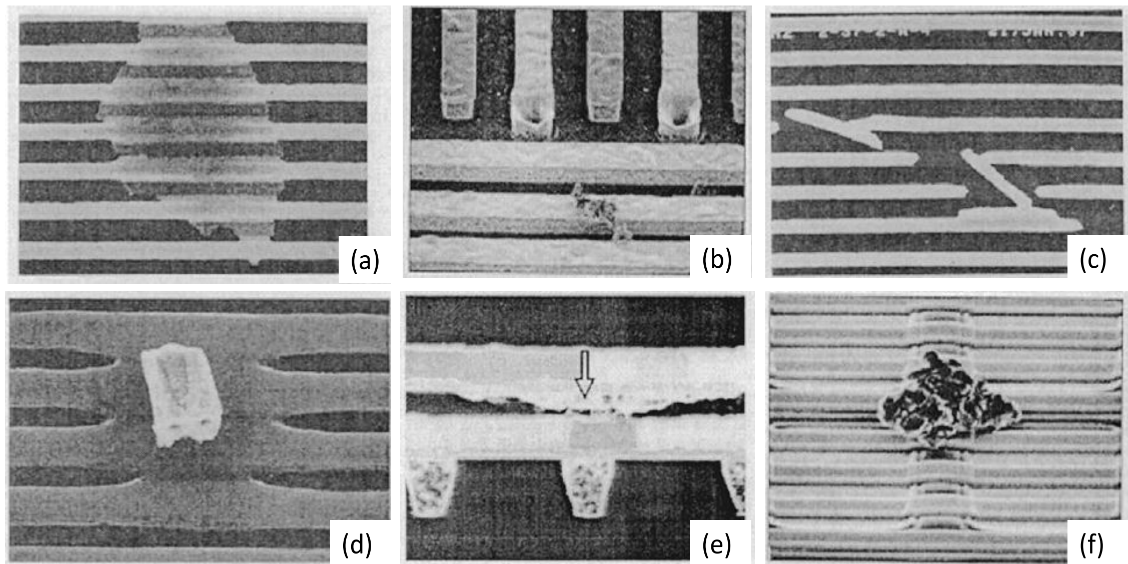

Figure 1.1: Common interconnect defects (a) shorting of metal lines owing unexposed photoresist (b) metallization defect causing a short between two lines (c) shorts and breaks of metal lines due to a scratch in the photoresist (d) shorting among several metal lines as a result of a solid-state particle on the metal mask (e) Inter-layer short between two interconnects (f) short among several metal lines due to a metallization defect [13].

1.2.1 Causes of Delay Faults

As the device size is continuously scaled down, both the speed of the device and its packing density are increased, which leads to an increase in IC performance. However, high performance ICs have a lower timing budget. The time budget is the smallest margin of time in the clock pulse which is necessary to ensure the correct temporal operation of a circuit, for example, latching data into a register. This narrow margin must take into account all the system delays, clock skew and clock jitter, and must be calculated as narrow as possible if the performance of the circuit is to be optimal. As the timing budget is decreased, the discrepancies in the temporal relationships between signals on the chip have become a major design issue, especially in synchronizer circuits where a clock or multiple clocks control the performance and function of the circuits. The faulty behaviour in the timing relationships between signals are typically caused by defects in the manufacturing process or the operating conditions in the circuit as described below.

a) **Delays resulting from fabrication defects:** Defects during manufacture which cause delay faults can be categorised into two main groups, namely, transistor and interconnect. Transistor defects can either decrease or increase the switching

speed of the device. For instance, the Gate-Oxide-Short is one of the transistor defects which has a large impact on the transistor structure affecting the electrical properties of a device [14, 15]. A Gate-Oxide-Short occurs when the integrity of the gate oxide is compromised, due to the lithographic defects or gate oxide growing defect, causing a short circuit between the gate and drain, source or transistor channel, as shown in Figure 1.2. This short circuit between the polysilicon gate and underlying silicon surface creates a resistance depending upon the defect size. The Gate-Oxide-Short increases the delay fault by an amount depending upon the value of the resistance which is created by this defect. In addition, there are several transistor defects causing a delay faults such as defective p-n junctions, transistor with incorrect threshold voltages due to the affects of process variations [14]. On the other hand, delay defects can be caused by the imperfections occurring, during fabrication of interconnect creating resistive opens and shorts [13, 14].

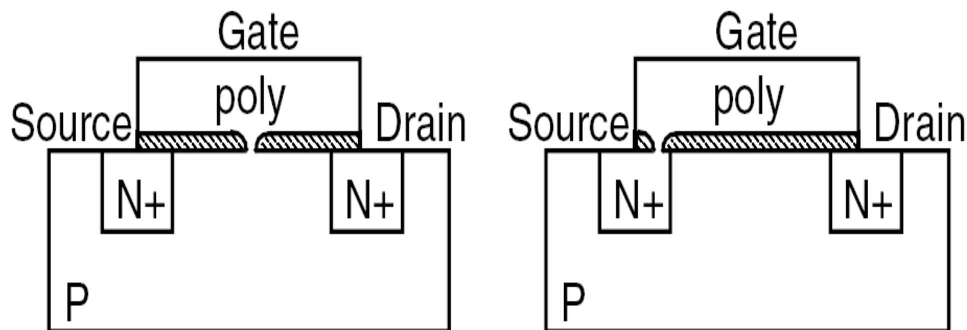

Figure 1.2: Gate-Oxide-Short (short between polysilicon gate and underlying silicon surface).

b) **Delays resulting from the operating conditions:** Intensive mixing of different circuits, which are composed of storage elements, dynamic gates, latches, and so on, combines with the defects in the transistors and interconnects create devices with different driving strengths and load mismatches, which leads to cross-talk and internal noise between elements. Cross-talk, according to its effect, can cause either a pulse or a delay [15-19]. The first type occurs when one of the wires is static, and transitions, through capacitive coupling, on the neighbouring wires cause a pulse on it, as shown in Figure 1.3 (a). The second type results from two neighbouring wires having transitions in the same or opposite directions. However, as shown in Figure 1.3 (b), if both transitions propagate in the same direction, the transition delay is reduced. This is called cross-talk

speed-up. By contrast, if both transitions propagate in the opposite directions, the transition delay is increased, as shown in Figure 1.3 (c) and is referred to as cross-talk slow-down.

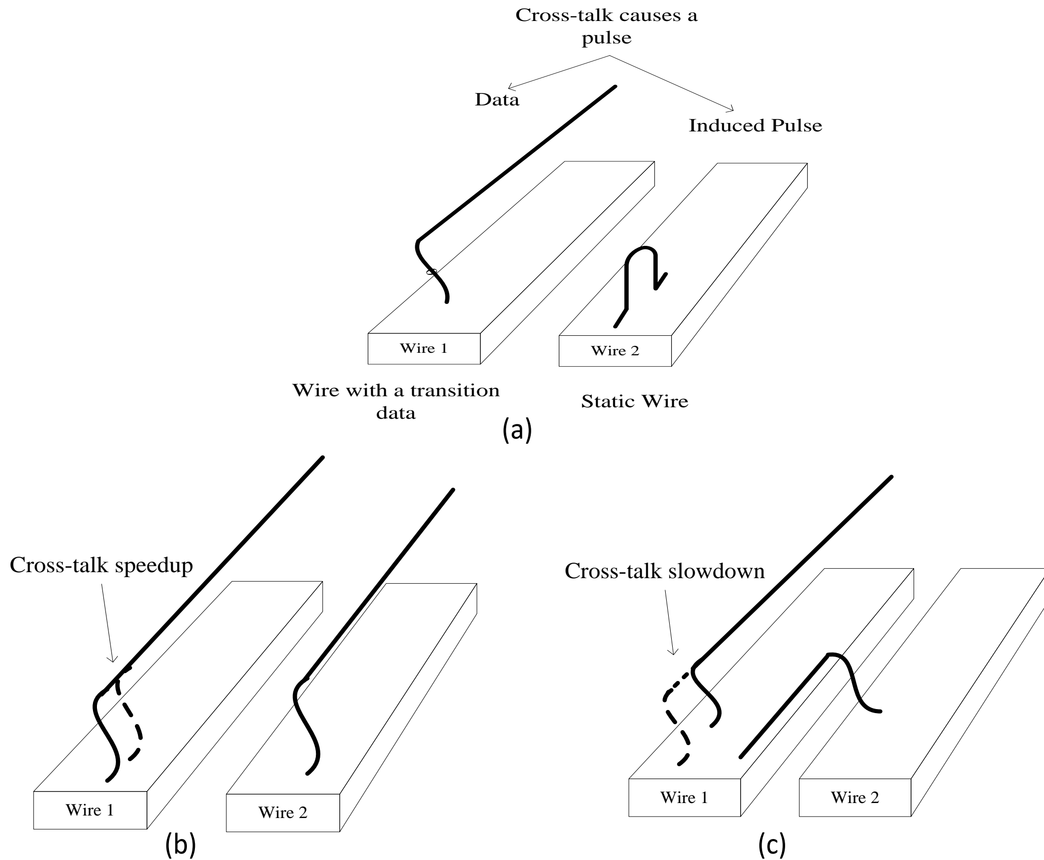

Figure 1.3: Cross-talk causing (a) a pulse, (b) cross-talk speed-up and (c) cross-talk slow-down.

Delay faults can also occur during normal operation due to variations in power supply voltage and temperature [8, 20, 21]. The difference in temperature within the die is one of the challenges for high speed ICs [21]. As shown in Equation (1) [22], the inverter delay is a function of the supply voltage and also the drain saturation current $I_{D(S)}$, which itself is affected by supply voltage and temperature [21].

$$T_P = \left[\frac{\frac{V_{TH}}{V_{DD}} + \alpha}{1 + \alpha} - \frac{1}{2} \right] \cdot T_{IN} + \frac{C_T \cdot V_{DD}}{2 \cdot I_{D(s)}} \quad \text{--- (1.1)}$$

Where v_{TH} = the threshold voltage, α is the velocity saturation index ($1 \leq \alpha \leq 2$) C_T is the total capacitance discharged, T_{IN} is the input rise/fall time, and $I_{D(s)}$ is the drain saturation current.

Delay faults as a result of fabrication defects and operating conditions cause discrepancies in the temporal relationships between signals, which are the main reasons for the occurrence of clock jitter and clock skew.

1.3 Timing Anomalies

The main timing anomalies which can occur within a circuit associated with clock signals are jitter, skew and metastability.

a) **Clock jitter:** Clock jitter can be defined as a variation or displacement in the phases of the clock from their ideal position. Jitter, depending upon how it is measured, can be classified as: cycle to cycle jitter, period jitter, and long-term jitter [23-27], as shown in Figure 1.4. Cycle to cycle jitter is the change in the cycle phase compared with the previous cycle; period jitter is the change in the clock phase compared with the fixed ideal position, where normally a reference clock represents the ideal clock. Long-term jitter is related to the change in the clock phases compared with their ideal position for a large number of cycles. Jitter values are represented either as an average value of the variation in the clock phases, the peak-to-peak value which is the maximum and minimum variation in the clock phases, or a combination of both.

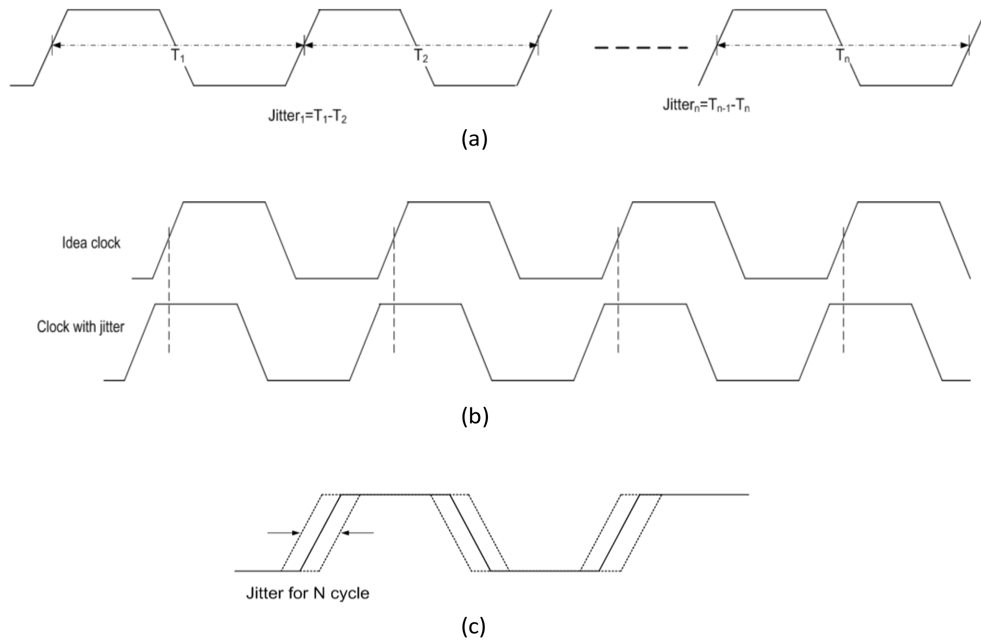

Figure 1.4 (a) Cycle to cycle jitter, (b) Period jitter, and (c) Long-term jitter.

b) **Clock skew**: Clock skew is defined as the differences in the arrival of the clock to several elements at different times which would cause a functional error [28, 29]. Figure 1.5 shows a clock skew which is caused by the delay in clock routing T_{skew1}, T_{skew2}, and T_{skew3}.

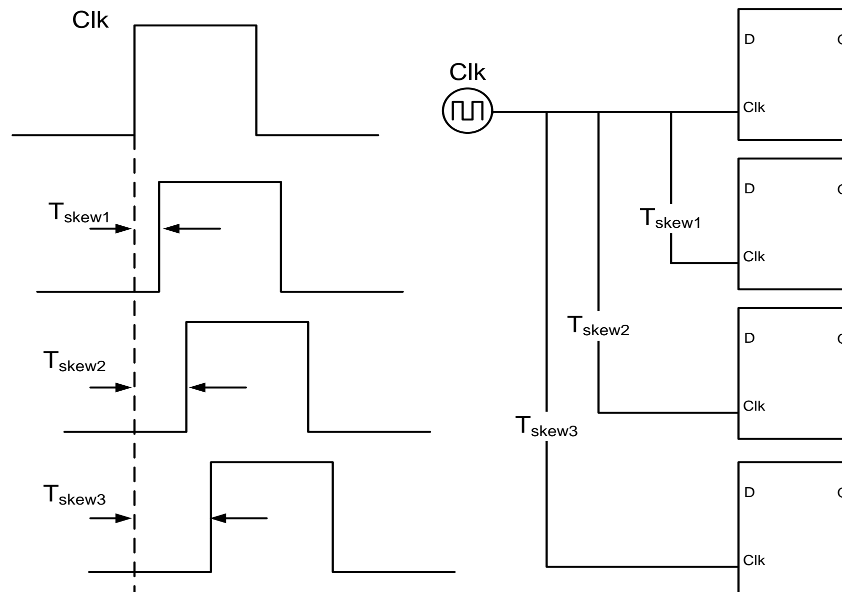

Figure 1.5: Clock skew signals.

c) **Metastability:** The metastability [30, 31] occurs in synchroniser circuits, such as flip-flops and latches, when the arrival-time differences between the data and clock violates the minimum set-up time leading the output to go into a metastable state. In this state, the output voltage remains in the middle between

the high and low values, where after a certain time the output settles to either a high or low value, the output becomes difficult to be predicted. This issue is normally avoided, as the output is estimated to be stable after each clock cycle. Figure 1.6 describes the behaviour of the flip-flop with variations in the arrival times of the data and clock, and the responses of the output.

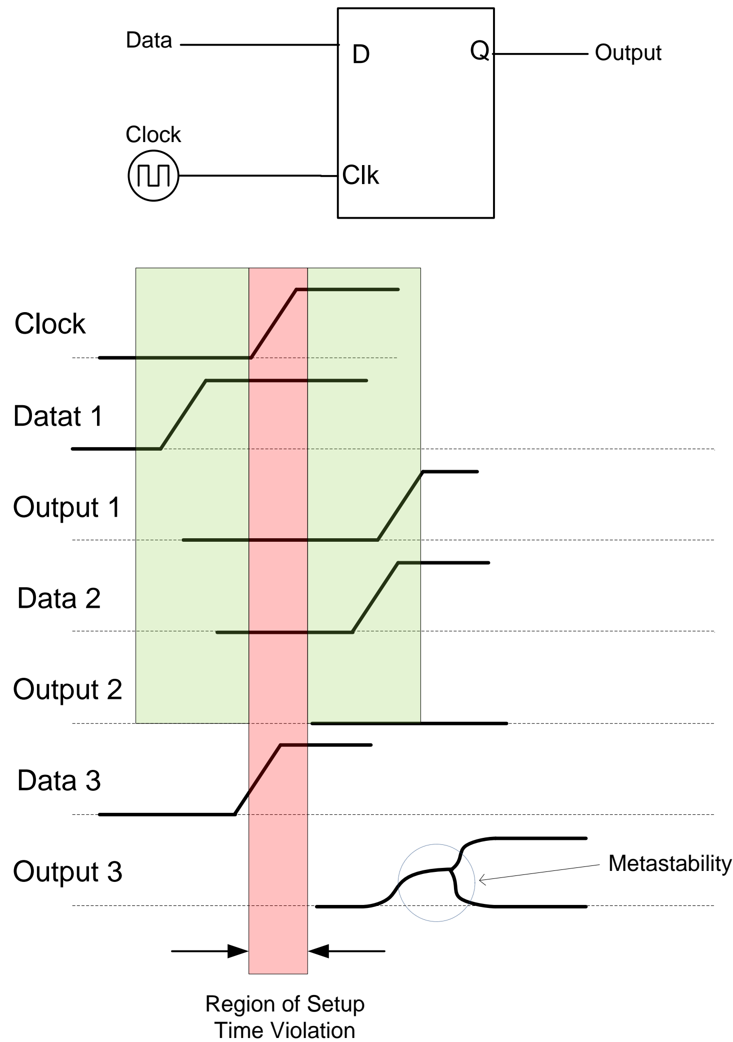

Figure 1.6: The responses of the flip-flop output to the different temporal relationships between data and clock signal.

1.4 On Chip Time Measurement

Since many of the timing anomalies occur within an IC, standard ATE cannot be used due not only to accessibility issues but also due to a lack of measurement resolution, necessitating in the use of "on-chip" time measurement schemes. The requirements to be met by the "on-chip" time measurement scheme depends upon the application and hence are quite diverse. However, there are five main design parameters which must be

considered; namely, measurement resolution, measurement dynamic range, time measurement, measurement error and calibration technique. These are described blow in more detail.

a) **Measurement resolution:** This term defines the minimum difference in the time interval which can be measured. The value of the measurement resolution depends on the requirements of the application. For example, jitter measurement requires a higher resolution than one used for some physical experiment, such as particle identification in Time-of-Flight (TOF) detectors, where a resolution of few tens of picoseconds is sufficient to attain a result [32].
b) **Dynamic range:** The dynamic range is the difference between the maximum and minimum values of the time intervals that can be measured. Defining the dynamic range also depends on the applications requirements.
c) **Measurement time:** This is the time taken to perform the measurement. However, this parameter is linked to the measurement dynamic range and the technique used for the time measurement.
d) **Measurement error:** The accuracy of a given measurement technique is affected by process, power supply and temperature variations. Moreover, as the device sizes are scaled down, the measurement error is increased owing to the increase in sensitivity to the variations of process, temperature and power supply. In addition, interconnects in the time measurement circuit can cause an additional delay between the two input signals, which leads to an error in the measurement. Therefore, an accurate calibration technique is required to reduce these defects.
e) **Calibration technique:** This is the method used to maintain the accuracy of the measurement. There are several methods of calibration, such as comparison with a standard measurement [33] or a statistical method [34]. The calibration technique not only impacts on a measurement technique in terms of the measurement accuracy, power consumption and area overhead but also in terms of the time taken and the complexity of the procedure itself.

The importance of each of the above criteria depends upon the application. When the various measurement schemes are reviewed in Chapter 2, the advantages and disadvantages of each, regarding the above design attributes, will be outlined.

1.5 Research Contribution

The following paragraphs outline the main research contributions described in this thesis:

a) **Improvements to time resolution:**

As clock speeds increase improvement in time measurement resolution are required. The use the concept of "time amplification" is a way of achieving this improvement. However, using a time difference amplifier in time measurement meets a major limitation due to the narrow dynamic input range of the time difference amplifier. In this work a time difference amplifier has been developed incorporating three techniques to improve the circuit and dynamic range. The first technique uses *Unbalanced Active Capacitance Loads* which have the same result as the buffer delay offset design (current method) [35], with a reduce area overhead and increased robustness to the effects of process variation, as discussed in Chapters 3 and 4. The second method uses *Unbalanced Active Charge Pump Loads*, in this design, the dynamic input range is extended by approximately 75% compared with the buffer delay offset design, as described in Chapter 3. The third technique uses *NAND Gate with Added Resistance* which can be use in conjunction with the buffer delay offset, the unbalanced capacitance load and the unbalanced charge pump load circuits extending their dynamic range, as highlighted in Chapter 3. For example, the dynamic input range of the unbalanced charge pump load design is extended from 70 ps to 300 ps using NAND gate with added resistance.

b) **Programmable time difference amplifier:**

The programmable time difference amplifier circuit is an all-digital wide dynamic input range time difference amplifier with adjustable gain as described in Chapter 3. The programmable time difference amplifier is designed to have a variable gain ranging from 4 to 117 with a very wide dynamic input range.

c) **Analysis of the effects of process variation:**

The robustness to effects of power supply, temperature and process variations was analysed on the buffer delay offset, unbalanced capacitance loads, unbalanced charge pump loads and NAND gate with added resistance techniques as described in Chapter 4. These studies were undertaken with the

aim of minimising the effects of the process variation on the time different amplifier circuits. The results show that unbalanced active capacitive load and unbalanced active charge pump load designs are more robust than the buffer delay offset design in terms of gain variation. In addition, although, implementing the three time difference amplifier circuits using NAND gate with added resistance creates a huge improvement in terms of the dynamic input range, the gain sensitivity to the process variations is increased. Moreover, the gain of the buffer delay offset design when implemented using the NAND gate with added resistance was significantly affected by the process variation compared with the unbalanced active capacitive load and unbalanced active charge pump load designs.

d) **A reconfigurable time measurement circuit:**
A reconfigurable time measurement circuit was designed with an adjustable resolution range of 15 down to 0.5 ps and a measurement dynamic range of 480 to 16 ps to perform a variety of time related measurements which require different test specifications; such as set-up and hold time measurements and jitter measurement. It is considered that a reconfigurable measurement system will occupy less chip area than a range of measurement circuits designed for one specific test. The reconfigurable time measurement consists of two parts, a programmable time difference amplifier and a 32 cell tapped delay line. The programmable time difference amplifier is designed to have a gain ranging from 4 to 117 with a very wide dynamic input range.

It is considered that the above contributions make an advancement to the state of art related the on-chip time measurement techniques. In addition, during this work, a journal and a conference papers have been published [36, 37].

1.6 Thesis Roadmap

The motivation, background and need for this work have been discussed in the previous sections, the roadmap of the remainder of the thesis is outlined below.

The techniques currently used for time measurement are reviewed in Chapter 2. In addition, the advantages and disadvantages of each method are discussed comparing the following parameters: measurement resolution, dynamic range, measurement time,

measurement error and calibration technique. The chapter is sectionalized depending on the methodology that has been used.

In Chapter 3, three techniques to improve the dynamic range of the time difference amplifier are outlined. In addition, the analysis of the buffer delay offset design is discussed and compared with the new techniques. Gain and amplification range are the main parameters which are compared. The chapter concludes with a description of the design of the programmable time difference amplifier.

In Chapter 4, the reliability of the buffer delay offset, unbalanced active capacitive load, unbalanced active charge pump load and NAND gate with added resistance techniques are discussed. In this study, Monte Carlo (MC) analysis is used, as it is more pragmatic to study the process variations effect than using multiple corner analyses [37]. The MC was run considering the process variation of 3σ with 2000 samples at Vdd = 1V and 27°C. Moreover, the effect of the voltage supply and temperature variation is discussed.

In Chapter 5, the design of a reconfigurable time measurement scheme with adjustable resolution and dynamic range is described. The reconfigurable time measurement scheme is first configured to measure the time difference between two signals. After performing the measurement, the time measurement circuit can be reconfigured to different resolution and dynamic range in order to be reused for other time measurements, such as jitter, set-up and hold times etc. The time measurement circuit with reconfigurable resolution and dynamic range can be considered to consume less area overhead compared to the fixed resolution time measurement, as the same circuit is used for different functions. In addition, in this Chapter, the calibration circuit for the reconfigurable time measurement is discussed. The calibration procedure is based on calibrating the tapped delay line to known delay values thereafter the gain of the time amplifier is measured using the calibrated tapped delay line. The reconfigurable time measurement circuit was designed in a 90nm CMOS technology where the chip layout is implemented as a full custom design. The area occupied by reconfigurable TIM circuit is 379.5 µm x 67.5 µm.

Finally, Chapter 6 outlines the summary and conclusions to this work and the possible future works.

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Chapter 2

Time Measurement Techniques

2.1 Introduction

Time measurement has become an area of interest for researchers as it can be used in several applications such as distance measurement, particle physics, astronomy, nuclear physics and dynamic testing of ICs. A wide range of methods have been proposed for time measurement in order to improve the resolution, dynamic range, and reduce area overhead, complexity of the calibration procedure and measurement time [1-8]. However, defining each of these parameters depends on the requirements of the wide range of time measurement applications. Figure 2.1 classifies the range of time measurement techniques based on their methodology.

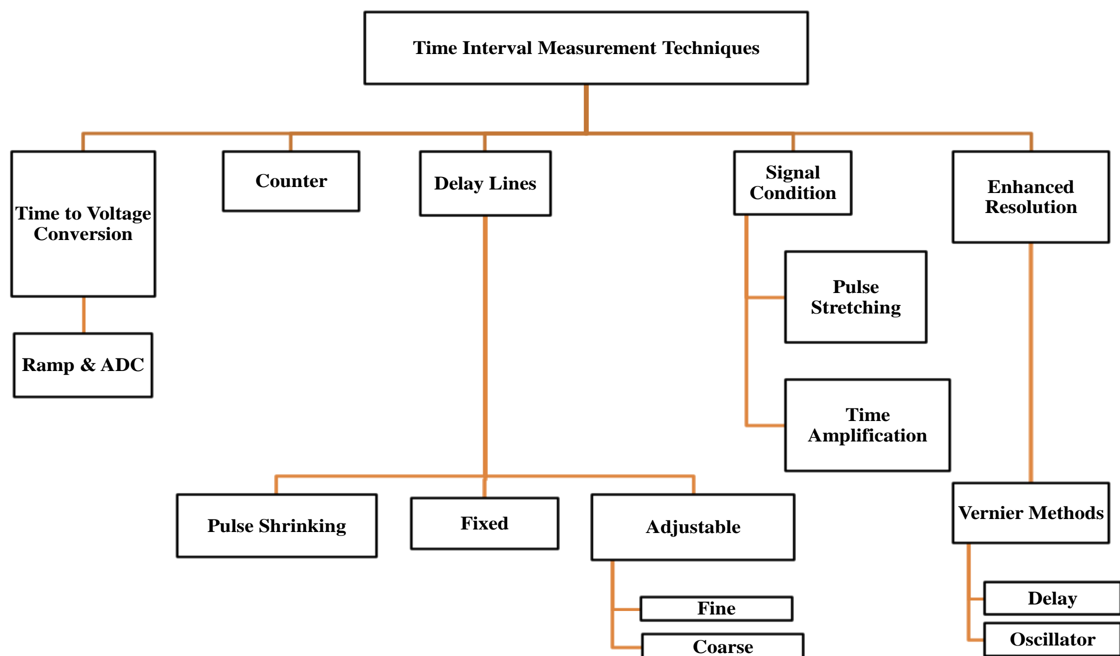

Figure 2.1: Taxonomy of time interval measurement techniques [9].

In this chapter a review is undertaken of examples of each of the cited generic time measurement techniques shown in Figure 2.1, highlighting the advantages and disadvantages of each. The subsequent sections of this Chapter comprise a description of the counter based method in section 2.2, followed in section 2.3 with an outline description of the time to voltage conversion technique. In section 2.4, the signal condition technique is discussed, followed, in section 2.5, by the description of the delay line method. The Vernier method and the combination of coarse and fine delay techniques are described in sections 2.6 and 2.7 respectively. A description of the time measurement in Field Programmable Gate Arrays (FPGA) is given in section 2.8, followed by a summary of the attributes of the techniques in section 2.9.

2.2 Counter Based Method [10, 11]

The counter based method is a basic and simple technique used to measure time intervals, it comprises two main parts, a counter and a frequency generator. It can be seen from Figure 2.2 that the generated frequency F_{gs} (or $1/T_{gs}$) must be much larger than the frequency of the signal under test ($1/T_{ps}$) as the resolution of the measurement is equal to T_{gs}. The rising edge of the signal to be measured is used to enable the counter, which is subsequently disabled by the falling edge. The measurement result is achieved by multiplying the value stored in the counter (N_m) by T_{gs}, that is $T_{ps\ (measured)} = N_m \cdot T_{gs}$. The magnitude of the error, as shown in Figure 2.2, depends upon the relative phase different between the rising edge of T_{ps} and T_{gs}. This error can be reduced provided that $T_{gs} << T_{ps}$. However, if T_{ps} is quite short, to ensure an acceptable measurement accuracy a high performance counter would be required. Alternatively, the effect of the error (T_{error}) can be minimised by repeating the measurement several times whilst T_{ps} is calculated as the average result of several measurements. However, the disadvantage of averaging is the increase in the overall measurement time.

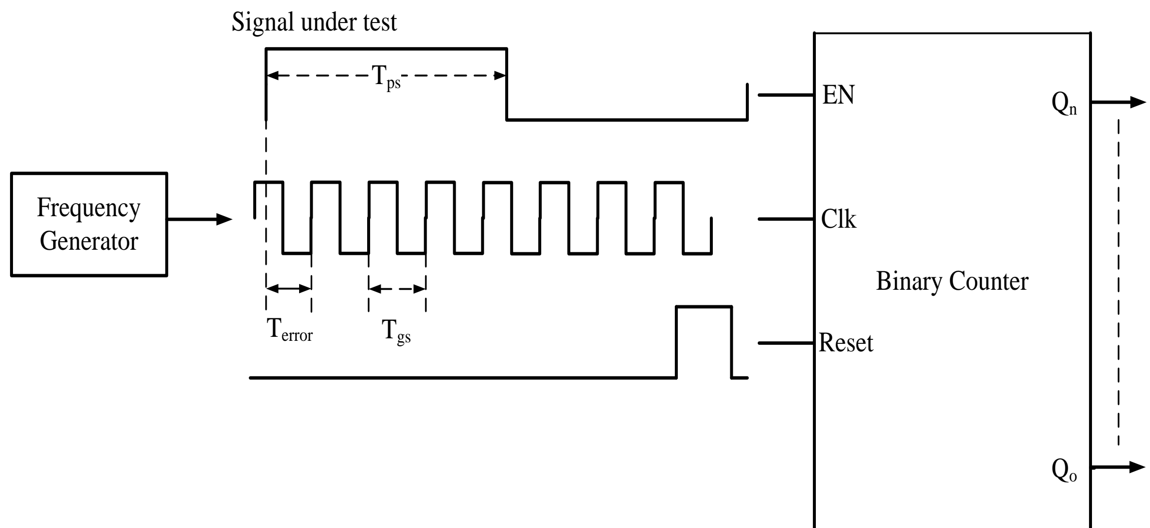

Figure 2.2: Time interval measurement using counter technique.

The main advantages of the counter technique are the simplicity of the method and the long dynamic range, although the method suffers from the low resolution unless a high frequency clock is used.

2.3 Time to Voltage Conversion Technique [12-15]

The time to voltage conversion technique is based on converting the time interval into voltage which is subsequently digitised. The main components used in this technique are a time to digital converter and an analogue to digital converter (ADC), as shown in Figure 2.3. The rising edges of the two signals whose time difference is to be measured are used, shown in Figure 2.4, as start and stop signals to the pulse width generator creating an output pulse T whose duration is equal to the temporal difference between the two input signals. This pulse switches on the current source to charge the capacitance with a constant current value (I), for the duration of the pulse T. The subsequent output voltage, V_C, given by Equation (1), is then passed to the ADC.

$$V_C = (I_o / C) \cdot T \text{ --- } (2.1)$$

Once the conversion is completed the capacitor is discharged and the measurement can be repeated.

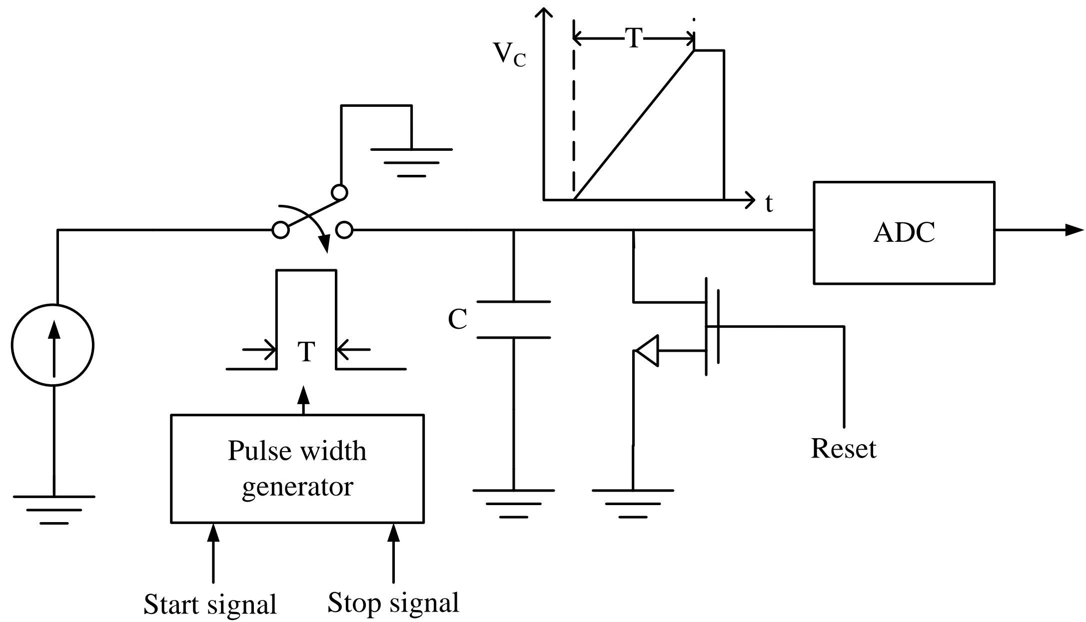

Figure 2.3: Time to voltage converter circuit [14].

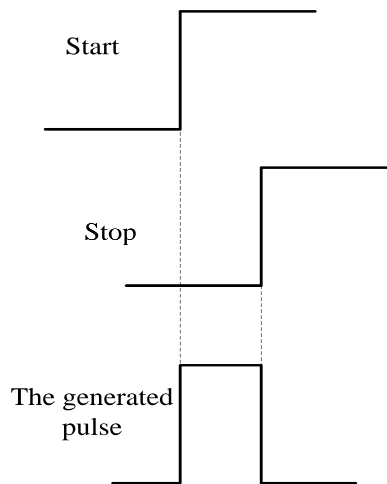

Figure 2.4: The generated pulse width equal to the time difference between start and stop signal.

It can be seen from Equation (1), the accuracy of the conversion is highly dependent on the ratio of the current I_o and the capacitance C which is required to be constant and stable. Therefore the accuracy is sensitive to process variation, temperature and power supply voltage, although a high resolution can be achieved by this method (1ps to 20 ps) [10]. In addition this method depends on analogue circuitry which is more sensitive to noise, temperature and power supply variation compared to the digital technique which will be discussed later.

2.4 Signal Conditioning

Signal conditioning is a technique used to enhance the resolution of time measurements by stretching the input time interval. Signal conditioning techniques can be divided into those which use a pulse stretching technique [10, 16] and those which use time difference amplification [17-20]. A combination of one of these techniques and a time measurement method can improve, greatly, the resolution of the time measurement system. For example, in the counter based method, whilst the resolution is low and limited to the value of the frequency generator, as described in section 2.2, a combination of the pulse stretching method and counter method can increase the resolution to higher value [16], as will be discussed later. Both pulse stretching technique and a time difference amplification techniques are described in detail below.

2.4.1 Pulse Stretching [10, 16]

The principle of the pulse stretching method depends on stretching the input time interval using the difference between the charge and discharge time of a capacitance, as shown in Figure 2.5. The current I_2 is designed to be much smaller than the current I_1. As a result, when an input signal with a pulse period, T, is applied to switch S_1, the capacitance starts charging with a time duration, T, and with a large current equal to (I_1- I_2), where $I_1 >> I_2$. However, during discharge, S_1 is switched off while the capacitance is discharged with a smaller current I_2 resulting in a longer discharge time (T_r) greater than the charge time (T). The relationship between T and T_r is nearly linear and is given by Equation (2).

$$T_r = A \cdot T \text{ --- } (2.2)$$

Where A is the stretching factor and can be calculated as

$$A = (I_1 - I_2)/I_2 \text{ --- } (2.3)$$

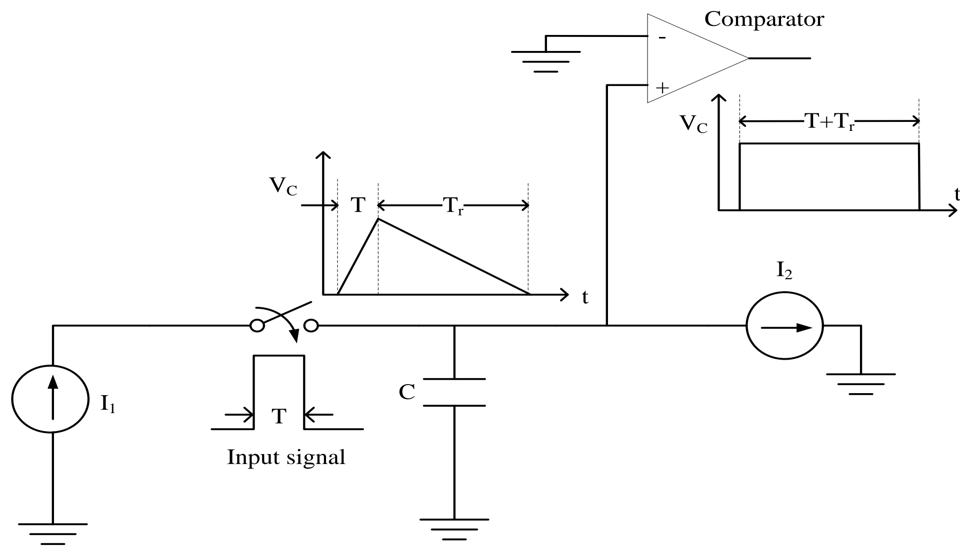

Figure 2.5: Pulse stretching circuit [10].

As mentioned previously, the pulse stretching method can be combined with the counter method to achieve a high resolution time measurement system where the resolution is calculated as $T_g / (A + 1)$ [10]. However, this method suffers from long time conversion, as the capacitor (C) is required to be charged and discharged for each single measurement, which limits the technique to be used for a low frequency or single shot applications.

2.4.2 Time Difference Amplifier

A time difference amplifier is another way to increase the resolution of the time measurement. The principle of the time difference amplifier, which was first proposed in [17], is to amplify the time difference between the two input signals (ΔT_{input}) with a constant gain (G), as shown in Figure 2.6. Time difference amplification can be achieved using either analogue or digital circuitry.

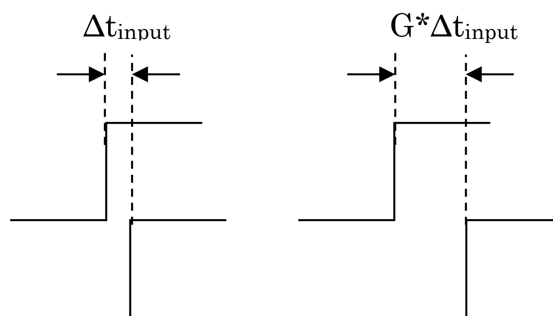

Figure 2.6: The concept of time amplifier.

a) Time difference amplifier using analogue circuitry: Two time difference amplifiers have been proposed which use analogue circuitry [18, 20]. The first time difference amplifier is designed using two cross-coupled differential pairs, as shown in Figure 2.7. The amplification in this technique is based on the charging and discharging between C_1 and C_2 in each differential pair. The time difference between the outputs (ΔT_{out}) of the coupled differential circuits is proportional to the time input difference (ΔT_{input}). The main advantage of this design is the higher gain which reaches 180 with a wide range of the input time differences, about several hundred picoseconds. However, this design requires a bias voltage to be set to a specific constant value in order to create the amplification between the two cross-coupled differential pairs. Therefore any variation in the value of the bias voltage affects the circuit stability and performance. In addition, as the design is analogue, it is highly sensitive to noise, variations in temperature, process and power supply voltage. However, this technique will not be discussed further, as this design is an analogue technique which is more sensitive to noise, temperature and power supply variation compared to the digital technique, thus this thesis is focused on the digital time difference amplification techniques.

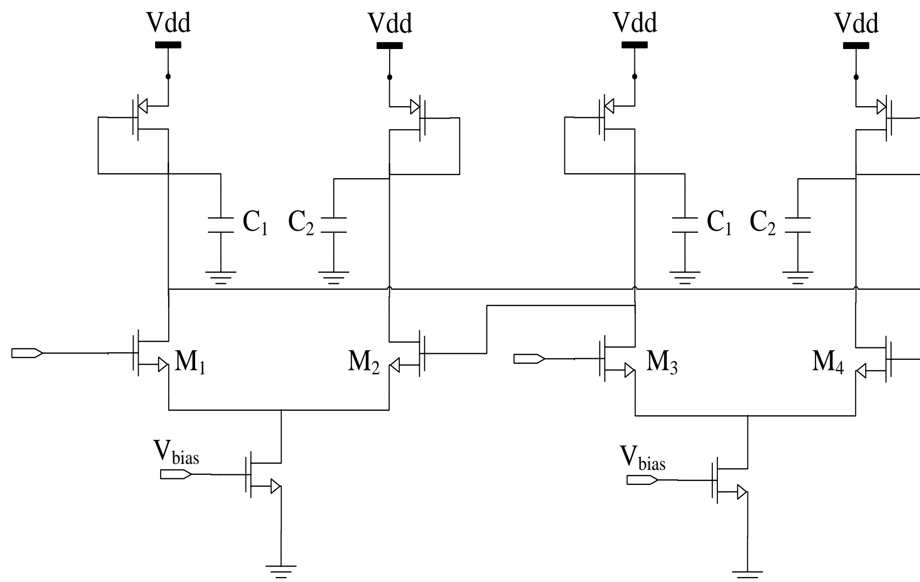

Figure 2.7: Time difference amplifier using analog circuit [20].

b) All Digital Time Difference Amplifier: The time difference amplifier can also be implemented using digital circuitry [17] comprising two MUTEX circuits, as shown in Figure 2.8. A MUTEX consists of an S-R latch followed by a metastability filter circuit consisting of two inverters, whose inputs also act as power sources, as shown in Figure

2.9. A MUTEX is normally used to determine which of the two inputs arrives first. However, when the inputs of a MUTEX arrive with a very small time difference, the output goes into a metastable state, a condition which is normally avoided. This metastable condition produces a delay dependent upon the time difference between the input signals. Based on this behaviour a time difference amplifier can be designed by using two MUTEX circuits with opposite offsets, as shown in Figure 2.8. The offset is created by increasing or decreasing the transistors size of the NAND gates. The equation for amplification gain is given in Equation (4).

$$\Delta T_{out} / \Delta T_{input} = (2 \cdot \tau) / T_{offset} \text{ --- } (2.4)$$

Where: ΔT_{input} is the time difference between the input signals, T_{offset} is the time offset created by the MUTEX circuit, ΔT_{out} is the time difference between the output signals and τ is MUTEX time constant.

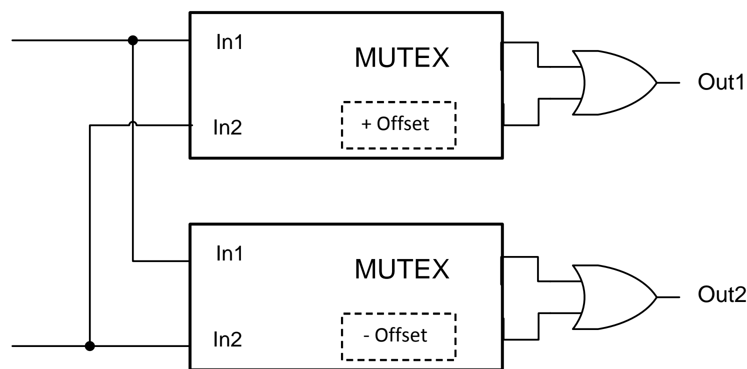

Figure 2.8: Time difference amplifier circuit [17].

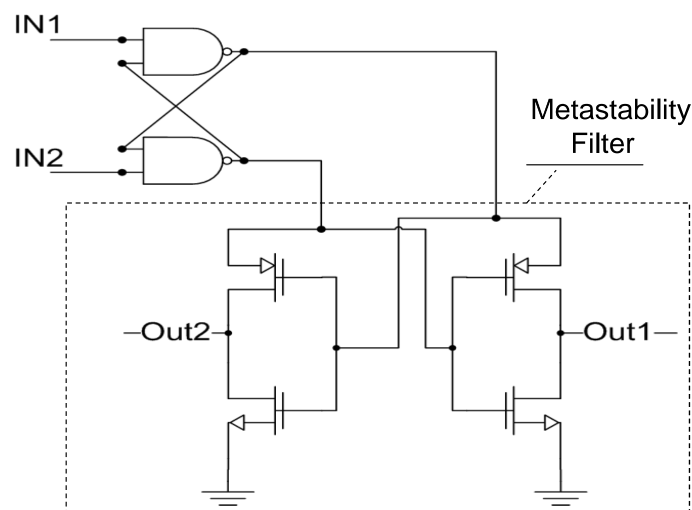

Figure 2.9: MUTEX circuit.

The main challenge in using the variation in the transistor size to create the time offset in a MUTEX circuit is the reduction in the dynamic input range as the transistor technology is scaled down. The dynamic input range of the time difference amplifier is referred to the range of the ΔT_{input} where the gain of the amplifier is linear. The effect of the scaled down technology on dynamic input range was discussed in [21] and is given by Equation (5).

$$t_m \propto -(L / W) \cdot C_{Tot} \cdot \ln(\theta \cdot \Delta T_{input} / \Delta v) \text{ --- } (2.5)$$

Where t_m is metastability time, L and W is the length and the width of the transistors respectively, C_{Tot} is parasitic capacitance of the MUTEX, θ is the conversion factor from time to initial voltage at the metastable nodes, ΔT_{input} is the time difference between the input signals and Δv is the voltage output difference during metastability.

Utilising the relationship given in Equations (4) and (5), another time difference amplifier, shown in Figure 2.11, was developed [19] incorporating buffer delay offsets. The gain, in the buffer delay offset design, was improved by adding more capacitance at the outputs of the NAND gates and reducing the transconductance of the all transistors in the NAND gates, while the dynamic input range was enhanced by creating the time offset using buffer delay. In the buffer delay offset design, a gain of the 20 with 40 ps dynamic input range was achieved using 90nm technology.

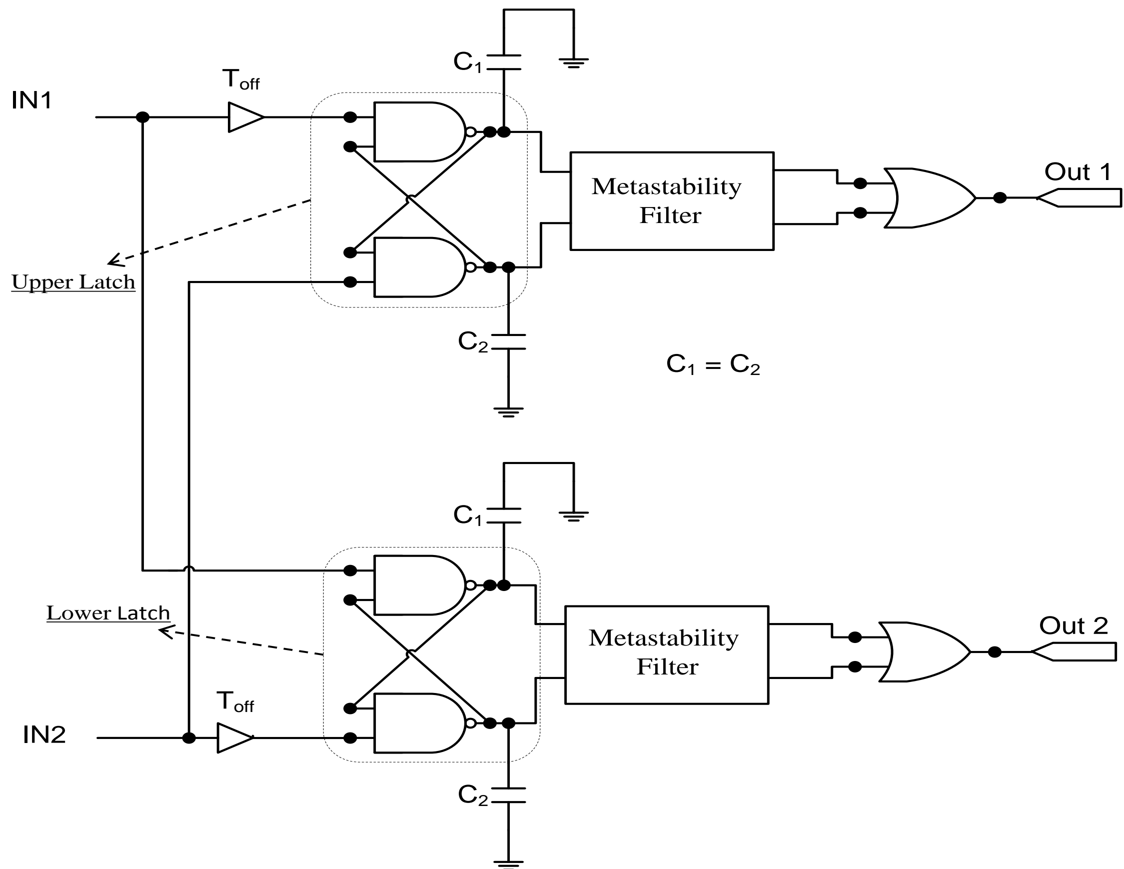

Figure 2.10: Time difference amplifier, buffer delay offset design [19].

Implementing the time offset as a buffer delay is susceptible to matching problems causing a mismatch in time offset; furthermore, for a wide dynamic input range a large delay is required which can only be achieved by either using large transistors or a chain of inverters. In addition, the dynamic input range in the buffer delay offset design is still limited to about 40 ps. Several new techniques to improve the performance parameters of time difference amplifier whilst avoiding the use of the buffer delay to create the time offset are discussed in Chapter 3.

2.5 Delay Lines

Time measurement using delay lines is one of the techniques which has been widely used, successfully, in a range of applications. It is based on creating a known difference in the delay between two paths propagating the signals whose time interval is to be measured. There are three types of delay lines, namely, fixed delay, adjustable delay and pulse shrinking technique as described below.

2.5.1 Fixed Delay Line [22]

The fixed delay line (tapped delay) comprises a buffer delay, which is implemented as a series of inverter pair and D-flip-flops (DFF), as shown in Figure 2.12. The test signals, which function as start and stop signals, are applied to the inputs of the circuit and compared after each buffer delay by a DFF. As both signals propagate through the circuit, the outputs of the DFFs are changed to a logic one as long as the start signal leads the stop signal. However, at a certain cell on the delay line, once the start signal lags the stop signal, the output of the DFF remains at zero and the measurement is terminated. Finally, the result of the time measurement is calculated by multiplying the number of the high state outputs by the value of a single buffer delay. It is clear that the resolution of this measurement is determined by the value of the buffer delay.

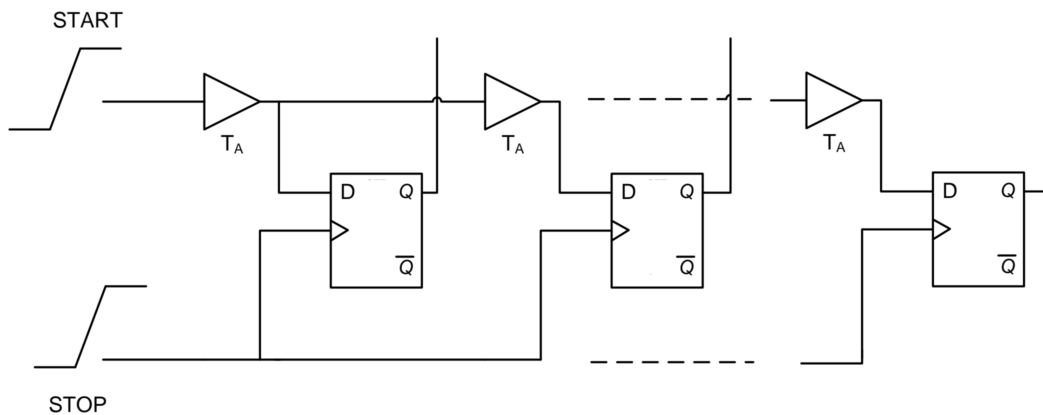

Figure 2.11: Block diagram of a tapped delay.

2.5.2 Adjustable Delay Line

As the name suggests, the adjustable delay line allows its value and hence the measurement resolution to be varied. The adjustable delay line is used for calibration purposes in some techniques and is essential in other applications such as laser altimeters, X-ray and ultraviolet imagers, etc [23]. Several implementations of adjustable delay line have been proposed [23-26], these can be classified as either coarse or fine. Figure 2.13 shows an example of a coarse delay line [9] which comprises a network of inverters. The delay of the line can be adjusted in steps of the delay of two inverters. The inverters are connected, as shown in Figure 2.13, through tri-state inverters which operate as switches in order to switch the delay elements in or out of the circuit. For example, assuming that $S_0 = 1$ while $S_1, \ldots, S_n = 0$ then inverters 1

and 2 only are switched into the circuit. However, if $S_1 = 1$ and $S_0, S_2, \ldots, S_n = 0$ then inverters 1, 3, 4 and 5 are switched into the circuit.

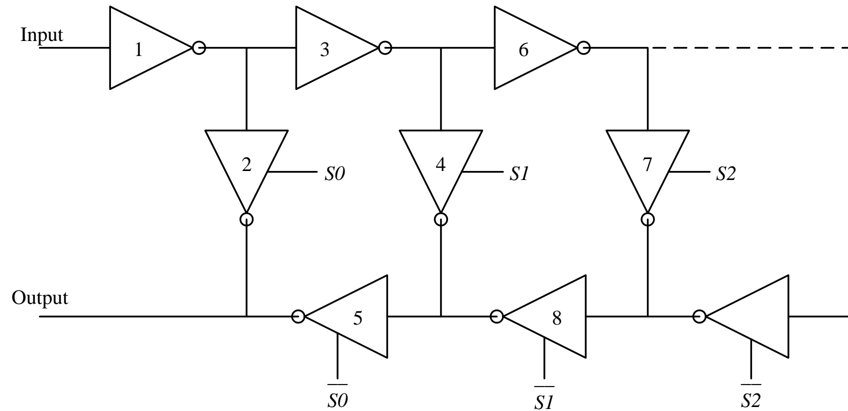

Figure 2.12: A simple adjustable coarse delay line [9].

On the other hand, the fine delay line has a higher resolution than the coarse delay line having smaller delay steps, which may have a value of 1ps or less [27]. Several fine delay line circuits are described below, namely, fine delay line using a bank of parallel NMOS capacitances, inverter matrix, the differential digitally-controlled delay cell and current starved delay element.

a) Parallel NMOS Capacitance Bank: In this technique a bank of NMOS capacitances are connected to a node between a two inverters as shown in Figure 2.14 [9]. The delay can be adjusted by switching the capacitances in or out of the circuit. The propagation delay is increased by switching more capacitance into the circuit. The adjustment of the number of the capacitance is controlled digitally. The sizes of the NMOS capacitances are designed to be equal in order to obtain equal delay steps. The delay step can be reduced by reducing the size of the NMOS capacitances.

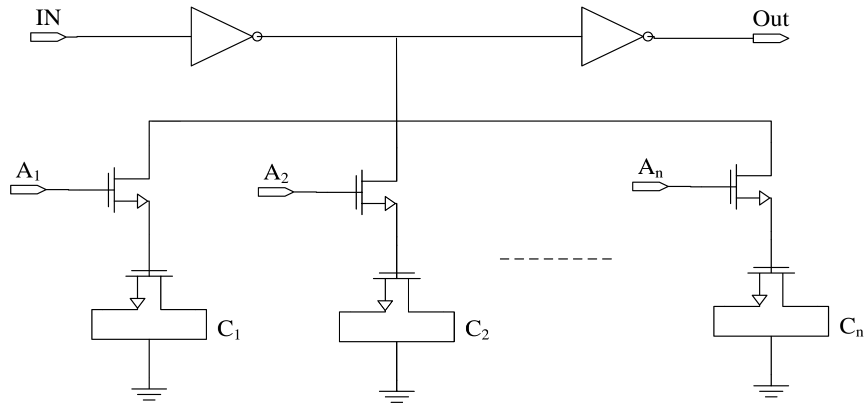

Figure 2.13: Adjustable fine delay line using a bank of parallel NMOS capacitances [9].

b) Inverter matrix [9, 24]: Figure 2.15 shows the circuit of a 2x16 inverter matrix delay, which contains two banks of parallel inverters. The delay is adjusted by enabling the required number of inverters in each bank providing a range of linear delays from 84 ps to 200 ps in steps of 2 ps. However the main disadvantages of this technique is the large area overhead as a large number of delay elements required.

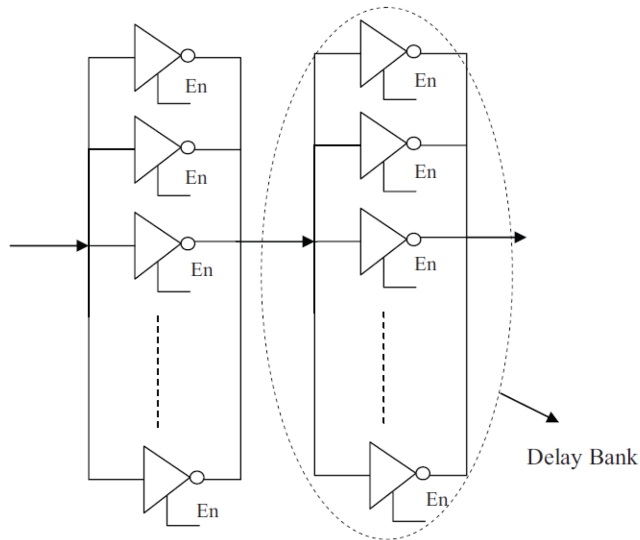

Figure 2.14: 2x16 inverter matrix [9].

c) The differential digitally-controlled delay cell [7, 28]: The differential digitally-controlled delay cell technique comprise two inverters whose delay is adjusted, as shown in Figure 2.16, by 16 control bits. The 16 bits control the charge and discharge current of the two inverters in order to adjust the gate delay. This system has a maximum resolution of 1ps in 0.35µm technology implementation which is linear over a wide range.

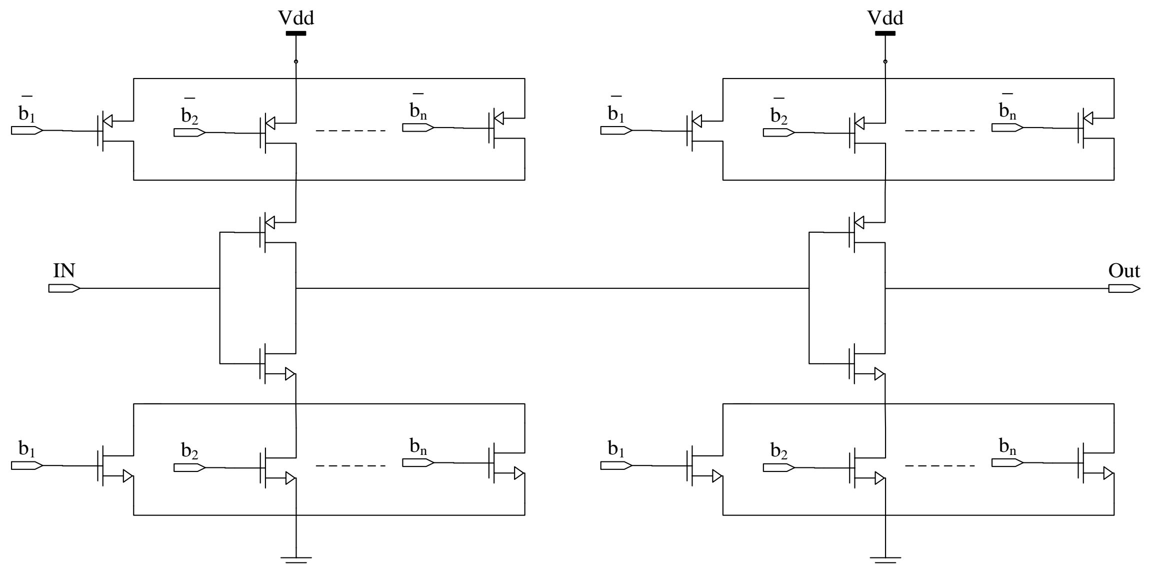

Figure 2.15: The differential digital-control delay cell [7].

d) Current starved delay element [27, 29]: The design of current starved delay element has an advantage of a very high resolution which is around a few hundred femtoseconds. The circuit contains a pair of inverters whose currents are controlled by adjusting the resistance of M2 and M5, as shown in Figure 2.17. This adjustment is achieved by tuning the gate voltage of M2 and M5 using four parallel transistors, M6, M7, M8 and M9. These transistors act as parallel resistances which can be switched into or out of the circuit digitally. The sizes of M6, M7, M8 and M9 are designed to support the adjustment in digital form. For example, if a small resistance is applied by switching M6, M7, M8 and M9 into the circuit, a large voltage is applied to the gates of M2 and M5 which lead to large current passing through the inverters. It is clear that larger inverters current leads to a speed up the inverters transitions which decreases the delay. However, if a large resistance is applied by switching only M9 into the circuit, which has the largest resistance as its width is the lowest, a small voltage is applied to the gates of M2 and M5 resulting in small inverter currents being passed to ground which increases the delay. This circuit is normally used for calibration purposes, as it has a very high resolution with fine steps, and has been used successively to calibrate a TDC [27] with a resolution of 0.6 ps. In addition it has been used [30] to generate a small delay of the order of femtosecond to measure the metastability of a bistable circuit.

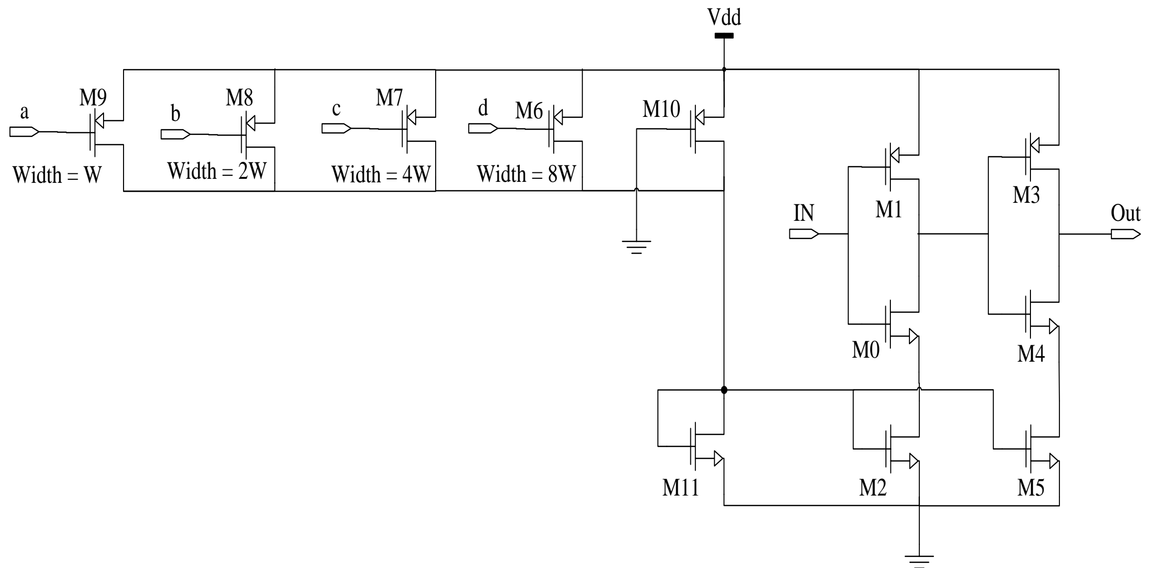

Figure 2.16: Current starved delay elements [27].

2.5.3 Pulse Shrinking Technique

The pulse shrinking method is based on reducing the period of the test signal gradually with fixed steps while a counter is used to count the number of reductions. Figure 2.18 shows a pulse shrinking circuit which comprises a NAND gate, pulse shrinking delay elements and a counter. In this technique, a single pulse shrinking delay element is used where its output is fed back to the input of the NAND gate. As the pulse shrinking delay element is arranged with regenerative feedback, a counter is used to count the number of cycles required for the input period to disappear. The measurement is started by, first, measuring a known reference signal of period (T_{ref}), followed by the measurement of the test signal (T_{test}). Then, the result of measuring T_{ref} is used in Equation (6) [31] to calculate the test signal period (T_{test}).

$$T_{test} = (n / N) \cdot T_{ref} \text{ --- } (2.6)$$

Where: N is the counter result of measuring T_{ref} and n is the counter result of measuring T_{test}.

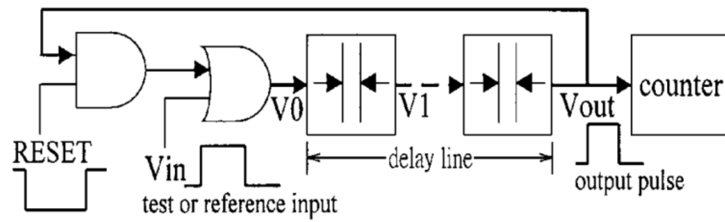

Figure 2.17: TDC pulse shrinking method [31].

The resolution of the pulse shrinking method depends on the pulse shrinking delay element circuit. The main challenge [31, 32] was the low resolution which is limited to 286 ps. In this technique, the pulse shrinking delay element circuit is designed as a pair of inverters, as shown in Figure 2.19. The first inverter is controlled by a bias current, N3, which slows down the input signal transition while the second inverter switches very fast resulting in a shortening of the input period by a value equal to the rise time minus the fall time of the input signal. It can be seen that the delay element is controlled by the bias current which is required to be set to a specific value to achieve stable reduction steps during the measurement. This system is thus very sensitive to noise, temperature and power supply variations.

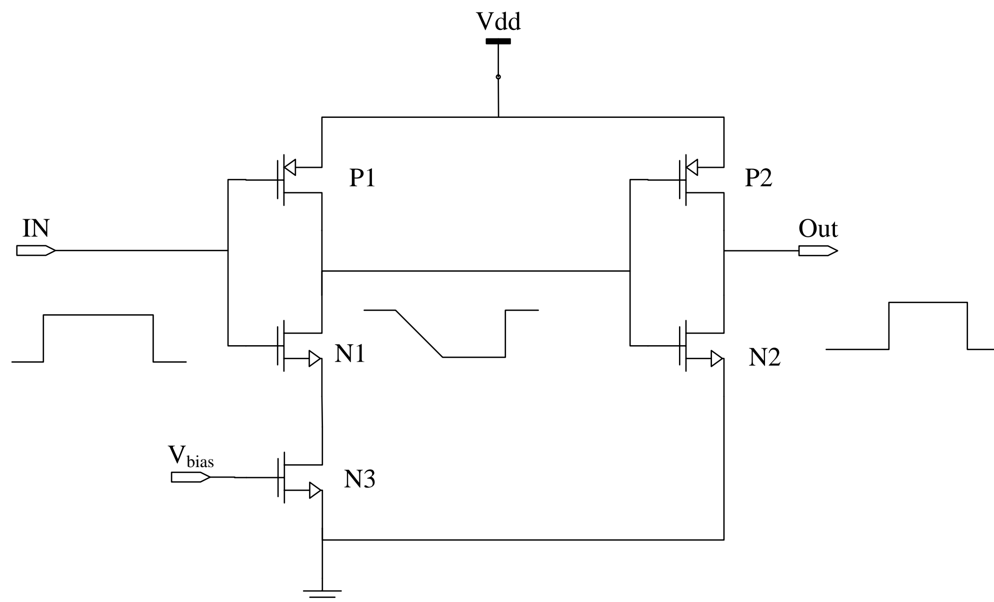

Figure 2.18: Pulse shrinking delay element circuit

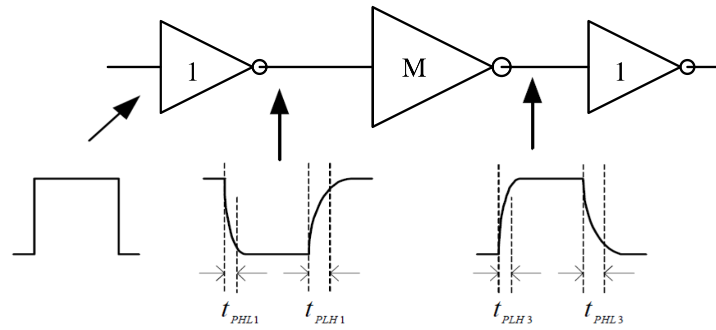

Figure 2.19: All-digital pulse shrinking delay element [2].

An all-digital pulse shrinking delay element was proposed [2] using a series of different sized inverters, avoiding the disadvantage of using a bias current. As an example of this technique, Figure 2.20 shows three inverters with the first and last inverters having the same transistors size while the middle one is larger. The larger inverter has a lower transition time than the other two which switch very fast. This results in a shortening of the input signal to a value proportional to the ratio of the inverter transistor widths. Using this method the measurement resolution was improved from 286 ps to 68 ps for 0.35-µm CMOS technology [2].

2.6 Vernier Method

The Vernier method is used to improve the resolution of the tapped delay line from one buffer delay to the difference between two buffer delays. This method is mainly divided into Vernier delay lines (VDL) and Vernier oscillator (VO) which are discussed below.

2.6.1 Vernier Delay Line (VDL) [3-5, 21]

Figure 2.21 shows a block diagram of a VDL which consists of two delay lines with different values. The difference between the delay T_A and T_B determines the measurement resolution. The measurement is started by applying two input signals, a data signal (start) and a clock signal (stop), to propagate through the two delay lines where, after each delay element, the signals are compared by DFF. If the data signal is earlier than the clock signal, the output of the DFF is set to a logic high. As the signal propagates along the line the difference in the delay between T_A and T_B in every cell causes the two signals to come closer together until the stop signal leads the start signal where upon the output of the DFF is set to a logic low and the measurement is finished.

Finally, the result of the time measurement is calculated by multiplying the number of the high state outputs by the measurement resolution. The dynamic range of this application is determined by multiplying the number of cells by the measurement resolution, the larger the number of cells the wider the dynamic range. However, implementing a large number of cells, to achieve a wide dynamic range, incurs a large area overhead which can be overcome using a combination of coarse and fine delay lines [8] as discussed later.

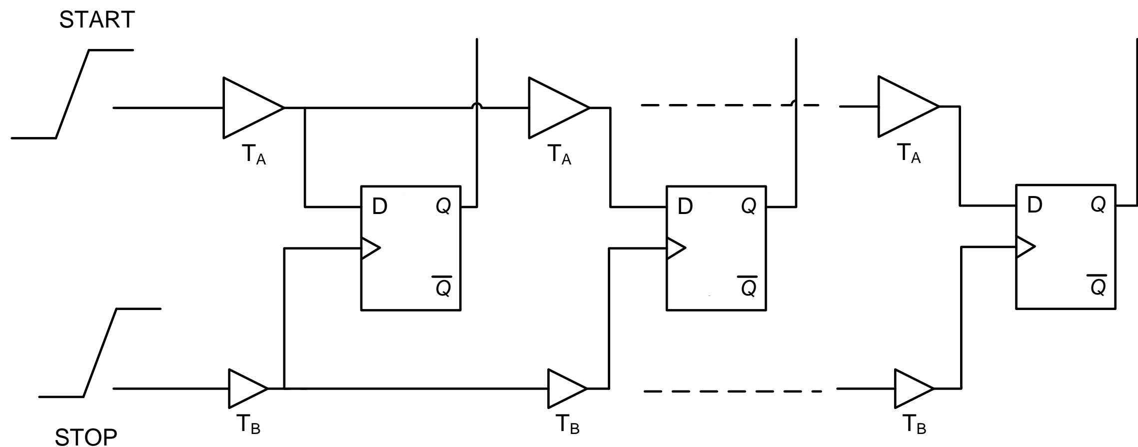

Figure 2.20: Block diagram of VDL.

2.6.2 Vernier Oscillator (VO) [6, 10]

The VO design consists of two oscillators, two edge detectors, a phase detector and two counters, as shown in Figure 2.22. Each oscillator has a different period where the resolution of the measurement is determined by the difference between the two periods. Assuming, the period of osc1 (T_1) is greater than the period of osc2 (T_2), then, the resolution (T_r) is equal to ($T_1 - T_2$). The two signals under test are applied to the inputs of the two edge detectors. The output of the edge detector turns to logic high as soon as the rising edge of the input signal arrives. When the outputs of the edge detectors go to a logic high, osc1 and osc2 are activated. While osc1 is slower than osc2 by T_r, the difference between the two oscillator signal rising edges is (T_r+ΔT_{input}), ΔT_{input} is the time difference between the two input signals. Now, the two counters are started counting the cycles of both oscillators whilst in each cycle, the rising edges of osc1 and osc2 are compared by a phase detector. As soon as both oscillators' rising edges coincide, the phase detector output is turned to a logic high and the measurement is reset. The stored values in the both counters (N_1 and N_2) are used to calculate the input time different using Equation (9) [10].

$$\Delta T_{input} = (N_1\text{-}1) \cdot T_1 - (N_2 - 1) \cdot T_2 \text{ --- } (2.7)$$

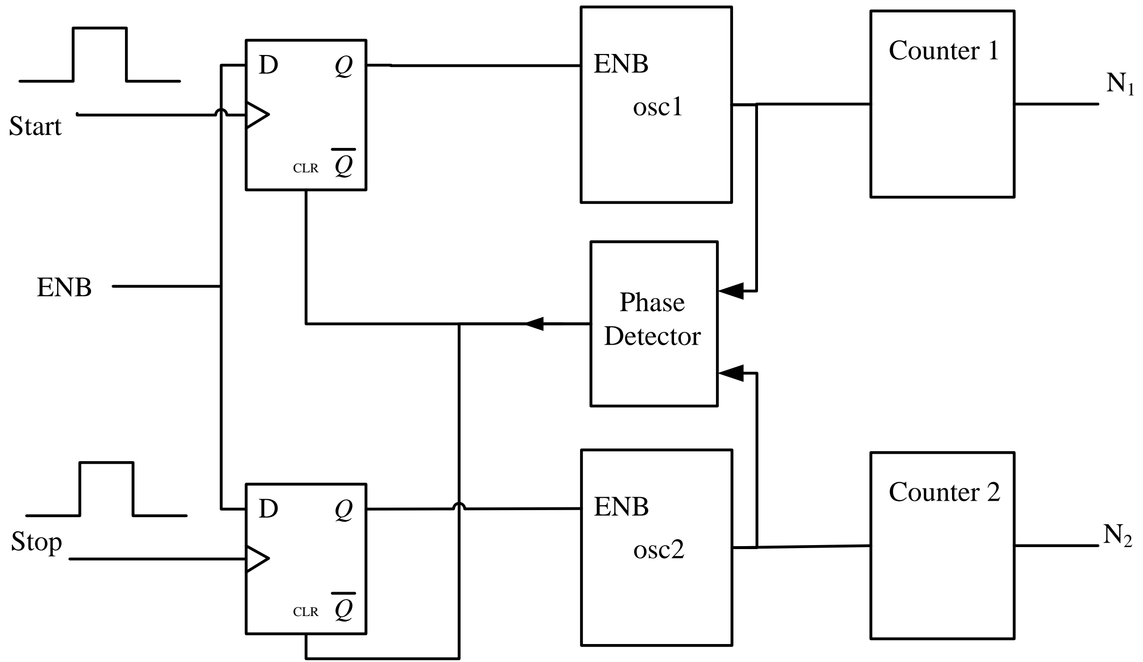

Figure 2.21: Time measurement using VO [10].

The main disadvantage of this system is the repetition of counting the oscillators' cycles which leads to a long measurement time. The time required for one measurement can be calculated using Equation (10).

$$\text{Time required for one measurement} = N \cdot T_2 \text{ --- } (2.8)$$

From Equation (10), the measurement time can be reduced by increasing the oscillators' frequencies. However, increasing the frequencies to very high values, the oscillators may suffer instability, jitter, and be very susceptible to the effects of process, temperature and power supply variation.

2.7 The Combination of Coarse and Fine Delay Method [8]

In the VDL technique, the dynamic range depends on the number of cells and the measurement resolution, as shown in Equation (11).

$$\text{Measurement dynamic range} = \text{Number of cells x the resolution of one cell --- } (11)$$

The high resolution value, which is counted as an advantage, has a direct impact on reducing the dynamic range of the measurement. In addition, increasing the dynamic range by increasing the number of cells can result in an increase in area overhead. On

the other hand, the VO technique has a disadvantage of a long time measurement, as discussed in section 2.6.2.

Both the VDL and VO techniques show a large improvement on the dynamic range and measurement time, respectively, when a combination of coarse and fine delay lines are used, as explained below.

2.7.1 The Combination of Coarse and Fine Delay Line [8]

In this technique a combination of a simple tapped delay line with VDL are designed to form a wide dynamic range, the dynamic range was approximately 1200 ps, with a high resolution, 10 ps. As shown in Figure 2.23, the time difference between the two input test signals is measured in two steps. First, they are passed through a coarse delay line with a low resolution; in this step the two input signals are measured to an accuracy of a buffer delay. Then, as the two input signals are within one buffer delay or less of each other, they pass through a high resolution Vernier delay line. The result is calculated from both steps as follows:

$$\Delta T_{input} = N \cdot t_{buf} + n \cdot t_{HR} \text{ --- } (2.9)$$

Where, ΔT_{input} is the input time difference between the two test signals, N is the number of high DFFs in the coarse delay line, t_{buf} is the delay of a single buffer in the coarse delay line, n is the number of the high DFFs in the high resolution Vernier delay line and t_{HR} is its resolution.

The most important part of this technique is the method which is used to switch the measurement from the coarse to the fine VDLs, as shown in Figure 2.23. It is based on enabling the corresponding multiplexer using the output of the DFFs in the coarse VDL. The switching takes place after CLKA lags CLKB by two buffer delays based on Equation (13). Thus three buffers, which have the same delay value as the buffer delay in the coarse VDL, are placed in CLKB signal path to the fine VDL in order to maintain the equivalent time difference.

$$EN = Q_n \cdot Q_{n+1} \cdot \overline{Q_{n+2}} \text{ --- } (2.10)$$

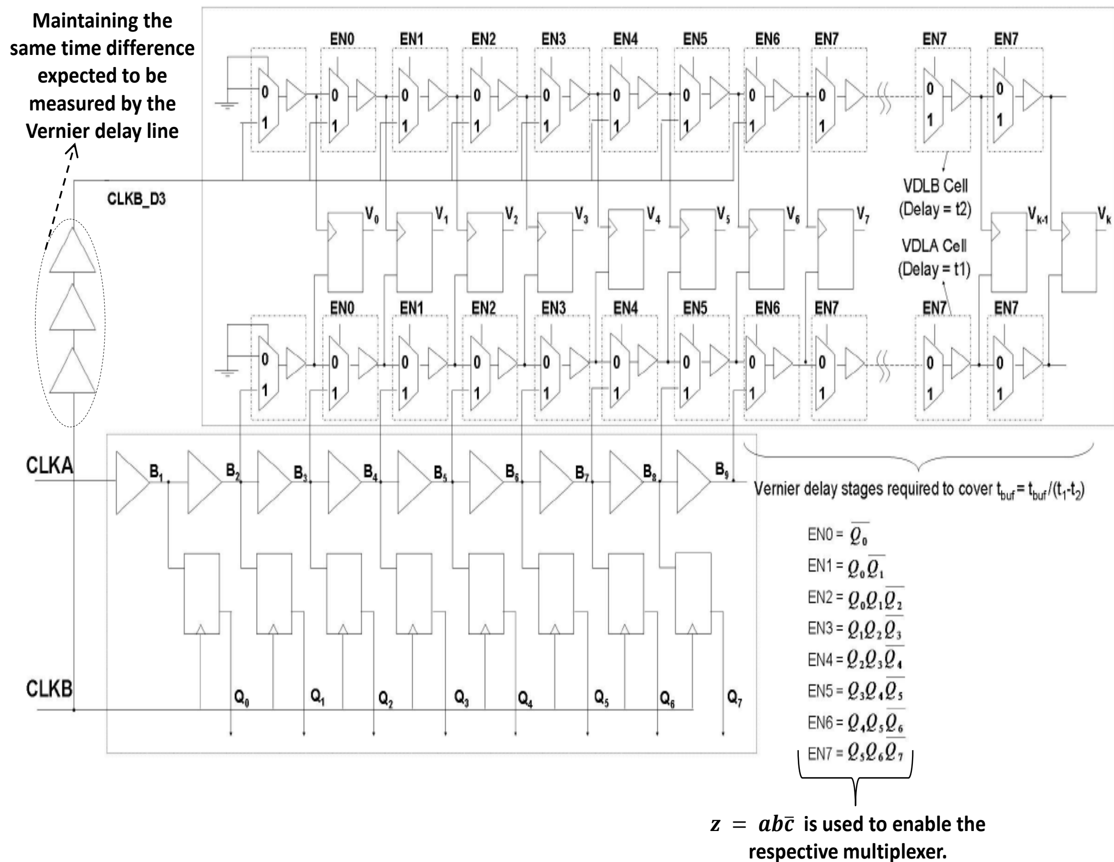

Figure 2.22: The combination of coarse and fine delay using tapped delay method with Vernier delay line [8].

2.7.2 The Combination of Coarse and Fine VO [7]

As described in section 2.5.2, the VO has the disadvantage of a long time measurement period. Nevertheless, this problem is solved using a combination a coarse and a fine VO method. In this technique the time measurement has been improved without any increase in the oscillators' frequencies. The method is divided into two steps, as shown in Figure 2.24. In the first step, the test signals is measured using coarse Vernier oscillator, low resolution VO (T_{LR}), and are measured to within the resolution value T_{LR}. When the difference between the signals becomes less than T_{LR}, the measurement is switched to be run through a very high resolution Vernier oscillator. There is a significant improvement in the time measurement using the dual resolution VO (DVO) compared with the single Vernier oscillator, as shown in Figure 2.25.

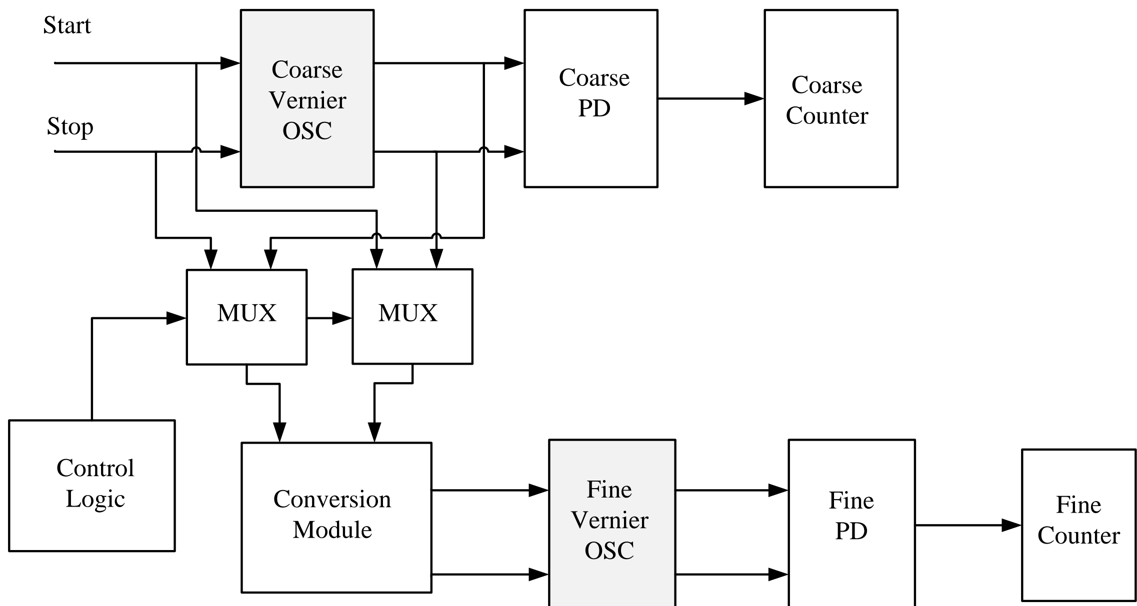

Figure 2.23: The combination of coarse and fine delay using VO [7].

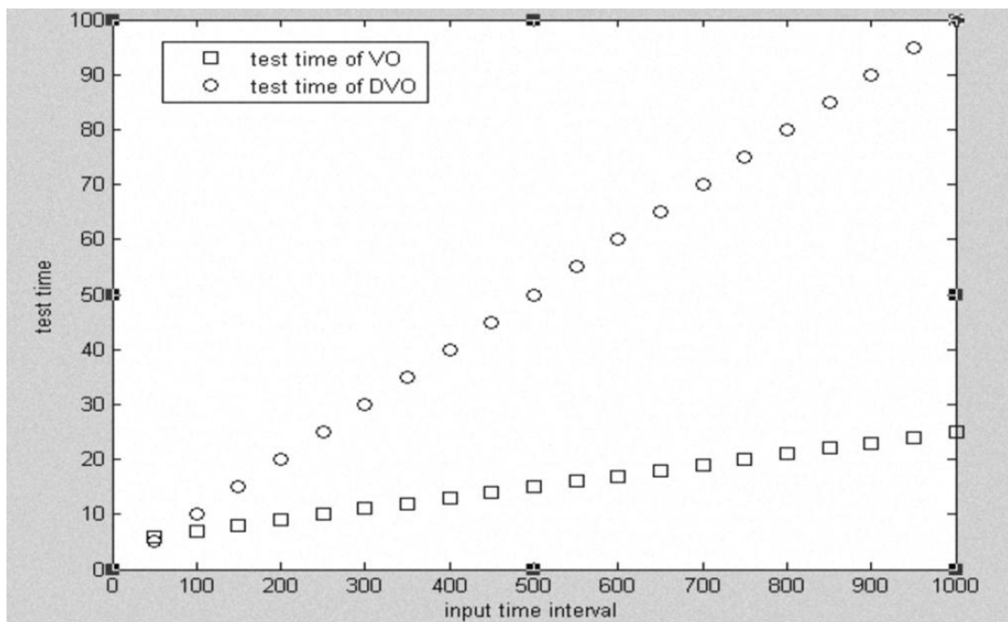

Figure 2.24: Comparison of the measurement speed between Dual resolution VO (DVO) and single resolution VO [7].

2.8 Implementation of Time Measurement Circuitry Using FPGAs [33-40]

All the previous designs for time measurement have been implemented successfully in Application-Specific Integrated Circuits (ASIC), these circuits face several implementation challenges when used in an FPGA particularly from the large routing delay mismatches. As the FPGA offers a greater flexibility, a lower cost for low volume and faster time-to-market, an FPGA implementation of a time-to-digital converter

(TDC) may be advantageous in several applications such as time-of-flight (TOF) experiments and in positron emission tomography (PET) [41]. However, TDC requires a very high resolution in order to be used in different applications such as delay, jitter, set-up and hold time measurements. Table 1 shows a comparison of different TDC designs which were implemented in an FPGA. It can be seen that the maximum resolution that can be reached is around 10 ps which is much lower than the ASIC implementation. In section 2.8.1, a design has been chosen and studied in order to understand the challenges facing the time measurement circuit implementation using FPGAs.

Reference	FPGA	Clock Frequency (MHz)	Resolution (ps)
[35]	QuicLogic	100	200
[42]	N/A	192	1302
[39]	ACEX 1K	35 / 70	400
[40]	Virtex	62.5	500
[37]	ACEX 1K	128	112.5
[37]	Virtex-II	96	69.5
[36]	Virtex-II	N / A	69.3
[38]	Cyclone-II	400	60
[33]	Spartan-3	125	75
[43]	Spartan-3	250	45
[34]	Virtex-5	300	17
[44]	Virtex-II Pro	100	50
[44]	Virtex-II Pro	100	25
[44]	Virtex-II Pro	100	10

Table 2.1: Comparison of different techniques to implement TDC in FPGS [44].

2.8.1 Process Variation Based TDC [36]

This method has similarities to the VDL technique except that no delay elements are used, as the difference in the delay between data and clock routing paths is used as delay elements, as shown in Figure 2.26. However, the clock path has a lower delay than the data path which is considered to be linked to the effects of the different loading on the DFF between the clock and data [36]. In order to implement this design in an FPGA all optimization, place and route software must be switched off. In addition the place and route should be done manually. This is because the optimization software adds a clock buffer which creates paths that make the connections amongst the cells in

parallel form. As a result the delays of the cells are not accumulated to have a series of delay cells forming a delay line.

Although the optimization option in the software is switched off and the place and route are done manually, the variation in the delay of the routing amongst the cells creates a challenge to have identical delays for each cell. Thus, XOR gates that are normally used in carry operations (XORCY) have been used to drive start and stop signals. The XORCY has a specific path with identical routing making the delay line predictable.

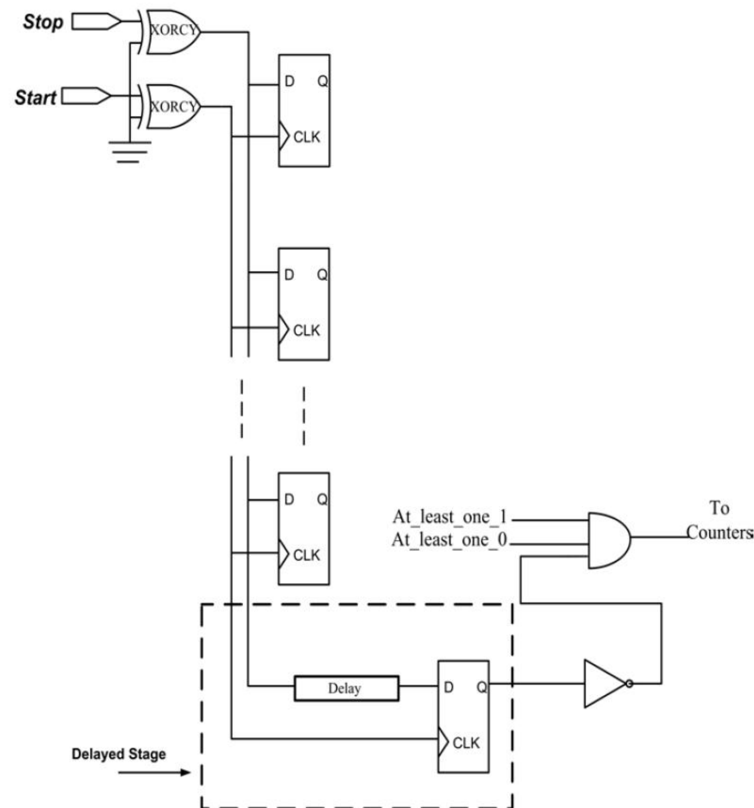

Figure 2.25: Process variation based TDC [36].

This method was implemented using Xilinx VirtexII 1000 FPGA with a 0.35 CMOS process [36] where a resolution of 62 ps was achieved. However, it has been repeated using a Virtex-4 Xilinx FPGA with 90 nm CMOS process while the resolution is improved to 14 ps. This improvement in resolution results from the higher speed of the Virtex-4 Xilinx FPGA. In addition, repeating this measurement in a very high speed FPGA such as Virtex-5 Xilinx FPGA with 65 nm CMOS process provides a higher resolution of about 9 ps. Nevertheless, from Figures 2.27 and 2.28, it is seen that the design suffers from the degradation in the linearity of the delay amongst the cells which leads to measurement error.

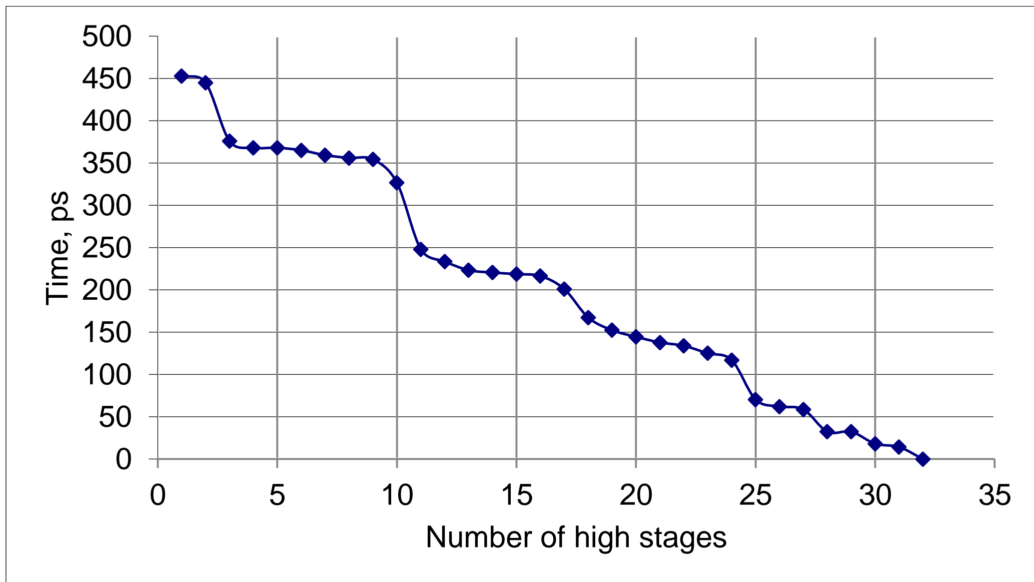

Figure 2.26: The value of each counter against time, Virtex-4.

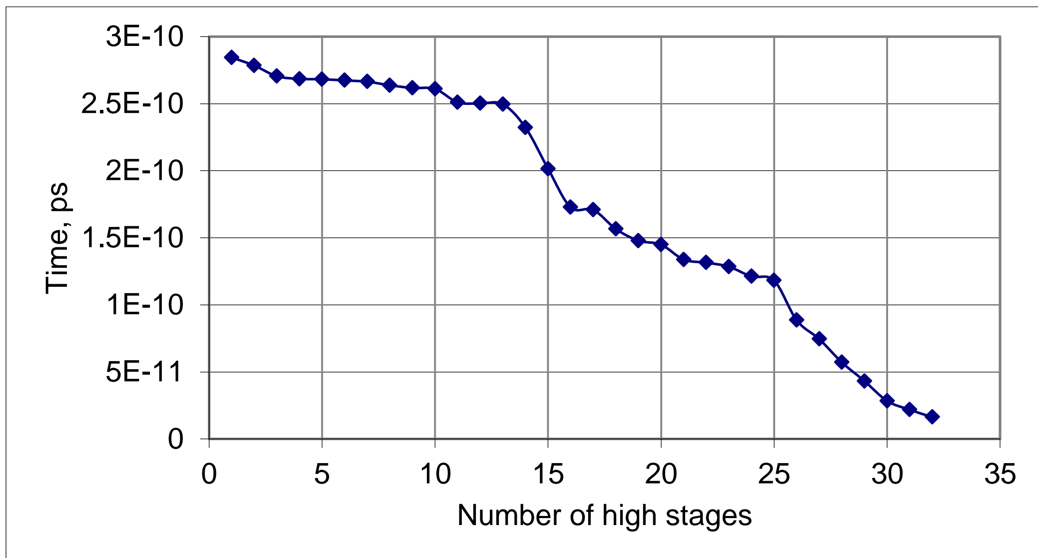

Figure 2.27: The value of each counter against time, Virtex-5.

2.9 Summary

In this chapter several time interval measurement methods are discussed highlighting the advantages and the disadvantages of each technique. These designs have a significant improvement in one or more, of the time measurement parameters. For example, despite the fact that the VDL method has a dynamic range limited by the number of cells in the delay lines, it has a significant advantage of a fine resolution. On the other hand, although VO method has a long time measurement period, it has a considerable dynamic range with sufficient resolution. It is clear that each of the time

measurement parameters is critically dependent upon the techniques used and hence is quite diverse. Finally, all techniques which are discussed in this chapter are summarized with their important features in Table 2.1, the shaded area on the table represents the analogue applications.

Methodology	Technique	Circuit type	Resolution	Dynamic range	Measurement time
Counter	Counter [10, 11].	Digital.	Low, limited to the value of the reference Clock frequency.	Wide.	Fast for a single measurement, slow if several measurements are averaged.
Time to voltage conversion (TVC)	TVC [10, 12-15].	Analog.	High resolution about 1 ps.	Depends on the linear region between the resulting voltage on the capacitor and input time interval.	Depends on the conversion time of the ADC.
Signal condition	Pulse stretching [10, 16].	Analog.	High resolution, about 1 ps.	Limited to the linearity region between the stretching factor and input time interval	Product of the input pulse width x stretching factor.
	Time difference amplifier [17-21].	Analog.	High Gain, about 20.	Wide range, about 400 ps.	----
		Digital.	High gain 20.	Narrow range, about 40 ps.	-----
Delay lines	Fixed delay line [22].	Digital.	Low resolution, limited to a single buffer delay.	Product of the resolution value and number of stages.	Depends on the buffer delay + propagation delay of DFF.
	Adjustable delay line [7, 9, 23-29].	Digital.	Very high resolution, a few femtoseconds can be achieved.	Depend on the used methodology.	Depends on the methodology used.
	Pulse shrinking [1, 2, 31, 32, 45].	Analog. Digital.	6 ps.	Wide, about 4500 ps.	Depends on the technique used for pulse shrinking.
Vernier	VDL [3-5].	Digital.	Very high, equal to the difference between two buffer delays, can reach 5 ps.	Product of the resolution value and number of stages.	Depends on the buffer delay + propagation delay of DFF.
	VO [6, 10].	Digital.	High, equal to the difference between two buffer delays.	Depends on the oscillators' periods.	Period of osc2 x number of cycles of osc2.
Combination of coarse and fine delay	Tapped delay line + vernier delay line [8].	Digital.	10 ps.	1200 ps.	Depends on the buffer delay + propagation delay of DFF.
	Coarse VO + Fine VO [7].	Digital.	1 ps.	Depends on the coarse oscillators' periods.	Faster than the single VO, see Figure 2.21.

Table 2.2: Time measurement techniques and their important features.

2.10 References

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Chapter 3

Time difference amplifier design with improved performance parameters

3.1 Introduction

In chapter 2, different time measurement techniques were outlined together with their measurement capabilities, in terms of resolution and dynamic range, limitations such as length of time to make the measurement were also highlighted. One of these generic techniques is the digital time difference amplifier whose principle has been used in several methods [1-4]. The time amplifier is used to increase a resolution of the time measurement by amplifying the time difference between the two input signals (ΔT_{input}) with a constant gain (G). However, the main limitation of this technique is the narrow dynamic input range, 40 ps, which has led to the lowering of time measurement range. A TDC [4] was designed incorporating time amplifiers attached to each cell in a delay line in order to overcome the limitation of the dynamic range of the time amplifier. However, this method incurs high area overhead and increases the complexity of the calibration process. In this Chapter, improvements on the performance parameters of the time amplifier are discussed. In this new development the dynamic input range is extended from 40 ps to 300 ps while the time amplifier circuit is designed to have an adjustable gain which can be controlled digitally.

Three techniques are used to improve the performance parameters of the time amplifier, namely, the unbalanced active capacitive load, unbalanced active charge pump load and NAND gate with added resistance. The unbalanced active capacitive load has the same performance as the buffer delay offset design (current method) [4], while the circuit area is reduced as there is no buffer delay circuitry. The unbalanced active charge pump load technique extends the time input difference range achieved by the buffer delay offset

technique from 40 ps to 70 ps. In addition, the buffer delay offset, unbalanced active capacitive load and unbalanced active charge pump load designs, show a large improvement in dynamic range by incorporating an additional series resistance into the pull-down network in the NAND gates. The buffer delay offset and unbalanced active capacitive load designs subsequently show an increase in the dynamic input range to about 180 ps whilst that for the unbalanced active charge pump load design is 300 ps.

The rest of this chapter is organized as follows. Section 3.2 describes earlier time amplifier design, followed by a description of the unbalanced active capacitive load design in Section 3.3. In Section 3.4, the unbalanced active charge pump load development is discussed. Subsequently, an explanation of the NAND gate with added resistance technique is given in Section 3.5. Section 3.6 discusses the programmable time amplifier, with a summary of the developments given in Section 3.7.

3.2 Analysis of the Time Difference Amplifier

The basic building block of the time amplifier is the MUTEX circuit, as discussed in section 2.3.2. The MUTEX is normally used to judge which of the two input signals arrives first and comprises an S-R latch and metastability filter, as shown in Figure 3.1. However, when the two input signals arrive to the latch with a very small time difference between them, the outputs of the latch go into a metastable state which is normally avoided. The metastability filter is used to resolve any metastability appearing at the outputs of the MUTEX. The filter circuit comprises two inverters, whose inputs also act as the power sources.

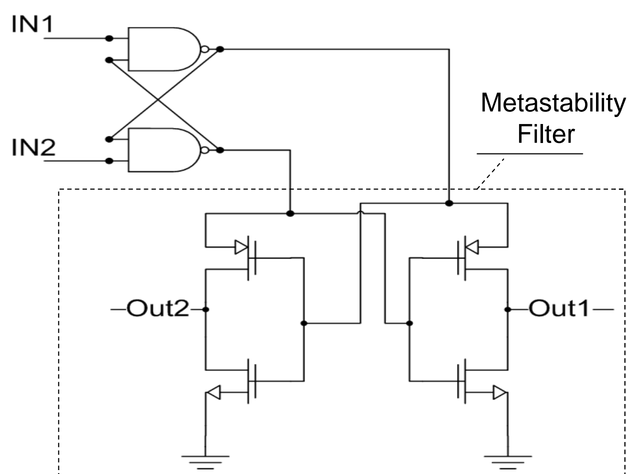

Figure 3.1: MUTEX circuit.

The metastable state in the latch circuit [5] creates a delay depending on the time difference between the input signals. Figure 3.2 and Equation (3.1) show the behaviour at the outputs of the latch during the metastability condition. The relationship between the input and output time difference can be obtained by taking the natural logarithm of Equation (3.1) as shown in Equations (3.2) and (3.3).

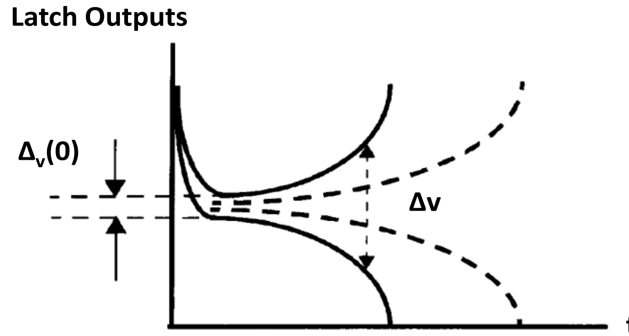

Figure 3.2: The behaviour of the output of the MUTEX circuit during metastability.

$$\Delta_v = \theta \cdot \Delta T_{input} \cdot e^{t/\tau} \text{ --- (3.1)}$$

Where Δ_v is the voltage output difference during metastability, θ is the conversion factor from time to initial voltage at the metastable nodes, ΔT_{input} is the time difference between the input signals and τ is MUTEX time constant (C/gm).

$$\ln(\Delta_v) = \ln(\theta) + \ln(\Delta T_{input}) + t/\tau \text{ --- (3.2)}$$

Then, the time output difference, t, is given as:

$$t = \tau \cdot \ln(\Delta_v / \theta) - \tau \cdot \ln(\Delta T_{input}) \text{ --- (3.3)}$$

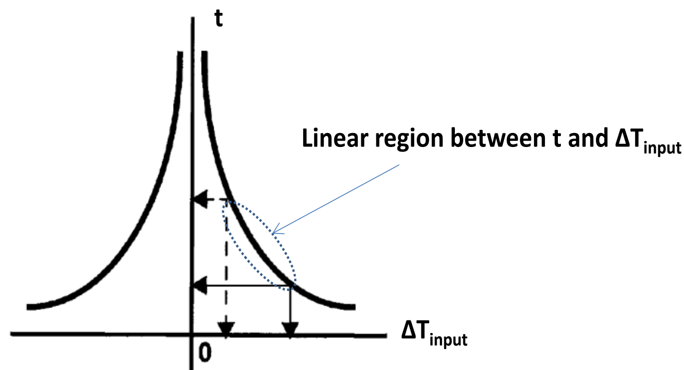

Figure 3.3: The relationship between the input and the output time differences of the latch circuit in the metastable state.

Figure 3.3 and Equation (3.3) represent the relationship between t and ΔT_{input} during a metastability condition for a balanced latch circuit, in which the latch has equal sized transistors in each NAND gate. It can be seen that the relationship between the input and the output time differences is linear over a certain range. Based on this relationship a time amplifier was designed [6] using two MUTEX circuits with opposite time offsets, as shown in Figure 3.4. The time offset (T_{offset}) of the unbalanced MUTEX can be adjusted by increasing or decreasing transistor widths. The first MUTEX of the time amplifier has a positive time offset where as the second has a negative time offset. The equations of the two MUTEX circuits with opposite time offset are given in Equations (3.4 and (3.5).

$$t_1 = \tau \cdot \ln(\Delta_v / \theta) - \tau \cdot \ln(\Delta T_{input} + T_{offset}) \text{ --- } (3.4)$$

$$t_2 = \tau \cdot \ln(\Delta_v / \theta) - \tau \cdot \ln(\Delta T_{input} - T_{offset}) \text{ --- } (3.5)$$

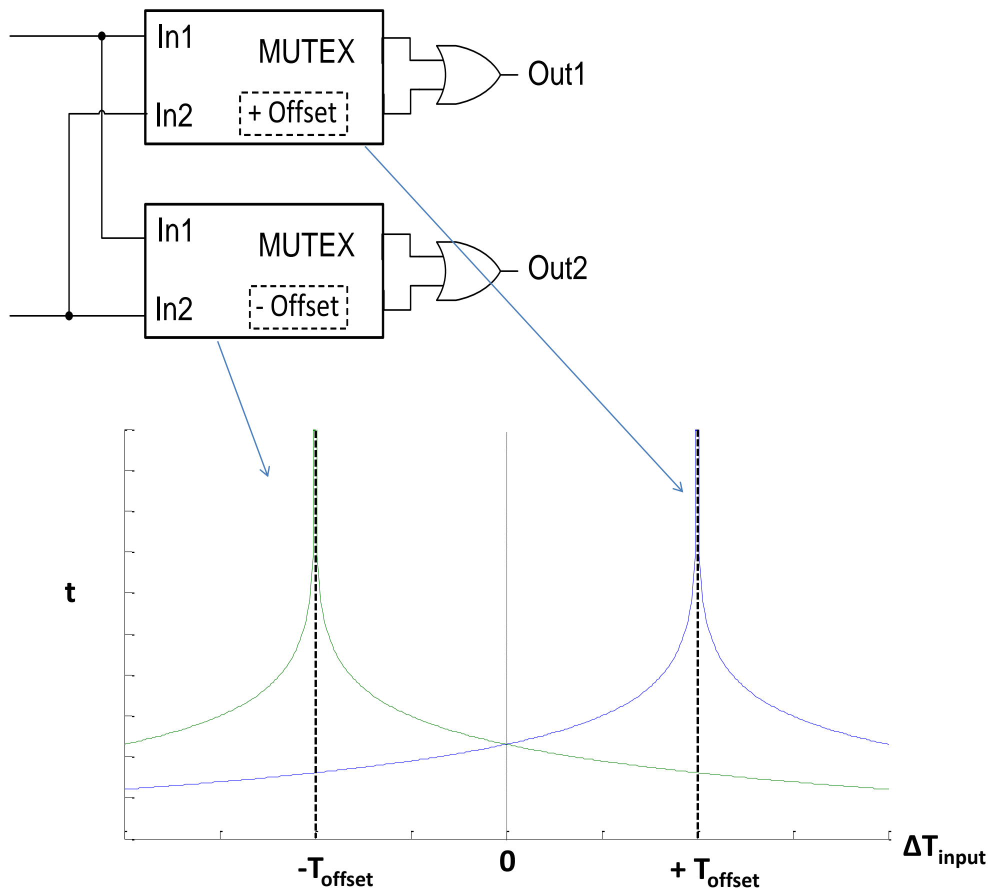

Figure 3.4: The plot of equations (3.4) and (3.5).

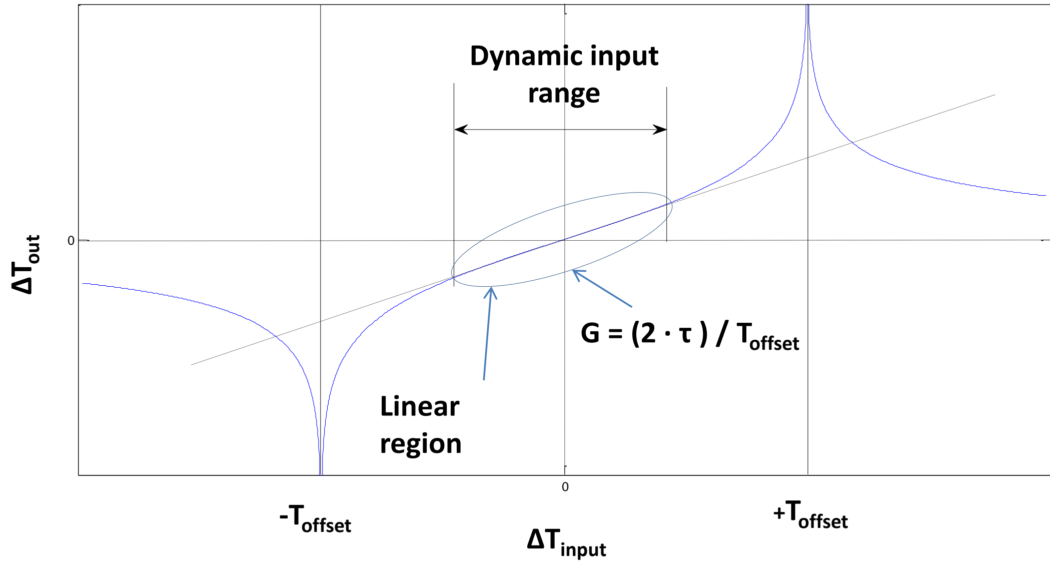

Figure 3.5: The plot of Equation (3.6) showing the linearity region around zero.

From Equations (3.4) and (3.5), it is possible to calculate the time difference output of the combination of the two MUTEXes with opposite offsets as shown below:

$$\Delta T_{out} = t_1 - t_2 = \tau \cdot [\ \ln(\Delta T_{input} - T_{offset}) - \ln(\Delta T_{input} + T_{offset})] \text{ --- (3.6)}$$

The plot of Equation (3.6) is shown in Figure 3.5 which demonstrates that the linear region of the amplification occurs around the zero. The gradient of the curve is calculated at $\Delta T_{input} = 0$ in order to determine the amplification gain at this region, as shown below. A variation of 10% in the gain is taken in this thesis as standard for acceptable variation in the linearity. This is calculated as 10% variation from extrapolated line through tangent at $\Delta T_{input} = 0$, as shown in Figure 3.5. Thus the dynamic range is from $\Delta T_{input} = 0$ to x, where x is the value of ΔT_{input} which has a gain value different than the one in $\Delta T_{input} = 0$ by 10%.

$$\frac{d\Delta T_{out}}{d\Delta T_{input}} = \tau \cdot \left[\frac{1}{\Delta T_{input} - T_{offset}} - \frac{1}{\Delta T_{input} + T_{offset}} \right] \text{ --- (3.7)}$$

$$\left. \frac{d\Delta T_{out}}{d\Delta T_{input}} \right|_{\Delta T_{input} = 0} = G = \frac{2 \cdot \tau}{T_{offset}} \text{ , } \left(\tau = \frac{C}{g_m} \right) \text{ --- (3.8)}$$

An amplification of 10 with a dynamic input range of 30 ps was achieved when 0.6 μm CMOS technology was used [6]. The dynamic input range of the time amplifier is

referred to the range of the time input difference where the gain of the time amplifier is linear, as shown in Figure 3.5. Nevertheless, the dynamic input range was decreased to 6 ps with 0.18μm CMOS technology. It is clear that scaling down of the transistor dimensions affects the gain and the dynamic input range. This is because the amplification behavior depends on the value of capacitance and transcondutance of the NAND gates which are affected by scaling down the technology. The effect of the scaling down technology on the time amplifier is summarised in Equation (2.5) [1]. It can be concluded that the main challenge in using the variation in the transistor size, to create the time offset in MUTEX circuits, is the reduction in dynamic input range as the transistor technology is scaled down.

Techniques to improve the dynamic range of the time amplifier are outlined below.

3.2.1 Buffer Delay Offset Design

By considering Equations (7) and (8), the gain can be improved by increasing the capacitance value at the output of the NAND gate and reducing the transconductance of the all transistors in the NAND gate. However, T_{offset}, as shown in Figure 3.5, controls the dynamic input range, large T_{offset} leads to wide dynamic input range. An optimization in designing T_{offset} and C/g_m must be considered, as the amplification gain depends on the ratio between T_{offset} and C/g_m. Thus in the delay buffer offset design [4], an improvement on the gain and dynamic input range were achieved by adding more capacitance at the output of the NAND gate and creating a large time offset using two buffer delays, as shown in Figure 3.6. In this design, the time offset is fixed to a certain value equal to the buffer delay, while the capacitance value improves the gain, as shown in Figure 3.7

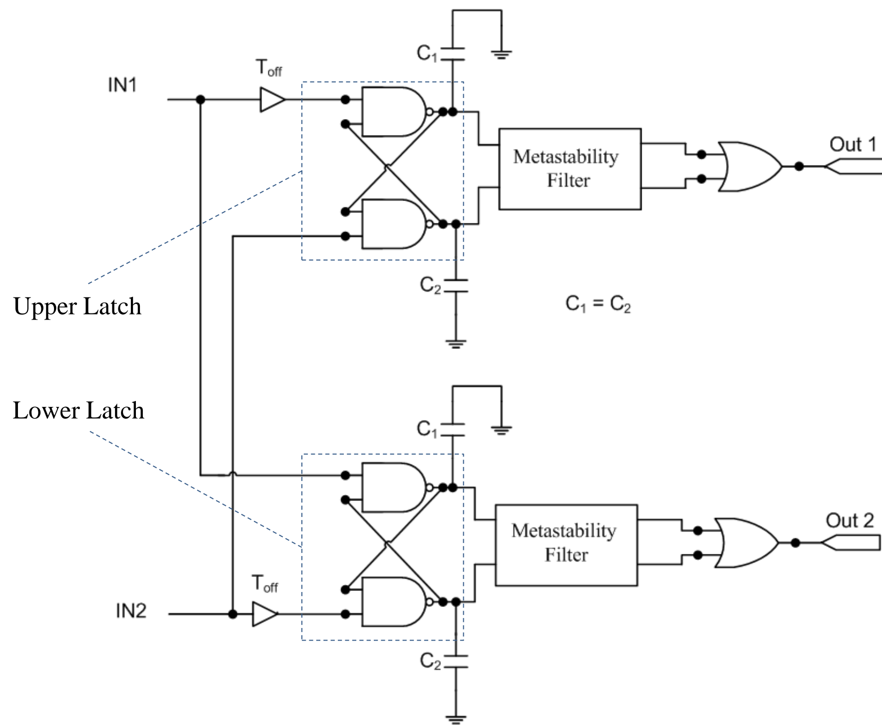

Figure 3.6: Time amplifier, buffer delay offset design [4].

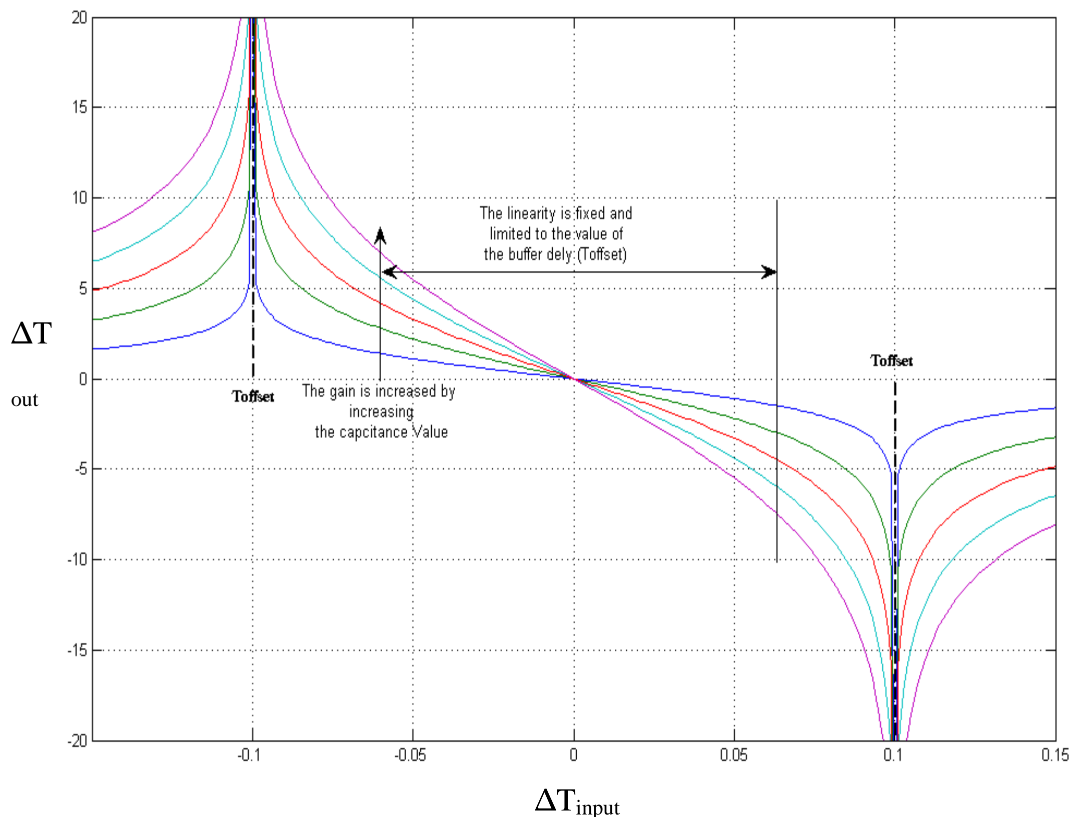

Figure 3.7: The effect of changing the capacitance value on the gain and the dynamic input range.

The analysis of the buffer delay offset design: Since the time amplifier circuit has two symmetric sides, as shown in Figure 3.6, only the upper latch is analysed. By

considering the upper latch circuit, shown in Figure 3.8, when no input signals are present, the transistors N_2, N_4, P_2, and P_3 are OFF while P_1 and P_4 are ON, the equivalent circuit at this moment is shown in Figure 3.9 (a). Both capacitances, which are attached to the NAND gate output, are charged to a value equal to (Vdd-V_{dsp}(sat)), where V_{dsp}(sat) is the drain to source voltage for the PMOS transistor in saturation mode. Assuming that IN1 leads IN2 and the time difference between them (t_d) is much smaller than the buffer delay T_{off}, which is added at the input to create a time offset, ($T_{off} >> t_d$). As a result, IN2 arrives at the upper latch first and the capacitance C_2 is discharged through N_4 and N_3 while P_4 is turned OFF. Although both inputs to $NAND_2$ are high, the output of $NAND_2$ is not logic 0 yet. This because the value of the charge left on the C_2 is sufficient to slow down the output switching to a low state.

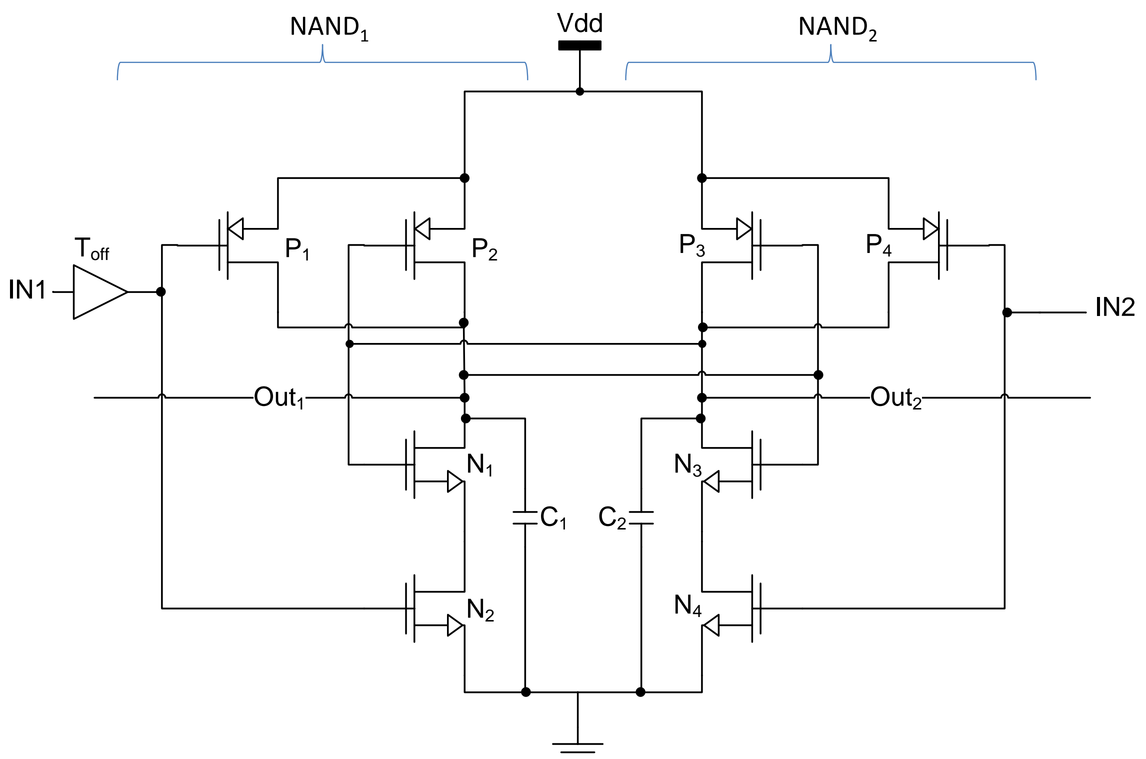

Figure 3.8: Upper latch circuit of TDA, buffer delay offset design.

When signal IN1 arrives at $NAND_1$, with time difference equal to ($T_{off} - t_d$) from the arrival of IN2, C_1 starts discharging through N_1 and N_2 while P_1 is turned OFF. At this time, P_2 remains OFF, since the output voltage of $NAND_2$ has not become zero and is equal to the value to the voltage left on C_2, that is V_{C2}, after the discharge time equal to ($T_{off} - t_d$). It can be construed that the metastability condition at the output of both NAND gates depends on the discharging of C_2 and C_1. In addition the value of the delay T_{off} has a direct impact on the gain, as it controls the difference between the discharge

time between C_2 and C_1. For example, if T_{off} is increased, the capacitance C_2 is discharged more before C_1 starts discharging while the gain becomes lower, as the amount of charge on the capacitance C_2 is not enough to hold the $NAND_2$ output for long before becoming a logic 0. Figure 3.9 (b) shows the equivalent circuit when each capacitance starts discharging. Furthermore, during the discharge time, N_1 and N_3 act as variable resistors. The values of their resistances depend on the gate voltage (Vg) which are equal to the voltages remaining on the capacitances (V_{C1} controls Vg of N_3 while V_{C2} controls Vg of N_1). In addition, as C_1 and C_2 discharge through the resistances of N_1, N_2, N_3 and N_4, the size of these transistors affect the discharge time and hence the gain of the time amplifier. Thus reducing the transconductance of the NAND gates, by reducing their transistors width, would increase the gain, as the resistance of NMOS transistors of the NAND gates is increased.

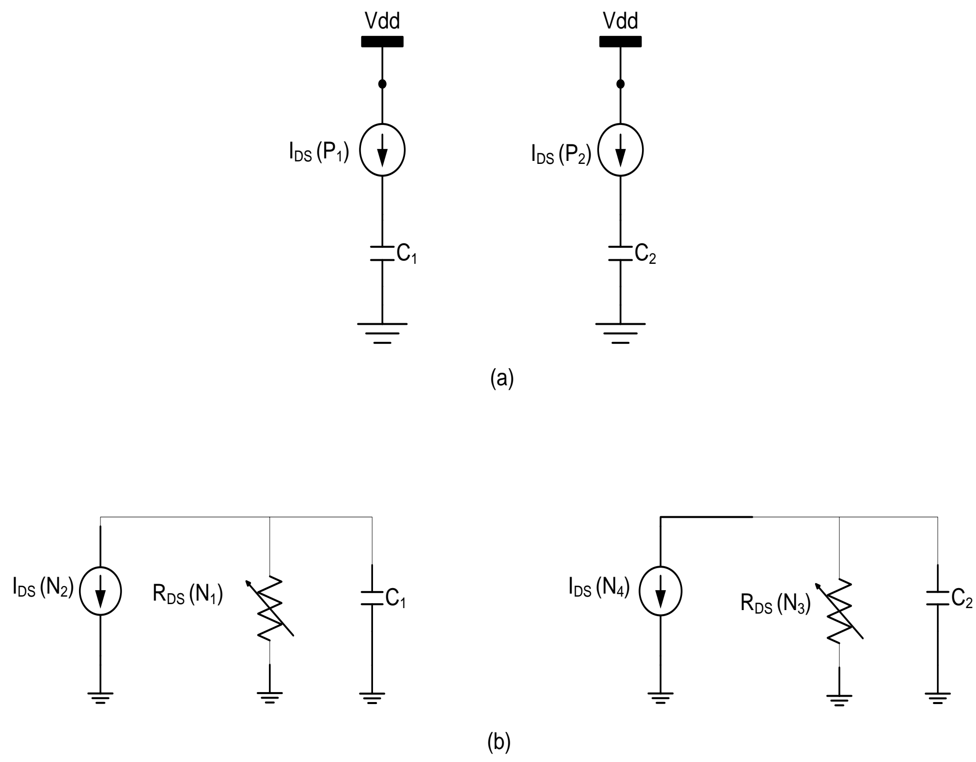

Figure 3.9: (a) The equivalent circuit of the upper latch before the arrival of IN1 and IN2. (b) The equivalent circuit when each capacitance starts discharging.

To conclude from the previous discussion, the key to making the gain higher and the amplification range wider is by increasing the amount of charge on both capacitances and making the discharge time longer; one way to achieve this goal is by adding more capacitance, reducing the transconductance of all transistors and creating the time offset using buffer delay [4]. However, implementing the time offset as a buffer delay may cause a mismatch in the time offset due to the effects of the process variation and for a

wide time input difference range a large delay is required which is achieved by either using large transistors or a chain of inverters. In addition, the time input difference range is still limited to about 40 ps. Other ways to improve the performance parameters of time amplifier which avoid the use of the buffer delay are discussed in the following sections.

3.3 Unbalanced Active Capacitive Load Design

As discussed in section 3.2.1, in the upper latch of the buffer delay offset design, shown in Figure 3.8, the input signal IN1 is delayed by T_{off} which causes C_2 to start discharging first, as $\Delta T_{input} << T_{off}$. The fixed time delay T_{off} creates a difference in charge between the C_1 and C_2 where the opposite scenario is happening in the lower latch. Figure 3.10 shows the discharge behaviour of C_1 and C_2 during the arrival of IN1 and IN2, for the upper latch which is shown in Figure 3.8. It is important to mention that all the circuits in this thesis were implemented in UMC 90nm technology; where the simulations were undertaken using Virtuoso Spectre Circuit Simulator in CADENCE suite of CAD tools. It can be seen C_2 discharges with current, I_{C2}, greater than the discharge current of C_1, I_{C1}. As described in section 3.2.1, V_{C1} controls Vg on N_3 while V_{C2} controls Vg on N_1 and hence the resistances of N_1 and N_3 are controlled by V_{C2} and V_{C1} respectively. However, from Figure 3.10, V_{C2} is lower than V_{C1}, as C_2 discharge before C_1, resulting in higher resistance in N_1 than that in N_3 which results in I_{C2} being larger than I_{C1}.

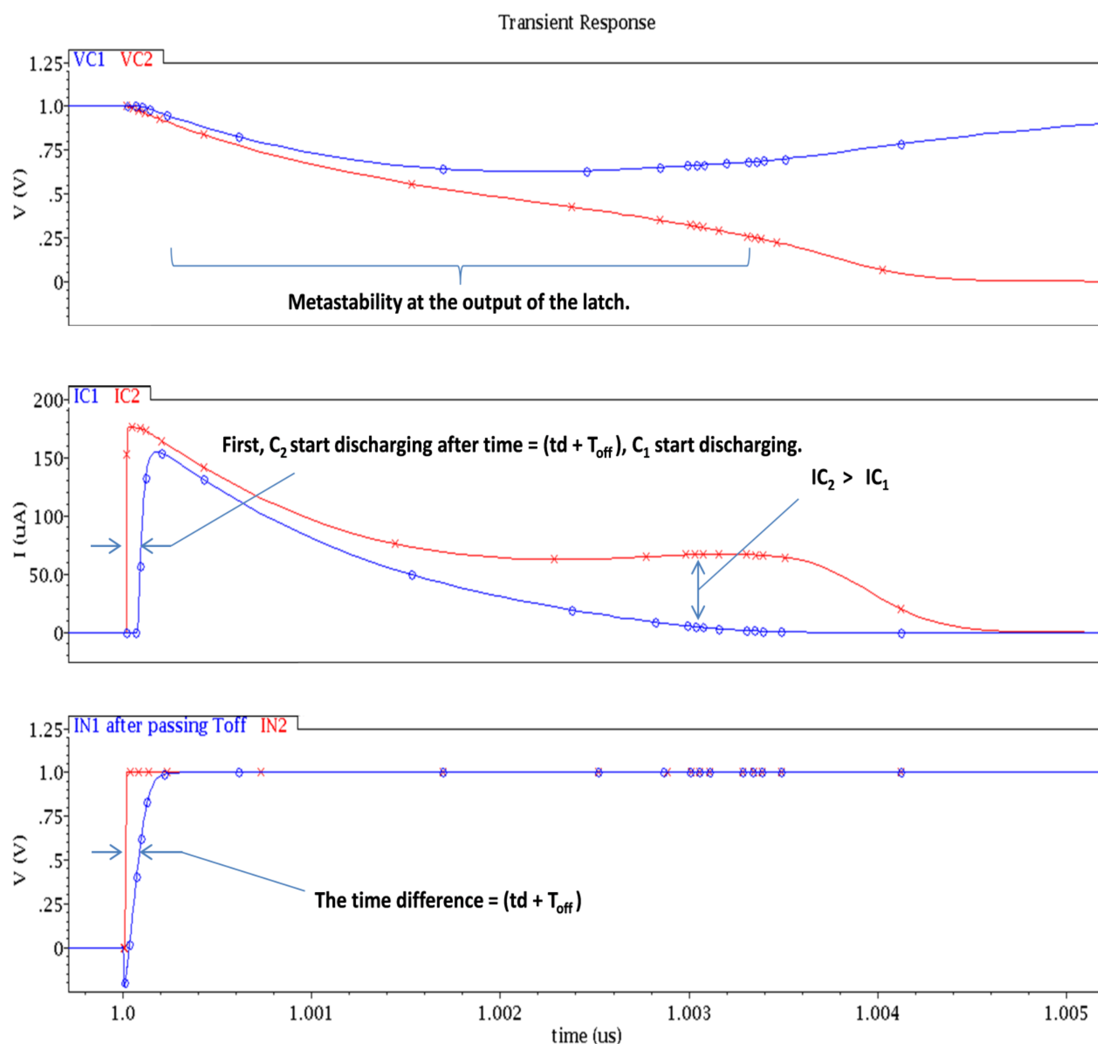

Figure 3.10: The behaviour of C_1 and C_2, and their discharge currents during the arrival of IN1 and IN2, for buffer delay offset design, using Virtuoso Spectre Circuit Simulator.

It can be construed that the difference in the stored charges in the two capacitances is the actual cause of the time offset in the latch. As a result, a time offset can be created in the latch by designing one capacitance to be larger than the other without adding a buffer delay while the same result of the buffer delay offset design is achieved, as shown in Figure 3.11. The time amplifier circuit using unbalanced active capacitive loads is shown in Figure 3.12. In addition, Figure 3.13 shows the performance of C_1 and C_2, in the active capacitive load design, and their discharge current during the arrival of IN1 and IN2. By comparing Figures 3.10 and 3.13, it can be recognised that the active capacitive load technique has a similar performance to the buffer delay offset technique.

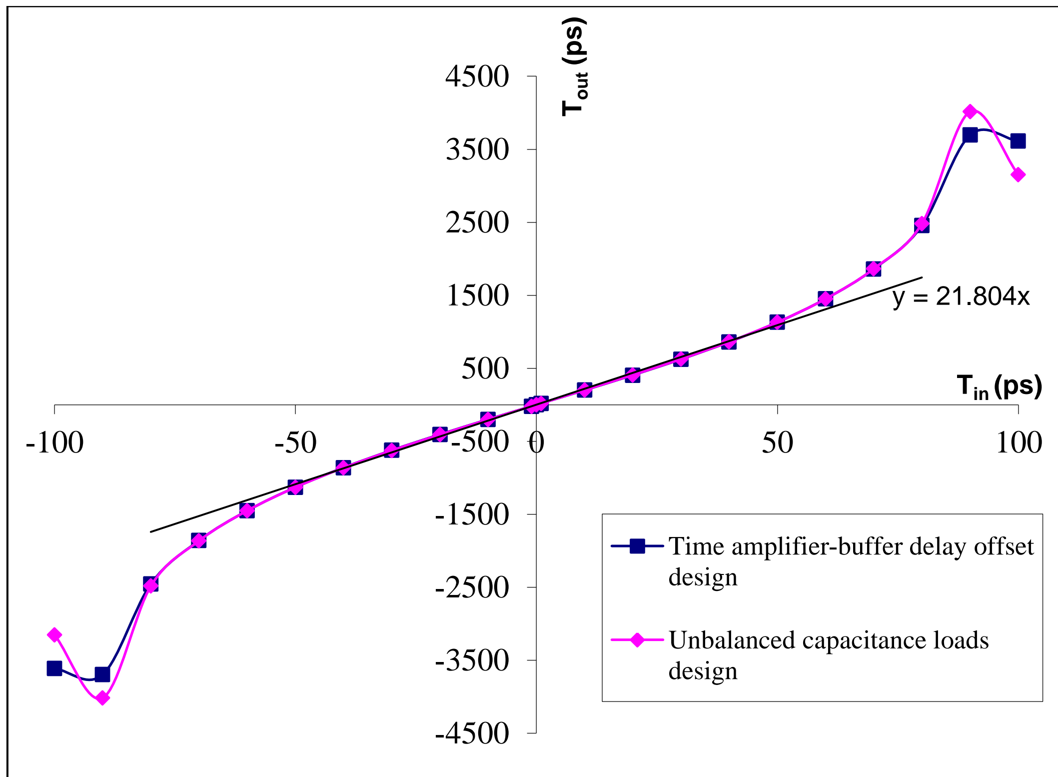

Figure 3.11: Time amplifier characteristics for buffer delay offset design and unbalanced active capacitive load design, using Virtuoso Spectre Circuit Simulator.

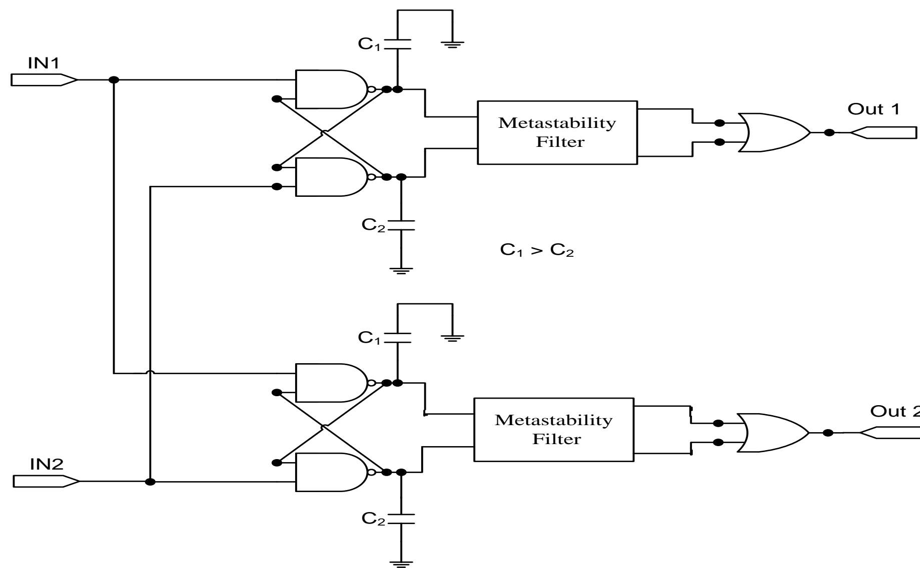

Figure 3.12: Time amplifier with unbalanced active capacitive loads design.

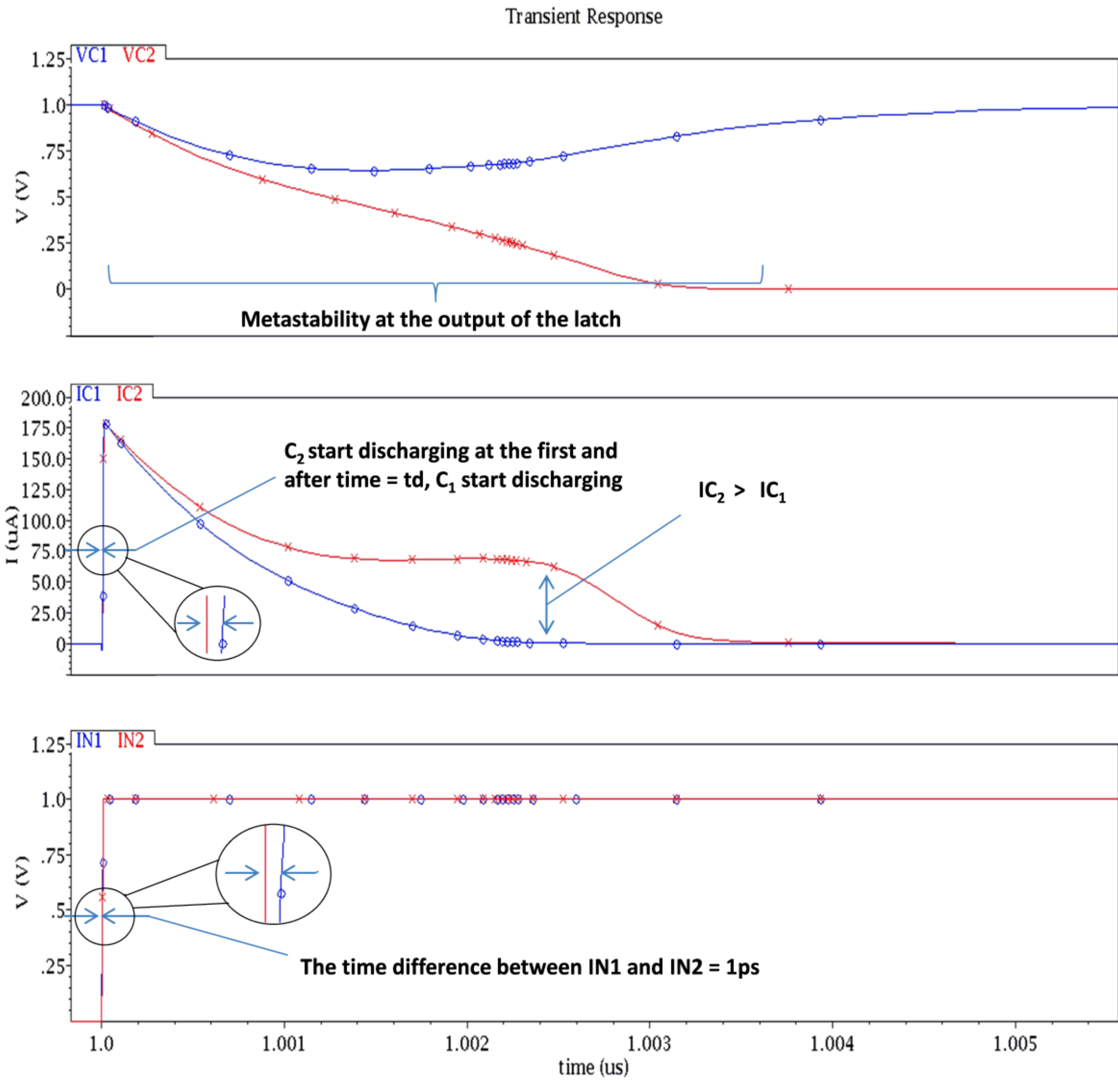

Figure 3.13: The behaviour of C_1 and C_2, and their discharge currents during the arrival of IN1 and IN2, for unbalance active capacitive load design, using Virtuoso Spectre Circuit Simulator.

The value of the gain in the unbalanced active capacitive load design is based on the difference between the value of C_1 and C_2, the smaller the difference the higher the gain. The large difference between C_1 and C_2, results in C_2 discharging much faster than C_1 which leads to a lower gain, as the amount of charge in the capacitance C_2 is not enough to hold the NAND output for long before becoming a logic 0. In other words, T_{offset} is created by the difference in the discharge time constant τ_1 and τ_2, which are the discharge time constants of C_1 and C_2 respectively. The large difference between C_1 and C_2 leads to large difference between τ_1 and τ_2 causing a large T_{offset}. From Equation (8), the gain is a function of T_{offset} and as it is increased the gain is decreased. Table 1 shows the relationship between the gain and the difference between the capacitance values.

C_1 (pF)	C_2 (pF)	G	Approximate Value of the Dynamic Input Range (ps)
0.42	0.4	71.83	10
0.42	0.38	34.03	22
0.42	0.36	21.46	35
0.42	0.34	15.24	50
0.42	0.32	11.54	65
0.42	0.3	9.107	80

Table 3.1: Gain and dynamic input range for the unbalanced active capacitive load design based on the difference between the value of C_1 and C_2.

The unbalanced active capacitive load design has the advantage of avoiding the use of the buffer delay as a time offset which reduces the circuit area overhead and avoids the effect of time offset mismatch caused by the buffer delay. However, the dynamic input range of the unbalanced active capacitive load design is still limited to 40 ps, similar to the buffer delay offset design.

3.4 Unbalanced Active Charge Pump Load Design

It is recognised that the key to making the gain higher and the dynamic input range wider are by increasing the amount of charge on both capacitances and creating a longer discharge time. Accordingly, the dynamic input range can be increased by nearly 75 %, from 40 ps to 70 ps, by substituting the capacitances with charge pump loads, as shown in Figure 3.14. This increase in dynamic input range results from the presence of Q_1 and Q_2. When no input signals have arrived, the capacitances of the charge pump loads are charging up; furthermore, with V_{DS} at a very low value Q_1 and Q_2 are in deep saturation turning them into a current sources for the capacitances, V_{DS} is the voltage drain to source for Q_1 and Q_2. However, during discharge, Q_1 and Q_2 act as resistances creating a longer discharge time which leads to an improvement in dynamic input range. In the unbalanced active charge pump load design, several ways can be used to create the time offset. The first is created by a difference between the sizes of capacitances of the active charge pump loads. The second by creating a difference between the channel lengths of Q_1 and Q_2, which effectively creates a difference between their resistances. Another way is to create the time offset and control the gain is by using different gate voltages on Q_1

and Q_2. However, these values of gate voltage require to be set to a specific constant value in order to achieve a constant gain. Therefor any variation in the value of the voltages, resulting from noise, variations in temperature, process and power supply voltage, affects the circuit stability and performance; hence this method will not be discussed further.

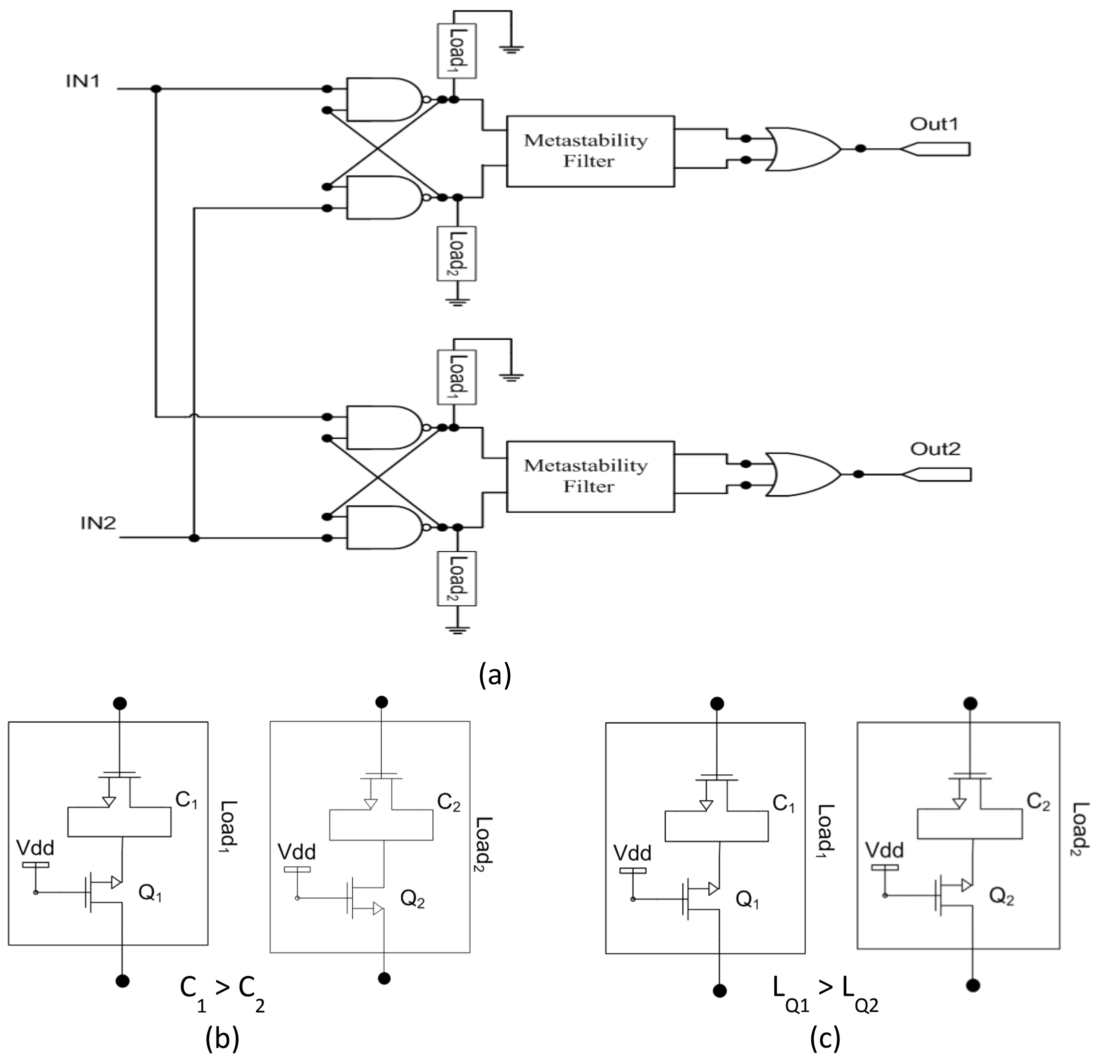

Figure 3.14: (a) Time amplifier using unbalanced active load design. Unbalanced active charge pump load using (b) $C_1 > C_2$ and (c) $L_{Q1} > L_{Q2}$.

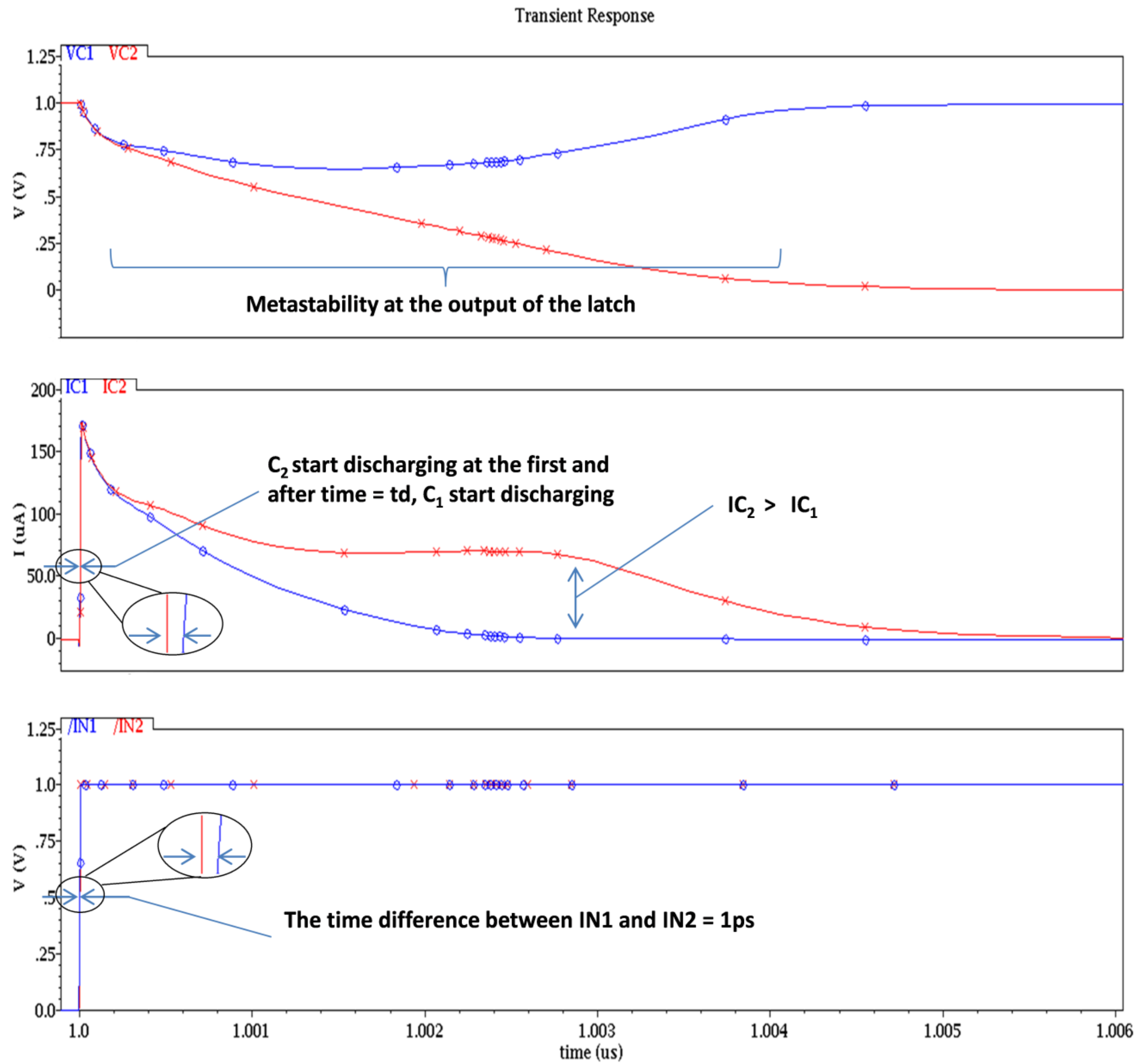

Figure 3.15: The behaviour of C_1 and C_2, and their discharge currents during the arrival of IN1 and IN2, for unbalance active charge pump load design, using Virtuoso Spectre Circuit Simulator.

Figure 3.15 shows the performance of $Load_1$ and $Load_2$ during the arrival of IN1 and IN2 when the difference between the sizes of capacitances is used to create the time offset in the unbalanced active charge pump loads design. From this figure the discharge time of the I_{C2}, about 5 ns, is longer than the discharge time of I_{C2} for the unbalanced active capacitive load design, Figure 3.13. This is because Q_1 and Q_2 act as resistances during the discharge period, as discussed before, creating a longer discharge time which leads to an improved the dynamic input range of nearly 75 % compared to the buffer delay offset and unbalanced active capacitance load designs, as shown in Figure 3.16.

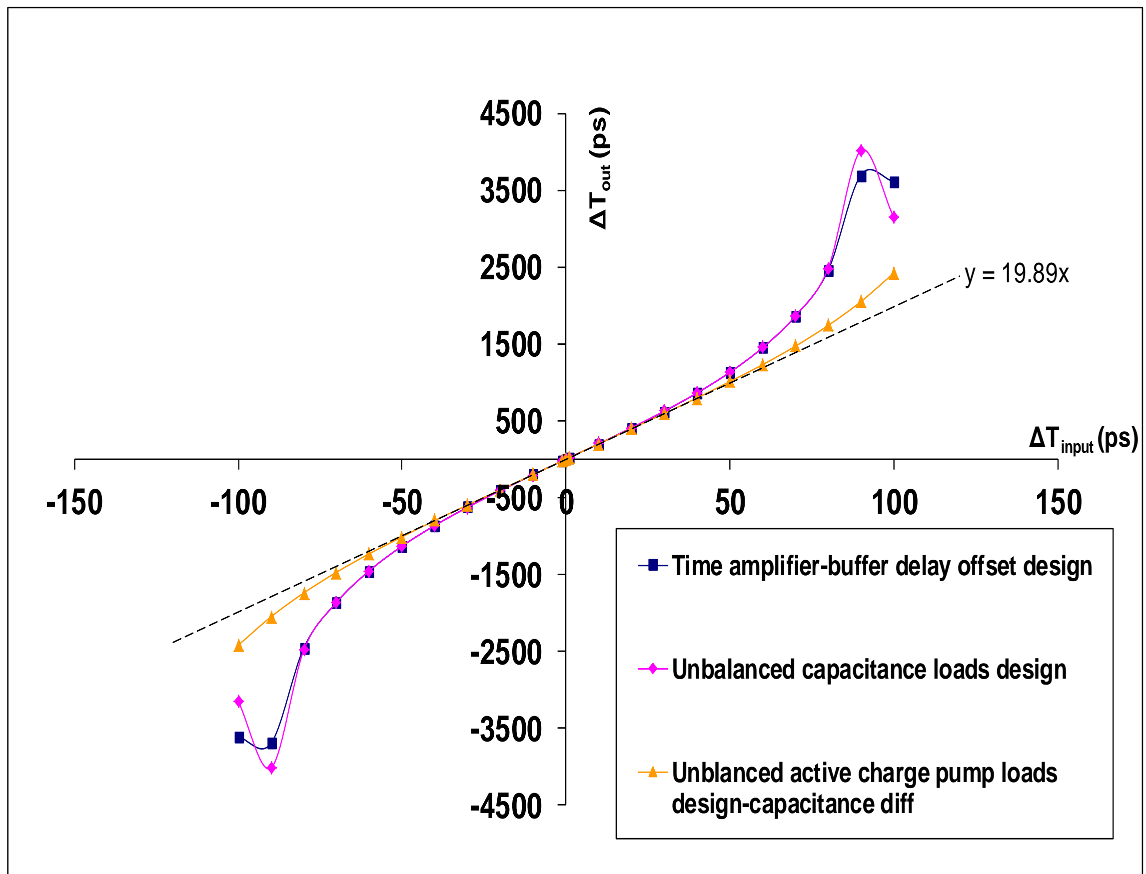

Figure 3.16: The characteristics for the three time amplifier designs, using Virtuoso Spectre Circuit Simulator.

Another way to create the time offset and control the gain is by designing Q_1 with a longer channel length, L_{Q1}, than the channel length of Q_2, L_{Q2}, while C_1 and C_2 are equal. The difference in size between Q_1 and Q_2 leads to a difference in the discharge time between C_1 and C_2. It can be seen from Figure 3.17, using different channel lengths between Q_1 and Q_2 has a similar result as using the difference in the capacitance values of C_1 and C_2. The gain value can be controlled by adjusting the difference between L_{Q1} and L_{Q2}, the smaller the difference the higher the gain. Figure 3.18 shows the relationship between the gain and the dynamic input range with respect to the difference in channel length between Q_1 and Q_2. However, the difference in size between C_1 and C_2 technique has a lower sensitivity to process variation than the difference between the channel lengths of Q_1 and Q_2, as discussed in Chapter 4.

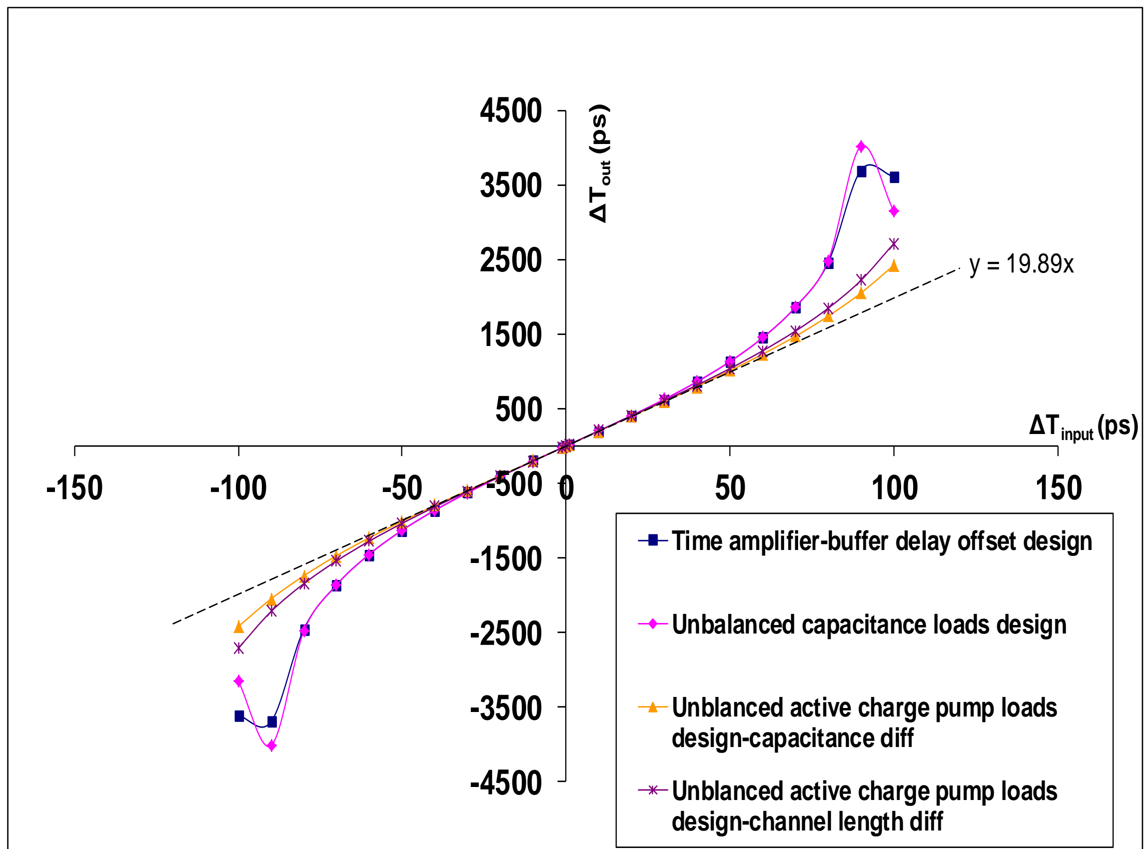

Figure 3.17: The characteristics for the four time amplifier designs, using Virtuoso Spectre Circuit Simulator.

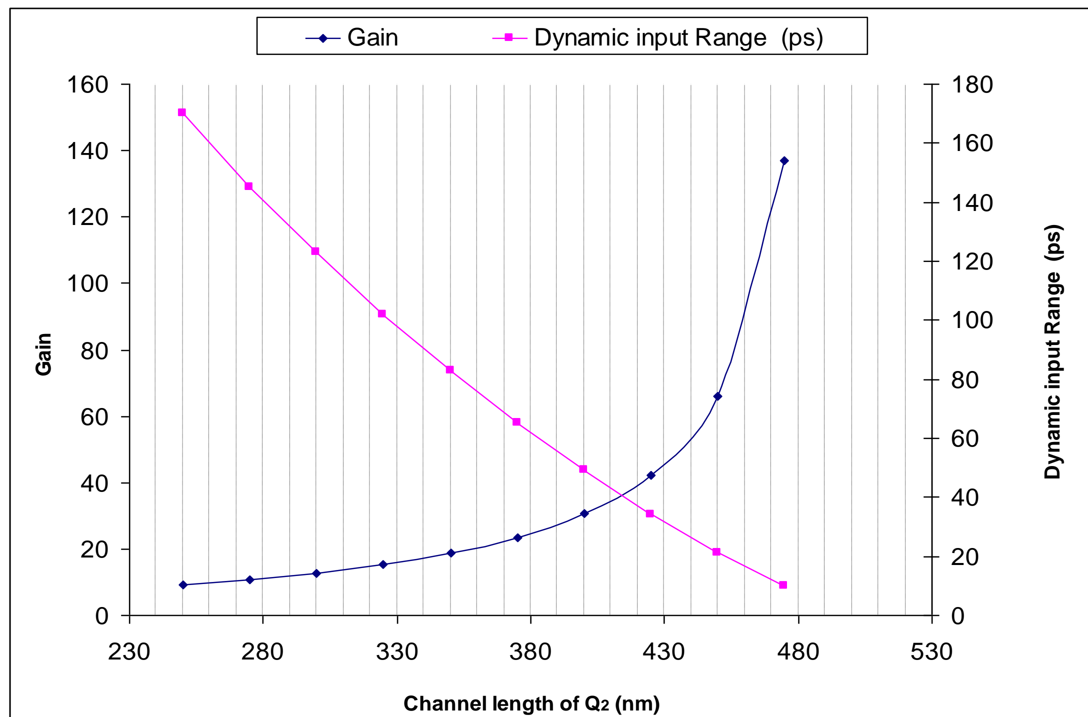

Figure 3.18: The amplification gain and range of the time amplifier with respect to the change in L_{Q2}, L_{Q1} is fixed to 0.5μm, using Virtuoso Spectre Circuit Simulator.

A further improvement on the results shown in Figure 3.17 can be achieved by reducing the transconductance of the NAND gate transistors and increasing the load capacitance. Nevertheless, reducing the transconductance by decreasing the size of the transistors close to the limitation of process technology leads to an increase in the effects of process variation. A different way to enhance the gain and dynamic range of time amplifier without further reduction in the transconductance of the NAND gates is presented in the following sections.

3.5 NAND Gate with Additional Resistance Technique

As previously discussed, the gain and dynamic input range of the time amplifier is improved by increasing MUTEX metastability. However, the metastability depends on the residual voltage on the capacitances during the discharge time. Therefore, the gain and dynamic input range was improved when the transconductance of the NAND gates is reduced resulting in a long discharge time. However, as mentioned in section 3.4, reducing the transconductance by decreasing the size of the transistor close to the limitation of process technology leads to an increase in the effects of process variation.

It is observed from Figure 3.8 that C_1 and C_2 discharge through the resistance of the NMOS transistors of the NAND gates; whilst the metastability and the dynamic input range of the time amplifier depends on the discharge time of C_1 and C_2. Consequently, the performance of the time amplifier could be improved if the discharge time for C_1 and C_2 could be prolonged. This goal can be achieved without reducing NAND gates transconductance, by adding more resistance in series in each NAND gate. This resistance can be either added between the NAND gates and voltage supply or ground, as shown in Figure 3.19. Adding resistance in the discharge path, between the NAND gate and ground, creates a long discharge time, as shown in Appendix A Figure A.1 and A.2 and hence improves the dynamic range. On the other hand adding resistance between the voltage supply and NAND gate increases the discharge time although this reduces the voltage on each capacitance. This is because the reduction in the capacitance voltage drive increases the resistance of the NMOS transistors in NAND gates resulting in a longer discharge time, as described in section 3.2.1, V_{C1} controls the resistance of N_3 while V_{C2} controls the resistance of N_1. All the previous designs, namely, delay buffer offset design, unbalanced active capacitive loads and unbalanced

charge pump loads, show a large enhancement in dynamic range using NAND gate with additional resistance technique, as discussed below.

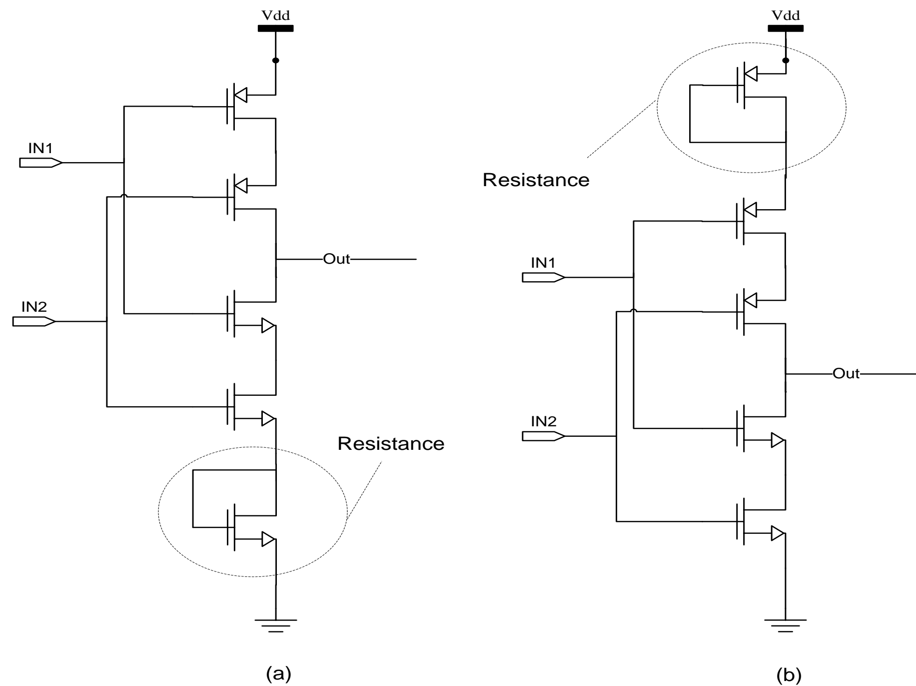

Figure 3.19: NAND gate with added resistance.

a) **Delay buffer offset design using NAND gate with added resistance:** When the delay offset design was implemented using NAND gates with added resistance, the gain was increased to large value. However, in order to undertake an objective comparison of the improvements to the dynamic input range of the various time amplifier configurations, it was decided to design each circuit with a fixed gain of 20; in this instance the buffer delays, T_{off}, had to be increased. As T_{off} is implemented using inverters, it is increased by reducing the size of the PMOS transistors and increasing the size of the NMOS transistors. By comparing Figure 3.10 and 3.20, it can be seen that there is a large increase in the discharge time of the buffer delay offset design when the NAND gates with added resistance in the discharge path are used, about 20 ns, while without using the added resistance technique the discharge time was about 4 ns. This increase in the discharge time leads to improvements in the dynamic input range from 40 ps to 180 ps, as shown in Figure 3.21. However, when the resistance is added between the voltage supply and the NAND gates there was a slight increase on the capacitances discharge time leading to a slight improvement on the dynamic range, about 70 ps, as shown in Figure 3.21. The improvement when the resistance is added between the voltage supply and the NAND gate is much lower than when placing a resistance in the discharge path,

that between the NAND gate and ground. This is because inserting a resistance between the voltage source and the NAND gates reduces the charge on both capacitances.

b) Unbalanced active capacitive load design using NAND gates with added resistance: There was a large improvement in the dynamic range for the unbalanced active capacitive load design when the resistance is added on the discharge path. Without using any added resistance, the dynamic range was 40 ps while when the resistance is added between the NAND gate and the ground the dynamic range was increased to 180 ps, as shown in Figure 3.22. On the other hand, placing the resistance between the voltage source and the NAND gate shows a slight increase on the dynamic range which is equal to 70 ps.

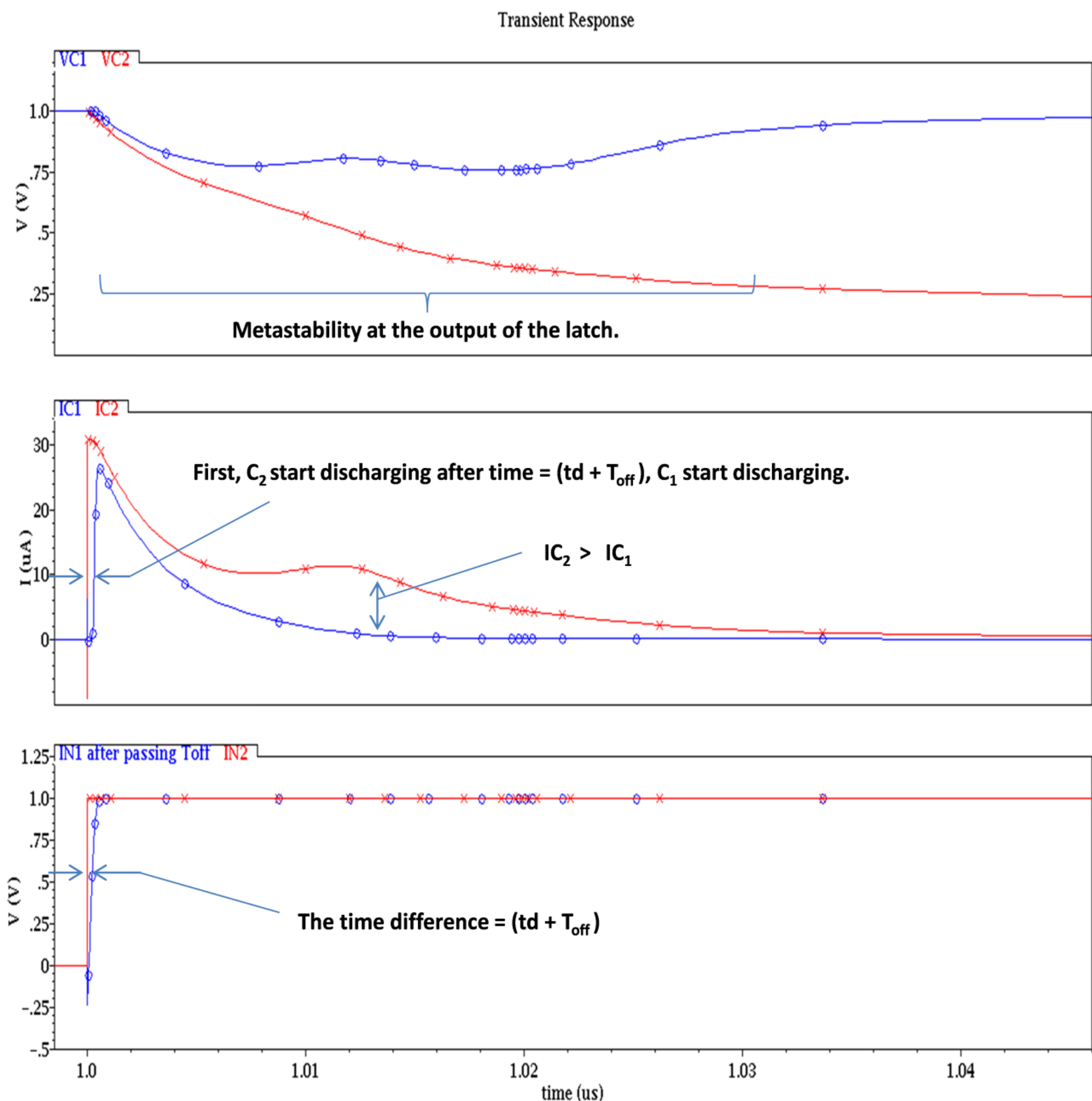

Figure 3.20: The behaviour of C_1 and C_2, and their discharge currents during the arrival of IN1 and IN2, for buffer delay offset design using a NAND gate with added resistance in the discharge path, using Virtuoso Spectre Circuit Simulator.

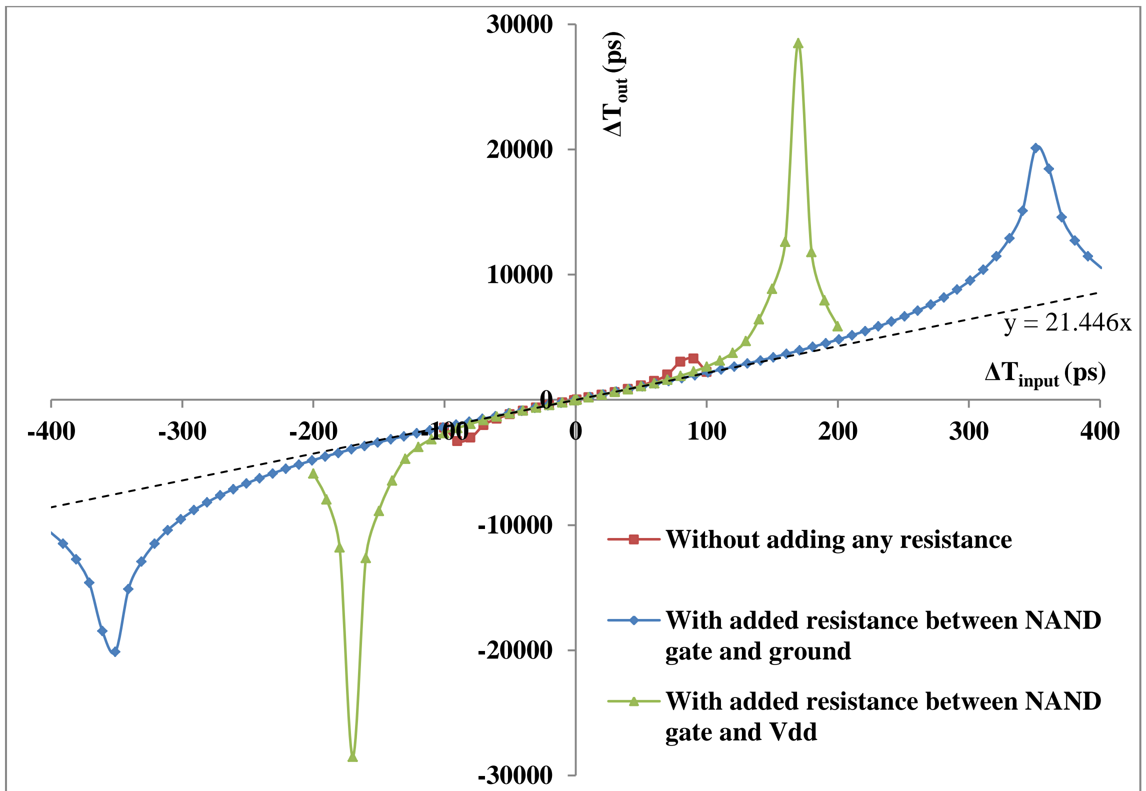

Figure 3.21: Time amplifier characteristics for the buffer delay offset with and without added resistance, using Virtuoso Spectre Circuit Simulator.

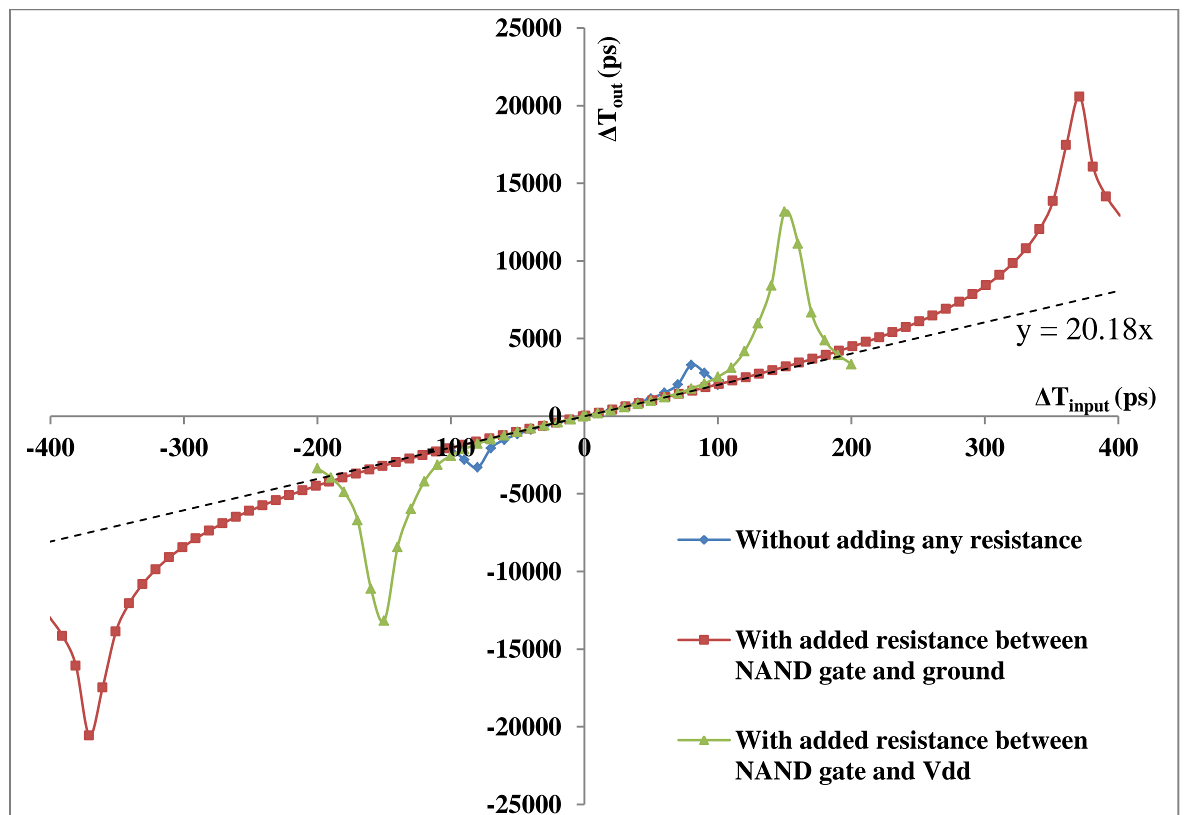

Figure 3.22: Time amplifier characteristics for the unbalanced active capacitive load with and without added resistance, using Virtuoso Spectre Circuit Simulator.

c) **Unbalanced active charge pump load design using NAND gates with added resistance:** The dynamic range without using any added resistance was 70 ps for the unbalanced active charge pump load technique, as shown in Figure 3.23, while when the resistance is added to the end of the pull down network of the NAND gate, the dynamic range increases to 300 ps. The improvement was, again, much lower when the resistance was placed between the voltage source and the NAND gate, the dynamic range being 120 ps in this instance.

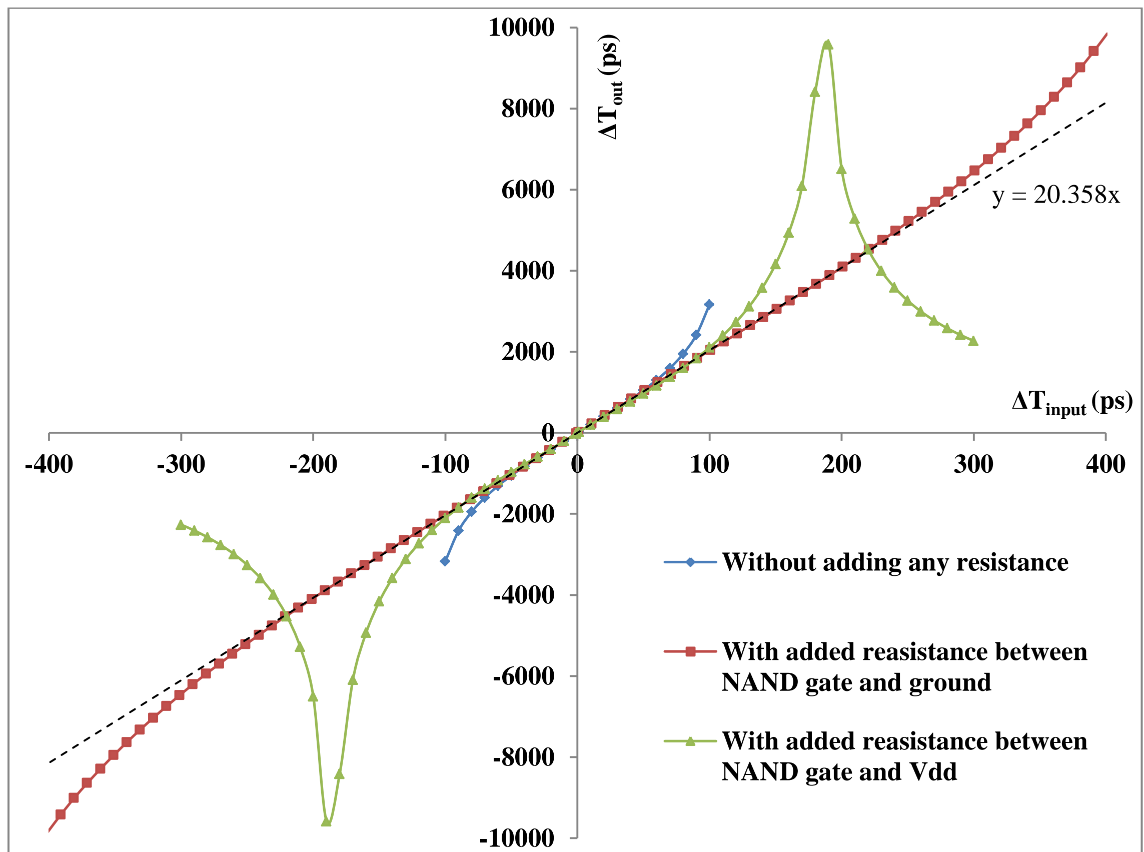

Figure 3.23: Time amplifier characteristics for the unbalanced active charge pump load with and without added resistance, using Virtuoso Spectre Circuit Simulator.

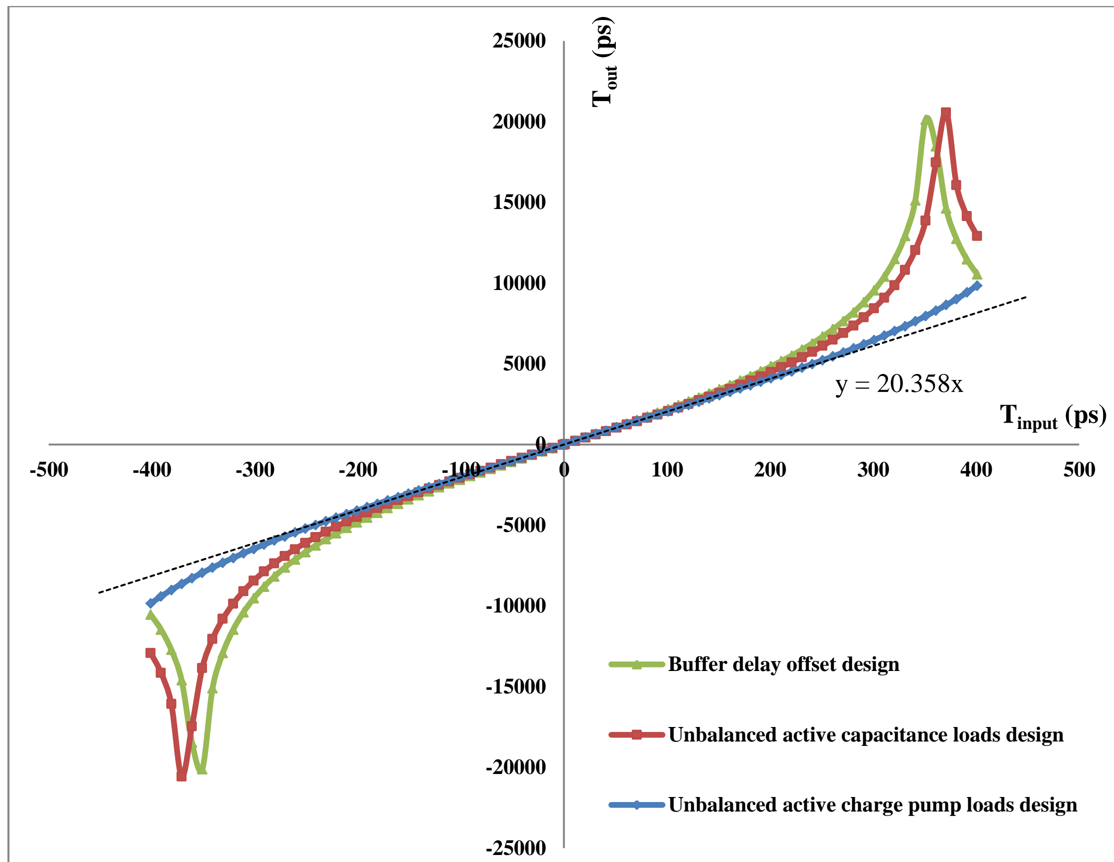

Figure 3.24: Time amplifier characteristics for three circuit implemented using NAND gate with added resistance, using Virtuoso Spectre Circuit Simulator.

Implementing delay buffer offset, unbalanced active capacitive load and unbalanced active charge pump load designs with additional resistance in the discharge path increases the dynamic range to large value. Figure 3.24 shows the largest development in the amplification range was achieved when a series resistance is added between the NAND gate and the ground in the time amplifier using unbalanced active charge pump load technique.

3.6 Programmable Time Amplifier

As previously discussed the time amplifier is mainly used to enhance the resolution of time measurements as it magnifies the time difference between the two input signals with a constant gain. In this work, the time amplifier is developed to have a programmable gain so that the resolution of a measurement can be adjusted to suit a given application. In sections 3.3, 3.4 and 3.5 the dynamic range of the time amplifier was increased from 40 ps to 300 ps which is sufficient to be used in several time measurement techniques, such as tapped delay line and VDL.

The programmable time amplifier is based on the unbalanced active charge pump load design implemented using NAND gates with additional resistance. As discussed in section 3.4, the gain of the unbalanced charge pump load circuit is designed by creating a difference between the capacitances of the active loads or the channel lengths between Q_1 and Q_2, as shown in Figure 3.14. However, in the programmable time amplifier, another method is used to form the difference between the active loads which is based on fixing load1 and being able to adjust the charge and discharge current of load2, as shown in Figure 3.25. The charge and discharge current of load2 is adjusted through Q_2, where the drain current is controlled digitally, as shown in Figure 3.25, by either using four transistors with different widths, as shown in Figure 3.25 (b), or by using sixteen transistors with the same width, Figure 3.25 (c), where these transistors work as a resistance which can be switched in or out of the circuit digitally in order to adjust the gate voltage on Q_2 and hence the discharge current. The result of the relationship between the gain and the control bits for both methods are shown in Figure 3.26 and 3.27. The step of the gain was designed to be approximately 7.5 ps and 8 ps using four transistors with different widths or using sixteen transistors with the same width respectively; these steps can be designed to be smaller or larger by adjusting the size of the transistors.

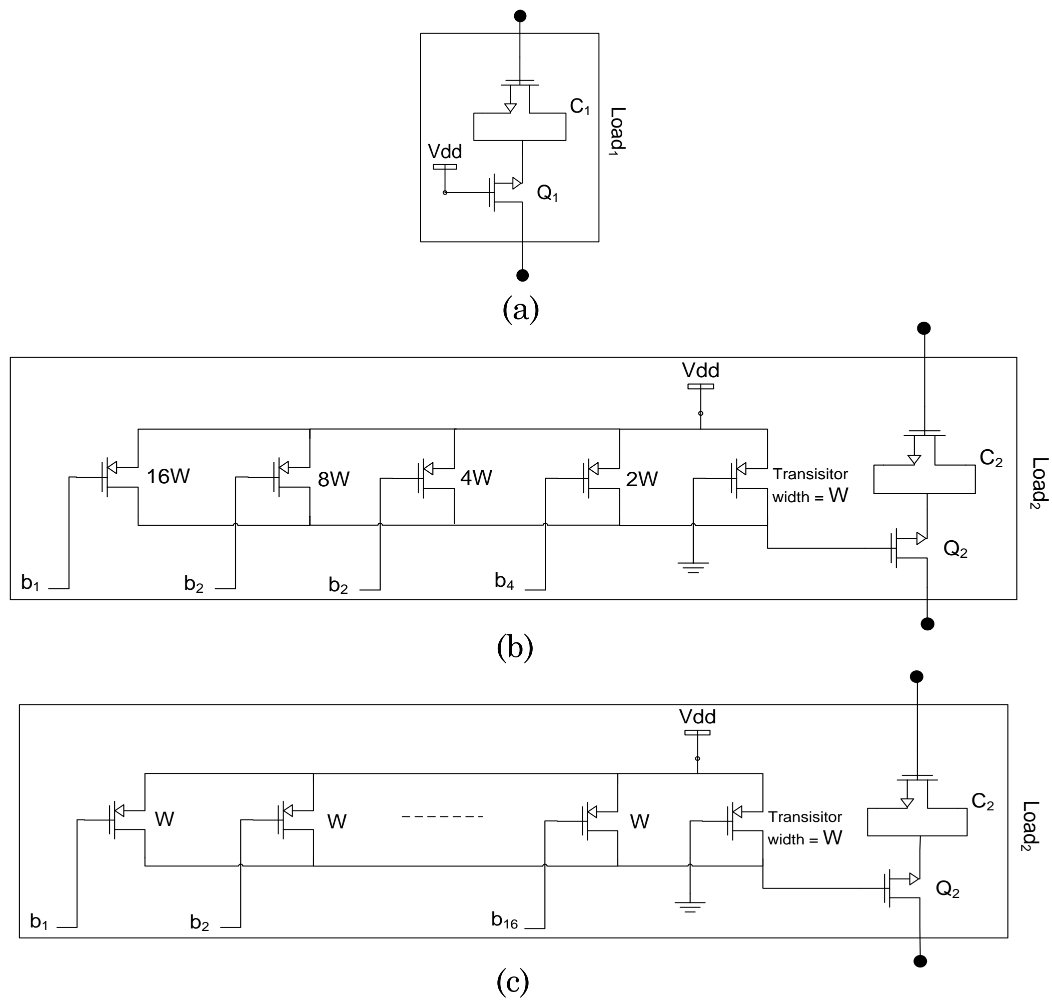

Figure 3.25: Programmable time amplifier active loads.

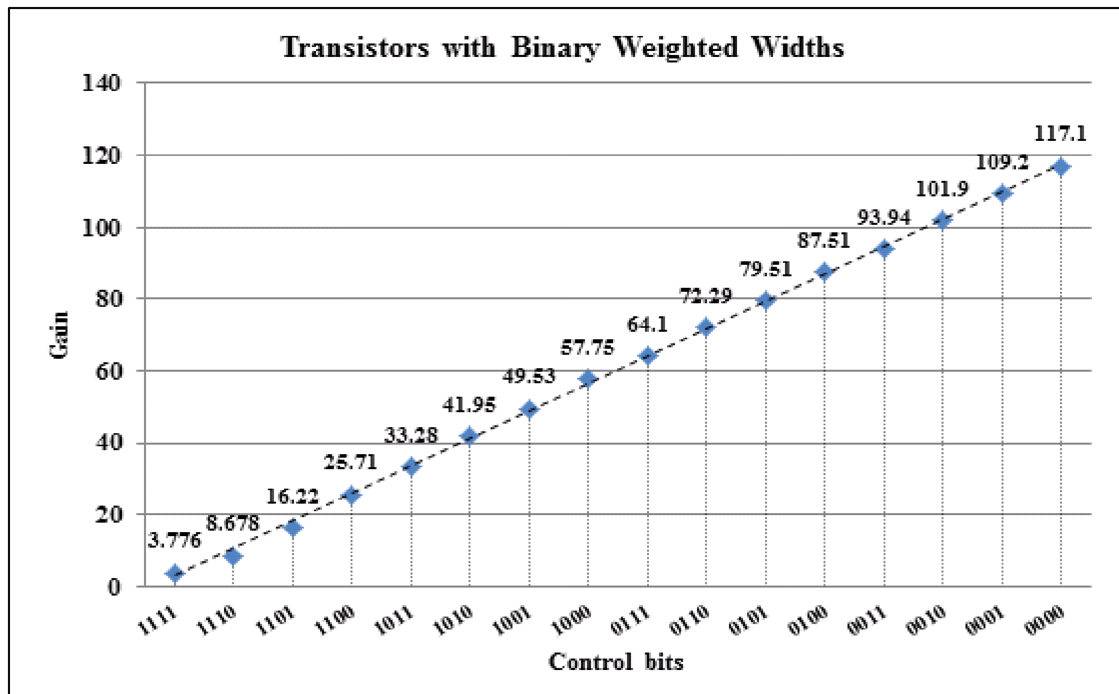

Figure 3.26: Programmable time amplifier gain versus input bit pattern, using Virtuoso Spectre Circuit Simulator.

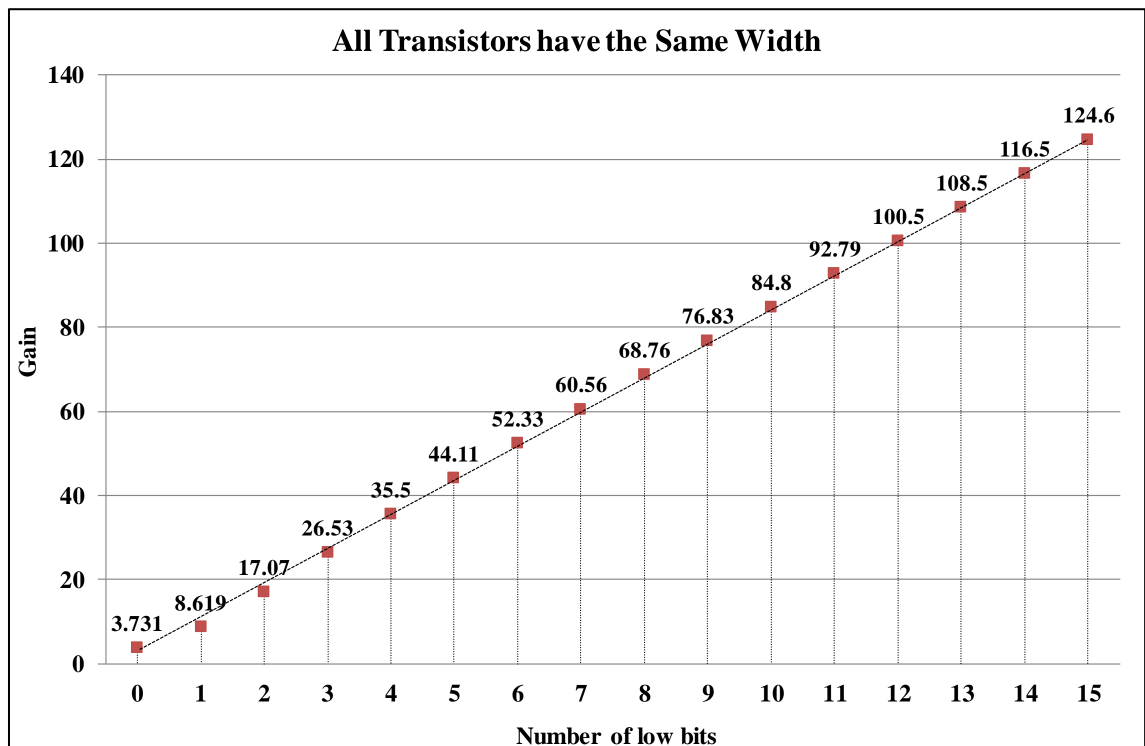

Figure 3.27: Programmable time amplifier gain versus number of low bits, using Virtuoso Spectre Circuit Simulator.

3.7 Summary and Conclusions

Improvements in circuit performance have been achieved by replacing the buffer delay on the input to create the time offset. The buffer delays comprised inverters which were susceptible to mismatch problems due to effects of process variations, furthermore as the value of the time offset increased the area consumed by the buffer delays also increased.

The enhanced design evolved in three phases, first the need for input buffer delays was removed by adding 'unbalanced' capacitance loading to the outputs of the cross-coupled NAND gates in the MUTEX. Although this modification had the same dynamic input range as buffer delay offset method, it removed the main disadvantage of using buffer delays to create time offset in the MUTEX. Subsequent improvements to the dynamic input range were achieved through the use of 'charge pump' loads and the addition of a series resistance to the 'pull down' network in the NAND gates.

The capabilities of the time amplifier circuit were further enhanced by including a programmable gain feature. Depending up the measurement resolution required by a given application the gain of the amplifier can be varied from 4 to 117 in discrete steps.

3.8 References

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Chapter 4

A Comparison of the Time Amplifier Circuits

4.1 Introduction

Three designs were discussed in Chapter 3 namely; buffer delay offset, unbalanced active capacitive load and unbalanced active charge pump load designs while the dynamic range of these designs were effectively improved using NAND gate with added resistance method. However, as technology is continuously scaled down, the design margins are decreased and it becomes more difficult for the circuits to meet the design specifications. In addition, the robustness of the design to the effects of process, temperature and power variations is decreased and hence it becomes necessary to study the reliability of the design. Different methods have been used to estimate the effect of the process variation while the most common methods are the Worst Case-corner Analysis [1] and Monte Carlo Analysis [2]. However, in this work Monte Carlo analysis is used, as it is more pragmatic to study the process variations effect than using multiple corner analyses [3].

The following sections comprise a description of the Worst Case-corner Analysis and Monte Carlo Analysis Techniques in section 4.2, followed in section 4.3 with an analysis of the effect of process variations on the three time amplifier designs using NAND gate with and without additional resistance technique. In section 4.4, the sensitivity to temperature variation is studied, followed, in section 4.5, by the description of the effect of the power supply variation, ending with a summary of the Chapter in section 4.9.

4.2 Worst Case-corner and Monte Carlo Analysis Techniques

Process variation has become an increasingly important issue in CMOS technology, as device dimensions have been scaled down to the nanometre range. Thus, the effect of process variation on the circuit performance is required to be analysed and hence design specifications can be developed to be more robust to their effects.

The most common techniques which have been widely used to study the effect of the process variation on the circuit performance are Worst Case-corner and Monte Carlo analysis techniques. The Worst Case-corner technique is based on studying the performance of the circuit using NMOS and PMOS parameters on the nominal and the worst-case slow and best-case fast process corners [1]. The main advantage of this technique is the computational time which is very short compared to other methods. However, ensuring correct circuit operation at the worst and best extremes of the process corners leads to overdesign, as it is very unusual for NMOS and PMOS parameters to be at on the extremes of the process corners [4], as shown in the process variation map, Figure 4.1, for ID_{sat} for NMOS and PMOS transistors. In addition it is accepted that studying the robustness of the circuit to the effects of process variations only at certain cases does not provide realistic assessment of the circuits immunity to these effects.

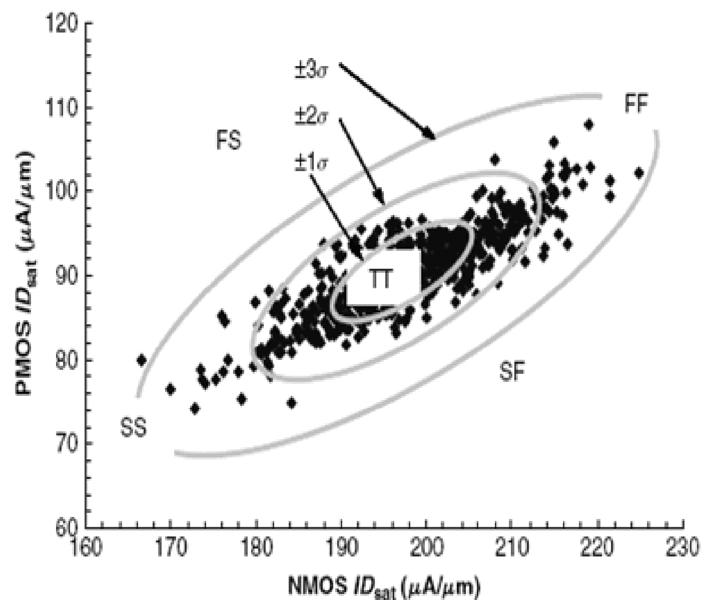


Figure 4.1: Process variation map for N and P-MOSFET devices [5].

An accurate prediction for the circuit performance is necessary, as the circuit sensitivity to the effect of process variation is increased, due to the continuous scaling down of the technology. One of the techniques which is used to achieve an accurate prediction for the circuit performance, under the effect of the process variation, is the Monte Carlo analysis [2]. It evaluates the performance of the circuit under the effect of the process variation based on repetitively generating random values of NMOS and PMOS

parameters, within a defined range of process parameter variations. The generated values are called iterations or samples and in Monte Carlo technique the number of samples is usually large, several thousands, in order to cover a large number of possible situations. The sample results are collected and studied to show the probability distribution of feasible circuit operations. This can provide an understanding of the circuit performance against the process variation and hence how to minimize this effect. The computational algorithm for the Monte Carlo analysis technique is shown in Figure 4.2 [6]. Comparing this with the Worst Case-corner analysis technique, the Monte Carlo technique is more realistic, as it covers a large number of possibilities, unlike the Worst Case-corner analysis where the result is only calculated at certain cases. One major drawback of the Monte Carlo analysis is the long computation times, where this can be accepted the advantage of the higher accuracy is obtained. Thus, the Monte Carlo technique was used in this work to study the robustness of the time amplifier designs to the effects of the process variations. However, before proceeding with the analysis some of the terms used regarding statistical distributions will be defined.

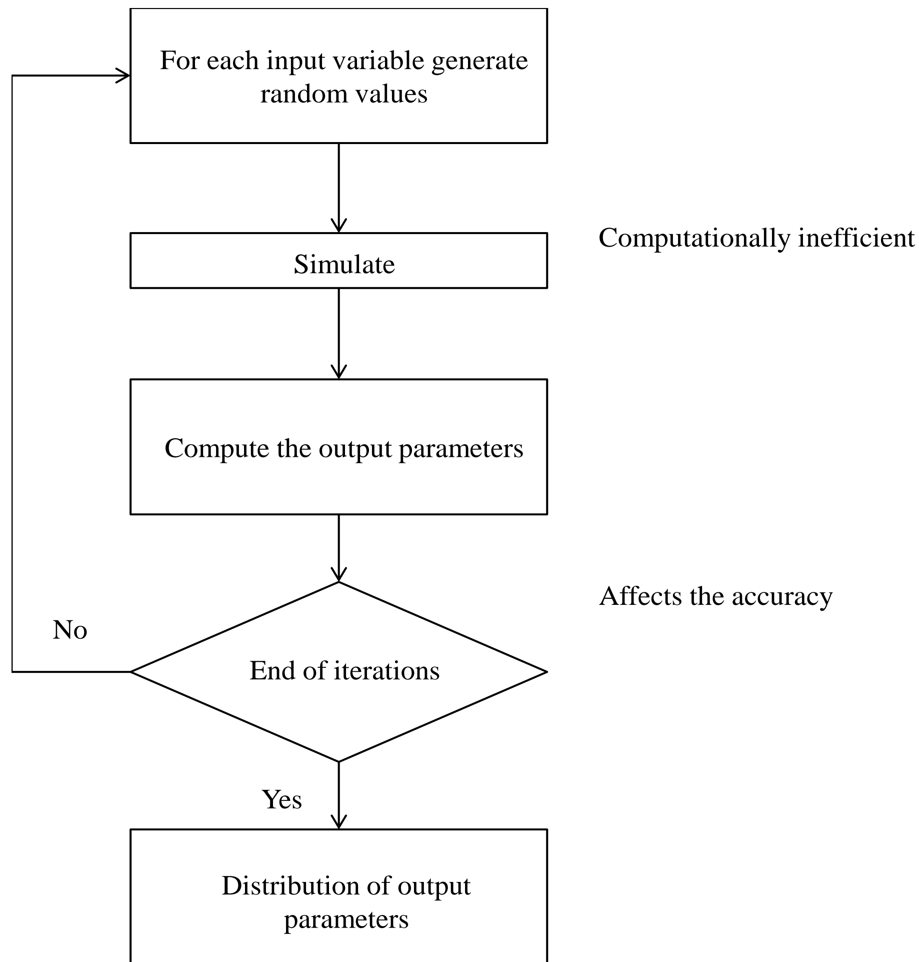


Figure 4.2: Monte Carlo analysis [6].

a) Mean (μ): The *mean* in statistics represents the average of a discrete random variable. It is calculated by summing up all the values of the discrete random data and dividing the result by the number of values (n), as shown in Equation 4.1.

$$\mu = \frac{\sum x}{n} \quad \text{--- (4.1)}$$

b) Variance: The *variance* describes the probability distribution of discrete random data or how far the data spreads from the mean. It is calculated as shown in equation (4.2)

$$Variance = \frac{\sum (x-\mu)^2}{n-1} \quad \text{--- (4.2)}$$

c) Standard Deviation (σ): The *standard deviation* is the square root of the variance, Equations (4.3), which indicates the level of variation of the data from the mean. A high standard deviation value represents a large spread in the data from the mean while a low standard deviation value represents a small spread from the mean.

$$\sigma = \sqrt{\frac{\sum(x-\mu)^2}{n-1}} \quad \text{--- (4.3)}$$

d) *Three-sigma rule:* The *three-sigma* or 3σ specifies the data sited within the range of 3 standard deviations from the mean in a normal distribution, as shown in Figure 4.3. It is worth noting that in the normal distribution 99.7 % of the data are include within the 3σ range.

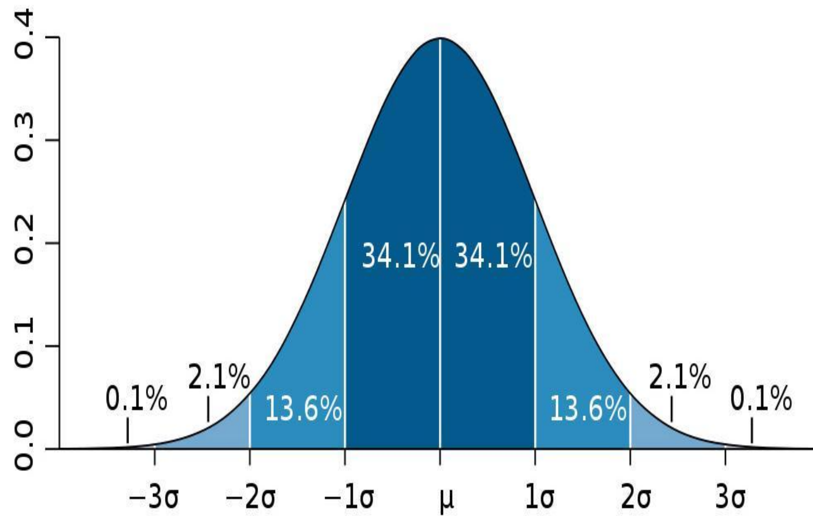


Figure 4.3: One, two and three σ ranges within the normal distribution graph [7]

4.3 Time Amplifier Process Variation Analysis

The main design parameters for a time amplifier are its gain and dynamic range, consequently the effect of process variation on them will be analysed. The study is first performed when the time input difference is 1 ps, ΔT_{input} = 1ps, to focus only on the gain variation without the effect of the degradation in the linearity along the amplification range. Thereafter, the gain variation is analysed along the dynamic range,

to address the effect of the process variation and the degradation in the linearity on the gain.

4.3.1 Gain Variation Analysis

The effect of the process variation on the gain of the time amplifier circuits using buffer delay offset, unbalanced active capacitive load and unbalanced active charge pump load designs were studied using Monte Carlo analysis, as it is more pragmatic to study the process variations effect than using multiple corner analyses, as discussed in section 4.2.

The Monte Carlo analysis was run considering the process variation of 3σ(of NMOS and PMOS parameters such as width, channel length, oxide thickness etc.) with 2000 samples at Vdd = 1V and temperature = 27°C using Virtuoso Spectre Circuit Simulator in CADENCE suite of CAD tools.. The effects of the process variation on the gain of the three time amplifier circuits was analysed first when ΔT_{input} = 1ps. Figure 4.4 shows that unbalanced active capacitive load and unbalanced active charge pump load designs are more robust than the buffer delay offset design in terms of gain variation. The T_{offset} in the unbalanced active capacitive load and unbalanced active charge pump load designs are created by the difference in capacitance values between the active loads. As a result the gain of these designs becomes a ratio between the capacitance values, from Equation (4.4). Thus, they are more robust than the buffer delay offset design which has two buffer delays to form the T_{offset}.

$$G = \frac{2 \cdot \tau}{T_{offset}} , \; (\tau = \frac{C}{g_m}) \text{ --- } (4.4)$$

Where: G is the gain, τ is MUTEX time constant, g_m is transconductance of the NAND gate at the metastable condition, and C is the output capacitance of the NAND gate.

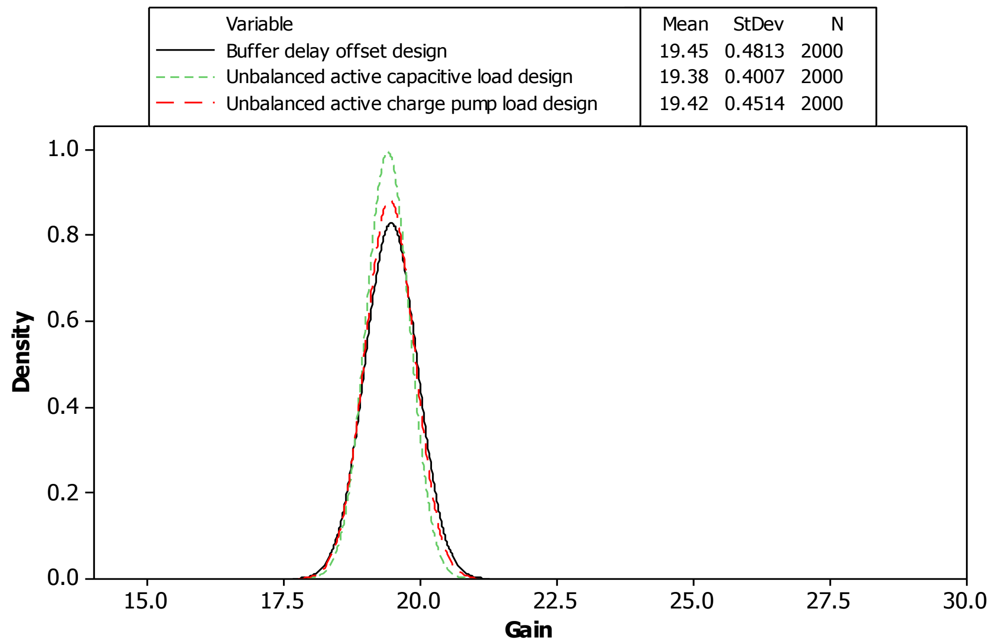


Figure 4.4: Histogram plots for the gain against process variation for the gain of the three time amplifier circuits.

On the other hand, although, implementing the three time amplifier circuits using NAND gate with added resistance on the discharge path creates a huge improvement in terms of the dynamic input range, the gain sensitivity to the process variations is increased, as shown in Figure 4.5. The increase in gain sensitivity to the process variations is related to the placement of the additional resistance between the NAND gate circuit and the ground, as shown in Figure 4.6, having a direct impact on the capacitance discharge currents. In addition, the transistor which forms the resistance is sized to be small in width, in order to achieve the required resistance value, leading to an increase the sensitivity to even small variations in the transistor size. Table 4.1 shows the effect of the added resistance on the discharge currents for the unbalanced active capacitive load and unbalanced active charge pump load designs. It can be seen that the values of the standard deviation over the mean (σ/μ) of I_{C1} Max, I_{C1} RMS, I_{C2} Max and I_{C2} RMS for the NAND gate without added resistance is lower than that for the NAND gate with added resistance on the discharge path which explains the increase in gain sensitivity to the process variations when the added resistance on the discharge path is used, the Max value of the discharge currents represents the peak value during the discharge time while the RMS value of the discharge currents represent the root mean square value of the current during discharge time.

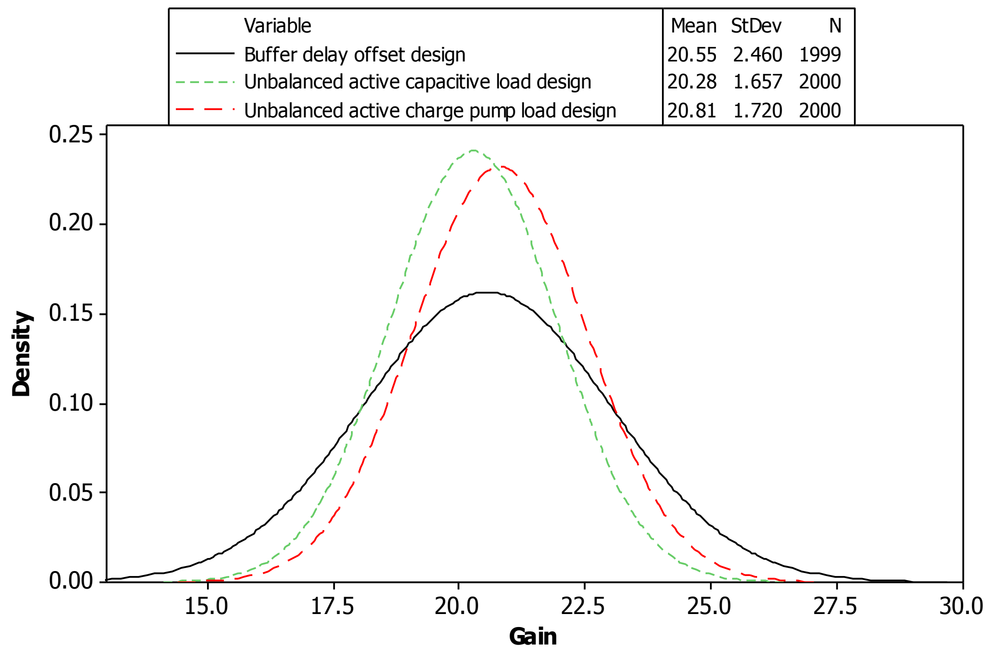


Figure 4.5: Histogram plots for the gain against process variation for the three time amplifier circuits implemented using the NAND gate with added resistance in the discharge path.

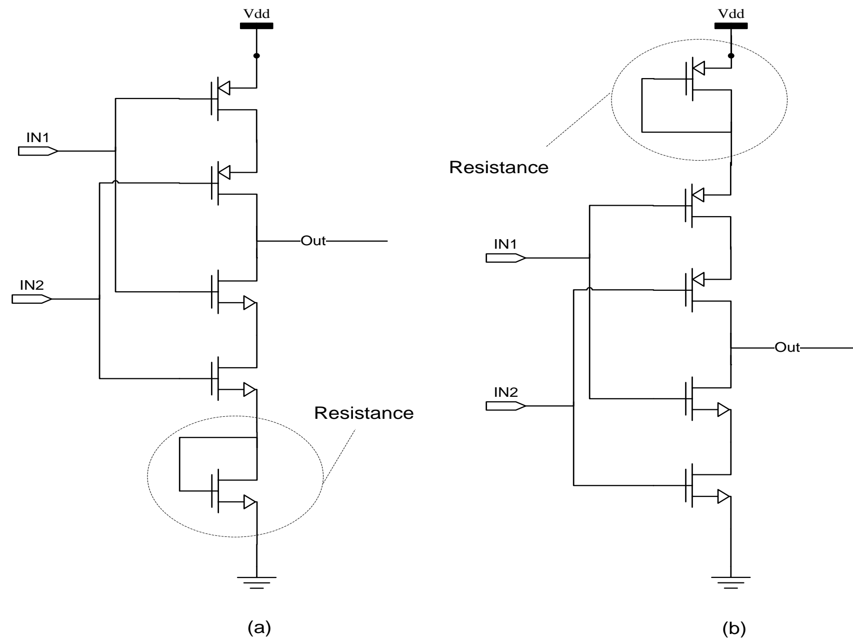


Figure 4.6: NAND gate with added resistance.

	Unbalanced Active Capacitive Load Design					
	Without added resistance			With added resistance in discharge path		
	σ (10^{-6})	μ (10^{-6})	σ/μ	σ (10^{-6})	μ (10^{-6})	σ/μ
I_{C1} Max	7.739	179.40	0.04314	3.81	30.60	0.12458
I_{C2} Max	7.726	179.20	0.04311	3.81	30.60	0.12458
I_{C1} RMS	0.263	7.36	0.03577	0.215	2.43	0.08842
I_{C2} RMS	0.307	9.62	0.03195	0.281	3.40	0.08239
	Unbalanced Active Charge Pump Load Design					
I_{C1} Max	7.79	175.90	0.04426	3.76	30.03	0.12521
I_{C2} Max	7.77	174.90	0.04443	3.75	29.99	0.12514
I_{C1} RMS	0.372	7.07	0.05253	0.213	1.81	0.11769
I_{C2} RMS	0.386	10.7	0.03604	0.287	3.02	0.09484

Table 4.1: The mean, standard deviation, and standard deviation over mean values of the discharge currents under process variation.

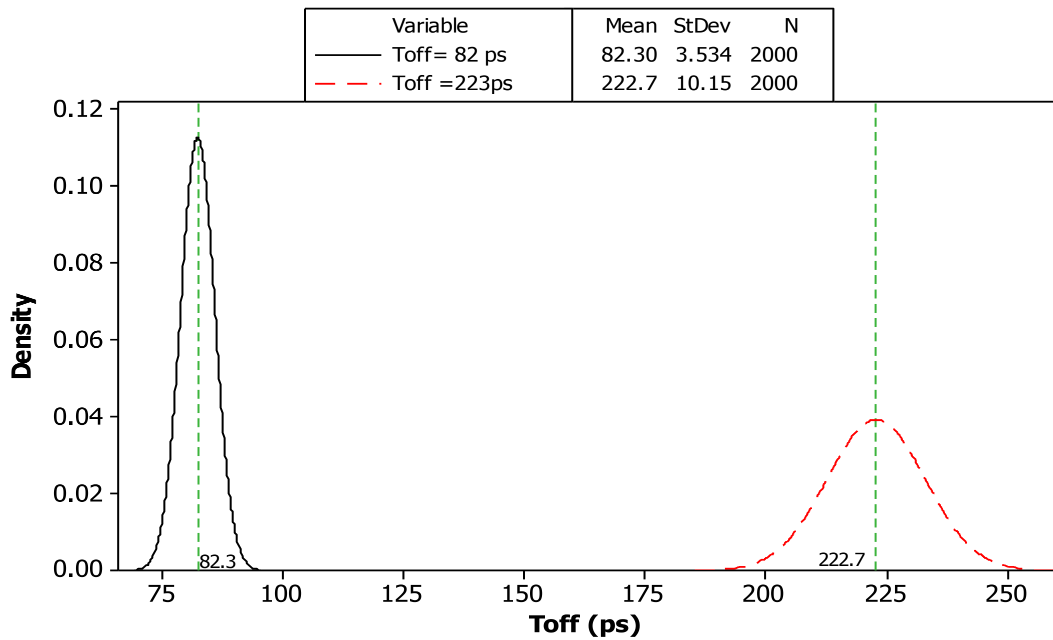


Figure 4.7: Histogram plots for two values of T_{off}, implemented using two inverters, against process variation.

Nevertheless, it can be seen from Figure 4.5 that the gain of the buffer delay offset design, when implemented using the NAND gate with added resistance, was significantly affected by the process variation compared to the unbalanced active capacitive load and unbalanced active charge pump load designs. This because when the buffer delay offset design is implemented using the NAND gates with added resistance, the value of T_{off} needs to be increased to achieve the nominal gain of 20 for all circuits, as discussed in Chapter 3. As T_{off} is implemented using inverters, T_{off} is increased by reducing the size of the PMOS transistors and increasing the size of the NMOS transistors. From the simulation results, the required value for T_{off} is approximately 223ps in order to have a gain of 20. Designing such a delay using two inverters makes the buffer delay, T_{off}, susceptible to even a slight variation on transistors size. Figure 4.7 shows the effect of the process variation in T_{off} before and after resizing the buffer transistors.

By considering the alternative position of the added resistance in the NAND gate, it can be seen from Figure 4.5 and 4.7 that implementing the time amplifier circuits with added resistance between the voltage source and the NAND gate are more robust in terms of gain variation than placing the resistance on the discharge path. This is because the resistance which is placed between the voltage source and NAND gate affects the discharge currents through reducing the gate voltage of the NMOS transistors in the NAND gate, as discussed in Chapter 3, leading to lowering of the effect of this resistance on the discharge currents when this is implanted directly into the discharge path. Thus, as it can be observed from Table 4.2, the I_{C1} Max, I_{C1} RMS, I_{C2} Max and I_{C2} RMS for the added resistance between the voltage source and NAND gate method has a lower standard deviation over the mean values (σ/μ) than added resistance in the discharge path.

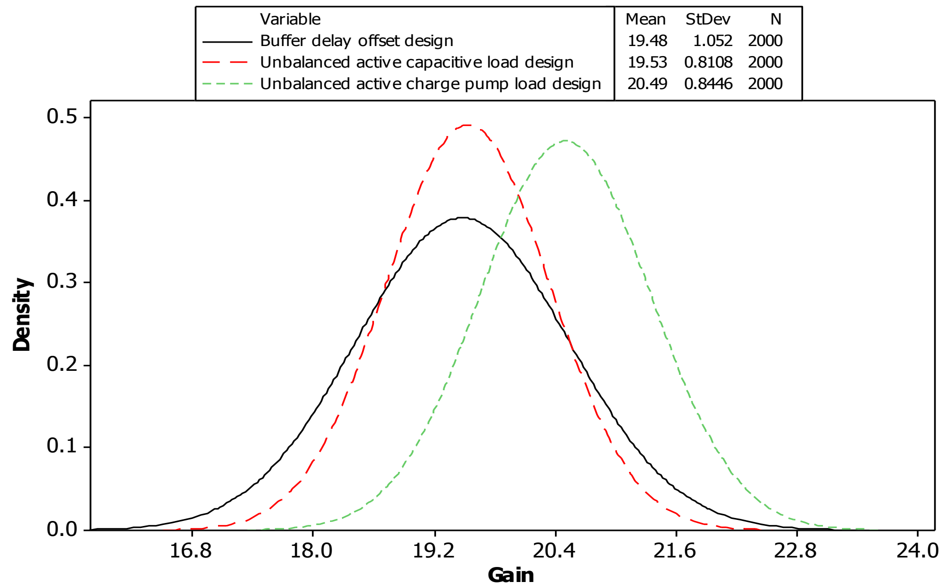


Figure 4.8: Histogram plots for the gain against process variation for the three time amplifier circuits implemented using the NAND gate with added resistance between Vdd and the NAND gate.

	Unbalanced Active Capacitive Load Design					
	With added resistance between NAND gate and Ground			With added resistance between voltage source and NAND gate		
	σ (10^{-6})	μ (10^{-6})	σ/μ	σ (10^{-6})	μ (10^{-6})	σ/μ
I_{C1} Max	3.81	30.60	0.12458	6.15	136.60	0.04504
I_{C2} Max	3.81	30.60	0.12458	6.14	136.50	0.04499
I_{C1} RMS	0.215	2.43	0.08842	0.192	5.16	0.03714
I_{C2} RMS	0.281	3.40	0.08239	0.223	7.05	0.03161
	Unbalanced Active Charge Pump Load Design					
I_{C1} Max	3.76	30.03	0.12521	6.65	145.70	0.04561
I_{C2} Max	3.75	29.99	0.12514	6.63	145.30	0.04566
I_{C1} RMS	0.213	1.81	0.11769	0.278	5.45	0.05094
I_{C2} RMS	0.287	3.02	0.09484	0.284	8.22	0.03461

Table 4.2: The mean, standard deviation, and standard deviation over mean values of the discharge currents under process variation.

The gain of the buffer delay offset design has the highest sensitivity to the effects of process variation among the three time amplifier circuits when the resistance is added between the voltage source and the NAND gate, as shown in Figure 4.8. This is because the additional resistance leads to increase the gain value which requires the gain to be redesigned by increasing the value of T_{off}, as discussed in Chapter 3, the required value for T_{off} is approximately 149 ps in order to have a gain of 20. However, as previously discussed in this section, the increase in the value of T_{off} leads to an increase in its sensitivity to the effect of process variation, as shown in Figure 4.9.

In the buffer delay offset design, the highest variation in the gain occurred when the added resistance on the discharge path technique is used while the lowest gain variation occurs when no resistance is added. In addition, the added resistance between the voltage source and the NAND gate is more robust than adding the resistance in the discharge path in terms of gain variation. Upon the previous discussion, the gain variation is highly related to the variation in T_{off} in the buffer delay offset design and as the value of T_{off} increased the effect of the process variations on T_{off} is increased, as shown in Figure 4.9.

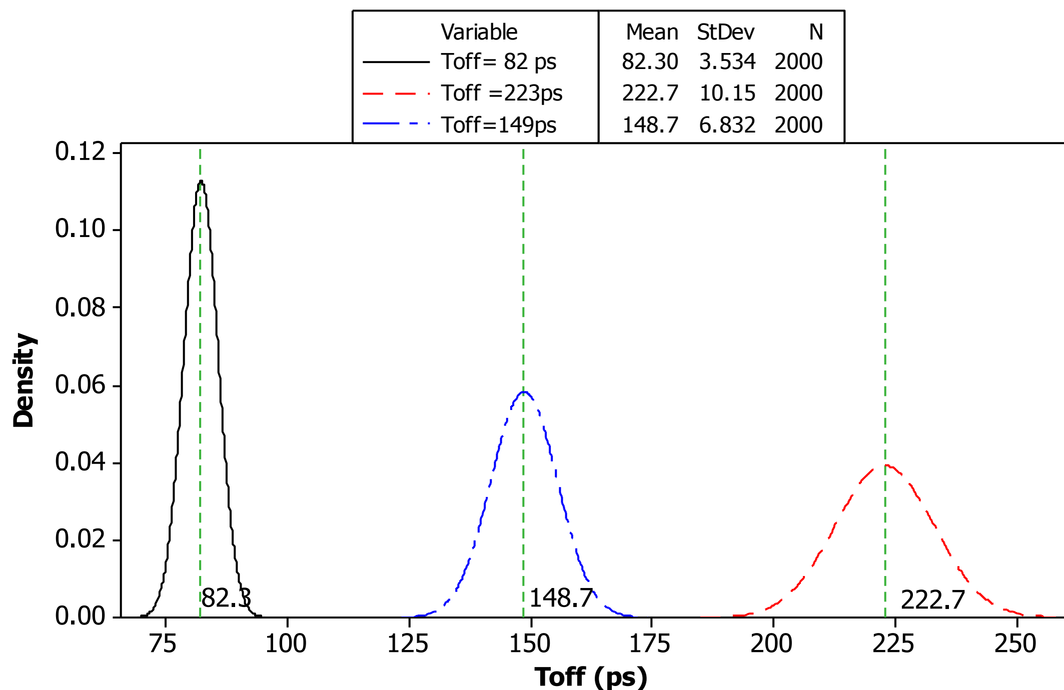


Figure 4.9: Histogram plots for the values of T_{off}, implanted using two inverters, against process variation.

4.3.2 The Linearity and Gain Variation Analysis

The dynamic input range is a critical issue in the design of a time amplifier, as discussed in Chapter 3. The widest dynamic input range occurred using an unbalanced active charge pump load with the NAND gate with added resistance in the discharge path. Although it has the widest dynamic range, it has the lowest robustness to the effects of the process variation among the three time amplifier circuits in term of gain variation, as shown in the analysis in section 4.3.1. However, all the analysis in section 4.3.1 was undertaken with ΔT_{input} = 1ps. In this section, the effect of the process variation on the gain over the dynamic input range is studied in order to analysis the effect of the degradation in the linearity of the gain. In this study the added resistance technique will only be used on the discharge path, as it produce a much wider in dynamic range than placing the resistance between the voltage source and the NAND gate.

By comparing Figures 4.10, 4.11, 4.12, 4.13, 4.14 and 4.15, it is clear that the mean values of the gain were nearly fixed to 20, over the dynamic input range of 300 ps, for the unbalanced charge pump design implemented using NAND gate with added resistance on the discharge path, while the mean values of the gain for the other designs were shifted by around 2ps along their dynamic input ranges. The change in the mean values of the gain for these designs occurred near to the edge of the dynamic input range. For example, for the unbalanced charge pump load design the mean values of the gain was nearly 20 for ΔT_{input} range from 1 ps to 50 ps while it starts increasing to 21.13 at 70 ps. By considering the time amplifier characteristic, shown in Figure 4.16, it can be seen that the linearity of the characteristic degrades around 70 ps where the gain variation around this region is higher than the one close to 1ps, as it is far from the nonlinear region. It is observed that as the value of ΔT_{input} is located further from the nonlinear region, the mean values of the gain are fixed to the defined value. Thus, a wide dynamic input range leads to constant mean values of the gain along a wider range, as shown in Figure 4.15. In addition, Figure 4.10, 4.12 and 4.14, which are for the three time amplifier circuits without added resistance in the discharge path, show that the gains for these design is shifted over the dynamic input range while this shift is smaller for the unbalanced active charge pump load design, as it has a wider dynamic input range.

Buffer Delay Offset Design

Without added resistance

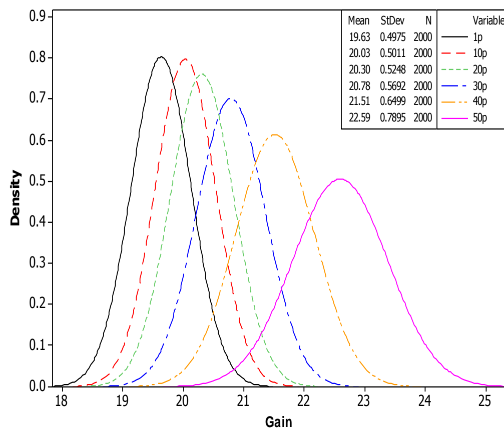


Figure 4.10: Histogram plots for the gain against process variation, over a dynamic input range from 1 ps to 50 ps.

With added resistance

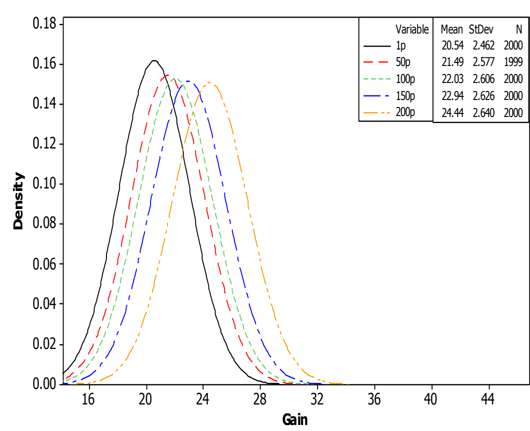


Figure 4.11: Histogram plots for the gain against process variation, over a dynamic input range from 1 ps to 200 ps.

Unbalanced Active Capacitive Load Design

Without added resistance

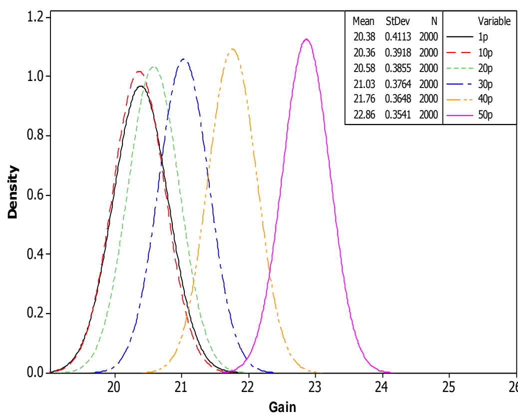


Figure 4.12: Histogram plots for the gain against process variation, over a dynamic input range from 1 ps to 50 ps.

With added resistance

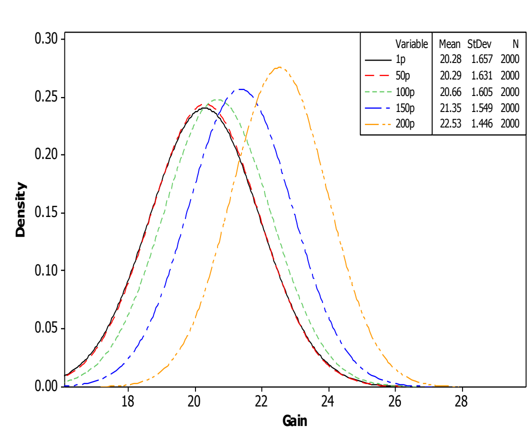
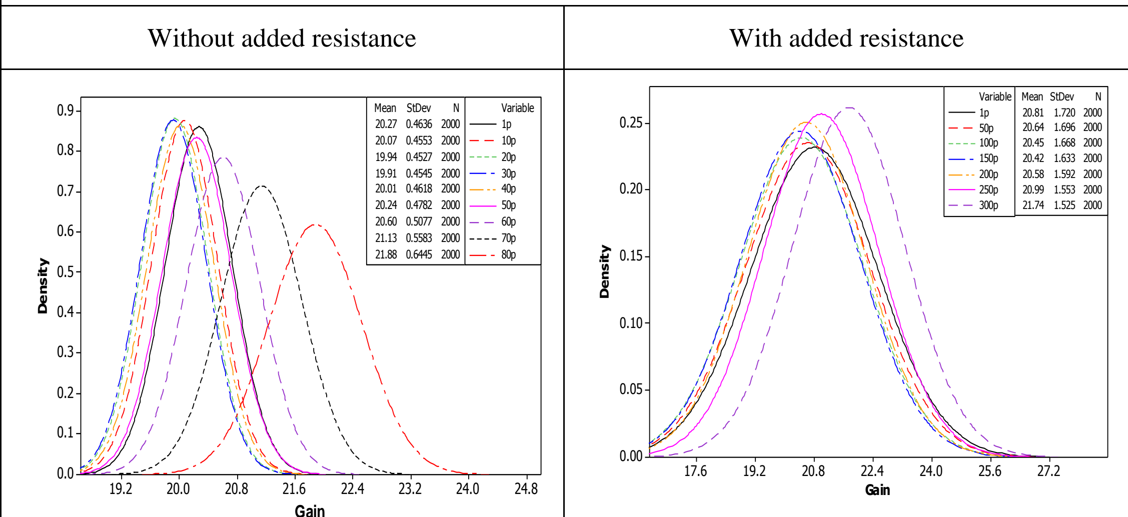


Figure 4.13: Histogram plots for the gain against process variation, over a dynamic input range from 1 ps to 200 ps.

<table>
<tr><th colspan="2">Unbalanced Charge Pump Load Design</th></tr>
<tr><td>Without added resistance</td><td>With added resistance</td></tr>
<tr><td colspan="2">
</td></tr>
<tr><td>Figure 4.14: Histogram plots for the gain against process variation, over a dynamic input range from 1 ps to 50 ps.</td><td>Figure 4.15: Histogram plots for the gain against process variation, over a dynamic input range from 1 ps to 300 ps.</td></tr>
</table>

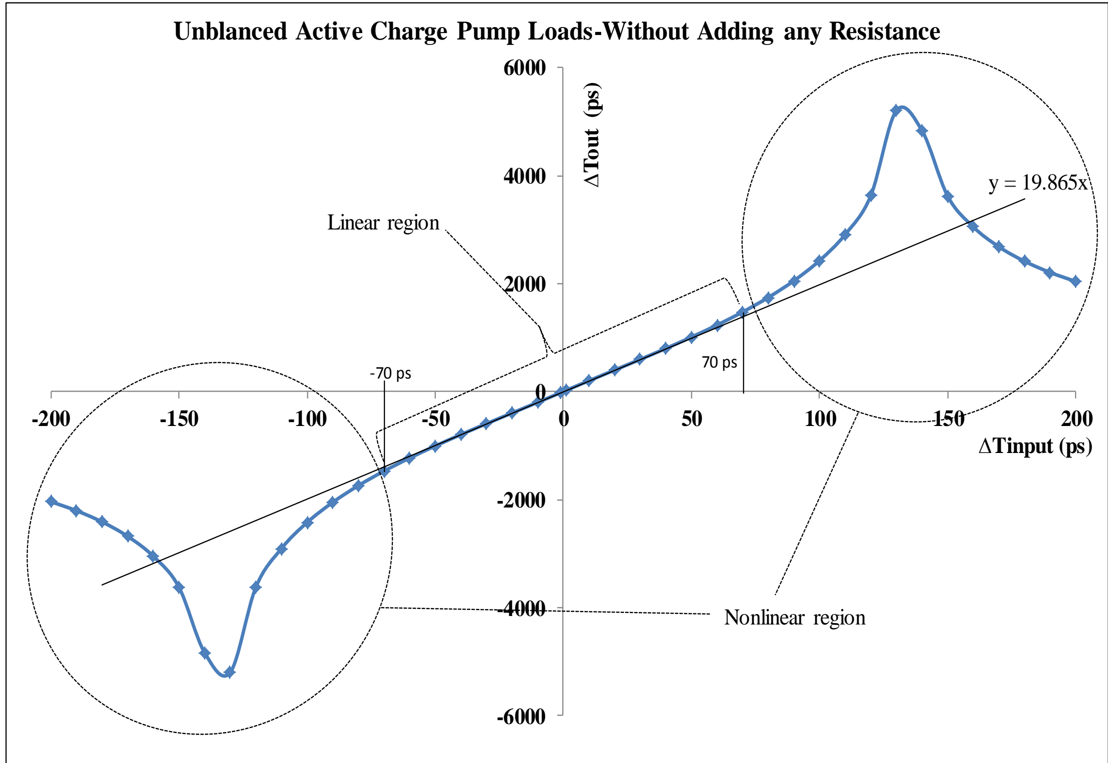


Figure 4.16: The characteristics for the time amplifier.

4.4 Time Amplifier Temperature Variation Analysis

As discussed in Chapter 1, transistor operation is affected by temperature variations which directly impact on the circuit operation. The sensitivity of the gain of the time amplifier to the effects of temperature variations has yet to be investigated. Consequently, in this section the effect of the temperature variation on the gain for the three time amplifier circuits with and without added resistance are discussed.

The effect of temperature on MOSFET behaviour depends on the operating conditions. There are two main operating states to be considered for the MOSFET when investigating the effect of temperature variation. First, the subthreshold condition, or weak-inversion mode, where the gate to source voltage V_{gs} is lower than the threshold voltage, V_{th}. In this condition, as the temperature is increased, the drain to source current, I_{DS}, is increased and the resistance of the MOSFET is decreased [8, 9]. However, when the MOSFET is in the linear and saturation mode, where V_{gs} is higher than V_{th}, the increase in the temperature leads to a decrease in I_{DS} and hence an increase in the resistance of the MOSFET [9, 10]. The effect of the temperature increase on the MOSFET current and resistance under these two operating conditions are summarised in Table 4.3

Operation condition	I_{DS}	MOSFET resistance
$V_{gs} < V_{th}$	Increase	Decrease
$V_{gs} > V_{th}$	Decrease	Increase

Table 4.3: The effect of the temperature increase on the MOSFET current and resistance.

Figure 4.17 illustrates the impact of the temperature variation on the gain of the buffer delay offset, unbalanced active capacitance load and unbalanced active charge pump load designs. From this Figure, it can be seen that the gain of the buffer delay offset and unbalanced active capacitance load designs are virtually unaffected by the change in the temperature while in the unbalanced active charge pump load design the gain is increased as the temperature increases.

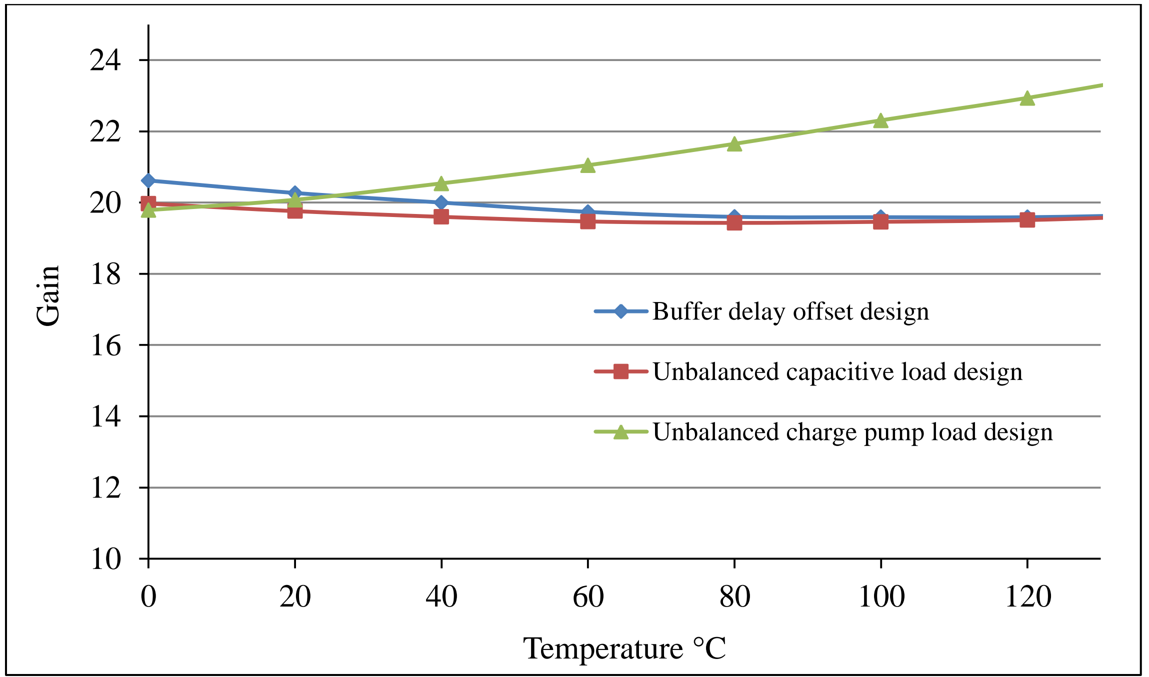


Figure 4.17: Variation of gain for the three time amplifier circuits against temperature.

To analyse the reason for the diverse sensitivity of the gain in each design to the effect of temperature variation, the three parameters which have a direct impact on the gain, namely, the capacitance at the NAND gate output, the resistance in the discharge path of the capacitance and the T_{offset}, as shown in Equation 4.5, need to be considered. All the designs have the same capacitance and equal NAND gate transconductance, while the effective T_{offset} is adjusted depending upon the circuit configuration. In addition, there is more resistance in the discharge path for the unbalanced active charge pump load design resulting from Q_1 and Q_2 in the charge pump load, as described in Chapter 3.

$$G = \frac{2 \cdot C \cdot R_m}{T_{offset}}, \ (R_m = \frac{1}{g_m}) \text{ --- } (4.5)$$

Where: G is the gain, τ is MUTEX time constant, g_m is transconductance of the NAND gate at the metastable condition, and C is the output capacitance of the NAND gate.

In the buffer delay offset design, the capacitances are discharged through the resistance, R_m, of the NMOS transistors in the NAND gate, as the temperature is increased the resistance, R_m, will increase; since during discharge their $V_{gs} > V_{th}$. The increase in the resistance in the discharge path, as discussed in Chapter 3, leads to an increase in the gain. However, as the temperature increases, the delay of the buffer, T_{off}, is increased, as

shown in Figure 4.18, leading to an increase in T_{offset}. Now from Equation 4.5, the increase in T_{offset} decreases the gain while the increase of the resistance, R_m, increases the gain. It can be observed that although the increase in the temperature increases the resistance in the discharge path, it also increases T_{offset} which leads the gain almost remain constant against the changes in temperature. The increase in the resistance in the discharge path, as the temperature increases, can be seen in the degradation in the discharge currents in Figure 4.18. In addition, the constant difference between I_{C1} RMS and I_{C2} RMS represents the stability of the gain as the temperature is increased.

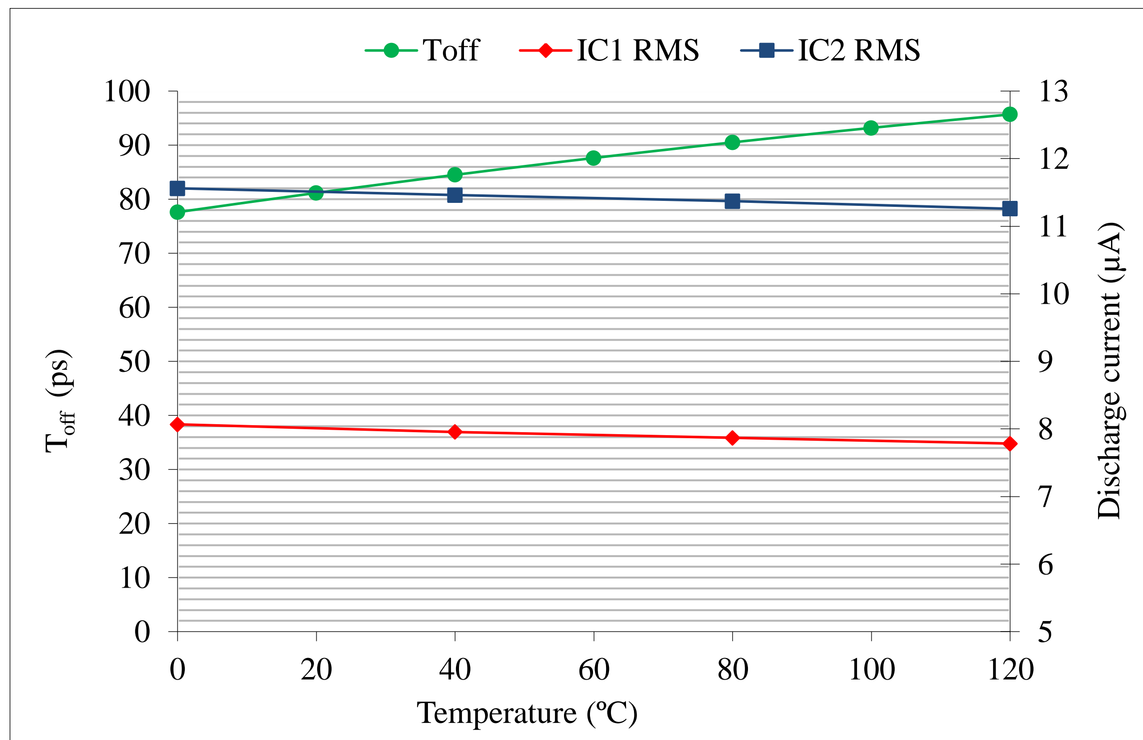


Figure 4.18: T_{off} and the discharge currents against the temperature-buffer delay offset design.

In the unbalanced active capacitance load design, the performance of the gain against the changes in the temperature is the same as in the buffer delay offset design, although T_{offset} is adjusted in different way. T_{offset} in the unbalanced active capacitance load is adjusted by designing one capacitance to be larger than the other, which creates a difference in the discharge time constant τ_1 and τ_2. As the temperature increases the resistance of the NMOS transistors in the discharge path also increases leading to an increase in the difference between the τ_1 and τ_2, as $C_1 > C_2$. Therefore T_{offset} is increased as the temperature is increased. However, similarly to the buffer delay offset design, from Equation 4.5, the increase in the temperature causes an increase in the value of R_m.

Thus, the gain becomes stable as the temperature is increased, an increase in the temperature causing an increase in both R_m and T_{offset} by nearly the same amount. The stability in the gain can be seen from the fixed difference between I_{C1} RMS and I_{C2} RMS, as shown in Figure 4.19.

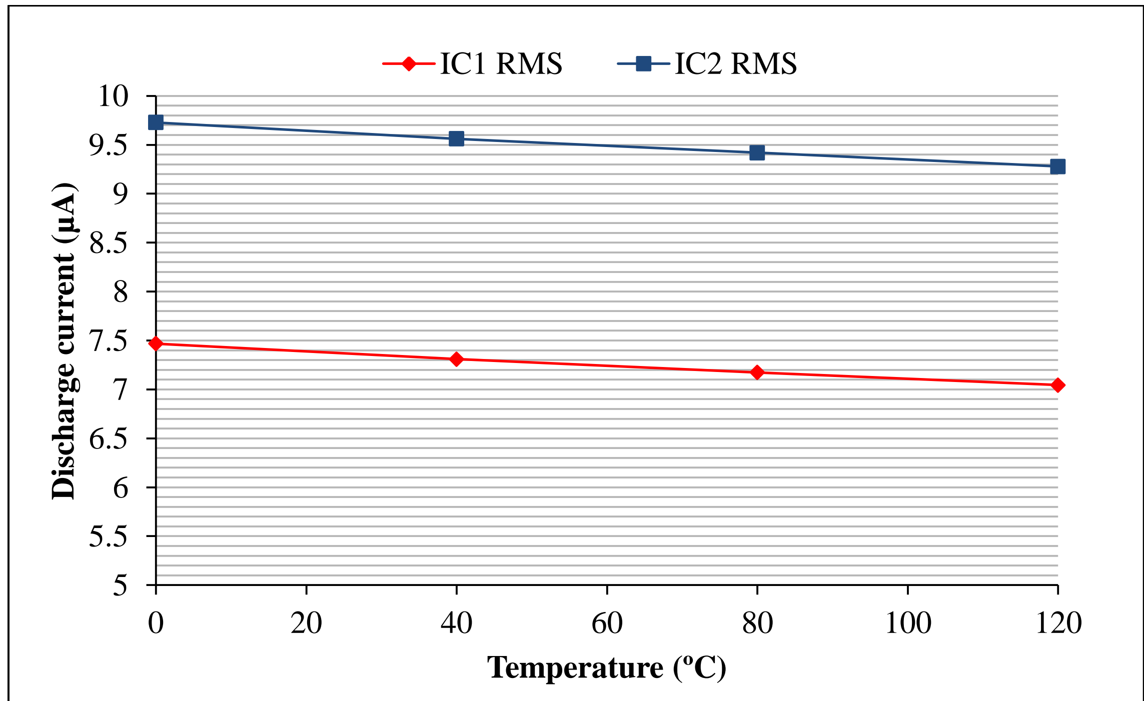
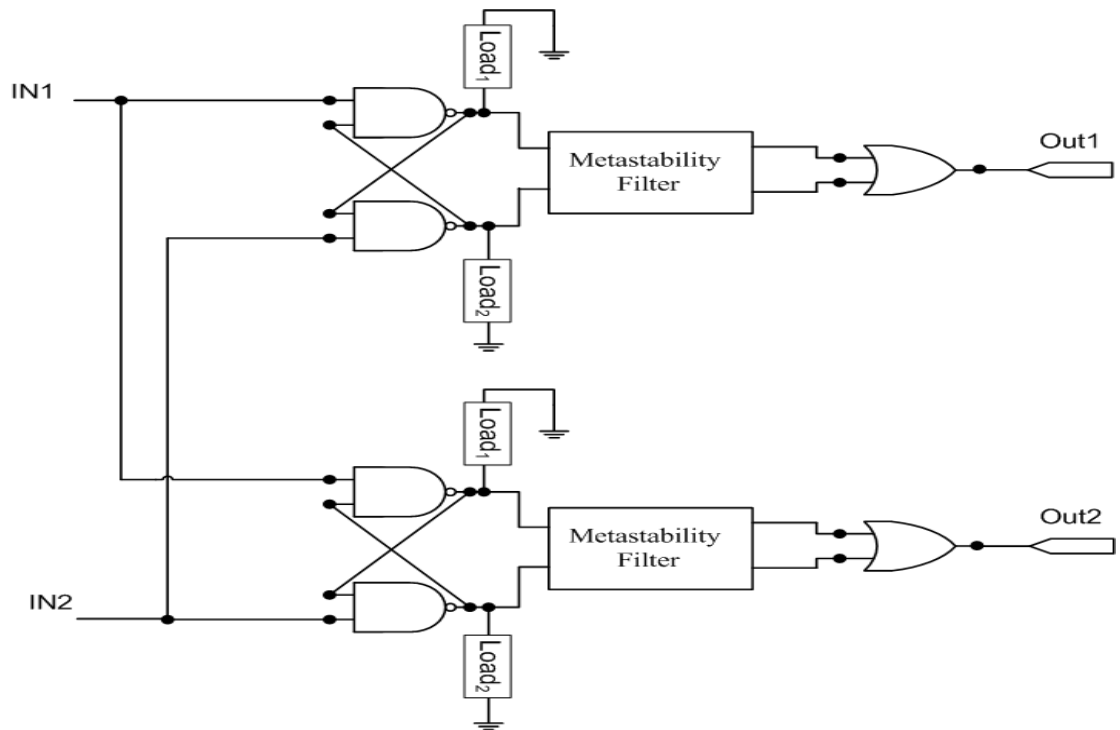


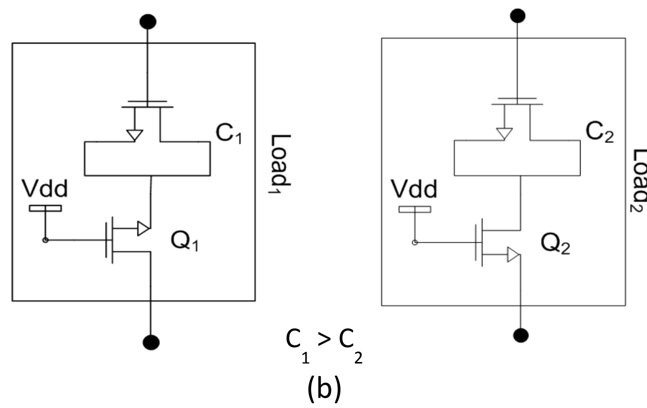
Figure 4.19: The discharge currents against the temperature-unbalanced capacitance load design.

Unlike the buffer delay offset and unbalanced active capacitance load designs, the gain of the unbalanced active charge pump load design is increased as the temperature is increased. The transistor Q_1, shown in Figure 4.20, during discharge, works in the subthreshold mode resulting from its V_{gs} being lower than V_{th}, V_{th} for both Q_1 and Q_2 is equal to 0.3 V. Figure 4.21 shows that V_{gs} for Q_1, during discharge time, is mainly below 0.3 V, where for Q_2 it is mainly above 0.3 V which leads to a decrease in the resistance of Q_1 and an increase in the resistance of Q_2, as the temperature is increased. T_{offset} is created in the unbalanced active charge pump load design in similar way as the unbalanced active capacitance load designs, by designing C_1 to be larger than C_2 which creates a difference in the discharge time constant τ_1 and τ_2. However, in the charge pump load design, as the temperature is increased, the resistance of Q_1 is decreased while it is increased for Q_2 causing the difference between τ_1 and τ_2 to become smaller, as $C_1 > C_2$, which causes a decrease in T_{offset}. Thus, as the temperature is increased, the gain is increased due to the reduction in value of T_{offset}. By considering the difference between I_{C1} RMS and I_{C2} RMS, shown in Figure 4.22, the effects of the opposite

behavior of the resistance of Q_1 and Q_2 on the discharge currents can be seen; as the temperature is increased, I_{C1} RMS is increased while I_{C2} RMS is decreased.



(a)



$C_1 > C_2$

(b)

Figure 4.20: (a) Time amplifier using unbalanced active load design. Unbalanced active charge pump load using (b) C1> C2 and

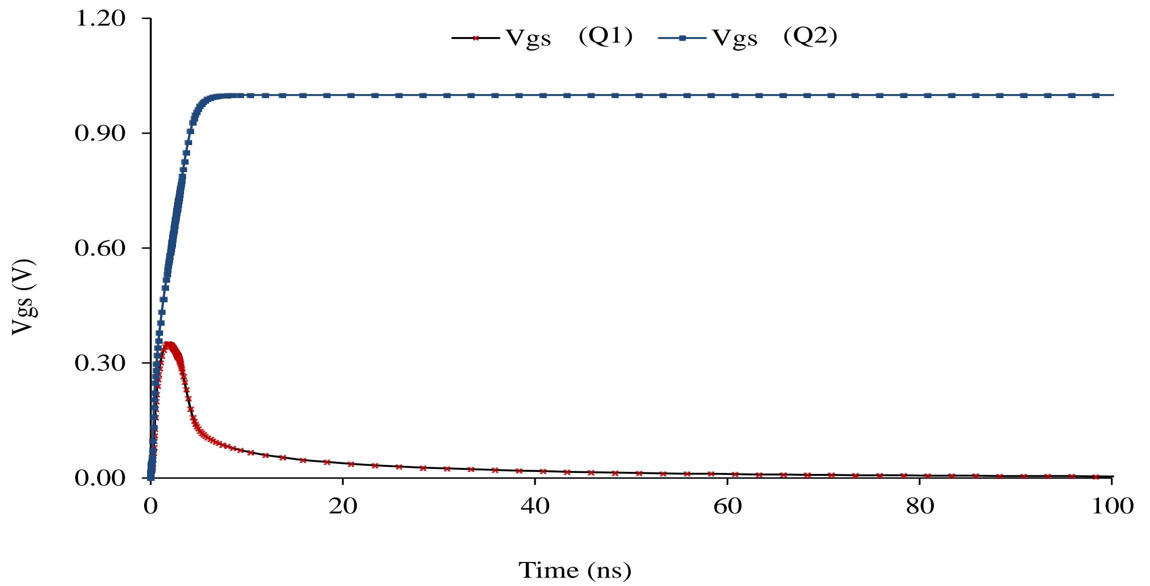


Figure 4.21: V_{gs} for Q_1 and Q_2, during discharge time.

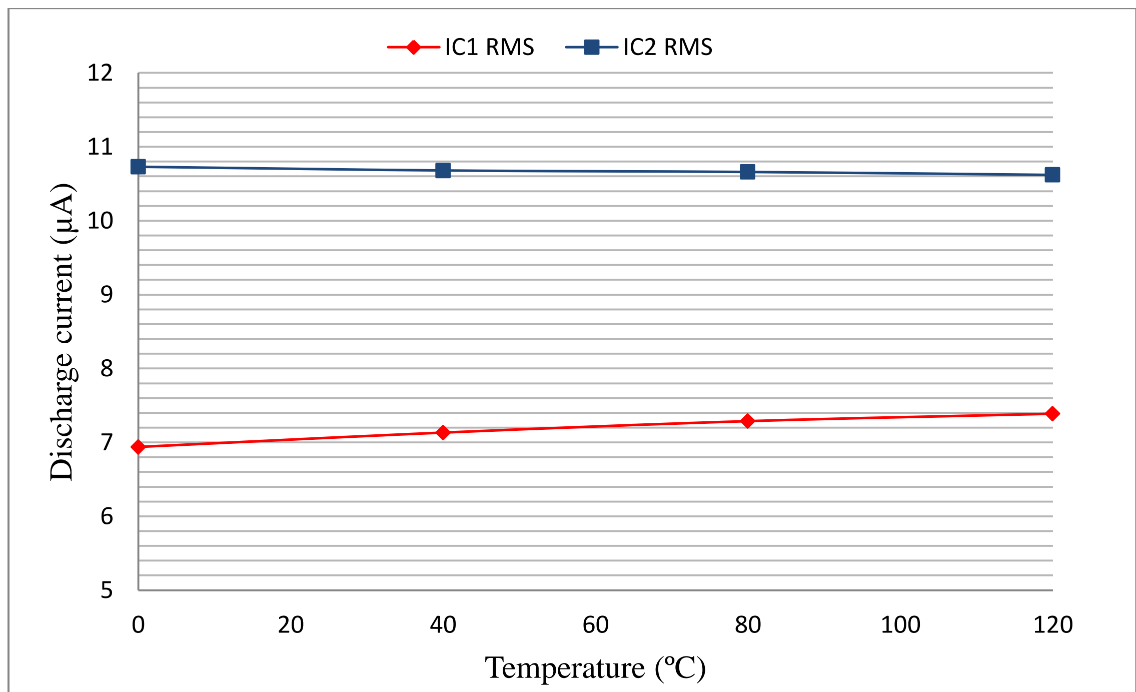


Figure 4.22: The discharge currents against the temperature-unbalanced charge pump load design.

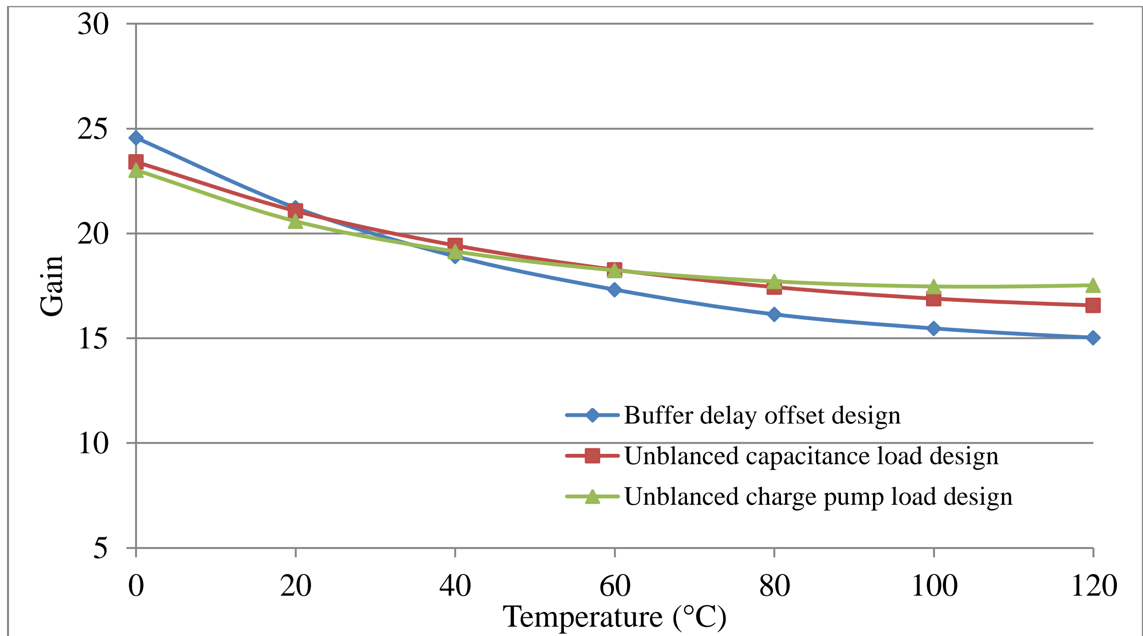


Figure 4.23: Variation of gain against temperature for the three time amplifier circuits using NAND gate with added resistance technique.

When the NAND gate with added resistance is used the gains of the three time amplifier circuits are degraded while the temperature is increased, as shown in Figure 4.23. The added resistance is implemented using an NMOS transistor, shown in Figure 4.6, where this transistor in each NAND gate, during discharge time, operates in the subthreshold mode resulting in a decrease in its resistance as the temperature is increased. The degradation in the added resistance has the same effect on the three time amplifier circuits which causes a reduction in the overall resistance of the discharge path (R_m), from Equation 4.5, resulting in a decrease in the gain.

4.5 Time Amplifier Power Supply Variation Analysis

The variation of the power supply can cause a considerable impact on circuit performance and hence design specifications, as described in Chapter 1, while the robustness of the design to these effects depends on the circuit configuration. Figure 4.24 illustrates the sensitivity of the gain, for the three time amplifier circuits, to the change in the supply voltage. It can be seen that the degradation in the voltage supply increase the gains of the unbalanced capacitance load and unbalanced charge pump load designs while it is decreased for the buffer delay offset design.

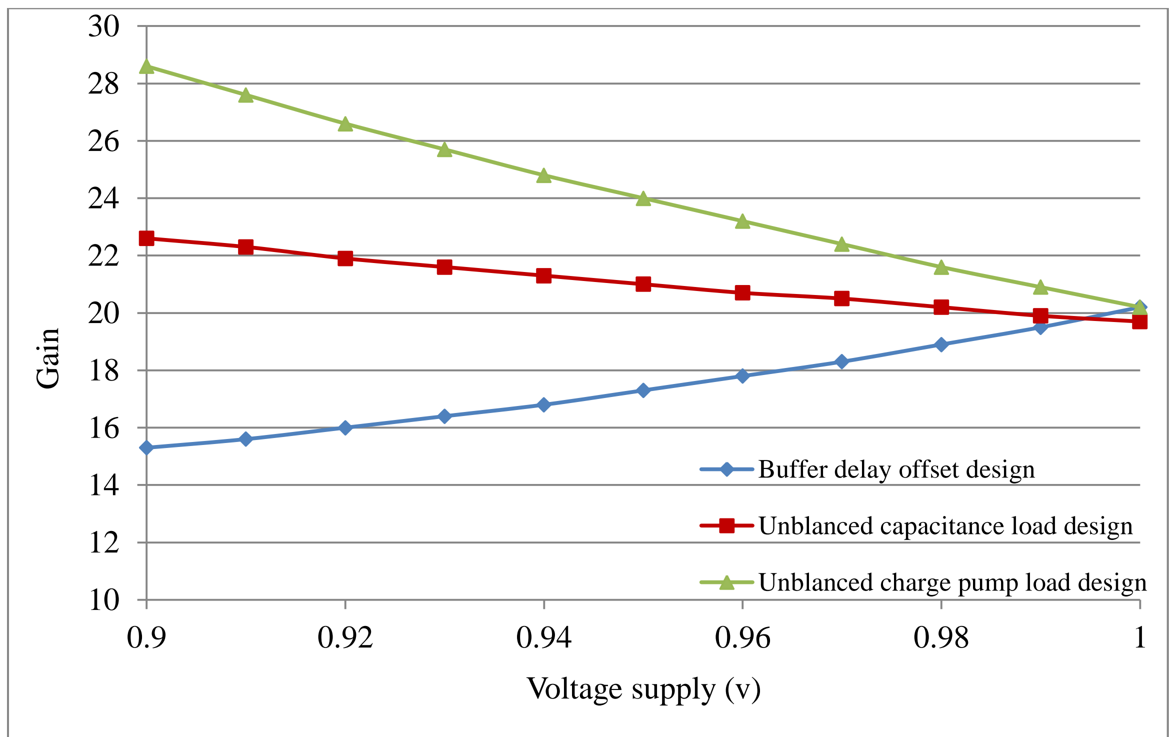


Figure 4.24: Variation of gain against the change in the supply voltage for the three time amplifier circuits.

In the unbalanced capacitance load design, when the voltage supply is decreased, the discharge time is increased although there is a reduced voltage on the capacitances. However, the reduction in the capacitance voltage leads to an increase in the resistance of the NMOS transistors in NAND gates creating a longer discharge time, as described in Chapter 3; V_{C1} controls the resistance of N_3 while V_{C2} controls the resistance of N_1. On the other hand, the increase in the gain for the unbalanced charge pump load design is larger than that for the unbalanced capacitance load design, as the supply voltage decreases. This is because the reductions in the voltage supply cause a reduction in the Vg of the Q_1 and Q_2 in the charge pump load which adds more resistance in the discharge path than the other design.

The opposite effect occurs regarding, the gain of the buffer delay offset design which is reduced as the voltage source is decreased. In this design, as the voltage source is reduced, the delay of the buffer, T_{off}, is increased leading to an increase T_{offset}, as shown in Figure 4.25. From Equation 4.5, the increase in T_{offset} results in a decrease in the gain.

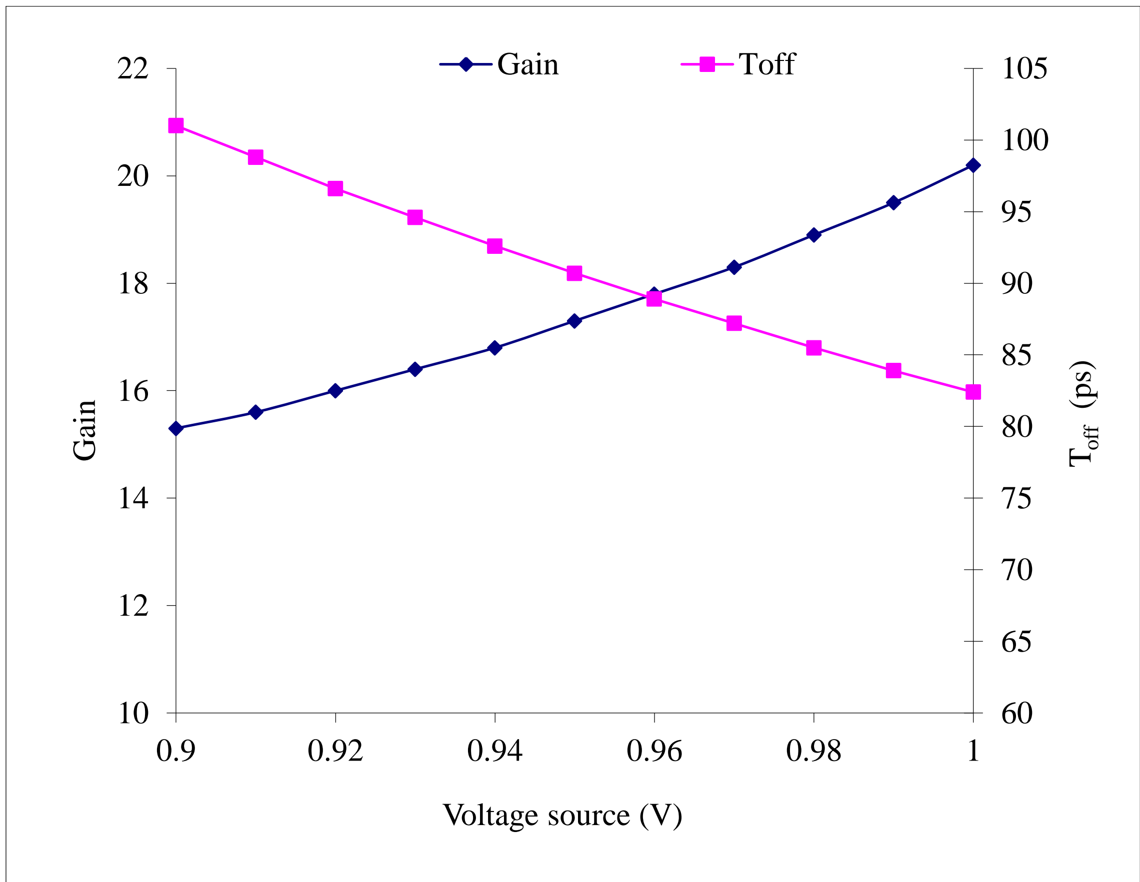


Figure 4.25: Variation in T_{off} and the gain against the voltage source-buffer delay offset design without using added resistance.

The effect of change the supply voltage for the three time amplifier circuits using the NAND gate with added resistance is similar to the effect on the gain without using the additional resistance, as shown on Figure 4.26. However, as the voltage source decreased, the amount of the increase in the gain value for the unbalanced capacitance load and unbalanced charge pump load designs is higher when the added resistance is in the discharge path. As previously discussed, the added resistance is implemented as an NMOS transistor, shown in Figure 4.6; the degradation in the voltage source leads to decrease the V_{gs} of this transistor which increases its resistance and hence the resistance in the discharge path resulting in a rise in the gain. In the buffer delay offset design, although the resistance is increased in the discharge path for the same reason, the gain is slightly decreased. This is because, the increase in T_{offset}, resulting from the decrease in the supply voltage, still has a greater impact on the gain value than the increase in the resistance in the discharge path.

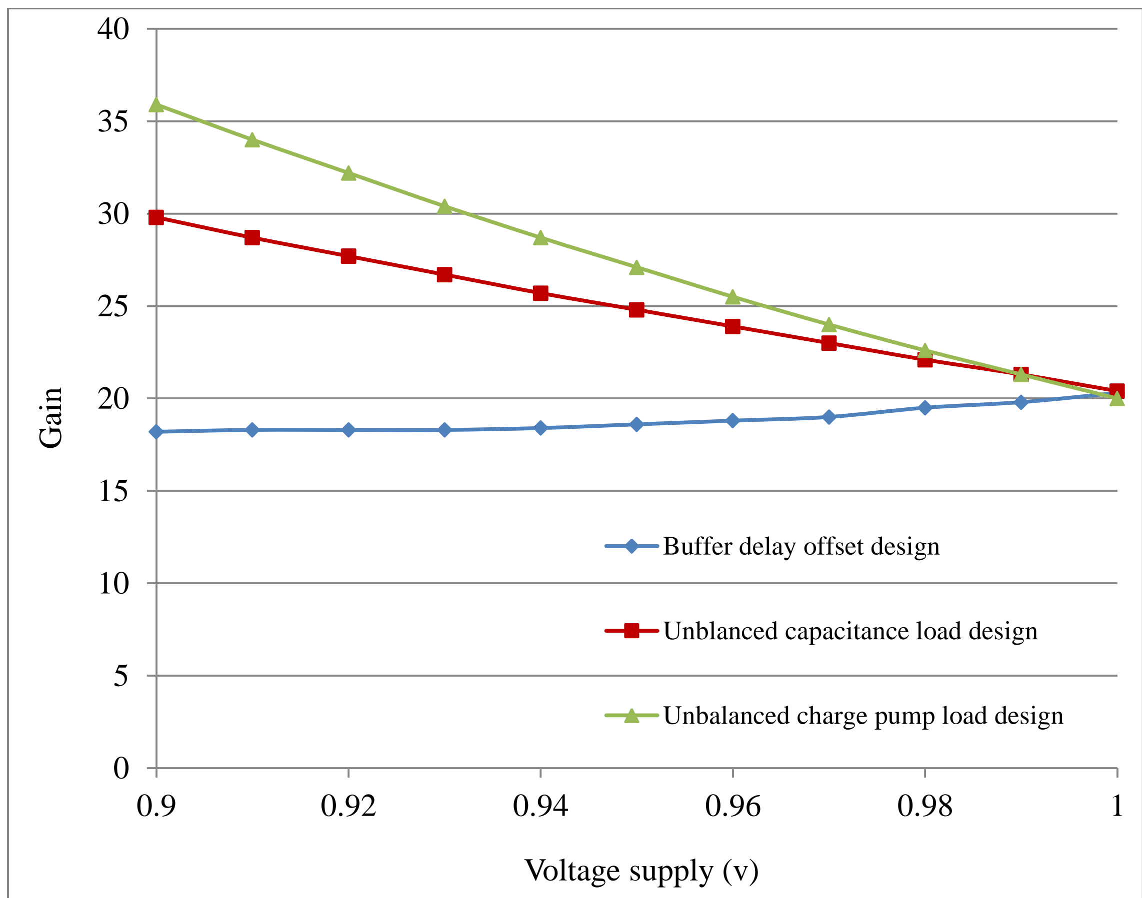


Figure 4.26: Variation of gain against the change in the voltage source for the three time amplifier circuits using NAND gate with added resistance technique.

4.6 Conclusion

In this Chapter, the robustness of the three time amplifier circuits, namely, buffer delay offset, unbalanced active capacitance load and unbalanced active charge pump load designs, to the effect of process, temperature and power supply variations was investigated. The results show that the gain of the unbalanced active capacitance load design is the least affected by process variations among the other designs. In addition, although, implementing the three time amplifier circuits using NAND gate with added resistance creates a huge improvement in terms of the dynamic input range, as discussed in Chapter 3, the gain sensitivity to the process variations is increased.

The effect of the temperature variation on the three time amplifier designs was also analysed. The gains of the buffer delay offset and the unbalanced active capacitance load are more robust to the effect of the temperature variation than the unbalanced active charge pump load design. However, as the temperature increases, the gain was decreased for the all designs when the NAND gate with added resistance is used.

Finally, in terms of the effect of power supply variation on the gain, the gains of unbalanced active capacitance load and unbalanced active charge pump load designs are increased as the voltage supply is decreased while it is decreased in buffer delay offset design. However, the increase in the gains were more in the unbalanced active capacitance load and unbalanced active charge pump load designs when the NAND gate with added resistance is used. On the other hand, there was a slight degradation in the gain of the buffer delay offset design, as the voltage source is decreased.

4.7 References

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Chapter 5

Reconfigurable Time Measurement Circuit

5.1 Introduction

Time interval measurement (TIM) has been used in several applications such as distance measurement, particle physics, astronomy, nuclear physics and dynamic testing of ICs. Typically, TIM is carried out using a Delay Locked Loop (DLL) [1], Vernier Delay Line (VDL) [2] and ring oscillator phase digitization [3]. A wide range of methods have been proposed, based on these techniques, in order to enhance the resolution, dynamic time range, area overhead, simplicity of calibration and measurement time [4-10]. Nevertheless, defining each of these parameters depends on the requirements of the diverse applications of the TIM. On-chip time measurement for built in self-test (BIST) is one of the critical integrated circuit tests which requires a high resolution TIM. However, as with all BIST schemes, the area overheads incurred is an important design issue. In this Chapter, a reconfigurable TIM with adjustable resolution and dynamic range is proposed which can be used for different measurement applications. The reconfigurable TIM is first configured to measure the time difference between two signals. However, after performing the measurement, the TIM circuit can be reconfigured to a different resolution and dynamic range in order to be reused for jitter, set-up and hold time measurements etc. Using a TIM with a reconfigurable resolution and dynamic range can be considered to consume less area overhead than specific TIM applications, as the same circuit is used for different functions and hence only one circuit needs to be calibrated.

The new reconfigurable TIM is all-digital and designed as a wide dynamic input range time difference amplifier with adjustable gain. The time amplifier is attached to a simple tapped delay line to create the new TIM. The tapped delay line comprises 32 cells where each cell consists of a single buffer delay and a D flip flop (DFF). The tapped delay line

is designed to have a resolution of 60 ps while the range of the time amplifier gain is designed to be adjustable from about 4 to 117 with a 7.5 increment. The results show that a resolution range of 15 ps to 0.5 ps with a dynamic range of 480 ps down to 16 ps can be achieved using 90 nm CMOS process.

The subsequent sections of the Chapter comprises an overview of the reconfigurable TIM in section 5.2, followed in section 5.3 with an outline description of the chip design, followed by the conclusions in section 5.4.

5.2 Reconfigurable TIM Circuit Overview

The design comprises two main parts, namely, a reconfigurable TIM and calibration circuits where the reconfigurable TIM, itself, comprises two parts, namely the programmable time amplifier and the tapped delay line, as shown in Fig. 5.1, each part of the design is described in detail below.

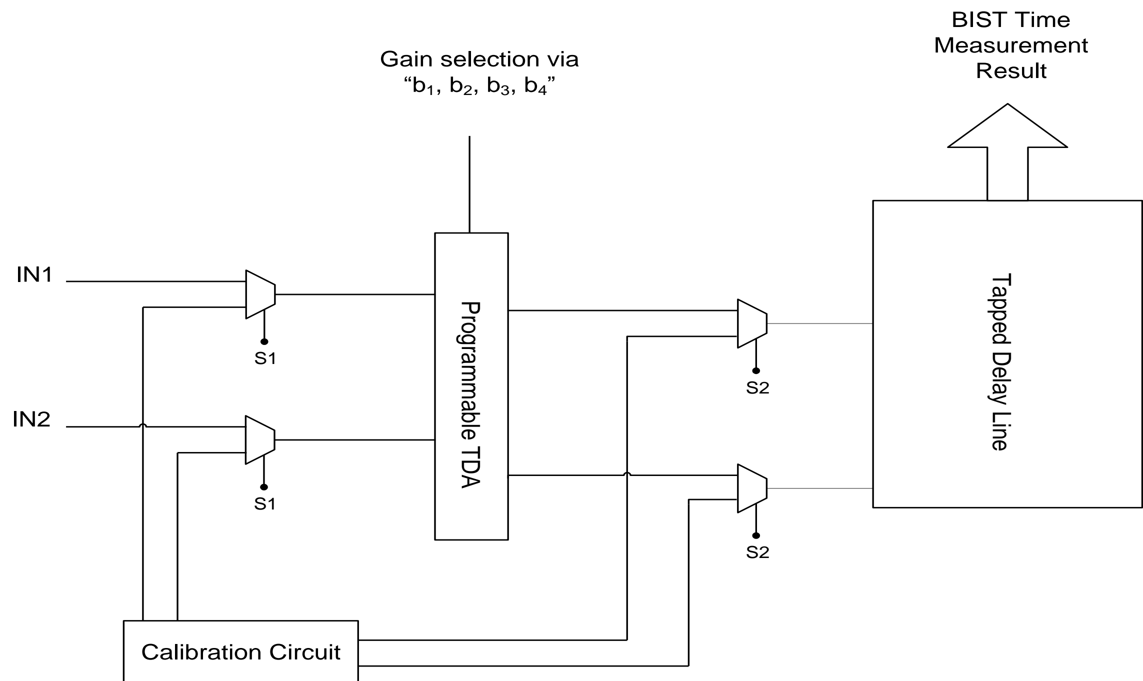


Figure 5.1: Block diagram of the reconfigurable TIM.

5.2.1 Reconfigurable TIM Circuit

The reconfigurable TIM circuit consists of two components, a programmable time difference amplifier and a 32 cell tapped delay line. Each stage of the delay line comprises a buffer delay, which, in this instance, is implemented

as an inverter pair, and a DFF, as shown in Figure 5.2. The resolution of the delay line is determined by the value of the buffer delay which is designed to be equal to 60 ps, as shown in the simulation results in Figure 5.3.

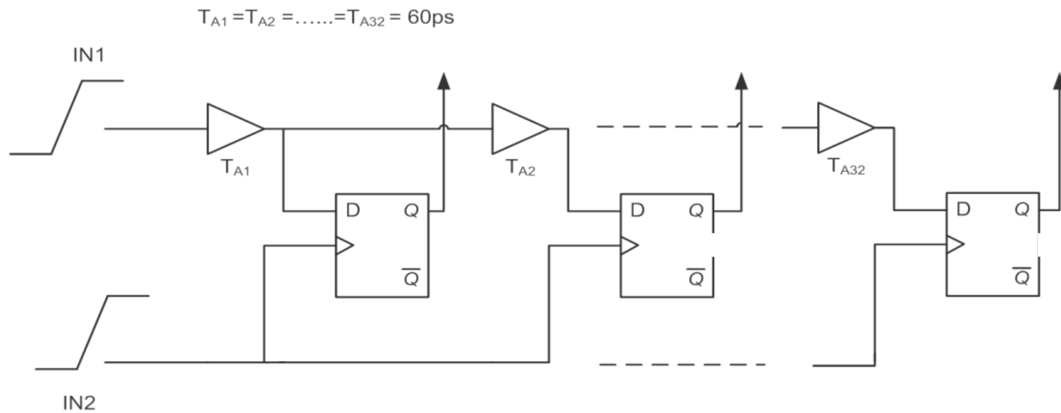


Figure 5.2: Block diagram of the tapped delay line.

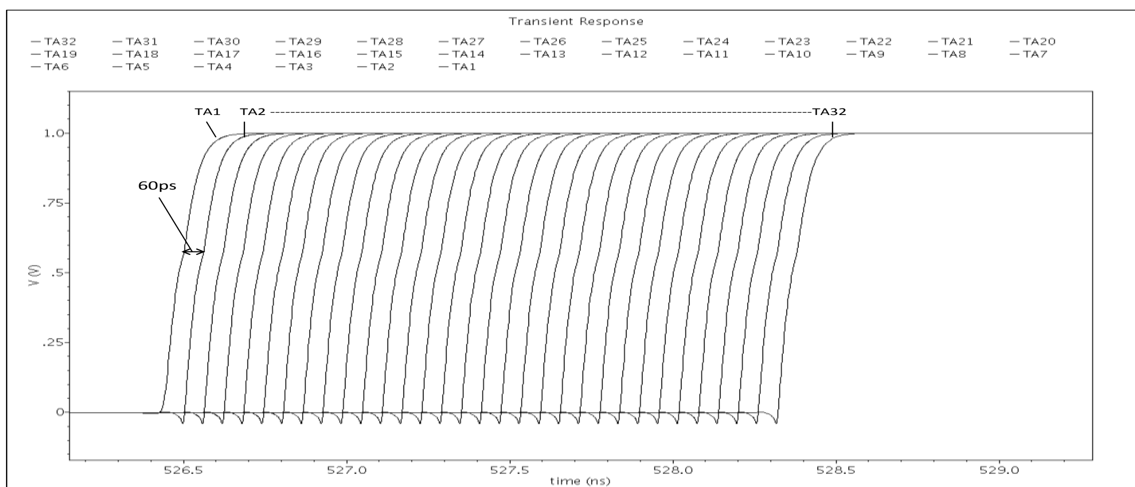


Figure 5.3: Spectre simulation results of the IN1 as it is propagated through the delay line.

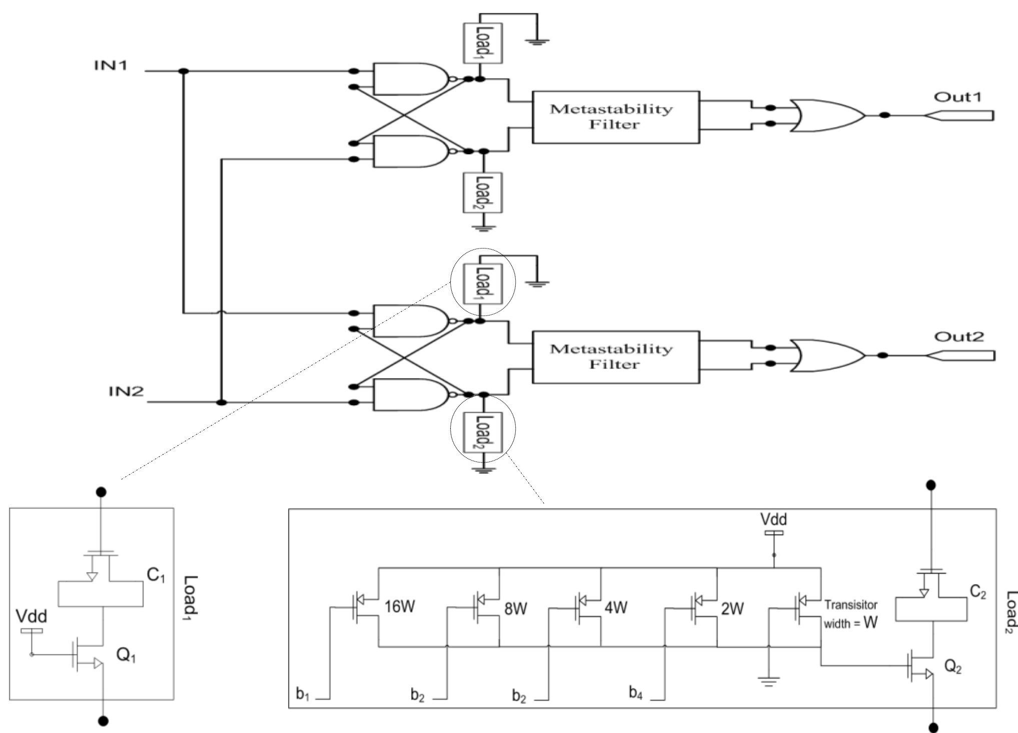


Figure 5.4: Programmable time amplifier circuit.

The programmable time amplifier has the flexibility to be adjusted to vary the gain in steps of 7.5, as discussed in Chapter 3. The programmable time amplifier is designed using the unbalanced active charge pump circuit with NAND gates with added resistance in the discharge path, shown in Figure 5.4, and has a wide dynamic input range of 300 ps.

The programmable time amplifier is attached to the tapped delay line to form the reconfigurable TIM circuit. The resolution of the reconfigurable TIM can be estimated using Equation (5.1). The gain of the programmable time amplifier is designed to be adjustable from approximately 4 to 117, as shown in Figure 5.5. The reconfigurable TIM, having 32 cells in the delay line, gives a resolution range of 15 ps to 0.5 ps which can be achieved with a dynamic range of 480 ps to 16 ps respectively.

Resolution = Delay line resolution / TDA Gain --- (5.1)

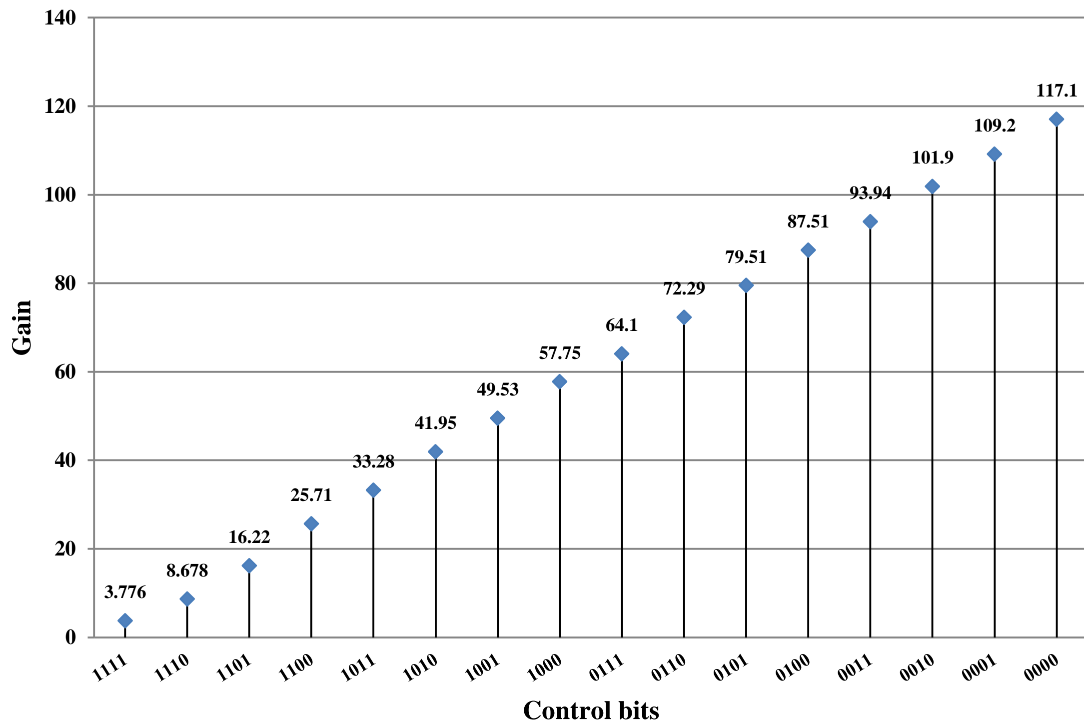
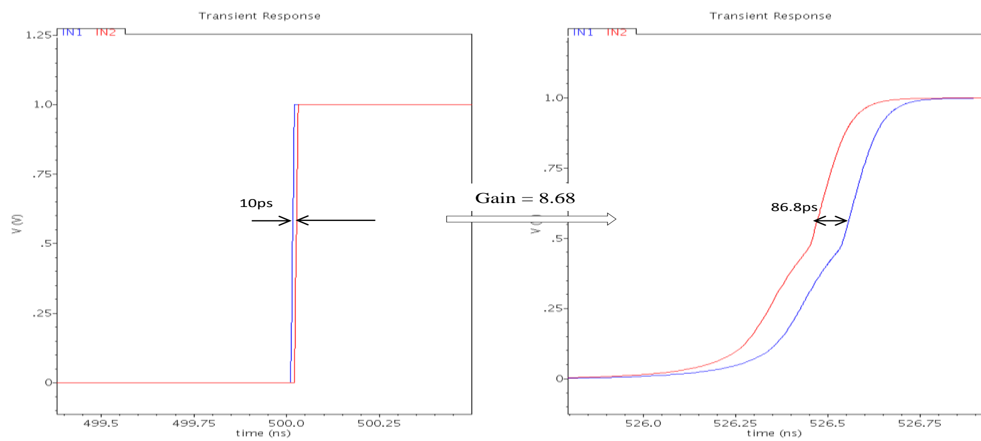


Figure 5.5: Programmable time amplifier gain versus Control Bit Pattern.

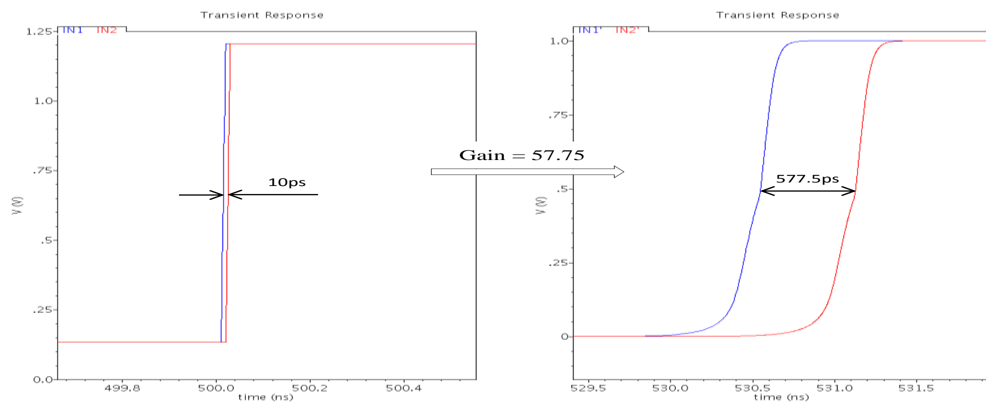
In time measurement mode, the TIM is programmed to the required resolution by adjusting the time amplifier gain while the signals under test, IN1 and IN2, are applied to the input of the time amplifier, as shown in Figure 5.1. The time amplifier amplifies the time difference between the input signals IN1 and IN2, which then passes through the tapped delay line. As both signals propagate through the circuit, the outputs of the DFFs are changed to a logic one as long as IN1 leads IN2. However, at a certain cell in the delay line, once IN1 lags IN2, the output of the DFF remains at a zero and the measurement is finished. The result of the time measurement can be calculated using Equation (5.2).

$$\Delta T_{input} = \text{number of the high states} \times \text{Resolution} \quad \text{--- (5.2)}$$

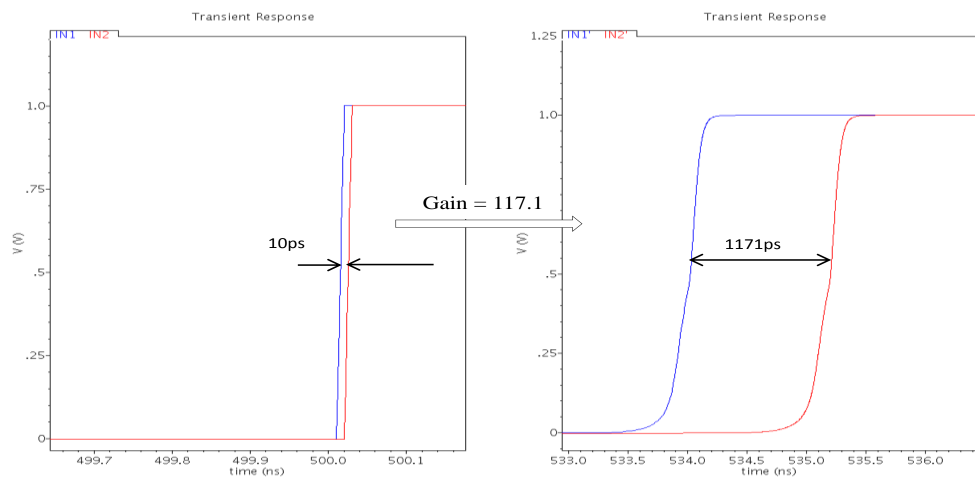
For example, Figure 5.6 and 5.7 show the result of applying IN1 and IN2 with ΔT_{input}=10 ps to the reconfigurable TIM for the control bits "1110", "1000" and "0000" (Figure 5.5) which create gains of 8.68, 57.75 and 117.1 respectively. From Figure 5.6, it can be seen that for ΔT_{input}=10ps, ΔT_{out} becomes 86.8ps, 577.5 and 1171ps, respectively, for the programmable bit settings, where ΔT_{out} is the time difference at the output of the time amplifier.



(a)



(b)



(c)

Figure 5.6: The result of the time amplifier for three gain values.

Figure 5.7 shows the result of time measurement for the gains 8.68 and 57.75, where for a gain of 8.68 the result was "100000000000000000000000000000". From Equation (5.1), the resolution in this case is calculated as:

$$\text{Resolution} = 60\text{ps} / 8.68 = 6.91 \text{ ps}$$

As the time measurement results show one cell set to a logic "1", then the measured ΔT_{input} is calculated as:

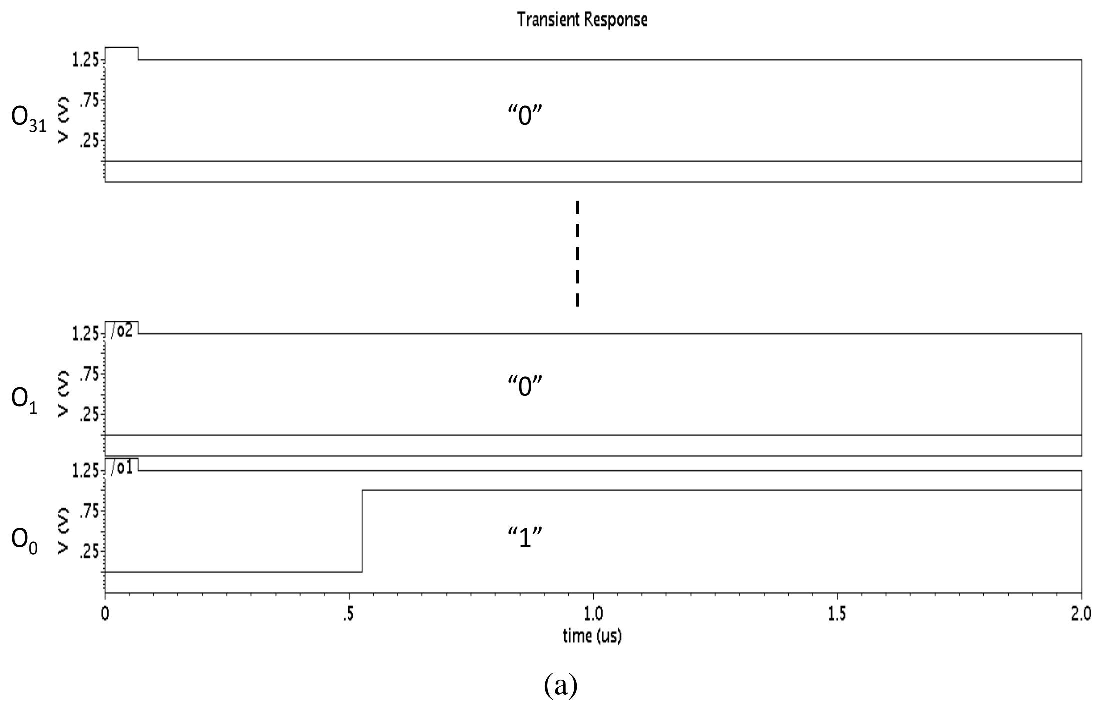
$$\Delta T_{input} \text{ (for a gain of 8.68)} = (1) \times 6.91\text{ps} = 6.91\text{ps}.$$

It can be seen that there is an error of 3.09ps in measuring a 10 ps time difference using a gain of 8.68. However, this error can be minimised by increasing the gain. A lower error was achieved from the result of the gain values "1000" and "0000" which have a resolution of 1.04ps and 0.51ps respectively. The result of the time measurement for gain "1000" was "1111111110…….0", as shown in Figure 5.7 (b). In addition the result of the time measurement for the gain value "0000" was "11111111111111111110…..0", as shown in Appendix B Figure B.1, leading to a measured ΔT_{input} values :

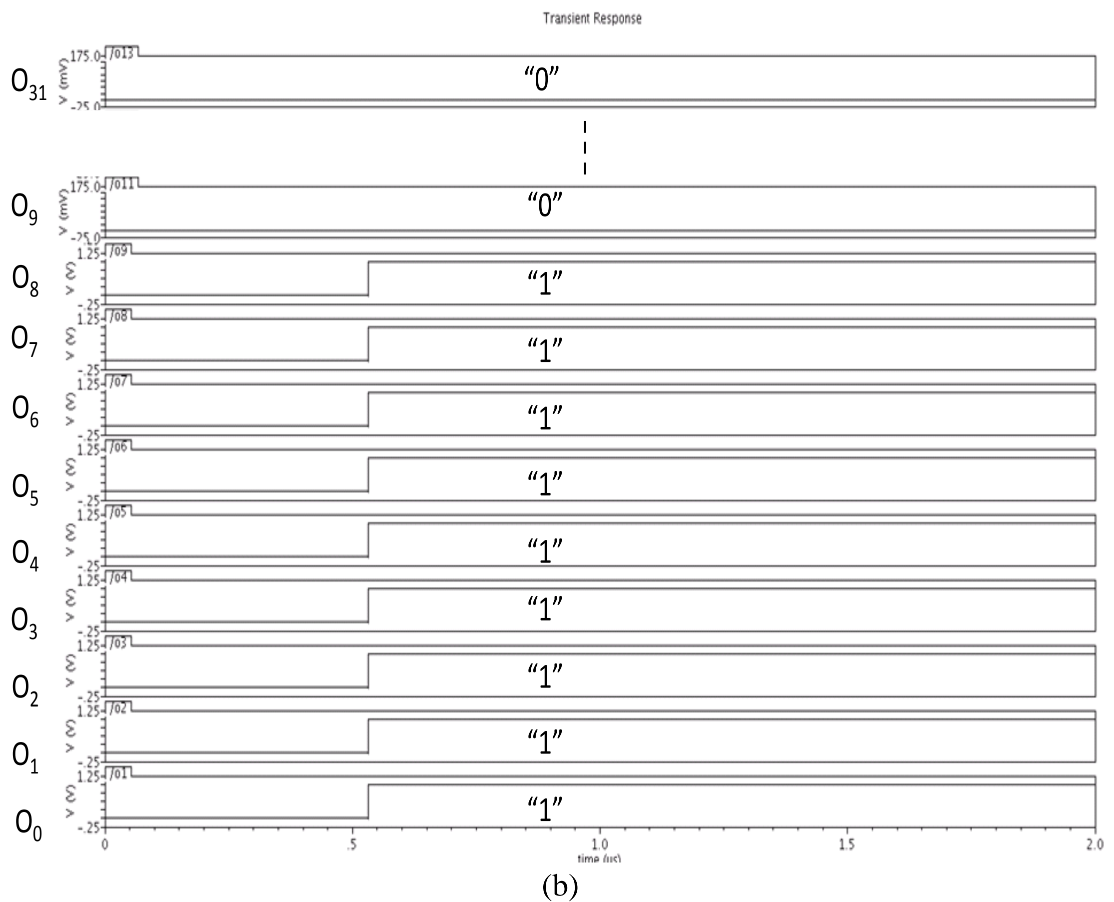
$$\Delta T_{input} \text{ (for a gain of 57.75)} = (9) \times 1.04\text{ps} = 9.36\text{ps}.$$

$$\Delta T_{input} \text{ (for a gain of 117.1)} = (19) \times 0.51\text{ps} = 9.69\text{ps}.$$

It can be seen from the result of using the gain of 57.75, the measured ΔT_{input} is very close to the exact value of ΔT_{input}, 10ps, with 0.64ps (6.4%) error while it is 0.31ps (3.1%) for a gain of 117.1. The gain value is chosen depending on the application, as mentioned previously, while although a gain of 8.68 provides a low resolution value, it has a large dynamic range, about 221 ps. However, for a gain of 57.75 and 117.1 the dynamic range is 33ps and 16 ps respectively.



(a)



(b)

Figure 5.7: TIM result for ΔT_{input}=10ps and gain value (a) 8.68 and (b) 57.75.

5.2.2 Calibration Circuit

Different methods have been proposed to calibrate time measurement circuits [11-14]. While some methods depend on using all on-chip calibration circuitry [13, 14], other methods are designed to have part of the calibration circuit off-chip [11]. As the objective of the calibration process is to maintain the accuracy of the measurement, the calibration circuit itself must be highly accurate; otherwise another circuit is required to check the calibration circuit. In calibrating time measurement circuitry, the critical parameter which is required to be accurately calibrated is the measurement resolution. However, as the measurement resolution has improved to be around 1ps, it becomes more difficult to calibrate such a high resolution. This is because in calibrating to 1 ps, or less, the effect of the process, voltage and temperature variation becomes a overriding issue, particularly when the procedure is done on-chip. However, for the partial on-chip calibration process, which is used to calibrate the reconfigurable TIM, the effects of process variations are minimised, as the on-chip part is based on an off-chip reference using a high frequency counter, as discussed later.

For the reconfigurable TIM, the resolution of the measurement is based on the gain of the time amplifier and the resolution of the tapped delay line. Thus the calibration process is divided into two stages. First, the tapped delay line is calibrated using a process similar to the calibration technique in [11] which depends on calibrating the delay line to known delay values. After calibrating the delay line, the gain of the time amplifier is measured using the calibrated delay line. The gain of the time amplifier is measured at more than one delay value where it is calculated as the average of the results. The error in calculating the gain can be minimised by adding more calibration points.

The calibration circuit consists of two variable delay lines where each delay line contains both a coarse and a fine step variable delay circuit. An external high frequency counter is also required for the calibration procedure. The variable delay values are measured by switching each variable delay line into a ring oscillator where their frequency is measured using the external high frequency counter. From the measured

frequency values the set variable delay values can be calculated. The block diagram of the calibration circuit is shown in Figure 5.8.

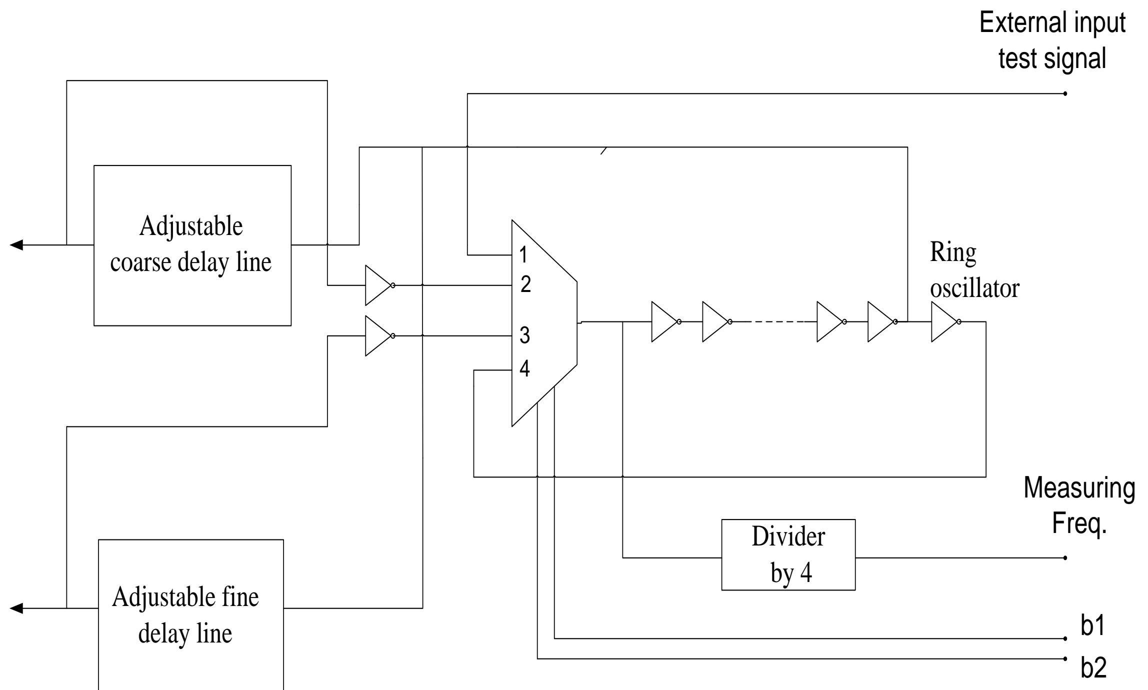


Figure 5.8: Block diagram of the calibration circuit.

The calibration circuit comprises a coarse step variable delay circuit, a fine step variable delay, a shift register, a ring oscillator, a divide by 4 circuit and an external high frequency counter which are discussed in detail below.

a) *The coarse step variable delay circuit:* The circuit for the coarse step delay is shown in Figure 5.9. As discussed in Chapter 2, the circuit contains a net of inverters which are connected through tri-state inverters which operate as switches in order to switch the delay elements in or out of the circuit. The delay of the circuit is adjusted in steps of the delay of two inverters. The simulation results for the coarse delay line are shown in Figure 5.10.

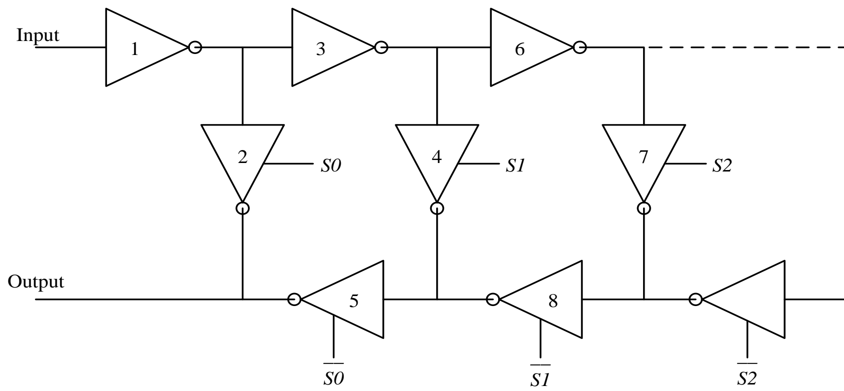


Figure 5.9: A simple adjustable coarse delay line [15].

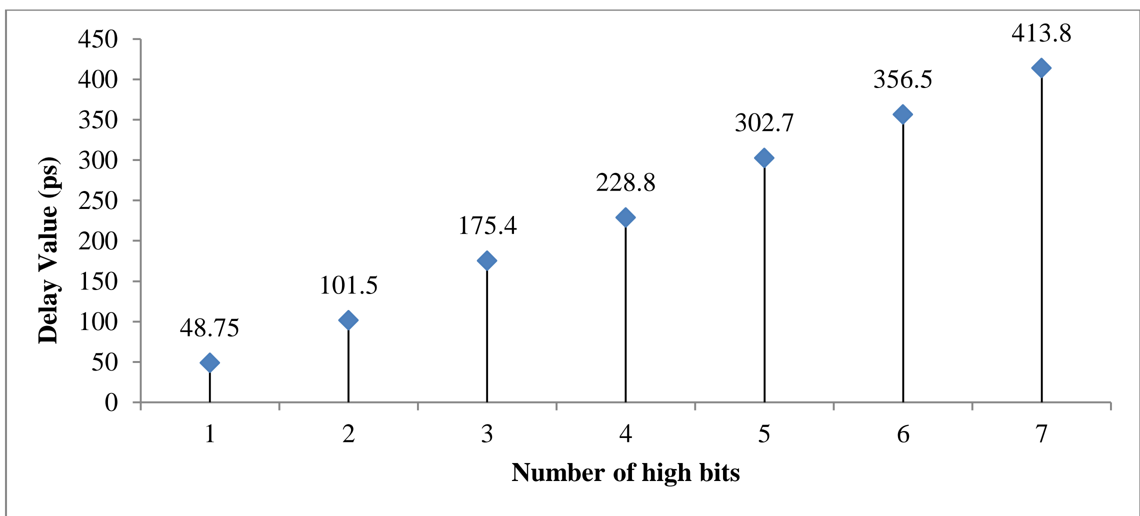


Figure 5.10: Simulation results for the adjustable coarse delay line.

b) The fine step variable delay: the fine step variable delay can be realised in several ways such as using a bank of parallel NMOS capacitances, an inverter matrix, the differential digitally-controlled delay cell and current starved delay element circuit, as described in Chapter 2. Two factors must be considered for the fine step delay line, namely, the linearity of the fine step and the sensitivity to the process variation. Thus, the parallel NMOS capacitances, the differential digitally-controlled delay cell and current starved delay element circuits were investigated regarding these two factors in order to choose the one to be used for the calibration process. The inverter matrix technique was not considered, as it consumed a large area overhead due to the requirement for a large number of delay elements. The remaining three fine step variable delay circuits are discussed below:

i) The parallel NMOS capacitance method depends on controlling the delay of the two inverters by adjusting the NMOS capacitance load which is connected to the node between the two inverters, as shown in Figure 5.11. The size of the NMOS capacitances are designed to be equal in order to obtain equal delay steps, where each step is designed to be equal to 1ps. From Figure 5.12, it can be seen that the delay step of the NMOS capacitances method has a high degree of linearity over its adjustable range.

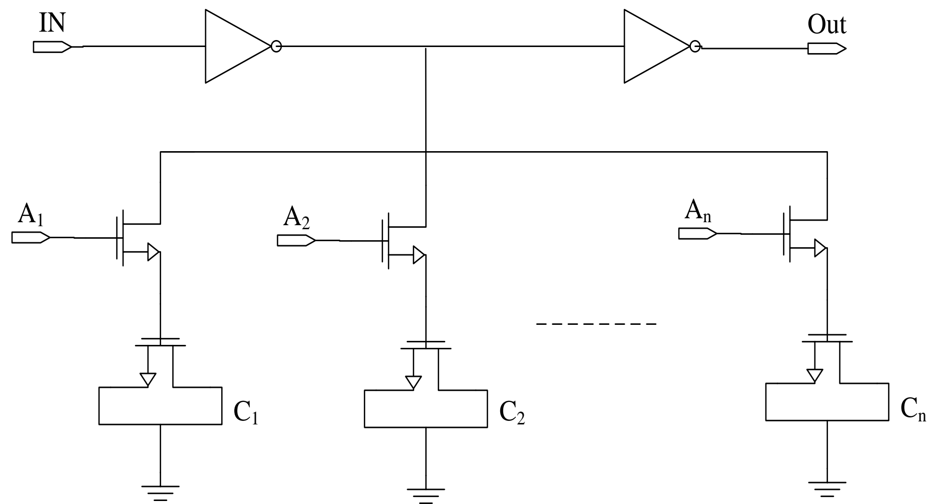


Figure 5.11: Adjustable fine delay line using parallel NMOS capacitances[15].

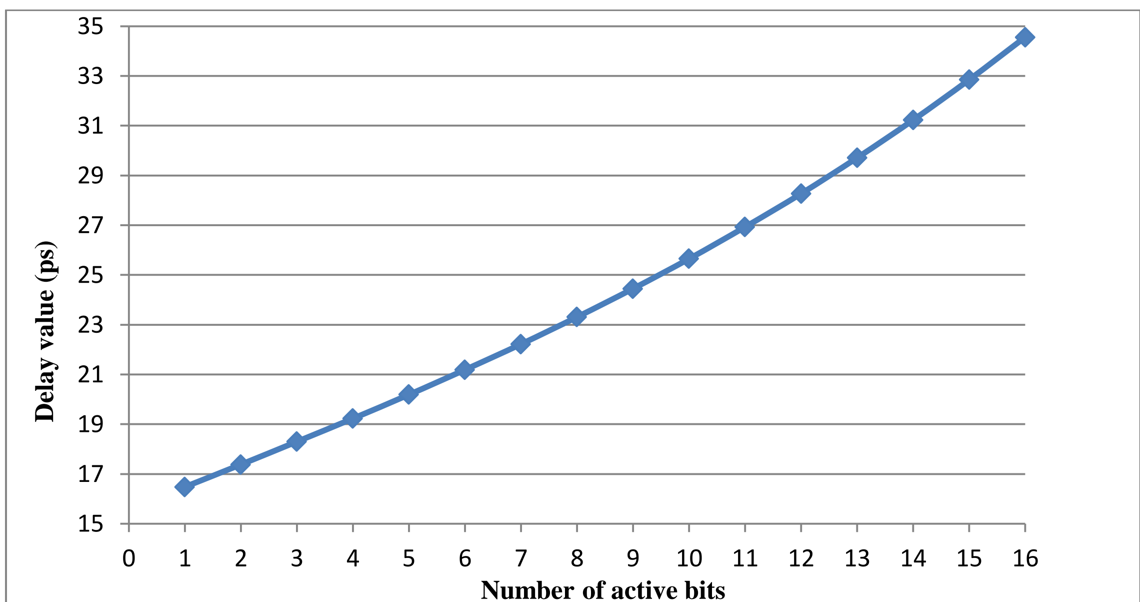


Figure 5.12: Linearity plot for the adjustable fine delay line using parallel NMOS capacitances.

ii) The differential digitally-controlled delay method comprises two inverters where their delay is controlled through adjusting the charge and discharge current of the two

inverters. The current is controlled by adjusting two variable resistances where one of them is placed between the voltage supply and the inverters, while the other is placed between the inverters and the ground, as shown in Figure 5.13. The variable resistance is formed from 16 transistors which are connected in parallel. These parallel transistors can be switched in and out of the circuit, switching more parallel transistors into the circuit reduces the overall value of the two variable resistances. The size of the parallel transistors is designed to achieve a step of 1ps.

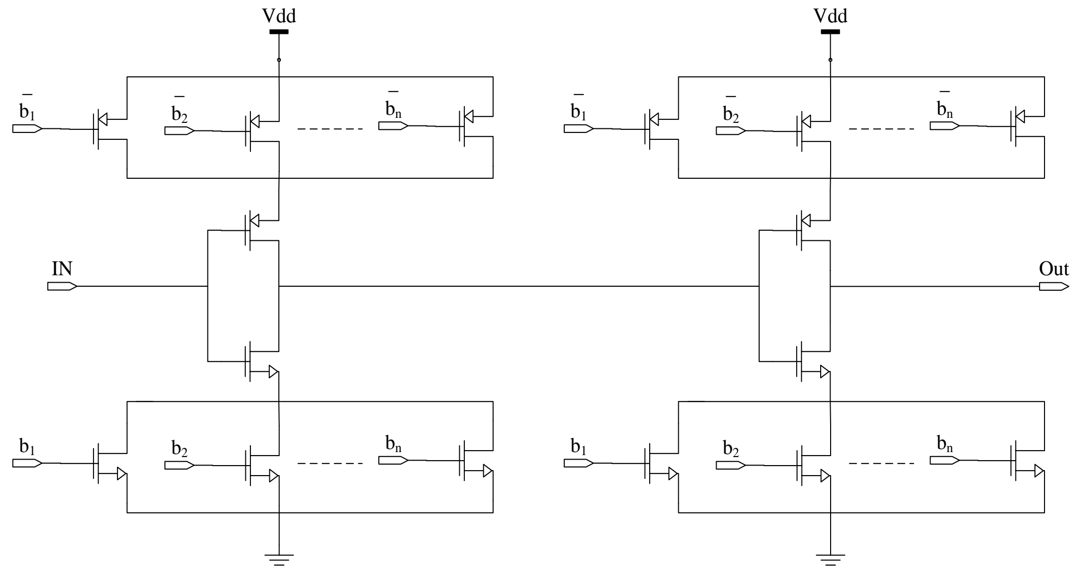


Figure 5.13: The differential digital-control delay cell [9].

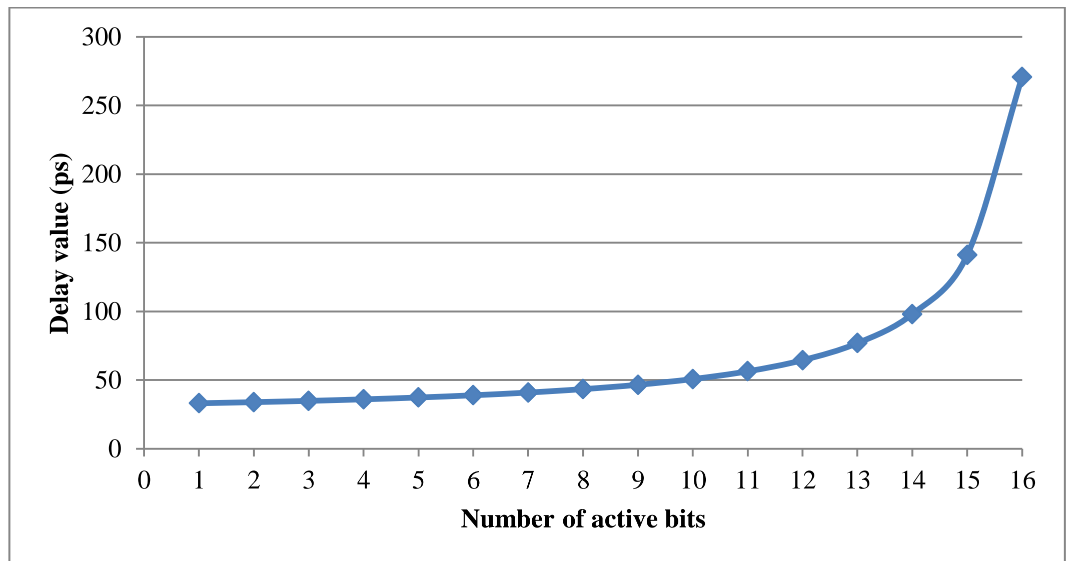


Figure 5.14: The result of the adjustable fine delay line using the differential digital-control delay.

From Figure 5.14, it can be seen that the delay step is only linear over a certain region, that is when up to 8 out of 16 bits are active (high). In the calibration process of reconfigurable TIM, the delay step is acceptable to be varied from 1 to 2.5 ps, as

within this variation the variable gains of the programmable time amplifier are covered in the calibration process. Thus the range from 1 to 8 of 16 bits is chosen as an acceptable range as the delay step in this range is varied from 1 to 2.5 ps. Comparing this with the parallel NMOS capacitance method, the delay step of the differential digitally-controlled delay method has much less linearity over the 16 bit range. As shown in Equation (5.3) [16], the estimation of inverter delay is based on the supply voltage, the drain saturation current $I_{D(S)}$ and the total capacitance, including the load capacitance. From this equation it can be seen the relationship between the capacitance and the delay is linear which explains the higher linearity of the delay step in the parallel NMOS capacitance method than the differential digitally-controlled delay method. As previously discussed, for the differential digitally-controlled delay method, the delay steps are controlled by increasing the resistance in two positions; first position is between V_{dd} and the inverters which adjusts the voltage value coming from V_{dd}, the other position is between the inverters and the ground which adjusts the discharge current of the inverter ($I_{D(s)}$). From Equation (1.1), the relationships between the delay and V_{dd} and $I_{D(s)}$ are not linear which explains the degradation in the linearity for the differential digitally-controlled delay method.

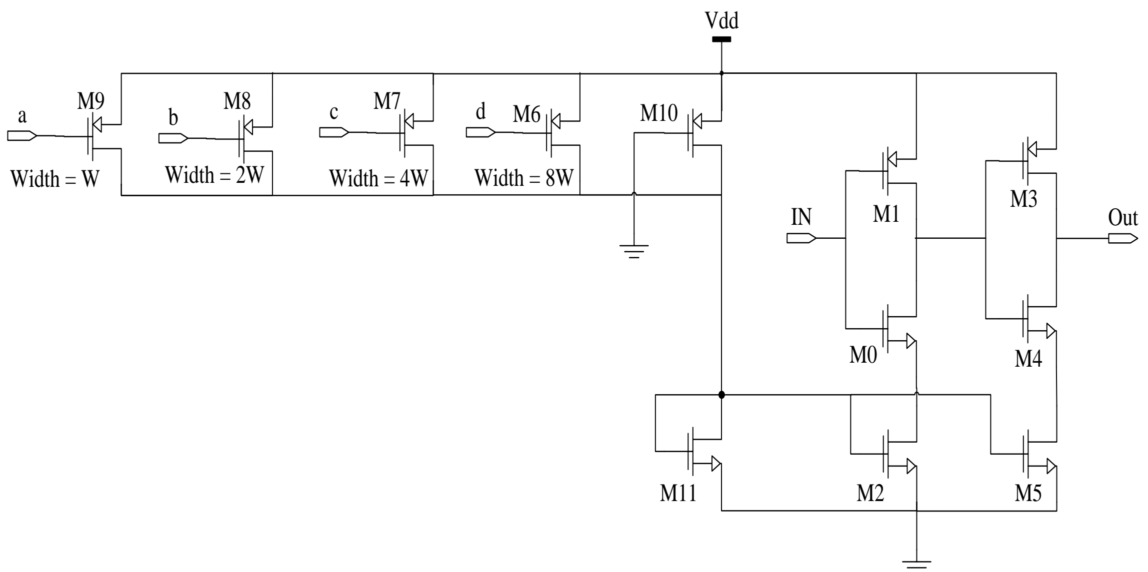


Figure 5.15: Current starved delay element [13].

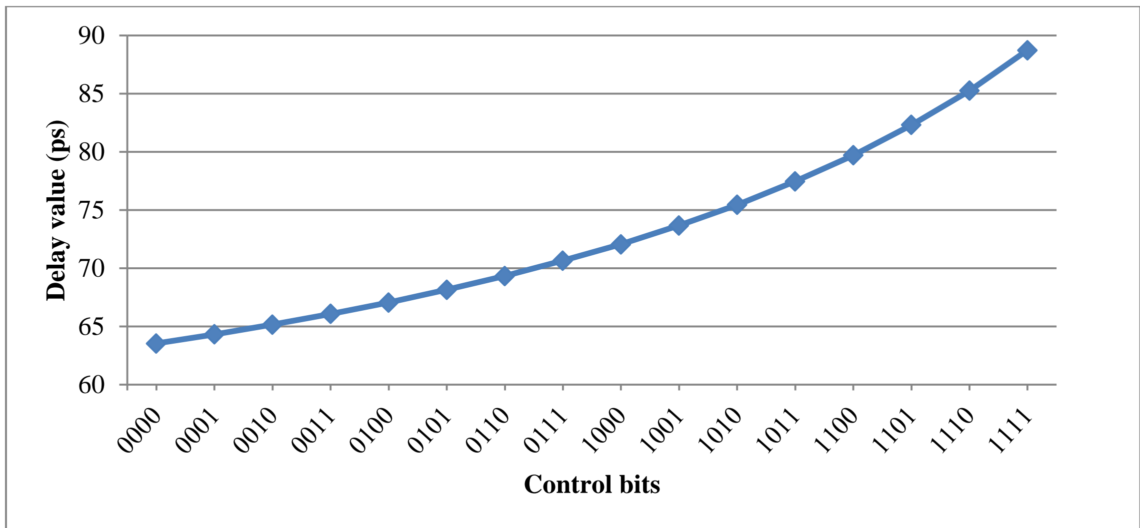


Figure 5.16: Linearity plot for the adjustable fine delay line using the current starved delay elements.

The current starved delay circuit is based on adjusting the delay of two inverters through controlling the charge and discharge of their currents, similar to the differential digital-control delay method. However, in the current starved delay circuit, the current of the two inverters is adjusted through the resistance of M2 and M5, as shown in Figure 5.15. This adjustment is achieved by tuning the gate voltage of M2 and M5 using four parallel transistors, M6, M7, M8 and M9. These transistors act as parallel resistances which can be switched in or out of the circuit digitally. The sizes of M6, M7, M8 and M9 are, again, designed to achieve a step of 1ps. From Figure 5.16, it can be seen that the delay step is only linear for the bit pattern range from '0000' to '1010', this range is wider than that of the differential digital-control delay, but less than that of the parallel NMOS capacitance method. The degradation in the linearity of the delay step for the current starved delay circuit is because it is controlled based on adjusting $I_{D(s)}$ which has a non linear relationship with delay, as shown in Equation (5.3). However, for a certain region, for the bit pattern range from '0000' to '1010', the linearity of this relationship is acceptable, as shown in Figure 5.16.

From the previous discussion, the delay step for the parallel NMOS capacitance method exhibits the best linearity over the complete 16 bit adjustable range among the three designs. It is important to mention that as all three methods depend on adjusting the delay of two inverters, the comparison among the three fine delay step circuits is undertaken using similar inverters for all methods; furthermore, in each case the delay adjustment was set to 1 ps.

In terms of studying the effect of the process variation on the three fine step variable delay circuits, the Monte Carlo analysis was used which was run considering 3σ process variation with 2000 samples at Vdd = 1V and temperature = 27°C.

Figure 5.17 shows the histogram plots for the delay step of the differential digitally-controlled delay circuit against process variation. It can be seen that the mean values of the delay variation were shifted with a fixed value, as the number of the delay steps is increased for control bit patterns set to less than 8 high bits while the mean values for the delay variation were shifted with a nonlinear step for control bit patterns of more than 8 high bits. In addition the standard deviation of the delay variation is increased as more bits are activated. This is because as more transistors are switched into the circuit the effects of the process variation are increased causing a greater variation in the inverter currents hence on the inverter delay.

In the current starved delay circuit, the mean values of delay variation were shifted with a fixed value as the number of the delay steps is increased, as shown in Figure 5.18. However, the linearity is degraded for the bit patterns greater than '1010'. It can be seen that the shift of the mean values of delay variation is related to the linearity of the delay step over the control bits range. Moreover, in the current starved delay circuit, as the number of delay steps is increased, the shift in the mean values of delay variation is fixed for a wider range than that for the differential digitally-controlled delay method. On the other hand the differential digitally-controlled delay is more robust in terms of delay variation than the current starved delay circuit, as it has a lower standard deviation value of the delay variation than the current starved delay. This is because the configuration of the circuit in controlling the delay for the current starved delay depends on tuning the gate voltage of M2 and M5 using four parallel transistors, M6, M7, M8 and M9, as discussed before, this increases the sensitivity to the process variation for even a slight change in the gate voltage on M2 and M5.

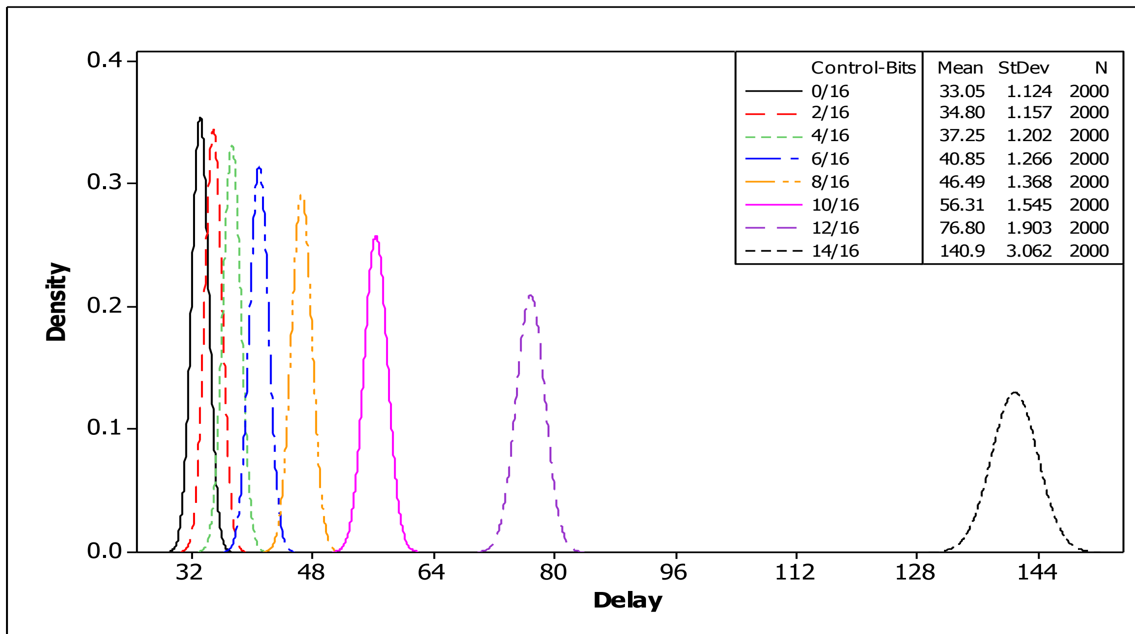


Figure 5.17: Histogram plots for the delay step of the differential digitally-controlled delay method against process variation.

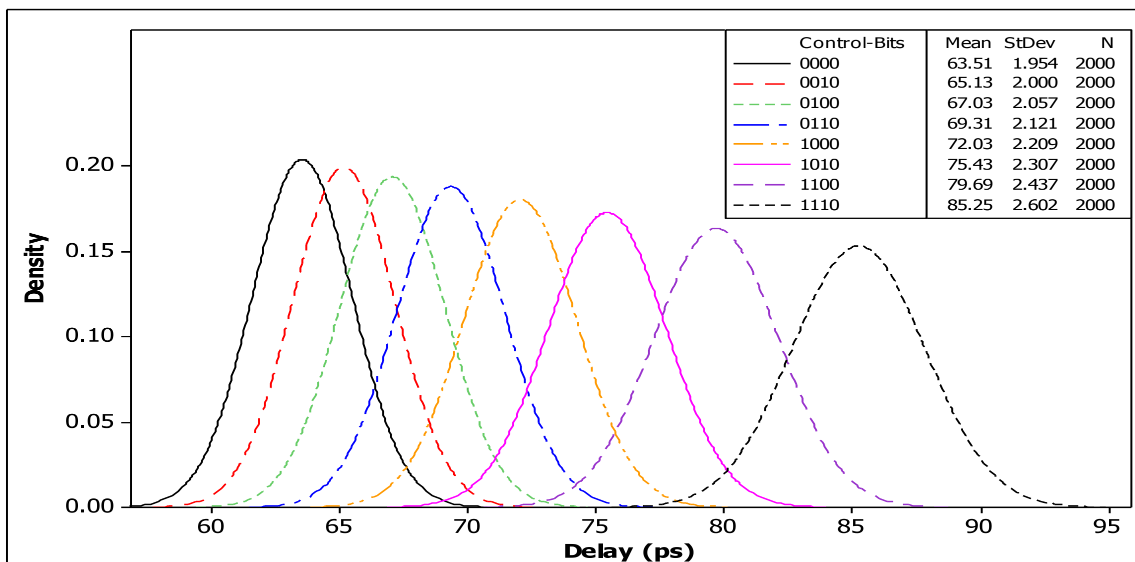


Figure 5.18: Histogram plots for the delay step of the current starved delay method against process variation.

The delay step for the parallel NMOS capacitance circuit is least affected by process variation among the three designs, as shown in Figure 5.19. It can be seen that the mean values of delay variation are shifted with a fixed value, as the number of the delay steps is increased over the full range of the input bit control patterns.

The previous study of the process variation is carried out using only a global variation method, die to die variation. This is because one reconfigurable TIM circuit is

implemented per chip while its transistors are implemented close to each other resulting in it being unlikely that the circuit will be affected by the process variation within a single die.

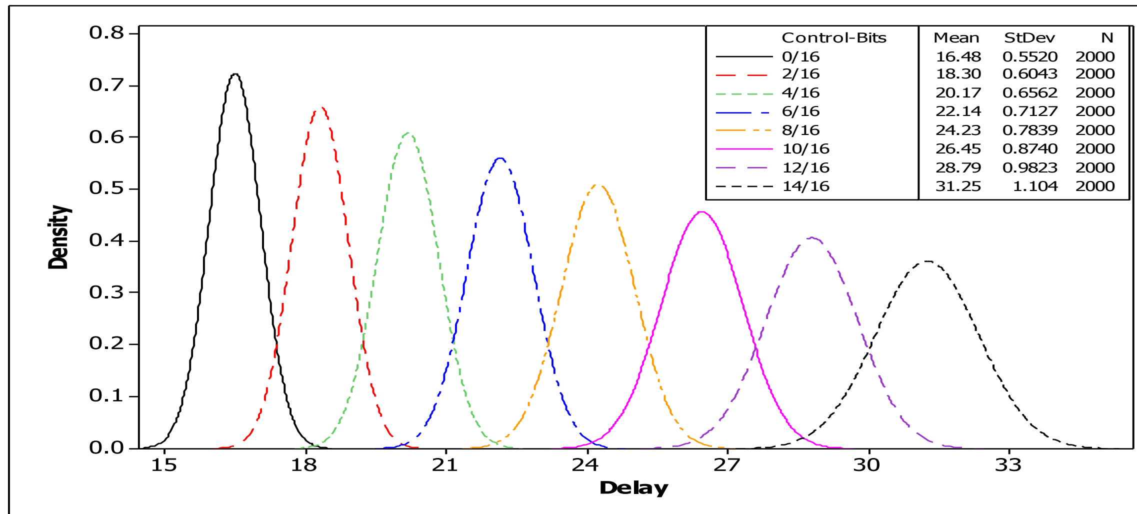


Figure 5.19: Histogram plots for the delay step of the parallel NMOS capacitances method against process variation.

The effect of the temperature variation on the three fine step variable delay circuits was also studied, as the sensitivity of the delay and delay step, and hence calibration process, can be affected by the temperature variations. At the outset, it is important to highlight two terms; first, the delay step which means the incremental value in the delay, second, the circuit delay which represents the whole circuit delay including the delay step.

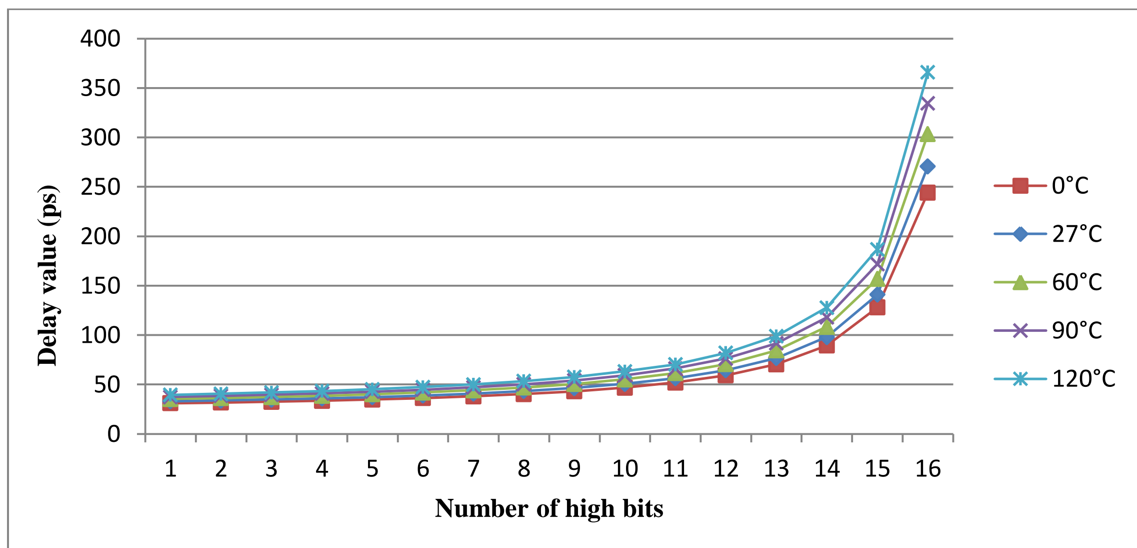


Figure 5.20: Variation of the delay for the differential digital-control delay against temperature.

For the differential digital-control circuit delay the temperature has a considerable effect on both the circuit delay and the delay steps, as shown in Figure 5.20 the circuit delay is increased as the temperature is increased. In addition the linearity of the delay step is degraded as the temperature is increased. For example, at 0°C the delay step is linear over a region from 0 to 9 active bits while it is up to 7 active bits when the temperature was 120°C.

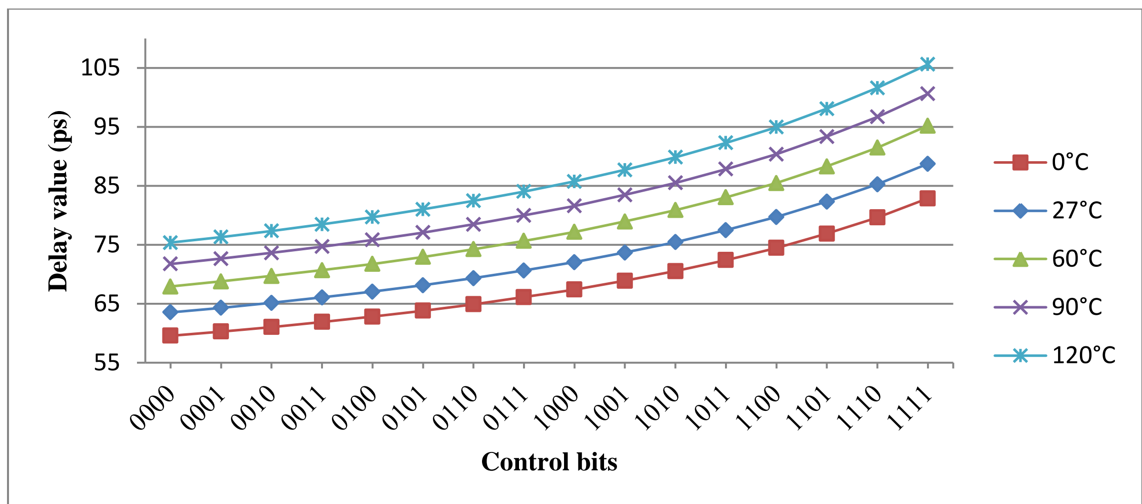


Figure 5.21: Variation of the delay for the current starved delay circuit against temperature.

From Figure 5.21, it can be seen that the delay of the current starved delay circuit is increased as the temperature is increased. In addition there is a slight degradation in the linearity of the delay steps as the temperature is increased. However, the effect of the temperature variation on the delay steps linearity for the current starved delay circuit is less than that for the differential digital-control delay circuit.

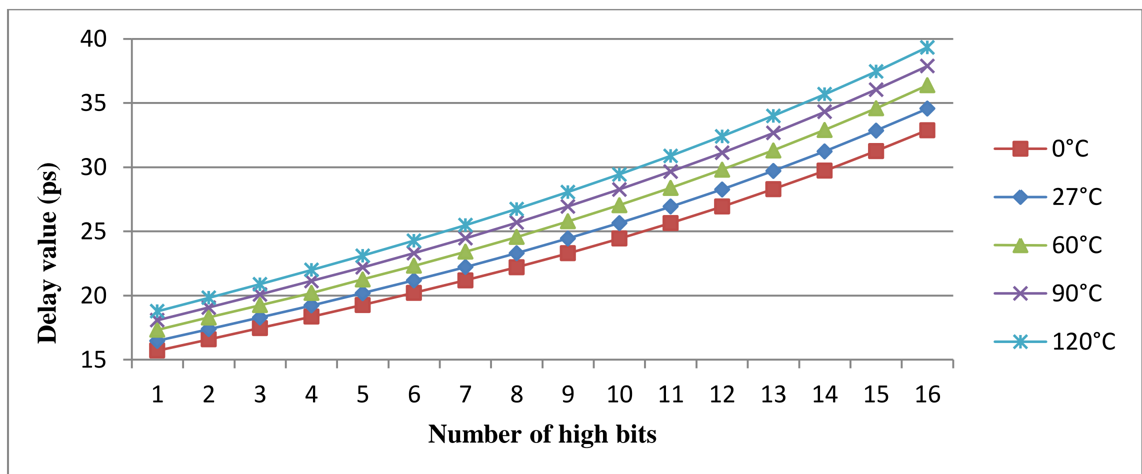


Figure 5.22: Variation of the delay for the parallel NMOS capacitances against temperature.

The least effect of the temperature on the delay step linearity among the three circuits was in the parallel NMOS capacitance circuit. Figure 5.22 shows a slight degradation on the delay step linearity as the temperature is increased.

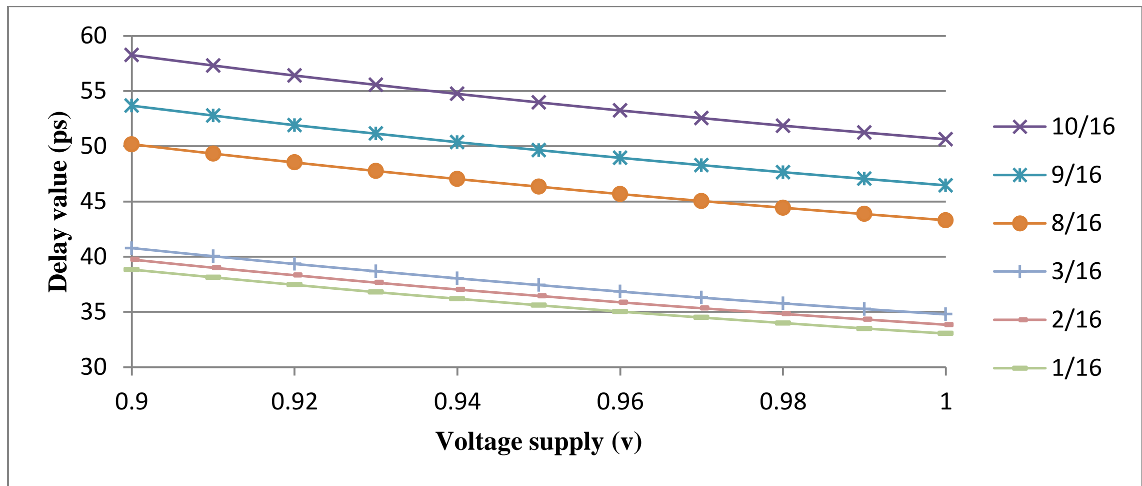


Figure 5.23: Variation of delay against the changes in the supply voltage for the differential digital-control delay circuit.

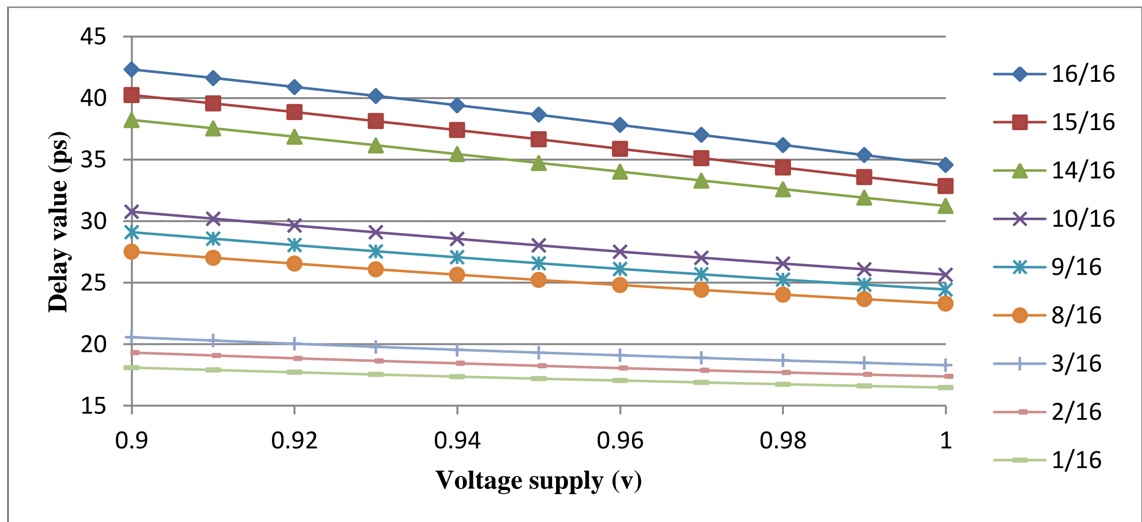


Figure 5.24: Variation of delay against the changes in the supply voltage for the parallel NMOS capacitances circuit.

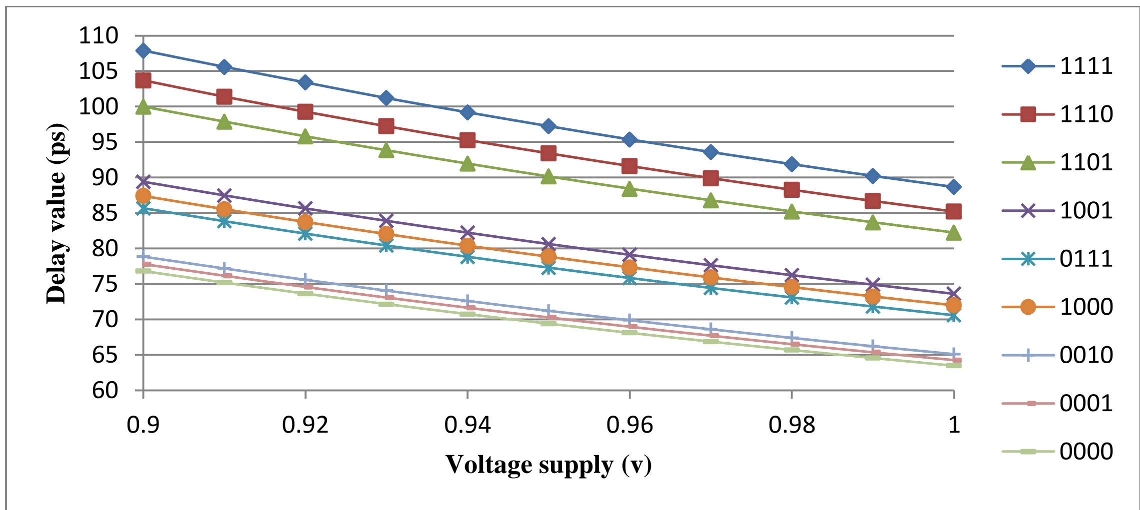


Figure 5.25: Variation of delay against the changes in the supply voltage for the current starved delay circuit.

Figures 5.23, 5.24 and 5.25 show the sensitivity of the delay steps for the three fine step variable delay circuits to the change in the supply voltage. It can be seen from Figure 5.23, the circuit delay is increased as the voltage supply is decreased while the delay step between the bit patterns 1/16, 2/16 and 3/16 is nearly fixed at 1 ps, as the voltage supply is decreased. However the delay step is nearly fixed at 2.5 ps for the bit patterns 8/16, 9/16, and 10/16 whereas this change in the delay step around the bit patterns 9/16 is because of the degradation in the linearity of the delay step, as discussed before. It can be construed that there is a considerable effect of the supply voltage variation on the delay circuit while there is nearly no effect of the supply voltage variation on the delay step. As previously discussed, Equation (5.3), The degradation on the voltage (V_{dd}) affects the delay of the inverters which forms the buffer delay in the differential digital-control circuit, as shown in Figure 5.13, hence, the delay circuit for this design is affected. However, as the configuration circuit for adjusting the delay is based on the resistances of transistors which are connected in parallel, the change in the V_{dd} in the range of 10% has nearly no affect on this resistance. From Figures 5.24 and 5.25, it can also be seen that the change in the supply voltage has affected the circuit delay while there is nearly no effect on the delay step, as the adjusted resistance and load for both design have not been affected by the change of V_{dd} in the range from 1V to 0.9V .

From the previous discussion, it can be concluded that the delay step of the parallel NMOS capacitance circuit has the greatest linearity in delay step and is the most robust to the effect of process, voltage and temperature variation regarding its impact on delay

among the three designs. Therefore it is used in the calibration process of the reconfigurable TIM.

c) Other calibration circuit components: Figure 5.26 shows the complete calibration circuit for the reconfigurable TIM. The picosecond test signal generator comprises two controllable high resolution delay lines; each delay line consisting of a fixed and adjustable section. One of the delay lines is designed to generate a large delay step while the other generating a fine delay step. In the fine step delay line, the delay step is designed to be 1 ps starting from 16.5 ps to 31.5 ps. However, in order to make the difference at the output of the delay line equal to the step delay value, a fixed delay line is added with a delay value equal to 15.5 ps. On the other hand, the coarse step delay line the value of the fixed delay section is designed to generate a step delay around 60 ps starting from 32 ps to nearly 400 ps. The step values of both controllable delay lines are designed to cover the calibration of the gain values. Each section of the controllable delay lines can be switched into a ring oscillator in order to measure the delay steps. An external high frequency counter is used to measure the frequency of the ring oscillator in order to calculate the delay steps. In addition two shift registers are used to control the input bit pattern of the picosecond test signal generator, as shown in Figure 5.26. The calibration process is discussed in more detail in the next section.

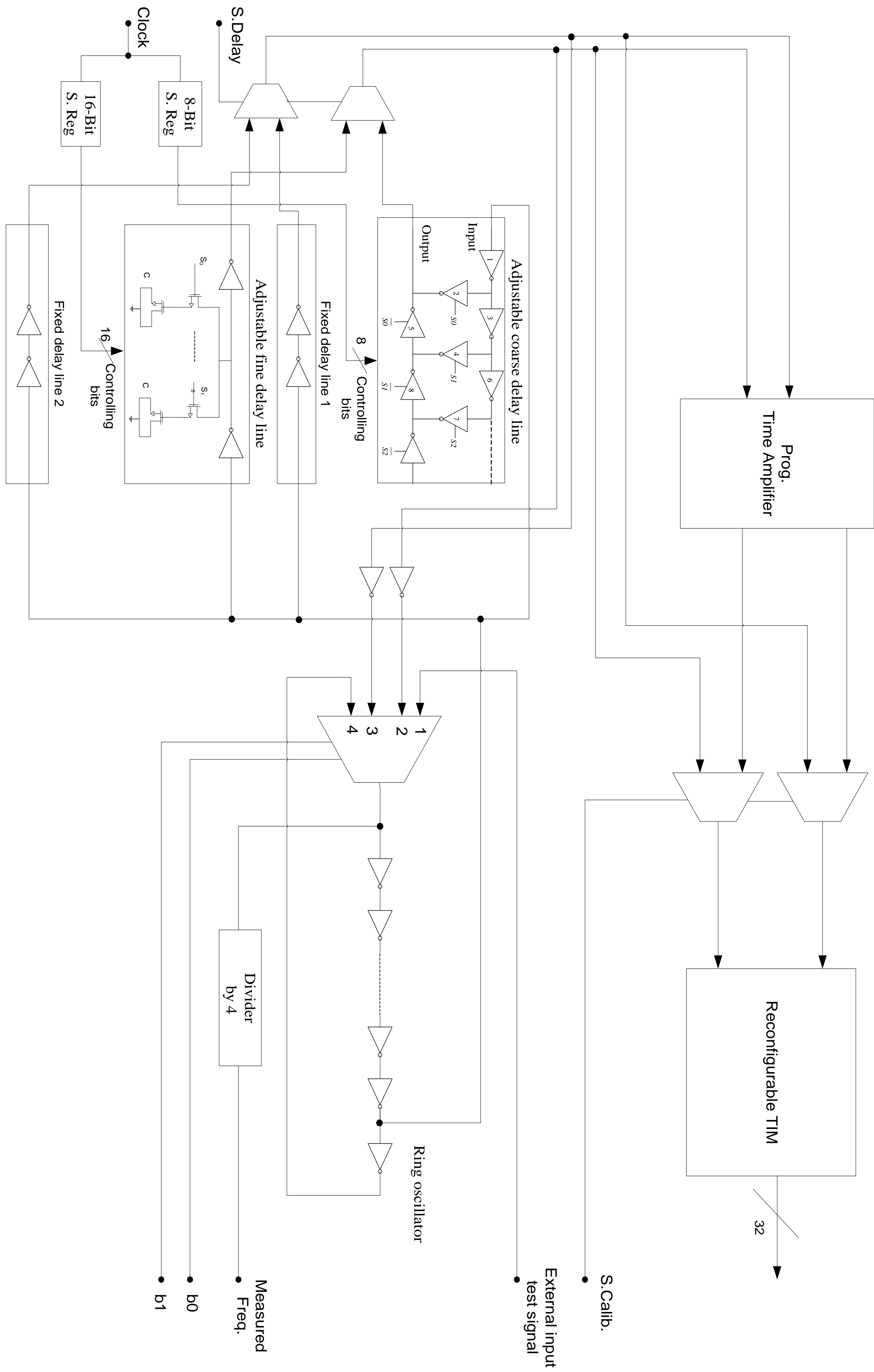


Figure 5.26: The calibration and reconfigurable TIM circuits.

5.2.3 Calibration Process

The complete circuit for the reconfigurable TIM is shown in Figure 5.26. The calibration process is started by calibrating the tapped delay line using the adjustable coarse delay block. The coarse delay block consists of fixed and adjustable sections; the adjustable section comprising a coarse step delay cell and a fine step delay cell where the fine step delay is used to correct the adjustment of the delay line with an increment of 1 ps, as shown in Figure 5.27.

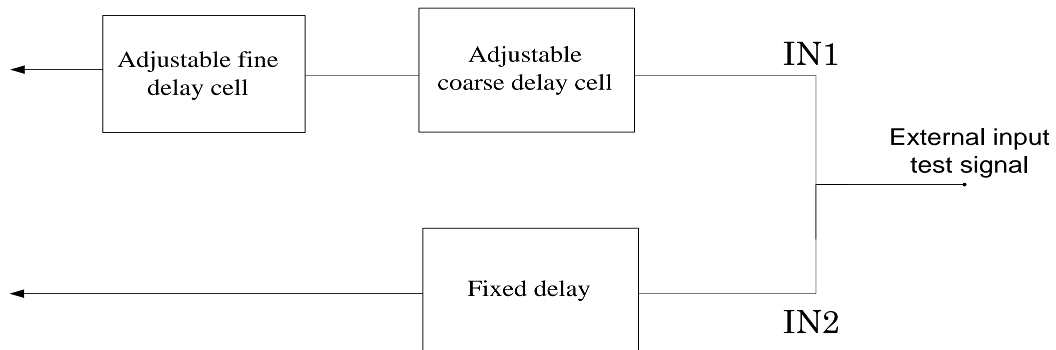


Figure 5.27: Block diagram of coarse delay block.

The calibration of the tapped delay line is started by applying an external test signal to the coarse delay line; at the input of the coarse delay line the test signal is split into IN1 which passes through the adjustable section and IN2 which propagates through the fixed section. At the output of the coarse delay block, two test signals are generated with ΔT_{input} equal to the adjusted delay value. For example, if the tapped delay line is calibrated with ΔT_{input} =101.5 ps, the resolution of the tapped delay line is calculated using Equation (5.4). However, as the tapped delay line is designed to have a resolution of 60 ps the time measurement result shows only one high bit, (0……….01).

$$\text{Tapped Delay Resolution} = \frac{\Delta T_{input}}{\text{Number of High Logic value in the output of the TIM}} \quad \text{--- (5.4)}$$

Tapped Delay Resolution = 101.5 ps / 1= 101.5 ps

It can be seen that there is a large error in determining the resolution value as ΔT_{input} has a value in between 60 ps and 120 ps hence in order to avoid this error a fine step delay cell was added to the coarse delay cell to increase the ΔT_{input} by fine steps (1 ps). This increase in the ΔT_{input} is continued until the time measurement result shows two high bits, (00000000000000000000000000000011). The new ΔT_{input1} is measured and has a value equal to 122.2 ps; hence the resolution can be calculated as shown below.

$$\text{Tapped Delay Resolution} = 122.2 \text{ ps} / 2 = 61.1 \text{ ps}$$

One important part in the calibration procedure is the method of measuring ΔT_{input} which depends on measuring the difference between the delay of the fixed and adjustable sections in the coarse delay block. From Figure 5.26, the fixed and adjustable sections can be switched into the ring oscillator loop where the signal which is generated from this ring oscillator is passed through a frequency divider, in order to reduce the value of the frequency to be measured by the external equipment (the measured ring oscillator loop frequency = 69.825 MHz).

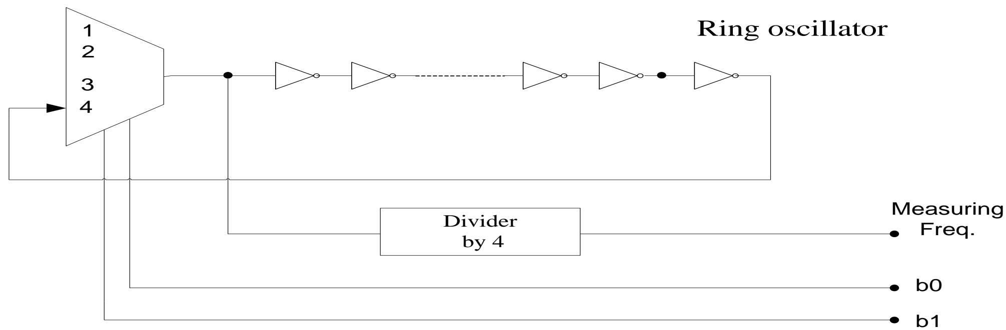


Figure 5.28: Calibration circuit configured to measure ring oscillator frequency.

The process of measuring ΔT_{input} starts by activating the ring oscillator without adding any delay section in the loop, as shown in Figure 5.28, where its frequency F_1 is measured at the output of divide-by-4 circuit, followed by switching the fixed delay section into the ring oscillator loop in order to measure its frequency F_2 as shown in Figure 5.29.

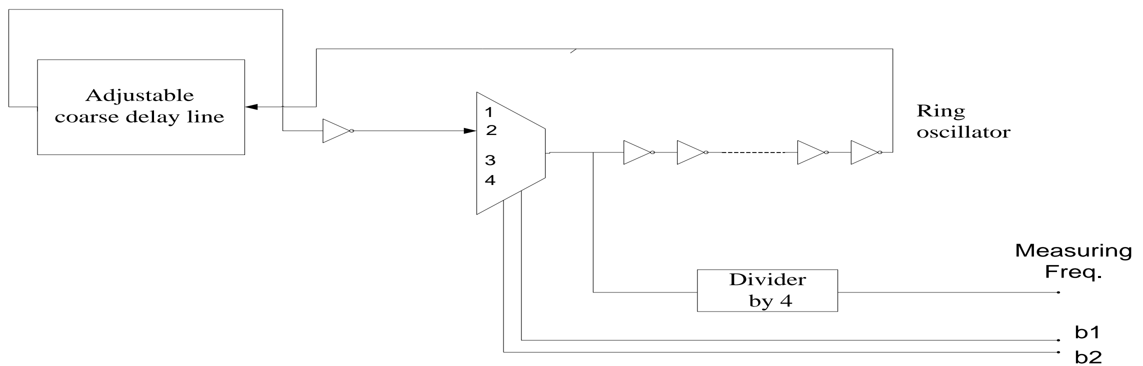


Figure 5.29: Calibration circuit configured to incorporate the effect of delay line.

The effect of the added delay in the ring oscillator loop can be calculated using the following equations [11].

$$F_1 = \frac{1}{4 \cdot \tau} \text{ --- (5.5)}$$

$$F_2 = \frac{1}{4 \cdot (\tau + \Delta t)} \text{ --- (5.6)}$$

Consequently,

$$\Delta t = \frac{(F_2 - F_1)}{4 \cdot (F_1 \cdot F_2)} \text{ --- (5.7)}$$

Where τ is the period of the ring oscillator without adding any delay section and Δt is the time delay difference; both F_1 and F_2 are divided by 4 as their signals are measured at the output of the divide-by-4 circuit.

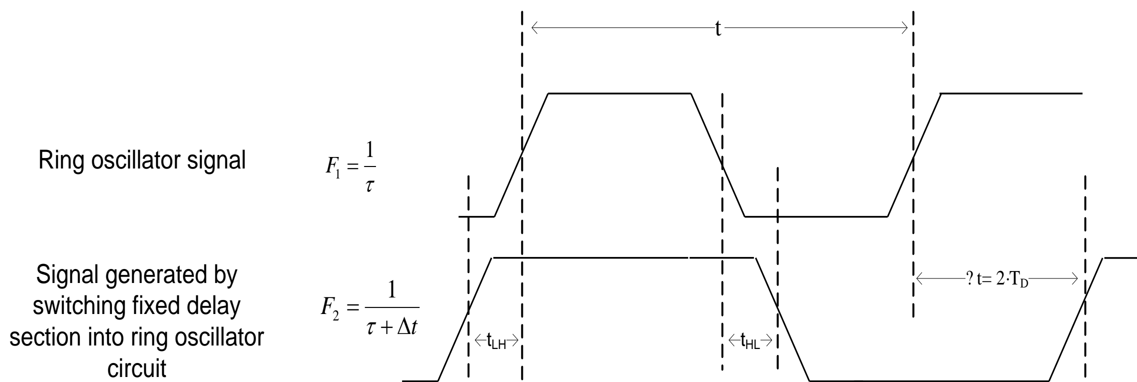


Figure 5.30: The effect of adding a delay section into the ring oscillator loop.

Adding the fixed delay section (T_D) into the ring oscillator loop affects the period of ring oscillator signal on both high to low and low to high edges, as shown in Figure 5.30. Thus, if it is assumed that the added delay has the same effect on both high to low and low to high edges, the rising edge (t_{LH}) and falling edge (t_{HL}) are equal, then the fixed delay cell can be calculated using Equation 5.8.

$$T_D = \frac{\Delta t}{2}, \text{ where } \Delta t = \frac{(F_2 - F_1)}{4 \cdot (F_1 \cdot F_2)} \text{ --- (5.8)}$$

After determining the fixed delay value, the adjustable delay section is measured following the same steps of measuring the fixed delay section which is started by switching the adjustable delay section into the ring oscillator loop in order to measure its frequency while its delay (T_{D1}) is calculated using Equation (5.8). Finally, ΔT_{input} is calculated using Equation (5.9).

$$\Delta T_{input} = T_{D1} - T_{D} \text{ --- } (5.9)$$

It is important to note that the calibration procedure is based on measuring the difference between two frequencies using the same path and divide-by-4 circuit, hence minimizing the error in the measurement of the delay.

Subsequently, the time amplifier is calibrated using the adjustable coarse delay line, the adjustable fine delay line or both of them depending on the selected gain value. Similar to the calibration process for the tapped delay line, the calibration of time amplifier is started by switching the adjustable delay section into the ring oscillator loop where the frequency at each delay step used is measured, followed by, switching the fixed delay line into the ring oscillator loop in order to measure its delay. By determining ΔT_{input}, using Equation (5.9), the gain of the time amplifier can be calculated based on Equation (5.10)

$$\text{Gain} = \frac{\text{Number of High Logic Value in the Output of the TIM} \times \text{Tapped Delay Resolution}}{\Delta T_{input}} \text{ --- } (5.10)$$

Table 5.1 shows the function of the mode selector for each control input in the calibration circuit. All of these modes are selected through a multiplexer circuit, as shown in Figure 5.26.

Control Input		Operation
b_0	b_1	
0	0	Allow the external signal to pass through the coarse and the fine delay line in order to generate the test signal.
0	1	Switch the adjustable delay section into the ring oscillator loop in order to measure its frequency at the output of the divide-by-4 circuit.
1	0	Switch the fixed delay section into the ring oscillator loop in order to measure its frequency at the output of the divide-by-4 circuit.
1	1	Activate the ring oscillator circuit without adding any delay section in order to measure its frequency at the output of the divide-by-4 circuit.

Table 5.1: The function of the mode selector in the calibration circuit.

Simulation results of the calibration circuit: The tapped delay is calibrated for a selected delay value which has a time measurement result equal to (0000000000000000000000000000011). The frequency of the ring oscillator without adding any delay section is measured and is equal to 69.825 MHz, the frequency when

the fixed delay section is switched into the ring oscillator loop is 68.525 MHz. Using Equation (5.8) the fixed delay value T_D is calculated as shown below.

$$T_D = \frac{(69.825\ \text{MHz} - 68.525\ \text{MHz})}{8 \cdot (69.825\ \text{MHz} \cdot 68.525\ \text{MHz})} = 33.9\ \text{ps}$$

Similarly, the delay of the adjustable section, T_{D1}, was switched into the ring oscillator and has a frequency value equal to 64.225 MHz, hence T_{D1} is calculated as follows.

$$T_{D1} = \frac{(69.825\ \text{MHz} - 64.225\ \text{MHz})}{8 \cdot (69.825\ \text{MHz} \cdot 64.225\ \text{MHz})} = 156.1\ \text{ps}$$

Then, ΔT_{input} is calculated using Equation (5.9),

$$\Delta T_{input} = 156.1\ \text{ps} - 33.9\ \text{ps} = 122.2\ \text{ps}$$

By determining ΔT_{input}, the resolution of the tapped delay can be calculated using Equation (5.4).

$$\text{Tapped Delay Resolution} = 122.2\ \text{ps} / 2 = 61.1\ \text{ps}$$

After calibrating the tapped delay line, the time amplifier is calibrated using the same methodology. For example, for selected gains, 8.68 and 57.75, the calibration is started by determining the value of the adjusted ΔT_{input}. However, ΔT_{input} must be chosen within the dynamic input range of the time measurement circuit which is estimated depending on the gain. For a gain equal to 8.68, as the time measurement circuit has 32 cells, the dynamic input range of the time measurement is from around 6.9 ps to 221.2 ps while for 57.75 it is between 1.04 ps and 33.02 ps. The simulation result for the calibration of the time amplifier for gains equal to 8.68 and 57.75 is shown in Table 5.2.

The calibration result of the gain for the programmable bit value "1110"				
Delay block type	T_D (ps)	T_{D1} (ps)	$\Delta T_{input} = T_{D1} - T_D$ (ps)	G (Eq. (5.9))
Fine	15.5	30.62	15.12	$= \frac{2 \cdot 61.1}{15.12} = 8.08$
Fine	15.5	44.06	28.56	$= \frac{4 \cdot 61.1}{28.56} = 8.56$
Coarse	33.9	152.1	124.2	$= \frac{18 \cdot 61.1}{28.56} = 8.855$
Average gain				8.45
The calibration result of the gain for the programmable bit value "1000"				
Fine	15.5	23.9	8.4	$= \frac{8 \cdot 61.1}{8.4} = 58.19$
Fine	15.5	30.62	15.12	$= \frac{14 \cdot 61.1}{15.12} = 56.57$
Fine	15.5	40.7	25.2	$= \frac{24 \cdot 61.1}{25.2} = 58.19$
Average gain				57.65

Table 5.2: The calibration results for the time amplifier for given gains.

5.3 Design of Chip Layout

The layout of the reconfigurable TIM, which is implemented using UMC 90 nm CMOS technology, was designed using CADENCE tools. For simplicity the design was divided into three cells, namely, tapped delay, time amplifier, and calibration cells. The CADENCE tools provide an option to merge these cells together into one cell. Four interconnect layers were used in designing the layout, namely, metal 1, metal 2, metal 3 and metal 4. From Figure 5.31 it can be seen that two thick wires are placed all around the boundary of the layout, one of them is connected to the supply voltage and the other to the ground. These two wires are connected all round the circuit to ease the connection between the reconfigurable TIM circuit and the voltage supply and ground.

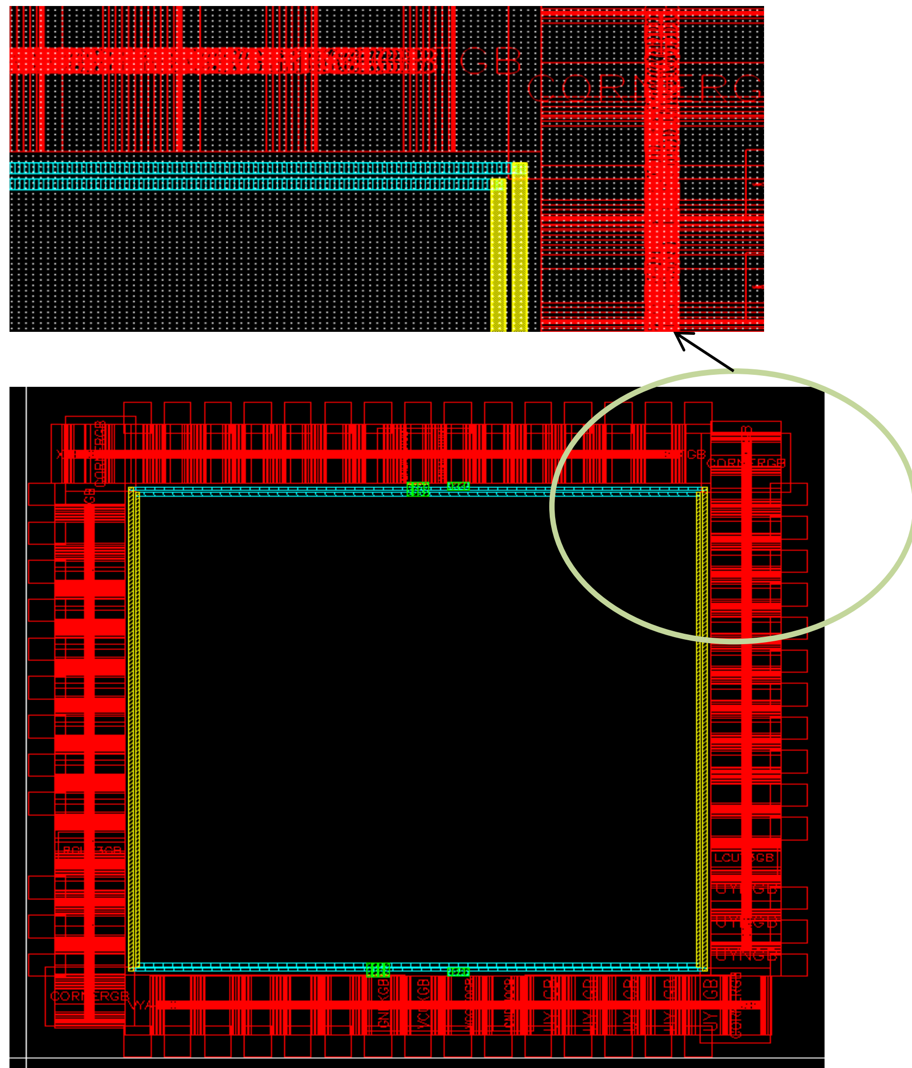


Figure 5.31: All around two thick wires are used for voltage supply and ground.

In designing the tapped delay line cell, the cell comprises two sub cells which are the DFF and inverter cells. The tapped delay line cell is formed from a series of these two sub cells where the interconnect length between the cells is designed to be equal in order to avoid any delay mismatch among the cells of the tapped delay. It is important also to mention that the time amplifier circuit was placed close to the tapped delay line circuit and the length of the two paths between them are equal as shown in Figure 5.32.

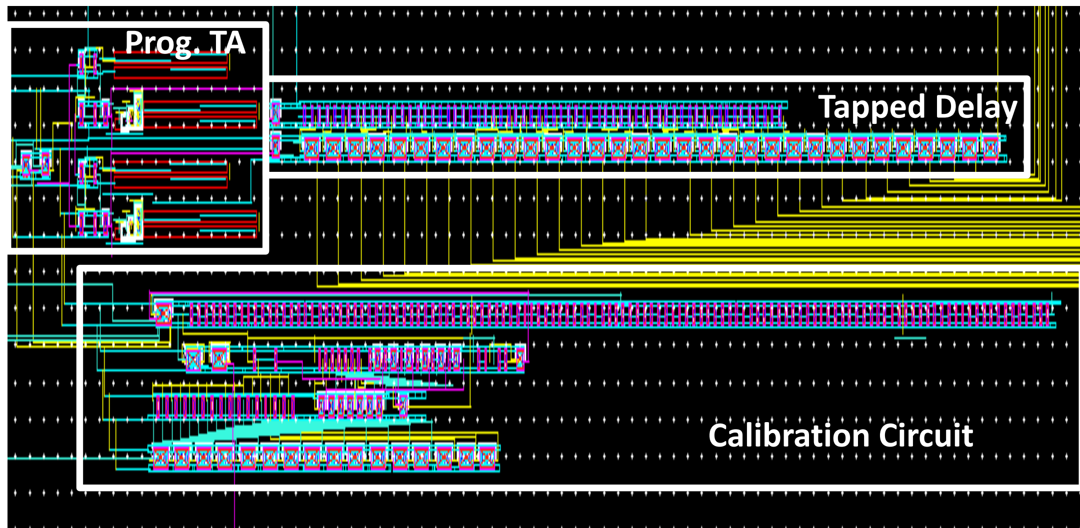
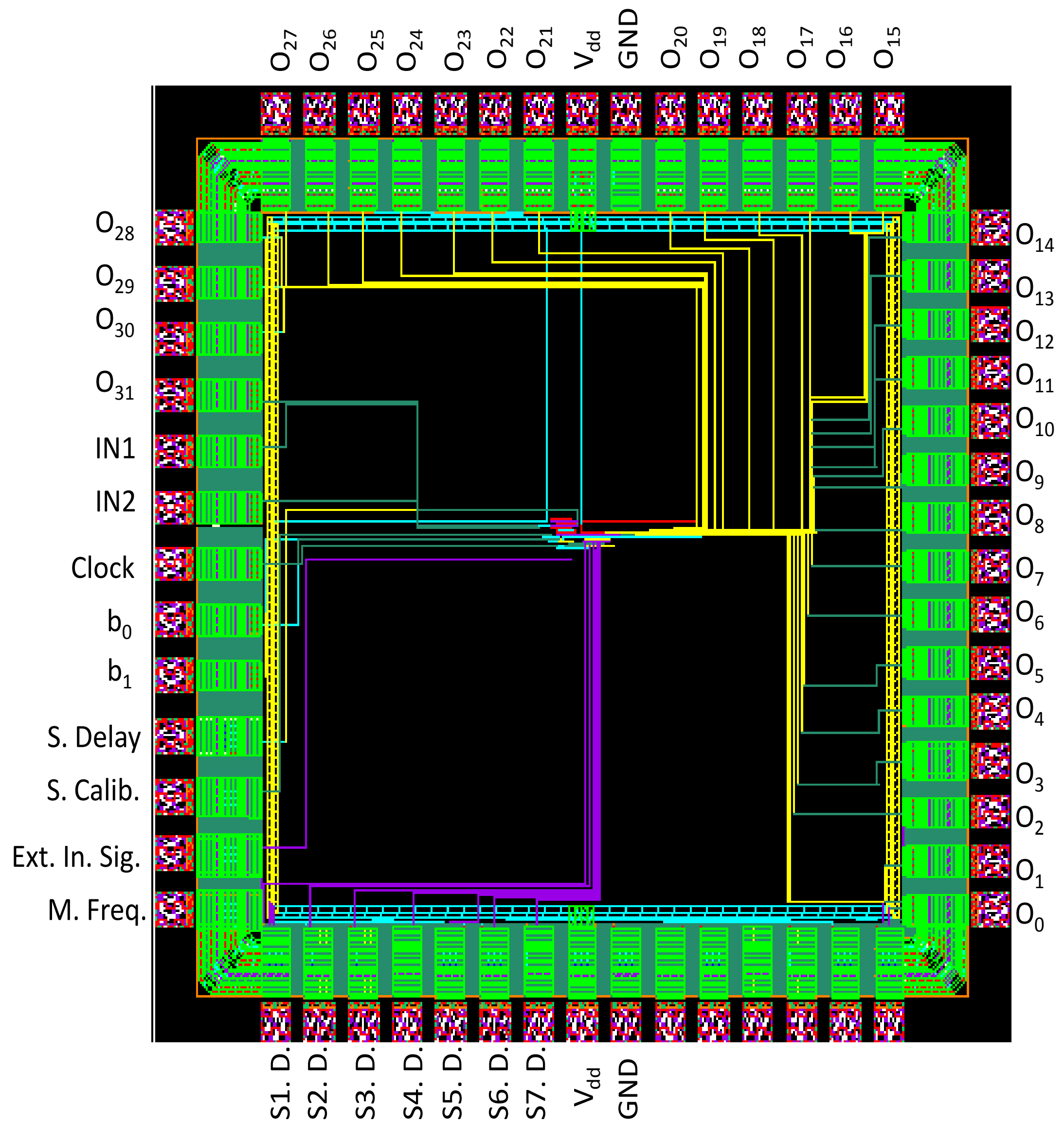


Figure 5.32: Reconfigurable TIM layout.

As discussed in Chapter 3, the time amplifier circuit comprises two MUTEX circuits whose gain is highly dependent on the time offset of the MUTEX. In addition, for the unbalanced active charge pump load design, which is used in this design, both MUTEXes must be symmetric, as discussed in Chapter 3. Thus, the design of the time amplifier is started by creating a cell of a MUTEX circuit. In this cell, the placement of the transistors and the length of the interconnect wires are designed to be equal, in order to achieve the symmetric MUTEX circuit. Two other critical paths that have to be considered are the paths between the calibration circuit and reconfigurable TIM. In these two paths, where the generated test signals from the calibration circuit are passed through to the reconfigurable TIM, the interconnect wire lengths must also be equal. The final layout for the whole chip is shown in Figure 5.33 while the pin definition is shown in Table 3.



<u>Layout specification</u>

Die size: 1.875 µm x 1.875 µm　　Area occupied by reconfigurable TIM: 379.5 µm x 67.5 µm

Number of transistor: 1364　　Number of chip I/Os : 58

Voltage Supply: 1V

Figure 5.33: The layout of the reconfigurable TIM chip.

Pin	Function
$O_{0.....}O_{31}$	Reconfigurable TIM output.
IN1 & IN2	Input of an external two signals to be tested.
V_{dd}	Voltage supply.
GND	Ground.
Clock	Connected to the phase shift to adjust the fine delay block.
b_0 & b_2	To select the calibration mode (see table 5.1).
S.Delay	To switch between the fine and adjustable block.
S. Calib.	To switch between the external input (IN1 IN2) and the calibration circuit.
Ext. In. Sig.	An external input test signal used in the calibration circuit to generate two input signals with adjustable ΔT_{input}.
M. Freq.	The output of the divided by 4 circuit.
S1. D… S7 D	The input of the selectors which is used to adjust the delay in the coarse block

Table 5.3: The description of the reconfigurable TIM circuit pin-out.

5.4 Conclusion

This chapter outlined the development of a time amplifier circuit which used the unbalanced active load designs with added resistance in the NAND gate pull down network. The design was tested using Virtuoso Spectre Circuit Simulator in CADENCE suite of CAD tools.The time amplifier was subsequently modified to incorporate a programmable capability which permitted the gain to be varied in the range 4 to 117; subsequently depending upon the gain setting the measurement resolution could be varied from 0.5 to 15 over the dynamic range 16 to 480 ps respectively. The reconfigurable TIM has the flexibility to be used in a number of time related measurements such as jitter and set up and hold measurements. The advantage of having a single circuit capable of being used for several different measurements applications rather than having a dedicated circuits is that not only is the subsequent area overhead minimized but also the calibration procedure is only to be performed on a single circuit.

The calibration circuit for the reconfigurable TIM comprises both on chip and off chip components. The calibration procedure is based on calibrating the tapped delay line to

known delay values thereafter the gain of the time amplifier is measured using the calibrated tapped delay line.

The reconfigurable TIM circuit was designed in a 90nm CMOS technology where the chip layout is implemented as a full custom design. The area occupied by reconfigurable TIM circuit is 379.56 μm x 67.565 μm.

5.5 References

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Chapter 6

Conclusions and Future Work

6.1 Introduction

As device dimensions are continuously scaled down, design parameter variability is increased which leads to unpredictable consequences in circuit performance due to the uncertainties in the relationships between signals internal to the chip. It is not feasible to measure the internal relationship between signals using Standard Automatic Test Equipment (ATE) due to the lack of measurement resolution and accessibility, resulting in the need for an 'on-chip' time measurement system. In this thesis, a reconfigurable time interval measurement (TIM) scheme with adjustable resolution and dynamic range was designed to address these issues and also have the flexibility to be used in a range of time measurement applications.

The TIM circuit which has been designed can have its operational parameters adjusted, that is, resolution and dynamic range depending upon the application, for example, jitter measurements, set-up and hold time measurements etc. Using a TIM with an adjustable resolution and dynamic range consumes less area overhead as the same circuit is used for different measurement functions. It also has the advantage that only one circuit needs to be calibrated.

The following sections comprise a summary of the thesis in section 6.2, followed by the conclusions derived from the simulation results obtained from the circuit design regarding performance and robustness to the effects of process variation etc. in section 6.3, ending with several proposals for future work in section 6.4.

6.2 Summary of the Thesis

In this thesis, several improvements on a time amplifier design, which used the buffer delay offset method, are outlined below which extend the time input difference range by approximately 650% whilst avoiding the use of large buffer delays to create the time offset; the gain of the subsequent circuit is also more robust to the effect of process variation. In addition the time amplifier was developed to incorporate a programmable gain capability. Finally, a reconfigurable TIM is designed comprising a programmable time amplifier, tapped delay line and calibration circuits.

6.2.1 Time Amplifier

The time amplifier using two MUTEX circuits with opposite offsets was proposed first in 2003 [1]. The time offset of the MUTEX circuit was created by increasing or decreasing the transistors size of the NAND gates, as discussed in Chapter 3. The most important feature of this design is that it is an all digital circuit. However, this method suffered from the narrow input dynamic range which is limited to 6 ps for a gain of 10 using a 0.18μm CMOS technology [2]. In 2008, the performance of the time amplifier, was improved by adding additional capacitance to the output nodes of the NAND gates and implementing the time offset by using buffer delays[3]. In this design, the input dynamic range was increased to nearly 40 ps for a gain of 20 using a 90 μm CMOS technology. Although the input dynamic range was improved, it was still limited to 40 ps. Another disadvantage of this design is the mismatch in the time offset which is created by a buffer delay realised using two inverters.

In this work three time amplifier circuits were designed and their performance analysed. The first method avoids the use of the buffer delay to create the time offset where the time offset is created using unbalanced node capacitance. By using this method the time amplifier circuit becomes more robust to the effects of process variation than the buffer delay offset design, as discussed in chapter 4. The second method incorporating active loads using the charge pump concept, at the output of the NAND gate which improved the dynamic input range from 40 to 70 ps. The final design incorporated unbalanced active loads with added resistance to each NAND gate, as discussed in Chapter 3, which extended the dynamic input range achieved by the buffer delay offset design by a factor of 6.5, from 40 ps to 300 ps.

The design of the time amplifier was a further developed by including a programmable gain capability over the range of 4 to 117. The flexibility of adjusting the gain led to the design of a reconfigurable TIM, as discussed in Chapter 5.

6.2.2 Time Amplifier and Process Variation Effects

The effect of the process, temperature and power supply variation on the time amplifier designs, namely, buffer delay offset, unbalanced active capacitance load and unbalanced active charge pump load designs, was studied in detail in Chapter 4. From the results, the gain of the unbalanced active capacitance load design is the most robust to the effects of the process variation among the other designs. In addition, from Chapter 3, implementing the three time amplifier circuits using NAND gates with added resistance creates a huge improvement in terms of the dynamic input range. However, the gain is more sensitive to the effects of process variation for this technique. These issues are discussed in details in section 4.3.1 in Chapter 4.

In terms of the temperature variation, the gains of the buffer delay offset and the unbalanced active capacitance load are less affected than the unbalanced active charge pump load design. However, as the temperature was increased, the gain was decreased for all the designs when the NAND gate with added resistance was used, which is discussed in section 4.4 in Chapter 4.

From section 4.5 in Chapter 4, it can be summarised that the voltage supply variations affect the three time amplifier designs in different ways. For the unbalanced active capacitance load and unbalanced active charge pump load designs, the gain is increased as the voltage supply is decreased while it is decreased in buffer delay offset design. However, when the NAND gate with added resistance is used, the gains of the unbalanced active capacitance load and unbalanced active charge pump load designs are increased more as the voltage supply is decreased. On the other hand, there was a slight degradation in the gain of the buffer delay offset design, as the voltage source is decreased.

6.2.3 The Reconfigurable TIM

As mentioned previously the reconfigurable TIM comprises three main parts, namely, a programmable time amplifier, a simple tapped delay line and the calibration circuit. The tapped delay consists of two components, a buffer delay and DFF, where the buffer delay is formed from two inverters. The resolution of the tapped delay line is designed to be equal to 60 ps, the programmable time amplifier is attached to it, as shown in Figure 6.1. The programmable time amplifier is designed to have a variable gain ranging from 4 to 117 with a very wide dynamic input range, as discussed in Chapter 3. As a result the reconfigurable TIM, overall, has a variable resolution range of 15 ps to 0.5 ps with a dynamic range of 480 ps down to 16 ps.

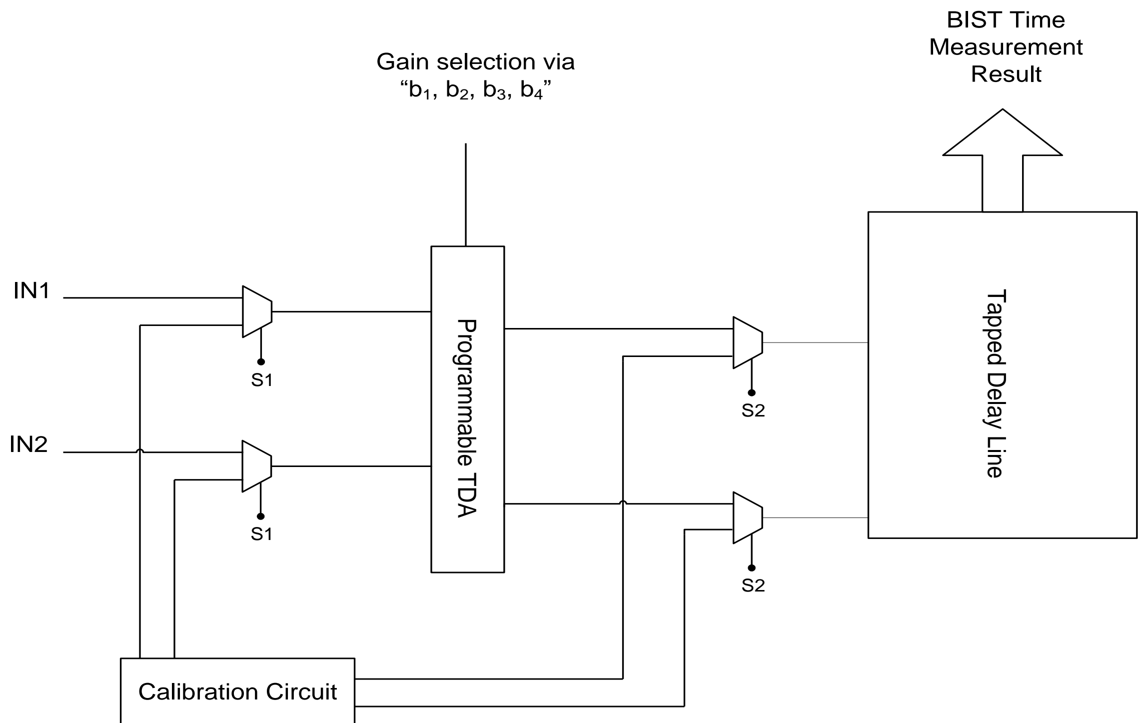

Figure 6.1: The block diagram of the reconfigurable TIM.

The calibration procedure for the reconfigurable TIM is designed to comprise two parts, on-chip and off-chip. As discussed in Chapter 5, using a partial on-chip calibration circuit has an advantage of minimising the effects of process variations; the on-chip part is based on the off-chip reference part.

The calibration methodology depends on comparing the time measurement result with a known delay value. Two variable delay lines are used where one of them has a coarse step variable delay and the other one has a fine step variable delay. Both delay lines can be switched into a ring oscillator in order to measure its delay steps, as discussed in Chapter 5.

The procedure for the calibration is started by calibrating the tapped delay line, followed by calibrating the time amplifier depending on the calibrated tapped delay line. The adjustable gain is calibrated at more than one point where the gain value is calculated as the average of the results. The error in calculating the gain can be minimised by adding more calibration values. The calibration circuit and procedure are discussed in detail in Chapter 5.

6.3 Conclusion

The work outlined in this thesis describes the design and analysis of three time amplifier circuits and reconfigurable TIM, from which the following conclusions may drawn.

1) The time amplifier implemented using the unbalanced active capacitive load design is more robust to the effects of the process variation than using the buffer delay offset and unbalanced active charge pump load designs. However, this design has a narrow input dynamic range which is equal to 40 ps.
2) The widest dynamic input range for the time amplifier can be achieved by incorporating unbalanced active charge pump loads at the output nodes together with added resistance in the discharge path of each NAND gate, the input dynamic range was increased to 300 ps.
3) The configuration of the active charge pump load circuit provides the flexibility for the time amplifier circuit to have a programmable gain capability, as discussed in Chapter 3.
4) The development of a programmable time amplifier led to the design of a time measurement circuit which comprises a time amplifier and a delay line, with adjustable resolution which was difficult to realise. This is because the delay line comprises a series of cells consisting of a buffer delay and a DFF, where each of these cells must have the same delay value in order to provide a fixed resolution, as shown in Figure 6.2. Any mismatch in the delay value among the cells leads to an

error in the time measurement result. Therefore it is not feasible to design an adjustable delay line by adjusting the delay of the cells. However, when a programmable time amplifier is attached to the input of the delay line, the resolution of the time measurement can be adjusted by changing the gain of the time amplifier.

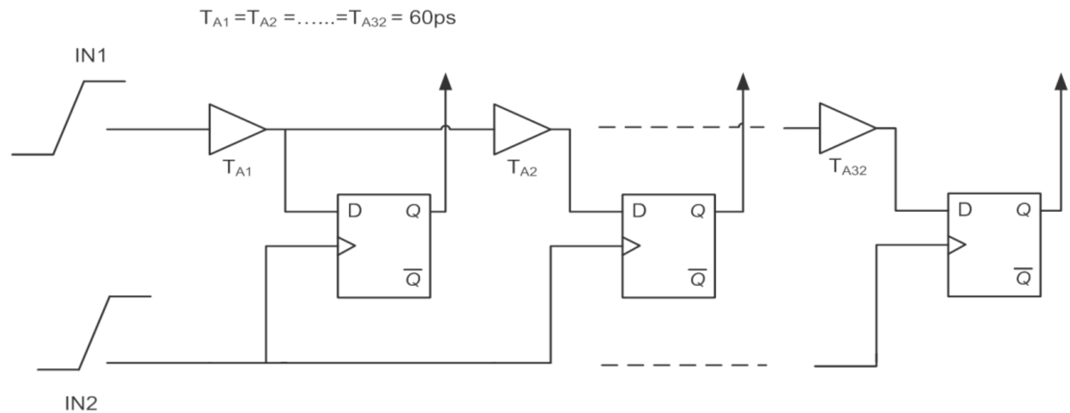

Figure 6.2: Block diagram of delay line.

5) It would not be possible to attach the programmable time amplifier to the delay line without improving its input dynamic range. This is because a narrow input dynamic range would limit the time measurement range. For example, if a time amplifier with an input dynamic range equal to 40 ps is attached to a delay line, the dynamic range of this system is limited to 40 ps. Consequently, in this work, the input dynamic range of the time amplifier was first increased to 300 ps.
6) The design of the reconfigurable TIM shows that a basic tapped delay line with a very low resolution, 60 ps, can be turned into a system performing a time measurement with a very high resolution, 0.5 ps, by attaching the programmable time amplifier to its input.
7) The flexibility of adjusting the resolution and the dynamic range of the time measurement in the reconfigurable TIM design, enables the resolution range to be adjusted from 0.5 to 15 ps and the dynamic range from 16 to 480 ps respectively, giving the reconfigurable TIM the capability to be used for different time measurement applications. Furthermore, the use of the reconfigurable TIM incurs less area overhead, overall, than TIM circuits design for specific applications, as the same circuit is used for different functions and, in addition, only one circuit needs to be calibrated.

8) Overall the final design of the TIM circuit satisfies the main design criteria outlined in Chapter 1 for development of a time measurement circuit, namely
    - Improve time amplifier dynamic range, 300 ps.
    - Modified the time amplifier to incorporate a programmable gain capability over the range of 4 to 117.
    - High measurement resolution, 0.5 ps.
    - Adjustable measurement resolution, from 0.5 ps to 15 ps.
    - Low area overhead, 0.026 mm^2 using 90nm CMOS technology.
    - Relatively simple calibration procedure.
    - Robustness to the effect of PVT variation.
    - Ease of use, one shot operation.

As such, it is considered that this design advances the state of the art regarding the design of on-chip time measurement circuits.

6.4 Future Work:

The reconfigurable TIM circuit offers several advantages over previous designs, one of which is the wide range of the adjustable resolution. However, in the delay line circuit, the dynamic range of the time measurement is calculated by multiplying the resolution value by the number of cells in the delay line. By considering the reconfigurable TIM which is designed in this thesis, it can be seen that the dynamic range for the time measurement when the gain is adjusted to 117 is from 0 up to ΔT_{input_Max}, which is calculated as follows:

$$\Delta T_{input_Max} = \frac{\text{Number of the Cells in the delay ine} \times \text{ Delay Line Resolution}}{\text{Gain}} \text{---(1)}$$

$$= (32 \text{ x } 60 \text{ ps}) / 117 \approx 16 \text{ ps}$$

From the previous calculation, the dynamic range for a gain of 117 is from 0 up to 16 ps which is very narrow. From Equation (1), the dynamic range can be improved by adding more cells however this incurs greater area overhead. This issue can be overcome by combining a coarse and fine delay lines.

The combination of a coarse and fine delay method is based on two steps; first the measurement is made to the accuracy of the coarse delay line, then it is switched to the

accuracy of the fine delay line, as discussed in Chapter 2. However, when implementing the combination method using the reconfigurable TIM, several factors need to be investigated and developed. First, a switching circuit between the coarse and fine delay line is required to be compatible with the adjustable resolution capability of the reconfigurable TIM circuit. Second, the calibration circuit for the combination method needs to be investigated, as this combination may increase the complexity of the calibration procedures. Finally, the robustness of the combination method to the effect of the process, power and temperature variations need to be investigated.

One of the major challenges facing 'on-chip' time measurements is the need for on-chip calibration, this technique is also called auto-calibration or self-calibration, where the calibration procedure avoids the use of any off-chip reference components leading to reduced the costs of the calibration process. This challenges arises from the effect of the process variation leading to the requirement of another circuit to check the calibration circuit. However, the checking circuit is also required to be checked. This is because in the procedure for calibrating a high resolution time measurement, around 1 ps, a comparison of a known delay value is required, the error in determining the exact value of this delay leads to difficulties in determining the resolution of the time measurement. Measuring this delay, around 1 ps, in the calibration circuit using only on-chip components has not been possible without a considerable error arising from the effect of process variation. The area of the auto-calibration requires more investigation in term of compensating for the effects of the process variation.

'On-chip' time measurement is effectively used to monitor the timing relationships between signals in an IC. Correcting the error in the timing relationships, generally, can be done in two ways; first by avoiding the critical path or speed it up; second, improve the circuit design to be robust against these errors. However, in debugging the critical path and devices, it is necessary to identify the sources of the timing error which is a challenging problem, as there are different reasons which can cause the same timing error, such as process, temperature and voltage variations and negative bias temperature instability (NBTI), etc.

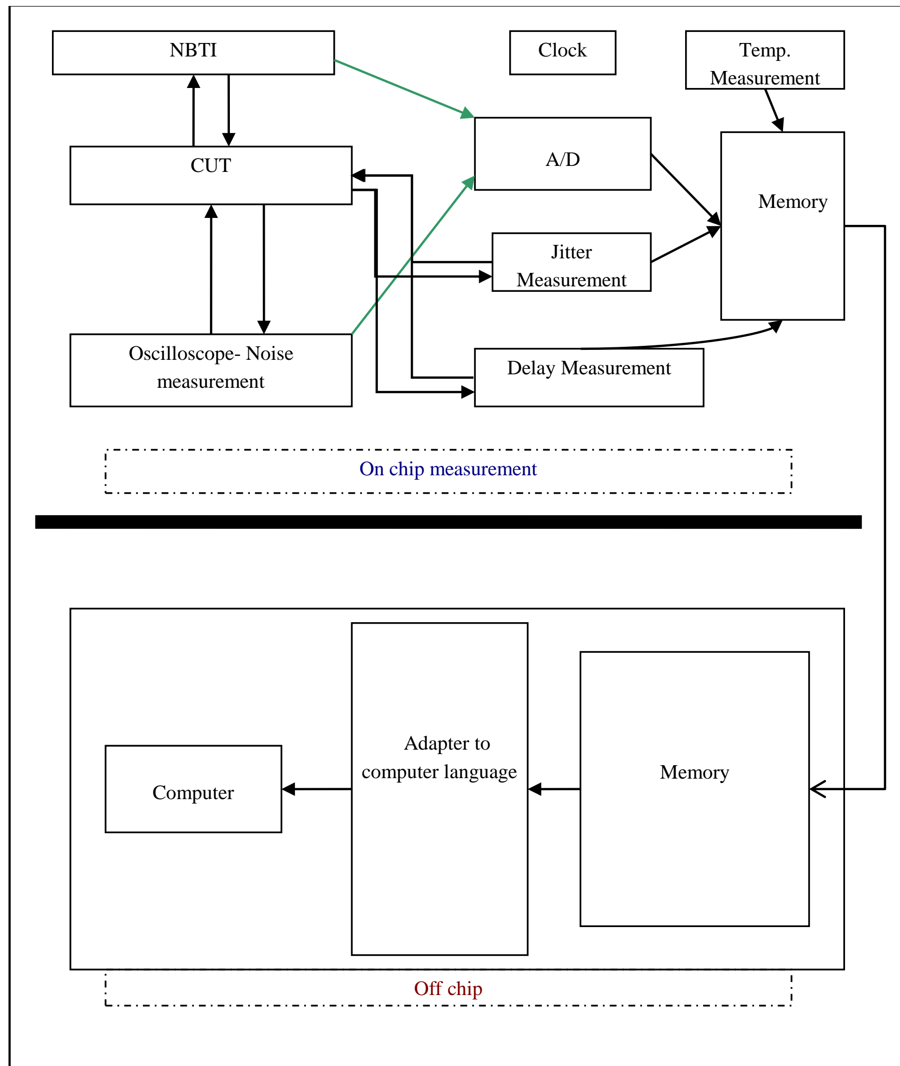

Figure 6.3: Block diagram for the LOC

Other researchers have used BIST approach for several parameter measurements such as measuring delay, jitter, threshold voltage, temperature and noise. However, each measurement circuit focuses on a single parameter. An idea for future work is to incorporate five parameter measurements, for example, time delay, jitter, temperature, NBTI and On-Chip Oscilloscope measurements on a single chip, which can be referred to as 'lab on a chip' (LOC), Figure 6.3 shows a block diagram for the proposed LOC.

6.5 References

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Appendix A

The simulation result of the time amplifier circuit, which was implemented in UMC 90nm technology; where the simulation was undertaken using Virtuoso Spectre Circuit Simulator in CADENCE suite of CAD tools.

Figure A.1 The behaviour of C_1 and C_2, and their discharge currents during the arrival of IN1 and IN2, for unbalanced active capacitance load design using a NAND gate with added resistance in the discharge path.

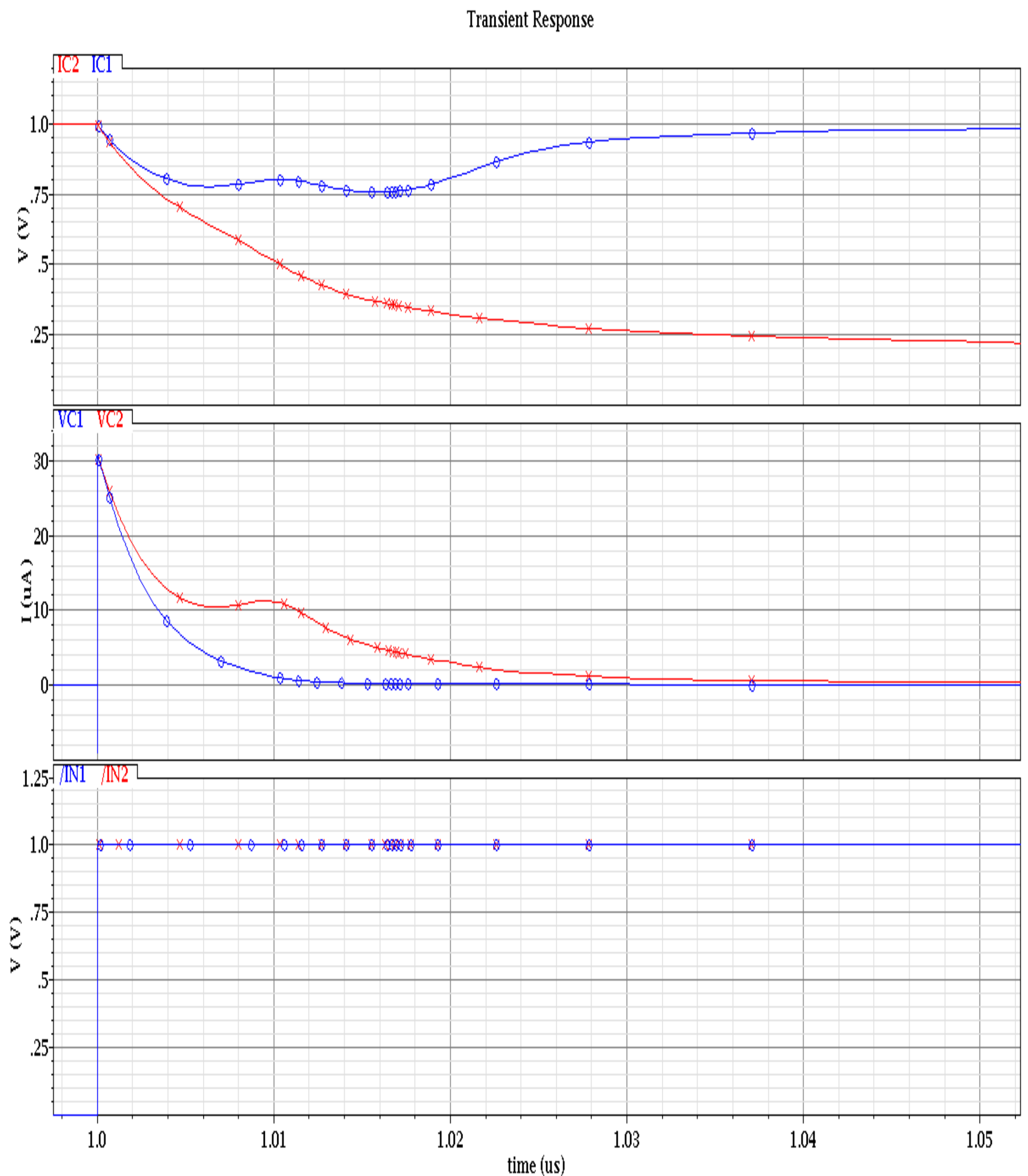


Figure A.2 The behaviour of C_1 and C_2, and their discharge currents during the arrival of IN1 and IN2, for unbalanced active charge pump load design using a NAND gate with added resistance in the discharge path.

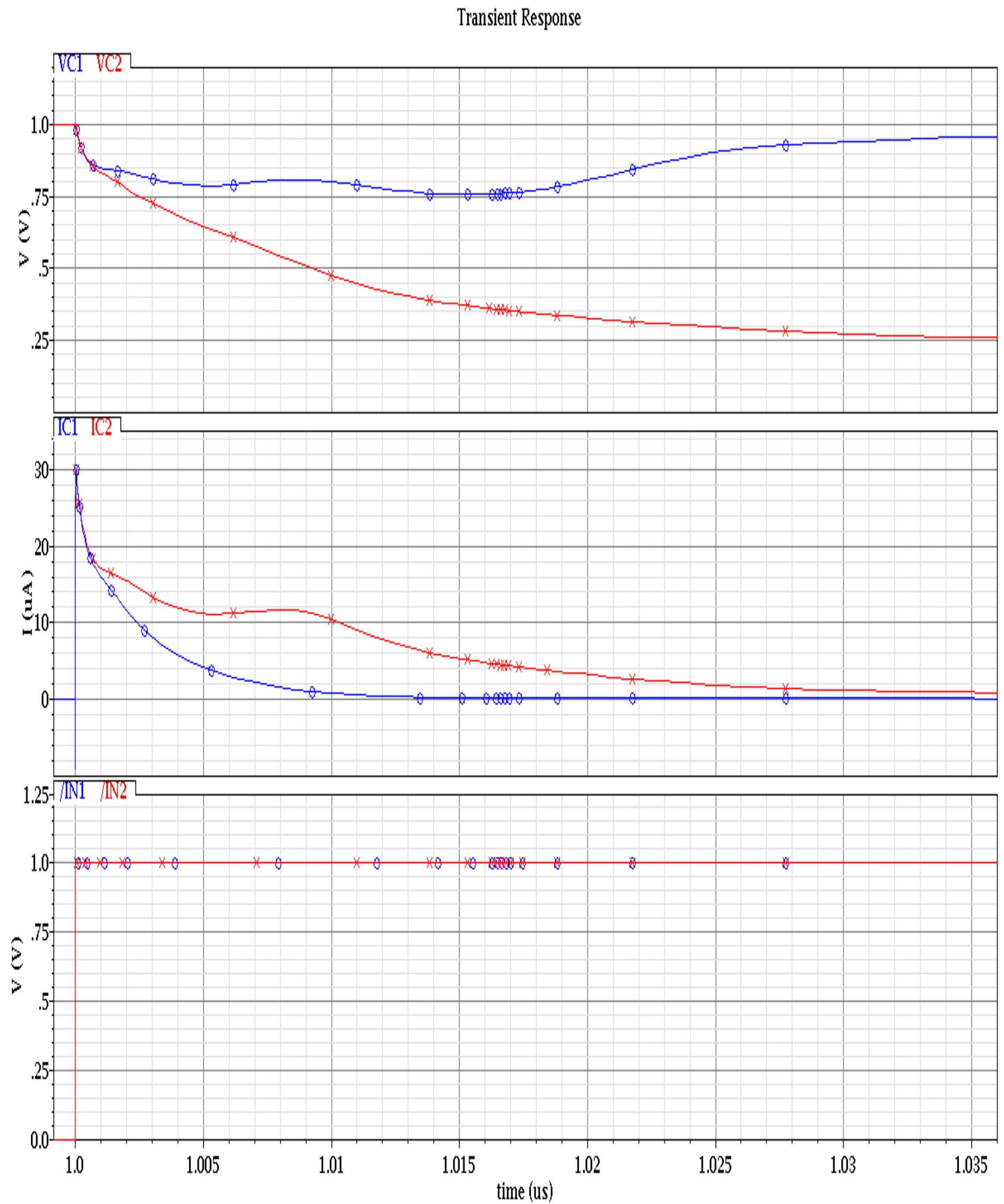
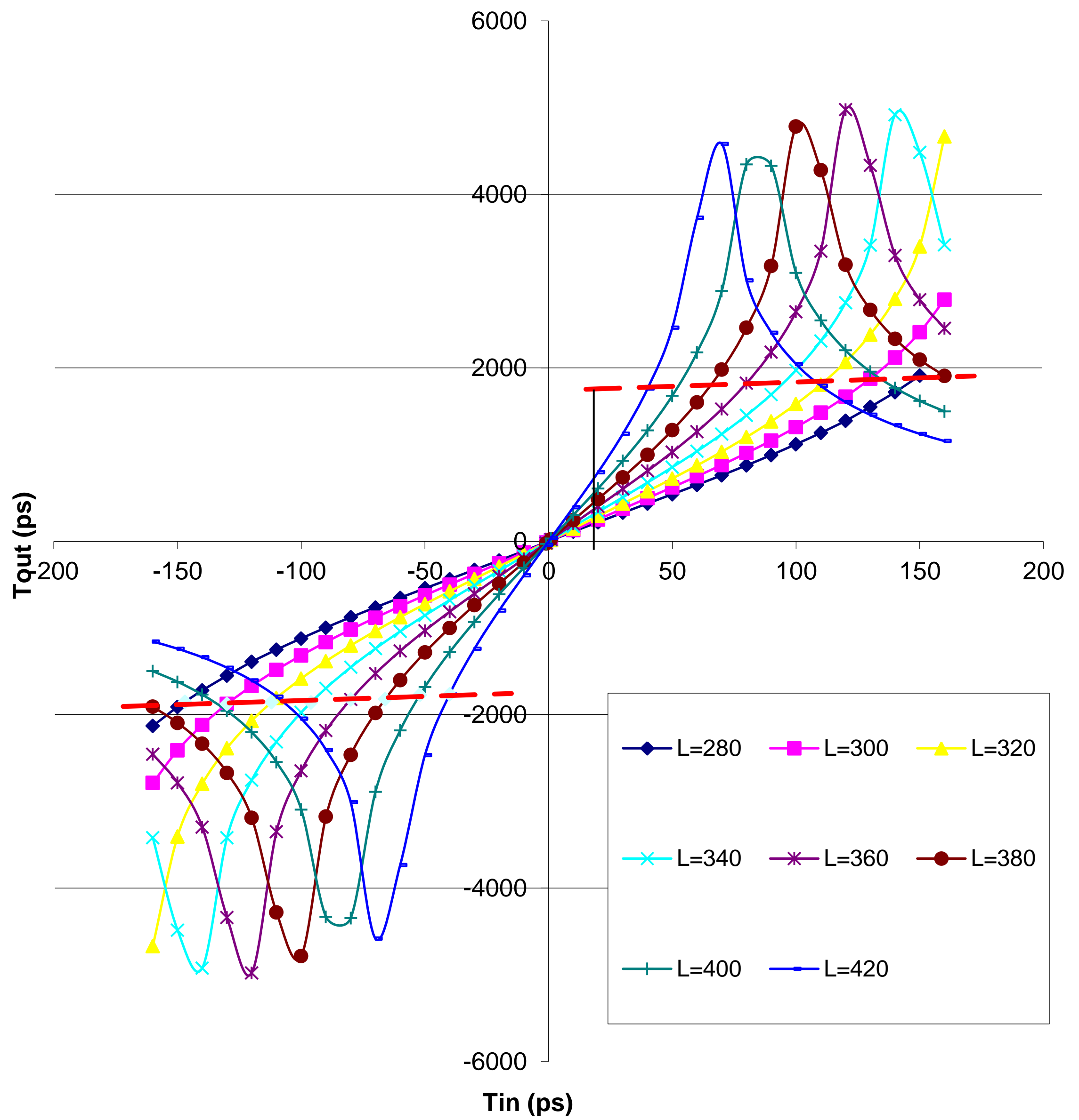


Figure A.3 The effect of changing L_{Q2}, L_{Q1} is fixed to 0.5µm, on the gain and the dynamic input range for unbalanced active charge pump load design.



Appendix B

Figure B.1 TIM result for ΔTinput=10ps and gain value 117.1.