IMPROVING FAULT TOLERANT DRIVES FOR AEROSPACE APPLICATIONS

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Preface

This thesis is submitted as part of the Engineering Doctorate (EngD) degree.

The EngD differs slightly from the traditional Philosophy Doctorate (PhD) in the sense that it is more a portfolio of work undertaken at industry. The Engineering and Physical Sciences Research Council (EPSRC) describes the Engineering Doctorate as:

"A four-year programme that combines PhD-level research projects with taught courses, and students spend about 75% of their time working directly with a company"

In the first year of the EngD, various modules from MSc and MBA programs are undertaken. The remaining 3 years focuses on the main body of research, in collaboration with the industrial sponsor.

The work undertaken in this thesis was done at Newcastle University with Goodrich Actuation Systems (part of Goodrich Aerospace, now United Technologies) as the industrial sponsor.

Abstract

The aerospace industry is moving towards the more electric aeroplane where traditional hydraulic systems are being replaced with electrical systems. Electrical technology offers some strong advantages compared to hydraulic technology including; cost, efficiency, power on demand and relative ease of maintenance. As with most new technologies, a major disadvantage is its limited reliability history. A lot of research in the aerospace field therefore focuses on improving fault tolerant electrical systems.

Work done in this thesis builds on an existing fault tolerant drive, developed by Newcastle University and Goodrich Actuation Systems as part of the ELGEAR (Electrical Landing Gear) project. The purpose of this work is to continue improving the drive's fault tolerant features; especially in areas where the drive is most vulnerable.

The first part of this thesis focuses on improving the overall system reliability by monitoring the health of the dc-link capacitors in the fault tolerant drive. The implemented estimation technique makes use of voltage and current sensors which are already in place for protection and control purposes. The novel aspect of the proposed technique relates to monitoring capacitors in real time whilst the motor is operational. No external interferences, such as injected signals or special operation of the drive, are required. The condition monitoring system is independent of torque and speed, and hence independent of a variation in load. The work was validated using analytical methods, simulation, low voltage experimentation and high voltage implementation on the ELGEAR drive.

The second part of this thesis focuses on single shorted turn faults, in fault tolerant permanent magnet (PM) motors. Despite the motor being able to withstand a wide range of faults, the single shorted turn fault remains a difficult fault to detect and handle. The problem arises from the magnets on the spinning rotor that cannot be 'turned off' at will. This thesis investigates the severity of the faulted current in a shorted turn and how it varies depending on the turn's location in the stator slot. The severity of the fault is studied using 2D finite element analysis and practical implementation on the ELGEAR rig. Finally, recommendations are proposed for improving the ELGEAR motor for future fault tolerant designs.

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I could not have done the engineering doctorate without support from my parents Frederic and Olivia as well as my sister Connie-Rose. My family have provided me with a huge amount of support and perseverance throughout the doctorate scheme. Special credit should be given to my father Frederic who helped me by providing me with technical support and ideas using his vast amount of experience of the industrial world.

List of symbols and acronyms

List of symbols

A	Availability of a system or cross sectional area
c	Specific heat capacity
C	Capacitance
e_f	Electro-motive force
f	Frequency
i	Current
i_C	Capacitor current
J	Current density
j	Imaginary component
l	Length
L	Inductance
L_m	Mutual inductance
N	Number of turns in a coil
R	Resistance
T	Torque or temperature
t	Time
v	Voltage
V_C	Capacitor voltage
V_{dc}	Dc bus voltage
V_{pp}	Peak to peak voltage
X_C	Capacitor reactance
X_L	Inductor reactance
ϑ	(rotor) Angle or temperature
ρ	Density or resistivity
σ	Conductivity
ϕ	Flux
ψ	Flux linkage
ω	Angular frequency

List of Acronyms

AC	Alternative current
ADC	Analogue to digital converter
CE	Conducted emissions
CMRR	Common mode rejection ratio
CS	Conducted susceptibility
DAC	Digital to analogue converter
DC	Direct current
dsPIC	Digital signal peripheral interface controller
ELGEAR	Electrical landing gear
EMC	Electromagnetic compatibility
EMF	Electro-motive force
EMI	Electromagnetic interference
ESL	Equivalent series inductance
ESR	Equivalent series resistance
IGBT	Insulated gate bipolar transistor
LED	Light emitting diode
MDE	Motor drive electronics
MMF	Magneto-motive force
MPPF	Metallised polypropylene film
MTTF	Mean time to failure
MTTR	Mean time to repair
PCB	Printed circuit board
PE	Protective earth
PLL	Phase locked loop
PM	Permanent magnet
ppm	Parts per million
pu	Per-unit
PWM	Pulse width modulation
RE	Radiated emissions
RLC	Resistor inductor capacitor
rms	Root mean square
RS	Radiated susceptibility
SRM	Switch reluctance motor

General Introduction

Chapter 1

1.1 Principles of fault tolerance

In everyday life we are often faced with the situation where a failure in an electronic device causes the device to malfunction or not to function at all. Causes of such failures may be traced to improper handling of the product, component failure, tear and wear etc. In most cases the disruption caused by the failed product is not too severe, and the product is usually replaced sooner or later (or not at all!).

In some cases however, a fault causing disruption in a system is simply not an option. Failure of such systems could lead to hazardous situations, financial losses, serious environmental consequences, human injury or even death. Examples include the military, telecommunication industry, banking sectors, nuclear industry and the aerospace industry [1]. In these vulnerable situations, fault tolerant systems are employed to significantly increase the system's reliability and availability.

The definition of a fault tolerant system is well described by White and Miles in [2]:

"A fault in a component or subsystem does not cause the overall system to malfunction"

A fault tolerant system is essentially a carefully designed system that is resilient to single-point failures. In the event of a fault, the system would still continue to function but this might be at limited or reduced capacity (depending on the specification for post fault operation).

Using statistical means, an important aspect of reliability can be analysed. Fault tolerance is typically evaluated through component history or life testing statistics. It is expressed as mean time to failure (MTTF). This variable indicates the typical time span until a component is likely to fail. The duration of a system being offline is defined by the mean time to repair (MTTR). Using both MTTF and MTTR, the availability *A* of a system can be calculated, shown in equation (1.1) [2].

$$A = \frac{MTTF}{MTTF + MTTR} \tag{1.1}$$

White and Miles also describe the four principle points which have to be taken into account when designing a fault tolerant system. These are:

1. Redundancy – The ability for a system to continue operating after a fault. This can be achieved by having an entire backup system that starts operating when the primary system is offline. Another form of redundancy includes partitioning, where the system is divided in failure groups. This way, vulnerable sections of the system can be designed to provide additional redundancy.
2. Fault isolation – Preventing the fault from propagating to healthy parts of the system.
3. Fault detection and annunciation – Ensuring a fault gets reported to maintenance, thus avoiding dormant failures or systems losing their redundancy.
4. Online repair – In some applications, systems are continuously operating and can therefore not be switched off for maintenance. Repairs have to take place whilst the system is running, also known as hot swapping.

Another factor to consider is that more redundancies in a system leads to a lower MTTF due to the increase of the number of components, and thus a higher probability for a component to fail. When a system is properly designed – incorporating effective redundancy switching – it considerably reduces the chance of a catastrophic failure. However, a significantly higher maintenance capacity is required as explained by Argile in [3].

1.2 Contribution to knowledge

This section outlines areas of work that have not been published before, or not covered in detail in the current literature.

- Work done in this thesis has resulted in a journal paper publication:

  Condition Monitoring of DC-Link Capacitors in Aerospace Drives
  This paper appears in: IEEE Transactions on Industry Applications
  Date of Publication: Nov.-Dec. 2012
  Author(s): Wechsler, A.
  School of Electrical & Electronic Engineering, Newcastle University, Newcastle upon Tyne, UK

Mecrow, B.C. ; Atkinson, D.J. ; Bennett, J.W. ; Benarous, M.
Volume: 48, Issue: 6
Page(s): 1866 - 1874
Product Type: Journals & Magazines

- Development and application of a novel online condition monitoring technique of dc-link capacitors in aerospace drives, by experimental and simulated verification.
- Examination of fault tolerant PM machine design parameters that influence the severity of turn-turn faults during fault and post fault operation.
- Experimental and simulated verification of the presence of negative leakage inductance in faulted turns of fault tolerant PM machines

1.3 Evolving aircraft technology

The fault tolerant drive described in this thesis is for the aerospace application. This section aims to provide a general background on the development of electrical systems on aircraft.

1.3.1 *The more electric aeroplane*

Hydraulically powered systems have been present on aircraft since the dawn of aviation. During the 1940's it was decided that future aircraft flight systems – mainly actuators – should be based on hydraulic technology and not electrical [4]. At the time aircraft simply did not have sufficient electrical power generation capacity to support electrical systems.

This situation changed in the 1980's (see Figure 1.1) where an increasing demand of electrical technology in combination of advancement in engine power and power electronic systems played a key role to introducing electrical systems on aircraft on a larger scale. Since then, aircraft were equipped with ever more electrical power consuming systems such as in-flight entertainment, multiple radar systems, navigation, flight data processors etc. As a consequence, aircraft must have an appropriate electrical infrastructure including ac power generation, power distribution, rectification and filtering [5-7].

Potential improvements are highlighted in the *All Electric Aircraft* by Cronin [8]. Electrical systems pose many advantages over hydraulic systems:

- Power on demand. Hydraulic systems require constantly pressurised systems, even when on stand-by where nominal power is consumed to maintain pressure. In contrast, electrical systems only consume power when operating.
- Ease of maintenance. Although the actual routine maintenance may not be any different, hydraulic fluids are more difficult to maintain. In contrast, electrical systems can be relatively easily replaced using appropriate interconnections. Furthermore electrical systems have wider possibilities for diagnoses.
- Reduction in weight. This point can be argued, since some electrical concept systems are actually heavier than their hydraulic counterparts. On the other hand, taking continuous progression into account it should be possible to significantly reduce the weight of many electrical components.

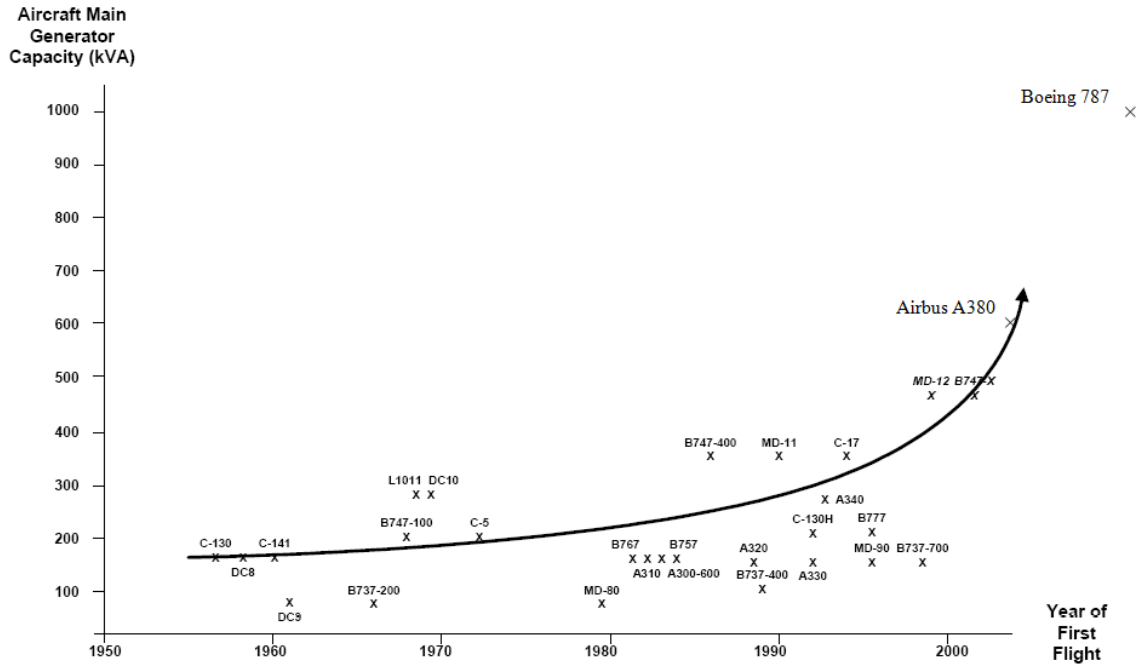


Figure 1.1 – Development of power generation on an aeroplane [6] (chart updated using [5])

Nevertheless, the aerospace industry is very cautious and reluctant to introducing new technologies due its limited reliability history. This has especially been the case for flight critical systems where reliability is top priority. In flaps and slats for example, a mean failure rate of under 10^{-9} per hour is required, which corresponds to a failure every 100,000 years of continuous operation. By comparison, industrial electrical machines typically have a failure rate of 2×10^{-5} failures per hour [9].

Today, the aerospace industry is moving towards the concept of the *more electric aircraft*, rather than the *all electric aircraft*. This essentially highlights the direction of

aerospace research towards hybrid technologies. Some mechanical and hydraulic components may be completely replaced (e.g. fly-by-wire in Airbus aircraft), other systems will simply operate in parallel in the form of an active redundancy or as auxiliary units.

Examples of electrical systems can be found in the new Boeing 787 Dreamliner, which has a generating capacity of 1000 kVA (250 kVA per engine) [5] incorporating many electrical systems including electric braking in the undercarriage wheels. Electrical equipment is also replacing pneumatic technology on the future Boeing 747-8 aircraft. Rolls-Royce is currently developing bleedless engines, suggesting that electrical compressors are now a more efficient way obtaining air [10].

The Airbus A380 (with a generating capacity of 600 kVA, 150 kVA per engine) [5] incorporates a number of electrical systems, examples include:

- Electrostatic hydraulic backup actuators (EHBA) – where the technology is still predominantly hydraulic but is backed up by an electrically powered actuator. One of such components can be found in the aircraft's rudder (Figure 1.2).
- Electrostatic hydraulic actuator (EHA) – Similar to the above, but operates as an active unit, under normal circumstances. It can be found in the aircraft's ailerons (Figure 1.3).
- Other electrical or hybrid systems can be found on the aircraft's spoilers and elevators.

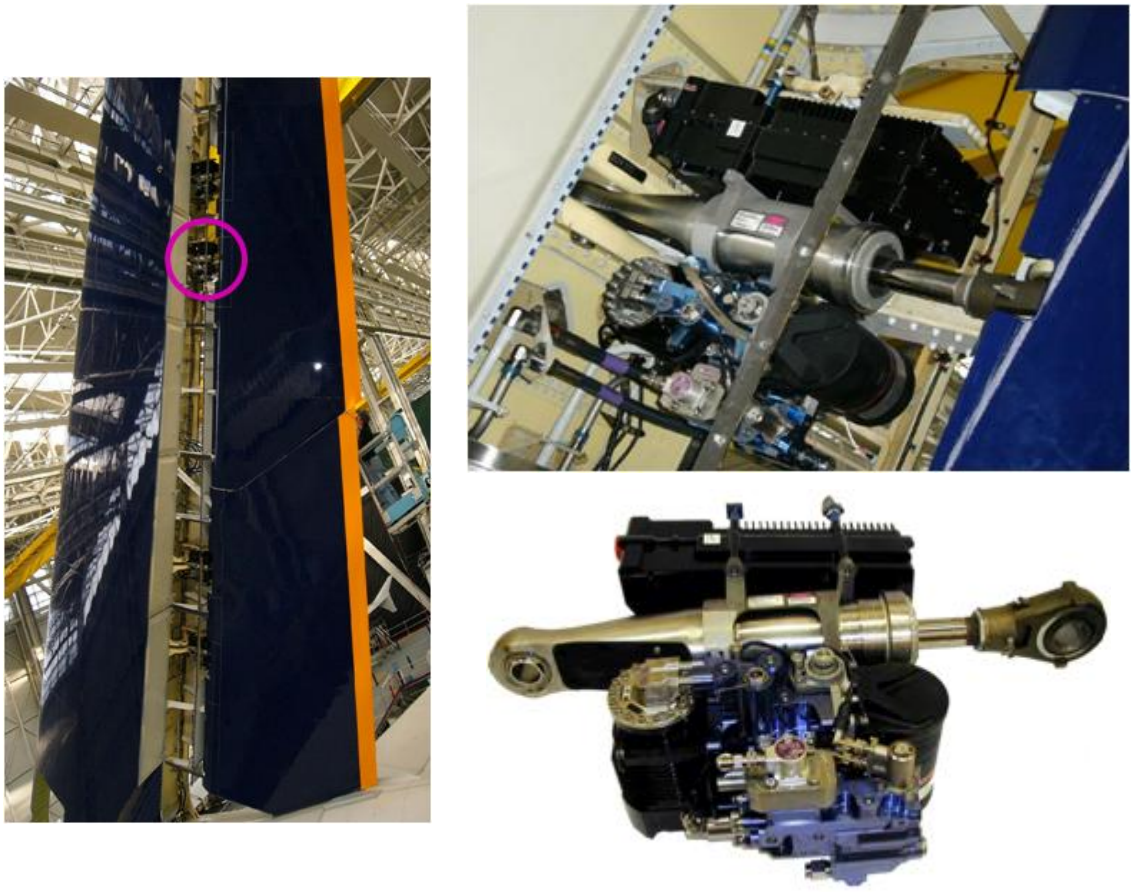


Figure 1.2 – Electrical Backup Hydraulic Actuator mounted on an Airbus A380 rudder

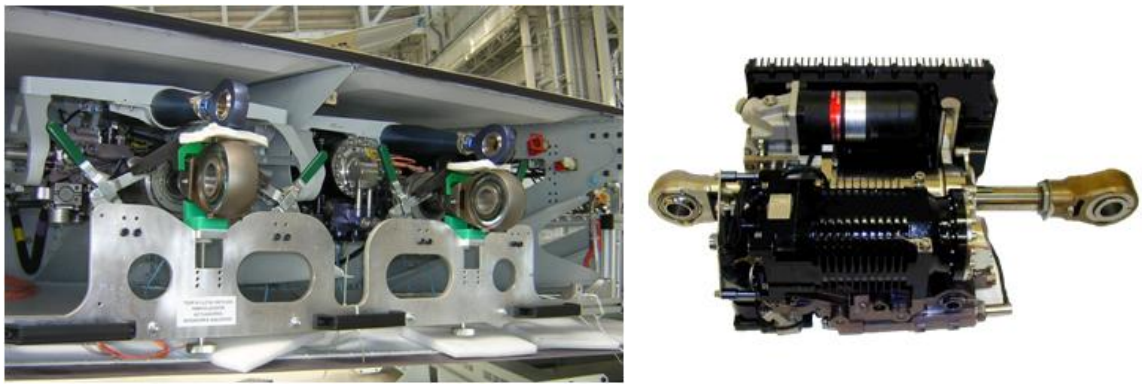


Figure 1.3 – Electrical Hydraulic Actuator mounted on an Airbus A380 aileron

1.4 Fault tolerant drives in aircraft

1.4.1 *Overview*

Today's aeroplanes incorporate various technologies that all have to be qualified for fault tolerant operation. There are a variety of systems on board an aeroplane as shown in Figure 1.4. The figure shows a simplified breakdown of the different technologies used which are further broken down in separate units consisting of components.

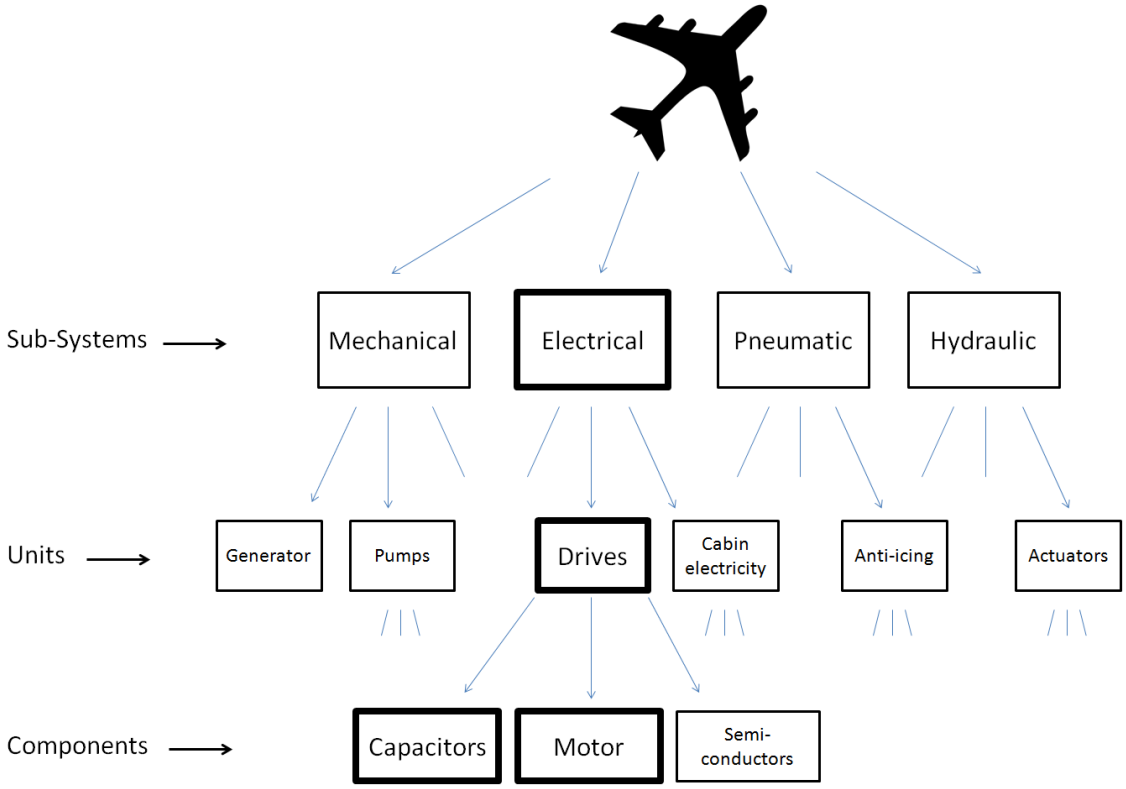


Figure 1.4 – Simplified overview of the various systems on board an aeroplane

The subsystems' power mostly originates from the engine. Mechanical power is extracted from the engine shaft and is distributed to hydraulic pumps, electrical generators, etc. Pneumatic power is obtained using a bleeding compressor in the engines that in turn is used to start up engines, maintain cabin pressure, power instrumentation and de-icing equipment. Hydraulic power is used to drive most actuators on an aeroplane, although some actuators are already replaced by electrical systems [11, 12].

An electric drive can be broken down in to the dc-link capacitor, inverter (including semi-conductors), controller and the motor. This thesis specifically focuses on the fault tolerant issues related to dc-link capacitors and permanent magnet (PM) motor design in aerospace drives.

1.4.2 *Redundant power generation and distribution*

In an aircraft, electrical power is generated by the engines. For redundancy reasons, there are typically two separate power sources originating from two or more engines. The ac generator output is then rectified to a symmetric dc voltage of +270V and -270V.

Another separately generated, redundant power source produces a dc supply voltage of 28V. This independent low voltage and low noise supply is dedicated to aliment instrumentation such as navigation, communications digital processors etc. Single instruments are often wired-or to both nominal and active redundant low-power supplies by use of diodes; a very simple and reliable method.

All aircraft dc power is transported to various electrical systems on an aircraft through a dedicated set of power lines known as a ‘bus’. Bus architecture implies that all users are connected in parallel. This approach clearly becomes a reliability issue since any user on the bus may disturb other users either by short-circuiting the power lines or producing excessive noise. Table 1.1 lists these errors under ‘fault propagation’. In order to avoid mutual interference, all electrical systems connected to the power bus have to conform to strict electromagnetic compatibility (EMC) regulations, outlined by the DO-160F standard in [13].

One of the topics covered in the DO-160F standard is associated with the amount of ripple or noise a system is allowed to generate. Over-current protection towards the power bus is also specified. For motor drive electronics, filters have to be introduced to suppress the switching noise of the inverter, and any spikes from being transmitted back onto the power bus. Usually power filters consisting of inductors and capacitors are introduced. Under the DO-160F standard, section 16.7.7.2 for 270 V equipment it states:

“For equipment of the same type that draws a combined total power between 1kW and 10kW, the peak to peak value of the individual equipment's line current ripple shall not exceed 0.140 times of the individual equipment's maximum load dc current draw.”

1.4.3 *Fault tree*

The fault tree in Figure 1.5 is used to highlight all the potential hardware faults that may occur in an electric drive and its corresponding consequences. For example, a diode in the inverter may fail open or short circuit, or a thermocouple fault would provide a wrong feedback value. All of these failures must be taken in to account and as aforementioned, none of these failures are allowed to cause the overall system to malfunction.

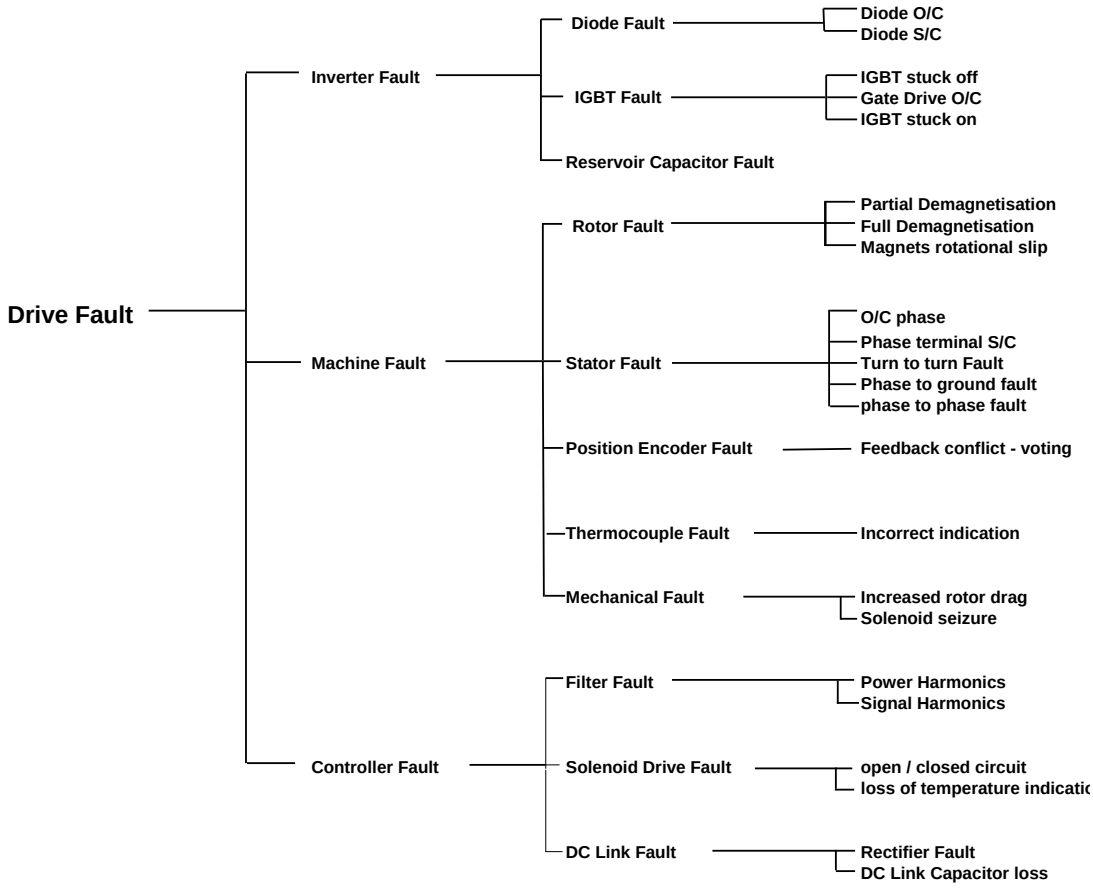


Figure 1.5 – Fault tree

The failures investigated in this thesis focuses on dc-link (or reservoir) capacitor faults, found under inverter fault, and the turn-turn fault found under machine stator fault.

1.4.4 *Type of failures*

Failure analysis is a broad topic as there are many different type of scenarios related to the type(s) of failure that could occur. From a failure handling point of view, there are various different type of failure cases as shown in Table 1.1.

Case	Failure Type	Means to avoid
1	Single-point Failure	Hot redundancy Redundancy switching
2	Systematic Failure	Failure supervision & preventive maintenance
3	Fault Propagation	Localised protection
4	Multi-point Failure	Out of scope

Table 1.1 – Failure cases

Single-point failures are failures that result in the shutdown of an entire system which must be avoided in fault tolerant systems. An example of a single-point failure is shown in Figure 1.6. The redundancy topology in this particular case is incorrectly designed as the power supply is vulnerable to single-point failures. A failure in the power supply will cause the entire system to shut down. Using appropriate redundancy by ensuring fault tolerance across the entire system (i.e. the addition of a back up supply) reduces the likelihood of such failures.

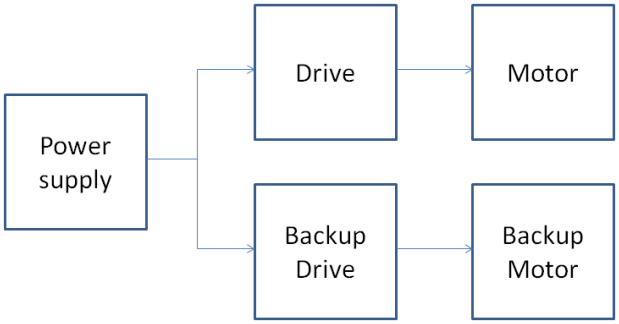


Figure 1.6 – Single-point failure example when the power supply fails

A systematic failure occurs when a device or component fails without it being repaired. A reason may be that the fault is not detected or by negligence. As a result, components or subsystems may lose their redundancy. For example, if the drive in Figure 1.6 fails, the backup drive will now be vulnerable to single-point failures. The failure of the drive must therefore be detected and repaired swiftly.

Fault propagation could occur if a fault is not isolated properly. For example, if a fault develops in a motor consequently causing excessive heating, the thermal fault may propagate to other parts of the (healthy) system.

Multi-point failures are more complicated. They independently arise simultaneously (e.g. when the drive and the backup motor fail at the same time for different reasons in Figure 1.6). The probability of this failure occurring is much lower than the other three failures, and will not be covered in this thesis.

1.5 General research on reliability and failures

1.5.1 *Dormant failures*

In this thesis the systematic failure will be investigated for dc-link capacitors. Dc-link capacitors are inherently less reliable than other power electronic components (as will

be covered later on). They are therefore placed in a circuit, considering sufficient redundancy. However, when a capacitor fault is left undetected, it could lead to a systematic failure.

Other than the degradation and limited lifetime of capacitors, there is another important reason as to why it is desirable to monitor dc-link capacitors – to avoid dormant failures (a form of systematic failure). In general it is not strictly mandatory to have multiple parallel connected dc-link capacitors, but there are various advantages in doing so. Firstly capacitors are generally bulky components, and having multiple capacitors as opposed to a single bulky component may have advantages for compact design. Secondly, capacitors are inherently less reliable than other power electronic components (as will be covered later on the thesis). By placing capacitors in parallel, an open circuit capacitor failure would therefore not necessary constitute to a total dc-link failure.

The diagram in Figure 1.7 shows that there are four capacitors in parallel per drive forming a redundancy of 4 × 20 µF equal to an 80 µF capacitance. If a single capacitor fails open circuit, the remaining capacitors will still ensure the drive is operational because the total capacitance is 4/3 overrated by design to guarantee the full performance.

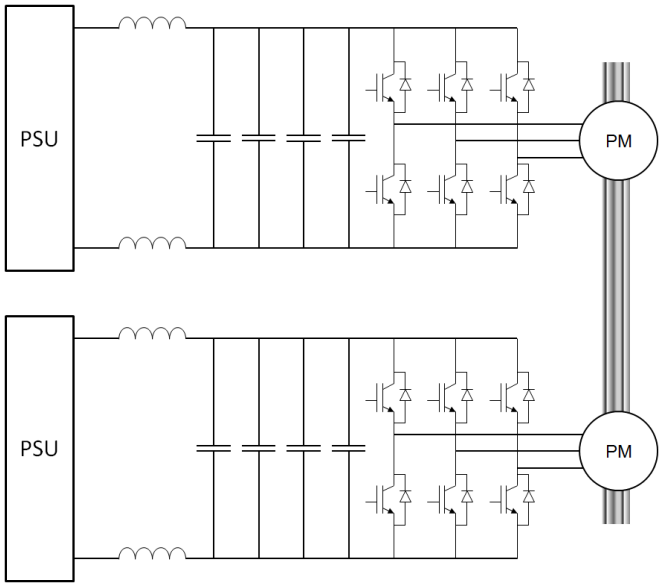


Figure 1.7 – Fault tolerant motor drive electronics

However, when a capacitor open-circuit failure occurs, the total capacitance on the dc-link reduces. This will cause an increased stress on the remaining capacitors as the ripple currents and voltages increase as a result.

When the faulted capacitor is left undetected, other capacitors in the dc-link could fail which would defeat the purpose of having multiple parallel capacitors. This effect is known as a dormant failure. Consequently, it is important to detect when a failure occurs in each of the capacitors, so the component can be replaced as soon as possible.

1.5.2 *The ELGEAR fault tolerant drive*

The motor used for this project is designed by Goodrich Actuation Systems and Newcastle University for the Electric Landing GEAR (ELGEAR) project [14]. The project was requested by Airbus to develop a concept electrical landing gear. The architecture of the fault tolerant drive used in the ELGEAR project is found in Figure 1.7. The figure shows a duplex fault tolerant 3 phase motor drive. Each drive is powered by a separate power supply unit, from two independent power sources on an aircraft [13]. Each drive also contains its own dc-link filter (two inductors and four capacitors), inverter (6 IGBTs) and a dual 3 phase fault tolerant PM motor.

Both drives are mirrored in operation to maintain redundancy across the entire drive system. The drives are continuously in operation and share the load torque under nominal conditions (active/active redundancy). Each drive is designed to maintain the fully rated torque in case its counterpart drive is out of operation. The only common fragment in the system is the mechanical actuator axle. The mechanical analysis of the axle is beyond the scope of this thesis; it is assumed that the axle is designed to meet the aerospace reliability requirements as it may constitute to a single-point failure.

1.6 Terminology and nomenclature

1.6.1 *Motor drive electronics (MDE)*

The motor drive electronics referred to in this thesis is depicted in Figure 1.8. This thesis also refers to a fault tolerant drive which is based on the same principle but is slightly modified to resist or accommodate various faults.

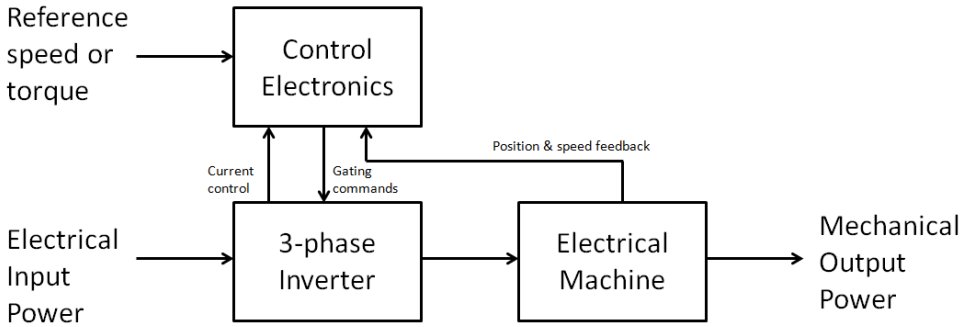


Figure 1.8 – Motor drive

3-Phase inverter

Three high power silicon bridges (IGBT technology) will commutate the three phases of an electrical machine. The standard aerospace bus voltage is ±270 V dc which is used by the bridges to produce the required phase voltage of 380V rms [13].

Control electronics

The control electronics subassembly contains all necessary functions to operate the inverter bridges in a desired manner. As the electronics work on an independent low voltage supply, the commanding interfaces to the inverter bridges are optically isolated. External inputs to control electronics are the desired motor speed and torque values which are compared with the motor sensors feedback.

Electrical machine

Finally, the output of the inverter bridge is connected to a 3-phase permanent magnet synchronous machine. The machine is equipped with a dedicated set of measurement sensors to provide information on motor torque and speed to the control electronics.

1.6.2 *Condition monitoring nomenclature*

In this thesis, a there are some specific terms which refer to the implemented dc-link capacitor monitoring system. The calculations carried out to determine the capacitance value is referred as the “estimator”. The estimator is of dsPIC technology (digital signal peripheral interface controller) and processes data originating from three modules, namely: the “timing circuit”, “voltage monitor” and “current monitor” (see Figure 1.9). Each module specialises in obtaining and transferring the appropriate signals to the estimator whilst maintaining high voltage isolation.

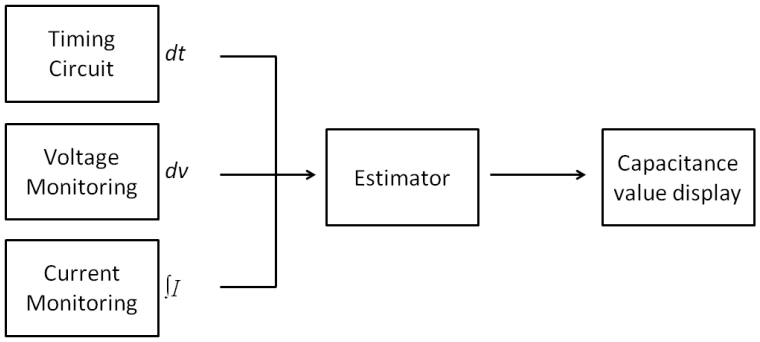


Figure 1.9 – Condition monitoring block diagram

1.6.3 *Fault tolerant permanent magnet (PM) motor*

The fault tolerant PM machine refers to a permanent magnet motor that is configured to resist or accommodate various faults. The motor design options ranges from a single overrated motor to multiple active and/or passive motors for redundancy purposes.

The motor used in this thesis is a 3-phase, fault tolerant, dual lane, interior rotor, permanent magnet motor. The term dual lane refers to a topology where two separate power supplies, drives and motors are used to drive the same shaft, or output torque as Figure 1.7 shows on page 11.

1.6.4 *Metallised polypropylene film (MPPF) capacitors*

This refers to the type of capacitor predominantly used as reservoir capacitors on aerospace drives. Although much larger in size, the capacitor is preferred to electrolytic technology due to its more fault tolerant nature.

1.6.5 *dsPIC (digital signal peripheral interface controller)*

This refers to the type of digital processor used in the control electronics. The microcontroller is a digital signal peripheral interface controller manufactured by the company Microchip. The type of controller is a specialized design for motor control applications.

1.7 Research objectives

The targets for the engineering doctorate are listed below:

- To analyse the mode of failure of dc-link capacitors in fault tolerant drives for the aerospace application.
- To develop a technique to monitor the dc-link capacitors and inform the user if an open-circuit dc-link capacitor failure were to take place.

- To investigate the impact and consequences of a turn-turn failure upon the fault tolerant ELGEAR motor.
- To provide recommendations for future fault tolerant motor designs to improve the resilience to turn-turn failures, both during fault and post fault operation.

1.8 Thesis overview

This thesis consists of two projects related to fault tolerant systems in the aerospace application. The first part of the thesis describes condition monitoring of dc-link capacitors in aerospace drives (chapters 2-5). The second part of the thesis describes an analytical study on shorted turn failures in fault tolerant permanent magnet motors (chapters 6-9). Finally, a general conclusion can be found in chapter 10, concluding the work and addressing the targets and the scope outlined in the introduction. A brief description of each chapter is provided below:

Chapter 1 contains a general introduction covering some of the more common terminology used in this thesis. The chapter provides an introduction to fault tolerant electrical systems for the aerospace application and focuses on typical fault tolerant architectures currently discussed in the literature.

Chapter 2 is a literature review covering the failure mode of MPPF capacitors and existing condition monitoring techniques in drives.

Chapter 3 introduces the proposed, novel, condition monitoring technique for dc-link capacitors. Using simulation software (Matlab Simulink), the design parameters are defined and applied for the ELGEAR project. Details of how the estimation technique will monitor the condition of dc-link capacitors, as well as its design can be found in this chapter.

Chapter 4 presents a low voltage experimentation of the proposed condition monitoring technique. This experimentation is an intermediate step before high voltage implementation. This step allows the proposed technique to be examined experimentally in a reduced noise environment where the individual components of the acquisition chain can be tested and calibrated.

Chapter 5 presents the high voltage experimentation of the condition monitoring system on a representative aerospace test rig. The limits of the proposed system are discussed in

terms of the accuracy of the data, as well as the response time of a potential capacitor fault.

Chapter 6 describes the physics and the severity of turn-turn faults in fault tolerant PM motors. The chapter consists of an introduction to fault tolerant PM motors, covering the development, variety of topologies in the literature as well as the various faults the motor can accommodate. The chapter continues by describing the type of fault tolerant PM motor used in this project (the ELGEAR motor).

Chapter 7 focuses on the impact and severity of turn-turn faults on the ELGEAR motor. The terminal fault is also covered since it is similar to the turn-turn fault. A detailed theoretical analysis of the faults is provided, where the origin and the remedial actions are discussed.

Chapter 8 analyses the terminal and single shorted turn fault using 2D finite element analysis simulation (MagNet by Infolytica). The parameters that influence the fault, such as resistance and inductance are analysed in detail, and results of the faulted current for various number of turns in the slot are plotted and discussed.

Chapter 9 follows up by introducing the faults on a high voltage test rig (ELGEAR). A comparison is drawn between the practical and simulation results, and the severity of the faults are analysed. The chapter concludes by recommending improvements to the motor for future fault tolerant design.

Chapter 10 is the general conclusion of the thesis, where both the condition monitoring and turn-turn faults are covered. The conclusion also refers to targets and objectives set in the introduction of the thesis.

Condition Monitoring Literature

Chapter 2

2.1 Introduction

This chapter commences with an assessment related to the general reliability of dc-link capacitors in drives. This is followed by a detailed study of the MPPF capacitor, where its failure modes are studied.

The chapter then focuses on condition monitoring techniques of capacitors. A literature review covers a wide range of existing monitoring techniques and proposals. It analyses both the reliability and availability of online and offline monitoring systems and how these could be applied to the aerospace application.

The chapter continues with a proposed, novel, online condition monitoring system of dc-link capacitors in aerospace drives. MPPF capacitors are the preferred technology used for the dc-link in aerospace drives. MPPF capacitors are more resilient to aerospace environments where changes to pressure, humidity and temperature play an important role upon the capacitor's health. It should be stressed that the condition monitoring system would work for other capacitor technologies as well and is thus not limited to MPPF technology.

2.2 General reliability assessment of capacitors

In order to monitor the condition of capacitors, it is important to understand why and how they fail. There are many factors that influence the failure of capacitors including:

- How the capacitor is handled and operated
- The quality of manufacturing and installation
- The environmental factors in which the capacitor operates

2.2.1 *Electrolytic capacitors*

In most power converter applications, the electrolytic capacitor is the popular choice for dc-link filtering. Electrolytic technology allows a high capacitance per volume and relatively low production costs [15-17]. Despite these advantages, electrolytic capacitors do have a vast number of disadvantages:

- Sensitivity to temperature variations as the electrolyte shows a significant dependence on temperature. According to Amaral et al. in [18], the capacitance typically varies from -40% to +5% for a temperature from -40°C to 105°C respectively. This significant change is due to the electrolyte solution having properties of conductivity and viscosity which varies quite significantly over temperature. Furthermore, the electrolyte solution is prone to a faster evaporation at higher temperatures, effectively reducing its operating life time. Induced self-heating can be observed when a high ripple current heats up the capacitor due to equivalent series resistance (ESR) losses [19, 20].
- Reduced operational bandwidth. Since it takes a finite period of time for the dipoles in the oxide dielectric of the capacitor to become orientated, the reduced capacitance is reduced at higher frequencies. This phenomenon is known as polarisation [20].
- Short shelf life. The electrolytic capacitor suffers from increased levels of DC leakage current when stored for more than 5 to 10 years. Additionally – during the capacitor's lifetime – reforming has to take place if not being exposed to a voltage for a certain period of time. Reforming is a process when the capacitor is slowly recharged at a low voltage to allow proper polarisation of the electrolyte. The length of time when reforming should take place depends on the capacitor and should be provided in the manufacturer's datasheet [15, 21, 22].

The above disadvantages add to the overall low reliability of the electrolytic capacitor. Figure 2.1 is a survey of the causes of failure in an electrical system. The survey is based on over 200 products, from 80 companies [23]. Figure 2.2 shows a separate statistical analysis by [24], based on the military handbook [25]. Clearly, (electrolytic) capacitors are responsible for most breakdowns in power electronic circuits.

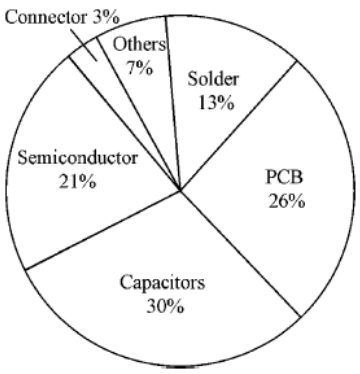


Figure 2.1 – Failure distribution of various electrical components [23]

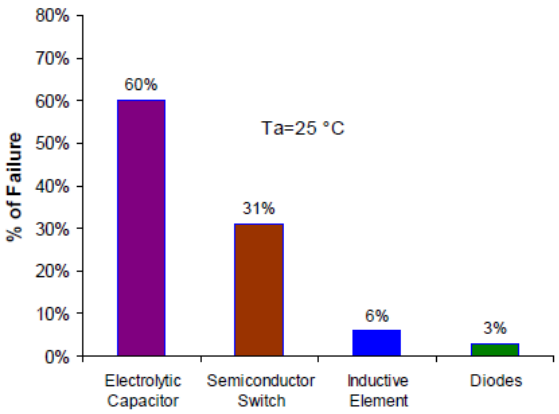


Figure 2.2 – Failure distribution of power components in power electronic circuits [24]

The most unreliable part of the capacitor is the electrolyte itself. Since it is a liquid based technology it is prone to faster evaporation and hence, faster deterioration in hostile environments – such as the aerospace environment, where variations in air pressure, temperature and humidity are extreme. As a result, the electrolytic capacitor is unsuitable for aerospace applications.

2.2.2 *Metallised polypropylene film (MPPF) capacitors*

MPPF capacitors have become an acceptable substitute to electrolytic capacitors for the aerospace and fault-tolerant application. This is mainly due to their low ESR, good filtering bandwidth as well as its unique self healing property. Moreover, MPPF capacitors are metal based and are therefore more resilient to environmental changes. Compared to electrolytic technology, MPPF capacitors offer the following advantages:

- High peak and rms current capabilities
- Not polarised
- Solid metal based technology
- More robust (able to withstand up to twice the rated voltage for short periods of time)
- Able to withstand a wide temperature range
- High reliability (long lifetime, and long shelf life)

Nonetheless, MPPF capacitors have a much lower capacitance per volume, resulting in a heavier, bulkier and more expensive component. Despite the MPPF capacitor showing significant improvement in reliability, they still remain one of the most unreliable electrical components [23, 25-27]. It is therefore desirable to monitor the condition of such capacitors to avoid dormant failures.

2.2.3 *MPPF parallel operation*

Since faults on capacitors are likely, Haylock in [28] described a configuration where dc-link capacitors are connected in series and parallel as shown in Figure 2.3.

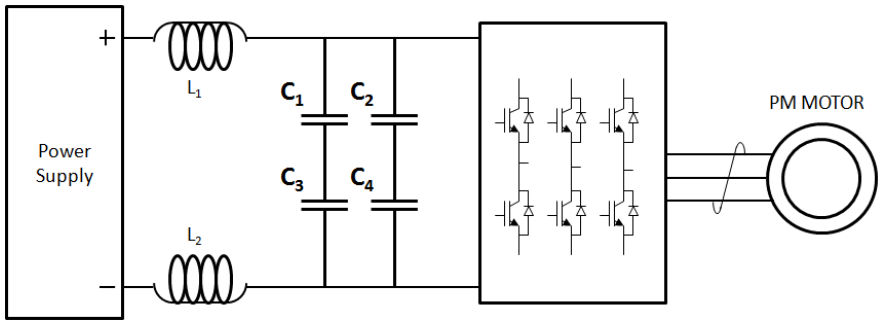


Figure 2.3 – Haylock's dc-link capacitor configuration

Such a dc-link configuration is able to withstand a capacitor open circuit and closed circuit failure. In the event of an open circuit failure, the overall dc-link capacitance is reduced. In the event of a closed circuit failure, the overall dc-link capacitance is increased. When handled correctly, the reliability of the system is increased, assuming when a capacitor fails, it is detected and replaced. However, since there are more components in the overall system, there is a higher chance of a component failure. The failure does not constitute towards a single-point failure, but the system is more maintenance intensive.

From a technical point of view, this configuration does come with many disadvantages, for example when placing capacitors in series, the effective capacitance is halved. Each capacitor still has to be overrated by the dc-link voltage in case a short circuit occurs in its series counterpart capacitor. An analysis by Argile shows that the proposed configuration is indeed much more fault tolerant [3], but comes at a price as more components are required.

2.3 Detailed study of MPPF capacitors

This section focuses on further details of how MPPF capacitors fail. This section discusses the failure modes, construction and the unique self healing property which makes this type of capacitor attractive to use in aerospace environments.

2.3.1 *Failure modes of MPPF capacitors*

Over time, the failures in MPPF capacitors may be classified in different categories. According to White and El-Husseini in [2] and [29] respectively, the typical failure

characteristic of MPPF capacitors can be described as a 'bath tub' curve shown in Figure 2.4. The failure periods are categorised in three areas:

- Early failure period
- Random failure period
- Wear-out failure period

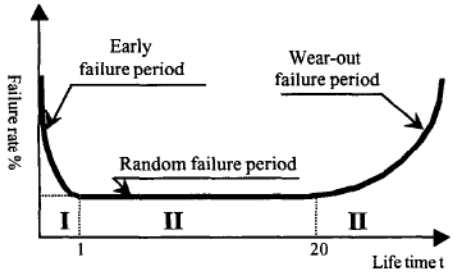


Figure 2.4 – Typical failure rate characteristic in MPPF capacitors [29]

The early failure period is usually a result of an imperfect or poor manufacturing process as well as improper operation due to design negligence. Examples are continuously applying overrated voltage or current, exposure to unspecified temperatures, improper installation etc. Mechanical failure may also arise as a result of incorrect fixation or poor soldering of the capacitor.

The second time period of the curve is called the random failure period. It is not related to any particular type of fault, and has a low failure rate statistically.

The third period is known as the wear-out failure period. In general it can be said that capacitors fail as a result of ageing and partial discharges during this period. The main causes of the wear-out failure are due to [29-31]:

- Temperature cycles/stresses – The metallised paper coil of the MPPF capacitor undergoes a great deal of mechanical stress when exposed to high temperature variations. Cracks in the metallic layers are a consequence of this, leading to a greater ESR or even open-circuit failures. Furthermore, the polypropylene dielectric tends to become brittle due to long term temperature variations. This could lead to flash through currents.
- Electrical stresses – Current ripples within the capacitor leads to electrostrictive forces (repetitive squeezing of the dielectric). The long term exposure of this type of stress results in degradation in the dielectric with the eventual cause of flash through currents.

- Corona effect – Partial electrostatic discharges occur due to enclosed air molecules in the capacitor. This failure mode will provoke electrical noise on the bus filtering until a flash through occurs resulting in the reduction of capacitance.
- Mechanical exposure – This may be caused by external issues such as the capacitor being exposed to shock and vibration for a continuous period of time resulting in the breakdown of the dielectric of the capacitor. In addition, the capacitor's bulky physical dimensions and weight also amplifies the mechanical stresses at the capacitor's fixation point.
- Environmental tear and wear. Due to general tear and wear, it is possible for the capacitor enclosure to be penetrated by moisture. This would lead to corrosion in the capacitor which in turn will lead to a significant reduction in capacitance, and eventually failure. The same problem appears due to dissimilar materials within the capacitor, for example the polypropylene dielectric and its metallic coating. Voltage and temperature difference between layers will accelerate ageing effects.

The various failures mentioned above causes the MPPF capacitor to fail either open-circuit or short-circuit in a resistive state. In most cases flash-through and self-healing is expected to occur in the ageing process. Under these events the capacitor will continue to work at a reduced capacitance, i.e. its capacitance will continuously reduce over time until it eventually fails open circuit. The self healing process is further described in section 2.3.3.

Other than losing the main function of the capacitor, the open-circuit failure is considered as a benign fault as it is not expected to result in the propagation of the failure to other components or subsystems. The fault can be prevented by placing another capacitor in parallel as redundancy.

The short-circuit resistive failure state is more worrying since high fault currents will continue to flow through the capacitor. This type of failure could lead to fault propagation in the form of heat, as currents could cause further melt down of the dielectric film. The melt down of a dielectric film could also release hydrocarbon-based gasses which are prone to ignition, potentially leading to an explosion [32].

2.3.2 *Construction of MPPF capacitors*

The MPPF capacitor cross sectional diagram can be found in Figure 2.5.

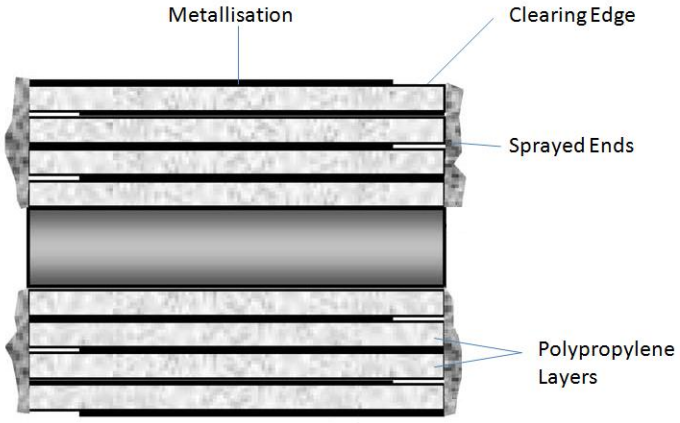


Figure 2.5 – Capacitor cross section of a typical MPPF capacitor [31]

The capacitor consists of dielectric layers of polypropylene film. The metal is evaporated in vacuum on to the film to allow a very thin layer of metal. The metal (or electrode) is typically Aluminium because of its resistance to corrosion and good bonding to polypropylene. On the axial contact sides, there is a relatively large clearance edge to avoid short circuits. To obtain high capacitance density, the entire structure is tightly rolled up in a cylindrical shape. The capacitor is sealed with a thin layer of resin to expel air cavities. Since winding the structure will add equivalent series inductance (ESL) to the capacitor, some capacitors are wound partially clockwise and partially anticlockwise to reduce the ESL effect. Finally, on both ends of the capacitor, a zinc coating is sprayed on to allow connection from all the electrodes to the external terminals [17, 31].

2.3.3 *Self healing property*

The self healing property implies that the capacitor is able to withstand (multiple) short circuit faults within the dielectric without breaking down completely. It is important to stress, that there are many type of failures that could occur, and not all of them will necessarily lead to the self healing property [33]. There are various methods of constructing MPPF capacitors to make use of the self healing property.

Carlen et al. in [34] discuss the construction of electrodes being segmented instead of having a single plane as depicted in Figure 2.6.

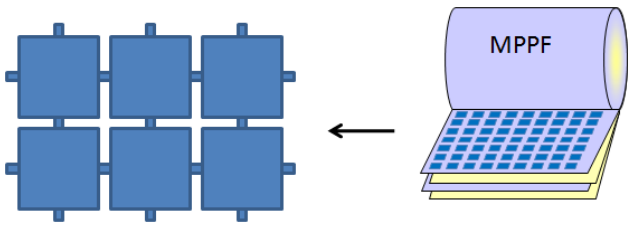
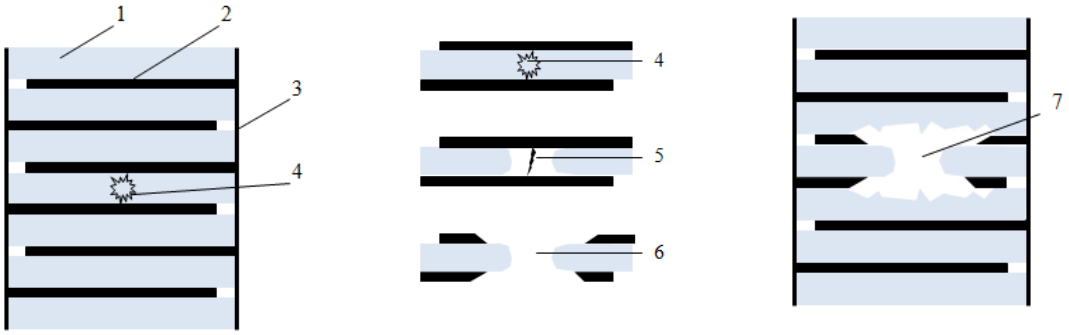


Figure 2.6 – Segmented construction of electrodes

The sectors are interconnected through narrow paths. Similar to a fuse, this path acts as a bottleneck for the current and will burn out in the event of a faulted current. In effect, the faulted sector will be isolated and hence the capacitor is able to continue functioning at a slightly reduced capacitance. The disadvantage of segmentation is that it adds towards a higher inductance value [32].

Another – more popular – way of constructing an MPPF capacitor is described by El-Husseini in [29] and WIMA in [35]. Similar to most capacitors, the electrodes are not segmented, but instead carefully designed to allow self healing to occur. Figure 2.7a shows the cross sectional area of the MPPF capacitor. In Figure 2.7b, a breakdown in dielectric is shown followed by a shorted current flowing between the electrodes. This faulted current will heat up the dielectric to such temperatures that it is transformed in to plasma. The plasma then vaporises the electrodes but it discharges relatively quickly to limit the fault from propagating within the capacitor. The result is a fault as seen in Figure 2.7c. The capacitor is therefore able to continue operating, but at a slightly reduced capacitance. The success of clearance depends on the applied voltage, thickness of electrodes as well as the mechanical pressure on individual capacitor layers [36].



(a) (b) (c)

1 – Dielectric
2 – Electrodes
3 – Sprayed ends
4 – A breakdown in the dielectric
5 – High shorted current. Dielectric transforms in to plasma
6 – Plasma melting away the electrodes
7 – Result: fault stops spreading, slightly reduced capacitance

Figure 2.7 – Self healing principle according to [29] and [35]

Ennis et al. in [37] explain that it typically takes hundreds or thousands of clearings to until a drop of a few percent is noticed. Furthermore, when a clearing takes place, certain by-products are released which will have an effect on the capacitor's electrical properties. Another side effect is a built up of internal gas pressure. The authors emphasise that these by-products are only significant after many clearances have taken place.

Anyhow, the self-healing process results in a reduced capacitance. According to Terzulli in [27] and Buiatti in [32], the theoretical end of life of the MPPF capacitor is after it has degraded by about 2% (see Figure 2.8). From then on, the capacitor will experience a significant drop in capacitance and eventually failing open-circuit.

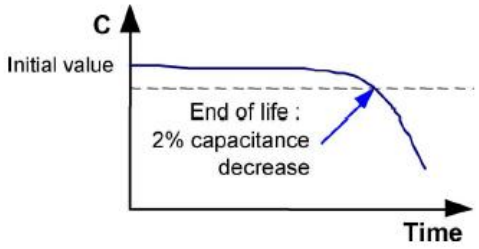


Figure 2.8 – Typical end of life behaviour of the MPPF capacitor [32]

2.3.4 *MPPF literature summary*

According to the literature, an open-circuit fault is the most common and likely fault to occur in MPPF capacitors. It is therefore acceptable to place four dc-link capacitors connected in parallel to achieve sufficient redundancy in the event of an open-circuit fault of a single capacitor. Should a capacitor open circuit take place, the remaining capacitors on the dc-link will be subject to an increased ac voltage ripple of $\frac{100}{x}$ %, where x is the value of the total number of capacitors before the fault (in the case of ELGEAR, $x = 4$, and an increased voltage ripple of 25% is observed). As a result, the remaining capacitors will experience more electrical stress even though they are typically in a similar state to the faulted capacitor (i.e. similar age, environmental exposure etc.). The chance therefore increases that a second fault in the same dc-link occurs. It is therefore advisable that the drive is inspected as soon as possible to prevent a potential dormant failure.

On the other hand should the lesser likely scenario take place where a shorted capacitor fault occurs, the drive in question will shut down. This is typically detected by the input

current sensor, which will register a surge. Consequently the controller will trip the circuit-breaker effectively isolating the faulted drive from the system. If such a scenario occurs, the remaining active redundant drive will take over operation.

2.4 Condition monitoring literature

The surveys shown in Figure 2.1 and Figure 2.2 (page 18 and 19 respectively) show that capacitor failures are 50% to 100% more likely to occur compared to power electronic failures [23, 24]. It is therefore desirable to have a system that will continuously monitor the condition of capacitors by observing its degradation in order to predict or detect a (possible) failure.

Significant amount of research has been done concerning condition monitoring of capacitors. Most of this research is related to electrolytic capacitors, although some papers, (e.g., Buiatti et al. [32]) discuss condition monitoring on MPPF capacitors. Most papers describe a condition monitoring technique by analysing the degradation of capacitance and ESR [17, 19, 24, 38]. Both variables are required for electrolytic technology due its sensitivity to temperature. A single variable alone does not necessarily indicate whether an electrolytic capacitor is degrading or simply being exposed to a varying temperature. According to Abdennadher et al. in [19], there is a generally accepted practice that electrolytic capacitors are considered to be at the end of their lives when the capacitance drops by 20% or their ESR doubles.

2.4.1 *Offline monitoring systems – by removal of the capacitor*

Since the work presented focuses on an online monitoring system, the literature of offline monitoring systems is only briefly covered here.

Offline monitoring systems are one of the simplest methods of monitoring. Literature indicates that capacitors are physically taken out of a circuit, and are subject to tests using RLC network analysers or equipment to analyse the capacitor's reduction in weight due to evaporation of the electrolyte [38]. The disadvantage however arises when issues such as ease of maintenance, cost, frequency of inspection and practicality are taken into account. Offline systems only provide a one off sample, ignoring the importance of operational load, temperature variations and the capacitor's individual health history [17] [27].

2.4.2 *Online monitoring systems – keeping the circuit intact*

A more popular type of condition monitoring system is an online in-circuit testing system where the capacitor is not taken out of the circuit. Typically additional electronics are integrated in the design and will perform regular checks during which the capacitor is not operational. Examples include during periods where the system is powered down or on standby.

Venet et al. in [39] use a simple and easy implementation circuit that computes the ESR of the capacitor in a power supply application. The authors are able to monitor the ESR to an accuracy of 10% which they claim is a good enough indication of when the capacitor needs to be replaced. In a similar case, Lahyani et al. in [40] compute the ESR in static converters to predict when the capacitor fails.

A method for diagnosing the health in capacitors in uninterruptible power supplies (UPS) and adjustable speed drives (ASD) are outlined in [38] by Aeloiza. The authors propose an online monitoring technique where the ESR is measured as the system is in operation. The proposed implementation is shown in Figure 2.9.

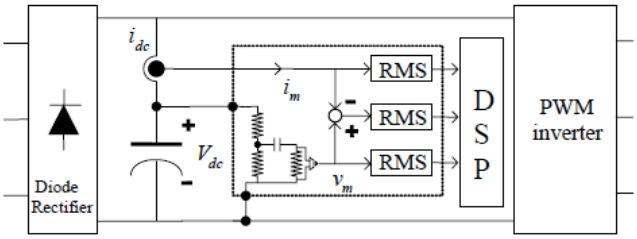


Figure 2.9 – Proposed condition monitoring by Aeloiza et al. [38]

The method makes use of analogue circuits and a current transducer in series to the capacitor to obtain the current and voltage ripples. The problem with this approach is that the transducer adds unwanted inductance to the circuit. In practice, the connection between the capacitor and the dc-link are kept small to ensure the ESR and ESL remains minimal. This is especially important for MPPF capacitors where the connection resistance may have a relatively large contribution to the total ESR. It is therefore very difficult to fit a current transducer at this point due to physical constraints [32].

Kwang-woon et al. in [17] discuss a health monitoring system on a drive. The dc-link capacitors are diagnosed when the motor is stopped. Once stopped, the inverter is no longer used to drive the motor, and can be used for monitoring instead. The technique uses the inverter to inject a current in the capacitors, and in turn it calculates the

capacitance and the ESR. An advantage is that no external equipment is required. The disadvantage however is that it still provides a one-off value, as it cannot be used whilst the motor is in operation. The number of samples taken may be limited and irregular, depending on how often the motor is offline.

Similar to the previous paragraph, Lee in [41] discuss a health monitoring system on a drive using a three phase back to back (AC/DC/AC) PWM converter. The monitoring operates under no load where the AC/DC converter injects a defined low frequency ac signal in to the drive which appears on the dc-link. Using digital filters, the ac voltage and current components are acquired and the dc-link capacitance can be calculated. The authors claim an accuracy of less than 0.26%.

In another case, Buiatti et al. in [32] monitor the health of an MPPF dc-link capacitor in a drive for the railway power train application. The monitoring technique calculates the capacitance only, and during the period when the drive is shut down. As part of the shut down procedure, the braking circuit in the drive discharges the dc-link capacitor rapidly and by monitoring the current and the voltage, the capacitance is derived. The authors claim that several calculations can be made in a day (i.e. each time the drive is switched off).

2.4.3 *Conclusion*

MPPF capacitors have more advantages than the electrolytic alternative, especially for aerospace applications. The main disadvantage of MPPF technology is that the costs and package size are significantly greater than that of electrolytic technology. Nevertheless, the disadvantages are justified in the gains of reliability, considering the consequences of a capacitor failure.

The work described in these papers sometimes involves additional hardware that may be difficult to implement in practice for the aerospace application. In terms of the aerospace application, an offline system where the capacitor is taken out of the circuit is not an option. It is impractical and too expensive for maintenance reasons.

The papers discussing an online monitoring system improve the method of sampling significantly, compared to an offline system. Nevertheless the monitoring techniques in the literature still only sample during very specific conditions (i.e. under no-load condition, when the motor is off, when the drive is off or shutting down etc). Some papers introduce additional external components to improve the accuracy of their

system, such as ac signal injection. It is also important consider reliability and availability when introducing more components than necessary. In general, for the aerospace application, the online monitoring technique is more plausible. However, the literature indicates that current online condition monitoring still provides a one-off sample rather than a continuous monitoring system whilst the drive is operational.

Proposed Monitoring Design

Chapter 3

3.1 Introduction

This section focuses on the theory and simulation of the proposed monitoring technique. Using this method, predictions can be made about the feasibility of the techniques as well as highlighting any difficulties in practical implementation. Finally, the parameters of the condition monitoring technique are defined for the ELGEAR project.

The condition monitoring technique that is presented in this thesis is a novel way of monitoring capacitors in drives. The technique provides capacitance measurement data in fractions of a second and is therefore able to detect a sudden loss in capacitance almost instantly. In contrast to the current literature, it allows continuous health monitoring of dc-link capacitors during nominal operation of the drive. Furthermore, the system is capable of operating under variable torque and speed conditions and is therefore flexible to adapt to various applications. The proposed technique makes use of existing current and voltage sensors which need to be modified slightly to interface with the existing hardware.

3.2 Matlab Simulink

In order to design the proposed capacitor monitoring technique, it is first simulated in the Matlab Simulink environment. The aim of the simulation would be to determine the parameters that have to be taken in to account when designing the condition monitoring system. Another advantage of a simulation model is that it acts as a comparison to the practical implementation.

The model differs from the ELGEAR drive in the sense that it is not fault tolerant. Only one drive is simulated, since its companion drive is identical. The condition monitoring technique only monitors the condition of one dc-link using the variables from the same drive. This therefore justifies why only one drive is used in the simulation.

The electrical diagram implemented in the simulation is shown in Figure 3.1. The dc-link input voltage is ±270 V dc. Since the simulation cannot cope with a single capacitance that bridges the positive and negative part of the dc-link bus, it has been

decided to split up the capacitors (i.e. C_1 and C_2). Each has a capacitance of 160 µF to allow a total capacitance of 80 µF for the series combination. The centre point of the capacitors is linked to ground via R_n to allow the simulation to work. The value of R_n has been made considerably large so as to assume that the centre point is effectively isolated from ground. For the same reasons, R_n can also be found in the star point of the motor. The whole simulation is representative to an aircraft symmetrical power system.

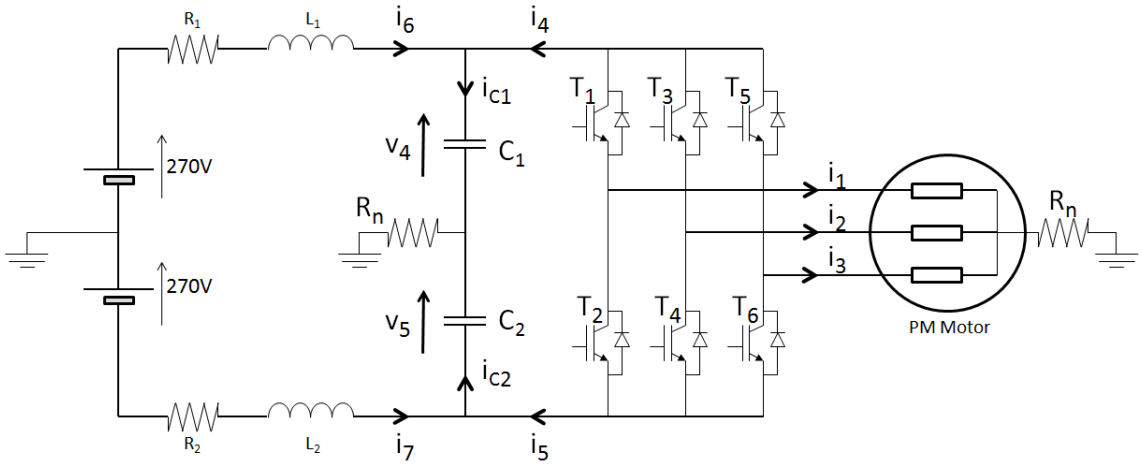


Figure 3.1 – Diagram layout of the Matlab Simulink model

The simulation model of the drive is set up in the Matlab Simulink environment. The overall scheme can be found in Figure 3.2. The simulation model shows 6 subsystems:

- The motor
- The controller
- The inverter
- The dc-link
- The state change (part of the proposed monitoring technique)
- The capacitor calculation (proposed monitoring technique)

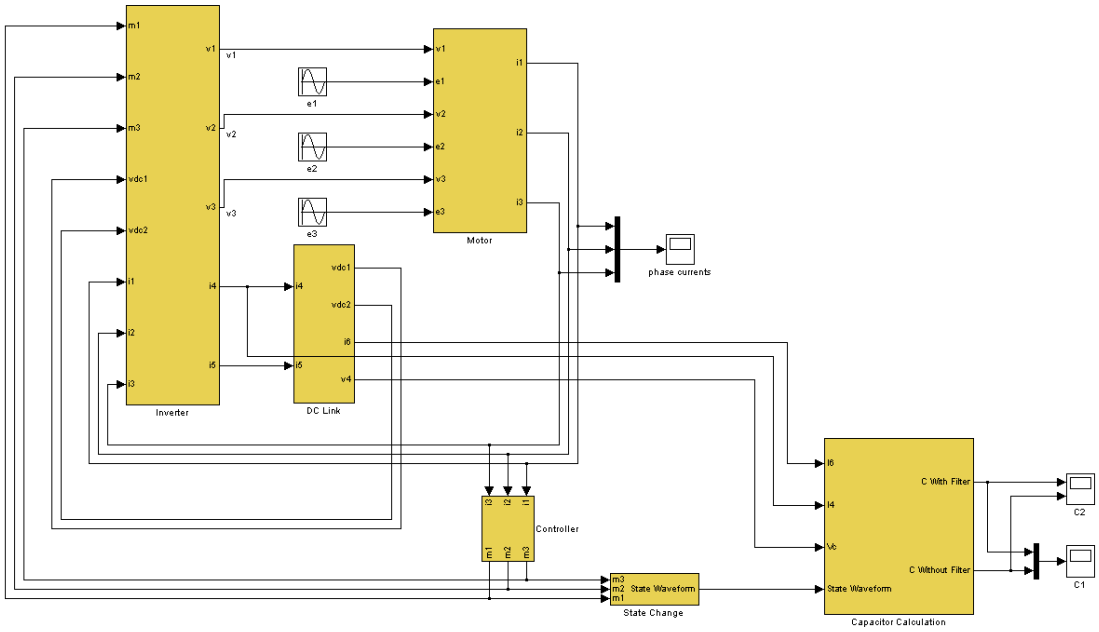


Figure 3.2 – Overall Matlab Simulink of the motor drive

3.2.1 *The motor*

The 3-phase star connected motor is modelled in the simulation block "motor" in Figure 3.2. The emf seen on each of the phases is modelled as a constant sinusoidal waveform displaced by 120°for each of the phases, since the steady state condition is assumed. The motor sub-system is detailed in Figure 3.3.

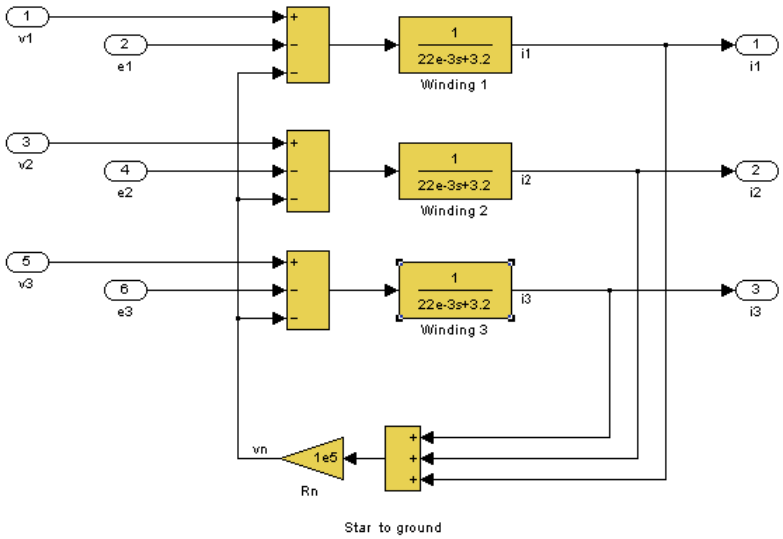


Figure 3.3 – Motor sub-system

The winding transfer function for each phase is based on equation (3.1), where the phase inductance is 22 mH and the phase resistance is 3.2 Ω.

$$v = L\frac{di}{dt} + iR + emf$$

$$v - emf = L\frac{di}{dt} + iR$$

$$v - emf = (Ls + R)i \qquad \text{(Laplace transform, frequency domain)}$$

$$i = (v - emf)\left(\frac{1}{Ls + R}\right) \qquad (3.1)$$

An additional high impedance resistance R_n is modelled in the diagram since the simulation model cannot cope without it (discussed earlier).

3.2.2 *The controller*

The controller sub-system is shown in Figure 3.4.

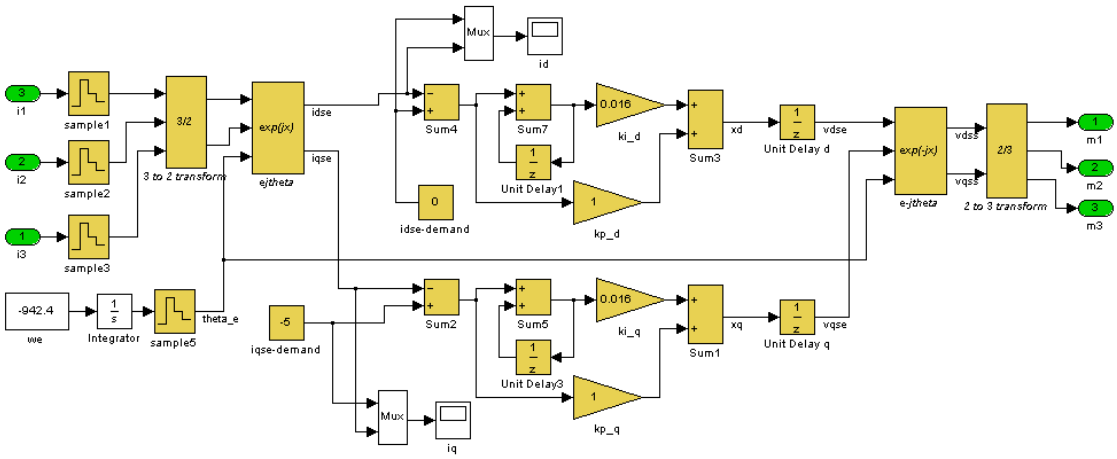


Figure 3.4 – Controller sub-system

The controller is a sampled digital controller, where the motor phase currents (i_1, i_2, i_3) are sampled at 10 kHz to be synchronous with the PWM carrier signals. The sampling blocks (sample1, sample2, sample3) are effectively analogue to digital converters (ADCs). The sampled currents are then transformed into the synchronous reference frame by blocks "3 to 2 transform" and "ejtheta" to obtain the d-axis and q-axis, stator excitation currents (idse and iqse respectively). The currents are then compared with its demanded currents (idse-demand and iqse-demand) to produce the error. Since no field weakening takes place, the idse-demand is set to zero.

The d and q axis current errors are fed to discrete PI controllers. For the d-axis error, the discrete integrator is composed of the block "Sum7" and "Unit Delay1". The delay

block is set to 100 μs corresponding to the 10 kHz sampling rate. The proportional gain is noted as kp_d and kp_q for the d-axis and q-axis PI controller respectively. Similarly, the integral gain is noted as kp_d and kp_q.

The output of the PI controllers for the d-axis and q-axis are xd and xq respectively. Unit delays are included to represent one sample execution time delay in the controller hardware. The signals are now the demanded voltage for the d-axis and q-axis. They are now transferred back to the stator reference frame to obtain the modulation signals (m1, m2, m3). The modulation signals interface with the inverter, as shown in the overall scheme in Figure 3.2 page 32.

3.2.3 *The inverter*

The inverter sub-system is shown in Figure 3.5. The three inverter legs are modelled as ideal switches, leg 1, leg 2 and leg 3. The inverters are switched using a basic PWM switching scheme at 10 kHz.

Three more switching legs are implemented with a 2 μs delayed time named leg 1_d, leg 2_d and leg 3_d. These create almost identical switching states, except that all of them are delayed by 2 μs. The delayed signal is used to compensate for a dead-time of 2 μs in the calculation. Using a switch, the dead-time influence can be switched off if necessary.

A third set of logic comparators output the direction of the current. This signal is used by the simulator during the dead-time state to determine whether the current would flow from the motor to the positive dc-link, or from the negative dc-link into the motor.

The “voltage calculation” block consists of a matrix lookup table that connects *vdc1* and *vdc2* to the motor phase voltages depending on the 9 digital input states. Similarly, the “current calculation” block calculates the currents flowing in to the dc-link using the same input parameters.

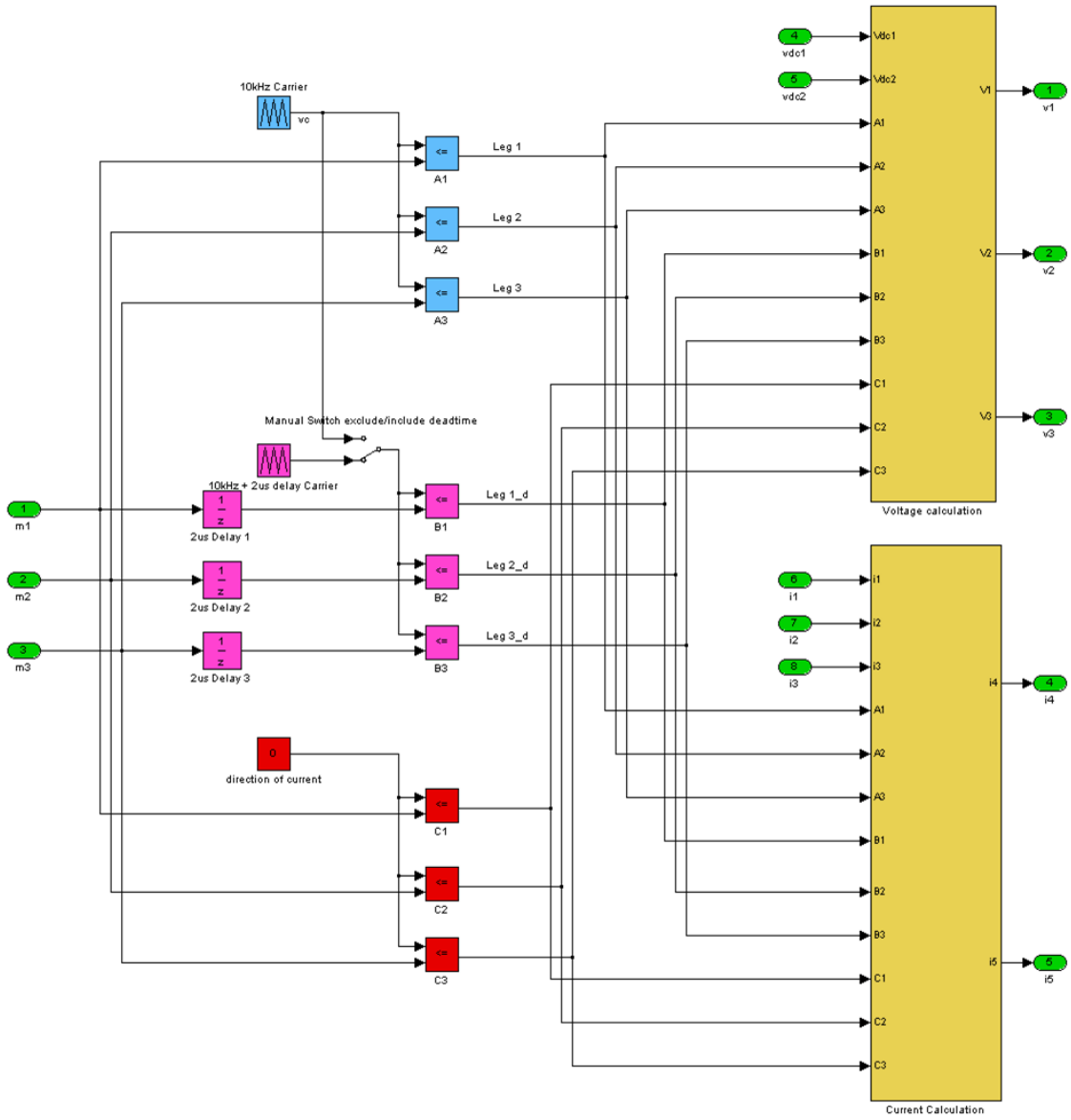


Figure 3.5 – Inverter internal structure

3.2.4 *The dc-link*

The internal structure of the dc-link circuit, shown in Figure 3.6 can be related directly to Figure 3.1 page 31. To calculate the current i_6, the following equation is derived from Figure 3.1:

$$270 - i_6 R_1 - L\frac{di_6}{dt} = v_{dc1}$$

$$\frac{di_6}{dt} = \frac{270 - i_6 R_1 - v_{dc1}}{L} \qquad (3.2)$$

The current i_6 is derived by integrating equation (3.2). Similarly, the current i_7 can be derived for the negative dc-link. The current i_6 is then added to i_4 – which originates from the inverter – to derive the capacitor current i_{c1}. At this point an amplifier block "1/C" is found which merely consist of a 160 µF capacitor. The internal structure of the 1/C block includes a setting where it could change the capacitance value after a given time period. This would simulate a capacitance fault. The signal is then integrated to obtain v_4, which is consequently added to v_5 to obtain the positive dc-link.

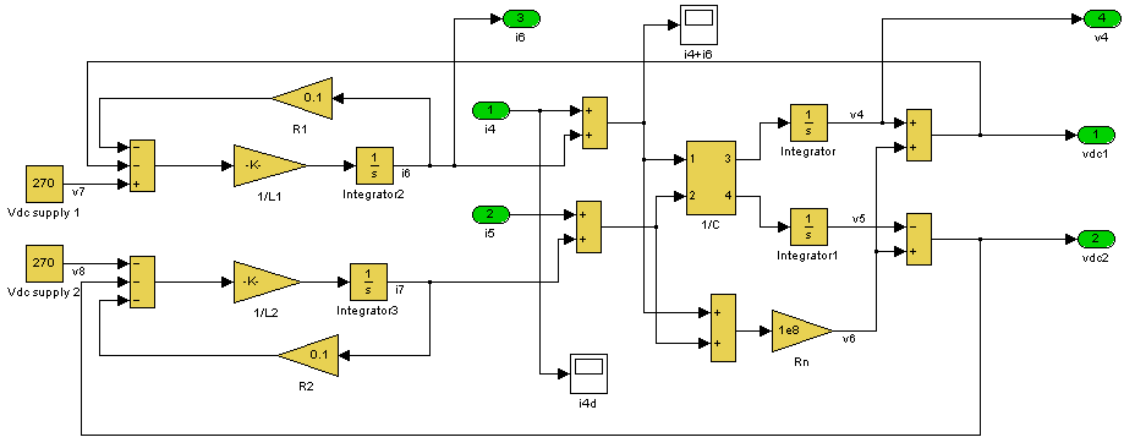


Figure 3.6 – Dc-link internal structure

3.2.5 *Capacitor calculation*

The state change and capacitor calculation blocks are covered in the following chapters in more detail.

3.3 Proposed dc-link capacitor condition monitoring system

The theory of monitoring the health of capacitors rests on the principle shown in Figure 3.7. Four parallel connected capacitors of 20 µF are modelled as a single 80 µF capacitor. An open circuit failure in one capacitor is therefore equivalent to a drop in capacitance of 25%.

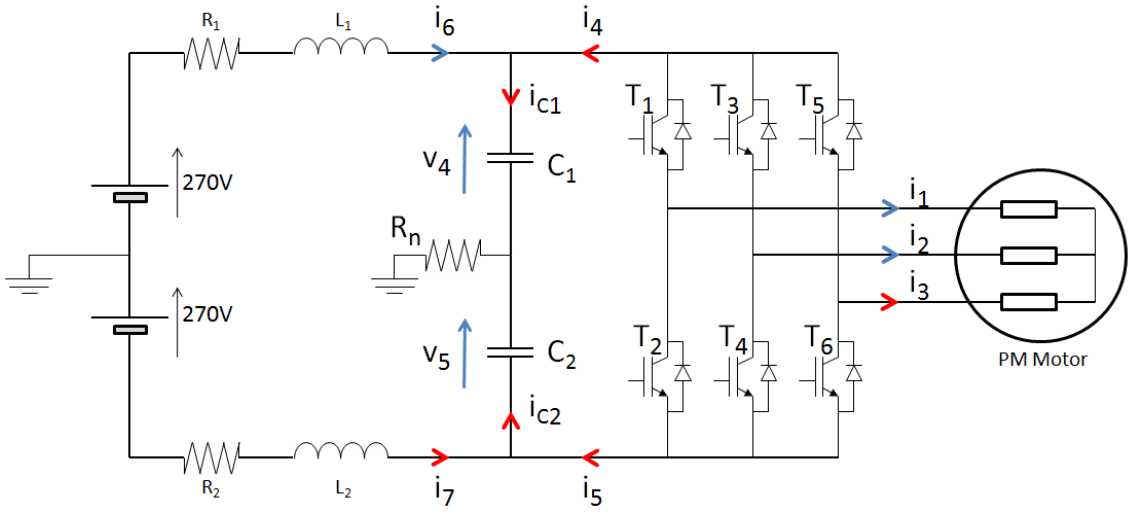
During normal operation, the IGBTs in the inverter switch at a frequency of 10 kHz. This will cause ripple voltages and currents to flow from the inverter to the dc-link bus. The inductor/capacitor dc input filter prevents the ripple from travelling to the power supply unit. More detailed information on the filter can be found in section 3.3.2 (page 40).

The dc-link capacitance can be calculated using the current flowing into the capacitor (i_c) and the voltage ripple across it (Δv_c). The formula for calculating the capacitance is shown in equation (3.3).

$$I_c = C\frac{dv_c}{dt}$$

$$C = \frac{\int I_c dt}{\Delta v_c} \qquad (3.3)$$

Due to given physical design constraints of the hardware, it is not feasible to place a current transducer at point i_{c1} or i_{c2}. This being that the dc-link capacitor has to be as close to the inverter as possible to minimise stray inductance [32]. To calculate C_1, the current i_{c1} has to be derived using the sum of i_6 and i_4. Similarly, the sum of i_7 and i_5 is used to calculate C_2.



Blue arrows (i_1, i_2, i_6, v_4, v_5) denote a sensor

Red arrows represent a calculated value using the blue sensors

Figure 3.7 – Motor Drive Electronics according to Matlab Simulink

The calculations below show how the total capacitance (C) is derived using the diagram in Figure 3.7. Finally, the formula in equation (3.4) is used to calculate C.

$$C = \left(\frac{1}{C_1} + \frac{1}{C_2}\right)^{-1}$$

since $C_1 = \dfrac{\int I_{C_1} dt}{dv_4}$

and $C_2 = \dfrac{\int I_{C_2} dt}{d(-v_5)}$

$$C = \left(\frac{dv_4}{\int I_{C_1} dt} - \frac{dv_5}{\int I_{C_2} dt} \right)^{-1}$$

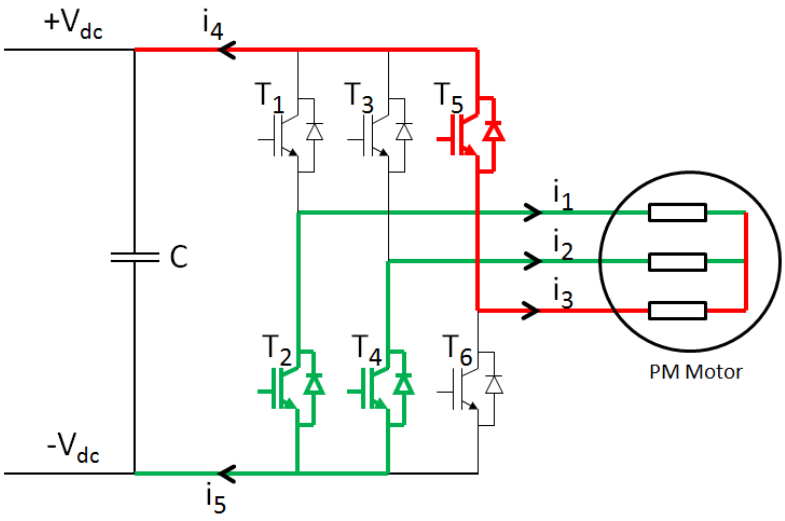
since $I_{C_1} = -I_{C_2}$

and $v_4 = v_5$

$$C = \left(\frac{dv_4}{\int I_{C_1} dt} + \frac{dv_4}{\int I_{C_1} dt} \right)^{-1}$$

$$C = \left(\frac{2dv_4}{\int I_{C_1} dt} \right)^{-1} = \frac{\int I_{C_1} dt}{2dv_4} \qquad (3.4)$$

Due to similar design constraints as mentioned above, no current transducer can be placed at point i_4 either. Instead, the current i_4 can be derived using the motor phase currents and the switching states of the IGBTs. For example, for a given state where transistors T_2, T_4 and T_5 are on, the current will flow from the $+V_{dc}$ bus through T_5, in to the motor and out to the $-V_{dc}$ rail via T_2 and T_4 as Figure 3.8 shows.



Red lines represent currents flowing in to the motor

Green lines represent currents flowing out of the motor

Figure 3.8 – Example of current flow for a given state when *T2*, *T4* and *T5* are on

The current i_4 can now be expressed in terms of the motor phase currents as shown in equations (3.5) and (3.6).

$$i_4 = -i_3 \quad (3.5)$$

$$i_4 = i_1 + i_2 \quad (3.6)$$

Similarly, the current i_5 can be expressed in terms of the motor phase currents in equations (3.7) and (3.8).

$$i_5 = i_3 \quad (3.7)$$

$$i_5 = -(i_1 + i_2) \quad (3.8)$$

The theory of deriving i_4 can be applied to all states, as shown in Table 3.1. The current i_c is then derived since: $i_c = i_6 + i_4$.

State	**Transistors on**	**Current i_4**
1 (zero voltage state)	T_2 T_4 T_6	*0*
2	T_2 T_4 T_5	$-i_3$
3	T_2 T_3 T_6	$-i_2$
4	T_2 T_3 T_5	$-i_2-i_3$
5	T_1 T_4 T_6	$-i_1$
6	T_1 T_4 T_5	$-i_1-i_3$
7	T_1 T_3 T_6	$-i_1-i_2$
8 (zero voltage state)	T_1 T_3 T_5	$-i_1-i_2-i_3 = 0$

Table 3.1– Currents of i_4 related to its transistor state

3.3.1 *Required sensors*

It can be seen from the equations, Table 3.1 and Figure 3.7, that most of the currents can be derived; only few need to be measured. Referring to the figure, the arrows in red and blue show a derived and measured value respectively.

Due to the isolated star-point of the PM motor, the sum of the motor phase currents is always zero; $i_1+i_2+i_3=0$. Only two current transducers are required to derive all three motor phase currents ($i_3= -i_1-i_2$). Moreover, the motor phase current sensors are already present in the system for the current feedback in the control scheme.

The dc-link input current sensor (i_6) is also part of the monitoring scheme. The input current sensor measures the average current filtered by the coils and dc-link capacitor. This sensor is also already present in the system, since it is used for over-current protection. The sensor is typically linked to a circuit breaker to isolate the drive from the main supply.

Finally, the voltage sensor $v_c = v_4 + v_5$ needs to be connected to the terminals of the capacitors. Again, a dc-link voltage sensor would often be present for protection and control improvement.

3.3.2 *Design of a dc-link input filter for ELGEAR*

To be able to measure ripple voltages across the dc-link capacitor with sufficient accuracy, an input filter according to Figure 3.9 is required, where series inductors form a filter with the dc-link capacitors.

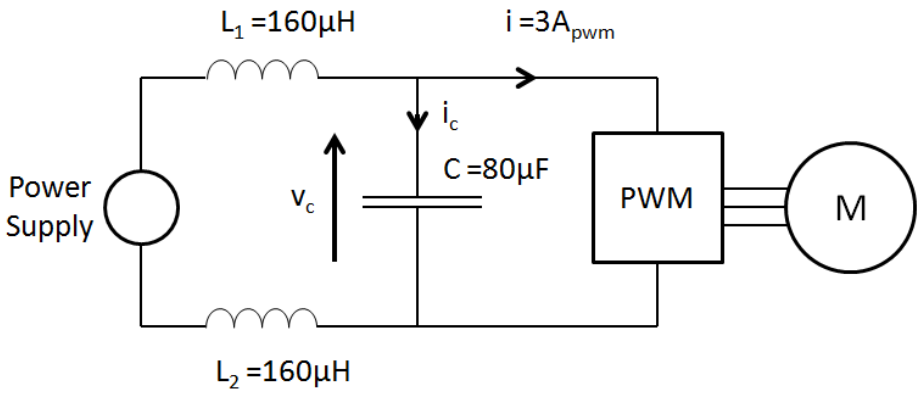


Figure 3.9 – Dc-link capacitor equivalent currents

The introduction of inductors has two main features:

1. The DO-160F standard [13] requires that PWM harmonics of an electrical system are isolated from the dc-link bus. The inductors are used to effectively increase the (ac) source impedance which in turn minimises the amount of PWM harmonics travelling back into the supply.
2. Higher frequency waveforms, including the voltage ripple seen on the dc-link, are isolated from the power supply. If these inductors are not present, the power supply – which acts as a voltage source – will help filter the ripple voltages. This would not make measurements possible, as the power supply will act as a large capacitor.

Referring to Figure 3.9, at a frequency of $f = 10kHz$ the impedance of the dc-link capacitor $C = 80\mu F$ is $X_C = 0.20\Omega$. To achieve the 1% shunt target at $f = 10kHz$ the dc-link impedance must be raised by factor 100 (i.e. to 20 Ω). The corresponding inductance calculated is 320µH.

In order to verify whether the dc-link filter is compliant with the aviation standard document, DO-160F [13], an analysis of the set up is performed below.

DO-160F specification

Maximum Power:	$540V \times 3A = 1620W$
DO-160F category:	$1kW...10kW$
Maximum current ripple allowed by DO-160F (see section 1.4.2 page 7):	$0.14 \times 3 = 420mA_{peak-peak}$

Dc-link filter design

Motor current:	$3A$ (for active PWM)
PWM frequency:	$10kHz$
Maximum ripple voltage Vc (see Table 3.3, page 50):	$1250mV_{peak-peak},\ C = 60\mu F$
Capacitor (Worst case, i.e. one capacitor open circuit):	$60\mu F$
Inductors:	$2 \times 160\mu \rightarrow X_L @ 10kHz = 20.1\Omega$
Dc-link current ripple:	$\frac{V_C}{X_L} = 62.2mA_{peak-peak}$

The filter is fully compliant to DO-160F since a ripple of 62.2 mA is observed where a 420 mA ripple is allowed.

3.3.3 *Zero voltage state monitoring*

Whilst the system is delivering power, states 2 to 7 are used. In Table 3.1, it can be seen that state 1 and state 8 are also used. These are known as the zero voltage states where power is not delivered from the inverter to the motor since the motor is effectively short circuited. Within the motor coils, there is still a current flowing; hence the motor is still delivering torque.

During these zero voltage states, the calculation is simplified since current i_4 becomes zero in the calculation (i.e., $i_c = i_6$). An example of such a zero voltage state is depicted in Figure 3.10.

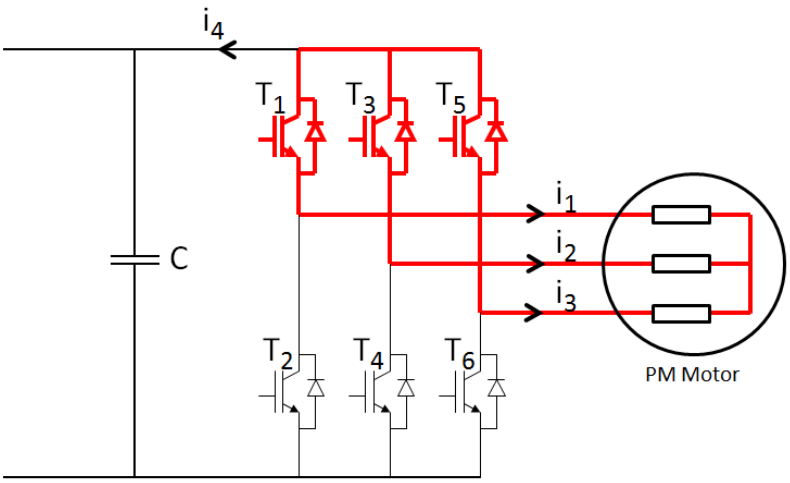


Figure 3.10 – During zero voltage state sampling, $i_4 = 0$

The zero voltage state is used for various reasons. Controllers are generally designed to use zero voltage states during every PWM cycle under nominal operation. The zero voltage states allow the magnitude of voltage to be controlled at a particular voltage vector angle.

3.3.4 *Zero voltage state current calculation*

During this period, a constant current will flow into the inverter (due to the input inductance). This will directly charge the dc-link capacitors, since no power is delivered to the motor.

Figure 3.11 is a representative diagram where the inverters are modelled as one phase at 10 kHz. The power supply and the inductors are modelled as a current source at 10 kHz. The PWM represents the total pulse-width-modulation of the 6 IGBTs seen on the dc-link. The higher the duty ratio, the more power is delivered to the motor.

To avoid confusion between the representative one phase system, and the actual three phase motor drive electronics, the currents have been labelled differently. The input current (measured at i_α) is equal to the mean value of the PWM duty ratio.

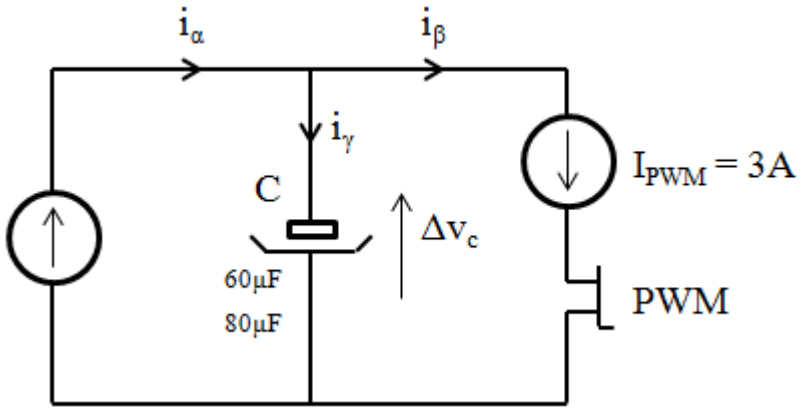


Figure 3.11 – Dc-link capacitor equivalent currents, where the drive is modelled as one phase @ 10 kHz

The value of the capacitor C was derived in equation (3.3) on page 37:

$$C = \frac{\int i_\gamma dt}{dv}, \text{ where } i_\gamma = i_\alpha - i_\beta .$$

3.4 Simulating the proposed condition monitoring system

This section shows the simulation in Matlab Simulink of the condition monitoring system.

3.4.1 *Drive simulation*

Figure 3.12 shows the dc-link ripple voltage (v_c), motor phase currents (i_1, i_2 , i_3), input current (i_6) and the transistor states of the simulated drive in operation. The ripple voltage shows a triangular charge/discharge cycle. The motor phase currents remain approximately constant as a result of the motor's relatively high inductance. At the bottom of the graph, the transistor states are shown, which correspond to Table 3.1, page 39. Note that state 0 in the graph represents the dead time. The zero voltage states are represented by state 1 and state 8.

The estimation algorithm relies on a technique where it samples the voltage and current a number of times within the period of a specific transistor state. Using the samples, the system is able to calculate $\int I$ (average i_c), dv and dt. The higher the number of samples taken, the more accurate the calculation will be. The time interval between the samples is programmed to be 4 µs. Depending on the modulation index defined by the control scheme, the duration of the period of a specific transistor state will vary as the modulation index varies. This means that some periods will not be long enough for

accurate sampling. It has therefore been decided to ignore all calculations that are based on three samples or less.

An example of two calculations is given during state 1 and state 6 in Figure 3.12 and Table 3.2.

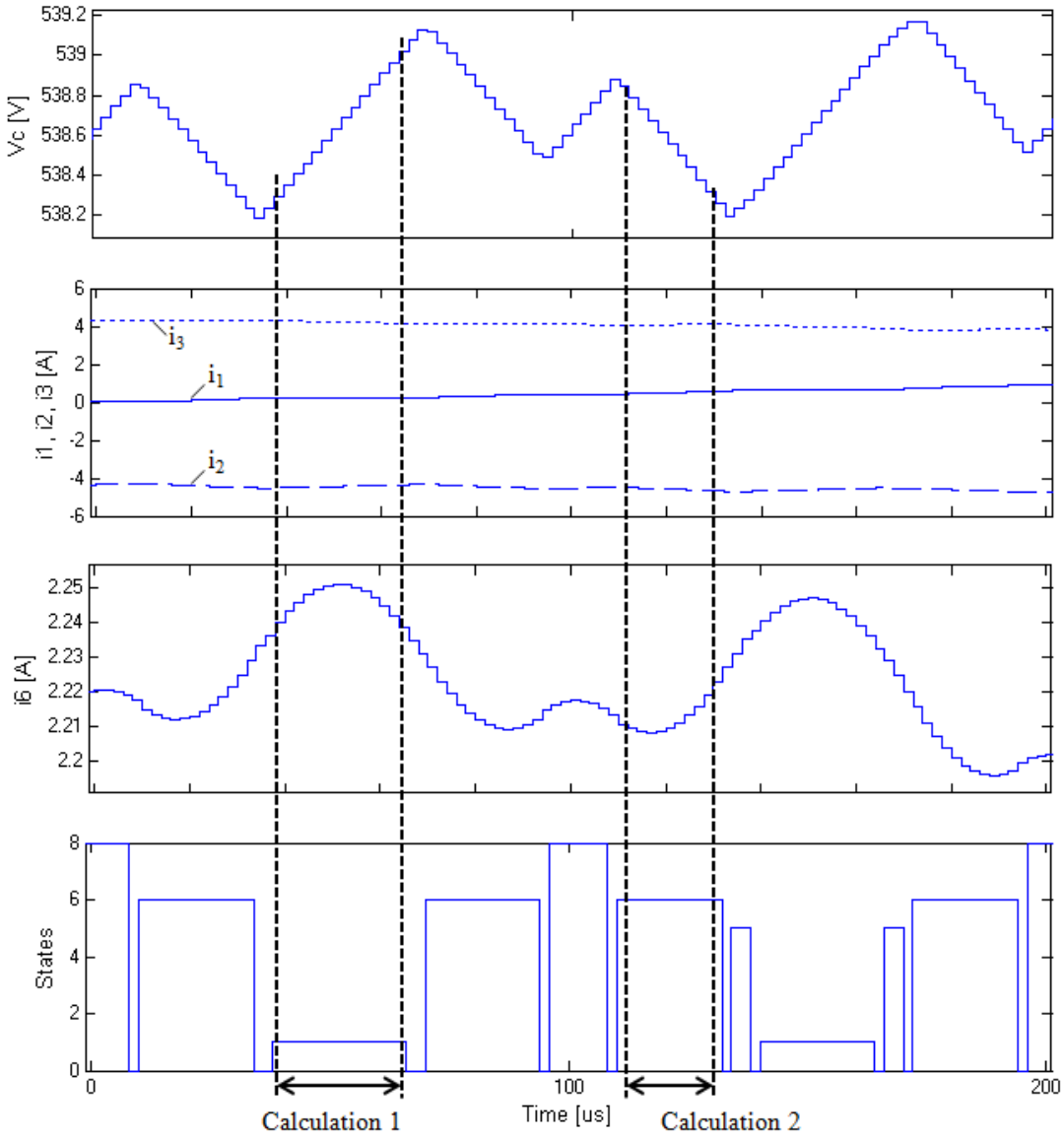


Figure 3.12 – Snap shot in time of v_c, i_c, i_1-i_4 and transistor states

	Calculation 1	Calculation 2	Units
Transistor state	1	6	
dv	0.80	-0.65	V
i_6	2.245	2.215	A
i_1	0.22	0.500	A
i_2	-4.45	-4.585	A
i_3	4.23	4.085	A
dt	28e-6	22e-6	s
i_c (calculated)	i_6 = 2.245	i_6-i_1-i_3 = -2.37	A
C	**78.6**	**80.2**	**µF**

Table 3.2 – Approximate analytical calculation of the capacitance

During state 1, $i_1 = i_c$, and therefore, the only current measurement required in this calculation is i_1 (similar to the diagram in Figure 3.10).

$$C = \frac{\int I_C dt}{dv_C} = \frac{2.245 \times \left(28 \times 10^{-6}\right)}{0.80} = 78.6 \mu F$$

Calculation 2 is based on transistor state 6. Following state 6 in Table 3.2 currents i_1 and i_3 are used to find i_4.

$$i_4 = -i_1 - i_3 = -0.50 - 4.085 = -4.585$$
$$i_c = i_6 + i_4 = 2.215 - 4.585 = -2.37$$
$$C = \frac{\int I_C dt}{dv_C} = \frac{-2.37 \times \left(22 \times 10^{-6}\right)}{-0.65} = 80.2 \mu F$$

It is evident that the estimation technique is reasonably accurate since the capacitance value in the simulation is set to 80µF.

3.4.2 *Capacitor open circuit fault simulation*

In order to determine how effective the monitoring system is, a simulated 20 µF capacitor open-circuit is implemented. The capacitance is instantly reduced from 80 µF to 60 µF, at 50 ms in to the simulation.

The graph in Figure 3.13 shows the calculated capacitance of the simulator. The top graph shows the capacitance calculation using the zero voltage state. In the above sections it has been determined that the monitoring technique functions best when calculations take place during the zero voltage state. Another non-zero voltage state is picked at random (6th state) so as to compare both monitoring techniques. The bottom graph shows the calculation during the 6th state.

In both cases, the monitoring technique appears to be reasonably accurate. Clearly, it can be seen that the simulation using the zero voltage state reacts almost instantaneously whereas the 6th state monitoring shows a delay in the order of milliseconds. Other states (1-7) show similarities to the 6th state in terms of its delayed reaction. This is due to the number of successful samples as well as the frequency of sampling. In general, the zero-state occurs at a much higher frequency than other states. Furthermore, the zero voltage state duration is generally much longer and therefore allows more multiple sampling.

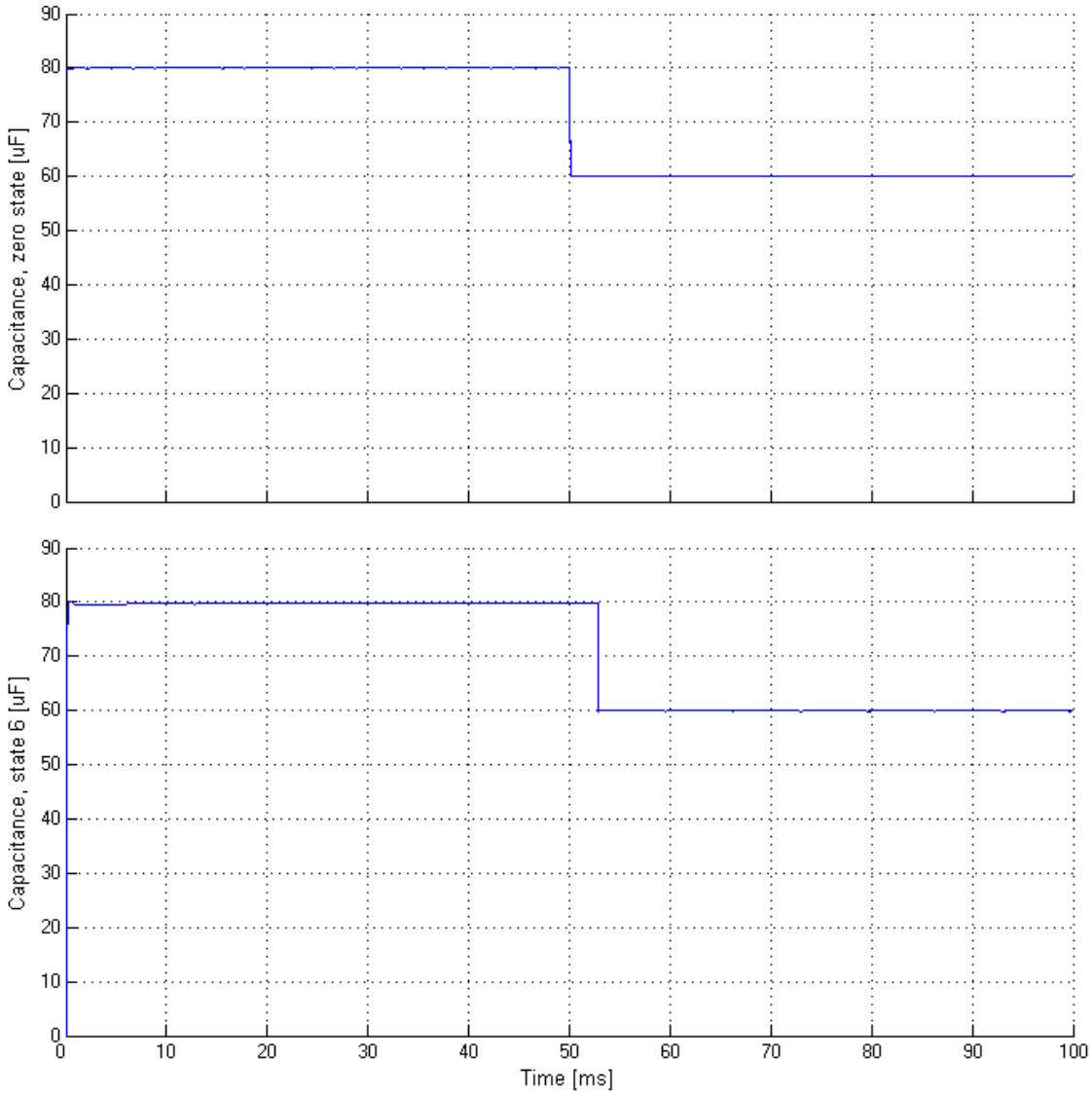


Figure 3.13 – Result of the monitoring simulation. Top graph, monitoring on the zero voltage state. Bottom graph, monitoring on state 6. Capacitor change programmed to switch from 80µF to 60µF at t=50ms.

The graph in Figure 3.14 shows the accumulation of the number of successful calculations that have taken place. After 100ms, the zero-state method has performed just over 900 calculations, corresponding to a refresh rate of 9 kHz. In contrast, the state

6 method only performed 16 calculations corresponding to a refresh rate of 160Hz. This would explain the delayed reaction of the 6th state method compared to the zero voltage state method after the capacitor is switched out.

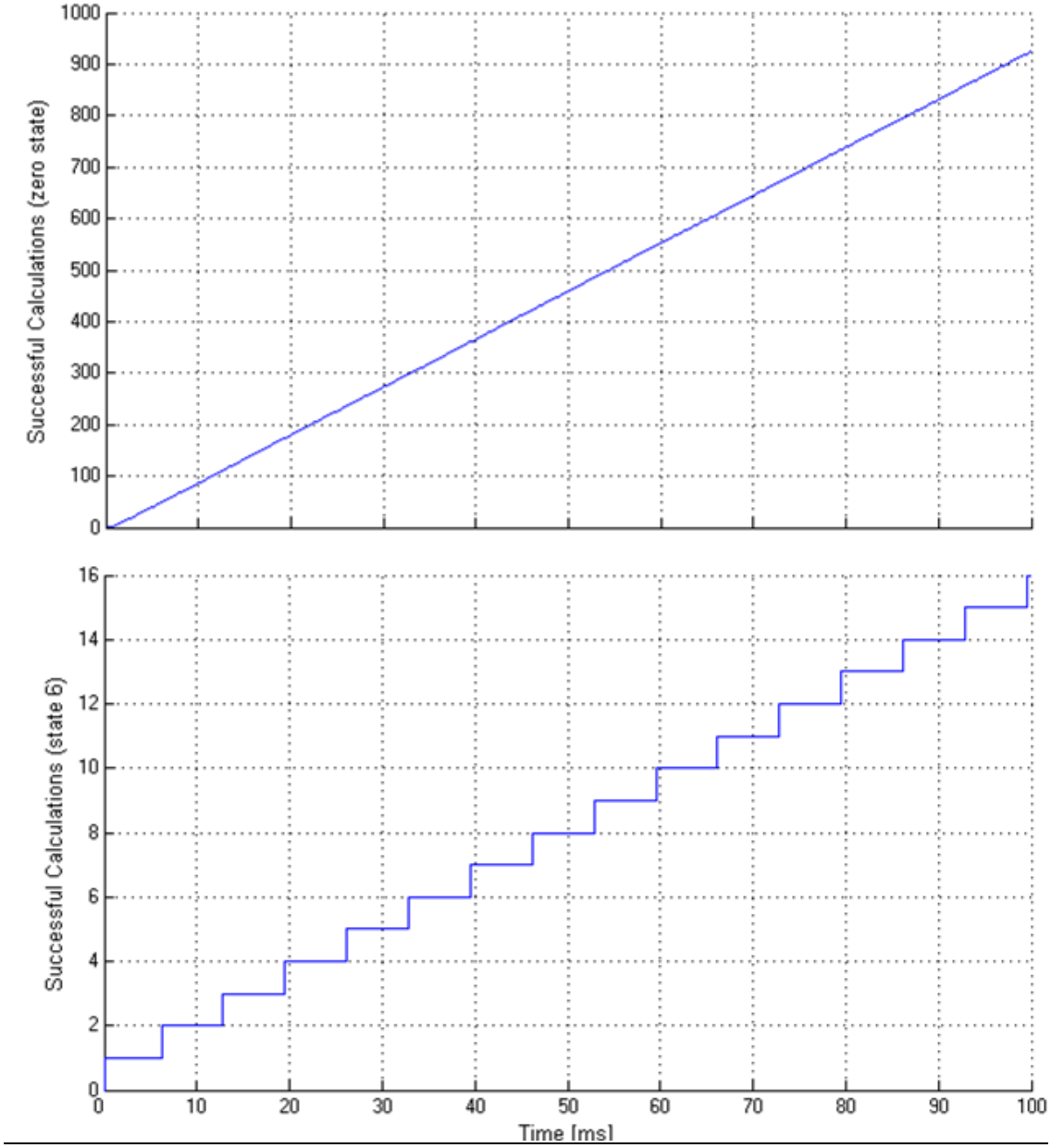


Figure 3.14 – Number of successful calculations for the zero voltage state (top) and state 6 (bottom)

3.5 Hardware layout

The condition monitoring hardware principle is outlined in Figure 3.15. The inverter is commutated by means of a main controller. The main controller uses feedback signals from the motor phases, and is analogous to the control electronics described in Figure 1.8, page 13.

The condition monitoring consists of a timing circuit, voltage and current monitor which sample the required variables as stated in equation (3.3):

$$C = \frac{\int I_c dt}{\Delta v_c}$$

The variables are then passed on to the estimator where the capacitance is calculated and displayed.

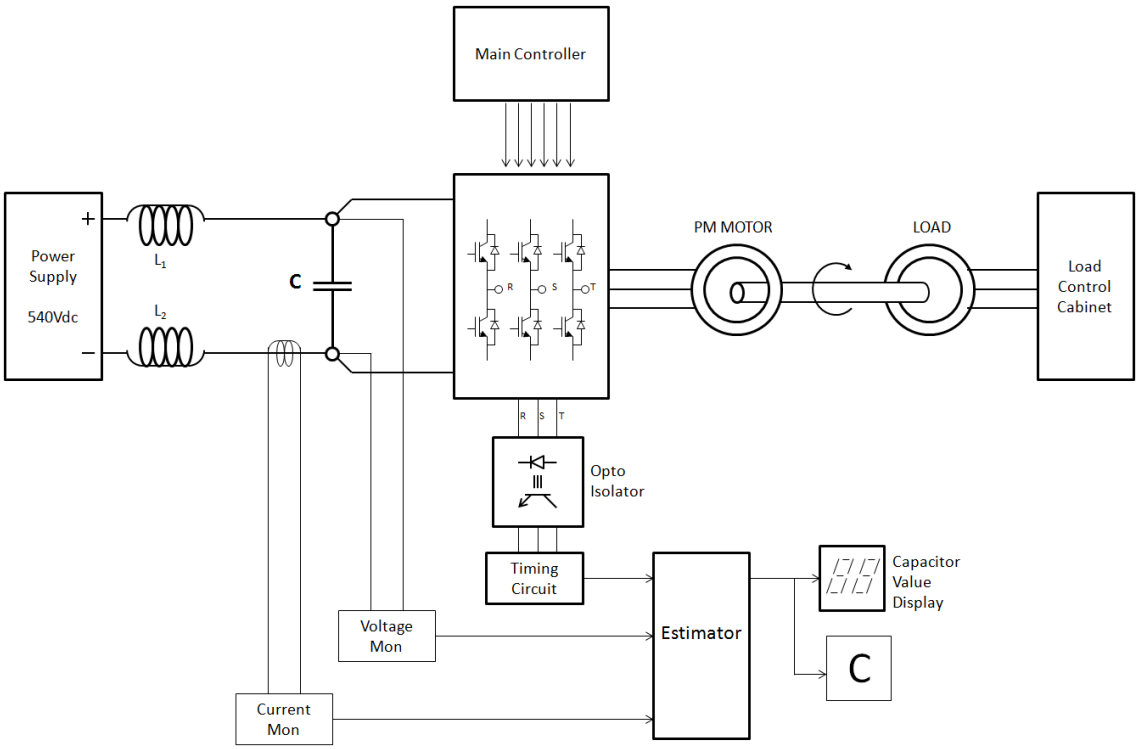


Figure 3.15 – Design overview

3.6 Designing the voltage monitor

The voltage monitor is required to measure the voltage ripple on a dc-link. This section will focus on the implications in doing so for the ELGEAR rig.

3.6.1 *Ripple voltage vs. PWM ratio*

From the assessment in the preceding sections, it is possible to derive the capacitor's ripple voltage with respect to the applied duty ratio. During every PWM cycle, the current flow in to the capacitor during the zero voltage state is equivalent to the average current consumption of the motor.

For example, referring to Figure 3.11, a 5% duty ratio implies that the capacitor will discharge for 5% of the time and charge for 95% of the time. The average current of i_β is equal to i_α: $i_\beta(5\%_{av}) = i_\alpha = 3A \times 0.05 = 0.15A$. During the 5% on-time, $i_\beta = 3A$ and hence the discharge of the capacitor is $i_\gamma = i_\alpha - i_\beta = 0.15A - 3A = -2.85A$.

Similarly, for a 95% duty ratio, the capacitor will discharge for 95% of the time with a discharge current of $i_\gamma = i_\alpha - i_\beta = (3A \times 0.95) - 3A = -0.15A$.

Table 3.3 shows how the ripple voltage varies versus the duty ratio. The maximum ripple voltage is observed at a duty ratio of 50%. The table also shows that a larger voltage ripple is observed when the capacitance drops.

Calculations for Table 3.3

$$i_\beta = 3A$$

$$i_\gamma\,(on\,state) = i_\alpha - i_\beta$$

$$i_\gamma\,(off\ state) = i_\alpha$$

$$dv_{charge} = \frac{i_\gamma\,(on\,state) \times t_{on}}{C}$$

$$dv_{discharge} = \frac{i_\gamma\,(off\ state) \times t_{off}}{C}$$

t_{on}	PWM	i_{α}	i_{γ} on-state	i_{γ} off-state	C = 80 µF		C = 60 µF	
[µs]	[%]	[A_{rms}]	[A]	[A]	dv discharge [mV]	dv charge [mV]	dv discharge [mV]	dv charge [mV]
0	0	0	-3.00	0.00	0.00	0.00	0.00	0.00
5	5	0.15	-2.85	0.15	-178.13	178.13	-237.50	237.50
10	10	0.30	-2.70	0.30	-337.50	337.50	-450.00	450.00
15	15	0.45	-2.55	0.45	-478.13	478.13	-637.50	637.50
20	20	0.60	-2.40	0.60	-600.00	600.00	-800.00	800.00
25	25	0.75	-2.25	0.75	-703.13	703.13	-937.50	937.50
30	30	0.90	-2.10	0.90	-787.50	787.50	-1050.00	1050.00
35	35	1.05	-1.95	1.05	-853.13	853.13	-1137.50	1137.50
40	40	1.20	-1.80	1.20	-900.00	900.00	-1200.00	1200.00
45	45	1.35	-1.65	1.35	-928.13	928.13	-1237.50	1237.50
50	50	1.50	-1.50	1.50	-937.50	937.50	-1250.00	1250.00
55	55	1.65	-1.35	1.65	-928.13	928.13	-1237.50	1237.50
60	60	1.80	-1.20	1.80	-900.00	900.00	-1200.00	1200.00
65	65	1.95	-1.05	1.95	-853.13	853.13	-1137.50	1137.50
70	70	2.10	-0.90	2.10	-787.50	787.50	-1050.00	1050.00
75	75	2.25	-0.75	2.25	-703.13	703.13	-937.50	937.50
80	80	2.40	-0.60	2.40	-600.00	600.00	-800.00	800.00
85	85	2.55	-0.45	2.55	-478.13	478.13	-637.50	637.50
90	90	2.70	-0.30	2.70	-337.50	337.50	-450.00	450.00
95	95	2.85	-0.15	2.85	-178.13	178.13	-237.50	237.50

Red graph

Blue graph

$\Delta V_{max} = \pm 20\%$

Table 3.3 – Discharge voltages of the capacitor depending on the PWM duty ratio. Highlighted columns indicate maximum ripple voltage.

Table 3.3 is graphed in Figure 3.16. From the graph it can be observed that the optimum duty ratio is 50%, which provides the highest amplitude for the ripple voltage.

The measurement needs to acquire voltage samples over a period of time *dt* – the longer the better. The compromise between the two competing variables is set at around 40%, i.e. the 40 µs range displayed in Figure 3.16. This gives the best combination where the largest amplitude and time sampling period is obtained.

This period was defined by allowing the ripple voltage amplitude to drop by 20% of its maximum amplitude. The ripple voltage has to be sampled by means of an ADC converter. The ADC converter has a defined accuracy of a couple of millivolts. The larger the ripple voltage, the more the signal to noise ratio is improved.

The sampling of the waveform in the estimator is further discussed in section 3.8.2 page 61.

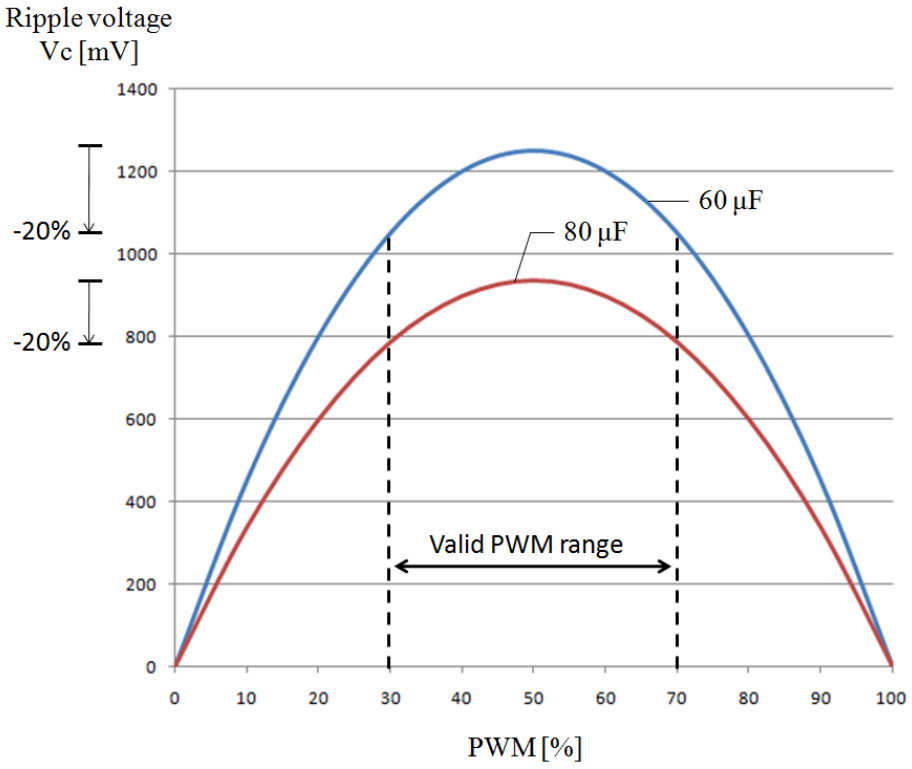


Figure 3.16 – Ripple voltage vs. PWM duty ratio

3.6.2 *Ripple voltage*

The ripple voltage simulation on the dc-link capacitor is shown in Figure 3.17. The ripple voltage consists of two frequencies superimposed. The high frequency 10 kHz

component arises from the PWM carrier signal. The peak to peak value is recorded between 0.5V and 1.2V, which is superimposed on the average dc value of approximately 540V. The peak-to-peak ripple as a percentage of the total voltage offset is between 0.1% and 0.2%.

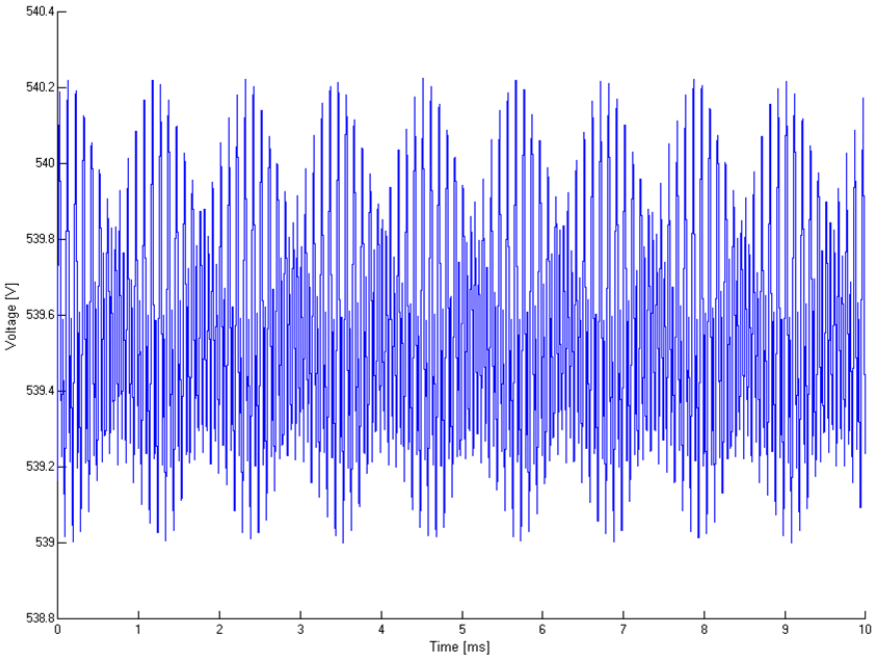


Figure 3.17 – Dc-link voltage

3.6.3 *Lower frequency dc-link voltage ripple component*

From Figure 3.17 a lower frequency envelope of 900 Hz is observed. The inverter switches at 10 kHz, which is modulated to produce a sinusoidal motor phase current between >0Hz to 150 Hz (see Figure 3.18). The frequency is proportional to the speed of the motor. The motor is a 10-pole machine with a rated speed of 900 rpm.

Referring to Figure 3.18, the PWM modulated voltage shown for one transistor produces one half of the sinusoidal motor phase current. The other half of the sinusoid is produced by the accompanying transistor of the same leg. As a result of the three phase 150 Hz sinusoids, a 900 Hz ripple is observed on the dc-link (i.e., 150 multiplied by 3 phases, multiplied by 2 for the rectification). The resultant ripple is therefore a combination of 10 kHz, enclosed in an envelope of 900 Hz when operating at rated speed.

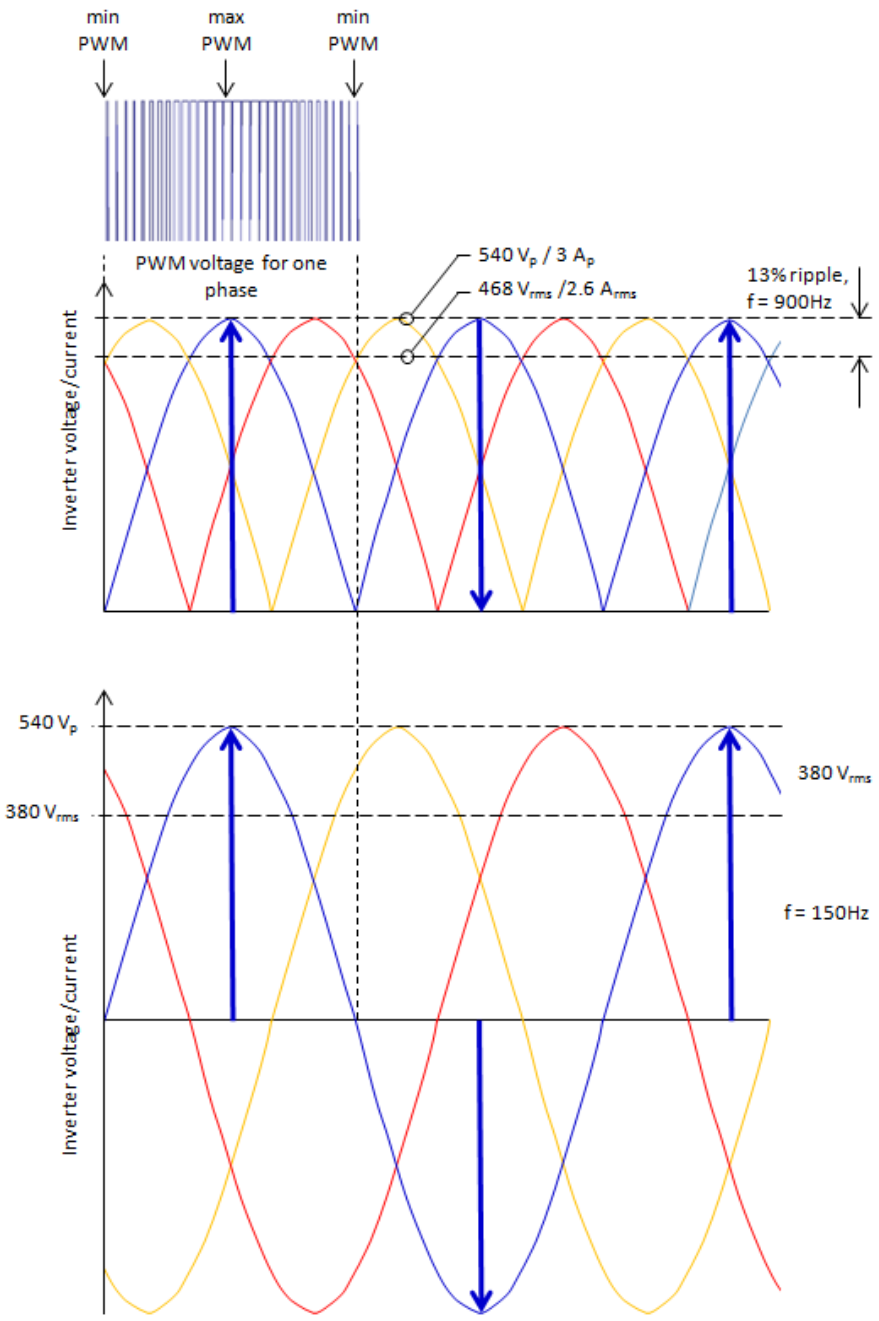


Figure 3.18 – Reconstruction of the ripple on the dc-link capacitor

The 900 Hz is not expected to significantly influence the result as long as the samples are averaged out over a longer time period than the wavelength (approximately 1/900 ≈ 1 ms). Since the low frequency ripple is alternating, the error will average-out over many samples for the ripple voltage. The 900 Hz should not pose any problems for the current monitor since its low-pass cut off frequency is set to 10 kHz.

3.6.4 *Cut off frequency*

The cut off frequency is an important factor in the voltage monitor. The voltage monitor should pass the charge/discharge cycle of the capacitor on to the estimator accurately.

The charge discharge cycle is shown in Figure 3.19 together with various cut off frequencies.

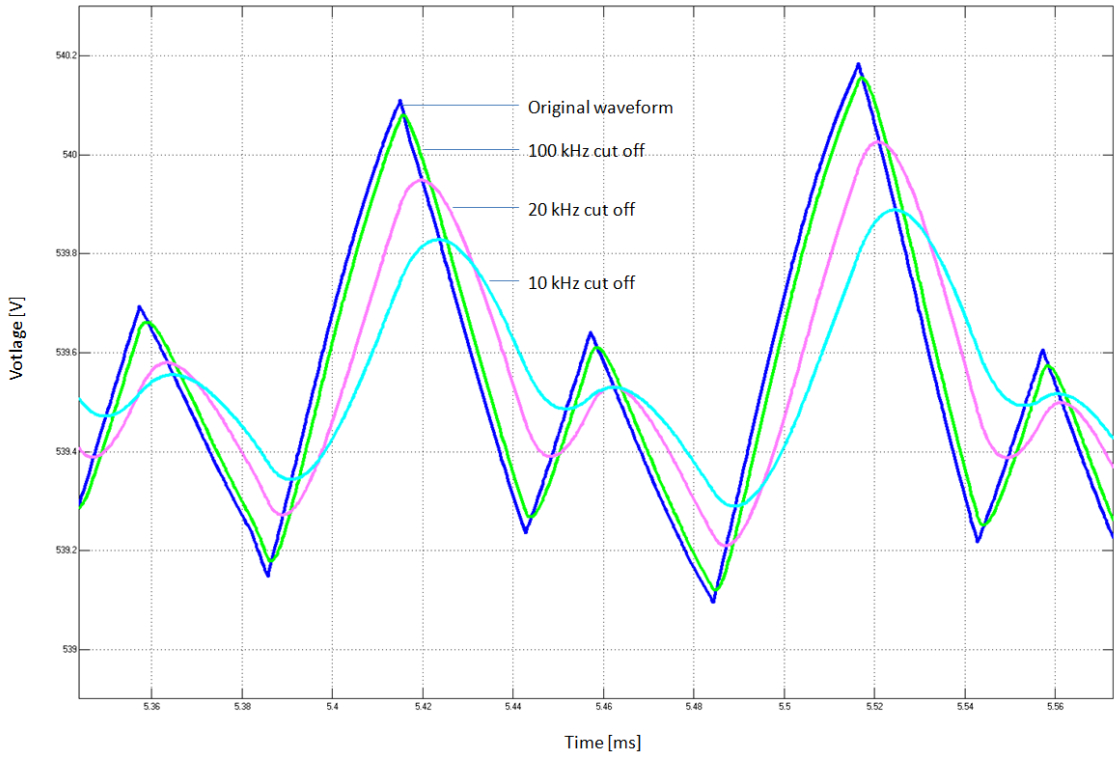


Figure 3.19 – Comparison of different cut off frequencies for the voltage monitor

The capacitor voltage waveform is triangular. This means – by Fourier analysis – that the waveform is composed of many harmonics. By introducing a low cut off frequency, the harmonics are significantly suppressed resulting in the rounding of the triangular peaks, as well as introducing a significant phase delay. This means that the delta voltage measured will be inaccurate. Moreover, since the condition monitoring technique samples all values at once, the phase delay may also introduce inaccuracies. In order to obtain an accurate enough sampling device, it was determined to have a cut off frequency of 100 kHz, to reproduce the original waveform accurately without significant phase delays.

3.6.5 *Voltage monitoring hardware for ELGEAR*

The voltage monitoring unit effectively removes the average dc bus voltage by means of a high pass filter. It then amplifies the ripple voltage by a factor of two and adds a dc offset of 2.5 V to allow a compatible interface with the ADC of the estimation processor (operating range 0 ... 5V).

For example, a duty ratio of 50% on a capacitor of 60 µF provides an output ripple of 2.66 V peak to peak at an offset of 2.5 V. The ac amplification factor is therefore 2.125 (i.e. $V_{monitor} = 2.125\,V_c$).

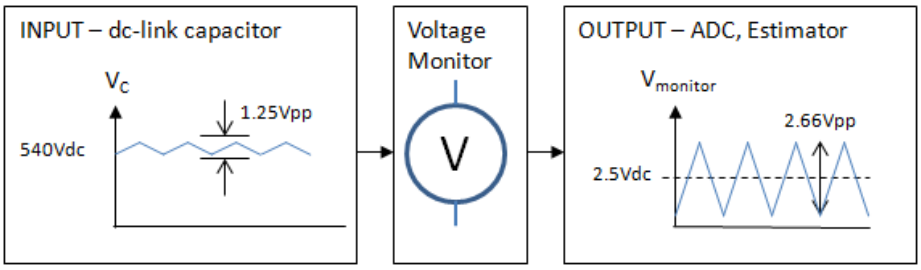


Figure 3.20 – Voltage monitoring adaptation, 60 µF capacitor example

The voltage monitoring circuit diagram is given in Figure 3.21 below, with the list of components in Table 3.5. The voltage monitoring circuit has an electrical safety isolation which isolates the primary high voltage from the secondary low voltage circuit. The circuit provides a high signal linearity over a wide bandwidth to allow precise analysis of the signal slopes and amplitudes.

The specification of the voltage monitoring circuit is summarised in Table 3.4.

Input dc voltage	±270 V, centre grounded*
Input ac ripple amplitude	2.5 V_{pp} for 60 µF
Ripple shape	Triangular
Ripple frequency	10….20 kHz
Output ripple	max 5 V_{pp} (compatible with estimator, ADC)
Output voltage offset	+ 2.5 V_{dc} (compatible with estimator, ADC)
Amplifier pass band (-3dB)	500 Hz … 100 kHz
Voltage amplification factor	2
Secondary power supply	+28 V
PIC ADC impedance	>1 MΩ

* for the laboratory test set up, a +540 V supply was used

Table 3.4 – Specification of the voltage monitoring circuit

The design of the monitoring circuit is based on the integrated high voltage signal isolation amplifier AD215. The AD215 was chosen for its high cut off frequency (3dB at 120 kHz). The AD215 converts the input signal to a digital signal which is transmitted through an isolation transformer. The signal is then converted back in to an analogue signal using a low pass filter.

The input circuit (C1 and R1) acts as a high pass filter, where the ac ripple voltage is coupled whilst the dc components are blocked. The capacitor C1 is therefore rated for high voltages.

The input of the AD215 provides a pre-amplifier stage. The pre-amplifier is used in non-inverting mode (R3 = R4). Resistor R3 has a capacitor C4 in parallel as recommended by the datasheet for stability reasons. The clipping diodes (D1 – D4) protect the pre-amplifier circuit, where the resistance of R2 limits the diode's maximum forward current. The zero bias of the amplifier is realised by resistors R1 and R2. Adequate rating for resistors is necessary since they have a high voltage protection function, especially when absorbing the surge current during switch on/off.

The output stage of the AD215 consists of a unity gain buffer amplifier. The amplifier provides a zero offset dc adjustment of ±35 mV. To comply with the ADC of the estimator, a dc level shift of +2.5 V is implemented by a high impedance voltage divider R6 and R7. The capacitor resistor combination of C7 and R5 couples the output ripple signal to the level shift. R5 is in place to protect the amplifier from overload as well as to limit the current for the protection diodes D5 and D6.

The AD215 requires a symmetric ±15 V power supply. The double output dc/dc converter is used to supply this power, which is fed from the +28 V signal power supply, compatible to aerospace. Capacitors C5, C6 and C2, C3 are recommended according to the datasheet. For the +5 V output stage (interfacing with the estimator), a D7 Zener diode stabiliser is used in combination with a filtering capacitor (C8).

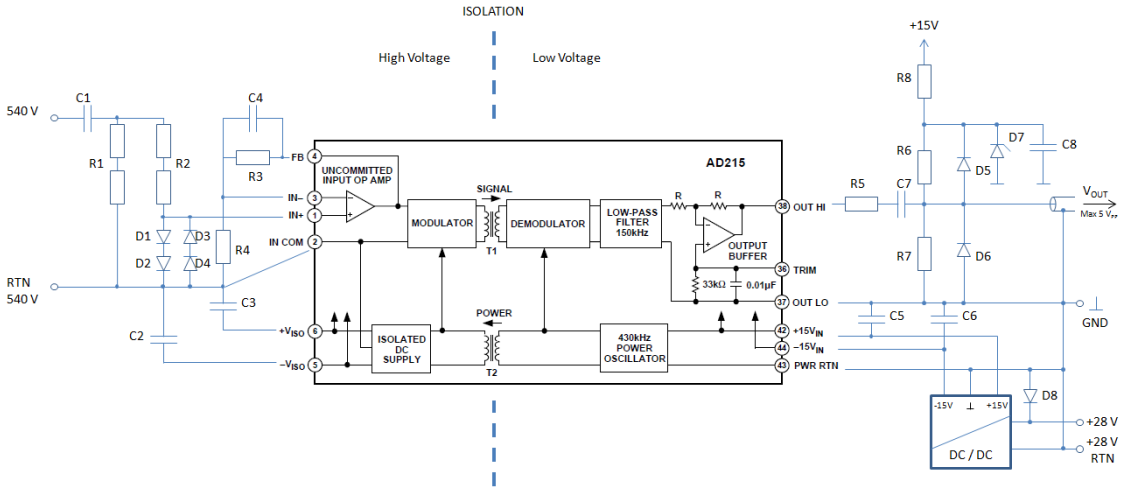


Figure 3.21 – Voltage monitoring circuit diagram

	Value	Unit
Resistors		
R1	2 × 56k	Ω
R2	2 × 12k	Ω
R3	6k49 (0.1%)	Ω
R4	6k49 (0.1%)	Ω
R5	1k0	Ω
R6	1M0	Ω
R7	1M0	Ω
R8	3k9	Ω
Capacitors		
C1	3.0 (1kV)	nF
C2	22	µF
C3	2.2	µF
C4	68	pF
C5	2.2	µF
C6	2.2	µF
C7	470	nF
C8	100	nF
Diodes		
D1	BAY 21	
D2	BAY 21	
D3	BAY 21	
D4	BAY 21	
D5	BAY 21	
D6	BAY 21	
D7	Zener (5.1 V)	
D8	1N4004	

Table 3.5 – List of components, voltage monitor

3.7 Designing the current monitor

The current monitor is a current transducer that provides an output voltage proportional to the current that flows through its primary path. The sensor's amplification factor is 1.575 V/A (i.e. $V_{currentmonitor} = 1.575 I_1$), allowing a maximum input current of 3 A to interface with the ADC of the estimation processor. The bandwidth of the current sensor ranges from dc to 10 kHz. The upper frequency limit – unlike the voltage monitor – is

not too important since the current is expected to be of low frequency due to the input inductors.

The circuit diagram of the current monitor is found in Figure 3.22, with the list of components in Table 3.7. The purpose of the current monitor is to measure the incoming dc-link current. There is a high voltage isolation separating the primary from the secondary side. The output dc voltage is proportional to the current sensed on the primary input, and is compatible with the ADC of the estimator. The bandwidth of the current sensor includes dc, with the upper frequency limit set at 10 kHz. The upper frequency limit – unlike the voltage monitor – is not too important since the current is expected to be of low frequency due to the influences of the input inductors.

The specification of the current monitor is outlined in Table 3.6 below:

Input dc line voltage	±270 V, centre grounded*
Input dc current	0 … 3 A
Out/in relation	1.6 V/A
Output voltage offset	0 V_{dc} for 0 A_{dc}
Amplifier bandwidth (-3dB)	0 … 10 kHz
Secondary power supply	+28V
PIC ADC impedance	>1 MΩ

* for the laboratory test set up, a +540 V supply was used

Table 3.6 – Current monitor specification

The current monitoring circuit uses a commercial current transducer based on the Hall effect principle. The current transducer output provides a voltage proportional to the current it measures (125 mV per amp). The output voltage is offset by 2.5 V to be able to accommodate negative currents as well. For example, when a current of -3 A is measured, its output will be $2.5 - (3 \times 0.125) = 2.125\ V$. Since the device only requires positive current, there is no need for an offset voltage.

The first amplifier CA3130 eliminates the offset voltage of 2.5 V. This has to be done very precisely to ensure the 125 mV per amp is not affected. The amplifier uses a reference of 2.5 V using resistors R2 and R3. Since the offset voltage of the transducer is not exactly 2.500 V, the amplifier can be manually adjusted using the variable resistor R10 to precisely tune the amplifier to the offset voltage. However, when the LTSR transducer is used, this process is not necessary, as the transducer provides an exact reference output signal, which can be connected directly to the operational amplifier.

The CA 3130 has a unity gain, so the output signal is directly proportional to the input current with an offset of zero volts.

The second operational amplifier, LT 1006, amplifies the 125 mV per amp to 1.6 V per amp, and its output interfaces with the ADC of the estimator. The amplifiers and transducer are powered by 5 V which is tapped from the +28 V supply.

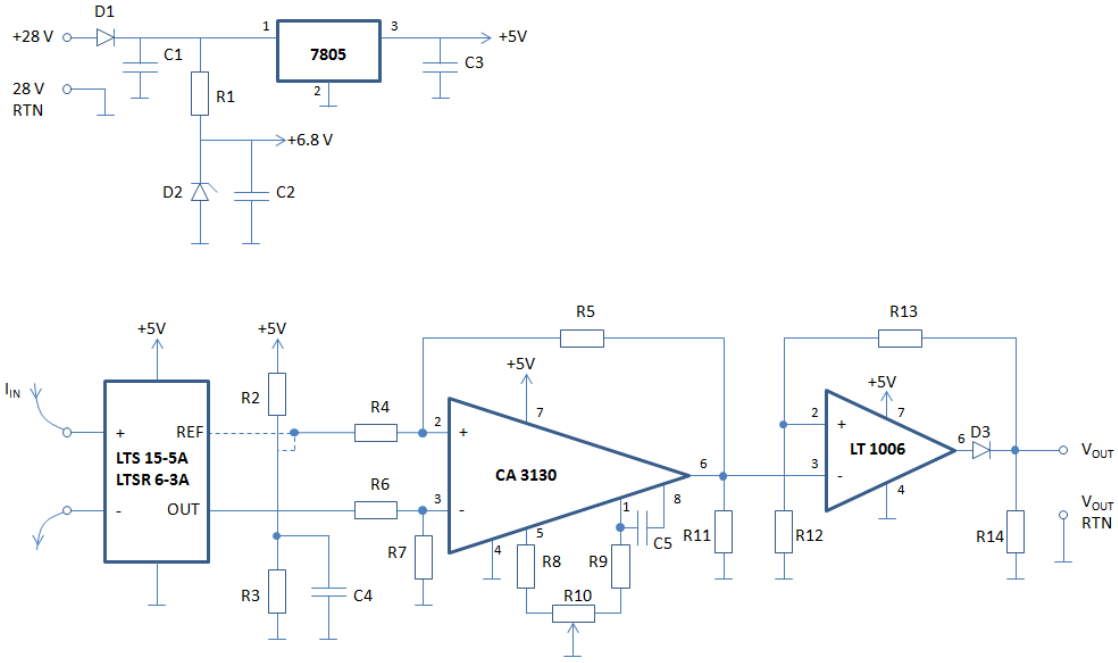


Figure 3.22 – Current monitor circuit diagram

	Value	Unit
Resistor		
R1	2k2 (½W)	Ω
R2 (only with LTS transducer)	4k7	Ω
R3 (only with LTS transducer)	4k7	Ω
R4	343k	Ω
R5	343k	Ω
R6	343k	Ω
R7	343k	Ω
R8	82.5k	Ω
R9	17k4	Ω
R10	10k	Ω
R11	300	Ω
R12		
R13		
R14	1k0	Ω
Capacitor		
C1	2µ2	F
C2	220n	F
C3	220n	F
C4	220n	F
C5	56p	F
Diodes		
D1	1N4001	
D2	Zener (6.8 V)	
D3	BAT 41	

Table 3.7 – List of components, current monitor

3.8 Timing

3.8.1 *IGBT opto-isolator*

As discussed earlier, it is best to monitor during the PWM zero voltage states. Information of when a zero voltage state occurs can be derived by observing the switching states of the IGBT legs. Three IGBT signals are required to derive the zero voltage states (i.e. T_1, T_3, T_5). The signals are isolated using an opto-coupler. It is important to have the analogue signal ground point at the estimator. An isolator is

therefore required between the main controller ground and the estimator ground. The opto-coupler interface diagram is depicted in Figure 3.23.

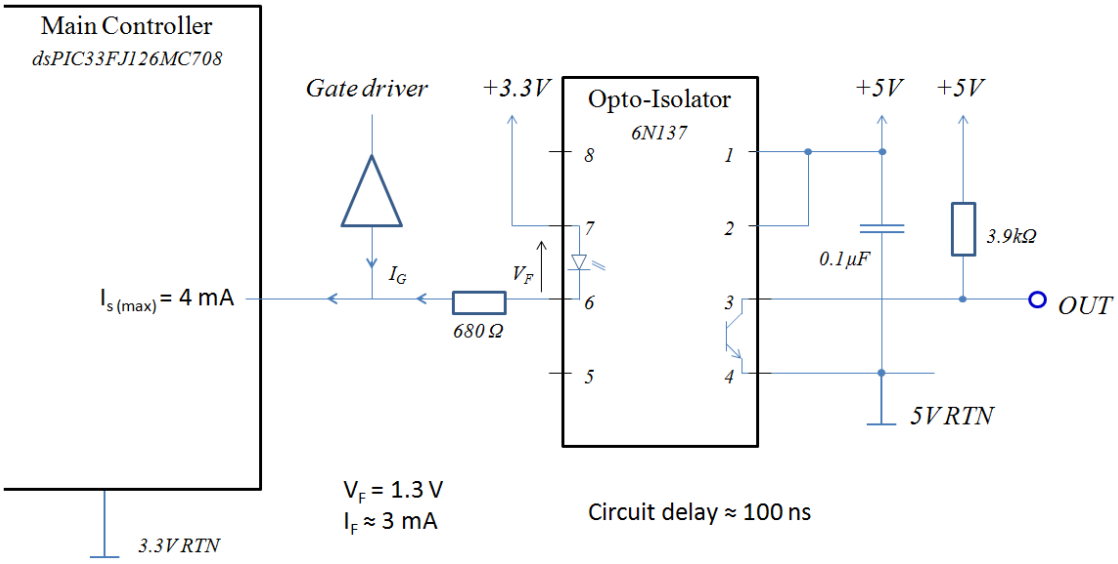


Figure 3.23 – Opto-isolator circuit for one IGBT signal

3.8.2 *Timing circuit design*

The three phase state inputs are decoded to derive the valid zero voltage state. When this condition occurs, the timing circuit is triggered by means of multiple pulses from the pulse generator. These pulses are separated using precision timing. The window generator ensures that the pulses take place during a valid time frame, which can vary depending on the duty ratio. Both the window and the pulse generator are driven by a precision oscillator to ensure accurate timing. The valid sampling signals are then fed in to the estimator where the actual samples and calculations take place. When the timing window is too small for valid sampling, an invalid signal is passed on which results on the sample being discarded.

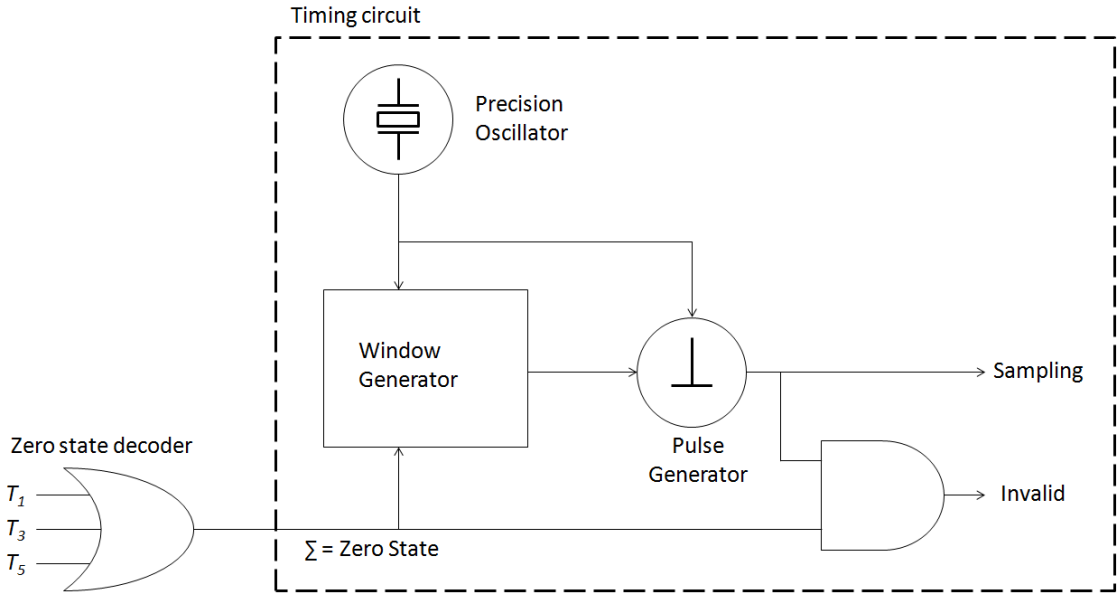


Figure 3.24 – Timing circuit

3.8.3 *Timing accuracy*

Errors during measurements in each of the variables will contribute towards the overall accuracy calculation of C. For the condition monitoring system, the aim is to reach a minimum targeted accuracy of 1%. Although the system should only detect a single open circuited capacitor (out of 4), a much higher accuracy target is given to ensure high accuracy of the system. In the whole scheme of things, there are many other variables that influence the accuracy (e.g. imperfect conductors, switching noise, electromagnetic interference etc.).

For a targeted accuracy of 1%, all of the variables (*dv*, *dt*, and I_c) require a higher measurement accuracy. This would especially be difficult for *dv*, as a relatively small voltage ripple has to be measured on top of a high dc-link voltage. Nevertheless, the timing of accuracy of *dt* can be easily achieved with high precision in the timing circuit. This way, the timing accuracy will allow the other two variables to be less accurate, whilst still achieving a 1% target.

A 10 kHz PWM cycle has a time period of 100 µs during which, the capacitor charges and discharges. In section 3.6.1, it was observed that a window with a time span of 40 µs was the optimum range for sampling (depicted in Figure 3.25, page 63). For the timing error to become insignificant it is estimated that an accuracy of ±20 ns should be envisaged (i.e. 0.1% tolerance).

Even though the estimator is quick at sampling (10-bit sampling @ 2M samples per second), it is doubtful whether the software programmed gating can achieve the target

accuracy. In fact, the absolute time span is not too important as long as the time between the samples taken is precise. A special dedicated timing circuit is designed based on high speed gates. Whilst the hardware implementation of logic gates focuses on the timing part, all other functions are left to the estimator.

3.8.4 *Valid sampling example*

Figure 3.25 shows a charge/discharge cycle for a capacitor of 80 µF at 10 kHz, for different duty ratios. Take for example the blue curve with a duty ratio of 30%. During the first 30 µs the capacitor discharges, with a difference in voltage of ~750 mV. The remaining 70 µs, the capacitor charges again (as discussed in section 3.6.1).

Both the early (30% duty ratio) and late (58% duty ratio) sample show a valid sampling frame. When the capacitor starts charging as a result of the zero voltage state, a guard time of 5 µs is introduced to avoid sampling on the apexes of the waveform. The waveforms are generally noisy near the apex due to the switching and ringing of the IGBTs. After the guard time, multiple samples will be taken for a minimum duration of 35 µs. The more samples, the more accurate the calculation will be, and hence a lower duty ratio is better, provided a sufficient amplitude is maintained.

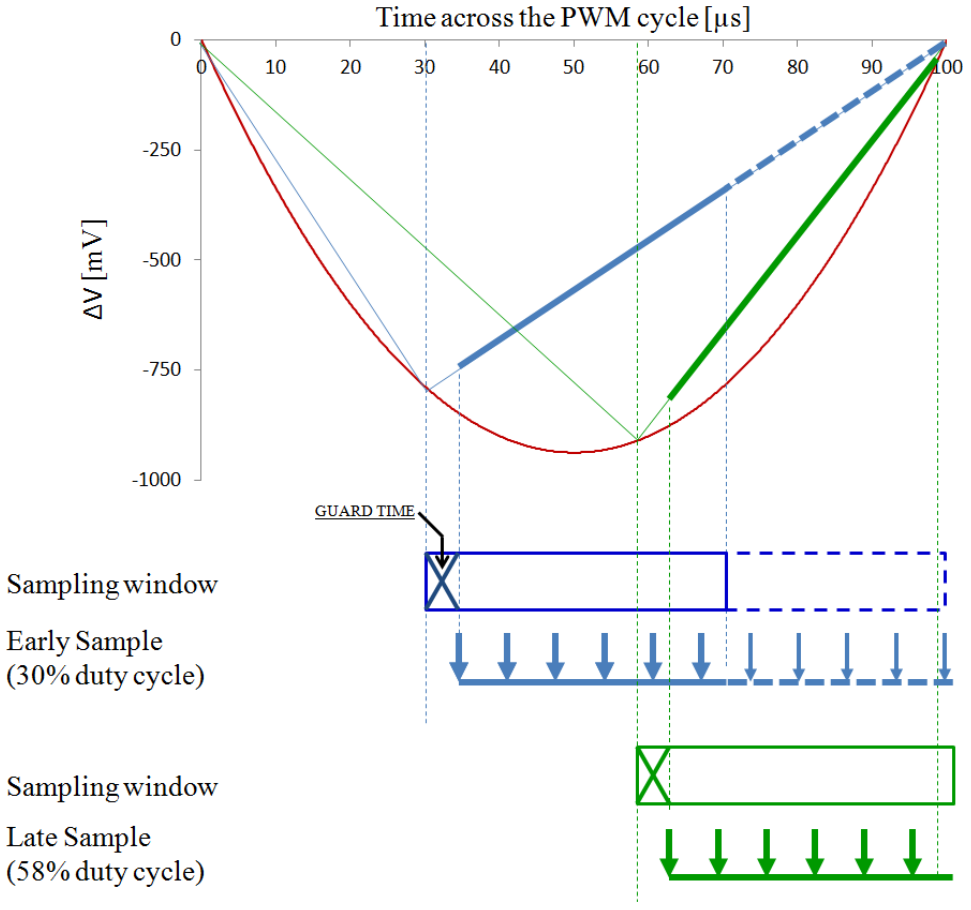


Figure 3.25 – Timing circuit diagram, valid samples

3.8.5 *Invalid sampling example*

When the duty ratio is too low (e.g. 10%), a lot of samples can take place, but the amplitude (*dv*) will be very low. The inaccuracy of sampling increases again since the signal to noise ratio at the ADC worsens. For high duty ratio (e.g. 80%), not enough samples can be taken within the valid window frame. This reduces the accuracy again, and an invalid signal is sent to the estimator. Invalid samples can be observed in Figure 3.26.

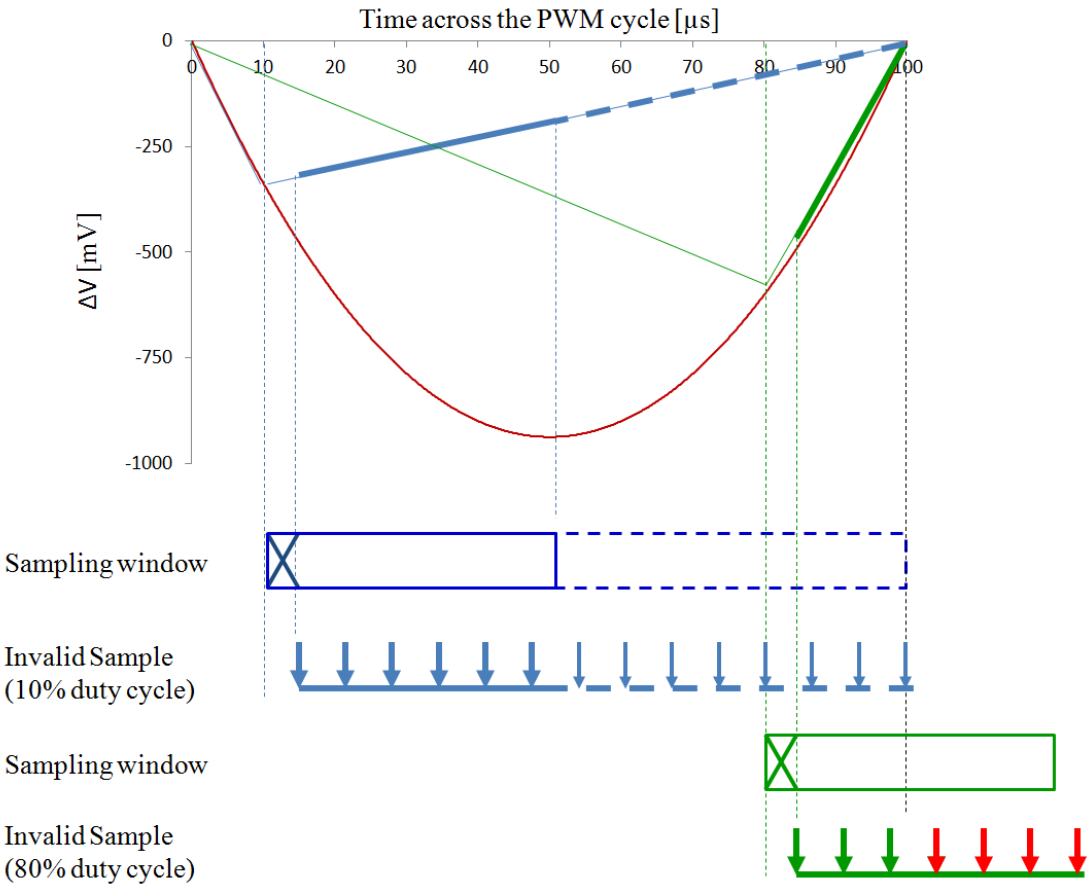


Figure 3.26 – Timing circuit diagram, invalid samples

3.9 Estimator

The estimator receives the inputs values for voltage (*dv*) and current ($\int I$) from the voltage and current monitors respectively. The timing circuit provides the valid sampling pulses (*dt*) as well as the invalid signal when the sample should be discarded.

The dsPIC used for the estimation processor is the dsPIC30F2020 by Microchip and is powered by a 5 V supply. The estimator has the following input characteristics:

- An ADC resolution of 10 bits (4.88 mV per bit).
- A sample rate of 2 M samples per second.

- Ability to sample two ports simultaneously (sampling the current and voltage at the same time).

The estimator output characteristics include:

- A PWM output port that can be converted in to an analogue output by means of adding a low pass filter. This port can be connected to the oscilloscope where the range 0 – 5 V is analogous to a capacitance of 0 – 100 µF.
- A 4-bit parallel output to interface a double seven segment display. This indicates the numeric value in capacitance (range 0 – 99 µF).
- An error LED lights up when more than 10 consecutive samples are rejected. This could be for the reasons stated in the sections above (e.g. out of range duty ratio, too low current, too low amplitude etc.)

3.10 Temperature dependence

The condition monitoring design outlined has a defined accuracy depending on the temperature. This section shows an analytical technique of determining the approximate accuracy of the voltage and current monitors as a result to temperature changes. The analysis is based on the datasheets of the components.

3.10.1 *Voltage monitor*

In the voltage monitor, there are two components that are most sensitive to temperature. This is the AD215 operational amplifier and the R4, R5 resistors that define the amplifier's gain. By analysing the datasheet of both components, an approximate accuracy can be determined for the voltage monitoring temperature coefficient.

For the R4 and R5 resistors, have a temperature coefficient of 25 ppm/K. This means that a 1 MΩ resistor will vary by 25 Ω per Kelvin. This relatively low temperature coefficient is due to precision resistors being selected. These resistors set the gain of the amplifier to 2.125. The output voltage range of the voltage monitor is 5 V. The voltage variation per degree due to the resistors is therefore:

$$2.5\times10^{-5}\times2.125\times5=0.27\,{}^{mV}\!/_{K}$$

The AD215 is specified for 30 ppm/K (part per million, per Kelvin). The variation of amplitude gain is:

$$3\times10^{-5}\times2.125\times5=0.32\,{}^{mV}/_{K}$$

3.10.2 *Current monitor*

Of all the components in the current monitor, the highest temperature coefficient by far is the transducer, with a coefficient of 200 ppm/K. The transducer has a total amplification of 12.6. (i.e. $\frac{1.575}{0.125}$). The variation of amplitude gain as a result of the current transducer is:

$$200\times10^{-6}\times12.6\times5=12.6\,{}^{mV}/_{K}$$

Other components that influence the gain are listed in the table below:

Component	Variation of voltage per degree [mV/K]
Current transducer LTS15-5	12.6
Precision resistor combination R12, R13	0.315
Operational amplifier CA3130	0.126
Operational amplifier LT1006	0.016

Table 3.8 – Components in the current monitor varying most with temperature

3.10.3 *Overall temperature variation*

All equipment was calibrated at room temperature, 20°C. For a variation of ±2°C, the voltage variation per degree is not too important for both monitoring circuits. For extremer conditions, the current transducer in the current monitor may require a separate casing where a more constant temperature is maintained. The work in this thesis is aimed to provide a concept monitoring technique, and therefore only operates under laboratory conditions. Further investigation of the circuit accuracy with respect to temperature is not carried out.

3.11 Conclusions

3.11.1 *Comparison with the literature*

The estimation technique proposed poses a number of advantages compared to existing capacitor monitoring systems in the literature:

- The monitoring system is an integrated system, thus not requiring the physical removal of the capacitor to perform tests.
- It is able to run passively in the background without interfering with the main control system.
- The proposed system is a continuous online monitoring system. Data can be recorded for long periods of time allowing the possibility to observe a gradual drop in capacitance over its lifetime.

3.11.2 *Proposed monitoring design*

The proposed condition monitor relies on existing sensors which are provided in the drive for safety and control reasons. Although some modifications are required on the voltage and current sensors, no major additional components are necessary on the actual drive. For the monitoring system to work effectively, the input filters must be upgraded. The minimum amount of differential inductance specified by DO-160F is insufficient to be able to measure the voltage ripple on the dc-link capacitors accurately.

Zero voltage state monitoring was proposed to be an effective method of calculating the capacitance compared to other states. Firstly, the complexity of monitoring is simplified since measurements from the motor phase current transducers will not be necessary. Secondly, the zero voltage state occurs at a relatively high frequency. Furthermore it was proposed that the optimum duty ratio for sampling was between 30 % and 70 %. This will provide optimum voltage amplitude, effectively increasing the signal to noise ratio.

The condition monitoring technique consisting of the voltage monitor, current monitor, timing and estimator were defined for the ELGEAR in this chapter. In the following chapters the condition monitoring technique will be implemented on a low voltage and high voltage test rig.

Low Voltage Experimentation

Chapter 4

4.1 Introduction

The low voltage experiment (30 V) is an intermediate step to verify instrumentation, interfaces and software before applying the monitoring system on the high voltage rig (540 V). The main advantage of such a step is to test the monitoring system in an environment without having to deal with the complications of high voltage (safety and EMI). Thus the monitoring system can be tested on its performance and the data processing software can be adjusted and debugged in real time, without having to switch off the system due to safety constraints. Furthermore, a low voltage test can be used to accurately calibrate the instrumentation.

4.2 Principle of operation

The low voltage experiment is essentially simulating a PWM charge/discharge ripple on a capacitor. It is constructed to operate in a similar manner to the high voltage rig and includes the following features:

- A charge/discharge PWM cycle at a frequency of 10 kHz.
- Adjustable PWM load currents from 0 to 4 A.
- The possibility of varying the PWM duty ratio from 0% to 90%. This would cover the preferred 30% - 70% duty ratio, as well as including states with a (very) low sampling time.
- A toggle switch to select a 60 µF or 70 µF dc-link capacitor.
- A representative dc-link power bus input filter (i.e. including differential mode inductors).
- A timing signal output that indicates when sampling should take place.

The block diagram of the low voltage set up can be found in Figure 4.1. A picture of the low voltage experimental unit is shown in Figure 4.2.

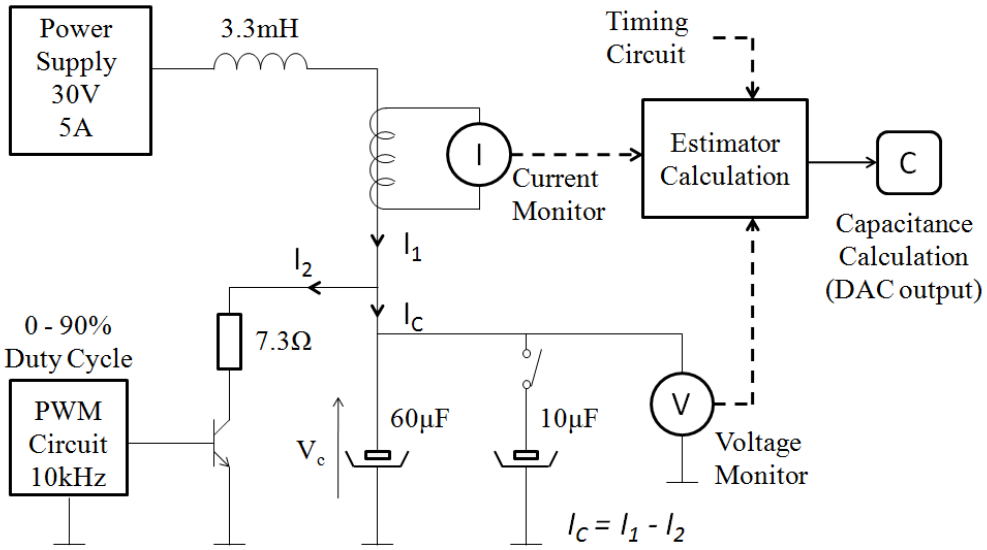
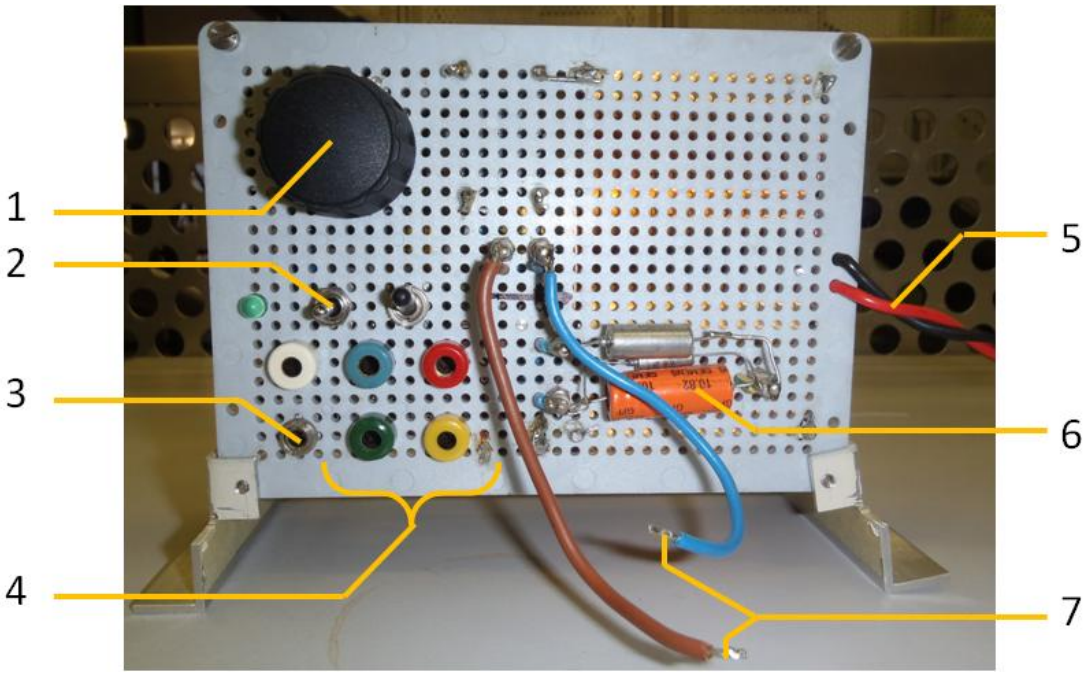


Figure 4.1 – Low voltage test circuit



1 – Duty cycle control (0%-90%)

2 – Switch in/out additional 10 µF capacitance

3 – Connection to timing circuit

4 – Connections to voltage monitor & test points

5 – Low voltage supply input (28V)

6 – Selectable 60 µF or 70 µF capacitance

7 – Current loop to interface the current monitor

Figure 4.2 – Low voltage experimental unit

The circuit operates by pulsing a 7.3 Ω, 75 W load using the 10 kHz PWM, where the pulse width can be manually adjusted between 0% and 90% duty ratio. It is assumed

that current I_1 is relatively constant, due to the 3.3 mH coil. Furthermore, there is a timing signal that is synchronised with the PWM controlling transistor. The timing signal output notifies the estimator of a zero voltage state and the system is able to sample and perform calculations during this state.

During the off-time of the PWM, the input current I_1 will directly charge the capacitor(s) and hence, $I_1 = I_c$. During the active PWM on-time, the capacitor load current I_2 is discharged through R. The current I_1 flows through the PWM transistor, thus preventing the capacitor from being charged.

For this experiment to work – using only one current monitor and one voltage monitor – monitoring must only take place during the charge cycle of the PWM. This would be analogous to monitoring during the zero voltage state since the input current will directly charge the capacitor. The output measurement signals of the voltage and current monitors are connected to the estimator ADC input where sampling and subsequent processing takes place.

4.3 Low voltage vs. the high voltage rig

Due to the limited resources available at the time of construction, there are a number of differences between the low voltage experiment and the high voltage test rig:

- The load is resistive and not inductive. This causes the waveform to have some exponential charge/discharge characteristics instead of obtaining a pure triangular waveform. Nevertheless, the waveform is deemed close enough to the triangular waveform for testing purposes.
- The monitored capacitor is of electrolytic and not polypropylene technology. This will contribute to issues including a high ESR resulting in i^2r heating.
- Another side effect of electrolytic technology is the slow reaction time of the capacitor due to polarization. The waveform shows this effect as a sharp transition in the order of a microsecond just after switching occurs, followed by a small reverse recovery.

Nevertheless, these shortcomings represent a worst case scenario, and consequently in a less accurate capacitance reading. It is assumed that the low voltage experiment is sufficient to validate the estimation technique and calibrate instrumentation.

4.4 Low voltage result

The set up of the low voltage experiment is as described in Figure 4.1 where the discharge current is set to 3 A and the PWM duty ratio to 50%. During this test, a constant capacitance is selected of 70 µF. The oscilloscope in Figure 4.3 shows the voltage ripple (trace 1), current waveform (trace 2) and timing trace (trace 4). The resulting capacitance calculation from the estimator is displayed in trace 3.

Trace 1 (blue) shows the charge and discharge cycle of the capacitor. Some of the features mentioned in section 4.3 are observed. A slightly exponential charge/discharge waveform can be seen, as well as a sharp rise/drop after the apexes of the waveform. The voltage monitor has a built-in amplification factor calibrated at 2.125 to optimize the ADC range of the estimator. In this waveform, a peak-to-peak voltage of 3 V is measured. The actual ripple voltage on the capacitor is therefore 1.412 V peak-to-peak:

$$V_{monitor} = 2.125 \times V_C \tag{4.1}$$

$$V_C = \frac{V_{monitor}}{2.125} = \frac{3}{2.125} = 1.412V$$

Trace 2 (turquoise) shows a voltage trace representing the current at I_1. A small amount of noise is observed, especially around the switching states. The calibrated conversion from the output voltage of the current sensor is a factor of 1.575 V/A. During the off-period of the PWM (i.e., rising voltage slope), the capacitor is charged with a current of 1.651 A, which is measured as 2.6 V on the trace.

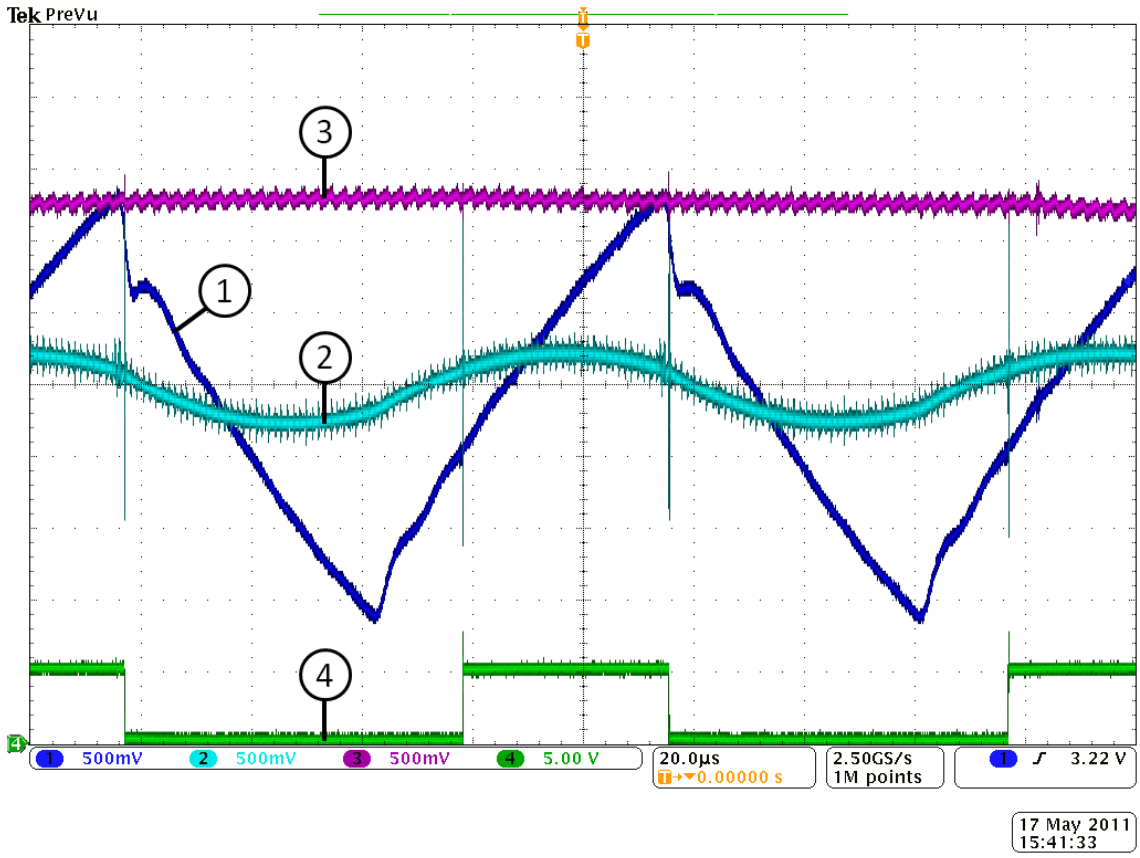
$$V_{current\,monitor} = 1.575 \times I_1 \tag{4.2}$$

$$I_1 = \frac{V_{current\,monitor}}{1.575} = \frac{2.6}{1.575} = 1.651A$$

Trace 3 (purple) shows the calculated capacitance output from the estimator. The scale is 20 µF per volt. The trace is hovering at around 3.7 V which is roughly 74 µF. A small ripple can be observed on the waveform due to the high frequency DAC output on the estimator.

Trace 4 (green) shows the timing signal. The signal provides an indication to the estimator when sampling should take place. A positive signal level indicates that the capacitor is charging ($I_1 = I_c$, analogous to the zero voltage state). The timing circuit

includes a ‘guard time’ delay, to avoid the ADC sampling during the PWM carrier waveform apex where a lot of noise is present. The reason for the guard time is mentioned in section 3.8.4, page 63.



Horizontal Scale

Time, 20 µs / div

Vertical Scale

Trace 1 – Voltage monitor, 500 mV / div ($V_{monitor} = 2.125V_c$)

Trace 2 – Current monitor, 500 mV / div ($V_{currentmonitor} = 1.575I_1$)

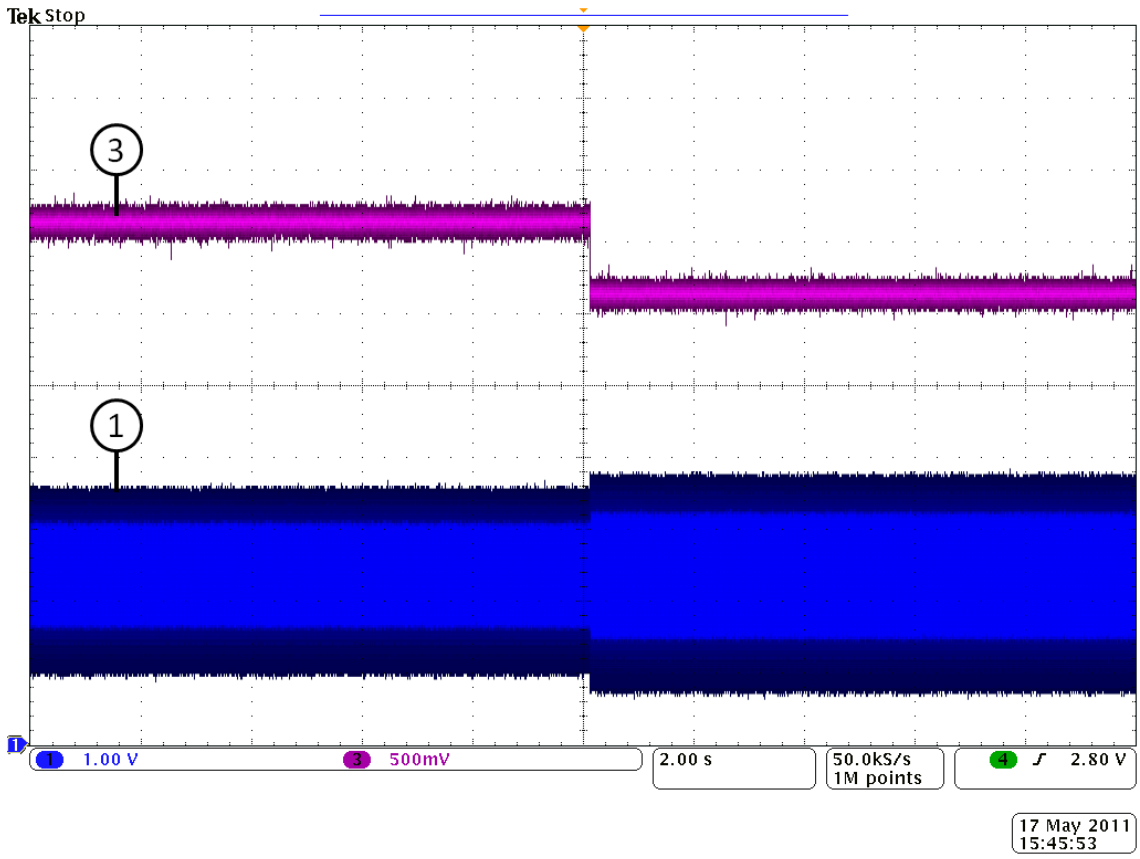
Trace 3 – Capacitance calculation DAC output, 500 mV / div (10 µF / div)

Trace 4 – Timing signal, 5V / div

Figure 4.3 – Low voltage test result, ~50% duty ratio

4.5 Capacitor switch out

Using the previous settings (duty ratio of 50%, current 3 A), a 10 µF capacitor is switched out after a period of time. This action is performed manually by toggling the switch shown in Figure 4.2, page 69 (label 2). The monitoring results can be found in Figure 4.4 below.



Horizontal Scale

Time, 2 s / div

Vertical Scale

Trace 1 – Voltage monitor, 1 V / div ($V_{monitor} = 2.125V_c$)

Trace 3 – Capacitance calculation DAC output, 500 mV / div (10 µF / div)

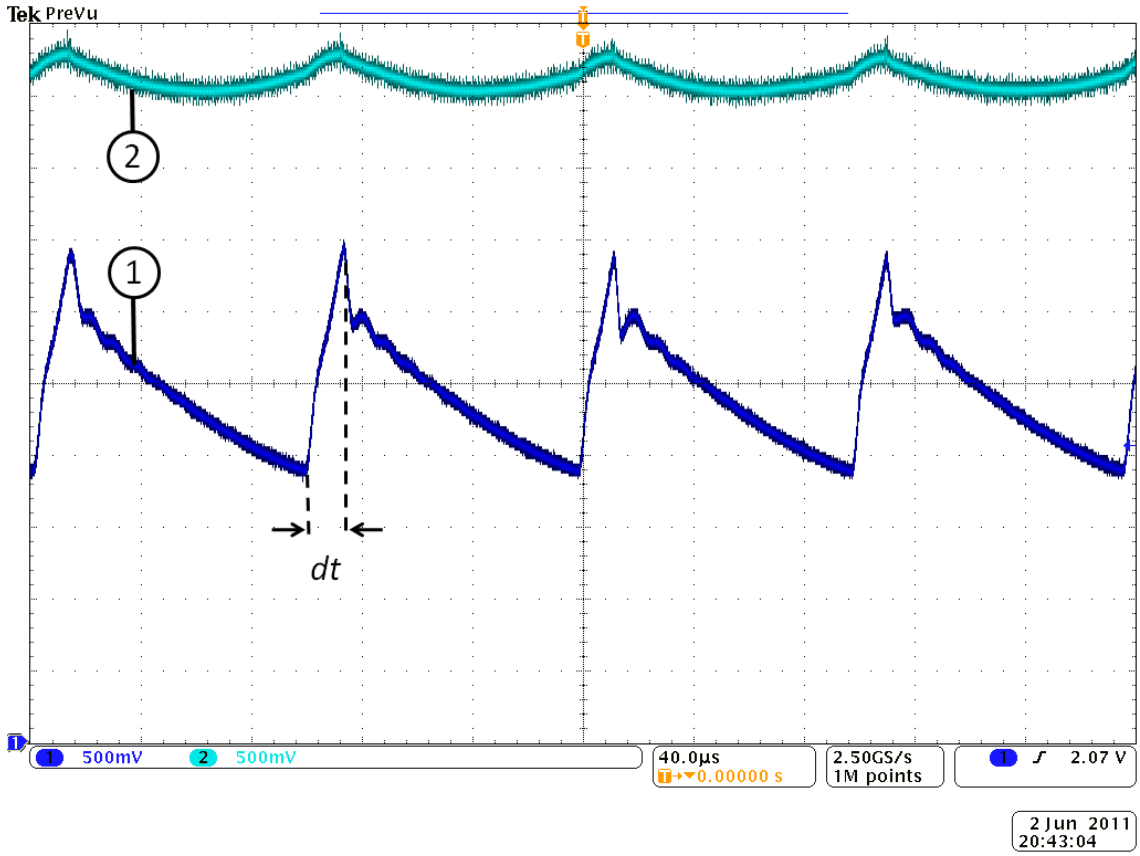
Figure 4.4 – Capacitor switch out transient

The graph in Figure 4.4 shows two traces. Trace 1 (blue) shows the voltage ripple on the capacitor, and trace 3 (purple) shows the calculated capacitance. The time resolution of the oscilloscope is set to two seconds per division in order to capture the step difference when the 10 µF capacitor is manually switched out. The point of switching can be clearly observed from the purple trace as the calculated capacitance drops from 74 µF to 62 µF. The result is subject to inaccuracies in the low voltage experiment as described above. At the point where the capacitance drops, the blue trace displays an increased voltage ripple as expected, since $C \propto \frac{1}{dv}$.

4.6 Duty ratio modulation

As mentioned in section 3.6.1 page 48, there are some issues related to monitoring when the duty ratio is varied to its extremes. The low voltage experiment confirms such issues.

For a high duty ratio as shown in Figure 4.5, a low *dt* and *dv* are observed (off-time) on the voltage signal (trace 1, blue). The issue with a low *dt* is that not enough samples can be taken for accurate measurements. The estimator is therefore programmed to ignore calculations where the duty ratio exceeds 70%.



Horizontal Scale

Time, 40 µs / div

Vertical Scale

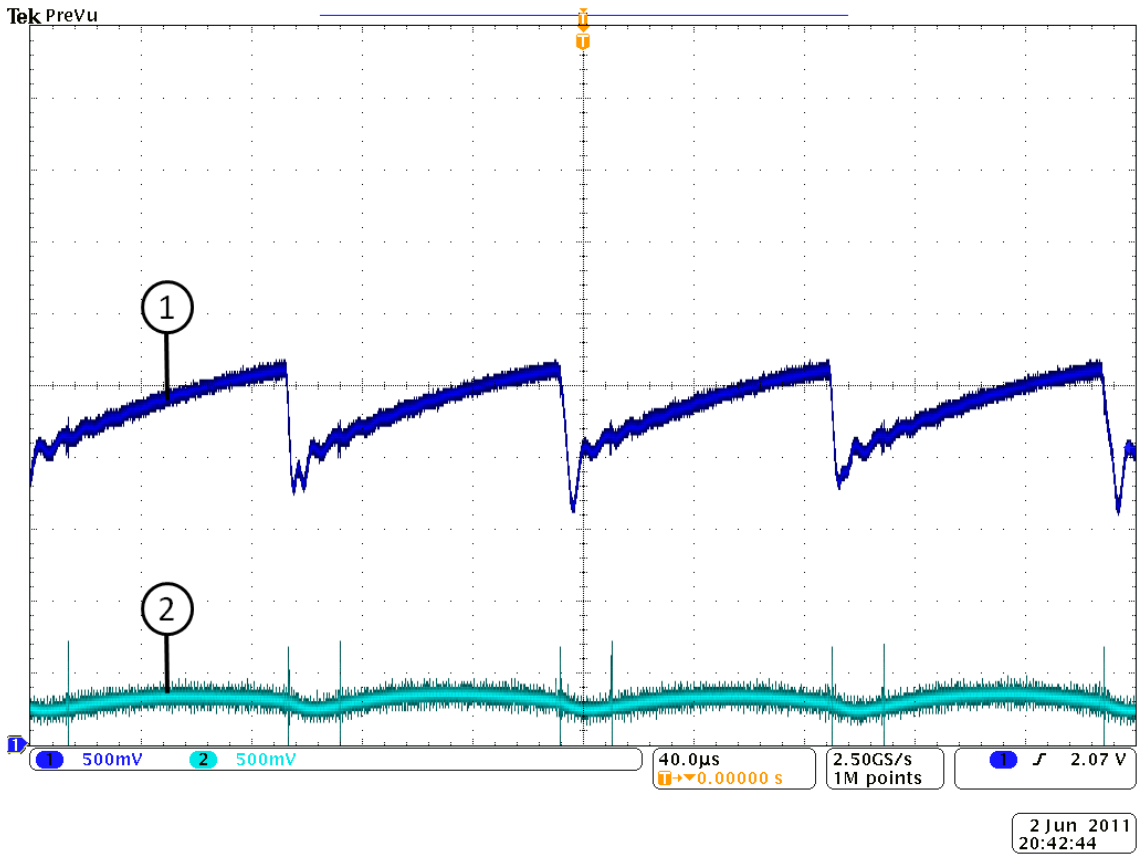
Trace 1 – Voltage monitor, 500 mV / div ($V_{monitor} = 2.125V_c$)

Trace 2 – Current monitor, 500 mV / div ($V_{currentmonitor} = 1.575I_1$)

Figure 4.5 – High duty ratio (~90%)

At the other extreme, when the duty ratio is low as shown in Figure 4.6, the voltage ripple – as in a high ratio cycle – has a very low amplitude. In addition, the sampled current is also very low, since little power is being delivered to the load. Inaccuracies

and noise become significant under this condition. The estimator will also ignore calculations below a 30% duty ratio.



Horizontal Scale

Time, 40 µs / div

Vertical Scale

Trace 1 – Voltage monitor, 500 mV / div ($V_{monitor} = 2.125V_c$)

Trace 2 – Current monitor, 500 mV / div ($V_{currentmonitor} = 1.575I_1$)

Figure 4.6 – Low duty ratio (~10%)

4.7 Conclusion

The capacitor measurement and switch out event was clearly observed in the graphs.

The expected limitations related to the PWM duty ratio have been confirmed in the test set up. When comparing the low, medium and high duty ratio ranges in Figure 4.3, Figure 4.5 and Figure 4.6 respectively, it can be observed that the value of *dv* is at its optimum at 50% duty ratio. Naturally, a high value for *dv* increases measurement accuracies. Figure 3.16 page 51 showed how the ripple voltage varies with respect to the PWM duty ratio. Monitoring between 30% and 70% duty ratio also provides optimum values for variables *dt* and *∫I*, as confirmed in the previous chapter.

It can be concluded that the estimator is able to successfully calculate the capacitance using the voltage and current monitoring waveforms for the low voltage experiment. The experiment allowed the entire condition monitoring chain to be calibrated, and verified for its operation.

High Voltage Experimentation

Chapter 5

5.1 Introduction

This chapter describes the high voltage implementation of the condition monitoring system discussed in the preceding chapters. The system will be implemented on the high voltage electric landing gear (ELGEAR) test rig, set up at Newcastle University, with the fault tolerant motor provided by Goodrich Aerospace.

The chapter will provide a description of how the rig is set up, and how the various test conditions (e.g. a capacitor fault) are implemented. This is followed by analysing how various factors and operating conditions influence the accuracy of the estimation technique, with suggestions of improvement.

5.2 High voltage test rig

The set up of the capacitor condition monitor is limited to one motor drive unit. The duplex system will still be operating simultaneously since this is the nominal condition. The high voltage test rig is powered using a single source of +540 V dc instead of a dual ±270 V dc source. This is due to the limited availability of laboratory equipment.

The complete set up of the high voltage rig is depicted in Figure 5.1. Both drives have individual controllers and feedback signals and are linked to the master computer which acts as a human interface device. The permanent magnet motor consists of two independent three phase windings, integrated in one stator.

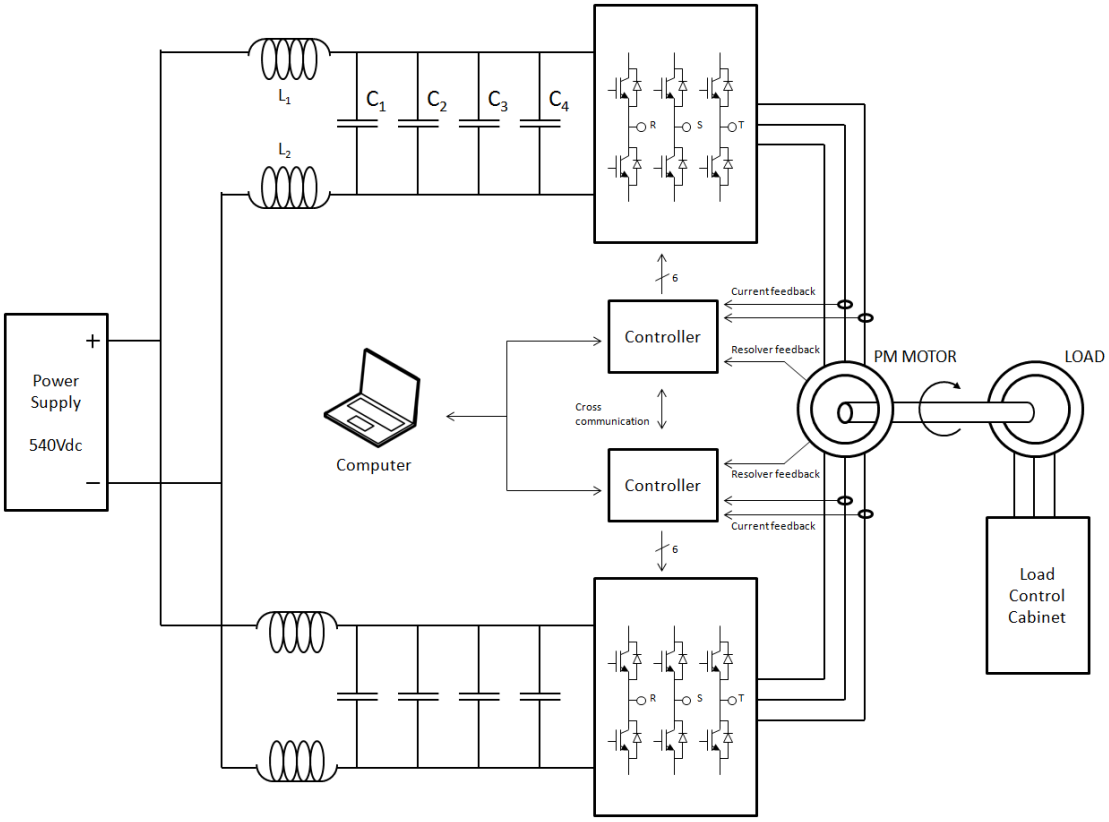
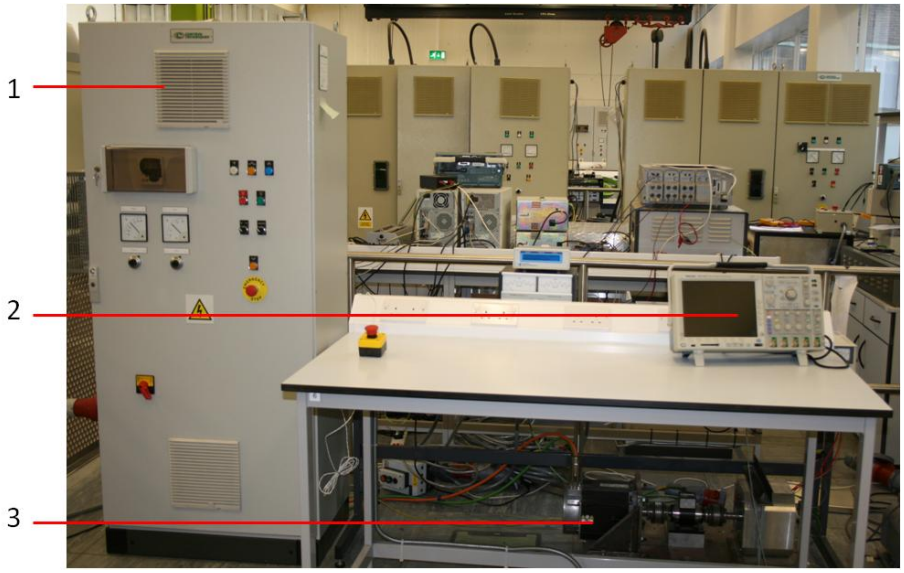


Figure 5.1 – Rig set up

5.2.1 *Pictures*

Pictures of the set up are shown in the figures below.



1 – Load control cabinet

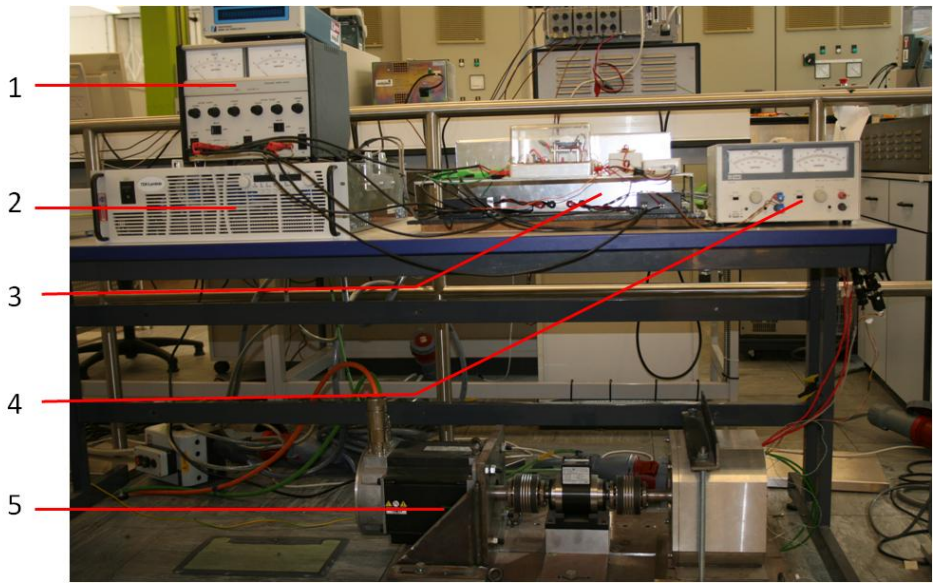
2 – Oscilloscope & working bench

3 – PM motor and load, mechanically coupled

Figure 5.2 – Set up of the rig

The set up in Figure 5.2 shows the load control cabinet on the left, the PM motor and load on the floor behind the bench, and the oscilloscope on the working bench. The equipment behind the working bench is related to high power and is placed there to prevent easy access. In addition, all high voltage equipment behind the bench is protected to prevent accidental contact.

The detailed picture of the rig behind the bench is shown in Figure 5.3. The set up shows the high voltage power supply (540 V dc), low voltage power supply (supplying the control electronics), the motor drive electronics (including the capacitor monitoring electronics) and the PM motor and load.



1 – Low voltage power supply (28 V)

2 – High voltage power supply (540 V)

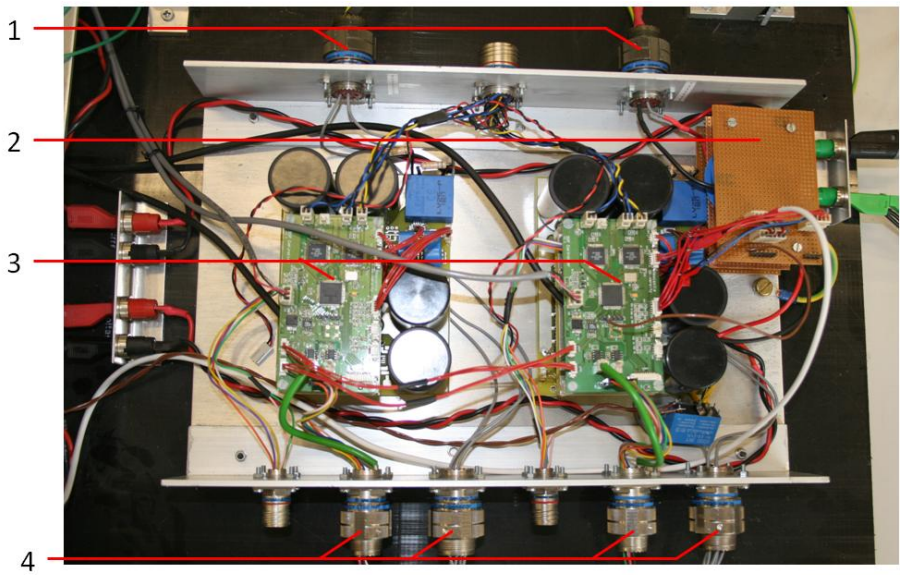
3 – Motor drive electronics & monitoring circuits

4 – Separate power supply to switch out one capacitor

5 – PM motor and load, mechanically coupled

Figure 5.3 – High voltage section of the rig

The motor drive electronics are detailed in Figure 5.4. The entire drive is enclosed in a grounded metallic casing (not on picture) secured by the emergency stop of the power supply to prevent high voltage exposure. At one end, two ARINC (technical standard for the data bus in aerospace) connecters interface with the 540 V dc supply. The drives are bolted onto an aluminium back plate that acts as a heat sink for the IGBTs as well. The ARINC cables on the other end of the drive interface with the PM motor.



1 – High voltage, 540 V dc input

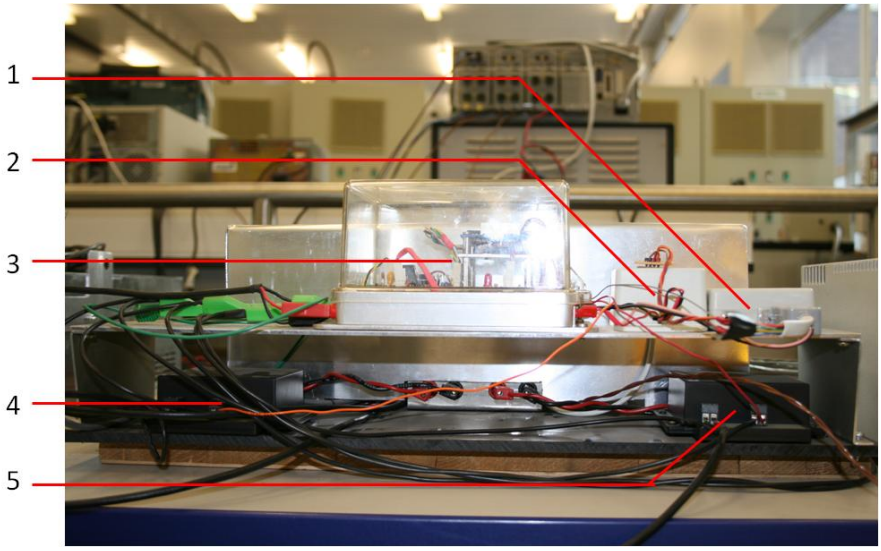
2 – Enclosure of the differential input coils

3 – Motor drive electronics

4 – Output to the PM motor & feedback signals

Figure 5.4 – Motor drive electronics modules

The details of the capacitor monitoring equipment are found in Figure 5.5. At the bottom, two black boxes can be seen. These are the current and voltage monitoring boxes where the high voltage is isolated. The estimator is enclosed in a see-through casing. To the right of the estimator box, two white boxes are found, which are the timing circuit and the isolation gate circuits.



1 – Timing circuit

2 – Gating isolation (from the IGBTs)

3 – estimator, capacitance calculation module

4 – Current monitoring circuit

5 – Voltage monitoring circuit

Figure 5.5 – Capacitor monitoring equipment

5.2.2 *Power supply*

The power supply used is a Regatron TopCon Quadro (ratings 600 V dc, 32 A).

According to DO-160F [13], there should be two independent power supplies to maintain fault tolerance across the entire system. These power supplies are two symmetrical ±270 V dc supplies. Due to the limited availability of equipment in the lab at the time, a single unit was used to power both drives.

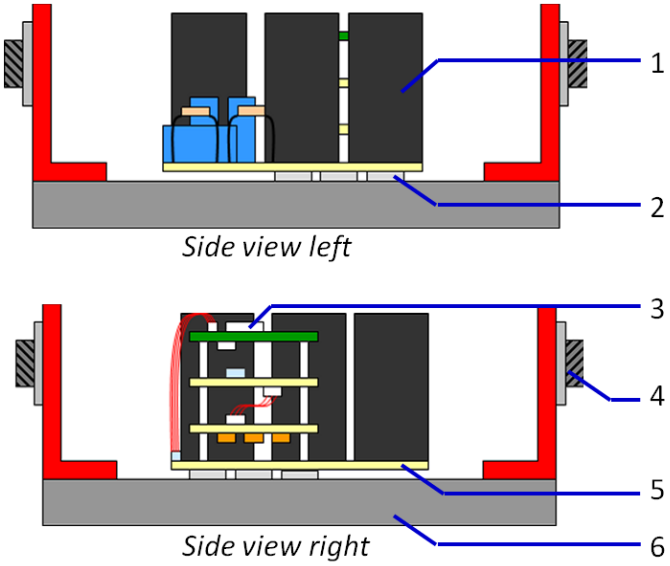
5.2.3 *Drive*

The two separate drives are photographed individually in Figure 5.6.

Figure 5.6 – Test rig details

Referring to Figure 5.7, the drives are identical and contain:

- A low voltage board. This board consists of the main controller, a dsPIC33F128MC by Microchip, two ARINC microprocessors that communicate with the aircraft bus standard, and various other ports that communicate with the master computer. Below the low voltage board, other boards can be found that contain high voltage gate isolators.
- Base plate. The base plate is made of Aluminium and acts as a heat sink to the IGBTs.
- Dc-link capacitors. Four capacitors of 20 µF 600 V each.
- High voltage board. This board holds the capacitors and has flooded plains of +540 V on one side, and 0 V on the other. This is to ensure laminated bus-bar design.
- IGBT transistors. These transistors are positioned between the high voltage board and the base plate. Between the base plate and the IGBTs is a thermal pad that isolates electrically, but conducts thermal heat.
- The drives communicate with the “outside world” through ARINC connectors mounted on to the base plate.



1 – 4 x 20 µF MPPF capacitors

2 – IGBT modules (inverter)

3 – Control board (low voltage)

4 – ARINC interfaces

5 – High voltage board

6 – Aluminium foundation plate, also acting as a heat sink

Figure 5.7 – Side view drawing of the MDE module

The controllers obtain motor phase current feedback from two current transducers placed in the motor's phases. Another feedback comes from the resolver of the motor which determines its instantaneous position and velocity.

The controllers are each linked with the inverter, controlling the six IGBTs. Both controllers are linked through cross-communication signals. These signals ensure that both controllers equally share torque.

5.2.4 *Master computer*

The master computer is used as a human interface device to the controller. From the master computer the demanded speed can be set. Many more configurations are possible, such as disabling a drive, varying the PI settings etc. The master computer is also used as a diagnosis of the system, ensuring the controller is functioning adequately.

5.2.5 *PM motor and load*

The permanent magnet motor used consists of two independent three phase motors integrated in to one stator. Both three phase connections are independently controlled by the two motor drive units. A 10 pole pair rotor drives the axel which is connected to the

load. The loading machine is provided by the company Control Techniques and can be controlled using the load control cabinet.

5.3 Experimental set up

The fault tolerant motor drive electronics of the aerospace test rig consists of two active drives as shown in Figure 5.1, page 78. As aforementioned, the monitoring system is only implemented on one drive and is set up according to Figure 5.8.

The leads of the voltage monitoring sensor are directly connected across the terminals of the capacitors (blue). The current monitoring sensor is connected in series to the return of the 540 V supply (turquoise). The top three IGBTs gate drive control lines are linked to the timing logic module using high voltage isolated opto-couplers.

The voltage and current monitors are galvanically isolated on the high voltage primary side, while the secondary side is referenced to the low voltage ADC ground at the estimator. The estimator is programmed in C-language and will simultaneously sample the voltage and current at the appropriate time determined by the timing module. The estimator outputs a voltage between 0 and 5V corresponding to a capacitor range from 0 to 100 µF (purple).

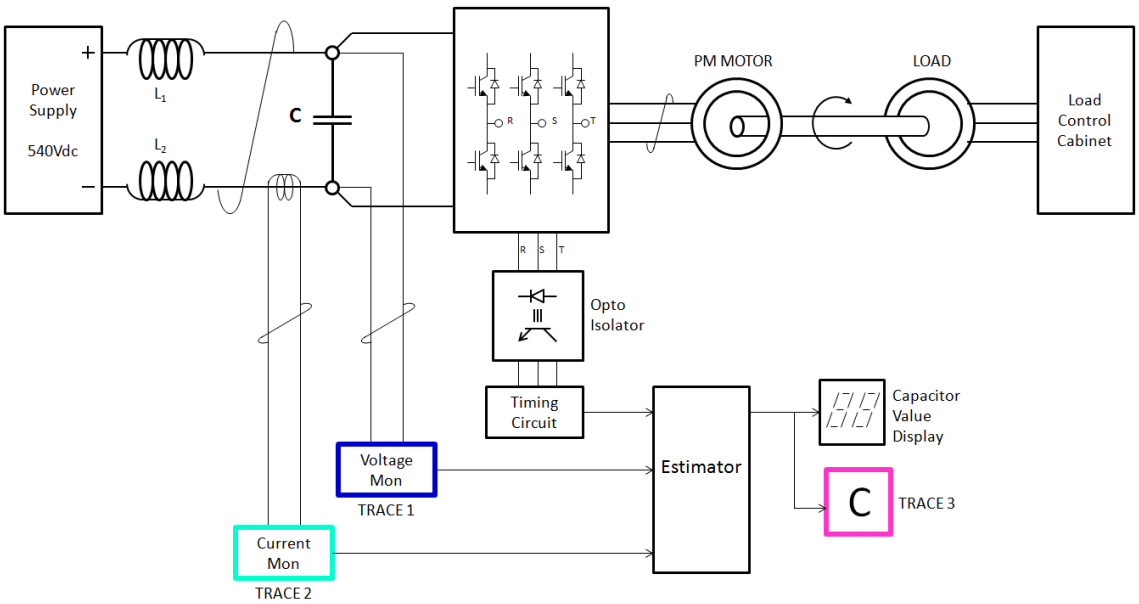


Figure 5.8 – High voltage experimental set up (one drive only)

5.4 Capacitor fault simulation

Figure 5.9 shows the detail of the four dc-link capacitors used in the drive. The literature indicated that the most common dc-link capacitor fault for MPPF technology

is the open circuit fault. This fault is simulated by purposely removing a capacitor from the dc-link by switching it out of the circuit.

5.4.1 *Switching method*

It has been foreseen that the capacitor must be switched whilst the drive is operating since a fault could occur at any instant, and must be monitored in real time. Referring to Figure 5.9, the capacitor C4 is switched whilst the circuit is operational. Due to the high voltage environment, a relay is used and remotely operated from a separate low voltage circuit. The normally-closed relay is used for the purpose of simulating an active open circuit fault (i.e. a decrease from 80µF to 60µF). The series resistor *Rs* is implemented for safety reasons, as discussed in the following section.

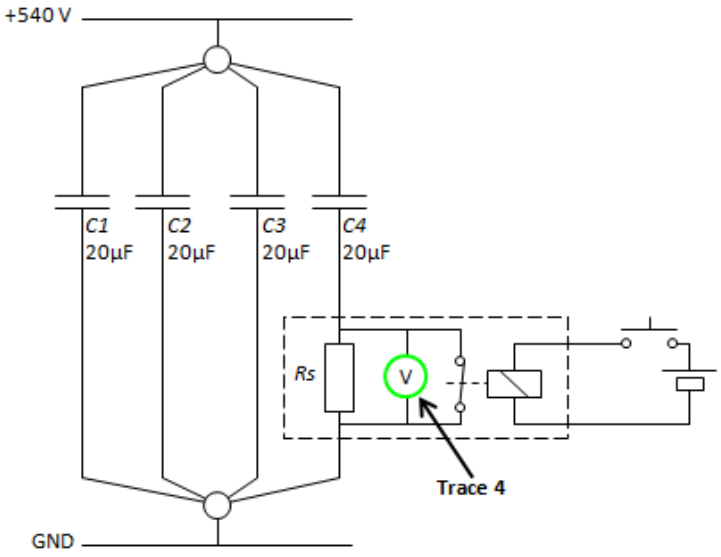


Figure 5.9 – Capacitor connection detail

5.4.2 *Capacitor fault switching*

It is important to pay attention that the additional components introduced do not impede the nominal functionality of the capacitor C4.

At 10 kHz the impedance of C4 (20 µF) is $X_c = 0.8\,\Omega$. The relay's contact resistance should therefore be less than 1%, (8 mΩ). This is to ensure that the relay resistance remains negligible compared to the capacitor's impedance. This value cannot be easily achieved since the best relay available was the *Rapid GZ-SS-124*, 2x16 A contacts, max 100 mΩ/contact. By connecting the contacts in parallel, the resistance should be brought down to <50 mΩ, corresponding to 6.25% of the capacitor's impedance.

The series resistor chosen will have a value of at least 100 times the capacitor impedance, >80 Ω. As a result a resistance of 1 kΩ is chosen to be well above this limit. An excessively low series resistor will partially shunt ripple current and falsify final capacitance readings. A resistor which is too high will cause a slower charge and discharge of the capacitor voltage when the system is powered up and down respectively. For the 1 kΩ resistor, the time taken to charge and discharge to 99% of its initial value is 100 ms. This is an acceptable time to wait until the rig is safe to handle in the event the high voltage supply is switched off whilst the relay is still powered:

$$99\% = 5\tau = 5 \times RC = 5 \times 1k \times 20\mu = 100ms$$

5.4.3 *Safety issues*

There are a number of safety issues related to switching in and out the capacitor C4:

- It is important that the capacitor is never charged when the circuit is switched off. This could cause a potential safety hazard when working on the rig when the set up is assumed to be powered down.
- Isolation probes must be used at all times. The relay is purposely mounted on the return of the dc-link to ensure the probe can be grounded while measurements take place. This is due to the oscilloscope being grounded as well.
- Another safety issue is when an uncharged C4 is switched in to the active dc-link. If this happens, the remaining three capacitors will immediately charge C4, where the current is limited by the equivalent series resistance.

The above points are solved by the following:

Switching in and out the capacitor of C4 is performed using a normally closed relay contact. The switch activating the relay is a push button type. In combination with the normally closed relay, it guarantees that the capacitor is only switched out whilst the manual switch is actively pressed. Regardless the case, due to the configuration it is impossible to switch in an uncharged C4. The worst case scenario occurs when the push button is pressed whilst the high voltage supply is switched on. In this case, the capacitor C4 will charge to 99% of the rated value in 100 ms.

As an additional safety measure, a (relatively) high ohmic resistor *Rs* shunts the normally closed contact. This guarantees that the capacitor will always remain charged at dc-link voltage in the event of a relay failure.

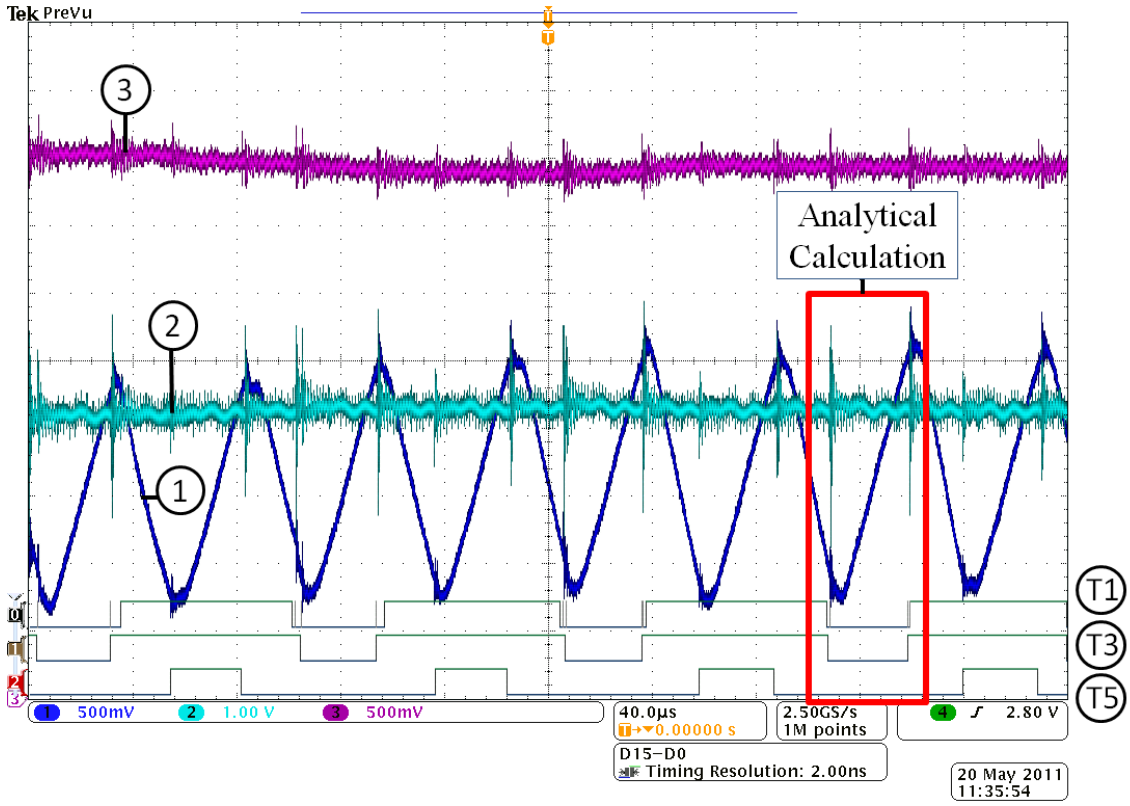
The switching in and out of the capacitor is monitored with an isolated voltmeter across the series resistance (green, trace 4, Figure 5.9, page 85).

5.5 High voltage nominal operation (80 µF)

For reasons of consistency, the colour and label of the traces in the results refer to those shown in Figure 5.8 and Figure 5.9, and is maintained throughout the chapter.

Figure 5.10 shows the high voltage measurement results during nominal operation (relay switch closed, total capacitance = 80 µF), during a 55% duty cycle. At the bottom of the graph, the digital control signals of IGBTs *T1*, *T3* and *T5* can be found which are also fed in to the timing logic.

In the graph, the zero voltage state occurs 8 times by observing the *dv* charging slopes (trace 1). The zero voltage states have a time period of approximately 40 µs.



Horizontal Scale

Time, 40 µs / div

Vertical Scale

Trace 1 – Voltage monitor, 500 mV / div ($V_{monitor} = 2.125V_c$)

Trace 2 – Current monitor, 500 mV / div ($V_{currentmonitor} = 1.575I_1$)

Trace 3 – Capacitance calculation DAC output, 500 mV / div (10 µF / div)

Digital trace 0, 1, 2 – IGBT T_1, T_3, T_5 respectively

Figure 5.10 – High voltage experiment

The analogue voltage output of the estimator DAC (trace 3) shows a calculation of 80 µF, confirming the expected value. A high frequency ripple is observed on the trace as a result of the DAC output on the estimator. Similar to the low voltage experiment, noise can be observed at the points where the IGBTs switch. This noise is caused by the parasitic inductances on the IGBT which have an effect on high transients.

Trace 2 shows the current monitor output. From the graph, it can be seen that the current is not precisely constant over the full span. This is due to the low frequency current ripple of 900 Hz which is generated by the inverter (as explained in section 3.6.2, page 51) and possibly due to the power supply regulation. In addition a higher frequency ripple is observed of approximately 60 kHz. This higher frequency is far out of the current monitor's cut-off frequency filter of 10 kHz, and is suspected to be either radio frequency interference or conducted noise.

From the same graph, an analytical calculation is performed to cross check the results of the estimator. Equation (5.1) confirms the accurate measurement.

Measured ripple voltage: $V_{monitor} = 1.9V$

Voltage calibration: $V_c = \frac{V_{monitor}}{2.125}$

Calculated *dv*: $\frac{1.9}{2.125} = 0.89V$

Measured current reading: $V_{currentmonitor} = 4.0V$

Current calibration: $I_1 = \frac{V_{currentmonitor}}{1.575}$

Calculated $\int I$: $\frac{4}{1.575} = 2.54A$

Measured *dt*: $28\mu s$

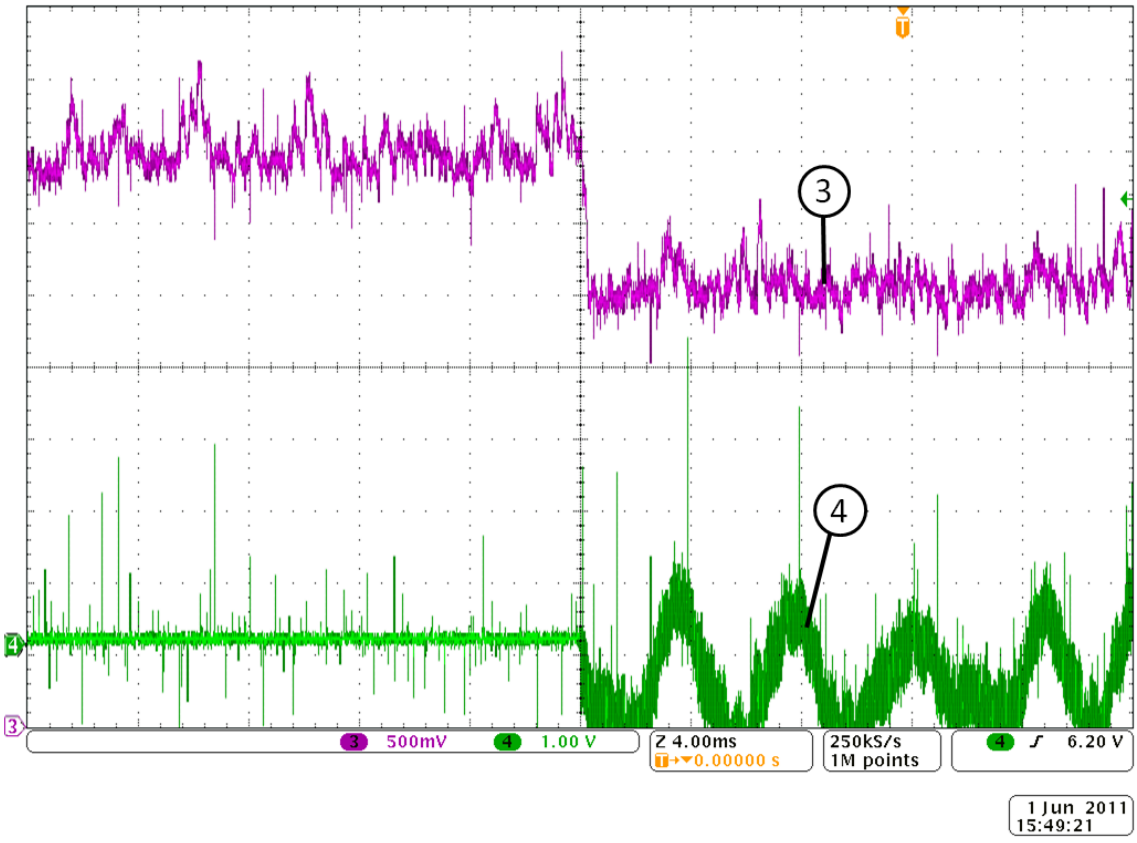
$$C = \frac{\int Idt}{dv} = \frac{2.54 \times 28 \times 10^{-6}}{0.89} \approx 80\mu F \qquad (5.1)$$

5.6 Capacitor switch out (80 µF to 60 µF)

Under the same conditions as in the previous section, capacitor C4 is switched out to simulate an open circuit fault, see Figure 5.11. An additional probe is connected across the resistor *Rs*, to indicate the exact point when the capacitor is switched out. This is

more accurate than observing the push switch, since the relay circuit is subject to a reaction delay caused by its magnetising inductance. The trace shows zero voltage when the relay is not energized (*Rs* is short-circuited) but when energised, the graph shows a ripple. This ripple is effectively the dc-link voltage ripple while the dc component is filtered out by capacitor C4. In effect, C4 and *Rs* form a high pass filter.

From the purple trace (3), it can be seen that the estimator is able to detect a switch out in capacitance since the trace drops from approximately 4 V (corresponding to 80 µF) to 3 V (corresponding to 60 µF). Figure 5.12 shows the same switch out event, but with a different time scale. It is evident that the condition monitoring system is able to detect a switch out of capacitance within 400 µs. In order to obtain the best reaction time, the calculated samples are not going through a statistical filter.



Horizontal Scale

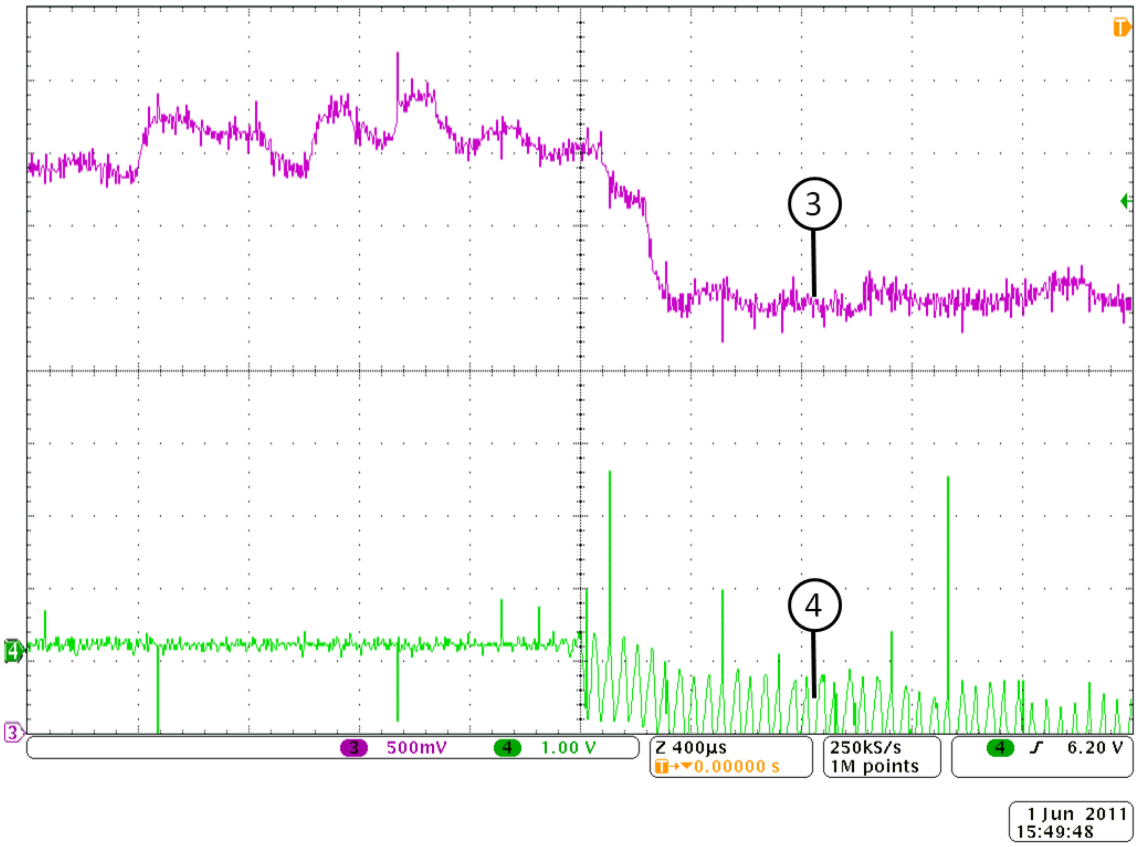
Time, 4 ms / div

Vertical Scale

Trace 3 – Capacitance calculation DAC output, 500 mV / div (10 µF / div)

Trace 4 – Voltage across the series resistor *Rs*, 100 mV / div

Figure 5.11 – Capacitor switch out (zoomed out), no filtering of data



Horizontal Scale

Time, 400 µs / div

Vertical Scale

Trace 3 – Capacitance calculation DAC output, 500 mV / div (10 µF / div)

Trace 4 – Voltage across the series resistor *Rs*, 100 mV / div

Figure 5.12 – Capacitor switch out (zoomed in), no filtering of data

5.7 Filtering techniques

In order to remove noise from the capacitance estimate data, filters must be applied. In general, the higher the time constant of the filter, the longer it takes for the system to display a change in the capacitance estimate.

5.7.1 *No filter*

The results in Figure 5.11 and Figure 5.12 are optimised for the fastest reaction time when the capacitor is switched out. To achieve this target the measurement process is restricted to a minimum number of samples for the zero-state (i.e., allowing sampling to take place beyond the 30-70% duty ratio). In addition, no form of filtering is applied, and the output data in the figures are in effect the 'raw data'.

Although a drop in capacitance of 20 µF is still observed, the quality of the waveform is rather poor as the deviation of samples is in the order of 5 to 10 µF. This is mainly due

to the modifications of reducing the number of samples for the zero-state. Part of the disturbance may originate from the contact bouncing of the isolation relay. It is therefore assumed that the bouncing time in combination of the measurement disturbances are significant factors to take in to account in Figure 5.12.

5.7.2 *Introducing a data filter*

In this particular application, there is no disadvantage in introducing a data filter. The aim of this system is to flag up a maintenance issue for the ground staff. As mentioned earlier, when an open circuit fault occurs in one capacitor, the drive is able to continue indefinitely without any sort of compromise in performance. Taking this in to account, a delayed reaction of several seconds or even minutes is acceptable.

Currently, a number of software filters have been introduced in the monitoring scheme:

- A minimum allowable current is set to 500 mA. When the current rating is lower than this value, the sample is discarded.
- A minimum of four samples will take place during each zero-state. This corresponds to three values for dv, four values for $\int I$ and three values for dt. It also indicates that the duty ratio is not above 70%. When a calculation is performed where there are less than four samples available, the sample will be discarded.
- A minimum allowable duty ratio of 30% will be permitted. The estimator analyses the average gradient of dv taken. When the gradient is too low, it is an indication of a low duty ratio. When this is the case, the sample is discarded.
- Invalid calculated samples. When the calculation result is zero or above 100 µF, there is an indication that an error in sampling took place. The sample will then be discarded.

When any of the above points trigger an invalid sample, the estimator will discard it accordingly. If 10 samples in a row are discarded, the estimator will send an error signal (in the form of a red LED), indicating that too many samples have been discarded.

Successful samples that fulfil the requirements are stored in a data array of 64 samples, where the average is computed. The filtering method is shown in Figure 5.13.

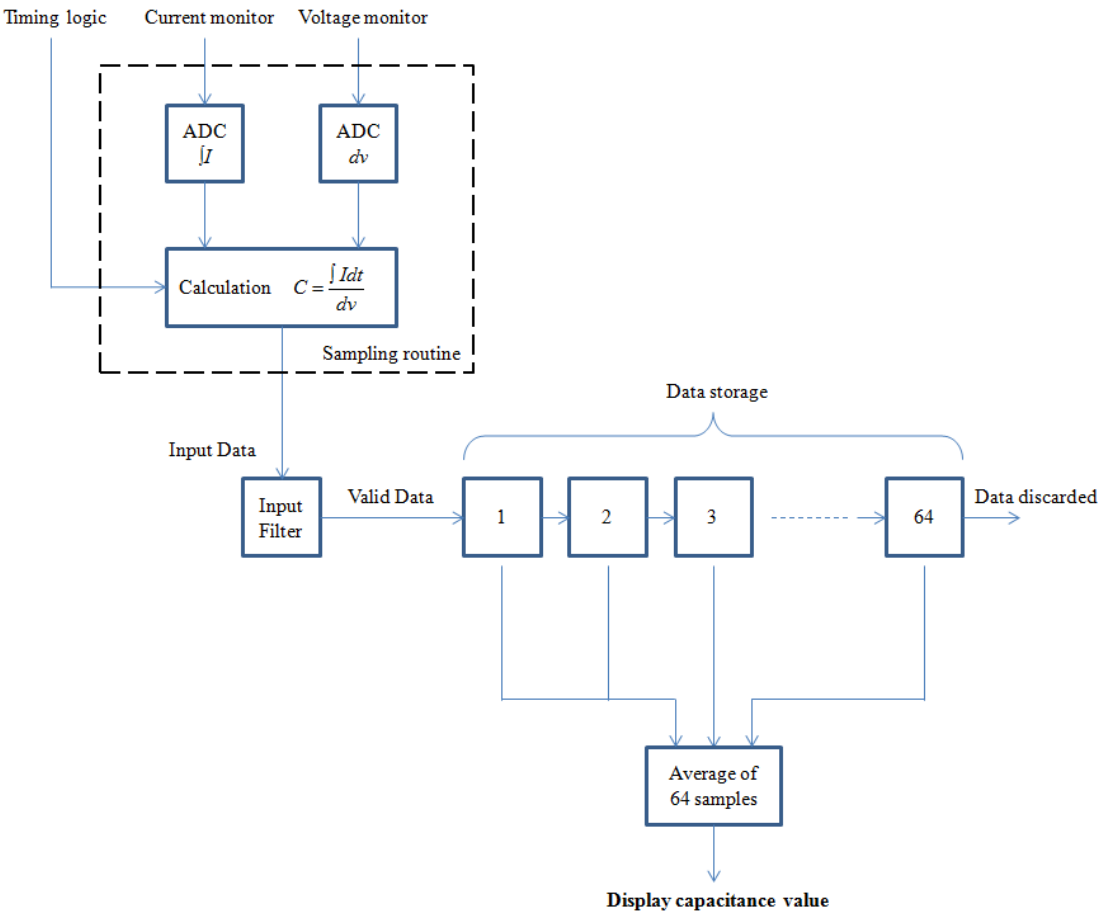
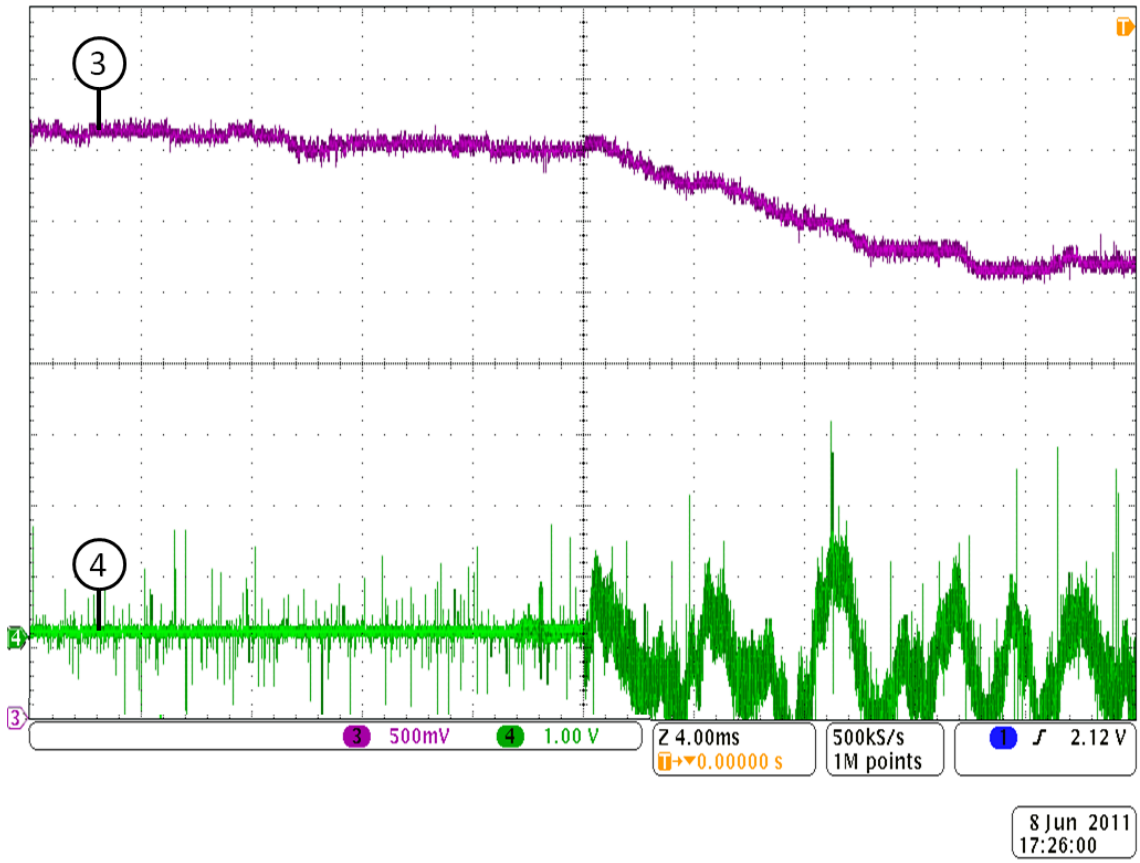


Figure 5.13 – The implemented filter

The results in Figure 5.14 show a significant improvement in terms of the data's deviation. Naturally, there is a much longer delay when detecting a change in capacitance, in this case it is approximately 16 ms. The filter proposed is rather simple, where just the average of the last 64 values are taken. Further improvements can be made by applying more adequate filtering algorithms depending on the application.



Horizontal Scale

Time, 4 ms / div

Vertical Scale

Trace 3 – Capacitance calculation DAC output, 500 mV / div (10 µF / div)

Trace 4 – Voltage across the series resistor *Rs*, 100 mV / d

Figure 5.14 – Results after filtering

5.8 Statistical analysis and accuracy

This section discusses the accuracy of the implemented technique. An independent RLC (resistor, inductor, capacitor) network analyser with a four wire sensing method is used to independently measure the exact dc-link capacitance (Fluke PM 6304). The RLC measurement is compared to the condition monitoring system during pre-fault (80 µF dc-link capacitance) and post-fault operation (60 µF dc-link capacitance). Furthermore, the experiment is performed with only one of the two drives operational and the analysis is summarised in Table 5.1 and Table 5.2 respectively.

One drive operational	Measured (RLC) [µF]	Mean Estimated [µF]	Standard Deviation
No filter			
Pre-fault	78.21	80.00	3.38
Post-fault	58.41	61.57	3.19
With filter			
Pre-fault	78.21	79.69	0.80
Post-fault	58.41	61.04	0.87

Table 5.1 – Statistical analysis with one drive operational

Two drives operational	Measured (RLC) [µF]	Mean Estimated [µF]	Standard Deviation
No filter			
Pre-fault	78.21	78.79	7.93
Post-fault	58.41	61.11	5.33
With filter			
Pre-fault	78.21	77.92	1.79
Post-fault	58.41	60.17	1.49

Table 5.2 – Statistical analysis with two drives operational

In all cases the mean value of the estimated capacitance is close to the independently measured value, with an accuracy ranging from 95 – 100%.

The presence of a filter reduces the standard deviation (the average deviation of any sample from the mean) by approximately 75%. The most accurate data can be found when operating one drive only, with a filter in place.

There is however a clear correlation between the accuracy of the sampled data and the operational drives. Under nominal condition, when both drives are operating, the second drive is causing noise that interferes with the capacitor monitoring in the first drive. This is a consequence of the independent controller clocks which are not synchronised. Whilst the monitoring device is sampling, the IGBTs in the second drive switch,

causing high frequency spikes to be induced in the first drive. The noise could propagate through conducted emissions, as both drives share the same power supply and are therefore not electrically isolated.

Details of this phenomenon are given in section 5.9.2 page 97. More details on the type of noise that is transmitted or received can be found in appendix B, page 182.

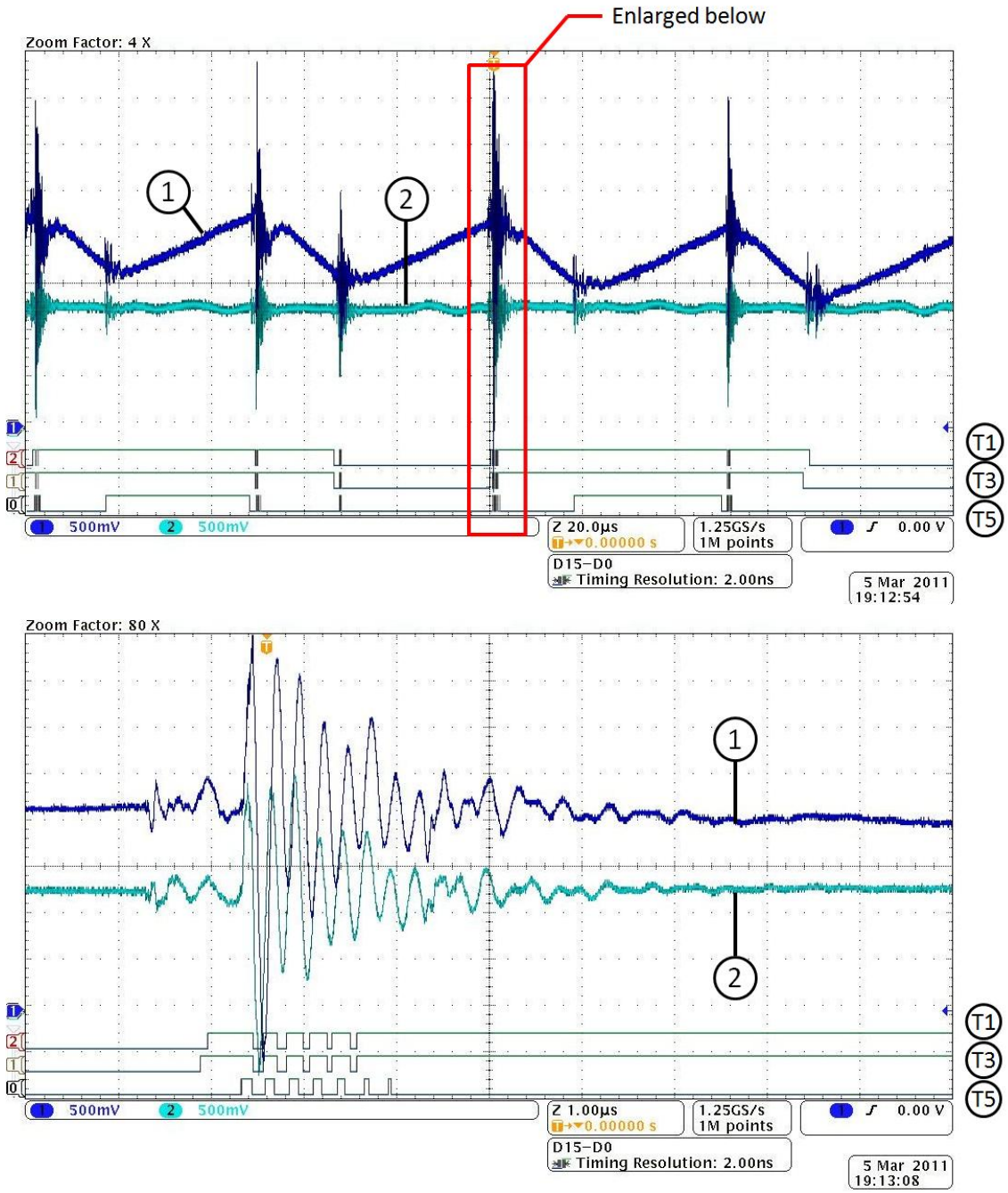
5.9 High voltage experimental evaluation of capacitance estimator

In this section, a number of issues were discussed related to the configuration of the duplex fault tolerant drive. Due to limitations of the lab environment as well as a non-ideal drive design, some improvements are proposed.

5.9.1 *Minimising IGBT switching noise*

The IGBTs in the inverter form the largest contributor to noise in the circuit. As with the dc-link capacitors, the inverter was designed to be compact rather than to comply with EMC standards. The noise produced by the inverter interferes with the sensitive instrumentation.

When an IGBT switches, it inevitably causes switching noise due to its inherent parasitic inductance and capacitance. When the design layout of the dc-link is not optimised, it may contribute towards inductance and capacitance which worsens the switching noise. An example of such noise is depicted in Figure 5.15. High frequency ringing noise is observed on the voltage and current waveforms.



Horizontal Scale

Top graph: Time, 20 µs / div

Bottom graph: Time, 1 µs / div

Vertical Scale

Trace 1 – Voltage monitor, 500 mV / div ($V_{monitor} = 2.125V_c$)

Trace 2 – Current monitor, 500 mV / div ($V_{currentmonitor} = 1.575I_1$)

Digital trace 0, 1, 2 – IGBT T_1, T_3, T_5 respectively

Figure 5.15 – Switching noise on the IGBTs

5.9.2 *Issues involving two drives in operation*

The duplex fault tolerant drive architecture consists of two identical motor drive electronics (MDE). These are independent and separately controlled running on its own clock.

Both units share a cross communications link to ensure the torque is equally shared between the modules under nominal operation. This is to prevent one unit from becoming dominant and taking over the system. Furthermore, when both drives do not communicate, two independent regulation mechanisms may lead to oscillation as the modules could work against each other.

Although the components are identical and communicate effectively, the clock frequency in one unit will still differ slightly from the other, which could be seen in the form of a temporary phase offset. The difficulty is that the inverters of both drives are not synchronised at PWM frequency.

The problem arises when the IGBTs switch in one inverter, the noise propagates to the other inverter through conducted emissions. The noise most probably propagates through the supply lines from one drive to the other, since both drives share the same power supply. This noise is picked up by the voltage and current sensors as shown in Figure 5.16.

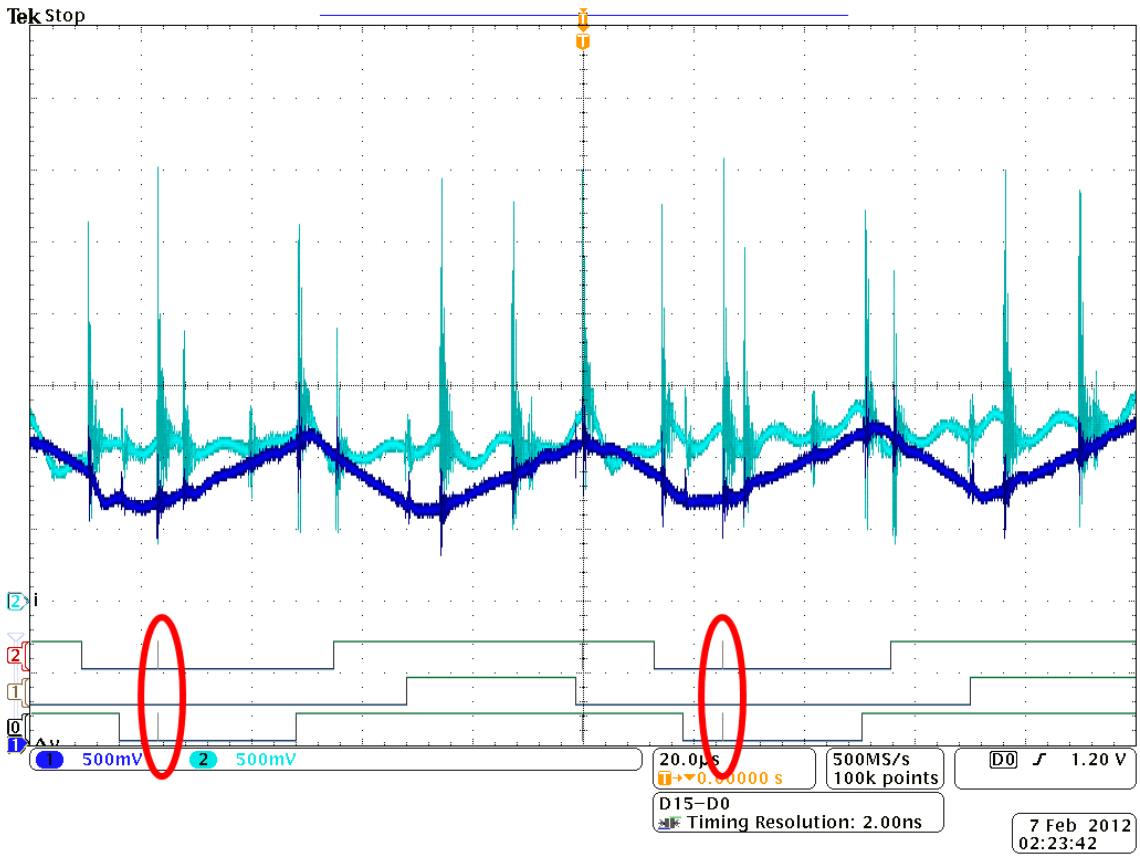


Figure 5.16 – Two drives operational, the red circle highlights the switching noise induced by the mirroring inverter

5.9.3 *Concept vs. flight model*

The duplex fault tolerant drive for ELGEAR was originally designed as a concept drive, focussing primarily on making the drive compact. The drive therefore had a number of differences in design compared to an actual flight model:

- Laminar bus-bar arrangement. In order to constitute to a low-inductance layout, the capacitor terminals are each connected to flooded planes which are separated by an insulating material. The concept drive contains the flooded planes on either side of a dual layer PCB, as appendix A (page 180) describes. The planes are not ideally flooded due to space constraints, and the flooded planes contain narrow gates separating some of the capacitors as a result. An equivalent model is depicted in Figure 5.17, where *R* represents the narrow gates in the flooded planes. A flight model on the other hand would incorporate a better laminar bus-bar design where narrow gates would not be present [42-44].

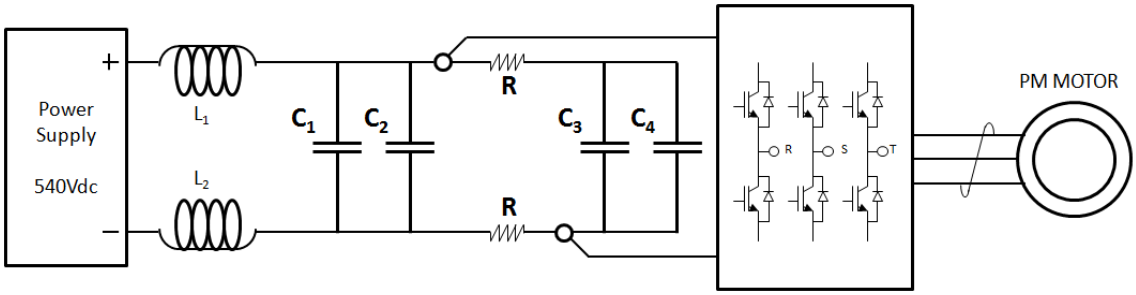


Figure 5.17 – Problematic dc-link layout due to narrow gates in the flooded planes

- Symmetric circuit layout. As discussed in the introduction of this chapter, due to limited resources a single 540 V supply was used instead of a dual ±270 V supply. Symmetric circuit designs have a lot more advantages than asymmetric circuit designs. The intention is that anti-polar currents and voltages compensate locally, and the entire circuit appears to be electrically neutral from the outside. In a flight model – as required by DO-160F [13] – a ±270 V bus supply is present which should significantly reduce the common mode noise in the system. Another advantage of a ±270 V bus supply is the reduction of the corona discharge effect which plays an important role in aerospace environments. For reasons of corona discharge, Boeing recommends that no motor or drive should be used above the 300 V peak [45].

5.10 Conclusion

The novel monitoring technique has successfully been implemented on the duplex fault tolerant drive. The results clearly show a transition when an open-circuit fault takes place.

The following has been achieved:

- Condition monitoring of the dc-link capacitor at a high sampling rate (PWM frequency).
- In-circuit monitoring was achieved under nominal operating conditions. No special action such as disconnection of the capacitors is required.
- The solution was proven flexible, as it functions under a wide range of duty ratios.
- The accuracy of this test setup is assessed to <5%.

The accuracy of the set up is assessed to be better than 95%. The accuracy can be further improved by optimising the electrical environmental conditions.

The monitoring system makes use of existing sensors. They do however require some modification. The current sensor should have a minimum pass-band of several magnitudes greater than 900 Hz (related to the rated speed of the machine). The pass-band implemented was 10 kHz.

The standard built in voltage sensor is in place for protection reasons, and is normally only required to measure the average value of dc-link voltage. The voltage monitor needs to be upgraded to cope with the higher frequency ac components, up to 100 kHz

Additional electronics required for the analogue signal adaptations are minimal. The estimator dsPIC unit can eventually be integrated in to the control unit. Accurate time gating can be derived from the controller's crystal oscillator by adding a small number of logic gates.

The only additional components required are those that modify the monitors as mentioned in the preceding paragraphs.

Faults in Permanent Magnet Motors

Chapter 6

6.1 Introduction

In the introduction of the thesis, fault tolerant topologies were covered. It was emphasised that fault tolerance must be applied across the entire system to avoid single-point failures. For example, auxiliary systems must not be powered from the same power supply. Similarly, the permanent magnet (PM) motor must be designed to sustain a wide range of faults to ensure continuous operation.

In order to test the machines' resilience, various faults are typically induced. The faults have to be picked up by the controller and the sensors, and appropriate remedial action should be taken to limit the damage. Some faults require immediate action of the controller, where the drive is configured in such a way that the fault is isolated from the system. More benign faults do not require any action but should still be reported for maintenance.

In aerospace applications, PM motors are currently the preferred technology due to their high torque per-unit mass. Recent works have shown that PM motors can be designed to accommodate various faults, leading to the fault-tolerant PM motor. Most faults induced on PM motors can be detected and dealt with effectively. More worrying is the turn to turn fault where adjacent wires in a coil are touching. This fault creates localised hot spots which could lead to fault propagation if not dealt with swiftly.

This chapter will cover various existing fault tolerant topologies in the literature. It then focuses on the ELGEAR motor, which is the fault tolerant motor used in this project. The chapter continues by covering the variety of faults that could occur on a PM motor, as well as the appropriate remedial actions that should be taken to limit the damage.

6.2 The development of the fault tolerant PM motor

Extensive work has been performed on improving fault tolerant PM machines and drives [46, 47]. One of the first principles of fault tolerant design was outlined by Haylock, Mecrow and Jack in 1996/1997 [48, 49]. The authors pointed out that switched reluctance motors (SRMs) had inherent fault tolerant characteristics, whilst the

PM machine was able to deliver more torque. The authors modified the PM machine to incorporate the fault tolerant features of SRMs. The result was that the fault tolerant PM motor was able to deliver almost twice the amount of torque per-unit mass compared to SRMs.

The principle modifications of the PM motor that lead to the fault tolerant PM motor are listed below:

1. **Physically isolating phases** – One of the more severe faults is the phase-phase fault, where two phases of the machine could potentially be disabled. For that reason, phases are physically separated by placing each winding in its own stator slot. In effect, the phases are separated by an additional stator tooth, as shown in Figure 6.1. This way, the likelihood of a phase-phase fault occurring is significantly reduced.

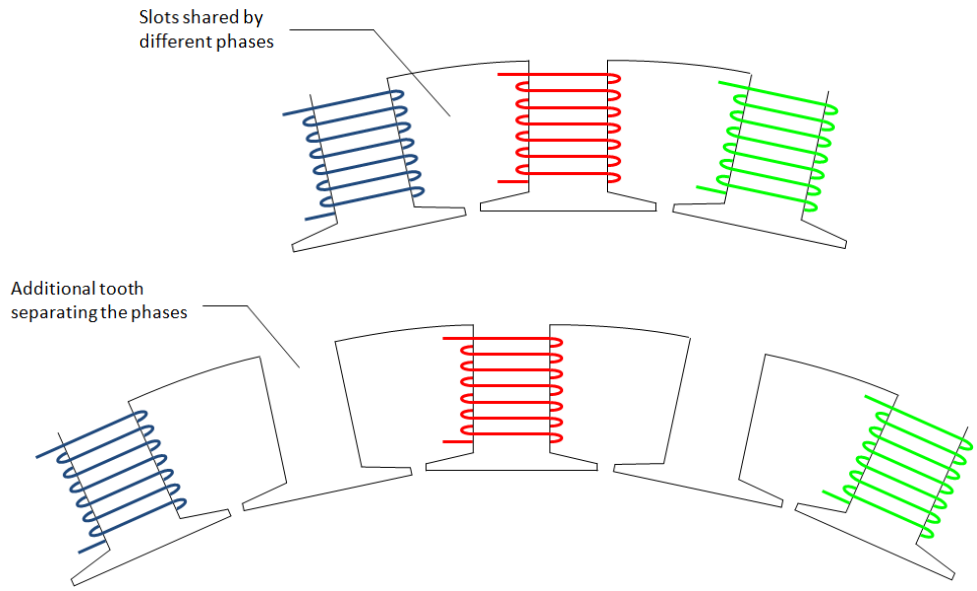


Figure 6.1 – Top diagram shows the conventional method when phases share the same slot. The bottom diagram shows the additional tooth incorporated in machine design to physically isolate the phases

2. **Thermal isolation** – If for any reason the motor windings were to heat up as a result of a fault, the thermal fault may propagate to healthy parts of the motor. The additional tooth to physically separate the phases also provides thermal isolation. Assuming the stator core back is sufficiently cooled; the additional tooth will conduct any heat to the stator core back, effectively acting as a heat sink.
3. **Magnetic isolation between phases** – When large currents are flowing in a faulted coil, it could produce large induced voltages on other (healthy) coils or

phases, potentially affecting the motor's performance. The separator tooth acts to magnetically isolate adjacent peaks.

4. **Complete electric isolation between phases** – Electric isolation between the phases is important in the event of a power device or winding failure. For example, in a star point system, if a terminal phase short circuit were to occur in any of the phases, the star point could potentially be raised to dc-link voltage. This would prevent other phases from producing torque (see Figure 6.2). Figure 6.3 shows the improvement where every phase is individually driven by separate H-bridges, similar to SRMs. This way, when a terminal shorted fault takes place, other phases will not be affected, and the system is able to continue operation with limited torque capability.

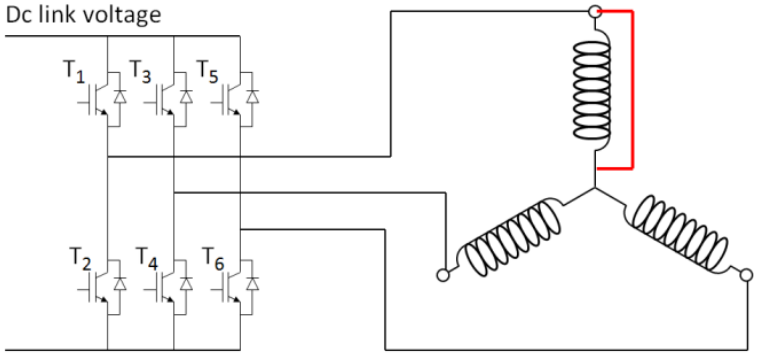


Figure 6.2 – Star point connected with terminal short

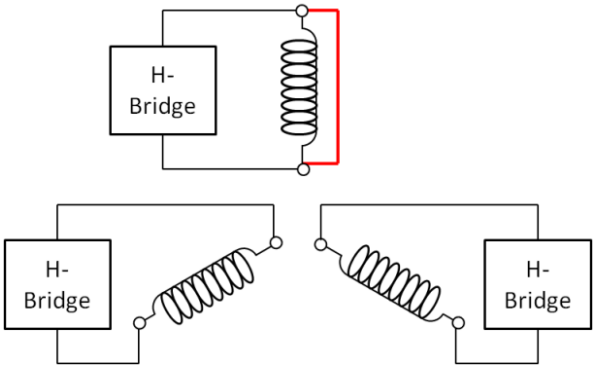


Figure 6.3 – Individual H-bridge connection

5. **Higher number of phases** – In the event of a phase malfunction, the remaining healthy phases should still be able to deliver the rated torque. The phases should therefore be overrated to accommodate such a fault. The formula in equation (6.1) shows how much each phase has to be overrated by; where *n* are the number of phases in the machine, and *F* the overrated percentage. For example,

a three phase machine would require each phase to be overrated by 50%. Furthermore, the authors ignore the braking torque that is created by the faulty phase. This is not always true for all faults or motors, as can be seen later on in Chapter 7 page 120.

$$F = \frac{n}{n-1} \qquad (6.1)$$

6. **1 Per-unit reactance in coils** – In PM machines, the magnets on the rotor cannot be 'switched off' at will. This means that a faulty phase will have a voltage induced by the magnets in post fault operation. The coils in the stator have to be designed to include a d-axis inductance of one per-unit. Should a terminal short circuit occur (Figure 6.4), the faulted current that flows in the coil will be limited to a magnitude of one per-unit. As a result, the coil will not thermally increase and the fault can be accommodated indefinitely. A one per-unit reactance is achieved by using a high number of poles and deep stator slots.

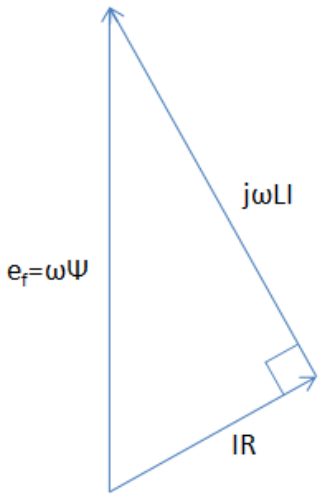


Figure 6.4 – Phasor diagram of a terminal shorted winding

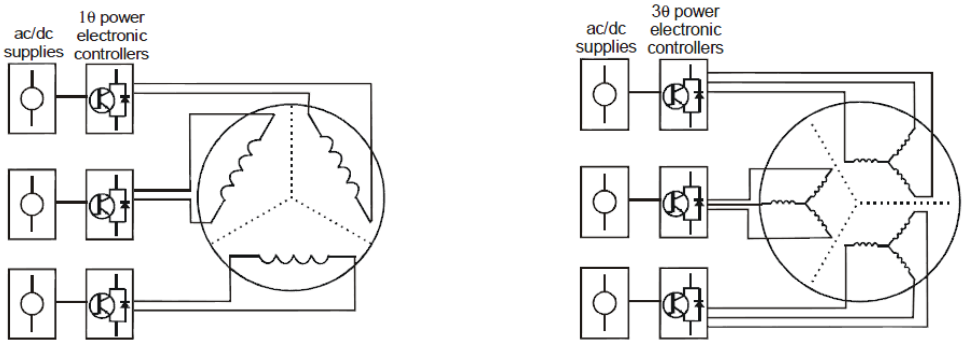
7. **Surface magnet design** – Surface magnets create a higher effective airgap from the coil's point of view than inset magnets. As a result, the coil produces less air-gap flux which links with other coils. The coil cross-inductance is made up primarily from the slot leakage flux and the mutual inductance between coils is reduced.

The authors conclude by proposing a 6 phase system in [50] according to all the points above.

6.3 Variety of fault tolerant PM motors and drives

There is no single type of fault tolerant topology for machines and drives. The applied topologies depend on the application and the system criticality. A factor influencing the preferred topology would depend on the compromise between the number of redundancies, the complexity and cost of the power electronics. For example, the higher the number of redundancies, the more fault-tolerant a system appears to be [28]. However, the cost and complexity of the system increases, as well as the likelihood of a fault occurring [3]. In general, most points introduced in the preceding section by Haylock are incorporated in fault tolerant PM motors. The exceptions are points 4 and 5 which relate to the topology of the system.

Fault tolerant PM motor topologies can typically be categorised in multiphase systems or multilane systems (or a combination of both). A multiphase motor usually consists of a single motor of 3 phases or more, as described by Haylock in point 5 above. A multilane system typically employs multiple three phase motor drive electronics, all operating in parallel. Figure 6.5(a) and Figure 6.5(b) show a multiphase (3 phase), and triple lane (3 phase) topology respectively.



(a) (b)

Figure 6.5 – Different suggested motor configurations for 3-lane systems [9, 51]

6.3.1 *Multiphase topologies*

The higher the number of phases in a multiphase motor, the higher the distribution of electric power. As a result, each inverter leg will carry less current. These inverter legs need to be overrated according to equation (6.1) in the event of a fault. Multiphase motors have the advantage that only one drive is required, although the drive should still conform to the fault tolerant topology [52-54].

Atkinson et al. in [55, 56] designed a fault tolerant PM motor for a main engine aircraft. A 4 phase motor was chosen, where each phase was separately controlled. The motor is of a 3+1 topology, implying that rated torque can still be delivered with only 3 phases

operational. Interestingly, the authors decided to use the aircraft fuel as a coolant of the motor. This way, the electric loading could be increased.

Five phase motors appear to be a popular choice for fault tolerant application, with many papers found in the field [46, 52-54, 57-67]. The motor is able to cope with a loss of two (adjacent) phases or a short circuit fault in one phase [59-62]. During post fault operation, a torque ripple is observed, which is due to the imbalanced forces present in the motor. The torque ripple increases as the number of faulted phases increase. However, Barcaro, Bianchi and Bianchini in [58-62] claim that using a proper control strategy, this torque ripple can be suppressed quite successfully.

6.3.2 *Multilane topologies*

The main advantage of adapting a multilane topology is the ability to retain balanced operation following a fault. If a fault occurs (whether that would be a shorted phase, phase-phase fault or a short circuit of all phases), the controller in the faulted drive can ensure that all phases are short-circuited, resulting in a balanced drag torque. The drag torque will not cause the faulted motor to heat up due to the one per-unit reactance design (point 6, section 6.2). The healthy lane will have to be overrated to be able to supply the rated torque plus additional drag torque the faulted lane produces. Similarly, in the event of an open circuit failure in any of the phases, the drive can open all phases so no (unbalanced) torque will exist [68].

Jie et al. in [68] compare a dual lane 2-phase topology with that of a dual lane 3-phase topology. The authors conclude that the dual lane 2-phase topology has higher average torque capability but the dual lane 3-phase topology has lower VA ratings.

Some papers identify two identical motor drive electronics, with the motors driving the same axis [69]. This is a similar topology as in Figure 1.7 (page 11), except that the phases of the motor are driven by separate H-bridges to ensure electrical isolation between the motor phases.

Bennett et al. in [9] discusses a topology of three separate motor control units consisting of individual H-bridges, that in turn power a 3-phase fault tolerant motor (Figure 6.5a). Bennett explains that this is better than a double lane system, since a majority vote can be introduced if one of these modules fails. With a double lane system, it is more difficult to discover which system is faulty.

Bennett [51] takes this approach further by introducing a 3 lane system that independently drives three 3-phase motors (Figure 6.5b). Although this system is more fault tolerant, it becomes more complex to connect the feedback sensors (resolvers and position sensors) whilst maintaining redundancy over the whole system. More lanes require more components, and thus higher cost.

6.3.3 *Other topologies*

Mitcham in [70] discusses an approach for selecting the pole and slot numbers to reduce the coupling between the phases. The authors energise one phase and track its flux paths to observe how these interfere with other phases. Based on this, a table is produced with various combinations of pole and slot numbers and their relation to the coupling of phases.

Most research relates to radial flux machines although some papers were found to be investigating fault tolerant axial flux machines. The Locment et al. in [71] and [72] presented a fault tolerant 7 phase axial flux motor.

The Bianchi and De Lillo in [73] and [74] suggest a design where four inverter legs are used to power a three phase PM machine. This design adds to the fault tolerance of the IGBT's in the inverter. The additional leg is connected to the star point and controls the zero-sequence current. The authors explain that this inverter is able to continue, even after one of the inverter legs malfunction.

Similarly, Ribeiro et al. in [75] also have an additional inverter leg, but this is connected through thyristors to all three remaining legs. It can effectively be used as a substitute leg if another leg were to fail.

6.3.4 *Literature conclusion*

In general it can be said that the inverter topology depends on the design of the motor. The choice between a full bridge and separate H-bridges is often discussed in the literature. There is a vast amount of fault tolerant drive topologies found in the literature, ranging from axial flux motors to multilayer, multiphase machines. The choice is made depending on the compromise between the level of fault tolerance and the complexity of the system. In general the 5 phase and the dual lane 3 phase motor appear to be the most popular choice.

In 5 phase motors, the torque ripple in post fault operation can cause problems depending on the interface specification. Another disadvantage is the use of non-standard components in drives, and incompatibility with the 3 phase infrastructure.

The dual 3 phase topology on the other hand does not suffer from any torque ripple in post fault operation. Standard components can be used and the system is compatible with the 3 phase infrastructure. The disadvantage is that the components require a higher overrating compared to the 5 phase motor. The complexity may also be greater as two separate units have to communicate to equally share torque.

In conform to the literature, the duplex three phase topology was chosen for the ELGEAR motor. For the landing gear application, a duplex 3 phase motor was preferred over a multiphase motor [76]. This was due to the reasons which were deemed important for this application:

- Good compromise between the level of availability and the drive complexity.
- Three phase system is more compatible with the aircraft power system.
- Triplet harmonics are eliminated from the stator phase voltage (since triplet harmonics cancel out in a 3 phase star point).
- Low torque ripple.

6.4 The fault tolerant ELGEAR motor

In section 1.5.2 the topology of the ELGEAR rig is described. The system consists of a dual lane 3 phase motor drive unit, as shown in Figure 6.6.

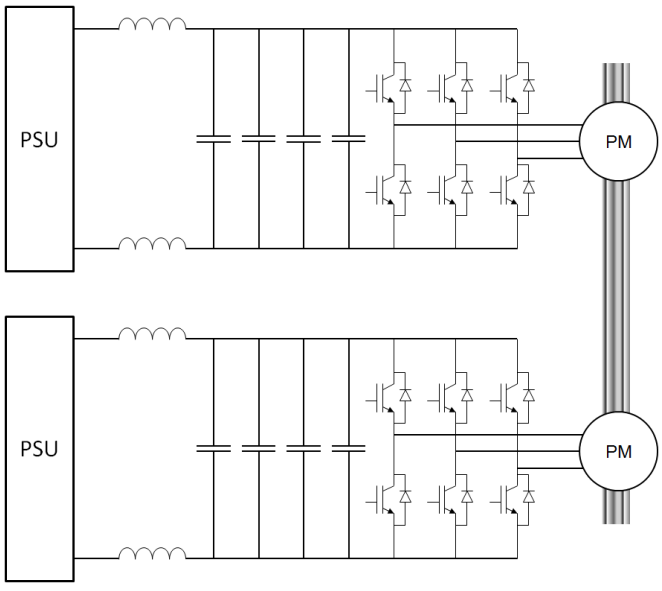


Figure 6.6 – Dual lane 3 phase motor drive unit

The motor chosen is a 24 slot, 20 poles, double three-phase permanent magnet motor and is shown in Figure 6.7 and Figure 6.8. The pictures of the motor can be found in Figure 6.9 and Figure 6.10 respectively.

The motor consists of two electrically separated three phase motors, integrated into one stator. Each phase consists of two coils which are 180° mechanically separated on the stator. For reasons of physical, magnetic and thermal isolation, the coils are wound around their dedicated tooth, with an additional tooth separating the coils. The coils of the two motors are interleaved on to the stator. This makes the connection of the motor more complex as the leads to the coils of each motor must be separated. However, in the event that only one drive is active, a balanced torque will be delivered across the rotor circumference.

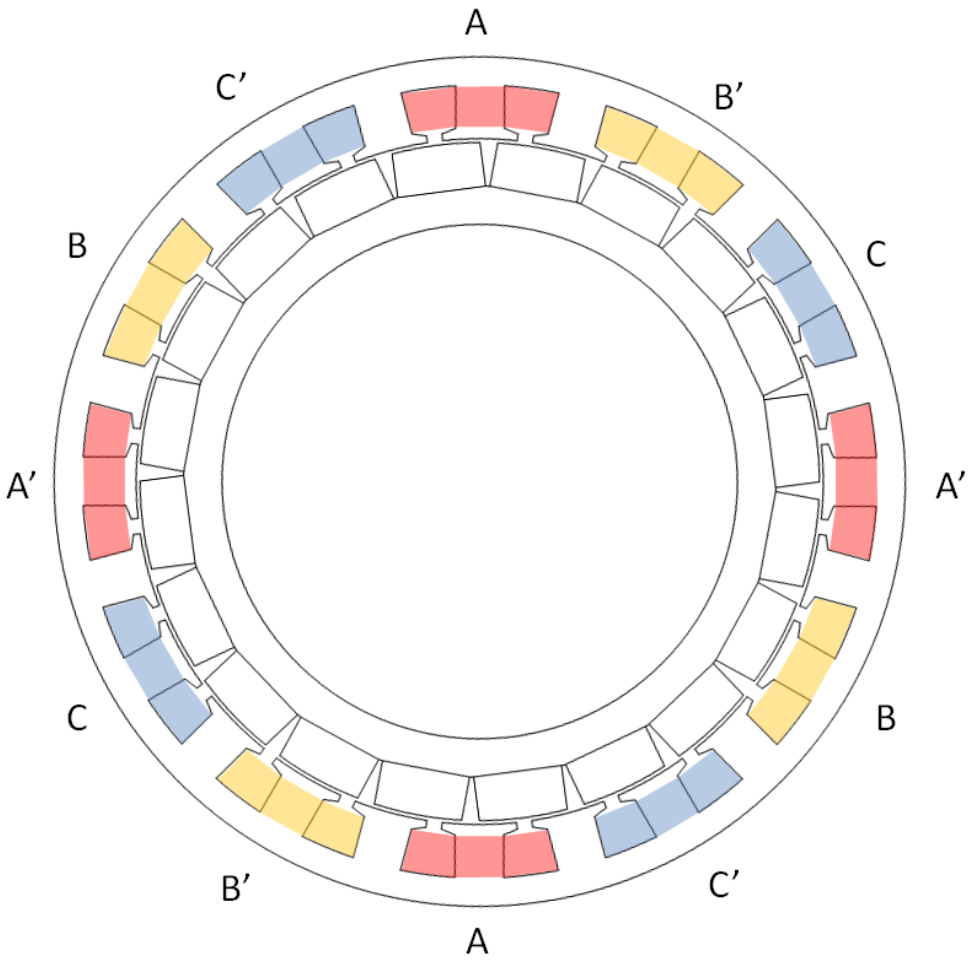


Figure 6.7 – Phase layout on the stator

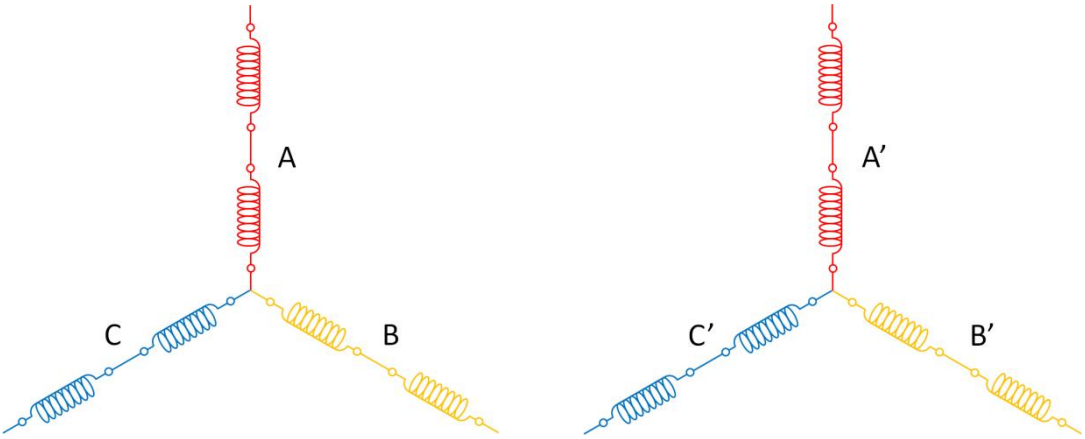


Figure 6.8 – Electrical layout of the phases

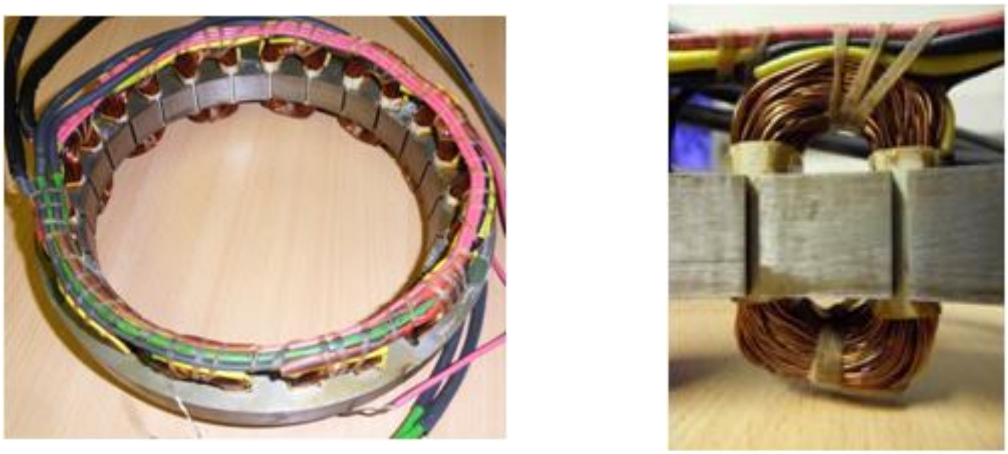


Figure 6.9 – Left, a picture of the ELGEAR stator. Right, a picture of a single coil

Figure 6.10 – Picture of the ELGEAR rotor.

The motors are designed to operate in an active-active configuration. During nominal operation the motors share the torque equally. The separate drives communicate with a dedicated cross communication link to ensure the torque is equally shared and the load resonance between the motors are minimised. If the cross communication link is not in place, one motor will end up taking the full load while the other motor will see that the demanded torque is reached without supplying any current to the phases.

The rotor consists of surface mounted magnets to ensure a high proportion of cross-slot leakage flux. The diameter of the rotor is large to allow a large number of poles (to achieve one per-unit reactance). As a result, there is a large space in the centre of the motor which is used by the gearbox.

The ELGEAR motor parameters are outlined in Table 6.1. The motor's physical characteristics are outlined in Table 6.2.

Parameter	**Value**	**Unit**
Rated speed	900	rpm
Number of poles	20	
Turns per coil	211	
Coils per phase	2	
Coil Resistance	1.60	Ω
Coil Inductance	7.00	mH

Table 6.1 – ELGEAR motor parameters

Parameter	Value	Unit
Number of stator slots	24	
Stator outside diameter	230.0	mm
Stator bore diameter	178.0	mm
Magnet thickness	7.0	mm
Magnet remnant flux density (@20 °C)	1.07	T
Magnet coercive force (@20 °C)	800	kA/m
Magnet maximum operating temperature	350	°C
Stator tooth width	14.5	mm
Slot depth from slot bottom to tooth stator bore	18.0	mm
Stator slot opening width	3.0	mm
Stator teeth tip thickness at opening	2.0	mm
Total air gap length	1.0	mm
Mechanical clearance	0.5	mm
Stack length	20.0	mm
Number of strands per turn	1	
Copper bare diameter	0.61	mm
Conductor area	0.292	mm^2
Lamination thickness	0.35	mm

Table 6.2 – Design characteristics of the ELGEAR motor

Each motor is overrated by 135%. This is to compensate for the missing motor (100% overrating) plus the maximum drag torque caused by the faulty motor (35%). The drag torque is covered in section 7.2.4, page 125.

6.5 Possible faults on the PM motor

This section provides a summary of the possible faults that could occur on the PM motor. The faults covered will only apply to the dual 3 phase topology. Some faults are more likely to occur whilst others may be more severe [77].

6.5.1 *Winding open circuit fault*

A winding open circuit fault implies that one of the coils is disconnected resulting in the loss of a phase (Figure 6.11). An open circuit fault could arise due to the stresses in a

coil or (more commonly) improper soldering connection at the terminal of the coil. This fault could also occur on the inverter side, when a transistor fails open circuit.

As a consequence, an imbalanced torque will be delivered to the rotor, causing an increased torque ripple output.

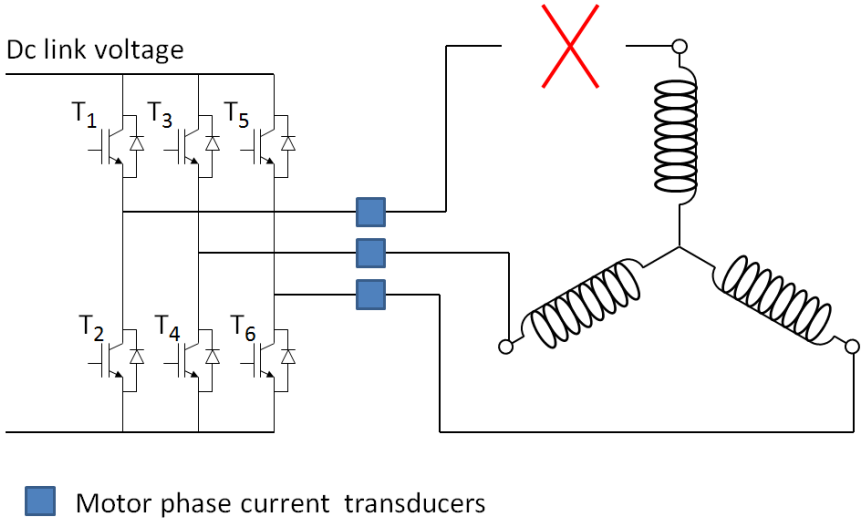


Figure 6.11 – Winding open circuit fault

The failure is typically detected using the motor phase current transducers. Continuous or discontinuous zero current will be measured in one phase, providing an indication to the controller that this fault occurred.

The remedial action would be to disconnect the motor by opening all the transistors in the inverter. This ensures that the faulty motor will be out of operation and will not produce any unbalanced torque. The healthy lane motor drive unit will take over operation and provide the demanded torque.

6.5.2 *Phase terminal short circuit fault*

The phase terminal short circuit fault is where two ends of the same coil or phase are electrically connected (Figure 6.12). This fault is more common in topologies where phases are driven by separate H-bridges since transistor failures could result in a phase terminal short circuit. In star connected systems this fault could occur in places where connection wires of phases or coils overlap. When the insulation of these wires degrades, an electrical connection may be the consequence.

As a result, the motor will have difficulty in providing any useful torque as the star point is connected to $+V_{dc}$ or $-V_{dc}$ depending on the inverter switches T_1 and T_2. The

magnets will induce a voltage in the faulted coil, and an imbalanced drag torque will result. The short circuit current in the faulted phase will be limited to one per-unit due to the reactance of the coil.

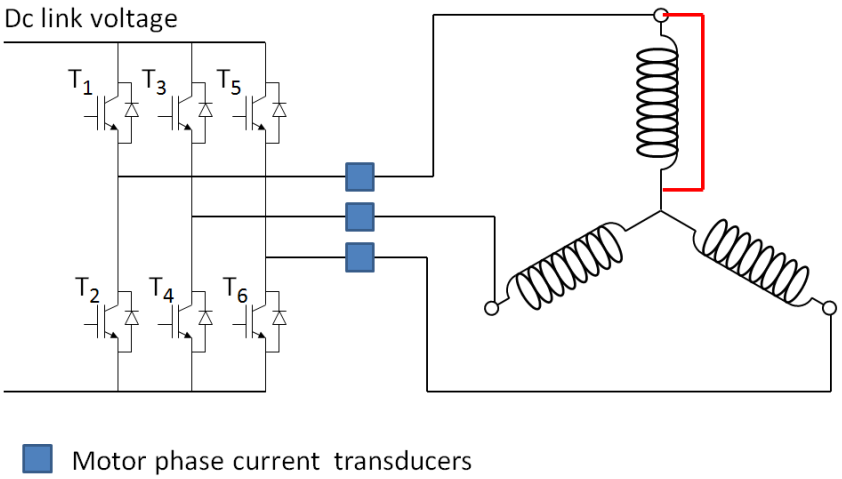


Figure 6.12 – Terminal short circuit fault

The failure is typically detected using the motor phase current transducers. The controller will detect excessive currents and reduced torque in a dual lane system.

The remedial action would be to apply a three phase terminal short circuit so a balanced drag torque will be produced by the faulted motor. The healthy lane will take over the demanded torque and compensate for the additional drag torque created by the faulty motor.

This fault is not considered very likely since care is usually taken to separate the connection wires, ensuring they do not overlap.

6.5.3 *Phase-phase terminal fault*

A phase to phase terminal short is very similar to the single phase terminal short. The fault occurs when the terminal of one phase connects to the terminal of another phase (Figure 6.13). In multiphase machines this is considered a more serious fault as two phases are taken out of operation. The fault could occur on the machine side at places where connection wires of phases overlap, or on the drive when a transistor short circuit takes place.

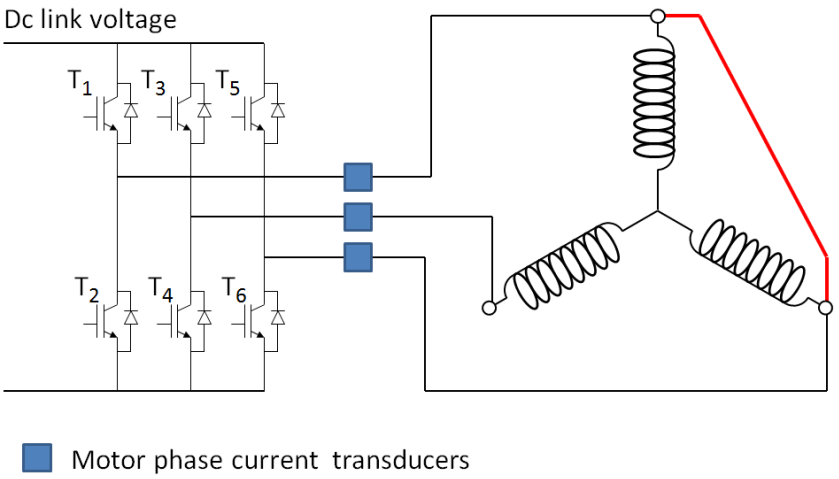


Figure 6.13 – Phase-phase short

Consequently, the faulted phases will carry rated current. The failure is typically detected on the motor phase current transducers, as short circuit currents will flow through two transducers.

Remedial action would be to short circuit all phases, thus creating a balanced drag torque. The healthy lane will take over the demanded torque of the system and compensate for the additional drag torque.

6.5.4 *Inter-turn, phase-phase fault*

This fault is described as a phase-phase fault where turns from one phase are electrically connected to turns from another phase (Figure 6.14). This fault would typically occur in the machine side, where windings of different phases share the same slot. In a fault tolerant motor, where the phases are physically isolated, the chance of this fault occurring is negligible.

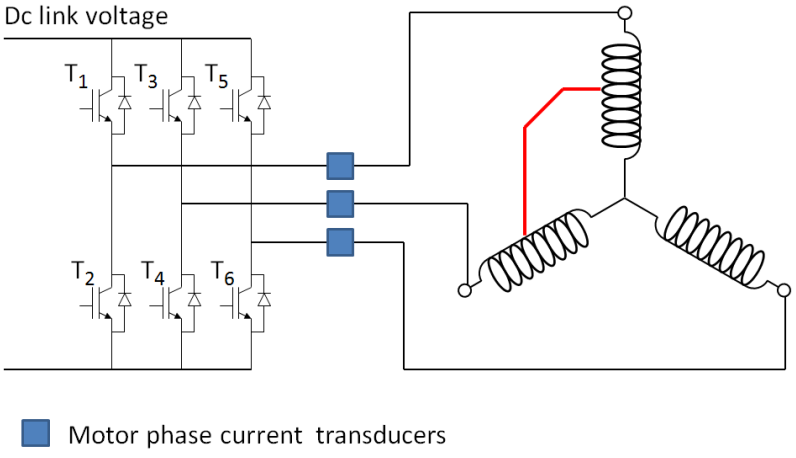


Figure 6.14 – Phase-phase fault

6.5.5 *Phase-ground fault*

A phase-ground fault is where a connection is made between the phase and the ground. This fault may arise as an insulation break down between a coil and the iron core back, which is usually grounded.

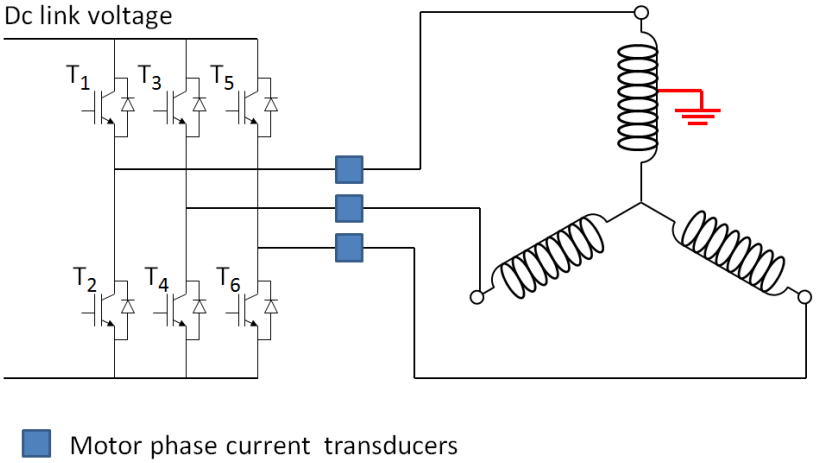


Figure 6.15 – Phase-ground fault

As a result, an imbalanced torque will be exerted on the rotor. The fault is detected using the current transducers since the sum of the currents will not add up to zero (imbalanced currents).

The remedial action would be to disconnect the motor by opening the transistors in the inverter. The faulty motor will not produce any drag torque, and the healthy lane will take over the system.

6.5.6 *Turn-turn faults*

One of the more severe faults is the turn-turn fault. In the literature, this is also known as an inter-turn fault. A turn-turn fault is a short circuit connection between two adjacent turns within a coil (Figure 6.16). The fault usually short circuits a single turn, but a short circuit of multiple turns is not excluded. This fault occurs in a coil as a result of the degradation of insulation.

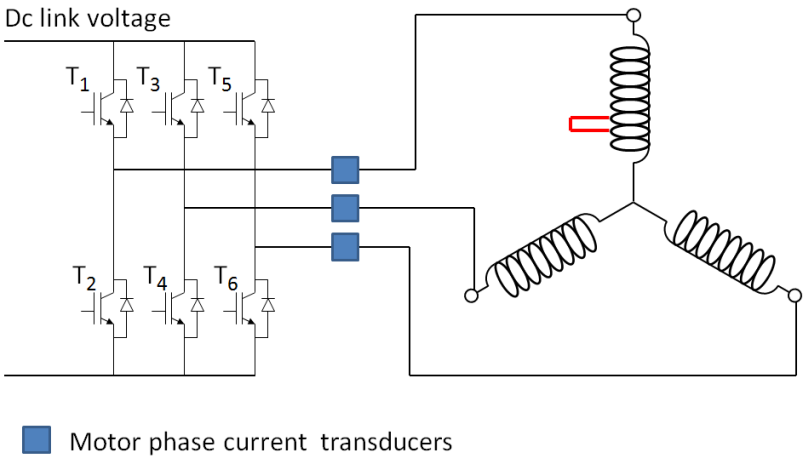


Figure 6.16 – Turn-turn fault

A winding with a single shorted turn can be described as two electrically separated coils (Figure 6.17 and its electrical equivalent in Figure 6.18). Since both coils are still wound around the same tooth, they are magnetically coupled. One coil represents the single shorted turn, the other represents the remaining healthy turns consisting of $N - 1$ turns.

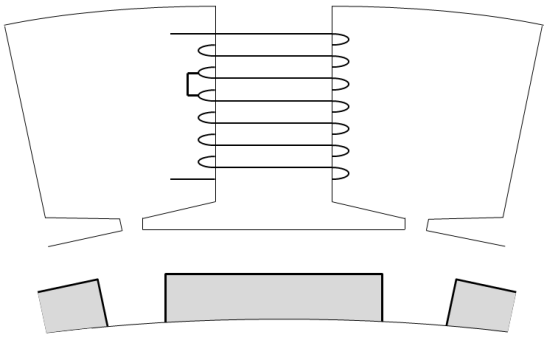


Figure 6.17 – Turn-turn short

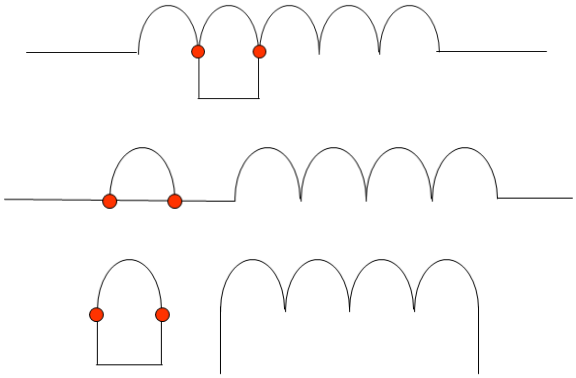


Figure 6.18 – Turn-turn short equivalent circuits

The fault is difficult to pick up since the phase currents only change by fraction of a percentage. The fault does not appear to be severe at first since the motor continues its normal operation. The faulted current will locally circulate in the shorted turn, where its magnitude depends on how many turns are shorted. Typically the faulted current will be several times the wire's rating, causing the turn to heat up rapidly. If remedial action is not taken quickly, the fault could propagate to other sections of the coil, further damaging the machine.

There are a number of ways of detecting the fault, some of them more successful than others, but it remains a difficult problem. From the outside, a coil of N-1 turns can be seen. The drop from N to N-1 is often unnoticeable for motors with high number of turns, but should theoretically result in a difference in current as the inductance is slightly reduced.

Haylock [28] implemented a lookup table where the flux linkage is measured with respect to the current and the rotor angle when the motor is healthy. This table – also known as the ψ, i, θ characteristic – is used by the current controller in conjunction with the PWM demand. This way, the controller knows the exact current value that is expected at the end of each PWM cycle. A deviation from the value of the lookup table therefore means a fault has occurred. Haylock states that the detection is very sensitive indeed, since it still relies on detecting a reduction in inductance. Moreover, the reduction in inductance also depends on the coupling between the shorted turn and the remaining turns, PWM strategy and frequency. Logically faults in larger motors with less turns are easier to detect, since a reduction in one turn is more significant.

When such a fault is detected, the remedial action is to short circuit the entire coil. In a star connected system, all 3 terminals are shorted. Since the shorted turn is closely coupled with the remainder of the coil, the faulted current is equally distributed across all turns. The resulting faulted current will be one per-unit in magnitude.

The faulty motor will produce a balanced drag torque, and the healthy lane will take over.

6.6 Conclusion

This chapter showed the development of the fault tolerant motor, and reviewed existing fault tolerant drive topologies in the literature. Depending on the application, the dual lane 3 phase motor and the 5 phase multiphase motor are the most popular designs in the literature. Various faults associated with the motor were covered, ranging from rare and benign faults to more likely and severe faults.

The single shorted turn fault was highlighted to be the most problematic of all. It is difficult to detect, and propagates very quickly when remedial action is not applied. It is therefore important to investigate the effects and consequences of such a fault upon the ELGEAR motor. In the following chapters the turn-turn fault will be covered in more

detail. Finally, the fault will be induced upon the ELGEAR motor to verify the predicted results.

Terminal and Turn-Turn Fault Analysis

Chapter 7

7.1 Introduction

This chapter will focus on the theory related to the turn-turn fault on a duplex fault tolerant PM motor. The terminal fault will also be discussed since it is mathematically very similar to the turn-turn fault. In the event of a fault, it is assumed that the healthy lane of the motor will provide the demanded torque for the system, whereas the faulted drive will focus on suppressing or minimising the drag torque or thermal instability.

7.2 Terminal short circuits

7.2.1 *Types of terminal short circuits*

In a three phase system, there are three types of terminal faults that can occur:

- The single phase terminal short (Figure 6.12, page 114). The details of this fault are described in the preceding chapter.
- The phase-phase terminal short. This fault arises when the terminals of one phase of a coil short circuit with that of another, as shown in Figure 6.13, page 115. The fault can also occur in the drive side when two transistors are shorted as shown in Figure 7.1. The failure of two transistors may occur when one transistor is failed short circuit, and the other is switched as part of the nominal control algorithm. This failure could also be purposely implemented as part of a remedial action strategy to suppress other failures in the machine.
- The 3 phase terminal short is where the terminals of all coils are connected (Figure 7.2). This configuration may occur naturally as part of the control algorithm in the drive during the zero voltage state, where all top or bottom transistors are switched on as part of the PWM control modulation. The zero voltage state was covered as part of the ‘dc-link monitoring project’ section 3.3.3 page 41. However, the 3 phase terminal short can also be purposely implemented by the inverter to suppress other faults in a similar manner to the phase-phase terminal short.

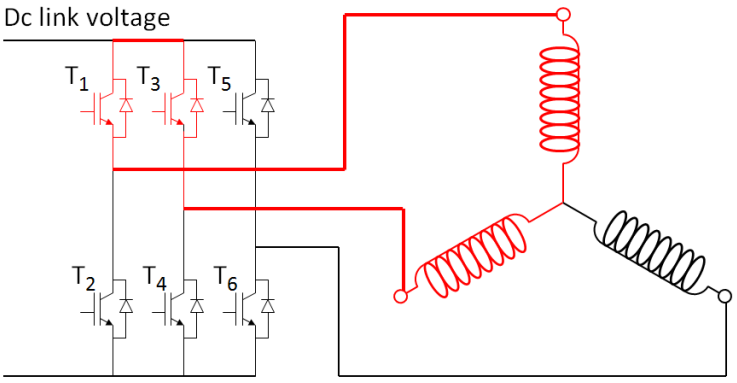


Figure 7.1 – Phase-phase short

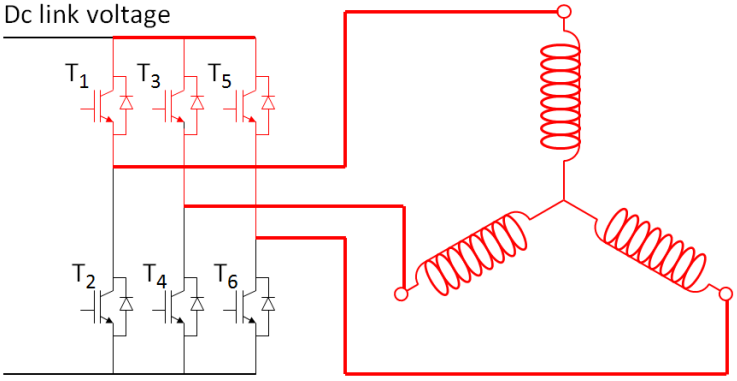


Figure 7.2 – 3 Phase terminal short

7.2.2 *Remedial action*

The phase-phase terminal and 3 phase terminal short can be applied as remedial action to some of the faults described in section 6.5.

In both cases, the healthy lane of the motor will take over control and supply the demanded torque. Since permanent magnets cannot be 'turned off' at will, the magnets will continue to induce an EMF in the faulted phases. The faulted current that flows in the winding as a result will predominantly be limited by the reactance of the coil. Hence, the faulted current is almost 90° out of phase with the EMF. The faulty motor will also produce a drag torque as a result of the faulted current.

A phase-phase short will result in a drag torque that is less than the drag torque produced by the 3 phase terminal short. However, the phase-phase drag torque will be an unbalanced torque. The 3 phase terminal short circuit will create a uniform drag torque, but will be greater in magnitude. For the 3 phase terminal short, detecting the exact location is not important as all phases are shorted.

The 3 phase terminal short is generally the preferred option for remedial action since it is simpler to implement and has better post fault performance.

7.2.3 *Mathematical analysis*

A mathematical analysis is presented to explain the terminal short in more detail. Figure 7.3 shows a cross sectional diagram of one of the coils in a PM motor. The rotating magnets on the rotor cause an approximate sinusoidal flux to be flowing in the stator teeth, described by equation (7.1). As a result, a sinusoidal EMF will be induced in the coil described by equation (7.2).

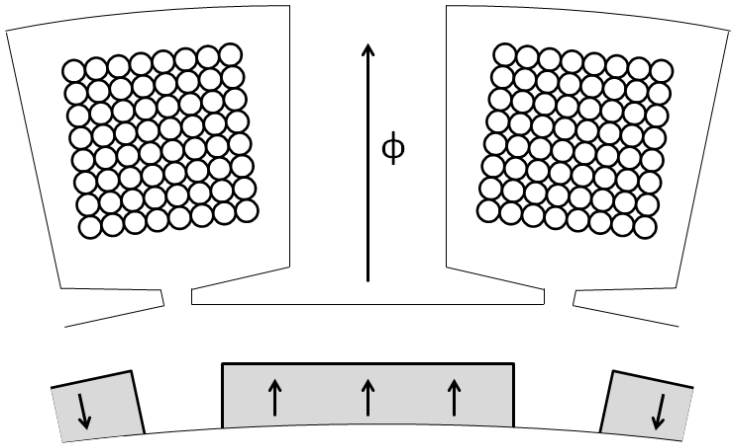


Figure 7.3 – Cross section, one coil

$$\phi = \hat{\phi}\sin(\omega t) \qquad (7.1)$$

$$\left(\frac{d\phi}{dt} = \hat{\phi}\omega\cos(\omega t)\right)$$

$$e_f = N\frac{d\phi}{dt} = \omega N\hat{\phi}\cos(\omega t) \qquad (7.2)$$

$$|e_f| = \omega N\hat{\phi} \qquad (7.3)$$

Where:

ϕ	Magnet flux linking the coil
ω	Electrical frequency
N	Number of turns in the coil
e_f	Induced EMF

The equivalent electrical circuit is shown in Figure 7.4, where the coil is represented by its resistance and inductance. The electric circuit is described in equation (7.4).

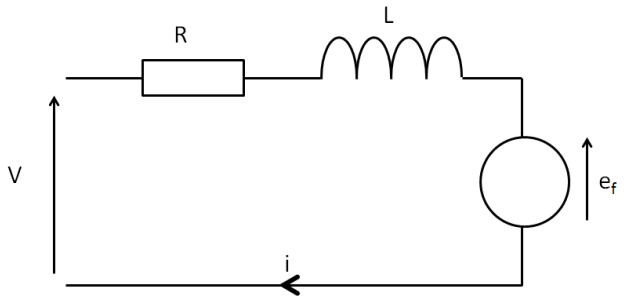


Figure 7.4 – Electrical equivalent diagram, one coil

$$V = iR + j\omega L + e_f \tag{7.4}$$

When a terminal short circuit is now applied across the coil, a faulted current will flow which is limited by the coil's resistance and inductance. In fault tolerant motors, the magnitude of current is < 1 pu, due to the reactance of the coil.

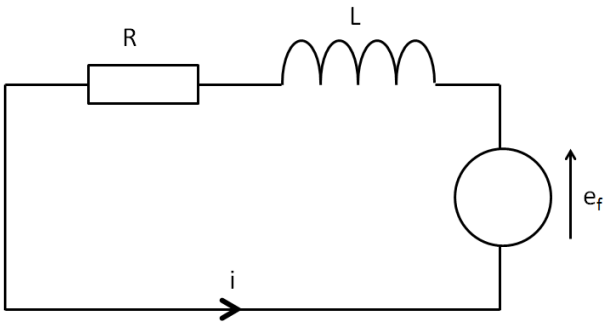


Figure 7.5 – Terminal shorted electrical equivalent diagram

Hence, the fault current is described in equation (7.5):

$$e_f = i(R + X_L)$$

$$e_f = i(R + j\omega L)$$

$$i = \frac{e_f}{R + j\omega L}$$

$$i = \frac{\omega N \hat{\phi} \cos(\omega t)}{R + j\omega L} \tag{7.5}$$

Equation (7.5) shows that the faulted current varies with ω since a higher rotor speed will induce a higher voltage in the windings. At lower speeds, the assumption can be made that the reactance of the coil is significantly lower than the resistance. The current

is therefore described by equation (7.6). At higher speeds, the opposite is true, and the reactance dominates as seen in equation (7.7).

Low ω

$$\omega << \frac{R}{L} \quad \rightarrow \quad \omega L << R$$

$$|i| \approx \frac{N\hat{\phi}}{R}\omega \qquad (7.6)$$

High ω

$$\omega >> \frac{R}{L} \quad \rightarrow \quad \omega L >> R$$

$$|i| \approx \frac{\omega N\hat{\phi}}{\omega L} = \frac{N\hat{\phi}}{L} \qquad (7.7)$$

At lower speeds, the faulted current is proportional to the rotor speed. At higher speeds, the faulted current is limited by the inductance of the coil, as its magnitude tends towards $\frac{N\hat{\phi}}{L}$.

Equation (7.5) is plotted in Figure 7.6 for the ELGEAR motor showing this relationship.

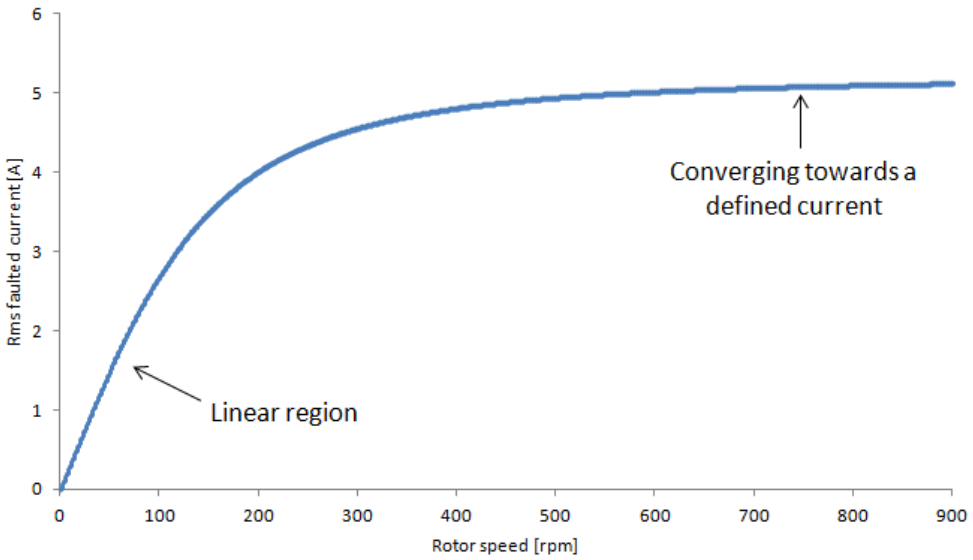


Figure 7.6 – Faulted current vs speed (terminal short circuit)

Haylock [28] stated that the coils should be designed to have 1 pu reactance, as to limit the faulted current to 1 pu. This essentially means that the motor is able to run indefinitely without the coil heating up. In practice there is an influence of drag torque and the per-unit current rating should therefore be higher than the terminal shorted current, as explained in the following two sections.

7.2.4 *Drag Torque*

When the machine is operating with a terminal fault condition, the fault will cause a drag torque. The healthy lane of the motor will have to supply twice the nominal torque (overcoming the lost drive) plus the additional drag torque created by the lost drive.

The power lost in the faulted winding is i^2R, which is a function of the fault current and the resistance of the coil [76].

Power lost in winding: $P = i^2 R$

From equation (7.5): $i^2 = \left(\frac{\omega N \hat{\phi} \cos(\omega t)}{R + j\omega L} \right)^2$

$$P = \left(\frac{\omega N \hat{\phi} \cos(\omega t)}{R + j\omega L} \right)^2 R$$

Drag Torque: $T_{drag} = \frac{P}{\omega} = \left(\frac{\omega N \hat{\phi} \cos(\omega t)}{R + j\omega L} \right)^2 \frac{R}{\omega}$

$$T_{drag} = \left(\frac{N \hat{\phi} \cos(\omega t)}{R + j\omega L} \right)^2 \omega R \qquad (7.8)$$

Figure 7.7 shows the plotted graph of equation (7.8) for the ELGEAR motor. The vertical axis shows the drag torque on a per-unit scale, where 1 pu is the nominal torque delivered. The maximum drag torque exists at low speeds, with a magnitude of 35% of the nominal torque.

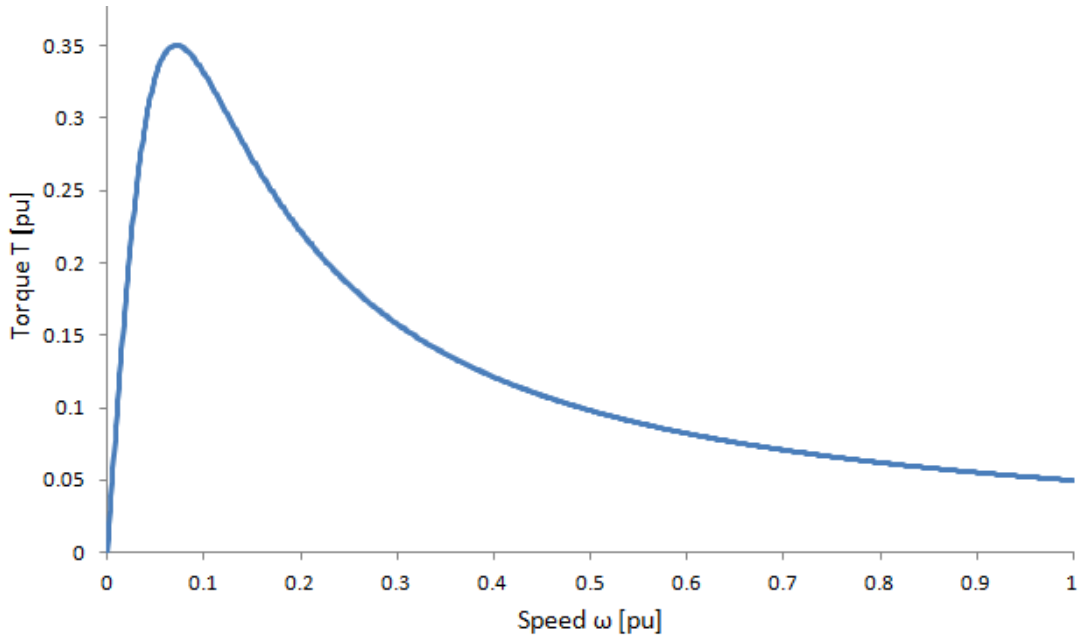


Figure 7.7 – Drag torque vs Speed

7.2.5 *Definition of rated current*

Figure 7.8 shows all the possible scenarios of torque sharing in a dual lane fault tolerant PM motor. In a healthy active-active configuration, each lane will supply half the load torque – see Figure 7.8(a). When one motor is disconnected due to open circuit faults on the motor, Figure 7.8(b) applies. The healthy motor will now supply the full load torque. At this point, the motor has to be overrated by 100%, relative to its normal operating condition. When one motor is 3 phase terminal short circuited, Figure 7.8(c) applies. The healthy motor now has to supply the full load torque plus compensate for the additional drag torque the faulted motor produces. In order to supply the load torque at all speeds, each motor should therefore be overrated by 135%.

The manufacturer's engineering report in [76] states that a peak phase current of 11 A is required for the ELGEAR motor to achieve an overrating of 135%. The 11 A peak is analogous to one per-unit current. At first this current appears to be high, considering the wires in the motor coil have a diameter of 0.654 mm giving an approximate current density of 23 A mm^{-2}. This is quite significant considering most wires have rated currents of around 8 A mm^{-2}. In transformers were coils are densely packed and poorly cooled, the rating may even drop to 2 A mm^{-2} due to the difficulty of cooling inner turns [78].

The high current density, 23 A mm^{-2}, is permitted due to the limited operational time of the machine. Goodrich subjected the motor to various load cycles according to the

specification. Using a thermal simulation model, it was reported that the motor operating at rated torque could only do so for 20 minutes maximum until the thermal limit is achieved. This was in accordance of the specification since there are long off-periods in between operation. [76]

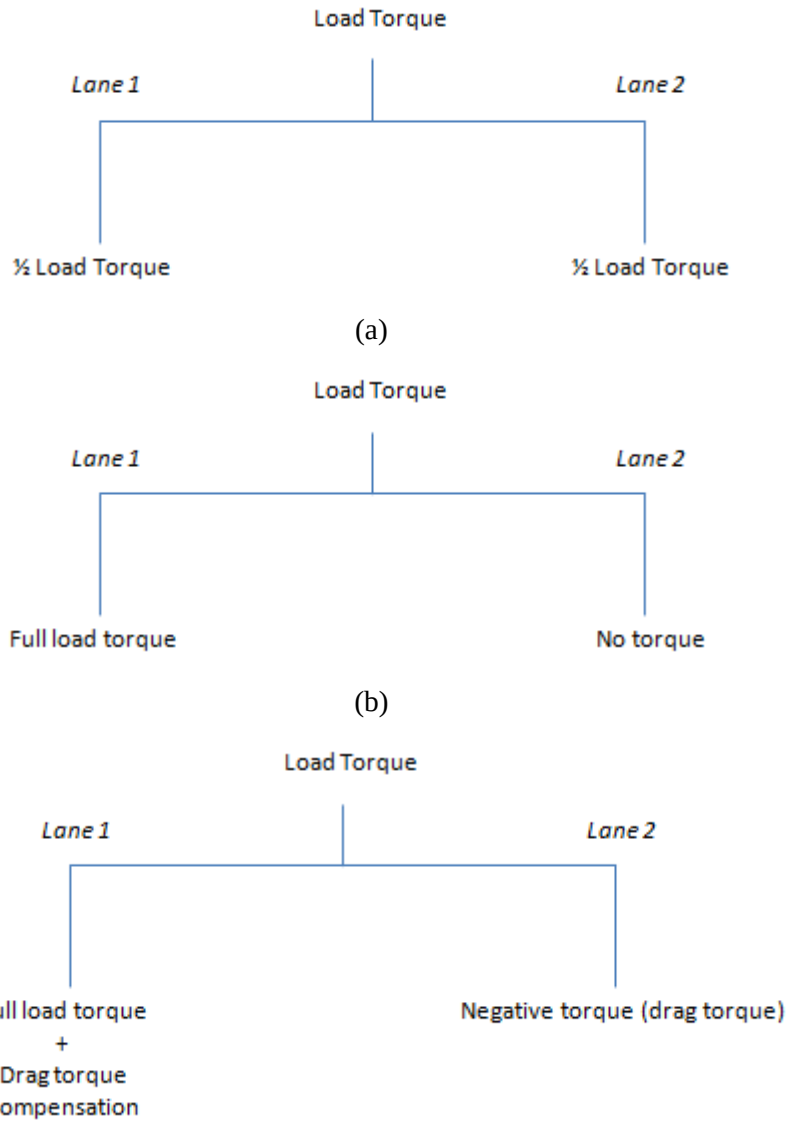


Figure 7.8 – Various torque sharing scenarios of both a dual lane

7.3 Turn-turn faults

As discussed in the literature, the turn-turn fault is a more worrying fault. Moreover, a turn-turn fault is much more likely to occur than a terminal fault due to the physical layout of the turns in a winding. In the worst case, a turn-turn fault causes the wire in a coil to heat up beyond its thermal rated value in a matter of milliseconds. The result is that the fault is able to propagate to other regions of the coil.

7.3.1 *Causes of turn-turn faults*

In order to achieve a high fill factor, turns are wound closely in the stator slot. As a result of long term exposure to mechanical vibration and temperature stresses, the insulation may gradually break down. Insulation break down is generally considered one of the more common causes of motor failure in brushless machines [28, 79, 80]. Consequently adjacent conductors may electrically connect, causing a shorted coil of *M* turns within a coil of *N* turns as Figure 7.9 depicts. The severity of the fault worsens as the value of *M* decreases.

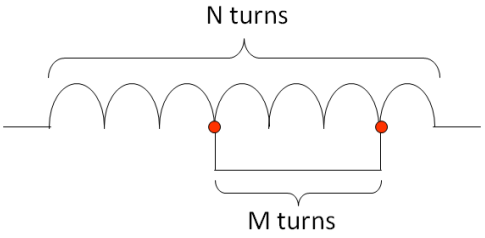


Figure 7.9 – Shorted coil of M turns within a winding of N turns

Due to the nature of how a coil is wound, a short circuit of adjacent conductors will most likely result in a single shorted turn (i.e. M = 1 turn). It is also possible for an entire layer to be shorted out as a result of two adjacent wires conducting.

An example is given in Figure 7.10 for a coil of 20 turns (N = 20 turns). In the first scenario a fault occurs between two adjacent conductors shorting one turn, known as a single shorted turn (Figure 7.10, red connection, M = 1 turn). In the second scenario the fault of two adjacent conductors short out a whole layer (Figure 7.10, blue connection, M = 7 turns).

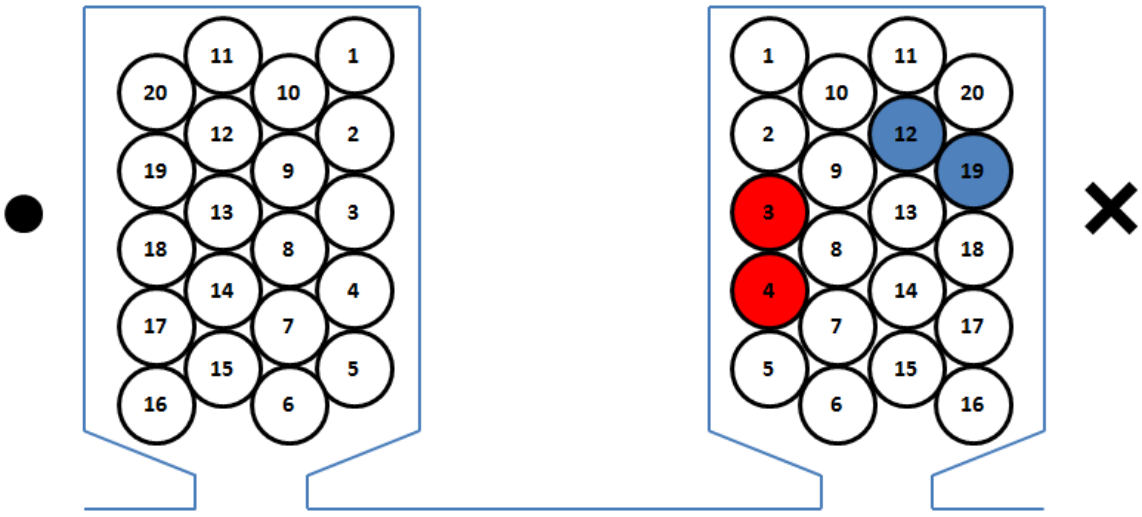


Figure 7.10 – Two scenarios of adjacent winding shorts

The number of turns shorted depends on the position of the turn, ranging from 1 turn to (2r – 1) turns, where *r* is equal to the amount of conductors that can be placed along the stator tooth (in the example given, r = 5). Other shorted turns are also possible, since coils are not wound as precisely as in the diagram. Connections between turns 6 and 16 are also possible, as are turns that overlap elsewhere (e.g. in the end winding region).

In general, the single shorted turn is the most likely fault to occur. Table 7.1 shows an analytical example based on Figure 7.10 of all the possible fault scenarios that may occur due to two shorting adjacent conductors.

Number of shorted turns	**Possibilities**	**Likelihood of happening**
1 (single shorted)	19	44%
2	3	7%
3	3	7%
4	3	7%
5	3	7%
6	3	7%
7	3	7%
8	3	7%
9	3	7%

Table 7.1 –Turn-turn fault possibilities

7.3.2 *The single shorted turn*

The worst type of turn-turn fault is the single shorted turn. The voltage induced in the turn by the magnets produce a current that flows in the turn which is limited by the turn's resistance and inductance. Since inductance is proportional to the square of the number of turns, the inductance of one turn becomes insignificant. The faulted current is therefore predominantly limited by its resistance – which is small – resulting in a faulted current well beyond its rated value.

The analysis of a turn-turn fault is very similar to that of the terminal fault. In Figure 7.11 and Figure 7.12, both electrical equivalents of the fault are compared.

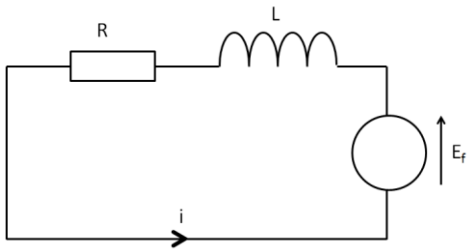


Figure 7.11 – Terminal fault, electrical equivalent

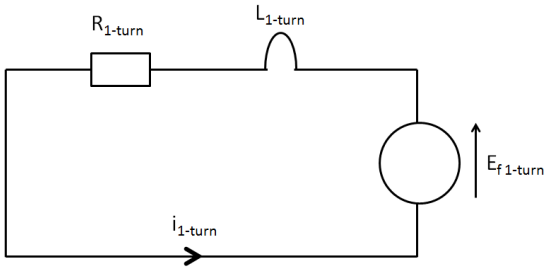


Figure 7.12 – Turn-turn fault electrical equivalent

Where:

$e_{f\ 1turn}$	The EMF induced in one turn:	$e_f = N \times e_{f\ 1turn}$
L_{1turn}	Inductance of one turn:	$L = N^2 \times L_{1\ turn}$
R_{1turn}	Resistance of one turn:	$R = N \times R_{1\ turn}$

The equivalent circuit of the terminal fault is quoted from equation (7.5):

$$i = \frac{e_f}{R + j\omega L} = \frac{\omega N \hat{\phi} \cos(\omega t)}{R + j\omega L}$$

From this equation and Figure 7.12, the equivalent electrical model for the single shorted turn is produced (assuming the coil terminals are open-circuit).

$$i_{1turn} = \frac{e_{1turn}}{R_{1turn} + j\omega L_{1turn}} = \frac{\omega \hat{\phi} \cos(\omega t)}{R_{1turn} + j\omega L_{1turn}} \qquad (7.9)$$

The equation is scaled down to a single shorted turn by substituting the variables of E_{1turn}, L_{1turn} and R_{1turn}.

Since:

$$R = N \times R_{1turn}$$
$$L = N^2 \times L_{1turn}$$

$$i_{1turn} = \frac{\omega \hat{\phi} \cos(\omega t)}{\frac{R}{N} + j\frac{\omega L}{N^2}}$$

And hence:

$$i_{1turn} = \frac{\omega N \hat{\phi} \cos(\omega t)}{R + j\frac{\omega L}{N}} \qquad (7.10)$$

7.3.3 *Severity of the single shorted turn*

The single shorted turn equation is analysed for low and high speeds:

Low ω

$$\omega << \frac{R}{L} \quad \rightarrow \quad \omega L << R$$

$$|i_{1turn}| \approx \frac{N\hat{\phi}}{R}\omega \qquad (7.11)$$

High ω

$$\omega >> \frac{R}{L} \quad \rightarrow \quad \omega L >> R$$

$$|i_{1turn}| \approx \frac{\omega N\hat{\phi}}{\frac{\omega L}{N}} = \frac{N^2\hat{\phi}}{L} \qquad (7.12)$$

At low speeds, the current of the single shorted turn is proportional to ω. This is similar to the faulted turn current of the terminal shorted turn – compare equations (7.6) and (7.11).

At higher speeds, the similarities end. The single shorted turn current converges to $\frac{N^2\hat{\phi}}{L}$, which is a factor of *N* higher than the terminal shorted turn current – compare equations (7.7) and (7.12). Although the single shorted turn current appears to converge to $\frac{N^2\hat{\phi}}{L}$, in reality the turn resistance tends to dominate throughout. For the range up to rated speed, the single shorted turn continuously increases proportionally to the speed, and therefore only equation (7.11) applies. Both equations are plotted in Figure 7.13 below.

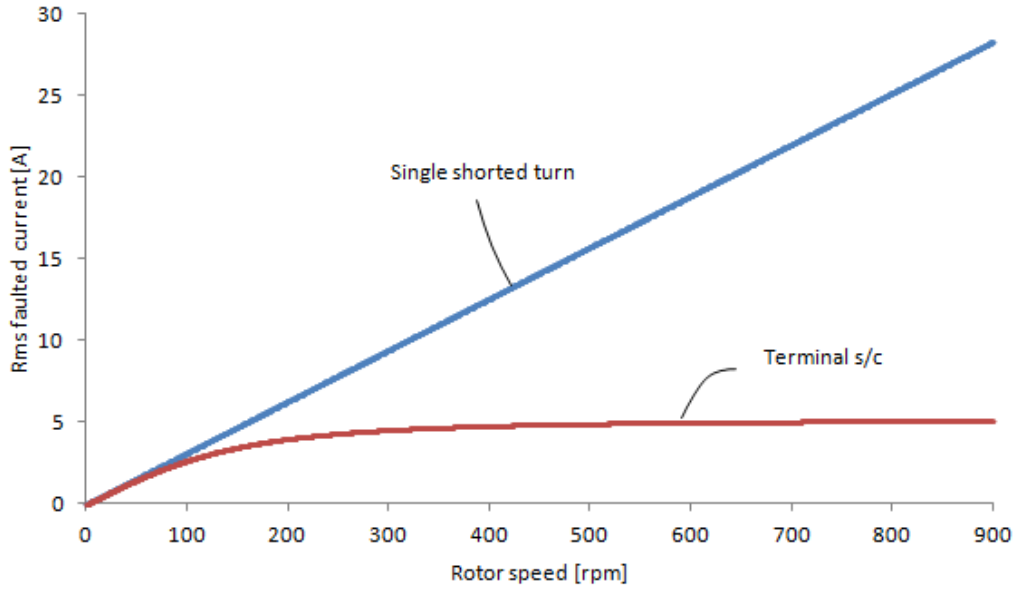


Figure 7.13 – Terminal fault vs single shorted turn

At rated speed, the single shorted turn current has a magnitude of 28 A rms, which is 3.6 times the rated current.

7.3.4 *Consequences of shorted turn faults*

The faulted current is significantly higher than the rated current. As a result, the temperature gradient will be large, causing the turn to heat up quickly. If action is not taken quickly, the fault may propagate to other parts of the coil or motor.

The faulted current will only flow inside the faulted turn. From the outside, a shorted turn will be difficult to pick up since the property of the coil is almost unchanged (N is reduced from 211 to 210 turns). This is especially true for motors with a large number of turns, where the percentage of one turn compared to the total number of turns is low.

7.4 Resistance of coils

Earlier it was found that the single shorted turn is limited by the resistance which was assumed to be $R_{turn} = \frac{R_{coil}}{N}$. This value is the average resistance of a turn and does not apply to the turns individually. The position of the turn within the slot determines the turn's end winding length and therefore its resistance.

In the ELGEAR motor, the tooth width is relatively large compared to the stack length. Figure 7.14 shows the side view of a stator coil. As a result, there is more wire in the end winding than in the stator. In the case of the ELGEAR motor, 73% of the coil is present in the end winding, and only 27% in the stack length.

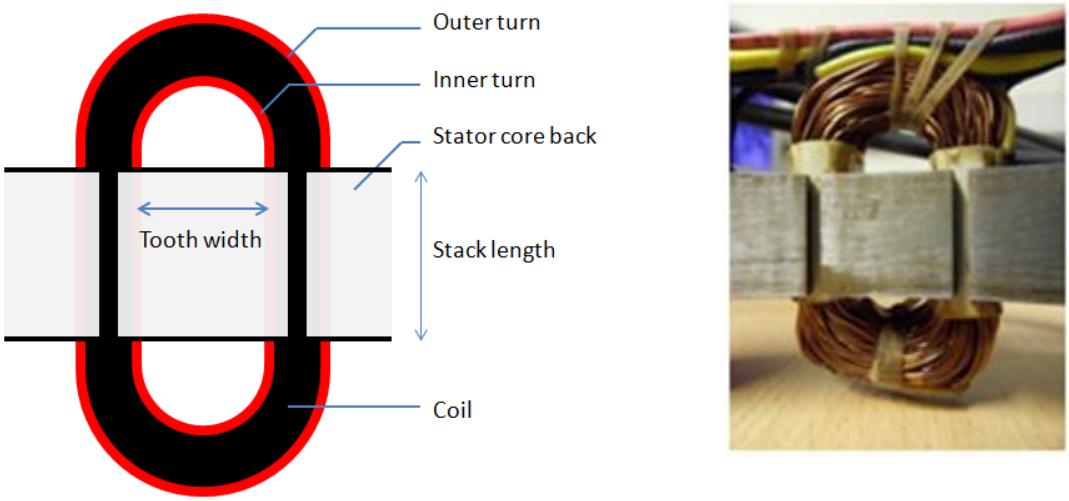


Figure 7.14 – Stator coil, side view

An inner turn has a much shorter end winding than an outer turn. Hence, a turn positioned closer to the tooth will have a smaller resistance than a turn positioned further away from the tooth. All turns have the same exposure length in the stack length which means that all turns will get the same voltage induced. Different turns with different resistances will therefore have different fault currents. To get an idea of how the faulted current varies versus its position within the slot, 5 single shorted turns will be investigated as shown in Figure 7.15. Four turns are positioned on the edges of the coil, and one turn in the centre. The different turns are labelled with letters and colours, and are consistent throughout the thesis.

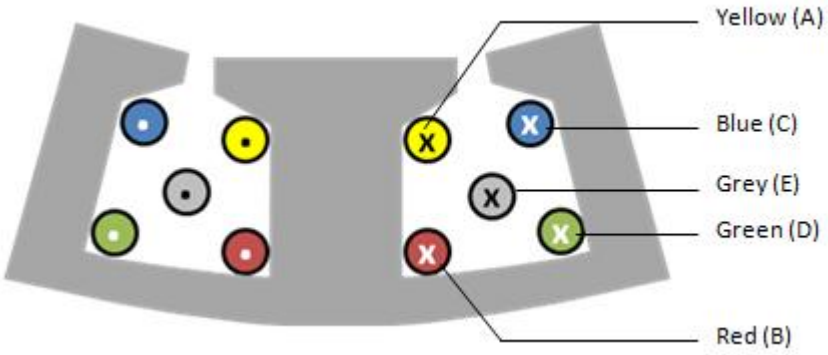


Figure 7.15 – 5 different locations in the stator slot

The resistance of the turns are outlined in Table 7.2 below. The resistances were obtained according to the method described in the next chapter, section 8.2 page 140. The table shows a wide range of resistances with the difference between the Green (D) turn and the Yellow/Red (A, B) turn being the greatest. The Green (D) turn has a resistance 70% greater than that of the Red or Yellow turn.

Turns	Turn resistance	End winding resistance	Unit
211 (coil)	1.60	1.160	Ω
Average turn	7.58	5.498	mΩ
Yellow (A)	5.15	3.087	mΩ
Red (B)	5.15	3.087	mΩ
Blue (C)	7.75	5.687	mΩ
Green (D)	8.75	6.687	mΩ
Grey (E)	6.90	4.837	mΩ

Table 7.2 – Resistance for each turn

7.5 Heating

When a current is flowing through a conductor, its temperature will rise due to i^2R losses. In the fault tolerant motor, the teeth that surround the coils help cooling as the temperature difference is conducted in to the iron core back. From there, the heat is dissipated in to the surrounding environment.

This equilibrium can be disturbed when the heat generation exceeds the heat dissipation. This is the case for the ELGEAR motor under faulted conditions, when the healthy part of the motor will see rated current (Figure 7.8(c), page 127). The motor can only operate for 20 minutes continuously until it reaches its critical thermal limit of 200 °C. An estimated faulted current of 3.6 times the rated current will cause even more problems since the temperature gradient is proportional to the square of the current density.

The rate at which a copper conductor heats up depends on the specific heat capacity, density, conductivity and current density of copper. The equation is found in (7.13).

Specific heat capacity, **c** (copper): $385\,\frac{J}{kgK}$

Density, **ρ** (copper): $8020\,\frac{kg}{m^3}$

Conductivity, **σ** (copper) $5.96\times10^7\,\frac{A^2s^2}{kgm^3}$

Loss density: $$JE = \frac{J^2}{\sigma} = \rho c \frac{\Delta\theta}{\Delta t}$$

Under adiabatic conditions, temperature rise: $$\frac{\Delta\theta}{\Delta t} = \frac{J^2}{\sigma\rho c} \quad (7.13)$$

Assuming all the heating goes in to the winding, the coils in the ELGEAR motor show a temperature increase of 2.9 °Cs^{-1} for the scenario given in Figure 7.8c, page 127.

If no heat is dissipated, the thermal limit of 200 °C is reached in just over a minute. Thermal simulation states that it takes 20 minutes to reach the thermal limit, which means that the motor is able to dissipate 2.7 °Cs^{-1} on average over 20 minutes for this fault condition. [76]

Current density: $J = \frac{current}{conductor\ area}$

Standard wire gauge 23
(0.61mm diameter)

Faulted current (rms) $\frac{11}{\sqrt{2}} = 7.78A$

Conductor area: $\pi r^2 = \pi \times \left(\frac{0.654 \times 10^{-3}}{2}\right)^2 = 3.36 \times 10^{-7}\, m^2$

Current density J: $J = \frac{7.78}{3.36 \times 10^{-7}} = 23.2 \times 10^6\, Am^{-2}$

Temperature rise in 1 second (Δt=1) $\Delta\theta = \frac{J^2}{\sigma \rho c} = \frac{\left(23.2 \times 10^6\right)^2}{5.96 \times 10^7 \times 8020 \times 385} = 2.9^{\circ} C$ (7.14)

In reality the temperature gradient should reduce slightly as the winding heats up since the resistivity of copper increases with temperature. A higher resistance means a lower fault current and a reduced temperature gradient. The rate at which the individual turns heat up is covered later on in section 9.4.2, page 166.

7.6 Relationship between the individual turns and remaining turns

7.6.1 *Remedial action of turn-turn faults*

According to Haylock [28] and the previous sections, the current flowing through a shorted turn winding may be several times its per-unit rating, resulting in extreme temperature gradients. One solution upon detection would be to short the terminals of the faulted coil. Although both coils in the slot are electrically separated, they are still magnetically coupled since they are wound around the same tooth. The healthy windings will closely couple the shorted turn(s), effectively sharing the faulted current

and therefore suppressing the single shorted turn current to the terminal shorted turn current [28, 81].

Work done by Mitcham [82] indicates that in larger bar wound motors with low number of turns per coil, a terminal short circuit may not necessarily reduce the faulted turn current to its rated value. The author states that the magnitude of which the faulted current is suppressed by depends on the location of the fault within the stator slot. Chai [83] shows that this is due to each turn having its own self and mutual inductance depending on its location within the stator slot. This is confirmed by the Zhigang et al. in [57] where an analytical model was applied.

7.6.2 *The transformer model*

The suppression of faulted current by shorting the remaining turns can be explained by using an analogy of the transformer model (Figure 7.16). The following analysis is based on Shang [84], but is further expanded to cover the details related to turn-turn faults.

During nominal operation, the magnet will produce a flux that will cross the airgap and link the coil. The voltage induced in the coil is analogous to the EMF. The magnet is represented by a coil and the magnet flux linking the coil is represented by the blue arrows. Two additional flux paths have been added to the transformer model which should be ignored at this stage.

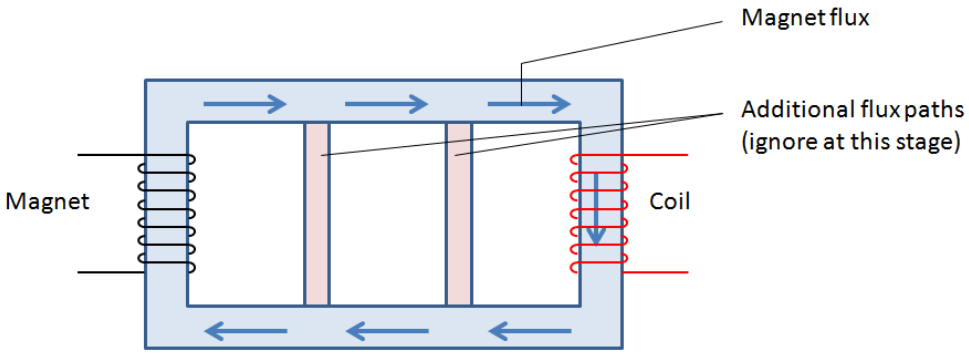


Figure 7.16 – Flux paths

When a single shorted turn fault arises in the coil, the coil and the turn can be represented as in Figure 7.17. The shorted turn is moved to another location in the transformer to show it is electrically disconnected from the coil, but not magnetically (assuming the iron core has ideal properties). The single shorted turn will now see significant multiples of per-unit current.

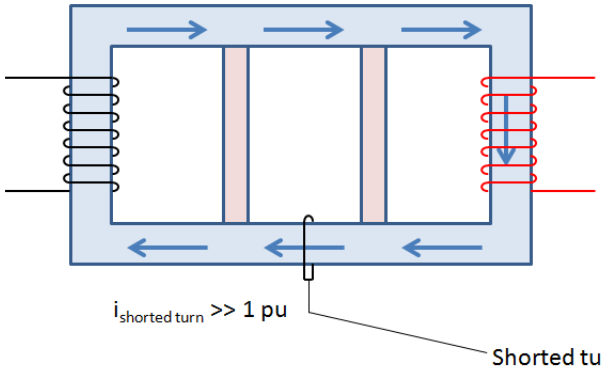


Figure 7.17 – Shorted turn

The remedial action described in the literature is to terminally short the coil where the faulted current is limited to the terminal short circuit current. The coil sets up an MMF that opposes the magnet MMF. As a result, the net flux linking the coil (and also the flux) is significantly reduced. Figure 7.18 shows the opposing flux as red arrows which are produced by the coil.

An important detail is that the opposing flux does not follow the same path as the magnet flux. This is due to the geometry of the motor as there are areas with high reluctance (airgaps), where the flux of the remaining turn may take a different path.

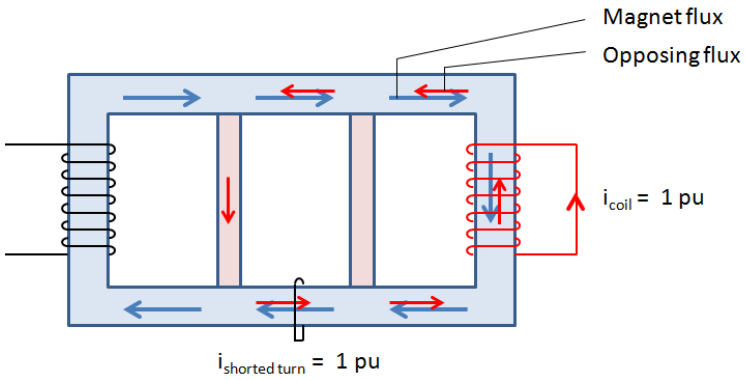


Figure 7.18 – Flux paths, terminal short

The problem arises when some of the opposing flux does not link the shorted turn because it follows a different path. As a result, the shorted turn current will only be partly suppressed, resulting in higher per-unit current as Figure 7.19 shows.

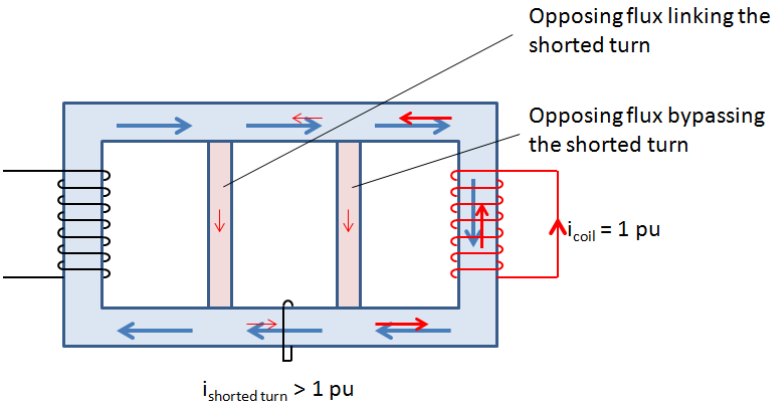


Figure 7.19 – Flux paths, terminal short with a shorted turn

7.6.3 *Mutual inductance*

The transformer equivalent model shows that the shorted turn current in post fault operation is influenced by how well the opposing flux of the remaining turns are linking the shorted turn. This influence is known as mutual inductance, and it is varies depending on the position of the shorted turn in the stator slot. More details on this phenomenon will be covered in the simulation chapter, section 8.5, page 144.

7.7 Conclusion

This chapter has covered a thorough analysis on terminal short circuits and turn-turn faults, in particular the single shorted turn. The influence of suppressing the single shorted turn using the terminal short circuit as remedial action was also covered and discussed.

This chapter discussed that the single shorted turn is influenced by its resistance, which changes depending on its position within the stator slot. The mutual inductance of the coil has a great effect when dealing with the remedial action, and it also varies with position within the stator slot.

The magnitude of current in the single shorted turn before and after remedial action differs quite significantly depending on the type of motor. Further simulation and experimental implementation of the ELGEAR motor should determine which parameters particularly influence the single turn fault.

Simulation

Chapter 8

8.1 Introduction

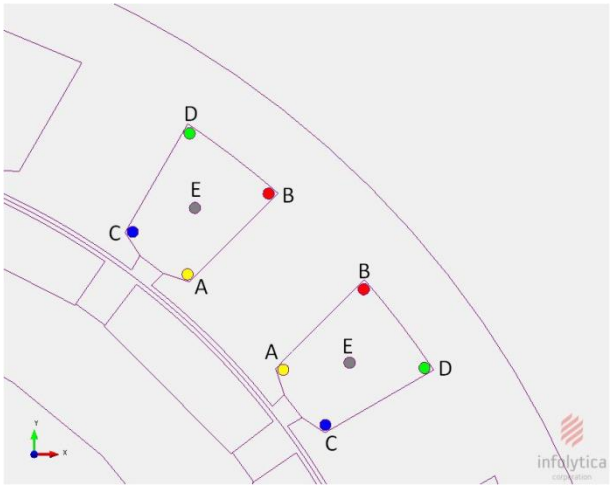
This section follows up from the previous chapter and presents the simulation results of the single turn fault and its post fault operation where a terminal short circuit is applied. The simulation model aims to highlight any potential hazards that may cause problems during the practical implementation, where faults are imposed on the ELGEAR motor.

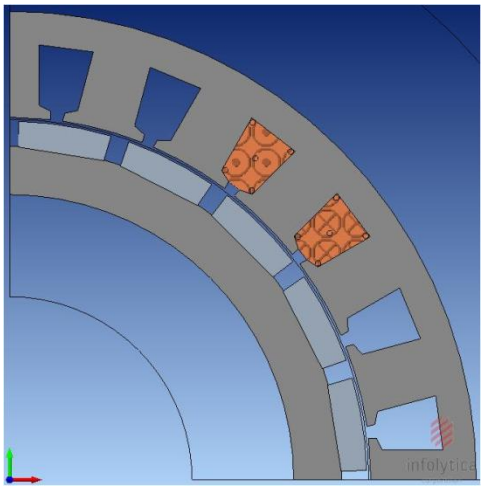
The software packages used are MagNet by Infolytica (finite element analysis) and Matlab. The motor dimensions entered are that of the ELGEAR motor, which can be found in section 6.4, page 108. Most simulations were performed using 2D finite element analysis, which means that the end windings are not taken into account.

Since the end windings carry a significant proportion of the resistance of the turns, the end winding resistances were measured on the actual rig and added to the simulation in the form of a resistor.

Due to the lack of end winding simulation, the self and mutual inductances will also be reduced. Most of the mutual coupling of the coils takes place in the region where the turns are in the stack and not in the end windings. This is because the relative permeability of iron is many times higher than that of air. The mutual coupling in the end windings have not been compensated for. This difference can be seen later on the thesis when the simulation and the practical results are compared.

The simulation set up is shown in Figure 8.1. It shows ¼ of the motor, as the rest is symmetric. Simulating only a section significantly speeds up the simulation.





(a) (b)

Figure 8.1 – Simulation set up in MAGNET (Infolytica)

The motor has a total of 211 turns in each slot. Five separate single shorted turns are introduced at the locations shown in Figure 8.1. Four of such turns (A-D) are placed in the corners of the slot and one turn (E) is placed in the centre. Only one shorted turn will be investigated at a time.

The rest of the slot is filled with the remaining 210 turns of the coil. The shorted turns are physically close to the remaining turns but are not electrically connected. The lack of an electrical connection does not make a difference as shown earlier in Figure 6.18, page 117.

8.2 Turn resistance and inductance properties

The resistance and inductance are found in Table 8.1 for each individual turn within the stator slot. The self and mutual inductances are obtained using 2D finite element analysis by MagNet (Infolytica).

On the actual ELGEAR motor, a coil was taken out and rewound precisely with the shorted turns positioned in the slot. The length of the turns was carefully measured as they were placed in the slot. Knowing the length, the resistance of each turn was calculated using the resistivity formula $\left(R = \frac{l}{\sigma A}\right)$ where l is the length of the turn, A its cross-sectional area and σ the conductivity of copper. This value was cross checked by the manufacturer's data sheet, and by measuring the same type of wire with a much longer length using a network analyser with a four wire sensing method (Fluke PM 6304), and scaling it down to length l.

Coil name	Length	Resistance	Self Inductance	Mutual Inductance (with remaining turns)
Remaining Turns	No data	1.60 Ω	7.188 mH	N/A
Yellow (A)	103 mm	5.15 mΩ	177.4 nH	30.75 µH
Red (B)	103 mm	5.15 mΩ	245.2 nH	36.58 µH
Blue (C)	155 mm	7.75 mΩ	177.6 nH	30.77 µH
Green (D)	175 mm	8.75 mΩ	245.2 nH	36.58 µH
Grey (E)	138 mm	6.90 mΩ	184.2 nH	34.80 µH

Table 8.1 – Turn resistive and inductive properties

8.3 Terminal short circuit

Figure 8.2 shows the estimated terminal faulted current of the remaining turns. The 2D simulation presents a much lower inductance (7.19 mH) compared to the 3D simulation (11.55 mH). The 2D simulation does not account for the end windings, and therefore a much lower inductance is measured compared to that of the 3D simulation. The inductance is dominating in coils with many turns, which is reflected in the estimated short circuit current.

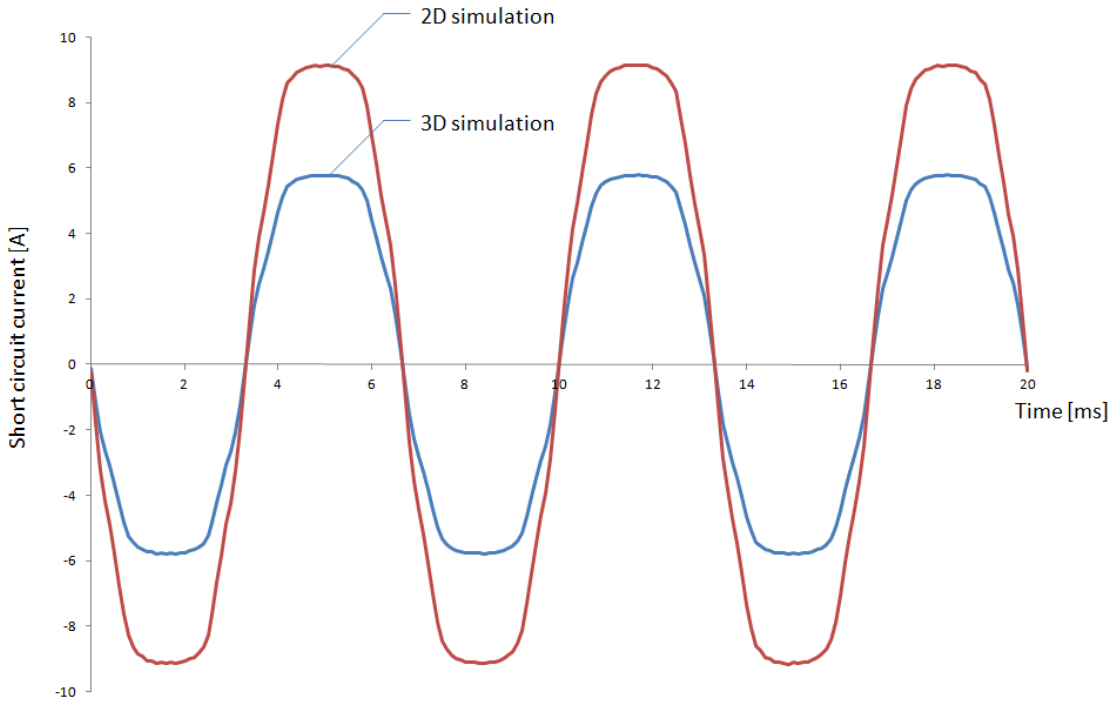


Figure 8.2 – Terminal short circuit

8.4 Single shorted turn

The single shorted turn is simulated and observed in this section. Every turn will be individually short circuited without the influence of any other turn in the slot. In the second part, the turns are given the same resistance in order to observe whether the position of the turn influences the faulted current. The faulted currents are then plotted in the same graph – including the terminal shorted turn for the remaining turns – for comparison.

8.4.1 *Actual resistance per turn*

Figure 8.3 shows the faulted current in a single shorted turn for each of the defined positions. The highest fault current appears in the Yellow (A) and Red (B) turns. These turns are closest to the tooth, and therefore have the minimum end winding resistance. The further away the winding is positioned from the tooth, the lower the faulted current since the end winding resistance increases.

The lowest faulted current is found in the terminal short of the remaining turns, since the inductance plays a significant role in limiting the fault current. Table 8.2 shows the per-unit current of all the turns, with a maximum faulted current of 5.3 pu.

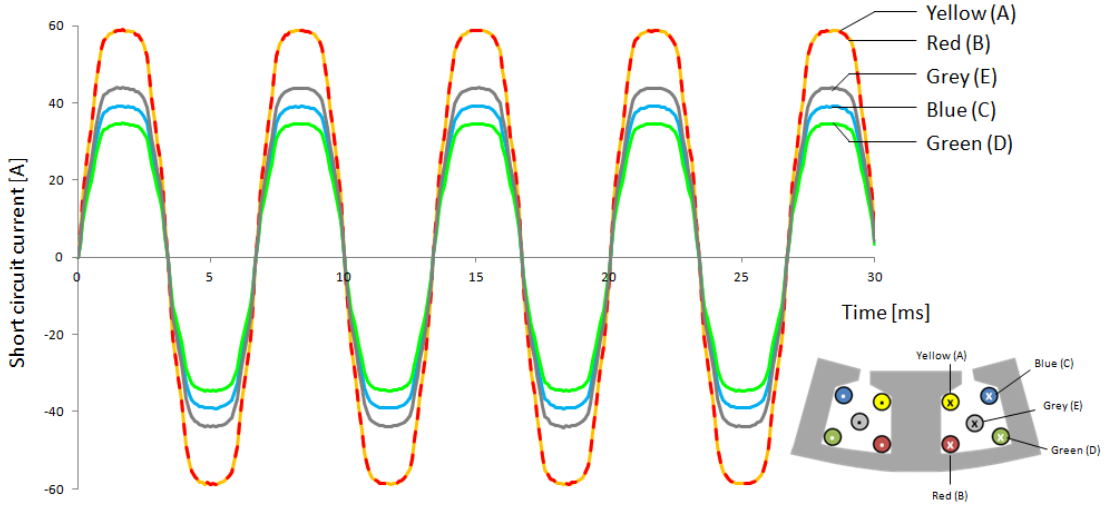


Figure 8.3 – Single shorted turn (actual resistance)

Winding	Per-unit current (1pu = 7.78 A rms)
Yellow (A)	5.3 pu
Red (B)	5.3 pu
Blue (C)	3.5 pu
Green (D)	3.1 pu
Grey (E)	4.0 pu

Table 8.2 – Per-unit faulted currents

8.4.2 *Heating per turn*

A shorted turn fault will increase heating in a turn, as mentioned in section 7.5, page 134. Using the same method to calculate the temperature gradient, the rate at which each turn will heat up is estimated using the simulation results. The result is given in Table 8.3.

Winding	Temperature increase [°Cs^{-1}]
Remaining turns	2.67
Yellow (A)	110
Red (B)	110
Blue (C)	49
Green (D)	38
Grey (E)	61

Table 8.3 – Temperature increase

Clearly, any of the faulted currents produce a very high heating. There is however a significant difference in heating between turns A and B compared to turn D. At this rate, the yellow and red turns will reach its thermal limit in just under two seconds, assuming the turns are unable to dissipate the heat effectively.

8.4.3 *Average resistance per turn*

In order to observe the influence inductance may have upon the faulted current in a turn, all turns are given the same resistance (i.e., the average resistance). This way the faulted current limited by the resistance will be identical in all turns. If a variation of current is observed between the turns, it would be because of the turn's unique inductance (since the inductance varies with the turn's position in the slot). The resistance given is the total resistance of the coil divided by the number of turns $\left(\frac{1.6}{211} = 3.64\ m\Omega\right)$.

The simulation results in Figure 8.4 conclude that the resistance is the only factor limiting the faulted current in a single shorted turn. The influence of inductance – as predicted in the previous chapter – is insignificant. The resulting fault current has an approximate peak of 40 A which is 3.6 per-unit current. This is in agreement with the predictions of the mathematical analysis in section 7.3.3, page 131.

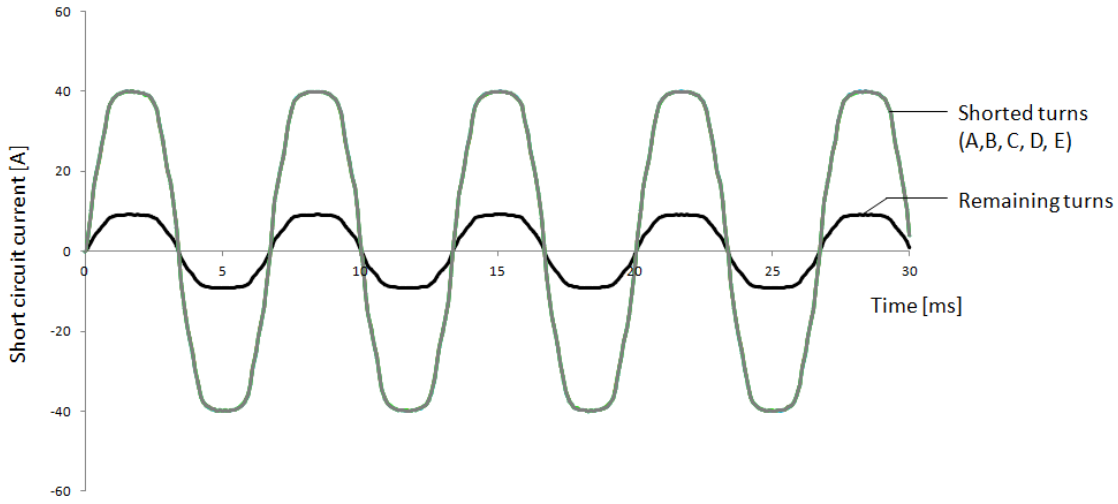


Figure 8.4 – Single shorted turn (average resistance)

8.5 Remedial action – terminal short circuit

8.5.1 *Flux analysis*

When the motor is running at rated speed, the magnets induce a voltage in the turns. If a terminal short circuit is applied on the coil, the faulted current will create a flux that opposes the magnet flux. The magnet flux and the opposing flux are shown individually in Figure 8.5 and Figure 8.6 respectively. Figure 8.7 (page 146) shows the resulting flux and flux density in the motor.

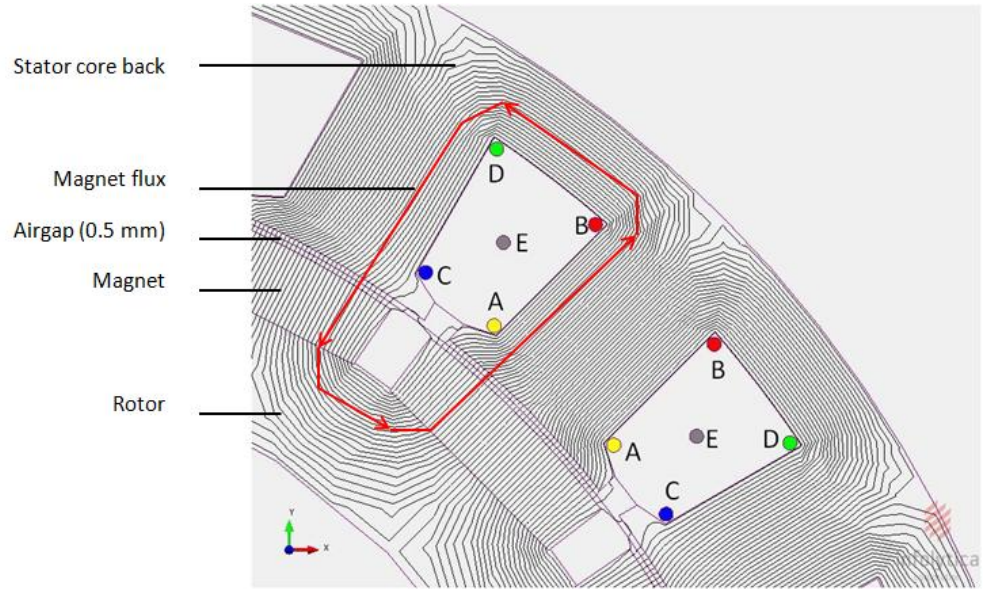


Figure 8.5 – Magnet flux component only

The magnet flux is simulated by open-circuiting the windings and running the simulation. The windings will not produce any flux since no current is flowing. The path of the magnet flux is shown in Figure 8.5 in red. The flux crosses the airgap, links the coil and turns, and returns via the stator core back, the isolation tooth and the airgap.

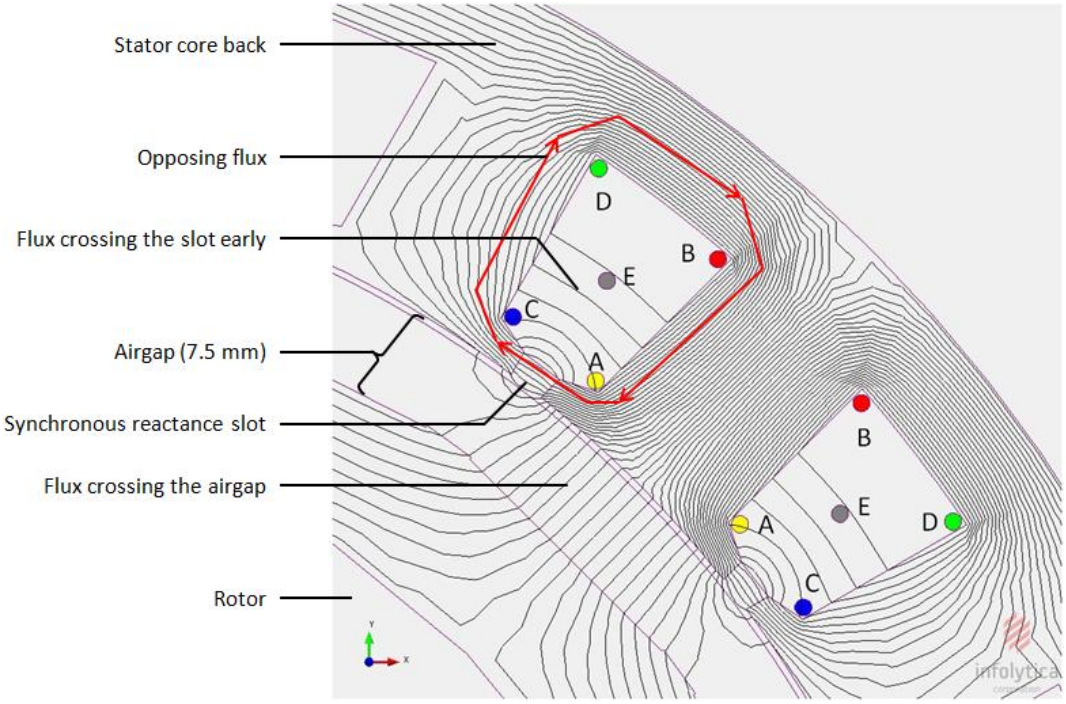


Figure 8.6 – Opposing flux only

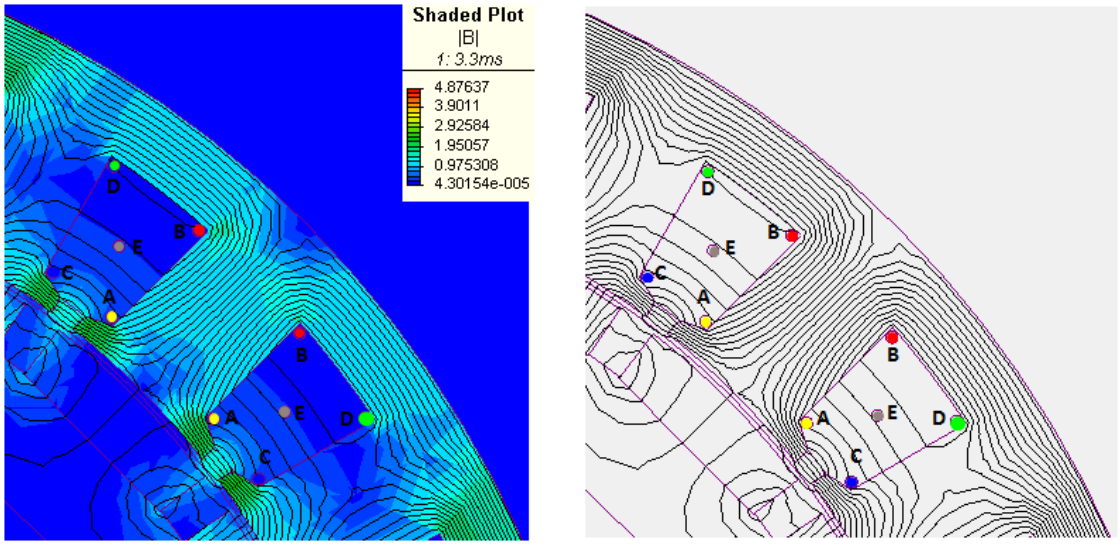
The opposing flux is simulated by removing the magnet and introducing the rated current in the remaining turns. Since the magnets are surface mounted and appear to be

an area of high reluctance from the point of view of the coil, the airgap is effectively increased to 7.5 mm (where 0.5 mm is the airgap, and 7 mm the magnet depth).

In an ideal scenario, the opposing flux path circulates around the entire coil and crosses the synchronous reactance slot as shown by the red arrows in Figure 8.6. The flux crosses the slot opening since this is an area of minimal reluctance. The path the flux follows is different to the path the magnet flux follows, since the airgap is not crossed. This is analogous to Figure 7.18 (page 137) of the transformer model.

In addition to the cross slot leakage flux some of flux crosses the air-gap and magnet. More problematic is the effect of the opposing flux crossing the stator slot early (i.e. before the slot opening). Depending on the turns' location, only a limited amount of the opposing flux will be linking the turns (analogous to the transformer model in Figure 7.19 page 138). If a shorted turn were to occur in the turns closest to the slot opening (locations A and C), it could potentially lead to fault currents greater than expected in post fault operation due to poor mutual inductances. The Red and Green turns (B and D) are clearly not affected by this phenomenon since all opposing flux is linking these turns.

The diagrams in Figure 8.7 show the resulting flux – or actual flux seen – in the motor. The flux density plot shows that the tooth tips are saturated at the slot opening, forcing some of the flux to cross the slot before the slot opening.



Flux density B [T] Flux plot

Figure 8.7 – Resulting flux in the motor (magnet flux and opposing flux superimposed)

8.5.2 *Self and mutual inductances*

The self and mutual inductance of two coils is obtained using 2D simulation. Take for example two coils, coil 1 and coil 2 as shown in Figure 8.8. In this example, coil 1 are the remaining turns (210 turns) and coil 2 is a single shorted turn located at A.

Inductance coil 1 = L_1+M Inductance coil 2 = L_2+M

Figure 8.8 – Mutual and self inductances of coil 1 and coil 2

In MagNet, the self and mutual inductance is derived using the following steps, assuming the flux does not saturate:

1. A 1pu current is forced in to coil 1 while coil 2 is open-circuited. The flux linkage is observed to be 7.188E-3 Wb-turn. Using Equation (8.1), it can be seen that the self-inductance L_1=7.188 mH.

   $$\lambda = Li \qquad (8.1)$$

2. Similar to the point above, a 1pu current is now forced in to coil 2 while coil 1 is open-circuited. The observed self inductance for coil 2 is L_2=177.4 nH.
3. The mutual inductance can be found by applying a 1pu current across coil 1, and observing the flux linkage of coil 2: M = 30.75 µH

The self and mutual inductance of every coil is shown in Table 8.4 below:

Coil name	Self Inductance	Mutual Inductance (with remaining turns)
Remaining Turns	7.188 mH	N/A
Yellow (A)	177.4 nH	30.75 µH
Red (B)	245.2 nH	36.58 µH
Blue (C)	177.6 nH	30.77 µH
Green (D)	245.2 nH	36.58 µH
Grey (E)	184.2 nH	34.80 µH

Table 8.4 – Self and mutual inductances of every coil or turn (2D simulation)

8.5.3 *Calculated fault current*

The above shows that self and mutual inductances change, depending on the position of the faulted turn within the stator slot. Mathematically, a shorted turn within a terminal shorted coil is described by equations (8.2) and (8.3).

Single shorted turn: $$V_1 = R_1 i_1 + j\omega L_1 i_1 + j\omega L_m i_2 + e_1 \quad (8.2)$$

Remaining terminal short: $$V_2 = R_2 i_2 + j\omega L_2 i_2 + j\omega L_m i_1 + e_2 \quad (8.3)$$

Where:

L_1 and L_2 = Inductance of coil 1 and 2 respectively

L_m = Mutual inductance

e_1 and e_2 = back EMF induced in coil 1 and 2 respectively

Combining both equations, the matrix equation in (8.4) is derived.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & j\omega L_m \\ j\omega L_m & R_2 + j\omega L_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} + \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} \quad (8.4)$$

Suppose coil 1 is shorted and the remaining turns (coil 2) are then subsequently shorted to limit the fault current. Both voltages V_1 and V_2 are equal to zero, the matrix equations are now solved for currents i_1 and i_2 to obtain equation (8.5).

Since: $$\begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} = \frac{\begin{bmatrix} D & -B \\ -C & A \end{bmatrix}}{|AD - BC|}$$

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} R_1 + j\omega L_1 & j\omega L_m \\ j\omega L_m & R_2 + j\omega L_2 \end{bmatrix}^{-1} \begin{bmatrix} -e_1 \\ -e_2 \end{bmatrix}$$

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left[\frac{\begin{bmatrix} R_2 + j\omega L_2 & -j\omega L_m \\ -j\omega L_m & R_1 + j\omega L_1 \end{bmatrix}}{\left| (R_1 + j\omega L_1)(R_2 + j\omega L_2) - (j\omega L_m)^2 \right|} \right] \begin{bmatrix} -e_1 \\ -e_2 \end{bmatrix} \quad \textbf{(8.5)}$$

The calculations in (8.5) are performed for every turn in Matlab, using the self and mutual inductance values from MagNet. Two simulations of the faulted current are being performed:

1. A fully simulated MagNet environment, where the faulted current is determined using finite element analysis.
2. A Matlab environment where the faulted current is calculated using the inductance values from MagNet in the method shown in 8.5.2.

To avoid confusion, point one is referred to the MagNet 2D simulation, and point two is referred to the Matlab mathematical analysis.

8.5.4 *Simulation and mathematical results*

The shorted turns with remedial action are individually simulated and analysed by MagNet and Matlab in Figure 8.9 and Figure 8.10 respectively. The faulted current of the Yellow (A) and Red (B) turns are not reduced to 1 pu as a result of the applied terminal short circuit. The turns' locations are closest to the stator tooth and therefore have the smallest resistance compared to the other shorted turns. The Red (B) turn is further back, close to the iron core back, and therefore has more self and mutual inductance compared to the Yellow (A) turn. The variation in self and mutual inductance of each turn do not appear to have a great influence at this point. The largest currents are those in turns with the least resistance.

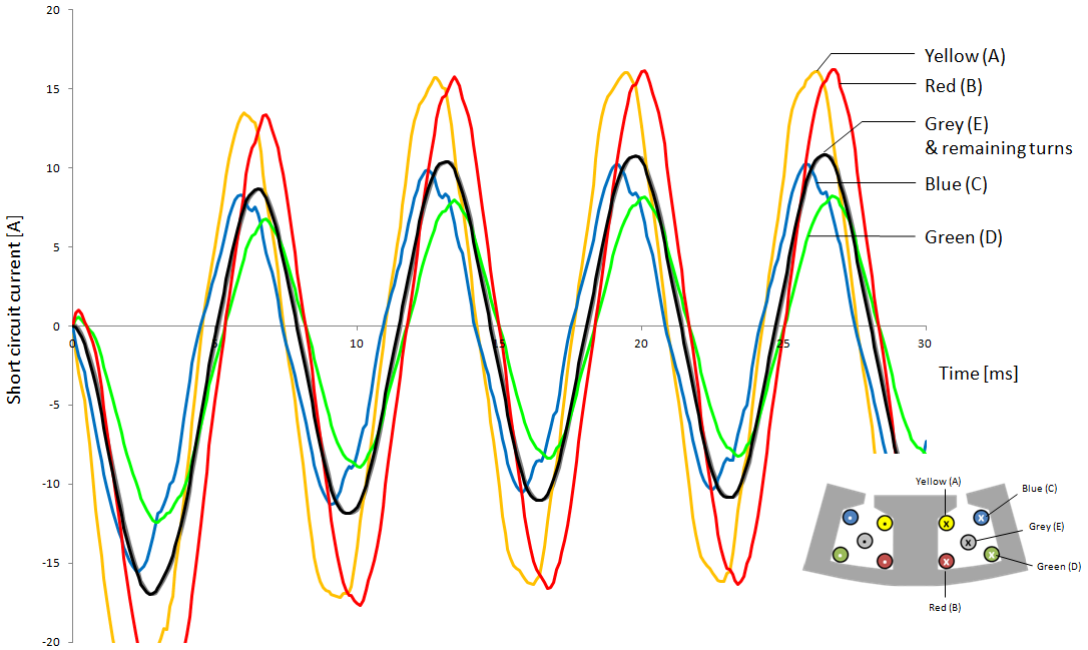


Figure 8.9 – by MagNet – Fault current in the single shorted turn with remedial action

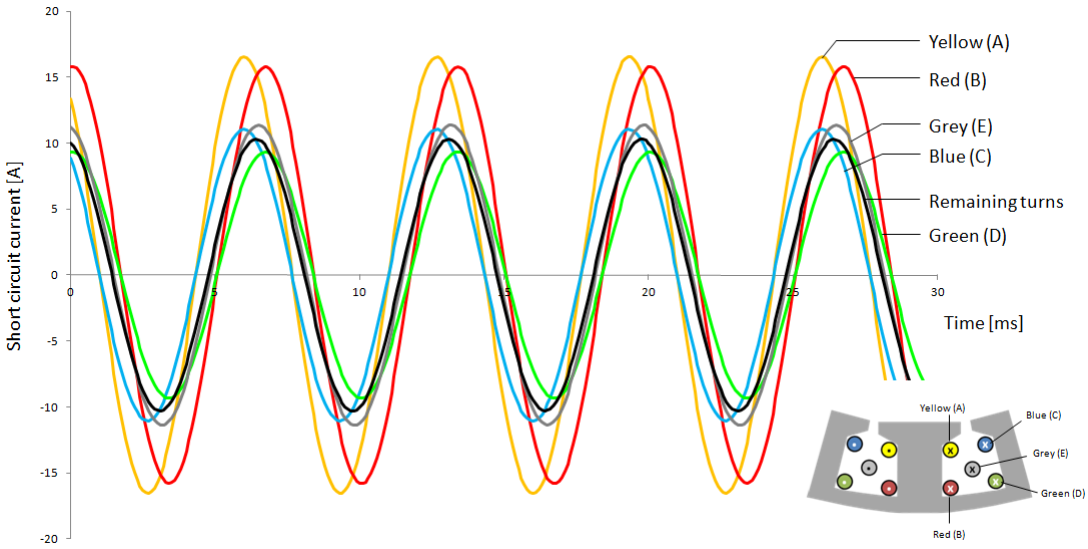


Figure 8.10 – by Matlab – Fault current in the single shorted turn with remedial action

Winding	Single shorted turn	Single shorted turn & remedial action	
	Matlab	MagNet	Matlab
Remaining turns		0.98 pu	0.94 pu
Yellow (A)	5.35 pu	1.45 pu	1.50 pu
Red (B)	5.35 pu	1.46 pu	1.44 pu
Blue (C)	3.56 pu	1.01 pu	1.00 pu
Green (D)	3.15 pu	0.82 pu	0.84 pu
Grey (E)	3.99 pu	0.98 pu	1.03 pu

Table 8.5 – Per-unit faulted currents

8.5.5 *MagNet versus Matlab*

Both simulation and analytical techniques display similar results – mainly because the inductance used in both cases originates from the flux linkage method defined by MagNet. The difference between the methods is observed by comparing Figure 8.9 and Figure 8.10. It can be seen that the simulation uses a time stepping method which incorporates an initial transient effect. From this point onwards only the mathematical analysis method will be shown in the thesis, although both methods are still applied for validation.

8.6 Terminal short circuit – ignoring resistance

In order to observe how the (self and mutual) inductances influence the faulted current in each turn, the resistance is reduced to zero. This means that the faulted current is now purely limited by the turn's self and mutual inductance. This is purely theoretical and can only be done in the simulation model, since every inductor will inherently carry an equivalent series resistance. The results are shown in Figure 8.11.

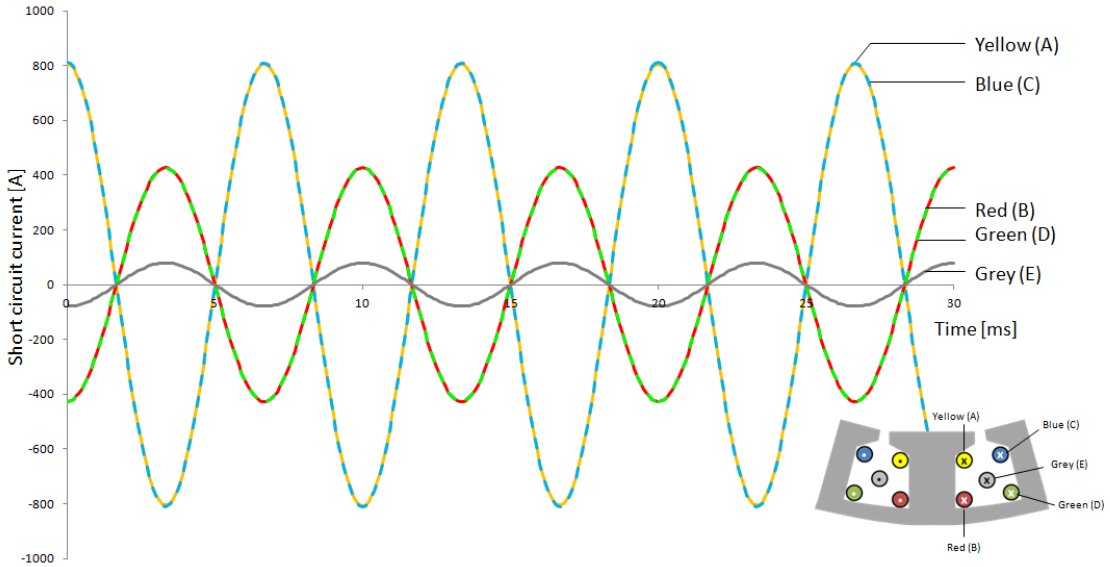


Figure 8.11 – Theoretic windings with no resistance

Since the current is limited by the inductance only, the current will lead the voltage, and therefore appears to look inductive. This is true for the Red, Green and Grey turns. The turns closest to the slot opening (Yellow and Blue), appear to be capacitive as the current lags the voltage by 90°. This unusual phenomenon occurs as a result of the leakage inductance.

8.6.1 *The effect of leakage inductance*

Figure 8.12 shows a diagram representing coil 1 and coil 2 in terms of reluctance paths. The diagram shows the leakage reluctance of coil 1, coil 2 and the mutual reluctance of both coils.

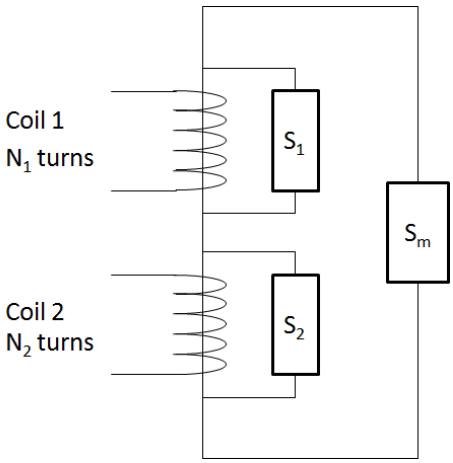


Figure 8.12 – Reluctance paths in coils

The flux can be expressed in the following equations:

Mutual flux: $$\phi_m = \frac{N_1 i_1 + N_2 i_2}{S_m}$$

Leakage flux, coil 1: $$\phi_{1l} = \frac{N_1 i_1}{S_1}$$

Leakage flux, coil 2: $$\phi_{2l} = \frac{N_2 i_2}{S_2}$$

The flux linkage is described by:

$$\psi_1 = N_1\phi_m + N_1\phi_{1l}$$

$$\therefore \psi_1 = \frac{N_1\left(N_1 i_1 + N_2 i_2\right)}{S_m} + \frac{N_1^2 i_1}{S_1} \qquad (8.6)$$

$$\psi_2 = N_2\phi_m + N_2\phi_{2l}$$

$$\therefore \psi_2 = \frac{N_2\left(N_1 i_1 + N_2 i_2\right)}{S_m} + \frac{N_2^2 i_2}{S_2} \qquad (8.7)$$

From equations (8.6) and (8.7), the flux linkages are now expressed in terms of currents i_1 and i_2 in the matrix equation (8.8):

$$\therefore \psi_1 = \frac{N_1^2}{S_m} i_1 + \frac{N_1^2}{S_1} i_1 + \frac{N_1 N_2}{S_m} i_2$$

$$\therefore \psi_2 = \frac{N_1 N_2}{S_m} i_1 + \frac{N_2^2}{S_m} i_2 + \frac{N_2^2}{S_2} i_2$$

$$\begin{bmatrix} \psi_1 \\ \psi_2 \end{bmatrix} = \begin{bmatrix} \frac{N_1^2}{S_m} + \frac{N_1^2}{S_1} & \frac{N_1 N_2}{S_m} \\ \frac{N_1 N_2}{S_m} & \frac{N_2^2}{S_m} + \frac{N_2^2}{S_2} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \qquad (8.8)$$

Coil 1 leakage inductance: $$L_{1l} = \frac{N_1^2}{S_1}$$

Coil 2 leakage inductance: $$L_{2l} = \frac{N_2^2}{S_2}$$

Mutual inductance $$L_m = \frac{N_1 N_2}{S_m}$$

By substituting the coil's leakage and mutual inductance into equation (8.8), the following equation is obtained:

$$\begin{bmatrix} \psi_1 \\ \psi_2 \end{bmatrix} = \begin{bmatrix} \frac{N_1}{N_2} L_m + L_{1l} & L_m \\ L_m & \frac{N_2}{N_1} L_m + L_{2l} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad (8.9)$$

Since:

inductance coil 1: $$L_1 = \frac{N_1}{N_2} L_m + L_{1l} \quad (8.10)$$

Inductance coil 2: $$L_2 = \frac{N_2}{N_1} L_m + L_{2l} \quad (8.11)$$

Equation (8.9) is now expressed as:

$$\begin{bmatrix} \psi_1 \\ \psi_2 \end{bmatrix} = \begin{bmatrix} L_1 & L_m \\ L_m & L_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad (8.12)$$

From equation (8.12) and (8.4) – when the resistances are equal to zero – equation (8.13) is obtained:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} j\omega L_1 & j\omega L_m \\ j\omega L_m & j\omega L_2 \end{bmatrix}^{-1} \begin{bmatrix} -e_1 \\ -e_2 \end{bmatrix} \quad (8.13)$$

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} \frac{jL_2}{\omega\left(L_m{}^2 - L_1 L_2\right)} & \frac{-jL_m}{\omega\left(L_m{}^2 - L_1 L_2\right)} \\ \frac{-jL_m}{\omega\left(L_m{}^2 - L_1 L_2\right)} & \frac{jL_1}{\omega\left(L_m{}^2 - L_1 L_2\right)} \end{bmatrix} \begin{bmatrix} -e_1 \\ -e_2 \end{bmatrix}$$

Take the assumption that coil 1 consists of one turn, and coil 2 consists of the remaining turns:

Now: $N_1 e_2 = N_2 e_1$

$$i_1 = \frac{je_1}{\omega\left(L_m{}^2 - L_1 L_2\right)}\left(\frac{N_2}{N_1} L_m - L_2\right) \tag{8.14}$$

$$i_2 = \frac{je_1}{\omega\left(L_m{}^2 - L_1 L_2\right)}\left(L_m - \frac{N_2}{N_1} L_1\right) \tag{8.15}$$

Substituting equations (8.10) and (8.11) back in to (8.14) gives:

$$i_1 = \frac{je_1\left(\frac{N_2}{N_1} L_m - \frac{N_2}{N_1} L_m - L_{2l}\right)}{\omega\left(L_m{}^2 - \left(\frac{N_1}{N_2} L_m + L_{1l}\right)\left(\frac{N_2}{N_1} L_m + L_{2l}\right)\right)}$$

$$i_1 = \frac{-je_1 L_{2l}}{\omega\left(\frac{N_1}{N_2} L_m L_{2l} + \frac{N_2}{N_1} L_m L_{1l} + L_{1l} L_{2l}\right)}$$

since: $N_1 = 1$

$$i_1 = \frac{-je_1 L_{2l}}{\omega\left(\frac{L_m L_{2l}}{N_2} + N_2 L_m L_{1l} + L_{1l} L_{2l}\right)} \tag{8.16}$$

8.6.2 *Positive and negative leakage inductance for different turns*

The current in the shorted turn i_1 is described in equation (8.16). The numerator of the expression contains the leakage term L_{2l}. Most turns will see a positive leakage inductance for coil 2, which equates to a negative imaginary component for current i_1 – the turn will appear to look inductive.

However, in two cases, the turns look capacitive since a negative leakage inductance for coil 2 is seen, as Table 8.6 shows.

Coil name	Self Inductance (L_1)	Inductance remaining turns (L_2)	Mutual Inductance (L_m)	Leakage inductance
Yellow (A)	177.4 nH	7.07 mH	30.75 µH	Negative
Red (B)	245.2 nH	6.98 mH	36.58 µH	Positive
Blue (C)	177.6 nH	7.07 mH	30.77 µH	Negative
Green (D)	245.2 nH	6.98 mH	36.58 µH	Positive
Grey (E)	184.2 nH	7.03 mH	34.80 µH	Positive

Table 8.6 – imaginary component of the s/c current, based on the self and mutual inductances

Single shorted turns which are positioned close to the iron core back are not influenced by the leakage flux, since the teeth and the iron core back provide a low reactance path for the flux at this location. The apparent capacitive coupling is actually due to a negative leakage inductance.

This unusual situation occurs in terms of the magnetic coupling between a complete coil, spread over an entire slot, and a single turn, depending upon the position of the turn. Current in the complete coil generates magnetic flux which crosses the slot. Conductors at the bottom of the slot, near the core back, such as conductors B and D, link all this flux, whilst conductors at the top of the slot, such as coils A and C, only link a proportion of it. Hence, when there is current in the complete coil, then the flux linking each turn A and C is greater than the average flux per turn of the complete coil. This is akin to having a negative leakage inductance.

8.7 Conclusion

The simulation and the mathematical results agree with the theoretical analysis of the previous chapter. A single shorted turn causes high fault currents with a magnitude that varies depending on the location of the turn in the slot. This is due to the turns having a smaller resistance when positioned closer to the tooth, or a larger resistance when wound further away from it. The per-unit currents vary from 3.1 pu to 5.3 pu. The consequence of high per-unit current is a localised high temperature gradient in the shorted turn. At this point, no influence of inductance in suppressing the faulted current was observed.

The fault can be effectively suppressed by applying a terminal short circuit to the coil as remedial action. This action significantly suppresses the faulted current in all the turns. The per-unit currents now range from 0.8 pu to 1.5 pu. This shows that the mutual inductance between the remaining turns and the single faulted turn have a significant effect. Nevertheless, the turns with the highest fault current are those turns closer to the tooth and not the slot opening. This effect occurs because the impedance is mainly due to its resistance rather than self-inductance. This would not be the case for large motors with only few turns, where the inductance would be more dominant.

The imaginary component of the single shorted turn is influenced by the leakage inductance. It was shown that most turns experience a positive leakage inductance, indicating that the turn looks inductive. Some turns – those closer to the slot opening – experience a negative leakage inductance, and the turns therefore appear to look capacitive. In the case of the ELGEAR motor this phenomenon is observed with a slight phase shift, as the faulted current in the turns closer to the slot opening are leading the EMF, whilst the shorted turn currents at the bottom of the slot lag the EMF. Since the resistance is dominant, the effects of the imaginary components are very small.

Based on the conclusions of this chapter, the approximate magnitude of the faulted turn-turn current was estimated for both fault and post fault operation. The faulted conditions will now be implemented on to the ELGEAR test rig. Using the variables determined in the simulation, the faults can now be induced on the test rig whilst still remaining in the safety zone (i.e. avoiding excess temperature gradients that could destroy the motor).

Practical Implementation

Chapter 9

9.1 Introduction

This section follows on from the theory, simulation and mathematical analysis of the previous chapters. The single shorted turns are now induced upon the ELGEAR motor.

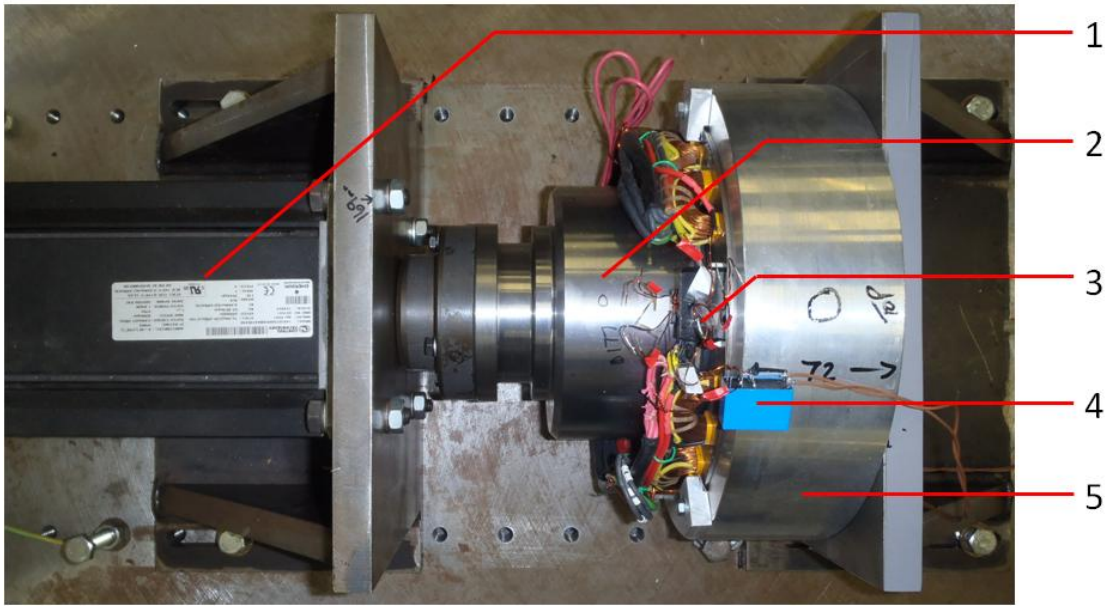
It was determined that a single shorted turn would significantly heat up the winding due to the high per-unit current flowing through it. Care must be taken that the single shorted turn must not exist for too long as this could cause the coils to heat up and damage the motor.

The results will be compared to the simulation results and other fault tolerant motors in the literature. Finally, recommendations will be made to improve the ELGEAR motor and hence, improve future fault tolerant motor designs.

9.2 Set up

9.2.1 *The ELGEAR rig*

The set up of the ELGEAR rig for the purpose of investigating single shorted turn faults is shown in Figure 9.1. The motor's architecture is dual lane, described in detail in section 6.4, page 108. In the event of a fault, the remaining healthy lane will continue to drive the rotor at rated speed. For these tests the secondary part of the motor is not connected to a drive: this scenario is reproduced using an external motor which turns the rotor at rated speed.



1 – Motor, connected to the rotor to provide rated speed

2 – Rotor

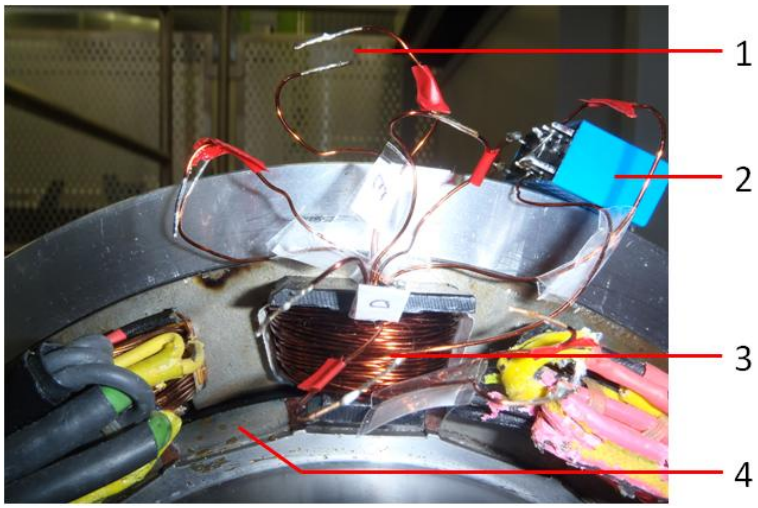
3 – Rewound coil in the stator winding

4 – Relay used to switch in and out the terminal short circuit of the coil

5 – Frame housing the stator

Figure 9.1 – Set up of the ELGEAR rig for the investigation of single turn faults (top view)

One coil of 211 turns is taken out and rewound as shown in Figure 9.2. A coil of 210 turns is wound in the stator instead, as well as five single shorted turns in the locations shown in Figure 8.1 page 140.



1 – One (of five) single shorted fault

2 – Relay used to switch in and out the terminal short circuit of the coil

3 – Rewound coil in stator slot

4 – One (of 20) surface mounted magnets on the rotor

Figure 9.2 – Coil rewound with 5 single shorted turns positioned in the slot

9.2.2 *Shorted turns*

From the physical location of the shorted turns A-E in the slot, it can be seen that their lengths differ. Earlier it was mentioned that turns closer to the tooth have shorter winding lengths. However, the shorted turns have to be extended to accommodate a current transducer.

The turns are placed in the slot and their true length measured. The turns are then extended for short circuit testing so that all turns have the same given length (a length of 250 mm per turn was chosen, see Table 9.1 *given length*).

The measured data is then compensated to predict the true shorted current in the windings under nominal condition (see Table 9.1 *true length*). A factor of $\frac{Given\ Resistance}{True\ Resistance}$ was applied to the data for compensation.

The inductance was not compensated, since the assumption was made that the inductance for the actual and given turns are the same. This assumption is reasonably accurate since the effect of the self inductance is negligible for single turns. Furthermore, the extended turns still cover the same path as the original turn, and the mutual coupling should therefore be similar.

Turn	**Given length**	**True length**	**Given resistance @ 20°C**	**True resistance @ 20°C**
Turn A	250 mm	103 mm	12.5 mΩ	5.15 mΩ
Turn B	250 mm	103 mm	12.5 mΩ	5.15 mΩ
Turn C	250 mm	155 mm	12.5 mΩ	7.75 mΩ
Turn D	250 mm	175 mm	12.5 mΩ	8.75 mΩ
Turn E	250 mm	138 mm	12.5 mΩ	6.90 mΩ

Table 9.1 – Turn's given length/resistance and actual length/resistance

9.2.3 *Measurement*

The faulted current in the single shorted turn will cause significant i^2R heating. The shorted turn cannot be exposed to a high temperature gradient for too long during the experimentation. A circuit has been constructed to ensure the remaining turns are shorted at all times. This would suppress the current in the faulted turn to the terminal shorted turn current.

A normally closed relay is connected to the terminals of the remaining turns. Using a simple 555 timer, the relay is programmed to open for 130 ms when the manual switch is pressed. During this period, the faulted turn current in the single shorted turn is measured. In the worst case, assuming adiabatic conditions, a maximum temperature increase of 14 °C will take place during this period. This is considered acceptable.

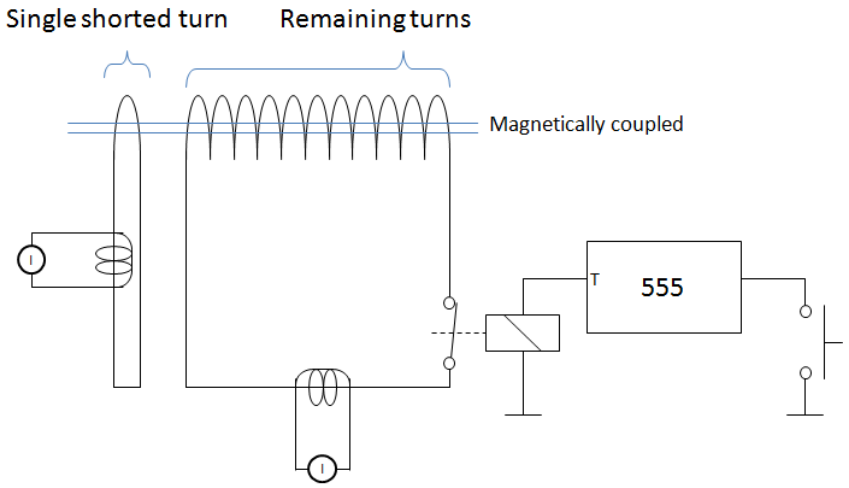
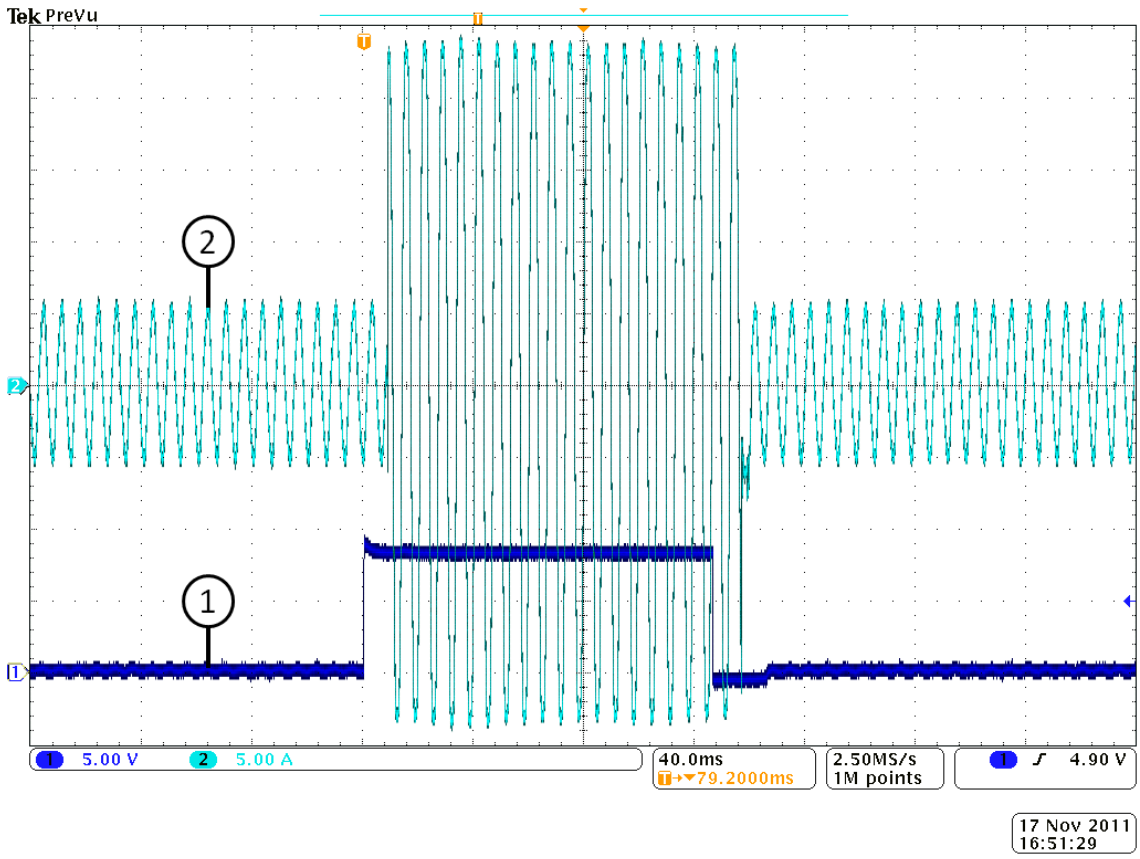


Figure 9.3 – Faulted current

Figure 9.4 shows an example of such switching taking place. A small delay was observed between the point the manual switch was pressed and the actual opening of the relay. This delay is due to the magnetising current required to operate the relay.

Once the relay is opened (i.e., the terminal short circuit is removed), it was found that the current in the single shorted turn increases dramatically, from ~10 A peak-peak to ~50A peak-peak.



Horizontal Scale

Time, 40 µs / div

Vertical Scale

Trace 1 – Switch signal to the relay, 5 V / div

Trace 2 – Current transducer of a shorted turn, 5 A / div

Figure 9.4 – Shorted turn current

9.3 Terminal short circuit on one coil

In this section, the terminals of the remaining turns in the coil are shorted and compared to the simulation results (from heading 8.3, page 141). All other single turns are open circuited.

The terminal short circuit current of the remaining turns for both the practical result and the simulation is shown in Figure 9.5. The practical waveform shows a peak current of 7 A (~5 A rms). This corresponds to a current rating of 0.64 pu.

In a dual lane system, the healthy part of the motor will supply the rated torque (corresponding to 0.64 pu current) plus an additional 35% drag torque. The total current in the healthy windings is estimated to be approximately 0.9 pu, when operating under the worst case condition outlined in Figure 7.8(c), page 127.

The 3D simulated waveform shows a magnitude of 7% less than that of the practical implementation. The 2D simulation – which does not take the end winding inductance in to account – shows a magnitude that is almost 50% higher than the practical implementation.

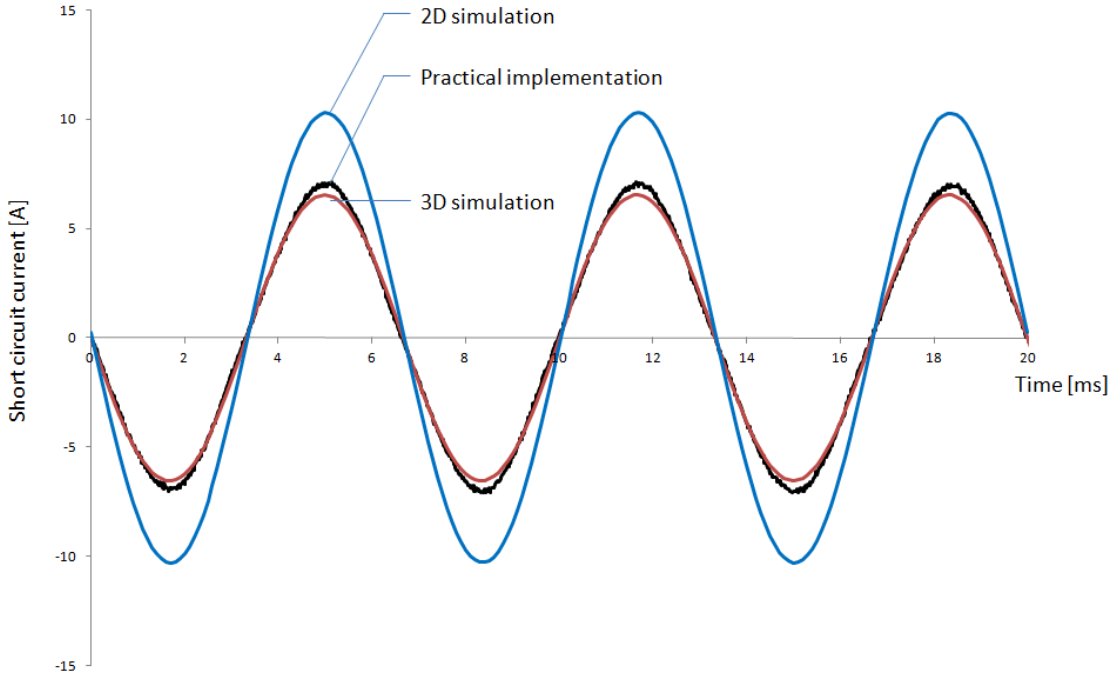


Figure 9.5 – Terminal shorted coil on ELGEAR rig

The details of the open circuit voltage and short circuit current are displayed below:

Practical results

Open circuit voltage (peak)	72 V
Short circuit current (peak)	7 A
Rotor speed	900 rpm
Number of pole pairs	10
Coil resistance	1.6 Ω

The inductance of the coil is calculated below:

Shorted current equation: $$\hat{i} = \frac{\hat{v}}{\sqrt{R^2 + \omega^2 L^2}}$$

Electrical frequency: $$\omega_e = \omega_m \times 10 = 300\pi$$

Inductance: $$L = \sqrt{\left(\frac{\hat{v}^2}{\hat{i}^2} - R^2\right)\frac{1}{\omega^2}}$$

$$L = \left(\frac{72}{7} - 1.6\right)\frac{1}{300\pi} = 10.78mH \quad (9.1)$$

The inductance of the coil is 10.78 mH, compared to the 3D simulation result of 11.55 mH. The difference between both inductor values is 7% and this could explain the similar difference in current magnitudes found in Figure 9.5, especially considering the inductance is dominant. Table 9.2 shows the differences between the simulated inductance and the measured inductance.

	Simulation (3D)	Measured
Resistance	1.60 Ω	1.60 Ω
Inductance	11.55 mH	10.78 mH
Reactance	10.89 Ω	10.16 Ω
Impedance (magnitude)	11.00 Ω	10.29 Ω

Table 9.2 – Simulation and practical comparison of the remaining turns' properties

Naturally, the resistance will also contribute to the difference between the simulated and the practical model. However, this has already been taken in to account, as the end winding resistance was manually applied in the simulation.

9.4 Single shorted turn (remaining portion of coil open-circuit)

The current in the single shorted turns are shown in Figure 9.6. Each shorted turn is compensated individually to predict the faulted current in the winding without the enclosure of a current transducer.

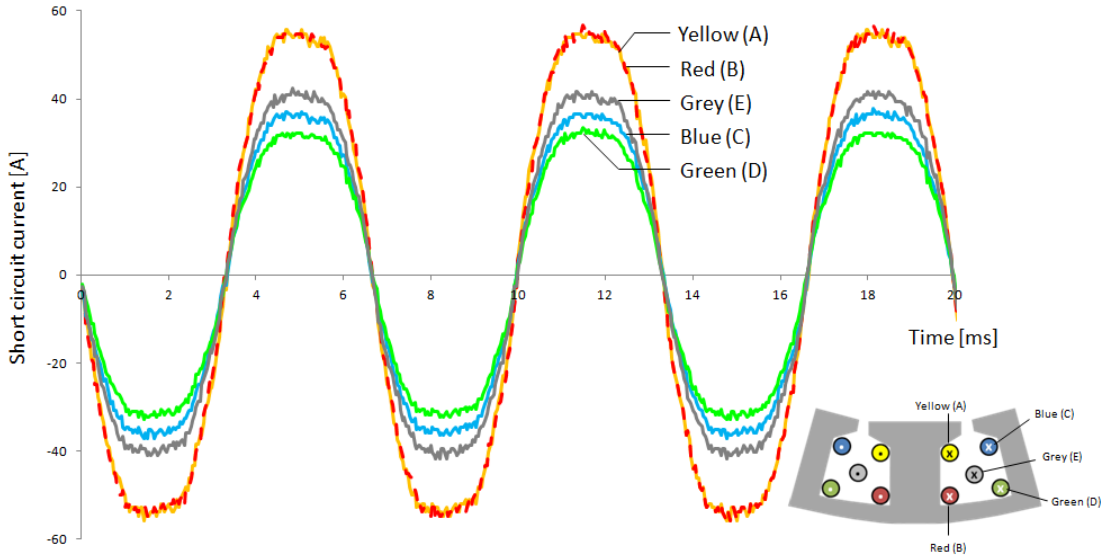


Figure 9.6 – Shorted turn currents

Winding location	Per-unit current (1pu = 7.78 A rms)	
	Simulation	Measured
Yellow (A)	5.35 pu	5.0 pu
Red (B)	5.35 pu	5.0 pu
Blue (C)	3.56 pu	3.3 pu
Green (D)	3.15 pu	2.9 pu
Grey (E)	3.99 pu	3.7 pu

Table 9.3 – Single shorted turn per-unit current, simulation vs. practical implementation

Table 9.3 compares the per-unit faulted current between the simulation and the practical implementation. The single shorted turn currents ranges from 2.9 pu to 5 pu current. This is approximately 8% less than the predicted shorted turn in the 2D MagNet and Matlab simulation.

This difference is due to the heating in the turn. As the temperature rises, the resistance increases, and the faulted current therefore decreases. A 10% increase in resistance occurs when the temperature is approximately 25 °C higher than room temperature. This is achieved within half a minute by the shorted coil.

Resistance is the main component limiting the current, which is in agreement with the simulation and the theory. Again, turns with the shortest end windings (Yellow and Red) have the highest faulted current.

9.4.1 *Comparison to the literature*

Even though the worst case scenario of 5 pu current is very high, it is less severe than in other fault tolerant motors described in the literature. A single turn failure in the fault tolerant motor by Haylock et al. [28], results in 33.2 times the rated current. Consequently a temperature rise of 1545 °Cs^{-1} is observed. In the case of Haylock, remedial action should be taken in milliseconds.

Similarly, Arumugam et al. in [85] propose a vertically distributed winding configuration. A 26 pu faulted current is calculated in the single shorted turn of the proposed motor.

In bar wound PM machines, designed for high electric loading, the effect of a single shorted turn becomes particularly significant. This is due to the low resistance of a turn. Mitcham et al. in [82] only discuss post fault operation and assume the resistance is negligible. It is however estimated that a single shorted turn will result in several multiples of ten per-unit current.

9.4.2 *Heating*

When wires are continuously exposed to overrated current, the effect of i^2R heating will be noticed. It is assumed that the winding will heat up since it is unable to dissipate the heat effectively. When the winding exceeds its thermal limit, the insulation may break down, causing the fault to propagate to other parts of the coil, or even other parts of the motor.

The wire used in the winding is polyester enamelled copper with a maximum permissible operating temperature of 200°C. It is assumed that all heating goes in the turn. The rate at which the turn will heat up is described by the loss density in equations (9.2) and (9.3). The temperature rise depends on the current density, specific heat capacity, density and the conductivity of copper.

The temperature rise of the turn is proportional to the square of the current density. The higher the per-unit current, the exponentially less reaction time there is to detect the fault and apply remedial action. Assuming adiabatic conditions, the rate of rise of temperature can be estimated as follows:

Loss density:

$$JE = \frac{J^2}{\sigma} = \rho c \frac{\Delta \theta}{\Delta t} \tag{9.2}$$

Hence, temperature rise: $$\frac{\Delta\theta}{\Delta t} = \frac{1}{\sigma\rho c} J^2 \quad (9.3)$$

Where:

Specific heat capacity, c (copper): $385 \frac{J}{kgK}$

Density, ρ (copper): $8020 \frac{kg}{m^3}$

Conductivity, σ (copper): $5.96 \times 10^7 \frac{A^2 s^2}{kgm^3}$

The current density is dependent on the current and the cross sectional area of the wire. The current in the single turn is dependent on the resistance, inductance and the frequency.

Current density: $$J = \frac{i_{1turn}}{A} \quad (9.4)$$

Current in one turn: $$i_{1turn} = \frac{e_{1turn}}{R_{1turn} + j\omega L_{1turn}} \quad (9.5)$$

As the temperature of copper increases, the conductivity of the material changes. This will affect the resistance of the turn shown in equation (9.5), as well as the conductivity in (9.3). The behaviour of conductivity as a function of temperature is related to the thermal coefficient, α, of the material shown in equation (9.6). The values denoted with a subscript of nought indicate the reference value at a defined temperature (in this case, room temperature of 20 °C).

Conductivity vs. temperature: $$\sigma(T) = \frac{\sigma_0}{1 + \alpha_0 (T - T_0)} \quad (9.6)$$

Assuming adiabatic conditions, the winding temperature will heat up to its rated value of 200 °C in a few seconds. The increase in temperature for the turns are shown using Matlab Simulink in Figure 9.7. The Yellow (A) and Red (B) turns show the worst case scenario where the thermal limit is reached in just 3 seconds. The Green (D) turn shows the best case scenario, as it will take 8.5 seconds to reach the thermal limit.

The exponential waveform relates to the temperature of the conductors. A short circuit current will cause i^2R heating. As the temperature rises, so does the resistance.

Assuming the emf is constant, if the resistance increases, the faulted current decreases, and therefore the temperature gradient decreases.

In reality it will take longer to reach these temperatures since the turns will dissipate a small amount of heat. The higher the temperature difference between the turn and the environment, the more the heat is dissipated. However, this is expected to make a difference of a couple of seconds only, since the $\frac{\Delta\theta}{\Delta t}$ heating is extremely high.

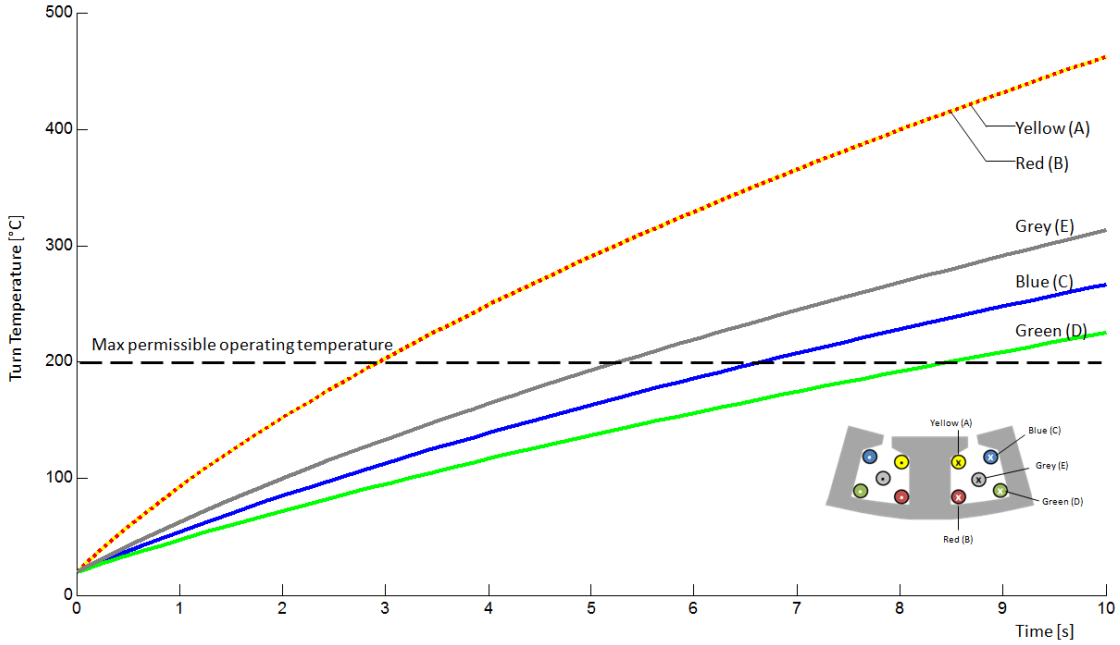


Figure 9.7 – Heating of a single shorted turn

9.5 Single shorted turn with remedial action

Upon detection of a single shorted turn, the terminals of the coil are shorted to suppress the faulted current. Figure 9.8 shows the current in the faulted turn when remedial action is applied. The simulation results from section 8.5.4 are copied to Figure 9.9 so both results can be measured. The measured magnitude of the faulted currents is noted in Table 9.4.

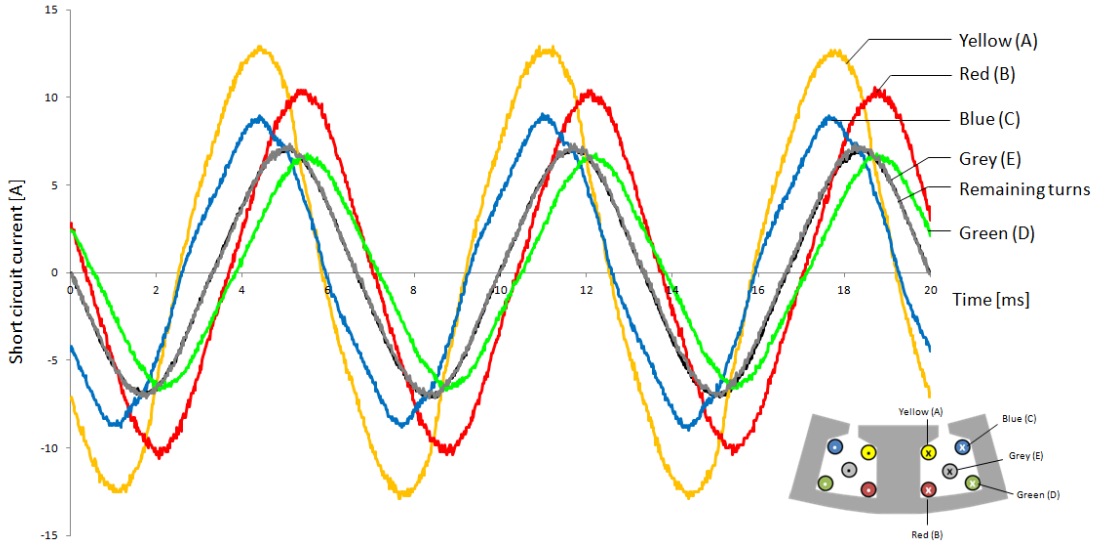


Figure 9.8 – Measured single shorted turn current, with remedial action

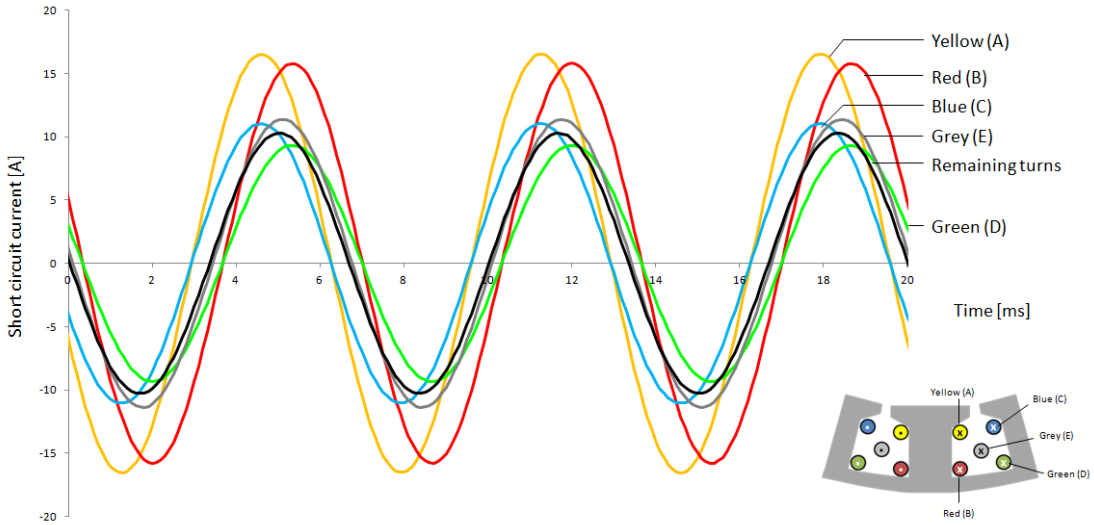


Figure 9.9 – Simulation results of the single shorted turn current, with remedial action
(figure copied from Figure 8.10 page 150)

Winding location	**Per-unit current (1pu = 7.78 A rms)**
Remaining turns	0.64 pu
Yellow (A)	1.17 pu
Red (B)	0.93 pu
Blue (C)	0.80 pu
Green (D)	0.59 pu
Grey (E)	0.64 pu

Table 9.4 – Single shorted turn per-unit current, with remedial action

9.5.1 *Simulation vs. practical implementation*

The measured results are compared with the 2D simulation results in Figure 8.10 page 150. In both graphs, a consistent difference in magnitude is observed which was discussed in heading 9.3.

The practical implementation shows that all the turns – with the exception of the Yellow (A) turn – are effectively suppressed to less than 1 pu current. The severity of faulted current in each of the turns is in agreement with the simulation model. The highest faulted current is recorded in the Yellow (A) turn, the lowest in the Green (D) turn. The simulation and the practical implementation also agree on the phase shifts caused by the capacitive or inductive looking turns due to the leakage inductance behaviour. The turns closer to the slot opening appear to look capacitive, those closer to the iron core back appear to look inductive.

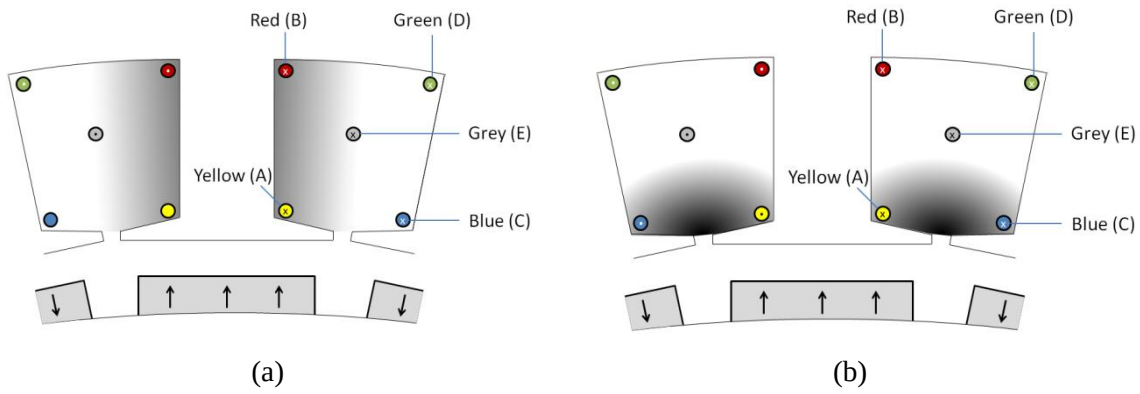
9.5.2 *Analysis of the suppressed currents*

Even though some of the turn-turn currents are higher than the terminal shorted value in post fault operation, they are still below the rated current. The rated current was defined as the current required in the healthy lane to be able to supply rated torque and compensate for the drag torque caused by the faulty lane (situation in Figure 7.8(c), page 127). The additional overrating of drag torque provides an additional margin for the faulted current to be higher than the terminal shorted current whilst remaining below the rated current.

As a result of the different mutual and self inductances of each turn, the magnitude of suppression differs. The Yellow (A) and Red (B) turns have the same resistance but the Red (B) turn is much more effectively suppressed. Similarly, the Yellow (A) and Blue (C) turns have similar mutual and self inductances, but the faulted current in the Blue (C) turn is more effectively suppressed due to its higher resistance.

9.6 Improvements – limiting the current

Figure 9.10(a) shows the locations of the turns where the faulted current is expected to be the highest as a result of the resistance. The turn resistance is the smallest in the areas closest to the tooth. Figure 9.10(b) shows an approximation of the locations within the stator slot where the faulted current is expected to be the highest as a result of the self and mutual inductances. The turn inductances are expected to be the smallest for those located in the darker shaded areas, closest to the slot opening.



(a) (b)

Figure 9.10 – Regions where single shorted turns are likely to have the largest currents

Figure 9.11 show the approximate locations where the single turn is expected to exceed its rated value even though a terminal short circuit is applied as remedial action. The area that is worse affected is where the Yellow (A) turn is located. This is because the turn has the lowest resistance and almost the lowest inductance. The turns close to the slot opening have an even lower inductance, but already a significantly higher resistance.

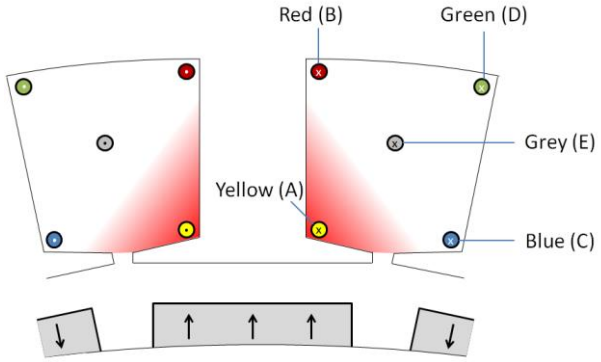


Figure 9.11 – Expected currents exceeding 1 pu in a single shorted turn with remedial action

9.6.1 *Varying the slot reactance*

One change is to increase the slot closure depth to increase the inductance. This would reduce all fault currents, but would increase machine armature reaction causing increased saturation and a larger converted volt-ampere rating. [86, 87].

A second method is to increase the slot depth so that there are no coils in the vicinity of the slot opening. This requires a larger machine volume, resulting in penalties of cost and weight [87].

9.6.2 *Increasing the coil's diameter*

One potential improvement would be to add more resistance to each turn by increasing the coil's diameter. This would result in larger end windings, making the resistance more dominant and hence, more effective suppression of the fault current. The disadvantage is that there will be turns that do not need this additional resistance since the fault current is already below 1 pu without increasing the coil's diameter. The motor also becomes less efficient as the coil resistance is increased, and more expensive since more copper is required.

9.6.3 *Cone shaped diameter of the coil*

Similarly to section 9.6.2 above, the coils' diameter can be increased, but only in areas where there is a requirement to do so. This way, the resistance of the whole coil is not significantly increased. Figure 9.11 shows that the turns closest to the slot opening require a higher resistance so the faulted current can be reduced to the rated value. The coil could be wound in a cone shape, where the turns closer to the slot opening would be designed with a larger diameter, as Figure 9.12 and Figure 9.13 shows.

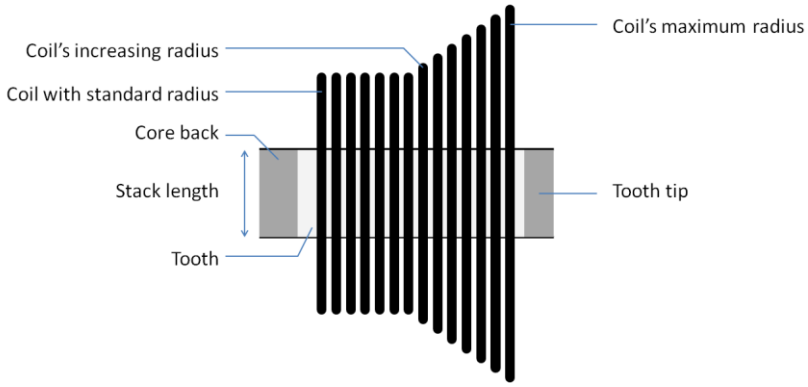


Figure 9.12 – Increase in the coil's diameter closer to the slot opening (side view)

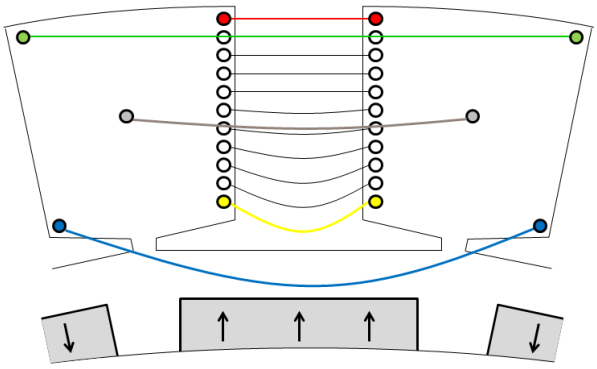


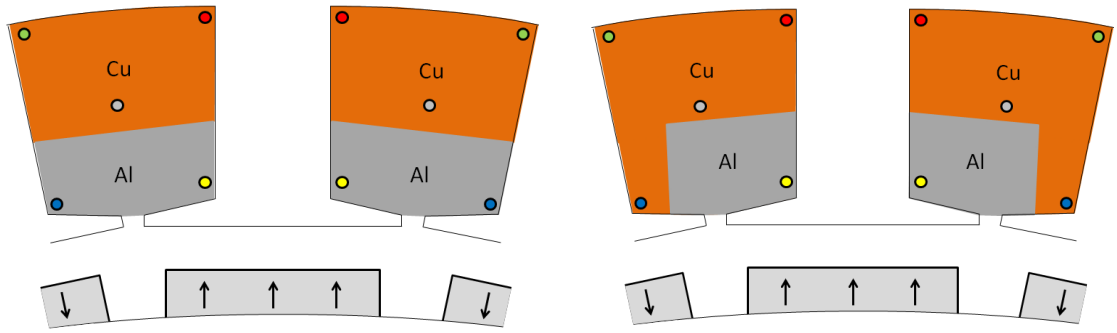
Figure 9.13 – Increase of the coils diameter close to the slot opening (top view)

The disadvantage is that all the turns closer to the slot opening will have an increased resistance. For example, the blue turn (C) does not require an increased resistance, but is on the outermost turn of the coil with an extended radius. It is however an improvement to section 9.6.1 where all the turns' resistances are increased.

9.6.4 *Using two coils of different material*

As a further improvement to the cone shaped coil, two series coils of different materials could be placed in the motor slot. For example, the top end of the slot would be filled with a copper coil and the bottom end of the slot (closer to the slot opening) could be with a material with a lower conductivity – say Aluminium (Figure 9.14a). The properties of inductance would remain unchanged.

Since the windings are wound from the stator tooth outwards, it may even be possible to place the aluminium coil first. This way the shorted turns in question could be targeted more effectively as shown in Figure 9.14b. The Yellow (A) windings and those positioned closer to the slot opening would contain higher resistance properties, whereas the blue (C) turn would simply be wound of copper. The advantage is that the two coil method is more compact than increasing the diameter of the coil.



(a) (b)

Figure 9.14 – Two series connected coil windings with two different type of materials

However, since aluminium has a higher resistivity, it would still constitute toward a higher resistance in the coil closer to the slot opening. The disadvantage of using two coils is probably from a manufacturing point of view. It would be more difficult to place two separate coils in a slot and connect them in series.

9.6.5 *Twisting the coil*

Another improvement would be to twist the windings so the turns occupy different places within the stator slot, as shown in Figure 9.15. The advantage is that all the windings will have similar resistances and inductances.

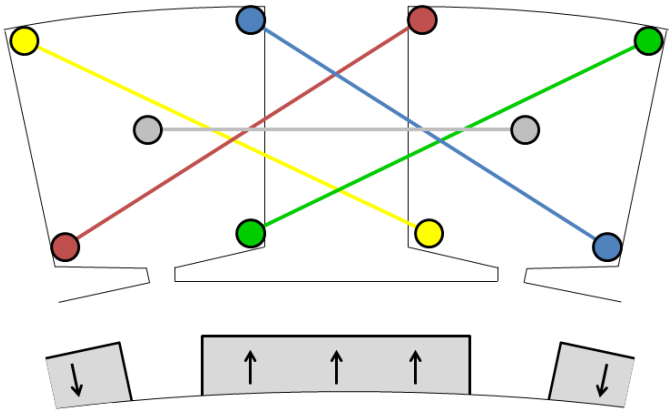


Figure 9.15 – Twisting the coil to allow the turns to occupy different positions within the stator slot

The disadvantage of such a winding configuration is that more copper is required. The end windings of most turns would have to cross the slot diagonally, thus increasing the total amount of copper used. This would mean that more winding space is required.

Another disadvantage is the method of winding. Usually a coil is wound around a tooth, and expands outwards as the number of turns increase. In the case of 211 turns per coil, it may be difficult to wind the coil as proposed. This method is probably more convenient in larger bar wound motors where the number of turns per coil is significantly lower. It would therefore be much easier to wind the motor in this manner.

9.7 Conclusion

The practical implementation results of the ELGEAR motor confirms the theory and the simulation results. This is especially the case when the single shorted turn currents are compared. The results start to diverge in post fault operation when remedial action is applied. This is due to the differences in self and mutual inductances between the 2D finite element simulation and the practical implementation.

A single shorted turn in the stator winding will result in a faulted current between 2.9 and 5 pu current. The fault should be detected within 3 seconds to avoid the fault from propagating to other parts of the coil or motor. Even though remedial action is crucial, the detection time is significantly better than other motors in the literature, where

detection and remedial action should take place within milliseconds rather than seconds. The current in the single shorted turn is only limited by the resistance since the inductance of the turn is negligible. The faulted current is therefore most significant in the turns positioned closest to the tooth where its resistance is the smallest.

The remedial action of single shorted turns is to short the terminals of the coil. The opposing flux of the coil will reduce the current in the shorted turn rated current, since the windings are closely coupled. This is not however the case for the turns located at the slot opening, where the opposing flux of the healthy coil does not completely link the faulted turn. As a result, the faulted turn will see higher currents than in the terminal shorted coil. This is not too much of a problem since the current is overrated to allow nominal operation including drag torque. There are some regions in the slot where the current does exceed the rated current. This is due to the combination of the turn having a low resistance and low inductance. This region is located close to the tooth and slot opening in the coil.

A number of improvements were proposed. An interesting improvement could be to increase the resistance of the turns at these vulnerable points in the stator slot. This could be achieved by using two coils of a different material.

General Conclusion

Chapter 10

The principle aim of the work done here was to improve the fault tolerant aerospace system. The scope of the work has been limited to two subjects in particular; the condition monitoring of capacitors in aerospace drives and the investigation of single shorted turn failures.

Both of the faults present major problems to the overall operation of the system. In the case of the condition monitoring project, dormant failures cause a systematic failure which results in disabling a drive. For a worst case turn-turn failure in the motor, overrated currents may flow resulting in high temperature gradients and fault propagation throughout the motor.

10.1 Capacitor monitoring

MPPF capacitors are popular in aerospace drives for dc-link filtering due to its inherent reliability compared to electrolytic capacitors. Nevertheless, capacitors are still regarded as the bottleneck of a fault tolerant system as they are more unreliable compared to other components. The MPPF capacitor typically fails open circuit which at first appears to be a benign fault. However, such a fault could lead to a systematic failure where all active redundant capacitors eventually fail when the fault is left undetected. Clearly, there is a need to monitor these components effectively to allow the faulty capacitor to be replaced before complete failure of the drive.

Work done in this thesis demonstrated a novel monitoring technique which was implemented on a representative high voltage test rig. A novel online condition monitoring system of dc-link capacitors in fault tolerant drives for aerospace applications was proposed. The estimation technique made use of voltage and current sensors which were already in place for protection and control purposes. The novel aspect of the proposed technique related to monitoring capacitors in real time whilst the motor was operational. No external interferences, such as injected signals or special operation of the drive, were required. The condition monitoring system is independent of torque and speed, and hence independent of a variation in load.

The results showed that the monitoring technique was 95% accurate in the worst case. The system was shown to be fast, as the detection time for a change in capacitance was recorded in the order of milliseconds. By introducing a filter, the accuracy and time response can be traded off.

The main issue related to the complexity of the monitoring system is the voltage monitor. An ac waveform has to be filtered out at PWM frequency on top of a dc value that is more than 100 times greater. A trade-off between accuracy and response time can be obtained using a digital filter.

10.2 Turn-turn faults

The fault tolerant permanent magnet motor has become an increasingly popular concept motor for fault tolerant applications in the aerospace industry due to its high torque density as well as its fault handling characteristics. The turn-turn short circuit remains a difficult fault to handle. The literature states that a single shorted turn in motors could result in extremely high per-unit currents and temperature gradients that should be detected in a matter of milliseconds.

This is, however, not the case in all motors as the single shorted turn fault depends on the machine's design parameters. In smaller motors, such as the ELGEAR motor, the resistance of a turn is much larger than its reactance. Consequently resistance is the dominant factor in suppressing the fault current in the shorted turn. The per-unit current which flows is approximately the inverse of the per-unit resistance of the machine, so typical currents of 3-5 per-unit flow in all shorted turns. In larger machines the per-unit resistance is smaller and, because there are less turns, the per-unit inductance of one turn is larger. Inductance starts to significantly influence the current in the shorted turn and, because the inductance of a turn is determined by its position in the slot, the current which flows varies between turns. The magnitude of the shorted current can be much larger – over 20 per-unit.

When remedial action takes place by shorting the coil that contains the single shorted turn, the faulted turn current is usually suppressed to the terminal shorted current value, which is typically around 0.7 per-unit in the ELGEAR motor. In some cases – depending on the position of the shorted turn within the stator slot – the current will be greater than this value. The literature highlights this as a problem, but the ELGEAR motor has the advantage that fault tolerant topology allows an additional margin (~0.3

pu) due to the requirement of drag torque in post fault operation. Nevertheless, there are still some cases where the faulted current of 1 pu is exceeded. These turns happen to suffer from a low mutual coupling as well as a low resistance. Since only a few turns exceed the 1 per-unit current, and only exceed it by a small amount, various improvements to the coil were proposed. An interesting concept proposed was a cone shaped coil close to the slot opening. This would not result in too much additional resistance of the coil, whilst effectively targeting the more vulnerable turns in the slot.

10.3 Review of objectives & contribution to knowledge

By referring to the targets in the introduction, the following was achieved:

- A journal paper on the *condition monitoring of dc-link capacitors in aerospace drives* was produced. Further details can be found in section 1.2, page 2.
- The failure mode of MPPF capacitors was analysed in the literature of this thesis. It was made clear that MPPF capacitors are the most popular dc-link capacitors in aerospace drives due to their unique self healing property, as well being more resilient to environmental changes than their counterparts.
- A novel online condition monitoring technique was successfully proposed and implemented on a representative aerospace rig. The technique merely required minor changes in the existing current and voltage sensors, which were already used for control and protection purposes. The implementation and verification of the technique was done in simulation by Matlab Simulink, low voltage implementation and high voltage implementation.
- The impact of the turn-turn fault upon the ELGEAR rig was analysed and examined in detail. Methods of analysis included finite element analysis simulation in MagNet by Infolytica, verified by implementation of the faults on a representative aerospace rig (ELGEAR). The reaction time of a turn-turn fault was compared with that in the existing literature. It is clear that although the turn-turn faults are not as severe as in the literature, they are still one of the most difficult faults to detect and handle.
- During post fault operation – when a terminal short circuit is applied to the coil – it was not always the case that the turn-turn faulted current was suppressed to its rated value. The effectively of suppression depended on the physical location of the fault within the slot. The concept of negative leakage inductance was introduced in the observations and analysis, as some of the turns appear to have

‘capacitive’ properties during post fault operation. A number of recommendations were provided for future fault tolerant design, to be able to suppress the turn-turn fault to its rated value in post fault operation, independent of the fault’s location.

10.4 Future work

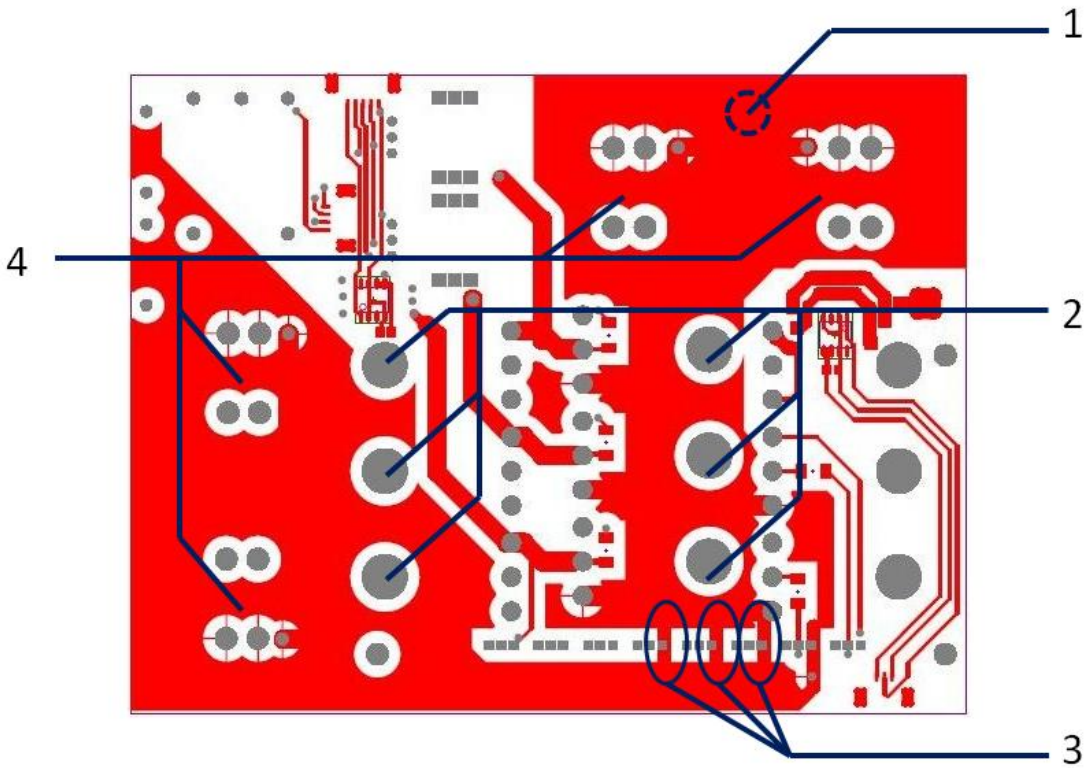
The field of fault tolerant analysis in dc-link capacitor monitoring and turn-turn faults is very large. Due and For future work, the following suggestions are made which builds upon the existing project.

- The condition monitoring project is currently a passive operating system. When a fault is detected, an alarm is tripped without providing any sort of feedback to the controller of the drive. A loss in a dc-link capacitor will place more stress on the remaining healthy capacitors, even though the healthy capacitors could be in a similar state to the faulty one (similar age, environmental exposure etc.). A future upgrade of the system would be to interface the monitoring technique with the controller. This way the controller could act upon the fault by distributing more torque to the healthy drive, thus reducing the stress on the drive where the fault took place. This could potentially avoid the accelerated process of other capacitors failing on the same drive, and could buy some time in the case where immediate maintenance is inaccessible.
- Another area for future work could be in the fault detection scheme. In general, detecting the turn-turn fault in motors with several windings in one coil is extremely difficult. Moreover, the literature does not point to one single reliable method of fault detection. One possibility would be to explore the thermal propagation of such a fault, as this would be one of the few indications of a turn-turn fault. In combination of monitoring the inverter as well as the current and voltage feedback sensors, other faults could be ruled out. This may be a method of concluding that the fault that has occurred is a single-shorted turn fault. In the past thermal tracking was not used since it was deemed to be too slow (typically in the order of milliseconds). In the analysis of the ELGEAR case, several seconds of reaction time was observed before fault propagation could potentially commence.

Appendix

A. Capacitor layout on the PCB

The dc-link capacitors are mounted on a high voltage PCB. The top layer of the PCB (Figure A.1) is connected to the zero voltage and the bottom layer (Figure A.2) to the 540V terminal.



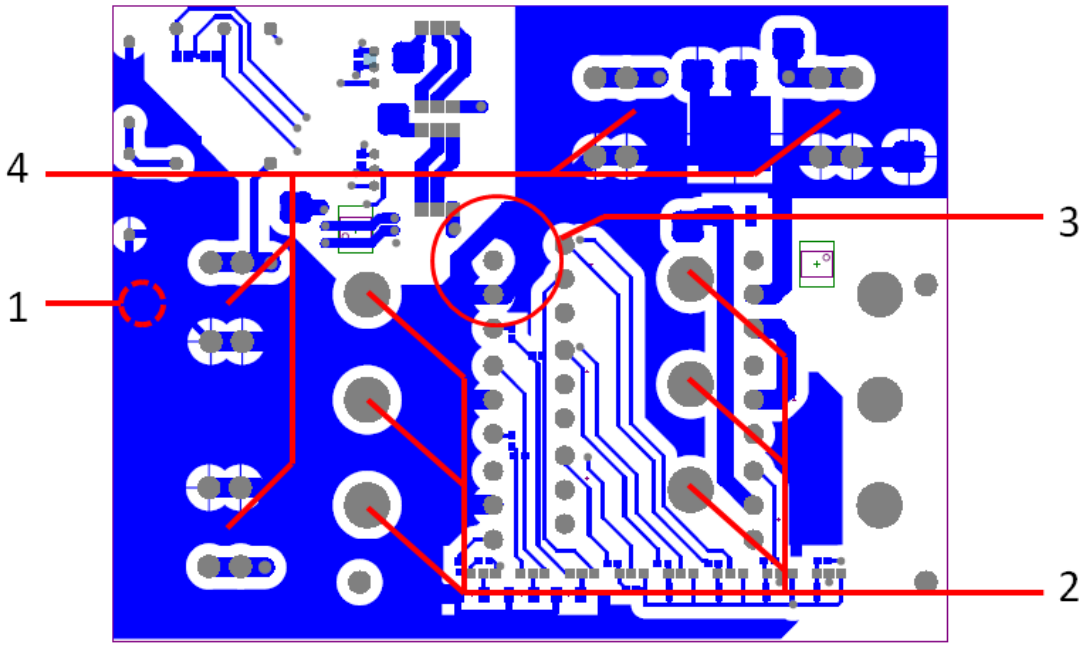
1 – Connection point to 0 V dc

2 – Positions of the 6 IGBTs

3 – Narrow gates in the flooded plane

4 – Positions of the 4 dc-link capacitors

Figure A.1 – PCB Layout top layer



1 – Connection point to 540 V dc

2 – Positions of the 6 IGBTs

3 – Narrow gates in the flooded plane

4 – Positions of the 4 dc-link capacitors

Figure A.2 – PCB Layout bottom layer

Figure A.1 shows the top layer of the PCB. The connection point from the 0 V end of the power supply is connected (via an inductor) to point (1) shown on the board. This point is a flooded plain that connects IGBTs (2) and capacitors (4). It can be seen, from point (4) that the four capacitors are spread around the board. Two of such capacitors are only connected to the negative voltage plain through a narrow gate, shown in (3).

Similarly on the bottom layer (Figure A.2), two capacitors are connected to the positive voltage plain through a narrow gate. The equivalent circuit derived for the dc-link layout is shown in Figure A.3. The narrow gates are represented as resistors.

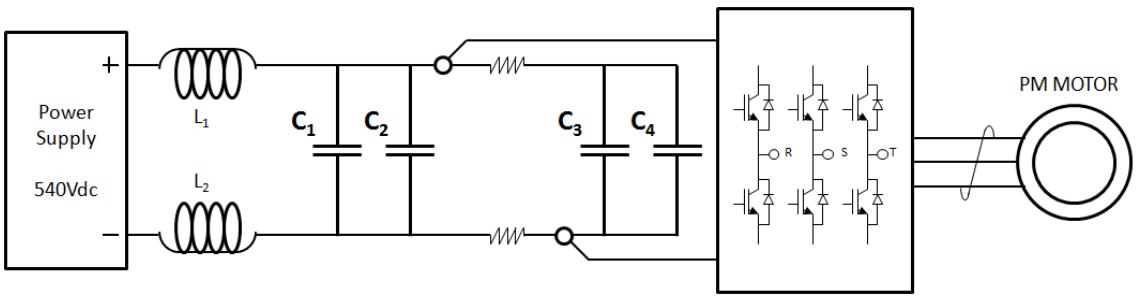


Figure A.3 – Capacitor layout

B. Electromagnetic compatibility (EMC)

To be able to successfully measure a small voltage ripple (in the order of millivolts) with sufficient accuracy across the dc-link capacitor at 540 V dc, special attention has to be paid to small signal quality. Whilst a proper ground wiring scheme is vital to reduce instrumentation noise interference, it also improves the aspects related to EMC.

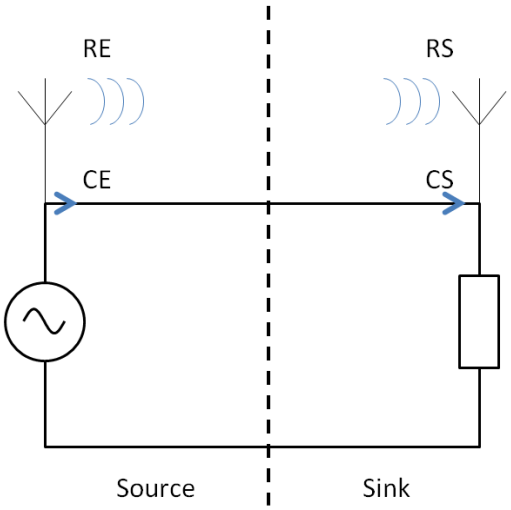


Figure B.1 – Electromagnetic interference disciplines

Figure B. shows the four electromagnetic interference (EMI) disciplines. There are two types of sources of noise; conducted emissions (CE) and radiated emissions (RE). Complementary on the receiving end, the noise interferences are referred to as; conducted susceptibility (CS) and radiated susceptibility (RS). A typical EMI specification will state the maximum boundary of each of the noise disciplines, in magnitude and frequency.

The four electromagnetic interference (EMI) disciplines are described in more detail below:

1. **Noise generated conducted emissions (CE)** – Any active electrical unit produces noise which is conducted along its electrical lines. In the case of the ELGEAR test rig, noise is generated by the high voltage dc power supply, as well as its active load (i.e., the inverter and PM motor).
2. **Noise radiated emissions (RE)** – Radiated noise emissions originate from wires or cables as a result of high frequency current components passing through them (i.e. a conductor acting as an antenna). This transmitted noise may cause interferences in other electrical instrumentation.

3. **EMC conducted susceptibility (CS)** – Any instrumentation or load is susceptible to receiving conducted noise. The instrumentation must be resilient to the CE noise frequency bandwidth and amplitude.
4. **EMC radiated susceptibility (RS)** – The same approach is taken as point 3 above, except that the receiver immunity margin should be significantly higher than the transmitter. This is due to the fact that wireless transmission levels at either ends can greatly vary depending on the frequency, medium, propagation, reflection, etc.

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