Electrical and Material Properties of Thin Film Perovskites

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“It doesn't make a difference how beautiful your guess is or how smart you are or what your name is. If it disagrees with experiment, it's wrong. That's all there is to it.”

Richard P. Feynman

Abstract

This thesis presents a study of negative capacitance in the robust perovskite $BaTiO_3$. Negative capacitance is an unstable state in ferroelectrics, which explains why there is a lack of experimental evidence in the literature. A positive capacitance in a series capacitor configuration allows stabilisation of negative capacitance. The key finding is the stabilisation of negative capacitance at room temperature in $BaTiO_3$.

Temperature constraints in back-end-of-line processing should be at 500 °C or below in order to avoid diffusion of dopants and to inhibit high resistivity silicide phases. Three deposition techniques, pulsed laser deposition, atomic layer deposition and sputter deposition are used to investigate the material and electrical properties of perovskites for back-end integration within this temperature constraint. $SrTiO_3$, $Ba_{0.8}Sr_{0.2}TiO_3$ and $BaTiO_3$ are all explored as possible solutions for tunable capacitance under low temperature processing. Evidence is shown for $SrTiO_3$ displaying fully crystallised structures through pulsed laser deposition at 500 °C growth temperature.

A refined model of effective oxide thickness is used to calculate interfacial layers that impact metal-oxide-semiconductor capacitors. The model is applied to $SrTiO_3$ metal-insulator-metal capacitors in terms of a dead layer. Calculation of the dead layer thickness, which has been previously unattainable using solely the series capacitance model, is carried out using the effective oxide thickness model. However, transmission electron microscopy images suggest that a physical layer of ‘dead’ material is abesnt in the capacitors. The results support the hypothesis of an intrinsic explanation to the dead layer phenomenon.

Finally, pulsed laser deposited $BaTiO_3$ is explored in terms of ferroelectricity when integrated with Si using $Pt/Ti/SiO_2/Si$ substrates. Here, a mixed phase relationship is shown in the films of $BaTiO_3$ in which the cubic phase, responsible for paraelectricity, dominates at room temperature. Increasing film thickness also correlates with higher remnant polarization in the films. The result confirms a size driven phase transition in thin film $BaTiO_3$ which has previsouly been studied on perovskite free-standing films or nanoparticles.

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Journals and Conferences

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Abbreviations

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BEOL	Back-End-Of-Line
BST	Barium Strontium Titanate
BTO	Barium Titanate
CMOS	Complementary Metal Oxide Semiconductor
CV	Capacitance - Voltage
CVD	Chemical Vapour Deposition
DC	Direct Current
DRAM	Dynamic Random Access Memory
EFM	Electrostatic Force Microscopy
FEOL	Front-End-Of-Line
FET	Field Effect Transistor
FRAM	Ferroelectric Random Access Memory
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors

IV	Current-Voltage
LD	Landau-Devonshire
MIM	Metal-Insulator-Metal
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PE	Polarization – Electric Field
PFM	Piezoresponse Force Microscopy
PLD	Pulsed Laser Deposition
PV	Polarization-Bias
PVD	Physical Vapour Deposition
PZT	Lead Zirconate Titanate
QV	Charge-Voltage
RF	Radio Frequency
RT	Room Temperature
RTP	Rapid Thermal Processing
SiP	System-in-Package
SoC	System-on-Chip
SRAM	Static Random Access Memory
SRO	Strontium Ruthenate

SS	Subthreshold Swing
STO	Strontium Titanate
TEM	Transmission Electron Microscopy
ULSI	Ultra Large Scale Integration
XPS	X-Ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
YSZ	Yttria-Stabilised Zirconia

Chapter 1

Introduction, Research Aims and Hypotheses

1.1 Introduction

In the past six decades, metal oxide semiconductor field effect transistors (MOSFETs) have shrunk in order to supply the demand for ever increasing circuit speeds. With the introduction of complementary metal oxide semiconductor (CMOS) technology, and the scaling of the MOSFET channel length from 1 μm to 22 nm, the CMOS industry is now into the nanoelectronics era. Transistor scaling is in adherence with Moore's law, who predicted that the number of transistors on a chip will double approximately every 18 - 24 months [1]. It is now commonplace to have upwards of billions of devices on a chip, which is at the heart of the expansion of the digital age. In the modern day, a shift has emerged where the pursuit of increasing the functionality of a circuit (more than Moore) is just as important as the scaling (more Moore).

As the MOSFET is scaled, in keeping with the more Moore agenda, the voltage supply, as well as the gate oxide thickness is also reduced [2]. A decreasing operating voltage may be beneficial for better power consumption, but problems arise when threshold voltages are too large, inhibiting the total drive current produced by the MOSFET. Furthermore, the gate oxide thickness, traditionally consisting of SiO_2, became a major issue as it reached its fundamental level in the 1990s at dimensions < 2 nm [3]. At this length scale, quantum mechanical tunnelling becomes a major factor as charge stored on the gate of the MOSFET tunnels through the thin insulator.

The difficulty in fulfilling the more than Moore agenda arises due to the limited functionality of conventional materials such as SiO_2. Silica offers very little capacitance density due to its inherent low permittivity. In addition, its capacitance stays constant when the applied voltage increases.

For both scaling and increasing circuit functionality, the incorporation of new materials has been proposed and executed. Scaling was furthered by replacing the silica gate oxide with a high dielectric constant (high-κ) material [4]. In doing so, the gate capacitance is allowed to stay at high densities with thicker film dimensions. This acts to mitigate some of the quantum mechanical effects and reduce the overall leakage of charge. Capacitors are also vital components in many circuit applications, but are relatively large. High-κ materials may also be used to offset any reduction in capacitance when the electrode area of these devices is reduced in the process of miniaturisation.

In order to achieve greater circuit functionality, materials with tunable capacitance are proposed [5]. This specific electrical characteristic of a material allows the capacitance to shift as a function of the applied voltage or electric field. Capacitance will be at a maximum at zero field, and decrease as the electric field across the insulator

is increased. The property is described through a voltage dependent permittivity, in contrast to that in silica which stays constant over the applied voltage. Applications of such a material are for hand held electronic components in microwave devices and tunable filters, among many others.

For both the aforementioned goals to increase circuit performance, perovskites offer both the high-κ, tunable characteristics for more than Moore, and the possibility of utilising negative capacitance for the more Moore agenda. The permittivity achieved in perovskite material can be three orders of magnitude greater than that in conventional insulators, which may act to shrink the large capacitance elements of an integrated circuit. Its tunable permittivity is also of keen interest for the applications mentioned above. However, perovskite thin films are known to be affected by "dead layers" which inhibit the achieved permittivity at zero bias [6-8]. Thin film forms of perovskites may therefore be limited in terms of the quality of the deposited film.

Recently, negative capacitance has been proposed in thin film ferroelectrics [9, 10]. If a ferroelectric with negative capacitance can be placed into the gate stack of a MOSFET, the required gate voltage to switch the transistor on would be lowered. This is described due to a reduction in the subthreshold swing, in which a fundamental limitation of ≥ 60 mV/dec is currently required in order to increase the drain current by an order of magnitude. The MOSFET will then achieve the same value of drive current at lower voltages. In this regard, the overall power dissipation of the chip will be reduced, leading to greater transistor packing densities and furthering the more than Moore technology track. Negative capacitance may also lead to more powerful single core processors which previously generated too much heat, causing a necessity to move to multicore processors. However, experimental evidence of negative capacitance in barium titanate, particularly at room temperature, has never been observed. This is

critical if the material is to be used in current state-of-the-art transistors incorporated with Si.

1.2 Research Objectives and Hypotheses

The overall goal of this thesis is to investigate the characteristics of thin film perovskites for the nanoelectronics industry. Since Si is the workhorse material in most electronic devices, nanometer scale perovskite thin films grown on Si are an important advancement. A range of deposition techniques and growth parameters must be used and understood if the films are to be grown at a high standard. Use of a variety of characterisation techniques is also essential in order to assess the quality of the grown films. High quality perovskite thin films that offer a wide variety of characteristics is therefore a general aim of the thesis.

The key property of ferroelectric negative capacitance is investigated in thin film barium titanate, and a model is used to show its existence at room temperature. The model involves a series capacitance system of a positive and negative contribution, as negative capacitance under normal circumstances is unstable. It is shown that negative capacitance is stabilised, resulting in an overall enhancement of the total capacitance, which would never be observed in a standard series configuration of two positive capacitors. The model is developed using Landau theory for ferroelectrics, and guidelines for the designs are presented.

For high density capacitors integrated in the back-end of an integrated circuit, growth temperature is of critical importance. At a temperature exceeding 500 °C, high resistive silicide phases, such as $NiSi_2$, can be created and disrupt circuit performance. As such, growing high quality ferroelectric thin films at 500 °C or below is a key issue if the films are to be incorporated with Si chips in the back-end-of-line. In contrast, front-end-of-line processes can be deposited at temperatures greater than 1000 °C, and is where a negative capacitive layer would be situated. There is a lack of evidence in the literature that addresses low temperature deposition of ferroelectric films, with the

majority of studies focusing on high temperature growth. Investigation into the perovskites, strontium titanate, barium titanate and barium strontium titanate are shown using three different growth methods. The results indicate that growth technique, as well as thermal treatment with regards to annealing or temperature during growth, is important when film crystallisation is required. The results also show that the concentration of Ba impacts the crystallisation temperature considerably. In order to achieve thin films with high-κ and tunable characteristics, strontium titanate grown at 500 °C using pulsed laser deposition (PLD) is the most successful technique applied.

Calculating the equivalent oxide thickness (EOT) is a well-known method for gauging the effectiveness of a high-κ material, but problems may arise in the analysis if interfacial layers are apparent. It is shown that the standard equation for EOT is unsuitable if such an interfacial capacitance is in series with the desired insulator. The EOT model is developed to take into account any double layer capacitances that may arise in MOS gate stacks, and is shown to be suitable for calculating the thickness of the interfacial layer. The results are similar to that of dead layers affecting high-κ perovskites, and the model is applied in order to calculate the actual thickness of dead layers acting upon strontium titanate capacitors integrated with Si. Further analysis is shown using high-resolution electron imaging of the metal-insulator-metal (MIM) interfaces. The tunable capacitance of the strontium titanate film is investigated in terms of the effective dead layers.

Finally, high temperature growth of barium titanate using PLD and integrated on Si substrates was investigated in terms of its retainable polarization and hysteresis. The ferroelectric properties of barium titanate integrated with Si substrates are important if the material is to be used as a negative capacitive layer. It was found that the achieved remnant polarization is minimal at the film thicknesses and temperatures

studied. Further analysis using a range of electrical and material experiments supports a hypothesis of a mixed phase relationship in the polycrystalline barium titanate films, where a cubic phase is dominating. The cubic unit cell of a perovskite is responsible for the paraelectric phase, and as such lacks the ability to retain polarization. The inherent lack of polarization retention and switching negates the films to be used as a negative capacitance layer.

A summary of the main hypotheses of this thesis is presented below:

1. Barium titanate displays effective negative capacitance. If the perovskite is stabilised in a series capacitance system, the total capacitance of the bilayer is larger than the constituent positive capacitance in the series.
2. Perovskite insulators may be crystallised at 500 °C for the purpose of back-end integrated circuitry.
3. A physical layer of 'dead' material is evident in high-κ nanocapacitors. The dead layer will exhibit contrasting regions from the bulk of the perovskite in high resolution imaging.
4. Barium titanate films integrated with Si substrates achieve remnant polarization in the order of ≥ 10 $\mu C/cm^2$.
5. A barium titanate thin film integrated with a Si substrate is affected by the size driven phase transition, which is known to impact bulk ferroelectric material.

The above hypotheses will be studied in chapters 4 through 6, and conclusions will be drawn in chapter 7.

Ferroelectrics are discussed in chapter 2, with particular attention placed upon Landau theory for the designs of negative capacitance stabilisation in bilayer structures. Chapter 3 will turn the attention to the fabrication methods and structures that were used in order to study thin film perovskites. The three main deposition

techniques were sputter, pulsed laser and atomic layer deposition. The characterisation techniques are also explored.

In chapter 4 evidence for negative capacitance in barium titanate at room temperature is presented. It offers the first experimental observation of this phenomenon in barium titanate at room temperature.

Chapter 5 explores low temperature deposition of strontium and barium strontium titanate films grown using PLD for integration with Si. In addition, strontium titanate is investigated using atomic layer deposition and low temperature rapid thermal processing. Pure barium titanate is also discussed in terms of sputter deposition and post deposition annealing.

Chapter 6 studies the EOT of high-κ films, which is developed to take into account any unwanted interfacial layers created in the thermal treatment of a capacitance structure. The model is then used to investigate dead layers in high-κ perovskites, and a thickness is calculated for the dead layer. High temperature growth of barium titanate on Si substrates is investigated in terms of the displayed ferroelectricity. Finally, chapter 7 concludes and summarises the study, and suggests future work.

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Chapter 2

Ferroelectrics and their Incorporation into the Si Industry

2.1 Introduction

Well before the discovery of ferroelectrics, pyroelectric, and following this piezoelectric, material were known and understood [1]. Pyroelectricity is the phenomenon of a material to possess a temperature dependent spontaneous electric dipole moment, while piezoelectricity generates dipole moments under the application of strain. Following this in 1920, Valasek discovered the first ferroelectric known as Rochelle salt. The key property defining the ferroelectric material over both piezo and pyroelectricity is the ability to reverse the direction of the electric dipole moment with the application of an electric field [2]. However, ferroelectrics remained simply a curiosity for study until the discovery of the more robust perovskite oxide barium titanate ($BaTiO_3$) in 1943 [3]. The simplified structure of this material allowed a

detailed understanding of ferroelectrics, which paved the way for its inclusion in the Si industry as $BaTiO_3$ insulated capacitors.

A number of key studies were published on the uncommon properties of $BaTiO_3$, some of which included connecting its crystal structure to the dielectric characteristics [4] and investigating the electric domains in the material [5]. Initially the electric domains were not well understood, which caused the ferroelectric properties to remain elusive until the 20th century due to zero net polarization in single crystals. Thus, it was not until the 1980s where the full scope of the material was realised; ferroelectrics were now being grown in thin film form for incorporation into semiconductor chips [6].

The main advantage of thin film ferroelectrics lie in the application of the voltage supplied from any hand held electronic device. A bulk ferroelectric of possible thickness 1 mm will require a 5 kV voltage supply to reach a specific switching field of E = 50 kV/cm, known as the coercive field. At this field the polarization is reversed and the dipoles align in the opposite direction. This required voltage is of course unsuitable for any of our modern day electronics. Thin film ferroelectrics with nanometer dimensions allow the coercive field to be attained at voltages used in modern integrated circuits. Therefore, ferroelectrics can now be incorporated into the nanoelectronics industry.

A substantial role for ferroelectrics, and in particular $BaTiO_3$, is memory based applications, with a detailed text on ferroelectric memories published in 2000 [7]. While the topic of memory is rather in depth, the main feature of ferroelectrics for this application is its ability to retain a bulk electric polarisation, and therefore is best suited to non-volatile ferroelectric random access memory (FRAM).

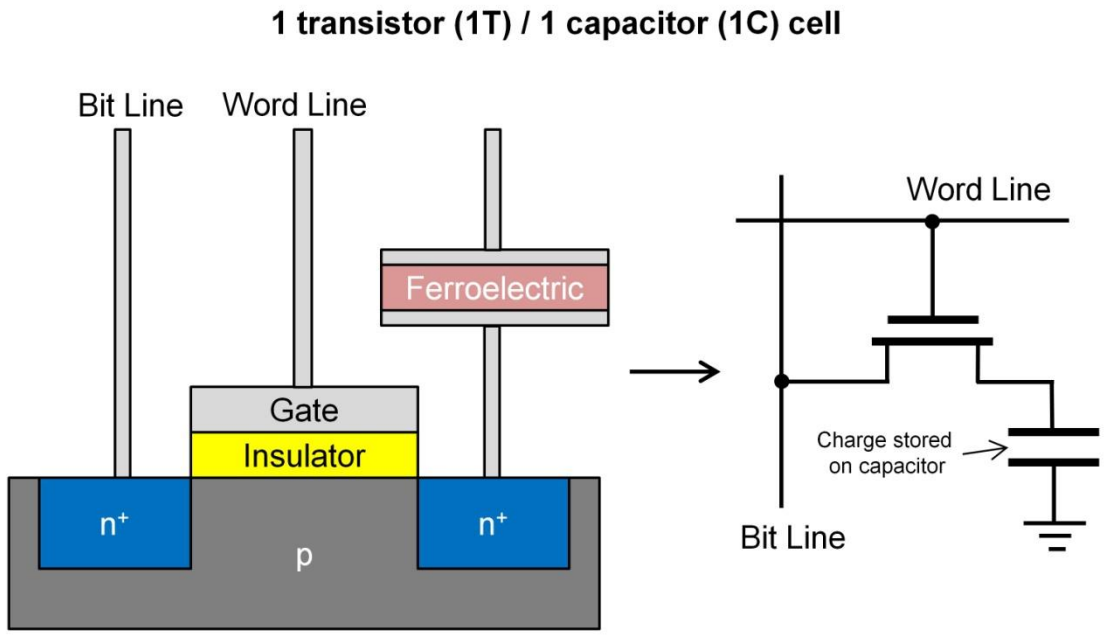

Figure 2.1: Schematic of the 1T/1C FRAM cell utilising ferroelectrics. Equivalent circuit shown as the transistor and capacitor connected to the word line and bit line, respectively.

Figure 2.1 highlights a well-established use of ferroelectrics in FRAM: a 1 transistor (1T) / 1 capacitor (1C) cell. The operation is similar to dynamic RAM (DRAM); however in this instance the ferroelectric capacitor is charged and retains its polarity. The polarity of the ferroelectric capacitor represents the digital logic state 1 or 0 such that it does not need to be continuously refreshed between read or write cycles. A detailed study on the use for ferroelectrics for non-volatile memory is given in ref. 8.

In the modern day, ferroelectrics are being studied and investigated for a number of different applications. A 2007 review of the applications of modern ferroelectrics is given in [9]. Some of the highlighted directions for ferroelectric research in the study are: substrate/film interfaces, high strain states, magnetoelectrics, phased-array radars, electrocaloric cooling, among others, which are beyond the scope of this thesis. However, the relevance of the depth of research that ferroelectrics have attracted is underlined.

Further to the above mentioned applications, $BaTiO_3$ has attracted attention due to its possible negative capacitance property. Salahuddin and Datta initially proposed the inclusion of a ferroelectric material with negative capacitance as a substitute into the gate stack of a MOSFET in order to reduce the subthreshold slope [10, 11]. Negative slopes in polarization-electric field hysteresis loops, indicating a negative capacitance property, were also shown in $BaTiO_3$ [12]. The study highlights the likelihood of ferroelectric materials possessing a negative capacitance property. However, if $BaTiO_3$ is to be used in a front-end transistor process for reducing the subthreshold slope, further experimental evidence is needed to support the negative capacitance hypothesis.

The subthreshold slope of a MOSFET is an important characteristic that describes the transition from its off to on state. A steeper slope shows that a lower voltage is required to saturate the transistor. However, using conventional insulators, and even high-κ material, there is a fundamental lower limit on the gate voltage that is required in order to increase the current by an order of magnitude. This is commonly referred to as the subthreshold swing, and at its minimum is 60 mV/decade at room temperature. The use of negative capacitance may surmount this roadblock, and reach values < 60 mV/decade. A reduced subthreshold swing past the ‘fundamental’ limit enables the switching energy of the transistor to be lowered, in turn mitigating some of the self-heating issues attributed to modern state-of-the-art integrated circuits. Negative capacitance may, therefore, aid in the pursuit of greater packing densities on a chip, and prolonging the lifetime of Moore's law. Equal drive currents may also be obtained at smaller supply voltages, which is a key area of interest for an integrated circuit for low power applications and increasing battery life.

However, the necessity of thin films for the nanoelectronics industry does not come without limitations. Bulk forms of ferroelectrics differ substantially in their electrical and material properties when compared to a thin film counterpart. Reduced permittivity and retainable polarization is common in thin films, and chosen substrates will impose a microstructural change which is otherwise absent in powdered ferroelectric material.

The aim of this chapter is to describe ferroelectricity, particularly in a perovskite, and develop Landau theory in terms of the negative capacitance model. The differences between thin film and bulk forms of ferroelectrics are discussed, such as dead layers. A review of current state-of-the-art ferroelectric films is shown from the literature. Finally, an overview of the nanoelectronics industry is given.

2.2 Ferroelectricity

2.2.1 Piezo/pyroelectricity and ferromagnetic comparisons

The name ferroelectric is a misnomer and does not indicate any iron in the material. It is derived from the similarities with ferromagnetism, which displays hysteretic properties due to its internal magnetic domains. A ferroelectric, therefore, displays electrical hysteresis, and domain structures consist of aligned electric dipole moments. This was first highlighted in Rochelle salt as displaying similar properties to magnetic hysteresis shown in the case of iron [2].

Ferroelectrics are both piezo and pyroelectric due to their polarization dependence on strain and temperature; however, the reverse is not true. A ferroelectric crystal should have two or more polar states in the absence of an electric field, and

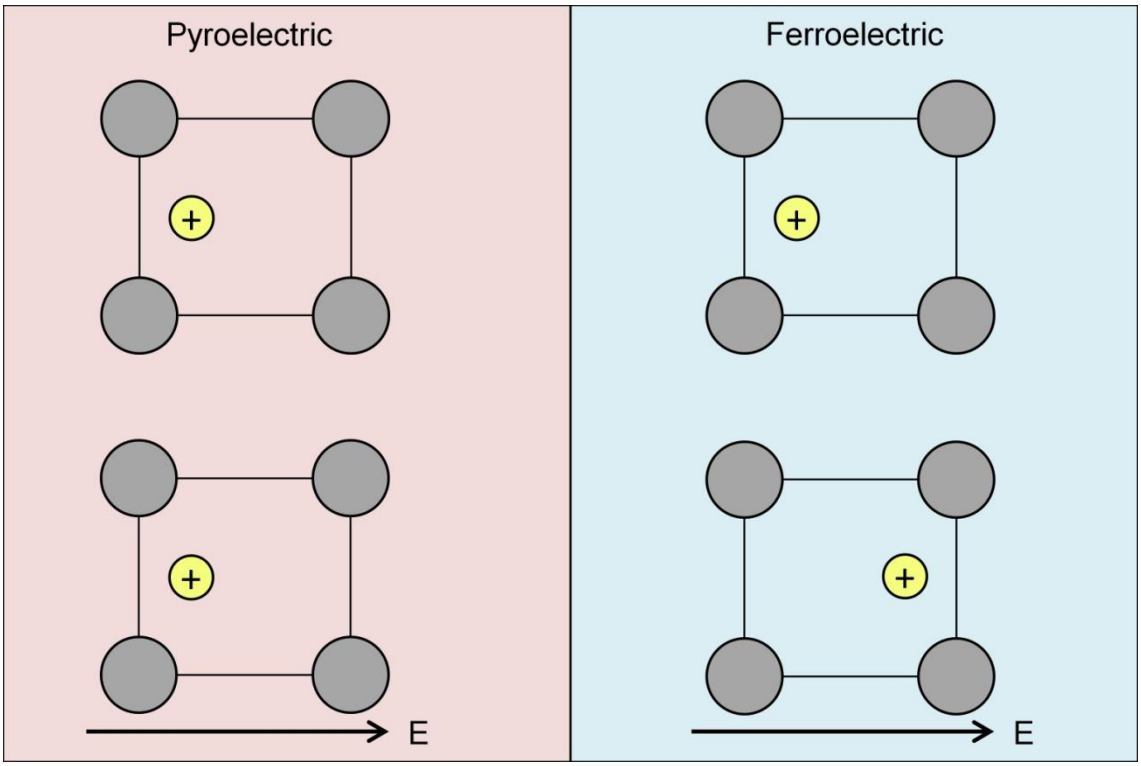

Figure 2.2: Pyroelectric and ferroelectric crystals are highlighted retaining their polar state. Application of an electric field switches the charge state in the ferroelectric, with the pyroelectric state remaining unchanged. Ferroelectrics are a subgroup of pyroelectricity (in addition to piezoelectricity) with this important switching characteristic.

have the ability to reverse between these states with the application of an electric field (figure 2.2). This is a key property that defines a material as ferroelectric and describes the reversible polarization in the material, where polarization is defined as a surface charge density.

The impact of switching polarization, P, with an applied electric field creating ferroelectric hysteresis, and also a comparison to a ferromagnetic hysteresis loop, is shown in figure 2.3. Also shown in the figure is the internal domain structure of the ferroelectric or magnetic material. A domain is defined as a uniform direction of either magnetic or electric moments in which the vectors associated with the dipoles are parallel. The internal magnetic domains consisting of the dipole moments in the ferromagnet are initially randomly oriented at zero magnetic field (figure 2.3 (a)). Applying an external magnetic field acts upon the domain structure within the material, shifting the dipoles towards alignment. As the individual domains begin to align, the magnetization increases and reaches saturation. Once the magnetic field is removed the ferromagnet retains a considerable amount of its magnetization as the domains do not revert back to their initial disordered state. If the magnetic field is reversed in direction, the magnetization is also reversed as the domains are ordered in opposite directions. The direct analogy to ferroelectricity is apparent in figure 2.3 (b), whose characteristic is showing the dependent nature of polarization on electric field. For the ferroelectric, an applied electric field acts upon electric dipole moments, whose alignment creates an electric domain. The resulting outcome is spontaneous polarization at the saturated point, and remnant polarization when the electric field is removed. The remnant polarization was described as representing the digital logic state 1 or 0 in figure 2.1. The remnant polarization P_r is reversed at a coercive field $-E_c$ in a ferroelectric, and the retained polarization in this regard will be $-P_r$ once the electric field is removed.

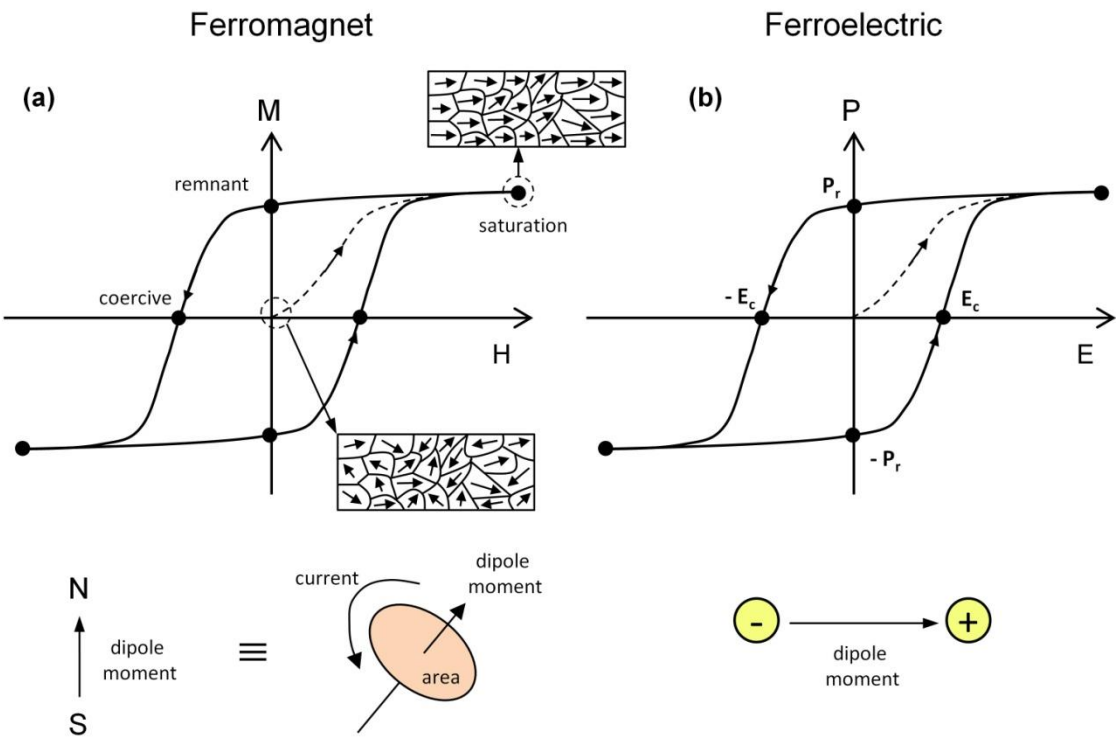

Figure 2.3: Illustration of the hysteretic nature of ferromagnetism (a) and ferroelectricity (b). As the field in each case is increased, the domains align through the force applied on the individual dipole moments, reaching saturation at high field. Removal of the field retains domain alignment, shown as a remnant polarization P_r for ferroelectrics. Reversal of the field switches the vector directions associated with the domains at the coercive point, E_c for the ferroelectric. Also shown is the magnetic and electric dipole moment, defining the properties in each case.

2.2.2 Domains

As described above, a domain in a ferroelectric crystal is a physical region with a uniform direction of electric dipole moments. For the case of $BaTiO_3$, which is described in detail in the following section, the Ba^{2+} and Ti^{4+} ions are shifted towards neighbouring O^{6-} ions. The relative shifting of the ions creates the electric dipoles within the crystal. A uniform domain would result if the Ba^{2+} and Ti^{4+} ions are displaced in equivalent directions toward the O^{6-} ions. At the boundary of each domain are domain walls, following from the analogy to ferromagnetism. However, in the case of ferroelectrics, domain walls are sharp transitions in polarization direction spanning

only 1 - 10 unit cells [13]. In the case of applying electric fields to switch polarization in a ferroelectric, the process can be regarded as the movement of domain walls, in turn reorienting the electric dipoles.

For a freestanding ferroelectric single crystal, where the surface bound polarization is not compensated by free charges on the plate of any electrode, an electric field will be induced anti-parallel to the polarization, known as a depolarizing field [1]. The energy resulting from this field can drive a shift in the domains in order to minimize the free energy of the system associated with the surface charges. The domain walls will reorient and the ensuing domains will be anti-parallel, which minimises the surface charges on the plane of the crystal. This process of free energy minimisation due to the induced depolarizing field can severely degrade ferroelectricity, and has been reported as one of the causes for dead layers in thin film capacitors [14]. Dead layers cause suppression of permittivity and reduced ferroelectricity in nanometer scale devices. Further discussion relating to dead layers is given in section 2.2.4. Even in the case of ferroelectric capacitors with electrodes, a lack of compensation of the surface polarization charge to the free charges on the electrode can lead to the creation of a depolarization field. Only in the case of a fully compensated bound polarization to free charge at the ferroelectric/electrode interface will the single domain state be energetically favourable [13]. Therefore, a keen interest of study is on electrode engineering in order to limit any depolarizing fields associated with degrading the ferroelectric properties.

2.2.3 Bulk and thin film ferroelectrics

The application of ferroelectrics in the nanoelectronics industry demands that thin films are necessary. However, there are variations in the properties of thin film ferroelectrics over a bulk counterpart. Figure 2.4 encapsulates some of the key differences between bulk and thin film ferroelectrics in which the permittivity response versus temperature is shown [4, 16]. Figure 2.4 (a) describes a bulk ferroelectric crystal of $BaTiO_3$, and a maximum peak in the permittivity is seen at approximately 120 °C, known as the Curie temperature. A description of permittivity decreasing as the temperature is increased past the Curie temperature is known as the Curie-Weiss law, given by

$$\chi = \frac{C}{T - T_c} \tag{2.1}$$

where χ is the dielectric susceptibility, T is the operating temperature, T_c and C is the Curie temperature and constant, respectively. The Curie temperature is typically just below a critical temperature [13], which delineates a phase transition in a perovskite crystal. Beneath the critical temperature the perovskite is tetragonal and retains

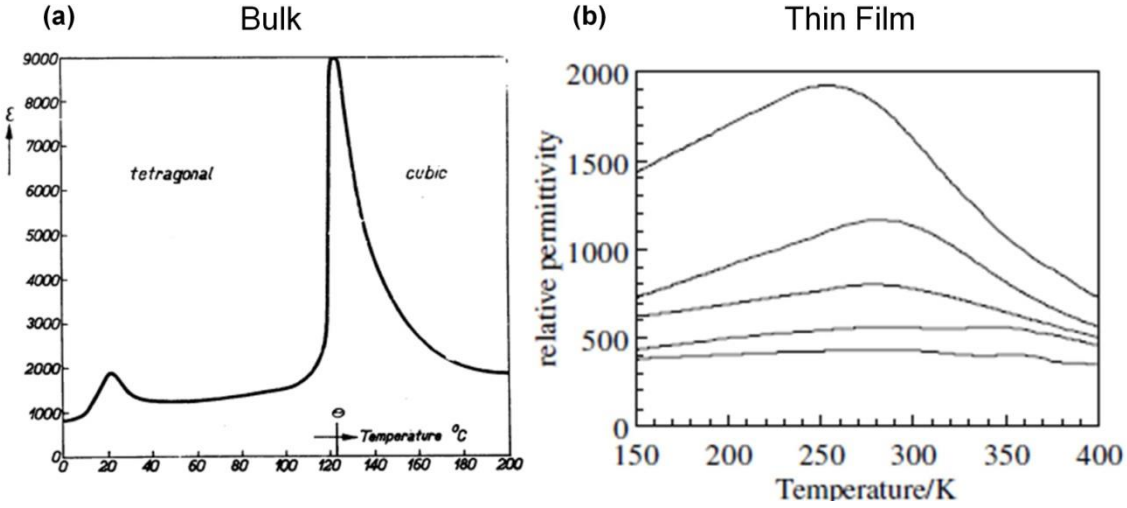

Figure 2.4: Permittivity response measured as a function of temperature in a bulk $BaTiO_3$ (a) (image taken from ref. 4) and thin film $(Ba_{0.5}Sr_{0.5})TiO_3$ (b) (image taken from ref. 16). The thin film maximum permittivity increases as a function of film thickness, starting from 175, 280, 340, 660 and 950 nm.

spontaneous polarization. The spontaneous polarization can be reversed using an external electric field (figure 2.3). However, above the critical temperature, the crystal is cubic and no longer retains its bulk electric polarisation in the absence of an electric field. The properties of each perovskite crystal phase are discussed in detail in section 2.2.5.

For comparison, thin film permittivity response is given in figure 2.4 (b) for $(Ba_{0.5}Sr_{0.5})TiO_3$. The results show a lack in peak permittivity, which diminishes further with a decreasing film thickness. In addition, the highest achieved permittivity is lower than that shown in figure 2.4 (a). The smearing of the peak makes analysis on the phase transition of a ferroelectric difficult. The apparent shift also means that the Curie temperature shifts with film thickness. Chapter 6 explores detail of a mixed phase relationship in thin film $BaTiO_3$ with regards to a shift in the Curie temperature.

Further to electrical boundary conditions described in the previous section in terms of domain configurations, mechanical boundaries are also influential in thin film forms of ferroelectrics. For example, in a film which is mechanically clamped to a substrate, strain is developed depending on the lattice parameters and thermal expansion differences between the two materials. The energy associated with the strain can also cause a shift in domain formation from what is expected in a bulk, freestanding ferroelectric crystal. Certain substrates will produce different electrical properties due to the induced mechanical boundary conditions. It is therefore important to consider and address the impacts that a substrate has on the design of a ferroelectric capacitor. A detailed study given by Pertsev *et al.* shows the impact on the phase diagrams of $BaTiO_3$ as a function of the imposed misfit strain [15]. The work becomes relevant in the design of the negative capacitance structures in chapter 4.

2.2.4 Dead layers

When the thickness of a thin insulating film decreases, its permittivity also decreases [14]. The phenomenon is not described when the standard equation for a single layer insulated capacitance is considered, and the reduction in permittivity has been expressed as a series capacitance configuration. The reason for this was originally thought to be due to a 'dead layer' at the insulator/electrode interface which acts in series with the bulk of the film. The electrical properties showing decreasing permittivity with film thickness is well described through the series capacitance model. However, it stipulates that a secondary material is present in the capacitor.

Previous studies have shown evidence of a distinct region of material that differs from the bulk of the insulator. Explanations to the origin of the secondary material were due to: inter-diffusion or reaction at interfaces [17], several nanometer layer at the interface due to diffusion of Pt [18], 3 nm thick fully strained region [19] and amorphous interfacial layer [20]. However, a range of other studies do not show any evidence of a physical or distinct dead layer [21 - 27].

Intrinsic influences leading to an explanation of the dead layer effect have also been explored, which explains why many studies have not shown evidence of a physical interfacial layer. A study by Black and Welser introduced the concept of a finite screening length in electrodes [28]. The electrons within the electrode are not arranged in an ideal delta function at the boundary of the electrode/insulator due to a combination of electron repulsion and their wave-like properties. The compensating charge then screens the bound polarization charge over a certain length within the electrode and, as a consequence, the applied electric field penetrates into the electrode. The penetrating electric field removes some of the voltage that would otherwise have been dropped across the insulator. In addition, the charge separation between the

compensating and bound polarization charge inherently adds a capacitive contribution in series with the bulk expected capacitance of the insulating layer. The concept supports the series capacitance model that is shown to accurately describe the dead layer effect. Furthermore, a study in ref. 29 discusses the impact of Ti and O inter-diffusion into the electrode and its resulting effect on the interfacial capacitive contribution to the series. The high polarizability of these ions can increase the achievable permittivity of the electrode, in turn increasing the capacitance of the electrode and reduce the dead layer effect. The result is a combination of an intrinsic case, resulting from the screening length of the compensating charge, with an extrinsic contribution from the diffusion of ions during deposition. Careful control of the thermal treatment of the capacitors during growth may inhibit some of the diffusion leading to dead layer effects.

A further intrinsic case that would be otherwise absent in electron microscopy imaging of the electrode/insulator interface is the depolarizing field. Depolarizing fields were previously discussed in section 2.2.2 in terms of free standing ferroelectric material without electrodes. If the compensating charge in the electrode does not fully screen the bound surface polarization charge of the insulator, an electric field is built across the insulator anti-parallel to the applied electric field. The result would be an overall reduction in the polarization of the insulator. Section 2.2.6 describes polarization and its proportionality with permittivity, however a reduction in polarization will lead to a reduction in the achieved permittivity in the insulating film. The overall result of depolarizing fields is that an insulator will show a suppressed permittivity, which is evident in thin films.

In either of the intrinsic cases, a reduction in film thickness increases the bulk capacitance. The increase in bulk capacitance when film thicknesses are now

nanometer scale in length ensures that this capacitance is comparable to the fixed interfacial capacitance. The result has led to the widely reported decrease in permittivity as the film thickness reduces into the nanoscale. It was previously not observed in thicker films as this bulk capacitance was the much smaller contribution in the series capacitance configuration.

A study in ref. 14 shows the impact of both the screening length in electrodes and depolarizing fields in *ab initio* calculations, which results in a total capacitance density of 258 fF/um^2, reduced from an expected 1600 fF/um^2 expected of the $SrTiO_3$ layer without the intrinsic dead layer influences. However, they propose that electrodes such as Pt should show minimal contributions to the finite screening lengths and depolarizing fields due to the high density of electrons in this metal. This is not the case in experimental studies with Pt used as the electrodes for high permittivity material [29, 30]. It is proposed that defects and inter-diffusion play an important role when using electrodes such as Pt [29]. Conducting oxide electrodes such as $SrRuO_3$ offer superior and ultra-flat epitaxial properties when used with other such materials ($SrTiO_3$, $BaTiO_3$, etc.) [14]. This will limit the interfacial capacitance contribution as the electrode/insulator interface approaches ideal infinitesimal thicknesses, and sharp boundaries between the insulating and conducting material are achieved. Chapter 6 explores dead layers in $SrTiO_3$ / Pt structures in a series capacitance model. A re-modelled effective oxide thickness equation allows extraction of a dead layer thickness to investigate the origins of any physical dead material. Furthermore, chapter 4 shows high resolution electron imaging of epitaxial $BaTiO_3$ grown on $SrRuO_3$ electrodes where sharp interfaces are evident.

2.2.5 Perovskite ferroelectrics

In the above description of ferroelectrics, the key property of the material is its ability to retain, and further reverse polarization with an electric field. Originally, this property was only seen in hydrogen bonded materials, and had little application due to their fragility. It was the discovery of the perovskite which changed what was thought possible with materials possessing ferroelectricity.

A perovskite is a material whose chemical formula is ABO_3, where the cations A sit on the corners of a unit cell and B is positioned in the centre, with remaining O anions surrounding B in an octahedral configuration. A range of different properties can be obtained depending on the composition of the ions in the perovskite; for example, metallic or insulating, Curie temperature tuning and many others.

Figure 2.5 shows schematically the perovskite of $BaTiO_3$ in which A represents Ba^{2+}, and B Ti^{4+}. An important property of the perovskite is the ability to change in phase at the Curie temperature. As described in equation 2.1, above the Curie temperature the material is cubic, which is the structure of the high temperature paraelectric phase. In this cubic phase the lattice constant ratio of the perpendicular and in-plane parameters, c/a = 1. Due to the higher operating temperature, the increased thermal energy is enough to overcome the long-range Coulomb forces between the dipoles, ensuring the Ti^{4+} ion is positioned at the centre (figure 2.5 (a)). In this form, the unit cell is centrosymmetric and non-polar such that it does not display any polarization retention or reversal due to the higher symmetry state of the crystal. However, the paraelectric phase does display a non-linear polarization response to an applied electric field, with much higher permittivity over conventional high-κ materials.

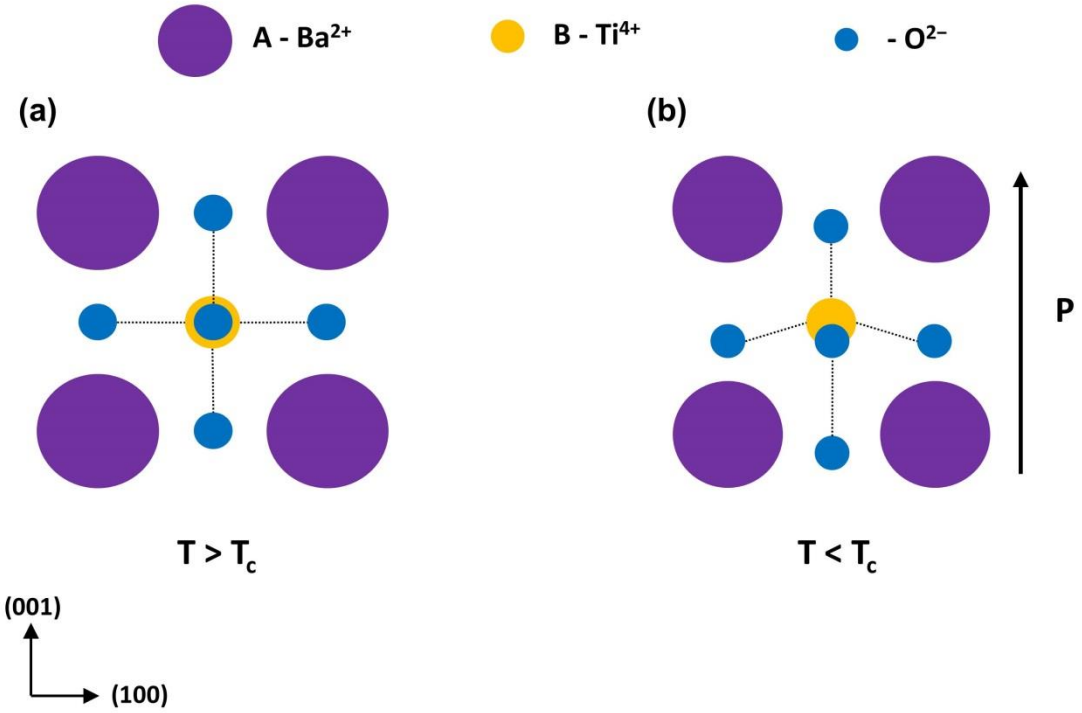

Figure 2.5: Schematic of the unit cell of a perovskite material $BaTiO_3$. The paraelectric phase is situated at temperatures above T_c where the unit cell is cubic (a). For the ferroelectric phase, temperatures lower than T_c induces a deformation along one of the axes and the unit cell is tetragonal, creating a permanent dipole with remnant polarization as shown (b).

Upon cooling the perovskite below T_c the ferroelectric phase is induced. The reduced thermal energy enables the creation of electric dipoles, in which the positive and negative ions shift relative to each other. The phenomenon is dominated by the displacement of Ti^{4+} towards its neighbouring O^{2-}. The broken symmetry of the system creates a tetragonal distortion into the unit cell (figure 2.5 (b)). In this instance the lattice constant ratio of the perpendicular and in-plane parameters, c/a > 1 (c/a = 1.07 for $BaTiO_3$ shown in chapter 4). Dimensionally, there is an elongation along one of the crystal axes, which dictates the direction of the resulting polarization. For the tetragonal phase, the polar c-axis is aligned along [001]. The cooperative phenomenon and alignment of the electric dipoles results in ferroelectricity displayed in the perovskite. The aligned dipoles along the polar axis lead to spontaneous polarization, and reversal

of any applied electric field acts on the relative displacements of the ions, switching the direction of polarization.

In addition to the cubic to tetragonal distortion, there exists two remaining transitions as the temperature is cooled further. The first is the orthorhombic symmetry and remaining transition is the rhombohedral phase. Each polar axis in the ferroelectric phases is aligned according to [001], [110] and [111], for tetragonal, orthorhombic and rhombohedral, respectively. Further details on the lower symmetry phases are given in refs. 13, 31. For the case of this thesis, the two key distortions are the cubic and tetragonal phase, and will be the subject of the following results chapters.

There exists a tolerance factor, *t*, which defines the type of distortion during the phase transition from paraelectric to ferroelectric [31]. Describing the ionic radii of the elements in the perovskite, the tolerance is given in equation 2.2

$$t = \frac{r_A + r_O}{\sqrt{2}(r_B + r_O)} \tag{2.2}$$

where r_A, r_B, r_O, are the radii of the A, B and O ions, respectively. When *t* is unity, the requirements for the formation of the perovskite are satisfied and all ions are close-packed and in contact. Increasing *t* such that $t > 1$, the framework set by the A-O arrangement creates an interstitial too large for the occupancy of the B ion. In this regard, a phase transition from cubic to tetragonal phase will lead to polar distortions of the ions, described above for a tetragonal deformation. This case is known to occur in perovskites such as $BaTiO_3$, whereby the Ba-O cage is too large for the Ti^{4+} cation, and the relative shifts of the ions act to reduce the cavity size within the unit cell. For the case of $t < 1$, a rotation and tilting of the oxygen octahedra is apparent. For perovskites such as $SrTiO_3$, in which the Sr ionic radius is smaller than that for Ba, this tilting and rotation occurs at the phase transition temperature, creating an anti-ferroelectric phase. For the remainder of this thesis, $BaTiO_3$ and $SrTiO_3$ are operated at temperatures

inducing the cubic phase for $SrTiO_3$, and either the cubic or tetragonal phase for $BaTiO_3$, as equation 2.2 describes. Further details on the anti-ferroelectric phase are given in [1, 13].

2.2.6 Electrostatics relating to capacitance

The main advantage for incorporating ferroelectric perovskites into the nanoelectronics industry is the electrical characteristics they exhibit. When compared to the traditional SiO_2 insulator, they offer wide ranging properties: ultra-high-κ, tunability through a voltage dependent permittivity, retainable and reversible spontaneous polarization and the more elusive negative capacitance. In order to describe the electrical properties of these materials, the electrostatic equations are now given. A comprehensive description of the background to electrostatics is given in [32] and is used for the purpose of this section.

The following analysis is based upon perovskites as insulating materials in parallel-plate capacitor structures. The charge, *Q*, on a capacitor is related to the applied voltage, *V*, as

$$Q = CV \tag{2.3}$$

Capacitance, *C*, can be derived using Poisson's equation for the charge density, ρ,

$$\frac{\partial^2 V(x)}{\partial x^2} = \frac{\rho}{\varepsilon_o} \; ; \; \rho = 0 \tag{2.4}$$

assuming *V* only varies in one dimension and neglecting fringing fields. Here, ρ is zero as no free charge exists between the plates. The equation then reverts to Laplace's equation. The solution is a function of the voltage with distance x across the capacitor

$$V(x) = \frac{V_1}{t_{ox}} x \tag{2.5}$$

where t_{ox} is the plate separation and V_1 the applied voltage. The electric field is now evaluated using the following expression

$$E = -\nabla V(x) \tag{2.6}$$

From equations 2.5 and 2.6 the magnitude of the electric field through the capacitor is $E = V_1 / t_{ox}$. The charge is calculated using Gauss's law over the surface area of the electrode

$$Q = \iint D \cdot \overrightarrow{dS} \tag{2.7}$$

where $\overrightarrow{dS}$ represents a vector normal to the plate and D is a displacement field relating the material permittivity ε and electric field E, $D = \varepsilon E$. Analysis of equation 2.7 gives a relationship for the charge on the surface area of the electrode A, $Q = DA$. Substituting the relationship for D and the electric field, charge is calculated to be

$$Q = \frac{\varepsilon A}{t_{ox}} V \tag{2.8}$$

From equation 2.3, it follows that capacitance is defined as

$$C = \frac{\varepsilon_o \kappa A}{t_{ox}} \tag{2.9}$$

where $\varepsilon = \varepsilon_o \kappa$, and the permittivity of free space and the insulator is ε_o and κ, respectively. Equation 2.9 is used extensively in the remainder of the thesis.

In the above definition of capacitance, the material permittivity κ and displacement charge D are used, which are both related to polarization. It is important to clarify the terms relating to polarization in an insulator as polarization is the order parameter for Landau theory, and is expanded in a Taylor series as described in the next section. Equation 2.9 shows that capacitance is increased proportional to κ, i.e. more charge is stored on a given fixed dimension capacitor with the same applied voltage

(equation 2.3). Below, it is shown that permittivity is related to polarization in a linear function as

$$P = (\kappa - 1)\varepsilon_o E \tag{2.10}$$

where κ - 1 = χ as defined in equation 2.1. Therefore, as the permittivity of a material increases, the polarization increases more readily in proportion with the applied electric field. The magnitude of polarization from equation 2.10 is also equal to σ_{pol} which is a fixed surface charge density in the insulator. Thus, capacitance is increased with permittivity when considering equation 2.10 as $|P| = \sigma_{pol}$; a greater permittivity increases the total fixed polarization charge in the insulator, which acts to screen the free surface charge density, σ_f, on the plates of the capacitor. The result is a lowering of the electrostatic repulsion energy between the electrons as more charge is added onto the electrode, and less external energy is therefore needed from the voltage source to achieve the same charge stored (equation 2.3).

In the absence of an insulator, σ_{pol} = 0 and equation 2.7 states $D = \varepsilon_o E = \sigma_f$, i.e. P = 0. The following relationship for the displacement field D describes this result as

$$D = \varepsilon_o E + P \tag{2.11}$$

The greater achieved permittivity in a material, and hence polarization, the lower the contribution of the $\varepsilon_o E$ term in equation 2.11, resulting in a higher screened σ_f. If the polarization is reduced, the electric field across the insulator increases, leading to greater σ_f due to lower achieved σ_{pol}. For ultra-high-κ materials such as perovskites, $D \approx P$, i.e. the free electrode charge is approximately screened by the fixed polarization charge. Equations 2.10 and 2.11 are used in the analysis of the electrical characteristics of paraelectricity and ferroelectricity in terms of Landau's theory in the next section.

2.2.7 Landau's theory

Landau's theory was initially a description of the equilibrium state of a system in the vicinity of a phase transition [33, 34]. The phase transition is discussed in terms of symmetry; there exists a higher symmetry phase in which an order parameter is defined as zero. As the symmetry of the phase lowers, the order parameter changes to finite values. The free energy of the system is then a Taylor series expansion of the order parameter. It is a phenomenological approach to describe the macroscopic properties of a phenomenon. It cannot, however, be used to describe the microscopic properties of the system, i.e. atomic displacements, polarizability, etc.

It was Devonshire who first recognised this approach could be applied to ferroelectrics [35, 36]. The analysis in this thesis will use the Landau-Devonshire (LD) theory of ferroelectrics. It is appropriate due to the high symmetry paraelectric phase transitioning to the lower symmetry of the ferroelectric phase, with the order parameter taken as polarization, P. It describes a displacive transition in which the free energy function evolves from double well minima to a single midpoint as the temperature increases past T_c, and conveys an accurate description of the majority of ferroelectrics [7]. Furthermore, the long-range ordering of a ferroelectric, in which the electrostatic interactions are largely Coulombic diminishing as $1/r$, which is slow in comparison to the strong force binding atomic nuclei. The assumption that each ion in a double well interacts with all others in the crystal is then valid, in accordance with mean field theory. This allows an averaging of the local fluctuations such that LD theory can accurately describe the macroscopic properties of the ferroelectric.

2.2.8 Linear dielectrics

The free energy of a well-known linear dielectric, such as SiO_2, is described in order to compare with paraelectric and ferroelectric properties, and equations 2.3 and 2.10 are used to analyse the results. The energy stored in a linear capacitor is evaluated from the integral of the voltage required to add an element of charge, *dq*

$$U = \int_0^Q V \cdot dq = \int_0^Q \frac{q}{C} \cdot dq = \frac{1}{2}\frac{Q^2}{C} \tag{2.12}$$

where *U* is the energy stored in the capacitor supplied from the voltage source and remaining definitions are taken from equation 2.3. Equation 2.12 shows that the energy needed to add subsequently more charge, *dq*, increases parabolically. Physically, this is explained by the increase in the electrostatic repulsion between the charges added onto the electrodes. Increasing the capacitance, for example from a higher permittivity/polarization, requires less work done by the voltage source to store the same charge, as expected from equation 2.11. The differential of supplied energy with respect to stored charge reverts back to the original definition of capacitance in equation 2.3, and is further differentiated with respect to *Q* to acquire the capacitance as related to the energy function from equation 2.12

$$\frac{dU}{dQ} = \frac{Q}{C} \rightarrow \left(\frac{d^2U}{dQ^2}\right)^{-1} = C \tag{2.13}$$

The analysis in equations 2.12 and 2.13 is shown for SiO_2 in figure 2.6, relating the energy stored in the capacitor, and its derived charge-voltage (QV) and capacitance-voltage (CV) relationship to the energy function. The required energy dependence on charge is showing a square law relationship described in equation 2.12. The derived charge from equation 2.13 shows a linear dependence on the applied voltage due to the polarization in a SiO_2 insulator (small ionic shifts with small contributions from

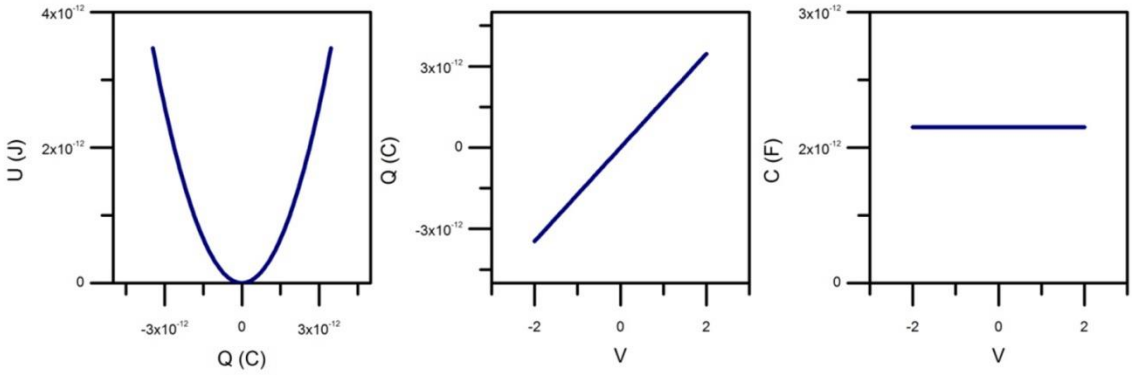

Figure 2.6: Energy stored by a SiO_2 capacitor and its related QV and CV relationship derived from the energy function. Value of capacitance is for 50 µm square electrodes and 50 nm thickness.

electronic sources). The resulting capacitance is then a constant across the whole range of applied bias.

2.2.9 Non-linear dielectrics

The LD equation is now analysed for non-linear polarization in terms of paraelectric and ferroelectric insulators. It is a series expansion of the free energy as a function of polarization, and includes non-linear terms which are omitted from equation 2.12

$$\Delta G = \frac{1}{2}\alpha_1 P^2 + \frac{1}{4}\alpha_{11} P^4 + \frac{1}{6}\alpha_{111} P^6 - E_{app} P \qquad (2.14)$$

α_1, α_{11}, α_{111}, are the dielectric stiffness coefficients discussed below, G is the Gibbs free energy which in this case is the energy density stored in the electric field across the capacitor and $E_{app}P$ is the externally applied electrostatic energy term. The series is truncated at the sixth term as it introduces no new physics into the equation [1]. The equation does not contain odd powers as the non-polar phase has a centre of inversion symmetry (paraelectric cubic phase).

Comparing equation 2.14 to the linear energy function in equation 2.12, there are similarities in terms of the formulation. Equation 2.12 gives energy in Joules, whereas equation 2.14 is a volume energy density. In addition, polarization is now expanded, which was shown to be a scaled version of charge, Q, in equation 2.10.

The material coefficients are now described in terms of the characteristics shown in a perovskite. The linear coefficient α_1 takes the form

$$\alpha_1 = \alpha_0(T - T_C) \approx \frac{1}{\varepsilon_0 \kappa} \tag{2.15}$$

where α_0 is a constant and remaining parameters are defined above. The sign of α_1 determines the phase of the perovskite: with temperature above T_c, α_1 is positive and zero polarization is retained in the absence of an applied field; below T_c, α_1 is negative and hysteretic jumps in polarization are shown (figure 2.3 (b)). Simulations using equation 2.14 and the effects of temperature on the sign of α_1 are shown in section 2.2.10. Also given in equation 2.15 is the relationship of the zero-bias permittivity with α_1. In equation 2.1, the Curie constant can be written as $C = 1/\varepsilon_0\alpha_0$, and the relationship reverts to that shown in equation 2.15 ($\kappa \approx \chi$). Substituting the relationship for α_1 (equation 2.15) into equation 2.14, setting the non-linear terms α_{11} and α_{111} to zero, and multiplying by capacitance area and thickness, the more familiar linear energy function in equation 2.12 is reproduced.

For the non-linear term α_{11}, the sign determines the order of phase transition in the perovskite. A positive α_{11} term ensures a second-order phase transition occurs, while negative values are such that first-order transitions result. Figure 2.7 shows how the order of transition impacts the free energy, polarization and dielectric susceptibility [34]. A second-order transition (figure 2.7 (a)) is continuous such that the spontaneous polarization develops smoothly from $T = T_0$, where T_0 is the phase transition temperature. The term T_0 is taken as T_c in second-order transitions as they are equal. For first-order transitions (figure 2.7 (b)), there is a discontinuous jump in polarization at T_c. There is a regime at $T_0 < T < T_c$ in which the paraelectric phase coexists with the ferroelectric phase, and the paraelectric phase is metastable. Cooling further below T_0, the double well energy minima are shown, which represents the thermodynamically

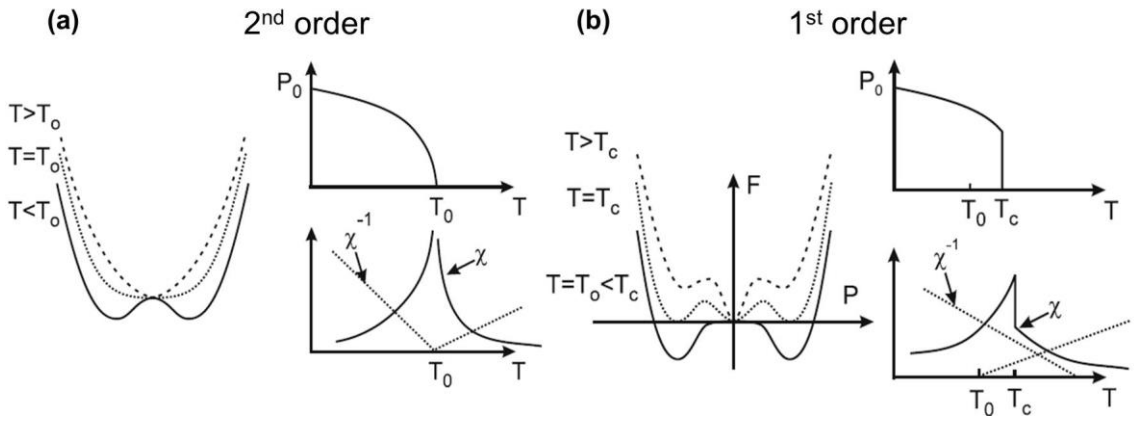

Figure 2.7: The impact on free energy, spontaneous polarization and dielectric susceptibility determined by the order of phase transition (image taken from ref. 34). Second-order phase transition (a), first-order phase transition (b).

favourable state of spontaneous polarization in the ferroelectric phase. The temperature parameters T_0 and T_c are then used to characterise a perovskite showing first-order phase transitions. Finally, the sixth-order term α_{111} in equation 2.14 is used for stability in cases where $\alpha_1 < 0$ ($T < T_c$) and a first-order phase transition is apparent ($\alpha_{11} < 0$).

Constructing the polarization-electric field (PE) relationship is now done using equation 2.14. The minima in free energy representing the stable operating points are derived using $\partial G/\partial P = 0$

$$\frac{\partial G}{\partial P} = E_{app} = \alpha_1 P + \alpha_{11} P^3 + \alpha_{111} P^5 \qquad (2.16)$$

where equation 2.16 results in a scaled version of equation 2.13. Equation 2.16 is used to simulate the polarization – electric field relationship for $BaTiO_3$ below T_c, along with $SrTiO_3$ which is operated above T_c (figure 2.8). The relationship to capacitance is also derived using equation 2.13 and 2.16

$$\frac{\partial^2 G}{\partial P^2} = C' = \alpha_1 + \alpha_{11} P^2 + \alpha_{111} P^4 \qquad (2.17)$$

where C' is capacitance density and depends on the material coefficients described above. Figure 2.8 shows the energy density function, PE curve and derived CV

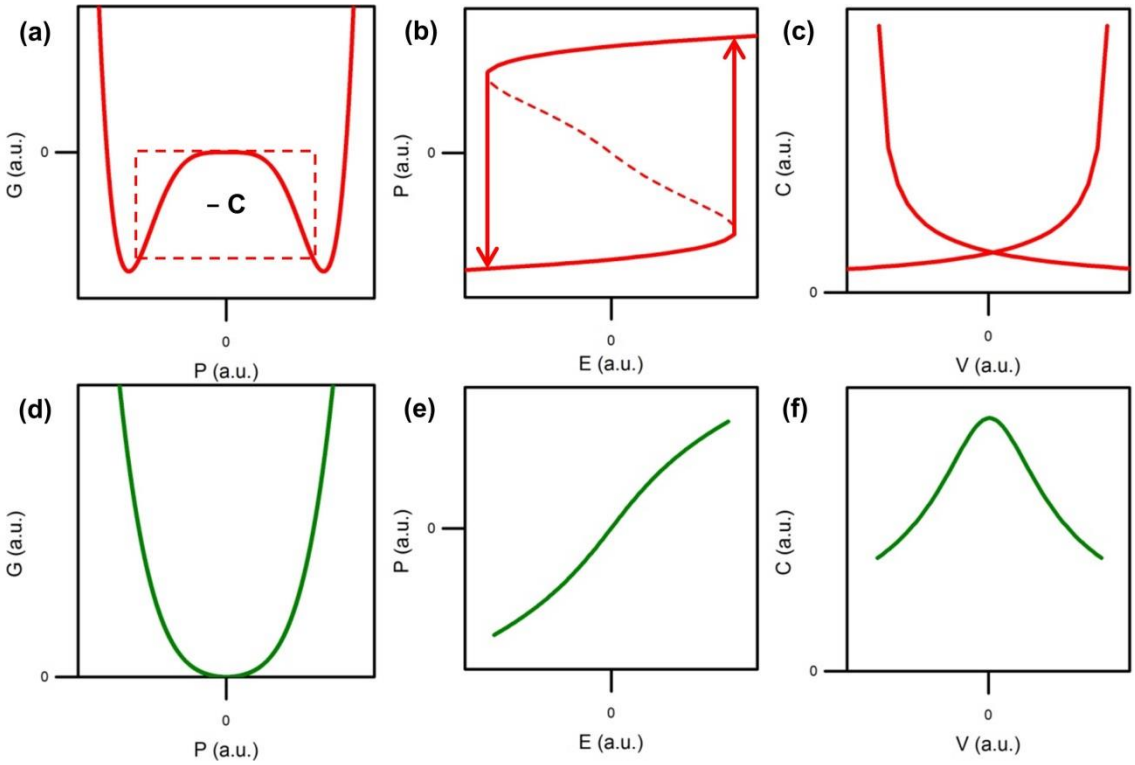

Figure 2.8: Simulated characteristics in $BaTiO_3$, energy density (a), PE (b), CV (c) and in $SrTiO_3$, energy density (d), PE (e), CV (f).

curve in the $BaTiO_3$ and $SrTiO_3$ perovskites at room temperature. Material coefficients used for the simulations are taken from ref. 37.

The energy function for $BaTiO_3$ (figure 2.8 (a)) and $SrTiO_3$ (figure 2.8 (d)) show different relationships. The $SrTiO_3$ function has a single energy minimum at zero polarization and is the highest symmetry state. In contrast, the $BaTiO_3$ energy function shows a break in the symmetry, whereby a phase transition has taken place from the cubic to tetragonal phase. In the lowered symmetry energy function, two energy minima are created at non - zero *P*, which represent the remnant polarization operating points under zero applied field (figure 2.3 (b)). The consequence of the double well minima is a region of negative capacitance, marked $-C$ in figure 2.8 (a), due to the relationship given in equation 2.13. This is also shown as the dashed negative slope in figure 2.8 (b), translating to negative capacitance through a scaled version of equation 2.3. Negative slopes in PE curves were first shown to be evident in $BaTiO_3$ films in ref.

12. Under normal circumstances, this region is not measurable as it is an unstable state. For this reason, negative capacitance has not been directly measured in experiments with capacitors insulated with $BaTiO_3$, and hysteresis ensues (figure 2.8 (b)). The differential of the PE curve shows the large-signal capacitance expected in a ferroelectric $BaTiO_3$ film (figure 2.8 (c)). However, the spikes in capacitance at the switching point of polarization are unphysical and will not occur in real measurements. It has been shown by Merz that polarization will switch in an initial nucleation of reverse polarization, and then forward growth of the domain through domain wall movement [38, 39]. In addition, a model based upon LD theory for polycrystalline ferroelectrics has been applied [40], and a more accurate switching polarization is shown and simulated. However, the negative capacitance region in devices studies in this thesis is designed around zero bias. Further studies with an adaption of LD theory may be conducted in order to optimise the tunability of the negative capacitance designs in chapter 4.

For $SrTiO_3$, the energy function has similarities to the SiO_2 energy function (figure 2.6); however, the region surrounding the minimum point is now deeper, which translates into a larger capacitance at zero bias as defined in equation 2.13. In addition to a higher achieved capacitance, the non-linear terms, α_{11}, α_{111}, have added a tunable characteristic to the $SrTiO_3$ energy function. The result is a non-linear polarization response to an applied electric field in figure 2.8 (e). The differential of the polarization with respect to electric field shows tunable capacitance (figure 2.8 (f)), with highest measured capacitance at zero bias. Decreasing capacitance trends are seen with an increase in the applied electric field. This is due to the bias dependent permittivity, and polarization is no longer a linear function of field, as it was shown to be in equation

2.10. In contrast to $SrTiO_3$, the SiO_2 capacitance is constant across all of the bias range (figure 2.6).

2.2.10 Temperature dependence

The definition of the linear coefficient (α_1) in equation 2.15 shows that temperature is a critical variable in the displayed characteristics of the perovskite. Furthermore, the sign of α_1 determines the phase of the material. Staying in the ferroelectric phase, temperature also impacts the energy function (figure 2.8 (a)), and therefore also the response of polarization to the applied electric field. Figure 2.9 shows how a changing temperature can modify the double well energy function in a ferroelectric, and also its resulting polarization response. A low temperature simulation at 100 K is given ($T << T_c$), at room temperature (300 K, $T < T_c$) and finally at the phase transition temperature (388 K, $T = T_c$).

The energy functions in figure 2.9 (a) change substantially as the temperature is increased towards T_c. Initially at $T << T_c$, two deep minima are shown, ensuring the

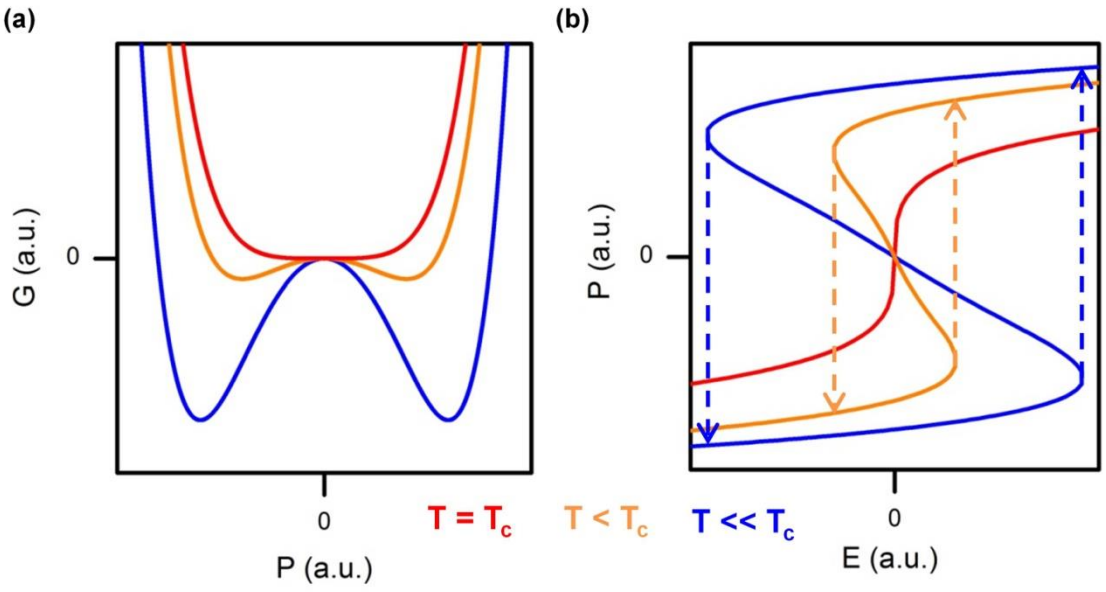

Figure 2.9: Simulated energy density (a) and related polarization as a function of electric field (b), at three temperatures, 100 K ($T << T_c$), 300 K ($T < T_c$), 388 K ($T = T_c$).

hysteretic nature of the polarization response in figure 2.9 (b). Increasing the temperature towards T_c, the minima move toward each other due to the increase in thermal agitation in the crystal. This is expected in a displacive phase transition. The impact this has on the PE curve is shown in figure 2.9 (b) where the polarization is reduced across the electric field, and the hysteresis window decreases. At each simulated temperature below T_c the negative slope of polarization, representing negative capacitance, is evident; however, the hysteretic jumps, indicated by the dashed arrows, occur in standard measurements of ferroelectrics. Moving towards the Curie temperature T_c, the double wells reach a single minimum point at zero, and all ferroelectric properties are lost. The implications on the PE loop in figure 2.9 (b) show a steep slope around zero bias, and relates to the permittivity maximum in figure 2.4 (a). At this temperature the crystal transitions to the cubic paraelectric phase and the negative capacitance property is no longer evident.

In chapter 4, the model for negative capacitance stabilisation is given based upon the energy functions described above. Temperature and insulator thickness are key parameters in the stabilisation of negative capacitance, and a room temperature design is given for three thicknesses of $BaTiO_3$ deposited on a fixed thickness of $SrTiO_3$. In the following sections, the background information relating to negative capacitance will be discussed, and some of the possibilities are highlighted if the technology is to be incorporated into electronic devices.

2.3 Nanoelectronics and the Si Industry

Since the invention of the transistor in 1947 by Shockley, Bardeen and Brattain [41], the modern world has been revolutionised. The transistor ushered in the digital age, enabling the creation of electronic devices from supercomputers, advanced medical equipment, mobile computing to the internet, among many others. It was the transistor that was at the heart of Gordon Moore's paper in 1965, in which he discussed cramming more components onto an integrated circuit [42]. Here, the drive towards ever faster and more powerful computing was projected as Moore first stated that the number of transistors on a chip will double approximately every 18-24 months. Now, this scaling of transistors is known as 'Moore's law', and has been upheld ever since. The first projected roadmap for the transistor given by Moore is shown in figure 2.10 (a) [42]. Extrapolating the data in figure 2.10 (a) to the modern day, the number of transistors on an integrated circuit has reached into the billions. This is primarily done by reducing the channel length in the MOSFET. In figure 2.10 (b) this is shown down the vertical scale as the dimension decreases from 130 nm to 16 nm [43]. Recent integrated circuits use tri-gate MOSFETs with channel lengths of 22 nm [44].

In addition to transistor scaling, the horizontal scale in figure 2.10 (b) shows an additional trend for integrated circuits. Known as 'more than Moore', in contrast to 'more Moore', the effort is placed in greater functionalities with the circuits at hand. Technology is now aiming to have multiple applications not necessarily focused on digital logic and memory storage. In wireless devices, the requirements may include RF and analog mixed-signal components, microelectromechanical systems (MEMS), in addition to the standard digital and memory contributions. Biochips are also a keen area of research. In either the more Moore, or more than Moore agenda, incorporating new

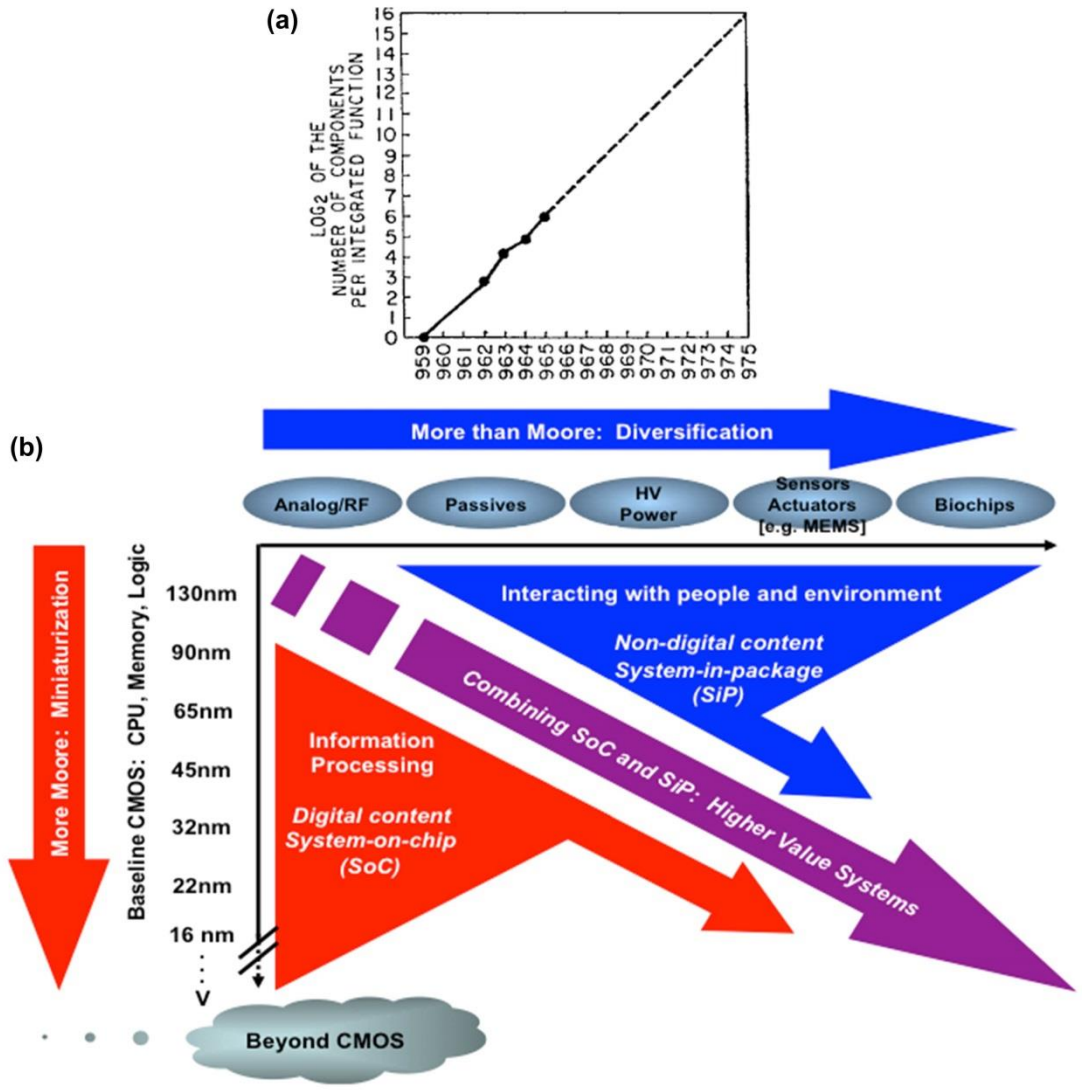

Figure 2.10: (a) The first account of Moore's law discussing the projection of the transistor as cramming more components onto an integrated circuit (image taken from ref. 42). (b) An up-to-date view of the direction of the nanoelectronics industry featuring both scaling and diversification (image taken from ref. 43, http://www.itrs.net).

materials into an integrated circuit is a key aspect of taking both the technologies forward.

2.3.1 More Moore and scaling

As mentioned previously, Moore's law, under the more Moore agenda, states that the number of transistors on an integrated circuit doubles approximately every 18 - 24 months. The benefits of miniaturisation come from greater circuit performance and speed, as well as cost saving per fabricated transistor. When the transistor is scaled to

smaller dimensions the device should become faster, but with the standard operations unchanged. In order to design faster devices with no change in their basic operation, scaling rules first set out by Dennard in 1974 stated that the electric field in the gate oxide should be kept constant [45]. A scaling factor was introduced, S ($S > 1$), in which device dimensions were reduced inversely to S, and doping concentrations increased proportionally. The scaling rules are summarized in table 2.1. Therefore, as the device dimensions shrink, in turn increasing the speed, the power dissipation reduces as a factor of $1 / S^2$. This saving in power dissipation is one of the main driving forces behind constant electric field scaling, and is the reason the voltage supply V_{DD} has reduced from 5 V, to 3.3 V and now 2.5 V and below.

However, it is often not possible to scale the voltage supply according to 1 / S. A major road block to voltage scaling is the threshold voltage, V_{TH}, of a transistor cannot scale in proportion to V_{DD} as reducing V_{TH} will lead to increased leakage from the subthreshold current. The supply voltage has scaled to approximately 20 % of its original value, while V_{TH} has scaled down to half. This impacts the overdrive voltage

Device Dimension or Parameter	Scaling Factor
Device dimension: L, W, t_{ox}	**$1 / S$**
Doping concentration	**S**
Voltage	**$1 / S$**
Current	**$1 / S$**
Capacitance	**$1 / S$**
Delay time	**$1 / S$**
Power dissipation	**$1 / S^2$**
Power density	**1**

Table 2.1: Scaling rules for device miniaturisation to keep the electric field constant.

(V_{DD} - V_{TH}), which is responsible for the achieved on-current, I_{ON}, such that the aggressive scaling of V_{DD} reduces the ratio of I_{ON} to I_{OFF}. For this reason, constant voltage scaling may be introduced. The resulting increase in electric fields can cause undesirable effects known as short-channel effects [46].

The adherence to scaling set in table 2.1 in order to follow more Moore shows that the gate insulator thickness decreases according to 1 / *S*. Figure 2.11 shows how the scaling of this insulating thickness has progressed over the past four decades [47]. The projection of the thickness of t_{ox} up to the year 2010 is sub 1 nm with SiO_2 insulators. Approaching this unphysical dimension leads to large increases in leakage current through the gate due to quantum tunnelling. Therefore, new materials were introduced in order to mitigate this increase in leakage current. High-κ insulators were used to counteract the need to decrease the thickness of the gate oxide. However, the increase in the insulating thickness inhibits the constant electric field scaling set in table 2.1.

It is apparent that scaling has become increasingly difficult as the transistor shrinks further. As the reduction in V_{DD} slowed, and the number of devices on an IC still doubles, the power dissipation increases on a chip. It was the volume of devices on an IC, and this inability to aggressively scale V_{DD}, that led to the need for multi-core

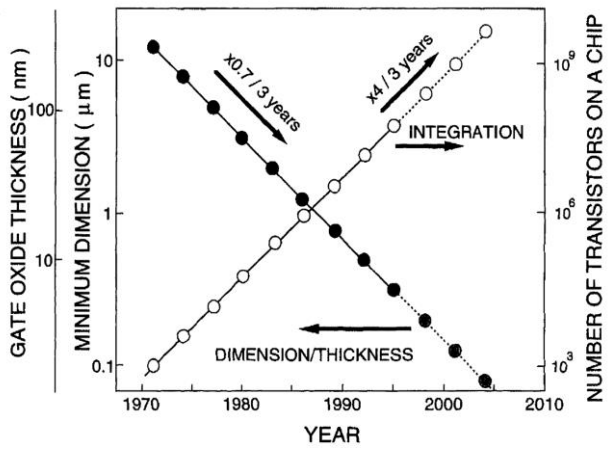

Figure 2.11: The historical trend of miniaturisation of the gate oxide thickness t_{ox} and gate length L. Also shown is the increase in the number of transistors on an IC into the modern day (image taken from ref. 47).

processors. This limited the amount of heat dissipation per chip that would have otherwise had catastrophic consequences on a single core. New technologies are needed in order to progress Moore's law further, and negative capacitance is explored in the following sections which may allow a new, faster and denser, single core processor to be designed.

2.3.2 More than Moore

Further to the success of the more Moore agenda with billions of transistors fitting onto a chip, more than Moore is working to complement ever-faster and greater densities of digital logic. The parallel goal is to enhance the functionality of a product that does not simply consist of billions of digital switches in CMOS technology. As shown in figure 2.10 (b), the trend for more than Moore is not necessarily scaling, but to provide value to the consumer in different ways. The non-digital components of more than Moore can then be combined within the digital aspect of the integrated circuit to produce system-in-package (SiP), or on the chip itself for system-on-chip (SoC) technology.

In each track of SiP or SoC, mixed technologies integrated with the Si wafer lead to systems with the computing power of modern CMOS, along with the diversification of advanced non-digital components. The non-digital functions constitute interactions with users using sensors and actuators, and also on powering the system itself, as well as any required mixed signal processing and passive devices and MEMs. Therefore, more than Moore is not seen as a replacement for the end of more Moore, ultimately arising due to the physical inability to scale the transistor further; rather it works in conjunction with the digital goal of miniaturisation in order to bring about a greater functioning system to fulfil the needs of the modern day.

The more than Moore agenda is a recent trend for the nanoelectronics industry, in comparison to more Moore. The International Technology Roadmap for Semiconductors (ITRS) has recently proposed that the more than Moore roadmap is likely to require the involvement of many researchers and organisations in order to reach a common goal, such as the case for digital scaling [48]. Here, transistor scaling leads to increased performance and reduced cost per function, leading to market growth and further investment. However, a clear consensus is still to be written for more than Moore.

One such material that has the potential to fulfil numerous non-digital functionalities is the ferroelectric perovskite. Its non-linear response to an applied electric field offers a tunable capacitance property (figure 2.8 (e), (f)) that is of interest when the insulator is used as an element in microwave devices. Possibilities include impedance matching and tunable filters for use in mobile devices. A candidate for the tunable ferroelectric perovskite is barium strontium titanate $(Ba_xSr_{1-x})TiO_3$. The concentration of Sr, controlled by the value x, allows T_C, and therefore the permittivity, to be selected depending on the required application. The selectivity of T_C with Sr alloying can also lead to ultra-high-κ at the operating temperature (figure 2.4 (a)). Integration of this tunable perovskite into the back end of line (BEOL) of integrated circuits can enable cheap SoC solutions for radio frequency (RF) CMOS.

While the characteristics of perovskite ferroelectrics are beneficial for more than Moore, it requires high quality film deposition in order to utilise the respective properties. For BEOL integration, temperature of deposition is an issue as inter-diffusion of dopants, and also the formation of high resistive $NiSi_2$ phases, can cause catastrophic circuit failure when the temperature is raised > 500 °C. Therefore, methods of depositing high quality perovskites are necessary at low temperature. Atomic layer

deposition (ALD) and pulsed laser deposition (PLD), along with sputter deposition may be solutions to deposit high quality thin films and are discussed in chapter 3. In addition, Sr alloying impacts the electrical properties, but will also shift the crystallisation temperature of the film. Crystallised films are necessary if the tunable property of the perovskite is required.

Moreover, high tunability (> 40 %) and low leakage currents are desirable in components of perovskites for non-digital functions. When deposition temperature is not limited, electrical properties are impacted by dead layers [14]. Understanding the impact of dead layers, and the influences of leakage in perovskite insulators, is imperative if these new materials are to be utilised for the more than Moore agenda. Chapter 5 of this thesis addresses some of the issues discussed above, showing results of low temperature deposition of perovskites.

2.3.3 Low power applications

With the invention of CMOS, power dissipation on a chip was considerably reduced. The complementary effect of both p and n - type transistors ensures that current mainly flows during switching, and leakage current is significantly reduced. However, as the scaling of Moore's law continues, the increasing number of devices still creates large amounts of dissipated power, which further increases with each new technology node. A critical design parameter for the modern integrated circuit is, therefore, power consumption. This is even more relevant today as the desire for portable electronics requires long lasting batteries without degradation in performance. Furthermore, even with standard desktop computers, high power dissipation arising in modern chips can cause reliability issues and failure mechanisms.

In order to assess the topic of power dissipation, the sources have to be identified. There are two main categories for power dissipation, named dynamic and static. For dynamic dissipation, logic nodes are switched, causing capacitances to be charged and discharged. During the switching, the current flowing through the channel of the MOSFET has associated dynamic power dissipation due to the generated self-heating. The secondary mechanism for dynamic dissipation arises when current is allowed to leak from the supply rail to ground under certain logic levels. However, in CMOS technology this does not occur as the network of p and n - type transistors ensures one transistor is always off. This is a major advantage of CMOS when compared to using only n - type transistor circuits. Nevertheless, there does exist a short period of time during clock cycles in which both the n and p - type transistors conduct. This dissipation depends on the rise and fall times of the MOSFETs, but it is considerably reduced when compared to previous circuit technologies. The relationship for dynamic power dissipation can be expressed as [49]

$$P_{dynamic} = f C_L V_{DD}^2 \tag{2.18}$$

where C_L is the output load capacitance of the digital network and f is the clock frequency. What is most apparent about equation 2.18 is that the dynamic dissipation does not depend on the dimensions of the device, and only increases proportionally to clock frequency and the square of the supply voltage. Therefore, as Moore's law continues, scaling the transistor does not impact the dynamic dissipation; reducing the voltage under constant field scaling (table 2.1) has lowered this contribution to overall power dissipation considerably.

Static dissipation is associated with leakage current when the logic levels on the gates are not changing. Originally, due to the saving of leakage current using

CMOS circuits, this was less of a concern. The relationship for the static power dissipation can be expressed as [49]

$$P_{static} = I_{leak} V_{DD} \tag{2.19}$$

where I_{leak} is the sum of all the associated leakage currents in the transistor when it is off. In contrast to the dynamic power consumption, the static contribution is affected by device scaling through the term I_{leak}. The leakage in the off state consists of pn junction reverse bias current, tunnelling in and through the gate oxide, injection of hot carriers, gate-induced drain leakage and punch-through [50]. However, one remaining contribution to I_{leak} is the subthreshold leakage current. When the supply voltage is scaled, in order to maintain high drive current by keeping a suitable overdrive voltage (V_{DD} - V_{TH}), the threshold voltage should be reduced. Reducing the threshold voltage causes a substantial increase in the subthreshold leakage. For this reason, the static power dissipation has become the major issue as devices are scaled, and has overtaken the dynamic contribution.

In order to describe the subthreshold leakage current, the subthreshold swing (*SS*) in a Si MOSFET is shown in figure 2.12. The sketch shows a typical logarithm of the drain current I_D against applied gate voltage V_G. It is a critical region in an n - type MOSFET whose relationship shows the transition between the off to on state, its saturated drain current, threshold voltage and subthreshold slope relating to the *SS*. The inverse of the slope in figure 2.12 describes the *SS*, and is defined as [51]

$$SS = \frac{\delta V_G}{\delta(\log_{10} I_D)} = \frac{\delta V_G}{\delta \Psi_s} \cdot \frac{\delta \Psi_s}{\delta(\log_{10} I_D)} = 2.3 \frac{kT}{q}\left(1 + \frac{C_S}{C_{ox}}\right) \tag{2.20}$$

$$\frac{\delta V_G}{\delta \Psi_s} = m = \left(1 + \frac{C_S}{C_{ox}}\right) \tag{2.21}$$

Ψ_s is the surface potential in the channel, k the Boltzmann constant, T operating temperature, q is unit charge, C_s is the semiconductor capacitance including depletion

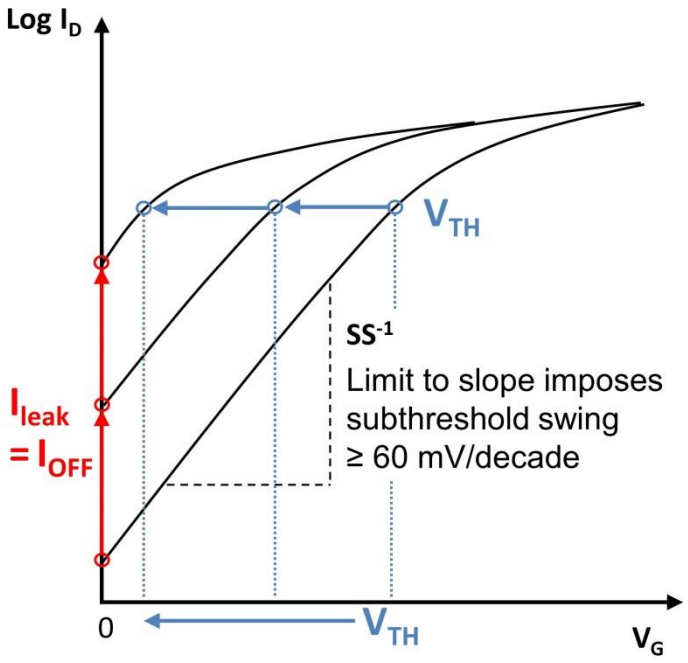

Figure 2.12: The subthreshold slope in a Si MOSFET. As the threshold voltage is reduced the leakage current in the off state is increased due to the limit of the slope.

width contribution and C_{ox} is the capacitance associated with the gate oxide thickness t_{ox}. It is therefore desirable to have a steep subthreshold slope as this dictates how easily it is to turn off the device from saturated I_D to I_{OFF} when the gate voltage is reduced below the threshold voltage. In equation 2.20 for Si transistors, the *SS* describes this transition and is related to $2.3V_t$ (V_t is the thermal voltage kT/q), and the body factor term '*m*'. There is a limit to the switching in Si transistors due to thermionic emission of carriers from the source to the channel. It is controlled by Boltzmann statistics which states that 60 mV is required to increase the current by an order of magnitude in a MOSFET at room temperature ($2.3kT/q$ = 60 mV). This is knows at the 'Boltzmann tyranny' [52] as it limits the abruptness of the subthreshold slope in figure 2.12. However, the *SS* is also proportional to the body factor term, where '*m*' in equation 2.21 is shown to be a ratio of the series capacitances associated with the gate stack of the transistor. If the oxide thickness t_{ox} approaches 0, then C_{ox} will be made infinitely

high, and '*m*' will be unity. With this 'ideal' limit imposed, the *SS* reaches its lowest value of 60 mV/decade at room temperature. Of course, this is an unrealistic scenario as an insulating thickness is required for maintaining capacitive control of the channel current. Solutions to aid in reducing the *SS* have arisen, such as scaling t_{ox} as explained previously, and also using high-κ dielectrics which in turn increase capacitance as described in equation 2.9. In either case, the limit imposed by $2.3kT/q$ still leads to a required 60 mV/decade, which impacts the slope in figure 2.12.

As described above, the limit on the subthreshold slope is such that decreasing the threshold voltage has severe consequences for the subthreshold current. In figure 2.12, this is shown as a series of shifted characteristics, where V_{TH} is seen to decrease at the expense of a large increase in I_{OFF}. The increase in I_{OFF} is due to the maximum achievable subthreshold slope, and so any reduction in V_{TH} causes the subthreshold current to increase. The difficulty then arises when the supply voltage is scaled as the threshold voltage should ideally be scaled in conjunction in order to maintain a high drive current. This factor for modern integrated circuits has been a major roadblock as the necessity to reduce V_{DD} for the prevention of dynamic power dissipation still holds. Any decrease in V_{TH} will then increase I_{OFF}, and it has caused the static power dissipation to become the dominating contribution to energy usage in modern chips. This problem may be alleviated if a solution to the *SS* limit of 60mV/decade is found. It would open up a route for low power transistors, allowing the supply voltage, V_{DD}, to scale concurrently with the threshold voltage, V_{TH}, without increasing the subthreshold current. Negative capacitance is a possible solution to achieve steep subthreshold slope MOSFETs and is discussed in the following section. Another proposal known as a tunnel MOSFET is also shown.

2.3.4 Negative capacitance

As highlighted in the ITRS, replacing the standard insulator in a MOSFET with a ferroelectric insulator of appropriate thickness may lead to steeper subthreshold slopes, provided the energy functions in each contributing layer are balanced [53]. Therefore, the simulations of energy density based upon equation 2.14 and shown in figure 2.9 (a) are critical if negative capacitance is to be utilised in a MOSFET. Chapter 4 will expand upon LD theory and show that negative capacitance can be stabilised in $BaTiO_3$ at room temperature, creating an overall positive capacitance that is greater than the constituent positive capacitance in the series.

The groundwork for negative capacitance and its possible inclusion in the gate stack of a MOSFET was first proposed by Salahuddin and Datta (figure 2.13) [10, 11]. Here, they recognise that the body factor term ($\delta V_G/\delta \Psi_s = m$) is related to the capacitances associated with the gate stack of the MOSFET (figure 2.13 (a)), and any attempt to use high values of C_{ox} simply makes the term unity. However, substituting a negative capacitance in replacement of C_{ox}, it should be possible to achieve $m < 1$, and hence a *SS* less than 60 mV/decade. A description of LD theory is given to support the hypothesis, which ultimately shows that in the ferroelectric phase, α_1 is negative and m is approximated as $\delta V_G / \delta \Psi_s \approx 1 + \alpha_1$. A simulation is presented from LD theory in figure 2.13 (b) which shows the predicted negative slope in PE loops for $BaTiO_3$ (figure 2.8 (b)). This is supported with a study on $BaTiO_3$ in which polarization is plotted with field through the ferroelectric film and negative slopes are evident [12].

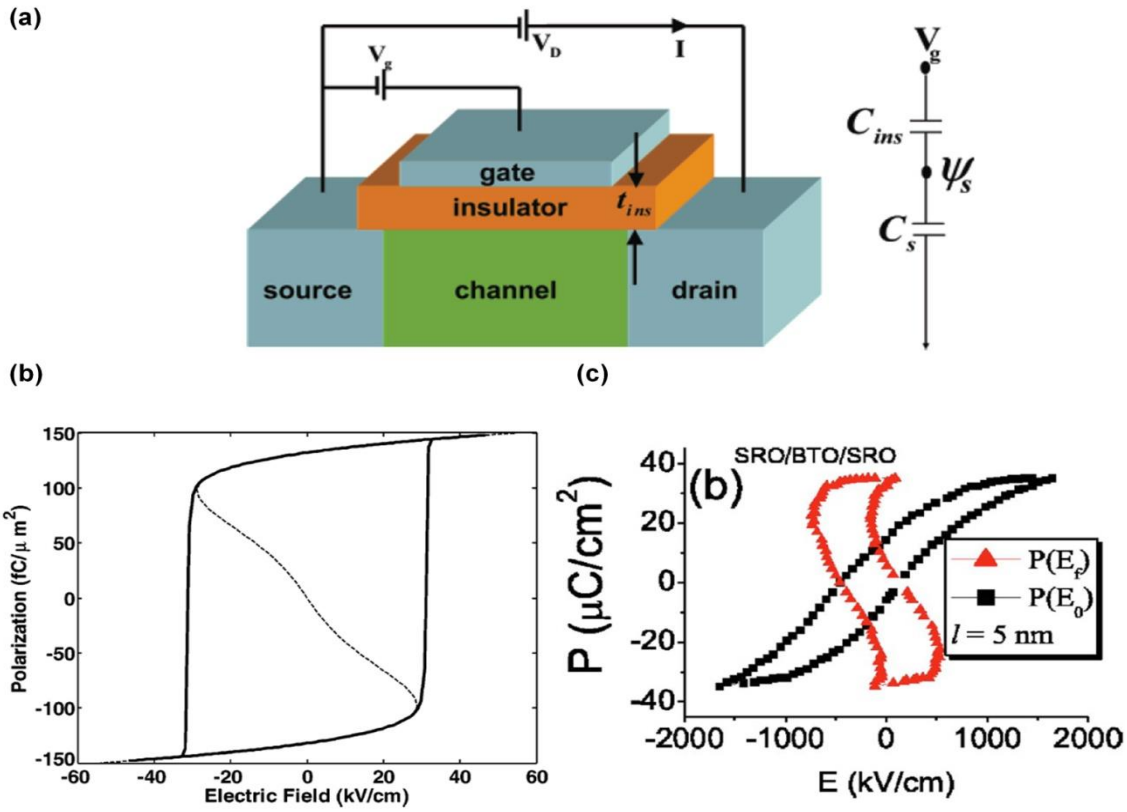

Figure 2.13: (a) Schematic of the MOSFET and its modelled series capacitance through the gate from equation 2.21 ($C_{ins} = C_{ox}$). (b) PE loop calculated from LD theory in comparison to that shown in figure 2.8 (b) showing a negative slope (images taken from refs. 10, 11). (c) 'Actual' PE loops, with field in the ferroelectric film E_f showing a negative slope (image taken from ref. 12).

The negative capacitance property is then discussed in terms of the energy functions in both a linear and ferroelectric insulator. The parabolic nature of energy in a linear insulator is shown to differ to that in a ferroelectric in which the energy is negative (figure 2.14) [11]. The energy function in the ferroelectric has an unstable minimum at zero ($Q = 0$), which is related to the instability of negative capacitance in a ferroelectric. Hysteresis then ensues in charge - voltage relationships, whereas the linear insulator is a straight line through the origin translating into constant positive capacitance. The plots in figure 2.14 are directly equivalent to figure 2.6 for a linear insulator, and figure 2.8 (a) - (c) for a ferroelectric. In order to stabilise the elusive negative capacitance region in the ferroelectric, they finally propose that it should be stabilised in a series capacitance system, creating an overall positive capacitance.

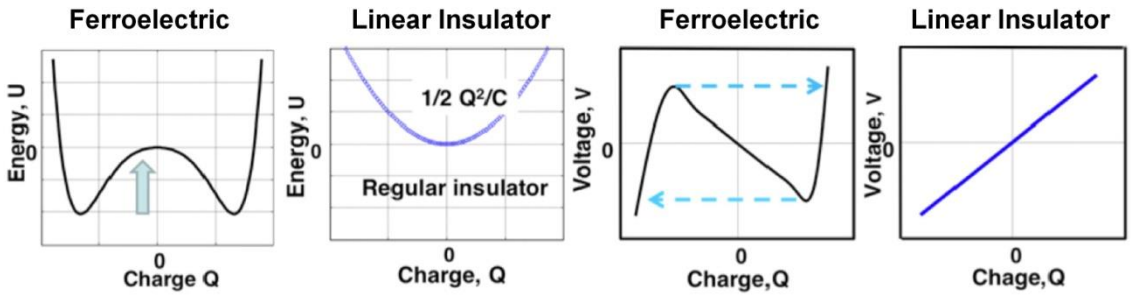

Figure 2.14: The energy functions in a ferroelectric and linear insulator and corresponding charge-voltage relationship (image taken from ref. 11).

A study by Khan *et al.* proposed a stabilised ferroelectric showing negative capacitance when placed in series with a positive capacitance [54]. A 'negative' $Pb(Zr_{0.2}Ti_{0.8})O_3$ ferroelectric in a bilayer structure with 'positive' $SrTiO_3$ paraelectric showed a total capacitance that was greater than the constituent $SrTiO_3$ capacitance, owing to negative capacitance of $Pb(Zr_{0.2}Ti_{0.8})O_3$. Simulations also showed that below certain temperatures, LD theory predicted the capacitance enhancement in the bilayer structures (figure 2.15). However, the effective negative capacitance was seen at temperatures up to 773 K and beyond the Curie temperature of the ferroelectric [37]. Furthermore, the operating temperature is unsuitable for inclusion into an integrated circuit. Therefore, experimental evidence for negative capacitance, particularly at room temperature, remains inconclusive.

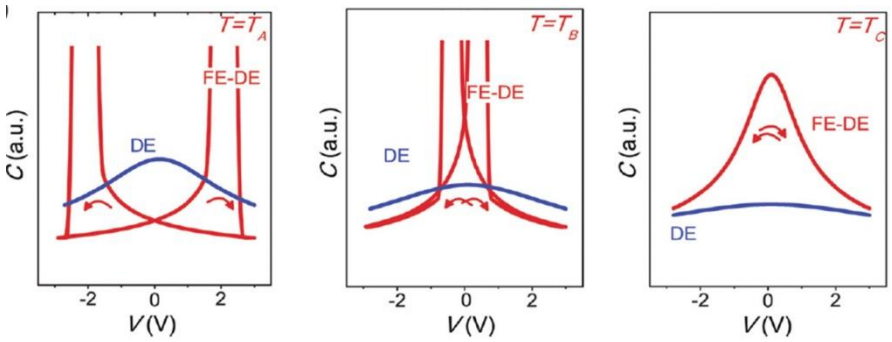

Figure 2.15: Simulations of capacitance from LD theory for a bilayer of $Pb(Zr_{0.2}Ti_{0.8})O_3$ (FE) on $SrTiO_3$ (DE) (image taken from ref. 54). At temperatures T_A and T_B the instability of ferroelectric capacitance is shown (figure 2.8 (c)). However, at T_C the total capacitance of the bilayer is greater than the constituent positive layer.

2.3.5 Tunnel FETs

In the case of a MOSFET, the injection of carriers over a barrier for current flow originates due to thermal injection. This mechanism in turn places the limit contained in equation 2.20 of $2.3kT/q$, and at room temperature in a Si transistor the SS is therefore 60 mV/decade. Capacitive coupling across the gate stack leads to further increases in the required voltage needed to increase the current by an order of magnitude. However, in moving away from the traditional physics of the FET, whereby thermal injection and capacitive control dictates the channel current, a tunnel FET (TFET) is another solution to lower the *SS*, and hence limit power dissipation.

The operation of a TFET is described by quantum mechanical band to band tunnelling of charge carriers between energy bands of a heavily doped diode. The tunnelling mechanism between heavily doped p^+n^+ junctions was first studied by Zener in 1934 [55]. Figure 2.16 shows the schematic of a gated p-i-n diode with heavily doped n^+ and p^+ regions representing the source and drain of the transistor, respectively [56]. When the TFET is off the channel valence band is situated below the conduction band in the source. Applying a negative gate voltage, the energy bands are allowed to move by an amount $q\Delta V_G$. If sufficient gate voltage is applied, the channel valence band moves above the conduction band in the source, creating a window for tunnelling electrons to flow into the channel. The green shaded arrow and energy window $\Delta\Phi$ for allowed electron flow are shown in figure 2.16. The tunnelling action allows the subthreshold slope to be steeper (figure 2.16 (c)) and, as a result, there is no longer a dependence on thermal injection, and the term kT/q is omitted from equation 2.20. The *SS* in this regard may be achieved less than 60 mV/decade. The action of the TFET in figure 2.16 may be reversed by applying a positive voltage to the gate of the p-i-n diode such that the transistor will operate as an n - type device.

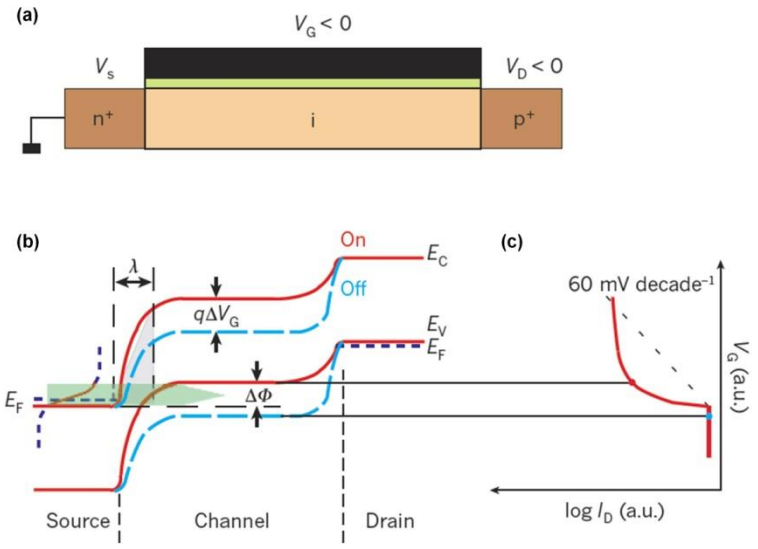

Figure 2.16: (a) A schematic of a TFET that is a gated p-i-n diode operating as a p - type transistor. Voltages of V_S, V_G, V_D are corresponding to standard MOSFETs but with different polarities. (b) Energy band diagram of the off (blue dash) and on (red line) state in the TFET. E_F, E_C, E_V, are the Fermi level, conduction and valence level, respectively. Applying a negative V_G allows the channel E_V to move above the source E_C to allow current to tunnel across the region shown by $\Delta\Phi$. λ represents tunnelling length. (c) The subthreshold slope is shown to be steeper for TFETs when compared to the linear dashed relationship for a MOSFET (image taken from ref. 56).

One major drawback of the TFET is that the achieved on-current in the devices is considerably lower than in standard MOSFETs. The on-current is exponentially dependent on the width between the barriers where the current flows (figure 2.16 (b)) [57]. A key parameter is the tunnelling length λ shown in figure 2.16, which should be minimised in order to produce a tunnelling probability of electrons from band to band close to unity. Among other influences [56], the gate capacitance affects the tunnelling length, and it has been shown that high-κ materials are desirable [58]. Therefore, the major drive for TFET devices is to achieve high on-current through material engineering, while maintaining the < 60 mV/decade *SS* over many magnitudes of drain current. Negative capacitance is a possible technology that may be

incorporated into the gate insulator in TFETs in order to lower the required gate voltage even further.

2.3.6 Further applications and associated issues

FRAM is now used in a variety of products and is based upon the 1T1C schematic shown in figure 2.1. Thin film forms of ferroelectric material offer low voltage applications, and high speeds of down to 60 ns access time. However, the dissimilarities between the perovskite and Si make it difficult to incorporate ferroelectric material into the Si driven industry. Perovskites requiring high annealing temperatures in order to crystallise the material may lead to inter-diffusion between the contacted films [59]. Furthermore, the differences between the lattice constants and thermal expansion coefficients of Si and $BaTiO_3$ are such that the polar c-axis of $BaTiO_3$ (figure 2.5 (b)) aligned along the electric field direction is difficult to obtain. This severely limits any remnant polarization in the perovskite crystal, and data retention in FRAM is inhibited.

Figure 2.17 shows remnant polarization in $BaTiO_3$ samples of different thicknesses and grain sizes [60 and references therein]. As the perovskite shifts from a single crystal state, the remnant polarization is seen to reduce drastically. This trend is seen to correlate with grain size, and to a lesser extent film thickness. Polycrystalline films achieve a maximum remnant polarization of 12 $\mu C/cm^2$ only if the grain size is 2 μm. Therefore, the crystal quality and grain size play a significant role in achieving high remnant polarization for data retention in FRAM. A well-known phenomenon referred to as the size driven phase transition has been previously studied [61]. It places a critical size on the grain of a crystal, where a smaller grain structure shifts the phase

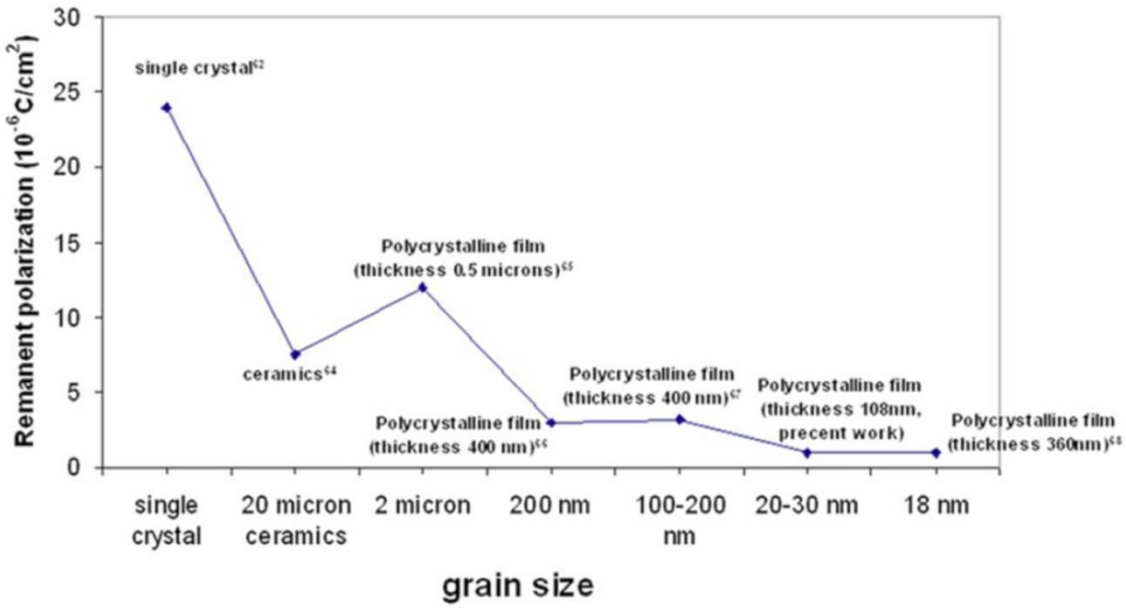

Figure 2.17: Remnant polarization in $BaTiO_3$ samples as a function of grain size (image taken from ref. 60).

transition temperature to lower values. This leads to materials that are paraelectric in phase at operating temperatures previously known to induce the ferroelectric phase. Chapter 6 studies thin films of $BaTiO_3$ incorporated with Si.

One recent study has proposed a buffer layer in between the Si/SiO_2 substrate [62]. The buffer layer is yttria-stabilised zirconia (YSZ) which promotes the epitaxial and c-axis oriented growth of $BaTiO_3$ when deposited on the Si substrate. A $LaNiO_3$ conducting perovskite oxide was used such that Pt electrodes are not necessary. Issues with Pt electrodes arise due to adhesion layer diffusion through grain boundaries [63] and agglomeration [64]. For film thicknesses as low as 33 nm the remnant polarization was as high as 10 $\mu C/cm^2$. The epitaxy of the fabricated films ensured no grain size dependence on the remnant polarization, as well as there being no film thickness dependence. The use of the buffer layer may be a solution for high data retention, greater density FRAM. In addition, YSZ may be used with bilayer insulators in order to stabilise negative capacitance in $SrTiO_3/BaTiO_3$ structures. Chapter 4 discusses the

designs on $SrTiO_3$ (100) substrates. YSZ may offer a route towards stabilisation on the required Si substrate, and is discussed further in chapter 7.

2.4 Summary

The purpose of this chapter was to introduce ferroelectricity, particularly relating to the perovskite crystal, and also discuss the current position of the nanoelectronics industry. For ferroelectric material, its unique electrical properties with an applied electric field open up a range of applications for both more Moore and more than Moore. Its piezo and pyroelectric nature also make it suitable for sensor applications. For this reason, the perovskite ferroelectric has been studied extensively for a number of decades for use in FRAM, tunable devices and high-κ capacitor structures. Ferroelectricity itself is also in close accord to ferromagnetism, and the similarities and differences are presented.

One particular characteristic in a ferroelectric, which is predicted through LD theory, is negative capacitance. LD theory described in this chapter shows that, due to a negative energy density in a ferroelectric, a window of negative capacitance is situated around zero polarization. Consequently, negative capacitance is in an unstable state and has not been previously measured in experiment. Stabilisation has been proposed through placing a negative capacitor in series with a positive one, such that the total capacitance is enhanced. This model matches closely to the series configuration of capacitors in the gate stack of a MOSFET. Therefore, if negative capacitance is stabilised and incorporated into the MOSFET, the SS may be reduced below 60 mV/decade. This technique involves engineering the body factor term, m, and does not change the standard physics of the MOSFET.

Another solution is shown in which band to band tunnelling removes the restriction of thermal injection of carriers into the channel. Thus, TFETs change the conduction mechanisms associated with the channel flow of current. It leaves the body factor term, assuming a negative capacitance may not be achieved. However, the gated

p-i-n diode structure still leaves a possibility of incorporating negative capacitance into the gate stack of this device. Combining the technologies may lead to even lower required voltages to turn the transistor on.

Ferroelectric films for low temperature applications in BEOL integration, as well as issues on achieving high remnant polarization with Si substrates, were discussed. Growing high quality thin films at low temperature is a keen area of interest in order to inhibit the inter-diffusion of previously grown material and limit the formation of high resistive silicide phases. The difficulty of high remnant polarization in ferroelectrics integrated with Si arises due to their different structural and mechanical properties. The following chapters will discuss recent results that address these pertinent issues.

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Chapter 3

Thin Films, Characterisation and Fabrication

3.1 Introduction

The need for thin film devices becomes ever more apparent as device scaling continues. A critical application of a thin film insulator is in the gate stack of a MOSFET. The role of this layer is to ensure charge does not leak from the channel, causing a degradation in drive current and unwanted power dissipation. Chapter 2 showed the endeavour for even thinner films for this application. In fact, the requirement for thin SiO_2 insulators became such that dimensions were unphysical. For ferroelectric insulators, thin films are required such that the electric fields across a capacitor reach the polarization switching electric field. Films of sub-micron dimensions allow these fields to be reached with batteries expected in hand-held devices, such as mobile phones or tablets. For example, a 200 nm thick film would only require 1 V voltage supply in order to reach a switching electric field of 50 kV/cm. As

the nanotechnology era of the 21st century develops, the necessity for high quality, ever decreasing dimensions of thin films will only increase.

One major application of a thin film is the capacitor. As previously stated, one area of importance for capacitor systems is the gate stack of a MOSFET. However, capacitors themselves are the most common passive components in electronics, finding applications in all forms of integrated circuitry, amplifiers and diverse ranging electronic equipment. Standalone capacitors are perhaps the most well-known devices, but as the more than Moore agenda develops, system-on-chip (SoC) and system-in-package (SiP) applications will require further advancements in thin film forms of capacitors. This is in addition to the already well developed application of capacitors in dynamic random access memory (DRAM), whereby new thin film dielectrics were highlighted as necessary in 2000 [1].

For integrated capacitors, two of the main forms of the device are metal-oxide-semiconductor (MOS), and metal-insulator-metal (MIM) structures. Applications of MOS capacitors are primarily the gate stack in a MOSFET, while MIM based capacitors are used in a range of memory elements such as DRAM. The characteristics of MOS and MIM capacitors vary substantially. For a MOS device there is strong voltage dependence, owed to the dynamic bottom plate situated within the semiconductor. The applied voltage allows accumulation, depletion, or inversion layers to form, which further depends on the semiconductor and doping of the material. Expected CV trends for a MOS capacitor are shown in figure 3.1 (a). For MIM devices, the capacitance is described using the parallel-plate formula derived in chapter 2 (equation 2.9). The capacitance is only voltage dependent if a tunable material is placed between the electrodes of the device, such as a perovskite. In such MIM capacitors

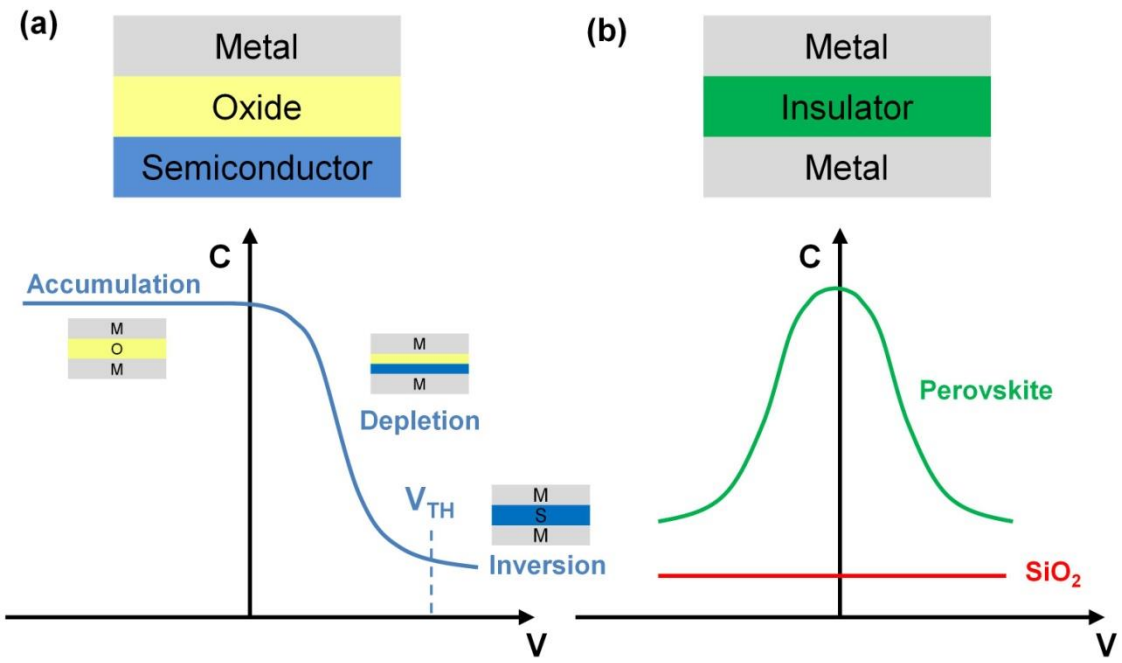

Figure 3.1: Schematic of capacitor structures and expected CV relationships. (a) p-type MOS capacitor with three operating regions of accumulation, where the oxide layer dominates; depletion, where the semiconductor capacitance acts in series with the oxide; inversion, where the semiconductor capacitance dominates due to largest depletion layer. This is for high frequency measurements where the inversion channel does not contribute to the capacitance. (b) MIM capacitor with either a linear (SiO_2) or tunable (perovskite) insulator.

using SiO_2, the capacitance will be constant across the bias range. MIM structures are the closest forms of capacitor to what is expected in more common standalone devices, but with considerably scaled dimensions. Figure 3.1 (b) shows an expected CV trend in a MIM capacitor.

For each described structure the insulator and electrode are both critical in the design and function of the capacitor. The choice of insulator can affect capacitance response to an applied voltage (Figure 3.1 (b)), as well as improve capacitance density using high-κ dielectrics. However, the use of certain insulators will also impact the leakage current through the device, which ideally should be minimised to retain charge storage and eliminate unwanted power usage. Further to the insulator, the type of metal used to gate the capacitance plays a crucial role. For example, polysilicon has been

used for a number of years in state-of-the-art MOSFETs, but the requirement is now shifting back to metal substitutes. Certain oxides, such as the perovskite $SrRuO_3$, can be used as a metallic electrode for MIM devices. They offer lattice matching properties with perovskites that promote the epitaxial growth of subsequent perovskite insulators. This design is explored further into the chapter, and the implementation is presented in chapter 4. Therefore, designing high quality capacitors using either MOS or MIM structure requires the correct conducting and insulating material for the application at hand.

Characterising the device is a crucial aspect of thin film design and implementation. For characterisation, the techniques can be split into two broad categories: electrical and material characterisation. Electrical results enable the exploration of properties under the application of an electric field, and can constitute current and capacitance trends of a thin film. Capacitance is the ability of a body to store electrical charge, and for a parallel plate capacitor the results depend on the geometry of the device. In addition, the permittivity of a chosen insulator situated between the electrodes also increases the capacitance due to the screening of the electric field. Leakage current, as previously mentioned, should be minimised in order to retain the charge stored on the electrode.

Material characterisation allows closer inspection of the individual material properties. Techniques including X-ray diffraction (XRD) and transmission electron microscopy (TEM) are used to study the microstructure and crystallinity of a material. Raman spectroscopy shows evidence for the composition of a film, or the phase of a perovskite. X-ray photoelectron spectroscopy (XPS) can be used to study film composition, and atomic force microscopy (AFM) and related modes of this experimental technique is used for topography and grain size analysis, as well as

measuring current or electrostatic properties for a film. Each technique is explored in detail further into the chapter. These methods of electrical and material characterisation of thin films are used extensively in this thesis.

Before characterisation may take place, the films must be grown to a certain specification. Perhaps the most important is the thickness of the required film. However, when films of thickness approaching 1 nm are needed, the deposition technique must be able to precisely control the growth of the films. Thin film deposition can be split into two main categories: physical vapour deposition (PVD) and chemical vapour deposition (CVD). For the purpose of this thesis, pulsed laser and sputter deposition were conducted as forms of PVD, and atomic layer deposition as a CVD technique, with each having corresponding advantages and disadvantages.

The aim of this chapter is to introduce the MIM capacitor, a ubiquitous device in many forms of integrated circuitry, and the basis of the structure used in this thesis. Due to its nature, thin films are of vital importance for the implementation and high quality fabrication and characterisation of the MIM capacitor. The materials under investigation for the insulating and conducting components of the MIM structure are shown, as well as the required substrates for growth. The characterisation techniques used to study each device and material are introduced. Finally, the deposition methods are shown which were used to fabricate the MIM capacitors.

3.2 Thin Film Capacitors and Materials

The discussion of capacitance in this thesis is based upon the parallel-plate structure, in particular the MIM capacitor. Charge is added onto one of the electrodes and compensated on the opposite plate, introducing an electric field that is situated across the insulating material. The equation that describes the capacitance in this regard is well known, and derived in chapter 2. Introducing a high-κ dielectric in-between the metallic plates acts to increase the capacitance due to an induced polarization, which reduces the electric field across the device. Other capacitors are also in production, such as the inter-digital electroded device in which the electric field is applied across the plane of the insulator [2]. However, in each design, thin film insulating and conducting materials are necessary.

Figure 3.2 shows the cross-section of a MIM capacitor, including electrodes, insulating layer and the required substrate. Also shown is the top view of the capacitor in which an array of electrodes is situated for electrical measurements. The substrate is the ground template for the ensuing thin films, with a possible adhesion layer situated between the bottom electrode and substrate. The adhesion layer is a thin 10 nm Ti film, and is discussed in detail in the next section. Each structure was designed with access to the bottom electrode for contacting the electrical probes. The top electrodes were deposited using electron beam evaporation and patterned in a lift-off process. The resulting array of square electrodes is seen in figure 3.2, and widths varied between 50 μm to 300 μm.

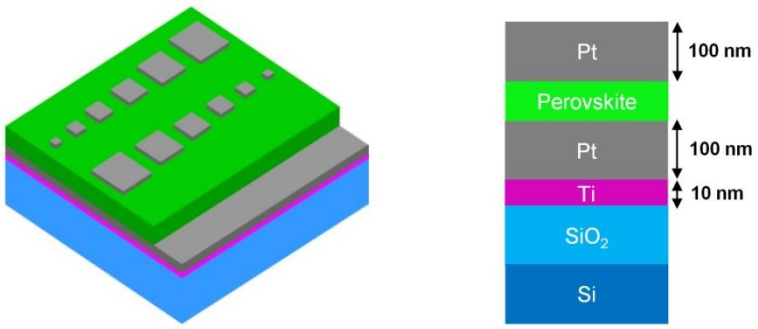

Figure 3.2: Schematic cross-section and full structure of the fabricated MIM capacitors. A thin section of the bottom Pt electrode is visible for contact with the probe.

3.2.1 Insulator choice

The choice of insulator is perhaps the most critical part of the MIM design. The job of an insulator first and foremost is to impede the flow of current such that charge does not leak from one electrode to the other. However, many such leakage mechanisms do impact the charge storage capabilities of capacitors, particularly in thin films. Poole-Frenkel emission is one such mechanism in which defects, such as oxygen vacancies, control the flow of current through the insulator as bulk trapping sites for charge carriers [3, 4]. Schottky emission is another mechanism by which electrons are controlled at the interface by a Schottky barrier, after which oxygen vacancies may again act as defects for trap-assisted conduction through the bulk of the insulator [5 - 7]. In either model, the oxygen vacancy is regarded as a possible defect in the insulating film that controls the flow of leakage current. Therefore, in oxide-based insulators, understanding the role of the oxygen vacancy and reducing the density of this defect in thin films is vital for limiting leakage current. A recent first-principles simulation study has shown the impact of migrating oxygen vacancies in strained $SrTiO_3$ [8]. Strain is an important parameter in the design of thin films, and the choice of substrate plays a central role. The choice of substrate is discussed in the following sections.

In addition to an insulator's ability to block current flow, its capacitive properties are also an essential characteristic, and derive in part from the polarizability of the material. Chapter 2 explored the differences between linear and tunable dielectrics, as well as introducing ferroelectricity, which all relate to the capacitance response to an applied electric field. In non-volatile memory applications, an insulator must be ferroelectric and retain its charge state after removal of the power source, in addition to reducing any leakage current that may cause a loss of the stored data. FRAM is an example of ferroelectric insulators as described in [9]. For applications of tunable filters or impedance matching, paraelectricity displaying decreasing capacitance with an applied electric field is necessary. Studies have focused on the dielectric quality of tunable materials, such as using ion beam assisted PLD [10] and chemical solution deposition methods [11], as well as deriving a model for the non-linearity of such devices as a function of geometry and temperature [12]. However, in either non-volatile memory applications, or tunable devices, perovskite material are suitable candidates for the insulating layer in the MIM stack. With correct composition of Ba or Sr, the phase transition temperature may be tuned in order to reach either the paraelectric or ferroelectric phase at the operating temperature. Further difficulties may arise in the crystallisation of the material as certain applications require temperatures of fabrication below a critical value. Chapter 5 explores the temperature of growth of perovskites using three thin film deposition techniques. In addition to ferroelectricity and tunability, high-κ insulators achieving greater capacitance density have been incorporated into modern digital logic gates [13]. In either application of thin film capacitors, the thicknesses required are now on the scale of the interfaces between the surrounding electrodes. In this regard the boundary conditions can play a critical role in the properties of very thin films, in particular the perovskite [14].

For the purpose of this thesis it is critical to grow ferroelectric thin films in order to investigate negative capacitance. As this negative region is unstable in most situations, placing a positive capacitance in series with the ferroelectric is vital for the stability of the system. As shown in chapter 4, the design of the capacitors will be a bilayer of a ferroelectric grown onto a paraelectric material, creating an insulating thickness in the MIM that constitutes both the negative and positive capacitance. The choices of materials are $BaTiO_3$ for the ferroelectric due to the correct phase transition temperature enabling the stabilisation of negative capacitance at room temperature, and paraelectric $SrTiO_3$ due to its high-κ property. The results show that under correct temperature and degrees of film thickness the total series capacitance is larger than the positive capacitance in the series. This will only originate if one of the capacitances is negative, which is due to the ferroelectric phase of the $BaTiO_3$ layer. $BaTiO_3$ and $SrTiO_3$ are also studied in terms of dielectric and material quality as a function of growth temperature and deposition technique for low temperature growth, as well as tunable and ferroelectric applications. $Ba_{0.8}Sr_{0.2}TiO_3$ is also studied in order to investigate the tunable property of the perovskite as an improvement over pure $SrTiO_3$.

3.2.2 Electrode choice

In a parallel-plate capacitor the area of the electrode is proportional to the achieved capacitance. Therefore, there is a need to control the areal dimension of the electrode, whereas the thickness is less critical. As previously stated, the electrodes in this thesis were fabricated using a standard photolithography and lift-off patterning process. Electrode dimensions were therefore well controlled and could be used in the extraction of permittivity using equation 2.9 once the capacitance was measured. Thicknesses of the deposited thin film electrodes are shown in the cross-section in

figure 3.2. The remaining design aspect for the electrode is the choice of material. Three electrodes were used in this thesis for the MIM capacitors: Pt/Ti, TiN and $SrRuO_3$. Not only should the electrode be conducting, the bottom plate acts as an initial growth layer for the depositing insulator and can control the texture, microstructure and overall electrical properties of the capacitor.

Platinum is chosen in this thesis as an electrode due to its chemical inertness and wide ranging usage in the electronics industry. The metal also has low resistivity as shown in table 3.1, showing the lowest value when compared to the other chosen materials. A major drawback of Pt is the cost of this transition metal due to its rarity. However, a further issue with Pt electrodes is their poor adhesion to Si, which is critical for MIM structures utilising a Si substrate. For this reason, a Ti adhesion layer is deposited onto the initial oxidised Si, creating a total substrate and bottom electrode stack of $Pt/Ti/SiO_2/Si$. This structure is used extensively throughout studies on MIM capacitors [15 - 20], and has been widely studied due to its widespread usage in thin film design. It is shown that the Ti layer can diffuse through the bottom Pt layer through grain boundaries and accumulate on the top Pt surface [21 - 28]. Due to Ti readily oxidising at ambient temperature, TiO_x compounds may be formed on the bottom interface where the initial growth layer of the ensuing desired insulating film will be. This is electrically equivalent to a series capacitance and therefore may

	ρ (μ Ωcm)
Pt	**30**
TiN	**< 300**
$SrRuO_3$	**300**

Table 3.1: Measured resistivity of the three electrodes used for the MIM capacitors. Values were obtained using 4 - probe sheet resistance measurements and measuring the thicknesses of the films using ellipsometry.

severely degrade the high-κ, ferroelectric, or tunable properties of a perovskite. Studies on Ti causing electrical shorts [29], or agglomerating Pt over certain exposure to high temperature [30, 31] can also lead to catastrophic consequences on thin film MIM capacitors. Furthermore, it has been reported that carbon contamination may be introduced from the crucible during electron beam evaporation of Pt [32], and may be the cause of electrically asymmetric characteristics in MIM capacitors from a fixed positive charge layer [33]. As this large body of literature suggests, the choice of Pt/Ti bottom electrodes does come at a cost, and the thermal budget and deposition of the electrodes should be thoroughly considered before deciding upon their usage. Chapter 5 discusses some of the impacts of this electrode on the characteristics of perovskite MIM capacitors.

As a cheaper alternative, TiN was also chosen as an electrode for the design of the MIM capacitors. This material is extremely hard, chemically and thermally stable [34], with low electrical resistivity (table 3.1). Many applications have already been found for TiN, such as adhesion layers [35], diffusion barriers [36], gate electrodes for CMOS [37] and many more [38, 39]. The TiN electrodes in this thesis were DC magnetron sputter deposited in a mixture of argon and nitrogen gas. The films have been extensively studied elsewhere [40]. It was found that increasing the nitrogen concentration during deposition reduced the resistivity of the films, reaching a low value of 80 μΩcm. Thermal stability was shown up to 1000 °C. However, a drawback of using the TiN films is the large lattice constant, and conflicting thermal expansion coefficient of the material over that in the perovskite insulators. Issues such as delamination and pin-holing occurred in the insulating layers undergoing post-deposition anneals. In order to mitigate these adhesion issues, a multilayer approach was used. Ultra-thin insulating layers were deposited and post-annealed, followed by

another ultra-thin film deposition. The process was cycled, with each new thin film undergoing an anneal before the next thin film was deposited, until the desired film thickness was reached. The multilayer approach is studied extensively in ref. 41. Furthermore, in chapter 5 it is shown that removing the necessity of the evaporated Pt bottom electrode and the possible introduction of carbon contamination, the leakage current is electrically symmetric in MIM devices utilising TiN bottom electrodes.

One further electrode choice is the perovskite $SrRuO_3$. This differs from $SrTiO_3$ only through substitution of Ti with Ru. However, its key property over that of insulating $SrTiO_3$ is it is a conducting oxide. The metallic nature of this perovskite was discussed as far back as 1992 by Eom *et al* [42] with regards to thin-films, and a recent material science review approach by Koster *et al* in 2012 [43]. The measured resistivity of the material is given in table 3.1. $SrRuO_3$ in this thesis is grown using PLD, and if resulting perovskite insulators are to be deposited, the full MIM structure may be kept under vacuum during the deposition. This may lead to reduced defect states at the interfaces, as shown to be problematic in the previously discussed Pt/Ti layers. A major advantage of using $SrRuO_3$ for an electrode is due to the closely matching material properties to perovskite insulating layers grown on top of this bottom electrode. The pseudocubic lattice constant in $SrRuO_3$ is 3.93 Å [43 - 46], which is close to that in $SrTiO_3$. Therefore, due to the similar crystal symmetry and close matching lattice constants, epitaxial growth of $SrTiO_3$ on bottom electrodes of $SrRuO_3$ is possible. For epitaxial growth, the films are clamped to the underlying layer and deposition ensues in a highly ordered phase. Therefore, no grain structure or resulting grain boundaries will affect the characterisation and properties of the film. With epitaxially grown perovskite thin films, properties matching that of single crystals may be achieved [47, 48]. For this reason, epitaxially grown perovskite MIM capacitors are used for the investigation of

negative capacitance in chapter 5. Uniform strain may also be imposed on insulating layers that are clamped to the bottom electrode. Correct straining may favour the c-axis oriented ferroelectric phase, i.e. under compressive in-plane stresses; however, under tensile straining, other such phases may be favoured [49]. The substrate also plays a major role in the epitaxial growth and induced straining of the resulting insulating films. The substrate choice is explored in the proceeding section.

3.2.3 Substrate choice

Silicon has been the most widely used material in the electronics industry, primarily due to the thermally grown native SiO_2 layer. This stable insulator enabled smooth interfaces between the gate dielectric and semiconductor channel with minimised collisions and scattering of charge carriers when the MOSFET was turned on. It is still relevant in today's nanoelectronics industry to incorporate new materials with Si due to its dominance in state-of-the-art digital or analogue circuitry. Therefore, Si substrates with thermally grown native oxides are the primary substrate choice in this thesis. Problems arise due to the differing crystallography of Si with a perovskite counterpart. For example the lattice constants of the investigated perovskites in this thesis are much lower than that of Si making epitaxial growth difficult [48]. However, as the SiO_2 gate insulator has been substituted for high-κ material, the choice of Si as the basis for high performance CMOS logic may not be necessary. In fact, III - V materials have recently been proposed as a replacement for Si [50]. Nevertheless, Si is still used extensively in the electronics industry, and incorporating new materials within this framework is still pertinent.

The remaining substrate used in this thesis is single crystal $SrTiO_3$ (100). As previously discussed, Si substrates make it difficult to achieve epitaxial growth when

depositing thin film perovskites. The benefit of a single crystal $SrTiO_3$ substrate is its matching crystallography between the deposited perovskite, and very close lattice constants with the thin films. Coupled with a $SrRuO_3$ bottom electrode, each interface will offer superior perovskite/perovskite lattice matching interfaces which should promote the epitaxial growth of each layer. The lattice matching in epitaxial films will promote in-plane strains which are controlled by the thick substrate. The misfit strain between the underlying substrate and deposited film is described by [49]

$$u_m = \frac{(b - a_0)}{b} \tag{3.1}$$

where b is the substrate lattice parameter and a_0 the lattice constant of the free standing perovskite film. Therefore, with $a_0 > b$, u_m is negative and a compressive strain is imposed at the interface. In the case of $BaTiO_3$, it has been shown previously that correct values of misfit strain can promote the c - phase where the out-of-plane polarization $P_3 \neq 0$ and in-plane polarizations P_1, $P_2 = 0$ [49]. This phase is most relevant for a parallel-plate MIM capacitor with a ferroelectric layer as polarization will be parallel to the applied electric field. The choice of $SrTiO_3$ (100) substrates with $SrRuO_3$ electrodes are the basis of chapter 4 in designing stabilised negative capacitance structures.

3.3 Electrical Characterisation

3.3.1 Small-signal capacitance - voltage

Due to perovskite material being highly non-linear under the application of an electric field, capacitance measurements are vital for understanding of the quality of the film under investigation. Extracting permittivity indicates how good a perovskite is at polarizing. Tunability is also shown in the paraelectric phase which is an important property if the material is to be used for certain tunable capacitance applications. Capacitance can also indicate ferroelectricity in the perovskite under correct measurement setups.

An Agilent 4294A impedance analyzer was used for small-signal capacitance measurements. The probes are attached across the MIM device as shown in figure 3.3. The procedure for measuring capacitance follows by applying a stepped DC bias, while measuring the device through an imposed AC signal. The frequencies used in this thesis vary from 1 kHz to 1 MHz. Measurements take into account parallel conductance in an equivalent parallel capacitance - conductance circuit.

The inherent nature of small-signal capacitance should mean any measurement is linearized as the signal amplitude should be small enough so as not to switch the polarization. Any measurement of a ferroelectric material using small-signal capacitance should, therefore, not contain any contribution from switching dipoles. However, there will still be some modulation to the capacitance from the remnant polarization that can be detected in small-signal measurements. Figure 3.4 shows expected trends when measuring small-signal capacitance on a thin ferroelectric film. A peak shift is observed depending on the direction of the applied electric field. The

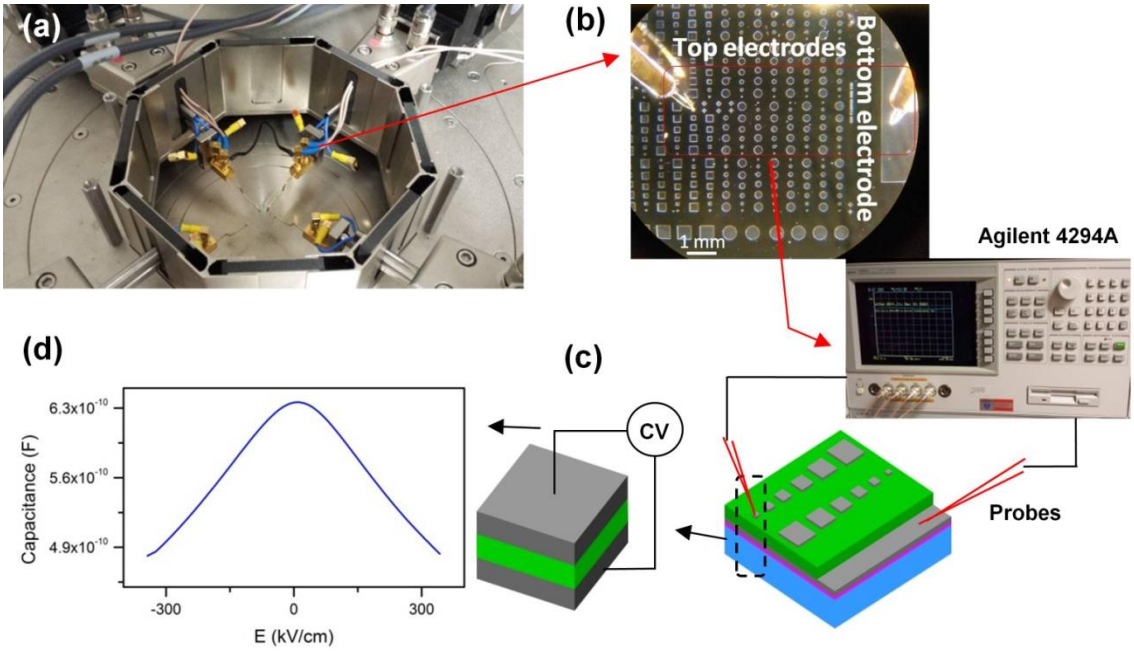

Figure 3.3: Experimental setup for CV. (a) The probe station. (b) Image of the top and bottom electrodes on a MIM sample. (c) small-signal voltage applied to one device. (d) Example capacitance trend of a tunable perovskite.

peak shift manifests signs of the switching dipoles as the coercive field is approached, showing evidence for ferroelectricity of the film. Due to the differential capacitive relationship of charge and applied voltage (equation 2.3), integrating the small-signal capacitance to reconstruct charge - voltage characteristics will show small hysteresis loops. This is due to the stimulated charge responding only to the applied small-signal, and as such the switching dipoles do not contribute greatly to the hysteresis.

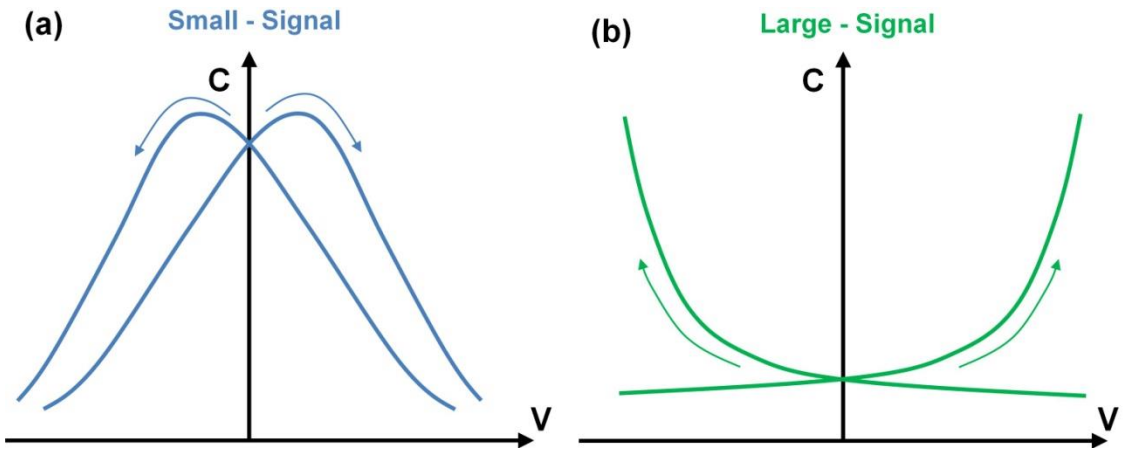

Figure 3.4: Capacitance trends measured using (a) a small - signal, (b) a large - signal.

3.3.2 Large-signal polarization – electric field

In order to capture the full polarization hysteresis loop in a ferroelectric, large-signal measurements are necessary. A large-signal measurement allows all components of the polarization to be captured, such as the remnant polarization and switching dipoles, and a full hysteresis loop is measured. A Radiant Premier II ferroelectric tester was used for hysteresis testing. The experimental setup is shown in figure 3.5. The test waveform consists of a stepped DC voltage signal that is sufficient amplitude to switch the dipoles in the ferroelectric material. The resulting current flow from the capacitor is measured and integrated to reconstruct the polarization - electric field (PE) relationship. Large-signal capacitance can be derived from the hysteresis loop from equation 2.3. The resulting capacitance will give large spikes at the switching field which is absent in the small-signal capacitance measurement (Figure 3.4). This is due to the remnant polarization switching, which gives greatest change in polarization with applied electric field.

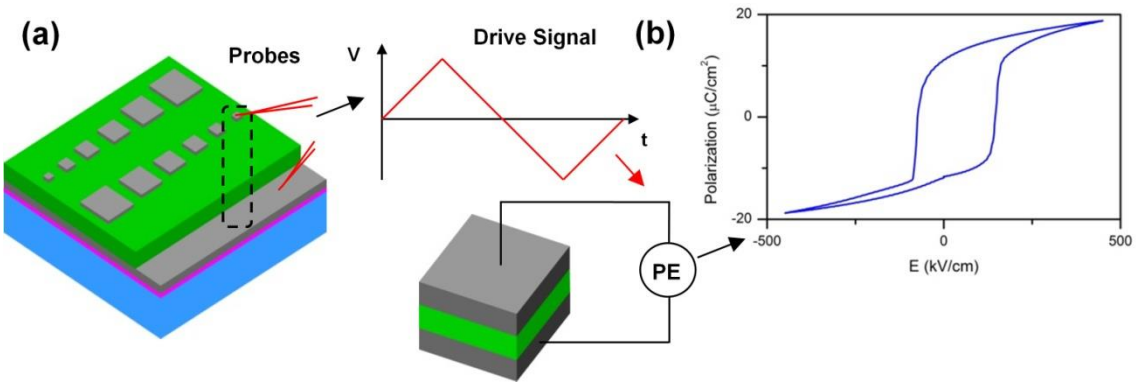

Figure 3.5: Experimental setup for PE. (a) Image of the top and bottom electrodes contacted by the probes with large-signal voltage applied to one device. (b) Example polarization response to an applied electric field in a ferroelectric.

3.3.3 Current-voltage

In addition to polarization and capacitance relationships in a perovskite, leakage current analysis also plays an important role in the characteristics of an insulator. The leakage current measurements were taken on an Agilent 4155C semiconductor parameter analyzer. Current is measured as a function of increasing a stepped DC bias applied to the top electrode. The remaining bottom electrode was grounded. Experimental setup is shown in figure 3.6. Labview was used in order to design a continuous sweeping bias and control the current meter. All leakage current measurements in this thesis are shown as current density and extracted depending on the electrode area.

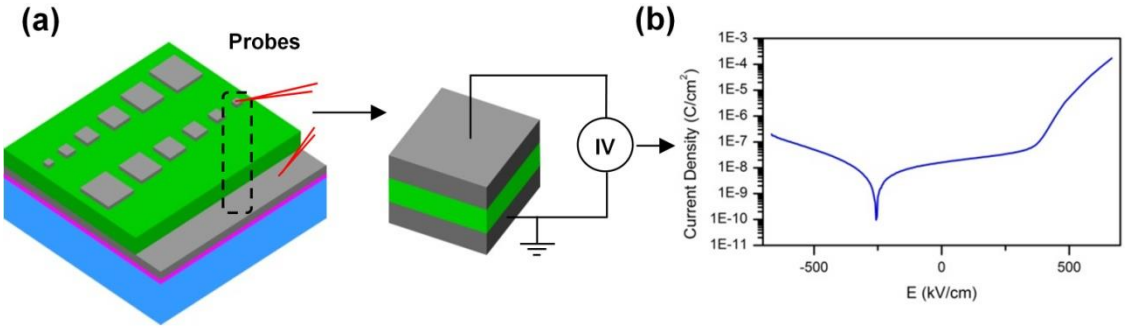

Figure 3.6: Experimental setup for IV. (a) Image of the top and bottom electrodes contacted by the probes with voltage applied to one device. (b) Example leakage current in a perovskite.

3.4 Material Characterisation

3.4.1 X-ray diffraction

X-ray diffraction (XRD) can be used to study the crystallography of a material, such as verifying crystallinity, grain orientation and further quantification of grain size using Scherrer analysis. Figure 3.7 shows a schematic of the XRD technique with a beam of X-rays of wavelength λ incident on a thin film at an angle θ. The incident x-rays are considered as electromagnetic waves that diffract when they come into contact with the atoms in the material. In a crystal or grain, the atoms are regularly spaced which creates a diffraction grating, and the resulting diffracted x-rays interfere with one another. In certain situations the diffracted x-rays constructively interfere under conditions determined by Bragg's law, described by

$$2d\sin\theta = n\lambda \tag{3.2}$$

where d is the spacing between atomic planes and n is an integer. Remaining parameters are previously defined and shown in figure 3.7. A detector is allowed to interpret the diffracted x-rays and collect information on the sample under test. A spectrum is constructed with specific diffraction peaks that correspond to the crystal structure. A first-order interpretation of a spectrum shows that if a diffraction peak is visible, the sample will be crystallised. In this thesis, XRD is used extensively for analysing perovskites and the crystallisation of the films. Epitaxial growth can also be interpreted from a spectrum if a specific arrangement of diffraction peaks is shown. Each spectrum will be discussed in detail in the appropriate chapter.

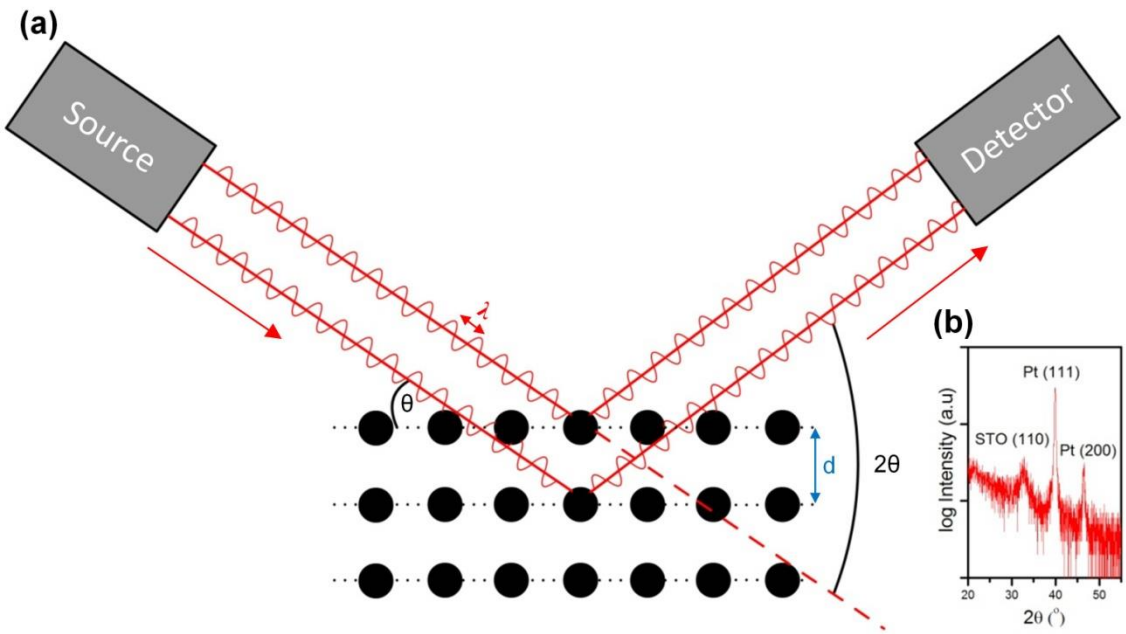

Figure 3.7: Experimental setup for XRD. (a) X-rays are incident onto a crystal plane and re-emitted from the atoms. The detector captures an interference pattern. (b) An example spectrum as the detector is moved about 2θ. Diffraction peaks are seen when constructive interference occurs as x-rays travel additional path lengths of $n\lambda$.

3.4.2 Atomic force microscopy

Atomic force microscopy (AFM) is a high resolution technique used to image the surface of thin films. In this thesis, a Park Systems XE-150 was used to perform the topography scans of the samples under test. A cantilever with a sharp probe tip is scanned across the surface of the material, and under certain conditions, forces are generated between the sample surface and probe tip. The forces are detected through the deflection of a laser beam on the top of the cantilever which then signals to a photodetector for the topographical image to be constructed. Figure 3.8 shows the experimental setup for AFM. The main mode of operation used in this thesis is non-contact AFM where the cantilever tip does not touch the sample surface. The tip is oscillated at a specific frequency close to its resonance, and van der Waals forces act upon the tip as it is scanned across the sample. The forces then decrease the frequency

of oscillation of the cantilever which is detected and interpreted for image construction. Specific modes for AFM used in this thesis are piezoforce microscopy (PFM) and electrostatic force microscopy (EFM). PFM sweeps an electric field on a spot on the material surface. Due to the piezoelectric response in a perovskite, the cantilever is deflected depending on the direction of the applied field. EFM scans a surface region of the material under DC bias in contact mode, acting to spontaneously polarize the material. The cantilever is then raised for non-contact mode and an AC signal is imposed on the tip. Scanning the matching region allows interpretation of any remnant polarization left over in the material due to an electrostatic force between the AC signal and remnant polarization. PFM and EFM are discussed in more detail in the relevant chapter.

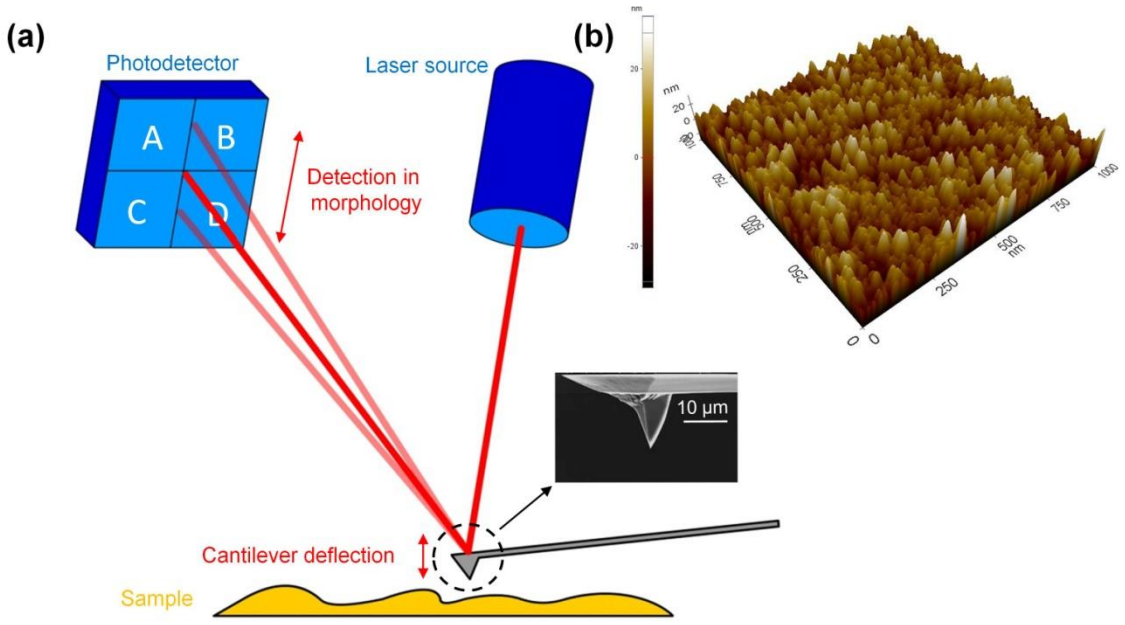

Figure 3.8: Illustration of the AFM experimentation. (a) A laser beam is directed towards the cantilever as it scans the surface of the sample. As the forces between the cantilever tip and sample surface interact the laser beam is deflected onto a photodiode. (b) Example surface scan using non-contact AFM.

3.4.3 Transmission electron microscopy

Transmission electron microscopy (TEM) allows imaging of thin specimens using an incident electron beam which passes through the sample. Electrons interacting with the sample are passed onto a detector for image construction. The benefit of using an electron microscope originates from the de Broglie wavelength of electrons, which is much smaller than what is possible in an optical counterpart (wavelength of electron λ = 2.5 pm after taking into account relativistic effects due to large accelerating voltage of 200kV, compared with wavelength in the visible spectrum λ = 390 - 700 nm). Therefore, as the electron wavelength is comparable to the interatomic spacings, much higher resolution images may be obtained. In this study, TEM was conducted on a JEOL-2100F microscope operating a 200 kV Schottky field emitter. Electron diffractions were processed using Fourier transforms in the Gatan DigitalMicrograph software. The experimental setup is shown in figure 3.9. TEM is used to analyse grain structure and epitaxial growth in this thesis, and comparing the growth and annealing impact on the thin films under investigation.

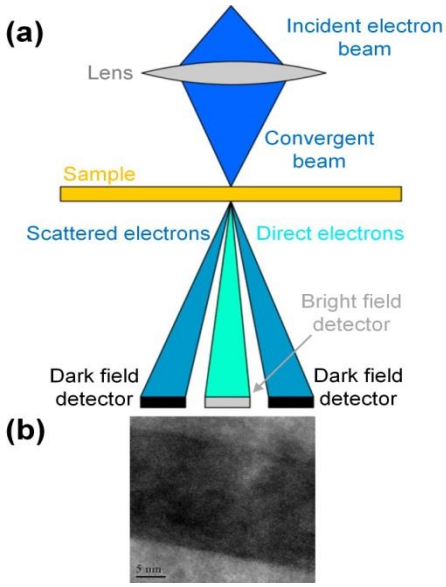

Figure 3.9: Illustration of the TEM experiment. (a) An incident beam is passed through a lens and electrons transmitted through the sample are interpreted as diffraction patterns or as an image. Bright field images use the direct electron beam, while dark field images are constructed from scattered electrons. (b) An example bright field image of a thin film.

3.4.4 Raman spectroscopy

Raman spectroscopy is a technique which uses lower frequency radiation (in comparison to the x-rays used in XRD for example) to study the vibrational modes of a material. Illuminating a sample with monochromatic light, photons of the incident beam interact with the molecular vibrations of the material causing a shift in the energy of the incident photons. This shift in energy is referred to as inelastic, or Raman scattering. A spectrum may be acquired which relates to the vibrational modes of the material. Raman scattered phonons are those whose atomic displacements provoke a change in lattice polarizability. The symmetry of the lattice can therefore determine whether a mode satisfies this change in lattice polarizability. For a perovskite in the cubic phase, which is the highest symmetry phase, each mode is triply degenerate (the individual components in all three lattice coordinate directions are equivalent) and forbidden in the first order Raman scattering [51]. When the tetragonal phase is reached the inversion centre of the perovskite unit cell is lost and Raman active modes appear. Certain modes in this phase are known as doubly degenerate (due to two equal sides with elongated c axis). The majority of the collected light is actually elastic, or Rayleigh scattered, such that no frequency or energy shift has occurred. This must be separated from the inelastic scattered signal as it brings no information about the sample under test. Figure 3.10 shows the experimental setup for acquisition of a Raman spectrum. In this thesis, Raman spectra were acquired on a HORIBA scientific LabRam using a 514 nm laser. The primary use for Raman spectroscopy was to investigate the tetragonal phase of the perovskite film. Evidence for tetragonality in a perovskite is shown by a sharp peak at approximately 300 cm^{-1} frequency shift (Figure 3.10), which is necessary for the ferroelectric phase.

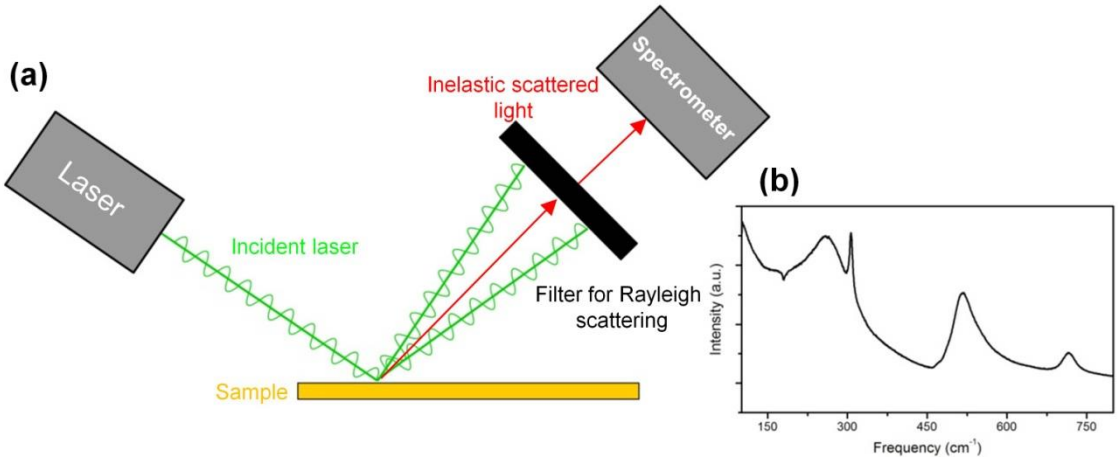

Figure 3.10: Illustration of the Raman spectroscopy setup. (a) Incident laser approaches sample and is re-emitted into elastic and inelastic components. A Filter is used to remove any elastic scattered light and remaining contribution is detected by a spectrometer. (b) Example spectrum of $BaTiO_3$ showing sharp peak at 300 cm^{-1}.

3.4.5 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a quantitative technique that can be used to study the elemental composition of a thin film. The sample surface is irradiated with an x-ray beam, and the kinetic energy of the escaping electrons due to the incident x-rays is measured. Figure 3.11 shows a schematic of the XPS setup in which an incident beam of x-rays of energy $h\upsilon$ hits the sample surface in order to excite the electrons out of the material at a depth of 1 - 10 nm. Once the emitted electrons and the corresponding kinetic energies are measured by a detector, the binding energy of the electrons can be calculated from

$$E_{binding} = E_p - (E_k + \varphi) \tag{3.3}$$

where $E_{binding}$ is the binding energy of the electron, E_p is the energy of the x-ray photons and E_k the kinetic energy of the emitted electrons measured by the detector. The term φ is the work function of the spectrometer and relates to the energy given up by the photoelectron as it is absorbed by the detector. Calculation of the binding energies allows a spectrum to be acquired, which plots the number of electrons detected at that specific binding energy. Analysis is performed on the spectrum which results in

qualitative assessment of the elements that constitute the material, and also quantification through peak broadening and electron count evaluation. In this thesis, XPS spectra were acquired on an AXIS Nova with monochromated Al K_α source. The spectra were considered for stoichiometry and carbon contamination analyses.

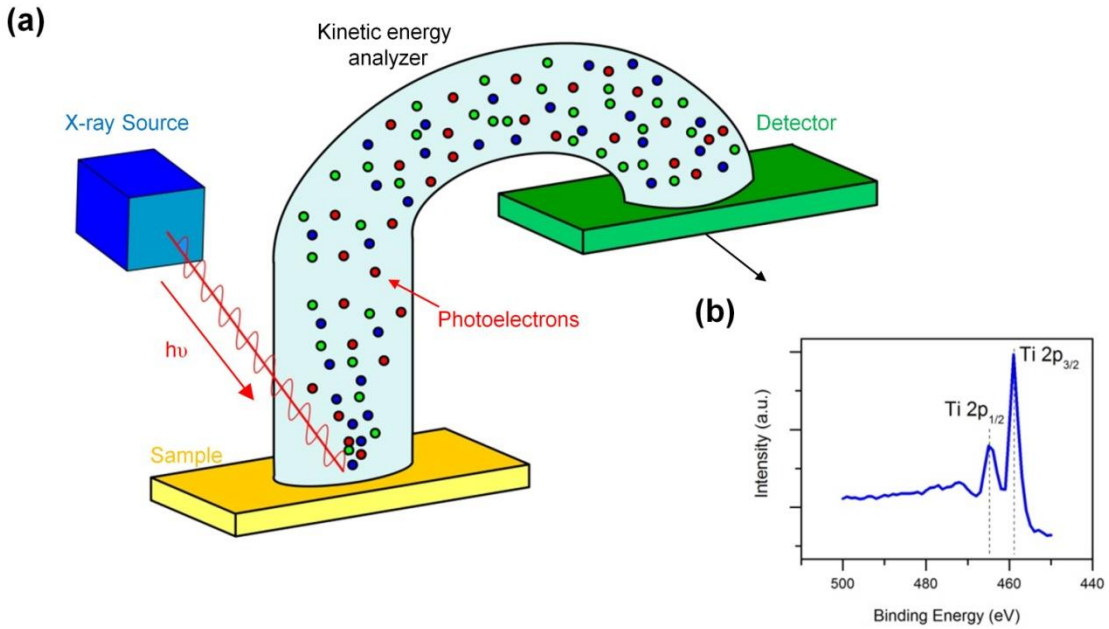

Figure 3.11: Illustration of the XPS experimentation. (a) Incident x-rays promote electrons of different kinetic energies out of the sample under test. Detection occurs relating to the electron kinetic energy. (b) Example spectrum from the detector.

3.5 Thin Film Deposition

The need for high quality thin films has been discussed in this thesis, and control over the thickness is an important aspect of film deposition. Various methods have been employed in order to deposit thin films, for example thermal evaporation [52], metal organic chemical vapour deposition [53] and molecular beam-epitaxy [54]. Three other techniques are explored in more detail below and were used in the fabrication of thin perovskite films in this thesis.

3.5.1 Atomic layer deposition

Atomic layer deposition (ALD) is a technique that offers excellent control over the thickness and conformal coating of a thin film [55]. It is a self-limiting processes in which the material to be deposited is constant in each cycle. It is this property that allows ultra-thin films to be deposited to a specific thickness in the sub nanometer regime, one layer at a time. Sequential steps are performed using reactions between two chemicals known as precursors. The precursors are allowed to react with the sample surface in a self-limiting manner, and the surface becomes saturated with the molecules of the precursor. The film thickness is then selected by varying the number of cycles of precursor reaction.

Figure 3.12 shows the four main steps for film growth through ALD. Each cycle is considered as one step in the deposition process. The initial step is the exposure of the sample surface to the first precursor (figure 3.12 (a)). This saturates the surface with the precursor and an initial layer is formed. The following step is to purge the chamber, removing any non-reacted precursors or by-products of the reaction (figure 3.12 (b)). In the third step, the secondary precursor is introduced into the chamber for reaction (figure 3.12 (c)). Following the formation of the secondary layer from this

precursor the chamber is purged again (figure 3.12 (d)). The following four steps are repeated until the desired film thickness is reached (figure 3.12 (e)).

In this thesis, thin film $SrTiO_3$ is grown by ALD using Sr and Ti precursors [56]. Due to the limiting temperature of 250 °C such that precursors are not damaged, deposited films are amorphous. An annealing schedule was then performed (see chapter 5) in order to crystallise the $SrTiO_3$ thin films under specific temperatures for back-end-of-line integration.

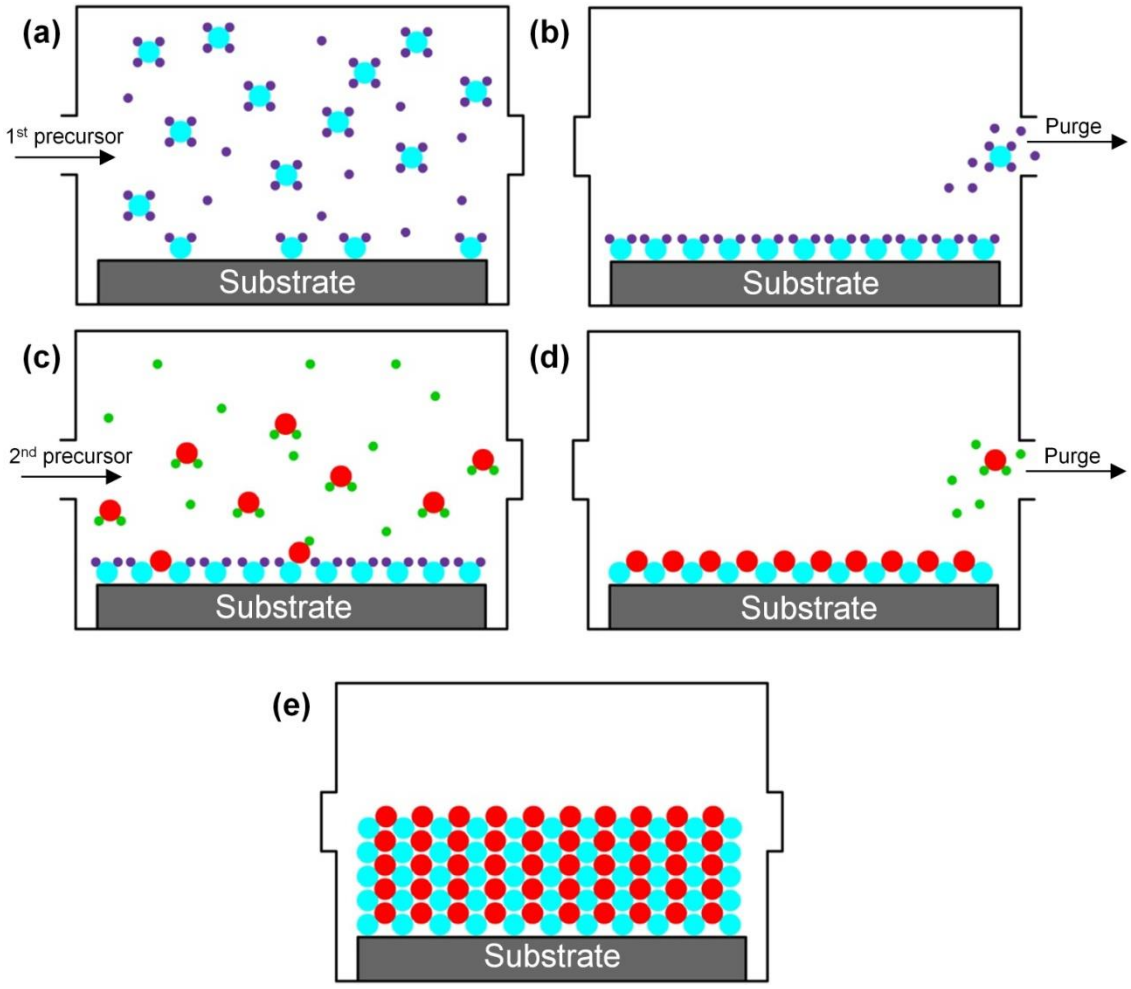

Figure 3.12: Schematic of the deposition process using ALD. (a) The initial precursor is introduced into the chamber. (b) Leftover precursor is purged from the chamber. (c) Second precursor is introduced into the chamber. (d) The chamber is purged of remaining precursor. (e) Steps (a) - (d) repeated until desired film thickness is grown.

3.5.2 Pulsed laser deposition

Pulsed laser deposition (PLD) allows the growth of thin films through use of a high-energy laser being pulsed against a specific target [57]. The laser is focused through a lens outside a chamber, and pulsed in short durations which evaporates material from the target. The target is rotated to ensure there is a uniform coverage on the surface. This ablation process creates a plume of plasma that leads to the deposition of material on a desired substrate. The substrate may be heated to specific temperatures to aid in the crystallisation of the thin film. During the deposition, the chamber may be under ultra-high vacuum, or filled with background gas, such as oxygen in titanate growth. Figure 3.13 shows a schematic of the process of PLD. A number of factors can affect the deposition rate, such as laser energy, gas pressure in the chamber, and target material being deposited. However, PLD suffers from small deposition areas and poor uniform coverage. In this thesis, films from 13 nm - 380 nm are grown using PLD for both tunable applications and negative capacitance. $BaTiO_3$ and $SrTiO_3$, along with $Ba_{0.8}Sr_{0.2}TiO_3$ were grown and measured.

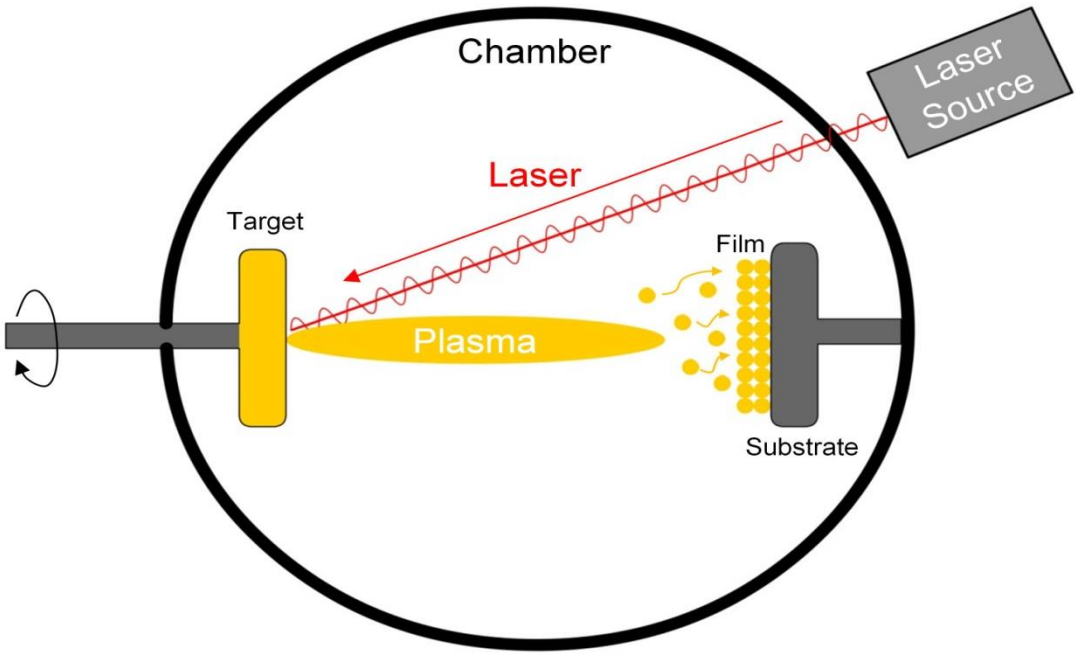

Figure 3.13: Schematic of the deposition process using PLD.

3.5.3 Sputter deposition

The process of sputter deposition involves ion or atom bombardment towards a target causing the material to be ejected. The expelled material is then deposited onto a substrate [58]. Usually, Ar^+ ions are used for the bombardment and ejection of the target material; however, heavier elements such as krypton may be used. Depending on the pressure in the sputter chamber, the ejected atoms or ions are fired directly towards the substrate, or allowed to collide with the gas introduced into the chamber and diffuse towards the substrate. Gas pressure can consist of Ar, or oxygen may be included for the deposition of titanates. For the deposition of insulating material such as $BaTiO_3$, RF sputtering is employed in which there is an oscillating bias across the anode and cathode of the sputter chamber. This removes any excess build-up of charge on the insulating target during deposition. The schematic of RF sputter deposition is shown in figure 3.14. In this thesis, RF sputter deposition was conducted in order to grow thin films of $BaTiO_3$. The substrate heater was limited to 400 °C and a post-deposition annealing schedule was conducted on the films for crystallisation purposes. DC reactive magnetron sputtering was also used to grow thin TiN electrodes.

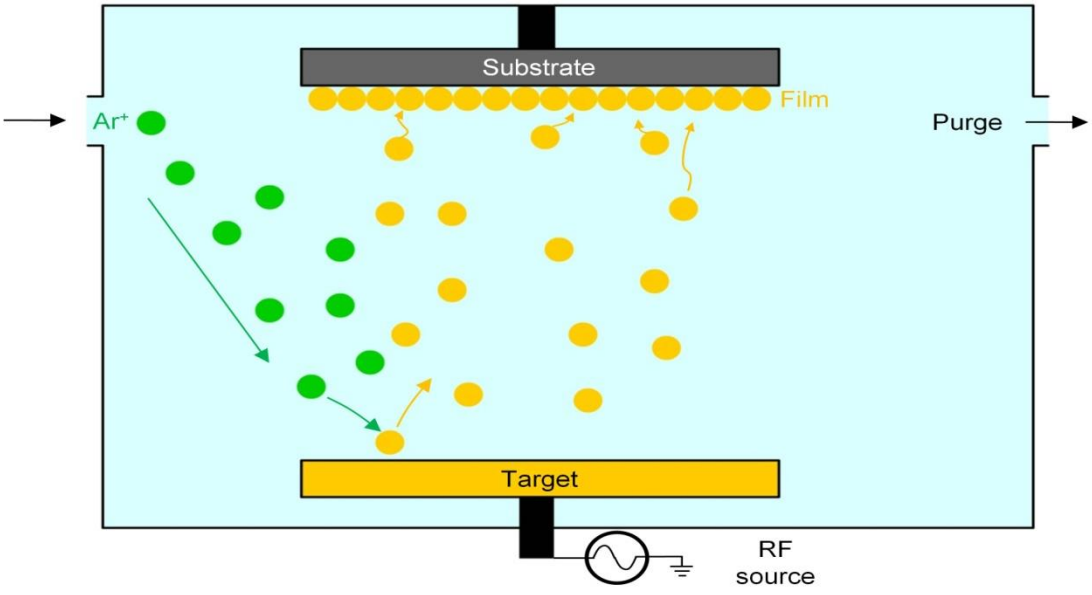

Figure 3.14: Schematic of the growth process using RF sputter deposition.

3.6 Summary

In this chapter, the importance of high quality thin films was highlighted for the nanoelectronics industry. The progression of Moore's law and the scaling of electronic devices have ensured that new materials are needed in order to further advance electronic components and circuits. Perovskite insulators in MIM capacitance structures were shown to be suitable candidates for this purpose. $BaTiO_3$, $SrTiO_3$ and $Ba_{0.8}Sr_{0.2}TiO_3$ are studied in this thesis, along with Pt/Ti, TiN and $SrRuO_3$ thin film electrodes. The substrates of choice are Si and $SrTiO_3$, which both offer different structural characteristics.

In order to characterise the thin film perovskites, material and electrical techniques were shown. The electrical characterisation involves measuring current and capacitance trends for the perovskites. Material characterisation techniques were shown to include XRD, AFM, XPS, Raman and TEM. The combination of all the measurement techniques allows extensive characterisation of the fabricated thin films.

Furthermore, high quality perovskite films need to be deposited in a well-controlled process. A key aspect of the MIM capacitor fabrication process is the deposition of the insulating film which needs to be of a certain thickness, and also stoichiometric. Three techniques were discussed, which were ALD, PLD and sputter deposition. Each technique is used for perovskite film deposition and the results are shown in the following chapters.

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Chapter 4

Negative Capacitance in Ferroelectric Oxides at Room Temperature

4.1 Introduction

Negative capacitance has attracted attention in recent years as a technology that can extend the lifetime of Moore's law. The groundwork firstly lay out by Salahuddin and Datta showed that the inclusion of negative capacitance in the gate stack of a MOSFET may reduce the subthreshold slope [1, 2]. A review article followed, asking whether negative capacitance may 'come to the rescue' and overcome the 'Boltzmann tyranny' [3]. Albeit an open ended question, the importance of negative capacitance was highlighted. Ionescu *et al*. have claimed a reduced subthreshold slope was due to negative capacitance using a copolymer P(VDF-TrFE) in the gate stack of a MOSFET [4, 5]. A theoretical framework for the surface potential in negative capacitance MOSFETs was also given [6], and limitations to negative capacitance due to multidomain ferroelectricity [7] have been shown. However, the use of a

ferroelectric oxide demonstrating negative capacitance has only been seen in $Pb(Zr_{0.2}Ti_{0.8})O_3$ in a stabilised series capacitance model at temperatures up to 773 K and beyond the Curie temperature (729 K from ref. 12) of the ferroelectric [8].

The importance of negative capacitance in FET gate stacks originates from the proposed voltage amplification; that is, an increase in the surface potential, ψ_s, over the applied gate voltage, V_G (figure 4.1). A first understanding of negative capacitance and its significance on the subthreshold slope (figure 4.2) is shown in equation 4.1

$$SS = \frac{\delta V_G}{\delta(\log_{10} I_D)} = \frac{\delta V_G}{\delta \Psi_s} \cdot \frac{\delta \Psi_s}{\delta(\log_{10} I_D)} \tag{4.1}$$

where $\delta V_G/\delta \Psi_s$ is the body factor term '*m*' that describes the achieved surface potential from the applied gate voltage, I_D is the drain current and *SS* the subthreshold swing. From equation 4.1, it is shown that a steep slope is most desirable as this requires less voltage to transition the FET from its off to on state. Figure 4.2 highlights this result, where the steep slope indicates a *SS* < 60 mV/dec, achieving a lower threshold voltage, V_{TH}, and reduced off current, while maintaining high on current at lower applied V_G. The *SS* is discussed in further detail in chapter 2.

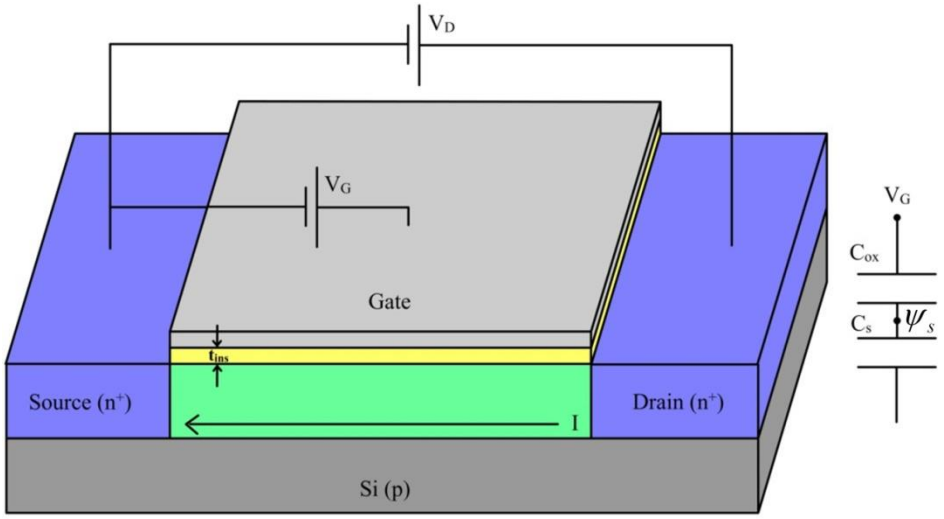

Figure 4.1: Illustration of a MOSFET under gate and drain bias voltage. Equivalent circuit shown as a series of the insulator and semiconductor capacitances with gate and surface potential.

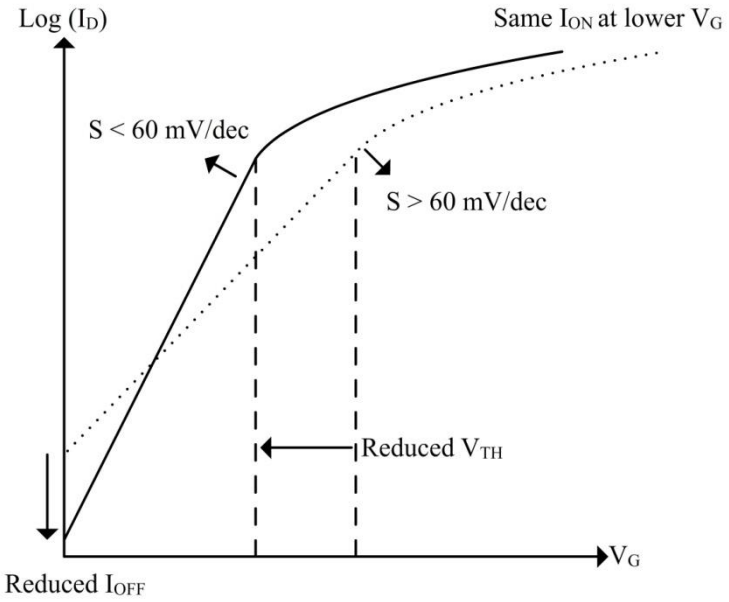

Figure 4.2: Sketch of the subthreshold region in a MOSFET showing a steep < 60mV/dec and a standard > 60mV/dec slope.

Expanding on equation 4.1 and defining the body factor in terms of the equivalent series capacitance model shown in figure 4.1, the influence of negative capacitance on the *SS* becomes evident. Equation 4.2 shows the body factor term as a function of capacitance

$$m = \frac{\delta V_G}{\delta \Psi_s} = 1 + \frac{C_s}{C_{ox}} \tag{4.2}$$

where C_s is the semiconductor contribution to capacitance from the channel of the MOSFET and below, while C_{ox} is the capacitance originating from the oxide thickness (figure 4.1). It is immediately apparent how high-κ materials impact the body factor term: increasing C_{ox} using a high-κ material allows $m \rightarrow 1$, and therefore ensures the majority of the gate potential is dropped across C_s ($V_G \approx \Psi_s$). However, if C_{ox} can be made negative, m can be < 1, and the internal surface potential is allowed to change more than the externally applied gate voltage, V_G. Negative capacitance, as defined in ref. 3, causes a decrease in voltage as charge is added; this decreasing voltage across

negative C_{ox} is given as a feedback voltage to the surface of the channel [1], which was first proposed by Feynman [9].

The property of negative capacitance in ferroelectric oxides was first hinted at through negative slopes in hysteresis loops [10]. When considering the definition of capacitance (dQ/dV), this is an important finding as negative slopes translate into negative capacitance. Bratkovsky and Levanyuk reported the significant result of domain structures in ideal thin films with imperfect screening, and as such, the role of depolarizing fields is highlighted. However, as previously discussed, experimental evidence for a reduced subthreshold slope originating from negative capacitance has been limited to a coploymer P(VDF-TrFE) [4, 5]. The results demonstrate a sub-threshold swing less than 60 mV/decade over limited current ranges below 10^{-10} A/um, compared with a typical MOSFET threshold current of 10^{-7} A/um.

The study mentioned above using the perovskite ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$ in bilayer capacitors has been shown to display effective negative capacitance [8]. Negative capacitance was stabilized across a temperature range exceeding 573 K, and therefore is unsuitable for integration into modern integrated circuits. Furthermore, stabilization was shown at temperatures up to 773 K [12] and beyond the Curie temperature of the ferroelectric. Explanations for this may be due to straining as the latticed matched structures impose strains that lead to increases in the Curie temperature [11]; however, this was not discussed in the study. The study highlighted that using low Curie temperature materials will enable negative capacitance stabilization at room temperature, such as $BaTiO_3$ used here.

In this chapter, effective negative capacitance in $BaTiO_3$ is shown at room temperature for the first time. $BaTiO_3$ is ferroelectric at room temperature, and is used as the negative capacitance layer in a series capacitance model. Capacitance

enhancement of the series capacitor system is the key result from the experiments due to there being a negative capacitor in series with a positive capacitor. The modelling framework is given, and is based upon Landau Devonshire (LD) theory shown in chapter 2 of this thesis. Stabilised negative capacitance at room temperature in $BaTiO_3$ shows a further use for the already versatile ferroelectric, opening up routes for steeper subthreshold slopes and low power MOSFETs. In addition, higher density bilayer capacitors with thicker insulating layers may be designed, which achieve greater capacitance when compared with a single layered insulator counterpart. Therefore, bilayer capacitors may be a solution to dead layers, which suppresses the permittivity when film thickness is reduced.

4.2 Series Capacitance Model

Measuring negative capacitance is not straightforward as the region of interest is unstable. The region is situated at zero polarization and electric field where the slope is negative, and is shown in figure 4.3 in a simulated hysteresis plot for $BaTiO_3$. Ordinarily, the negative slope predicted by LD theory is not accessed in standard measurements and, as a consequence, hysteretic jumps in polarization occur.

It becomes important to stabilise this region by placing it in series with a positive capacitance [1, 8]. The model allows indirect measurement of negative capacitance through the total capacitance of the series being larger than the constituent positive capacitance. The model of this system is shown in figure 4.4, and equation 4.3 describes the characteristics

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} \tag{4.3}$$

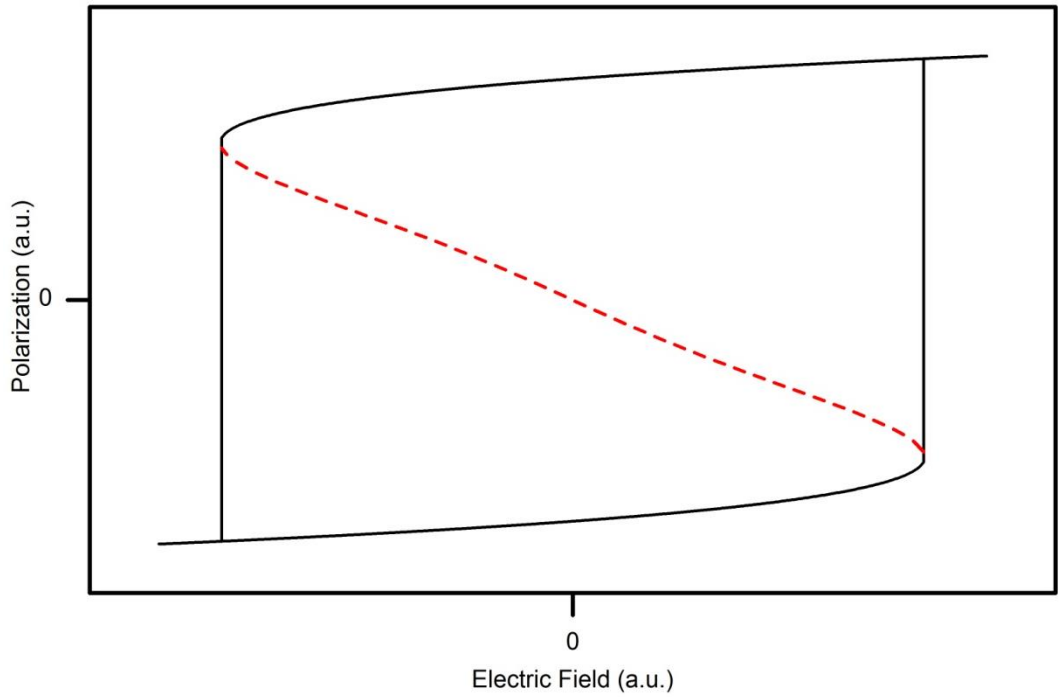

Figure 4.3: Polarization vs. electric field for $BaTiO_3$ simulated using LD theory (equation 2.16). Negative capacitance region (red dashed negative slope) is situated around P = 0 and is not accessed due to instability. Material parameters were taken from reference 12.

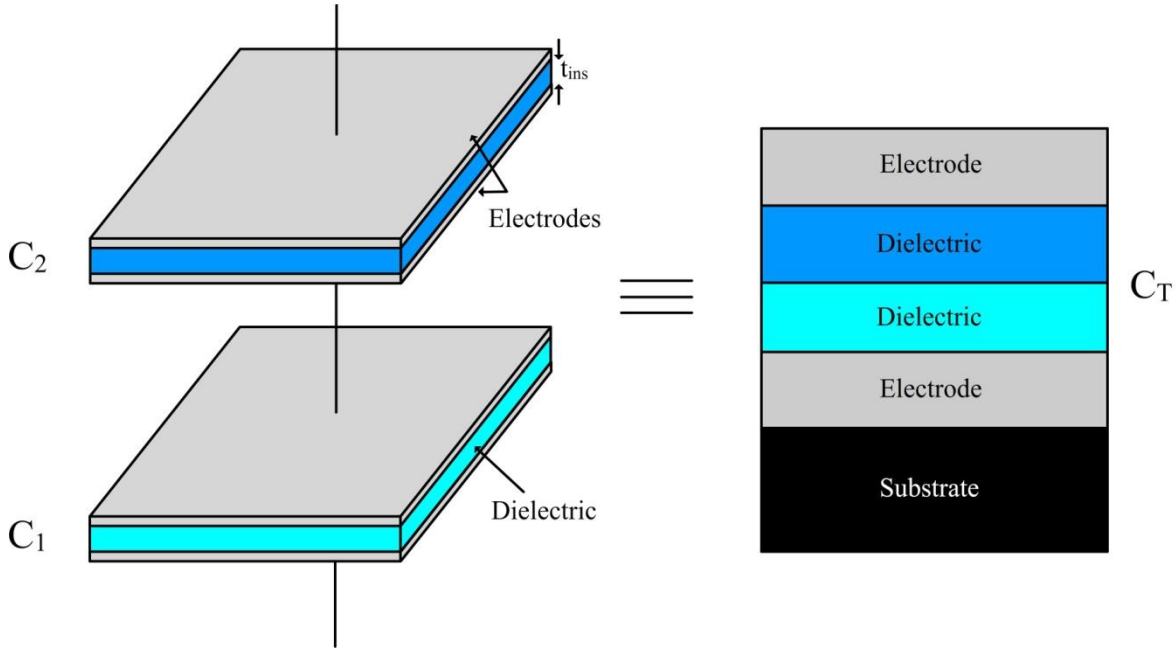

Figure 4.4: Series capacitance consisting of capacitors C_1 and C_2. The equivalent MIM stack is shown as the total capacitance C_T.

where C_T is the total measured capacitance and C_1, C_2, are the constituent capacitances shown in figure 4.4. A plot of equation 4.3 in figure 4.5 shows the impact a negative capacitance has on the total measured C_T capacitance. If capacitor C_2 is negative, C_T can be greater than C_1, the positive stabilising capacitance in the series. This is in contrast to two positive series capacitances; the total capacitance C_T is never larger than the smallest of the two contributing capacitors in this case. There is an additional region shown in figure 4.5 where C_T is negative. At this point, the capacitance system is not stabilised and hysteretic jumps in polarization will ensue, i.e. C_T acts as a standard ferroelectric capacitor. A design constraint is set on the fabrication of the MIM structure (figure 4.4) shown in equation 4.4

$$|C_2| > C_1 \tag{4.4}$$

The capacitors have to be designed with correct thicknesses using equation 4.4 in order to show effective negative capacitance at room temperature.

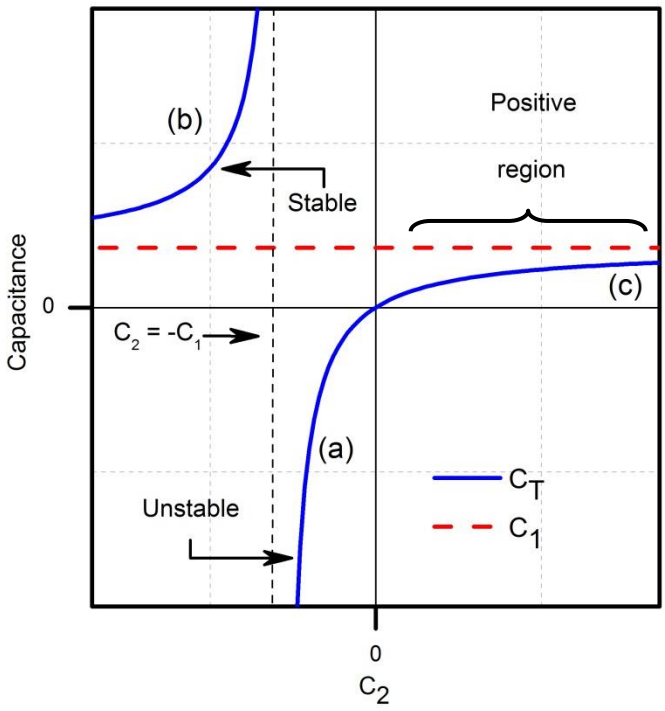

Figure 4.5: Series capacitances equation plotted as a function of capacitor C_2. When C_2 is negative the total capacitance C_T is greater than C_1.

The marked regions on figure 4.5 correspond to the energy density functions in figure 4.6. Region 'b' is identified as the design window where effective negative capacitance is stabilized, corresponding with a positive total energy density. Moreover, the total capacitance C_T is larger than the constituent positive capacitance C_1, due to the negative capacitance C_2. Region 'a' is unstable, as it has a total energy density that is negative, while region 'c' comprises two positive capacitances in series that combine to have a reduced total capacitance. This is discussed in more detail below.

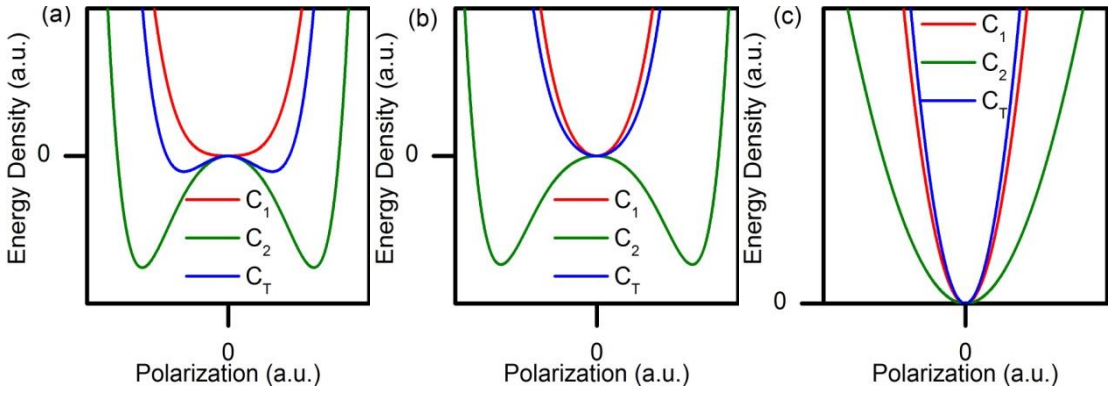

Figure 4.6: Simulated energy density at (a) 100 K, (b) 300 K, (c) 500 K. Shown is $SrTiO_3$ as C_1 at 25 nm, C_2 $BaTiO_3$ at 50 nm and the bilayer capacitor C_T of $SrTiO_3$ / $BaTiO_3$ at 25 nm / 50 nm.

In order to provide a better understanding of this phenomenon, the relationship between the total energy density and negative capacitance is described. The ability of a body to store electrical charge, *Q*, is defined by its capacitance, *C*. It can be described in terms of a change in energy density, *U*, as a function of changes in stored charge, *Q*,

$$C = \left(\frac{d^2U}{dP^2}\right)^{-1} \tag{4.5}$$

where *C* is capacitance, *U* is the energy density stored in the electric field across *C* and *P* is polarization which is a scaled version of charge. LD theory (equation 2.14) describes the ferroelectric by relating energy density to the order parameter *P*, coupled with material coefficients for the specific perovskite. For a parallel plate MIM capacitor with a single layer perovskite insulator, the energy density can be written as

$$U = t_1(\alpha_1 P^2 + \alpha_{11} P^4 + \alpha_{111} P^6) \tag{4.6}$$

where t_1 is the thickness of C_1 and α_1, α_{11}, α_{111}, are the material coefficients that describe the properties of C_1. *U* is now a surface energy density as the thickness of the capacitor is multiplied across.

The resulting capacitance based on equation 4.5 and 4.6 is given by

$$C_1 = \frac{1}{2\alpha_1 t_1} \tag{4.7}$$

where the nonlinear terms α_{11}, α_{111} are neglected as a first approximation to investigate the capacitance around zero bias where the slope is negative (figure 4.3). The significance of capacitance in equation 4.7 is its relation to the material coefficient α_1. A first order solution for the coefficient shows that $\alpha_1 = \alpha_0(T - T_c)$ [13], where *T* is the operating temperature, T_c the Curie temperature and α_0 a constant (equation 2.15). The linear coefficient α_1 is strongly temperature dependent, and further, is negative when *T* is less than the Curie temperature of the given material under investigation. Equation 4.7 shows that if α_1 is negative, then a negative capacitance will result.

For the bilayer structure shown in figure 4.4, two thicknesses contribute to the insulating layer of the MIM capacitor. Equation 4.6 can be modified in order to attribute both energy density functions from C_1 and C_2 in the bilayer

$$U_T = t_1(\alpha_1 P^2 + \beta_1 P^4 + \gamma_1 P^6) + t_2(\alpha_2 P^2 + \beta_2 P^4 + \gamma_2 P^6) \qquad (4.8)$$

where a second capacitance C_2 has been summed to the original energy function creating a total energy density U_T. The resulting capacitance derived from equation 4.8 is given in equation 4.9

$$C_T = \frac{1}{2(\alpha_1(T - T_{c1})t_1 + \alpha_2(T - T_{c2})t_2)} \qquad (4.9)$$

where T_{c1} and T_{c2} are the Curie temperatures of capacitors C_1 and C_2, respectively, and the nonlinear terms are neglected. Equation 4.9 allows simulation of the temperature dependence of the bilayer capacitance. Thicknesses are designed based on equation 4.4, with capacitance enhancement in the bilayer optimised for room temperature operation.

Figure 4.7 shows C_1, C_2 and C_T varying with operating temperature using equation 4.7 and 4.9. The material coefficients were taken from [12], α_1 for $SrTiO_3$ as C_1, and α_2 for $BaTiO_3$ as C_2. Thicknesses of the layers were 25 nm and 50 nm for $SrTiO_3$ and $BaTiO_3$, respectively. The results show that, for the selected thicknesses of capacitors, C_T is greater than C_1, the constituent positive capacitance in the series, at RT (~300 K). There is a region at lower temperature where either C_2, or both C_2 and C_T are negative. Due to C_2 consisting of a single layer of $BaTiO_3$, this operating temperature places the material in its ferroelectric phase and, as a result, hysteretic jumps in polarization occur. The origin of negative C_T at temperatures below 200 K is due to the limitation set in equation 4.4. At this temperature, $|C_2| < C_1$, and hysteretic jumps in polarization would occur in C_T, resulting in a loss of capacitance enhancement. The unstable section labelled in figure 4.5 highlights this region of operation. It is evident in figure 4.7 that stabilising a ferroelectric negative capacitor in series with a positive

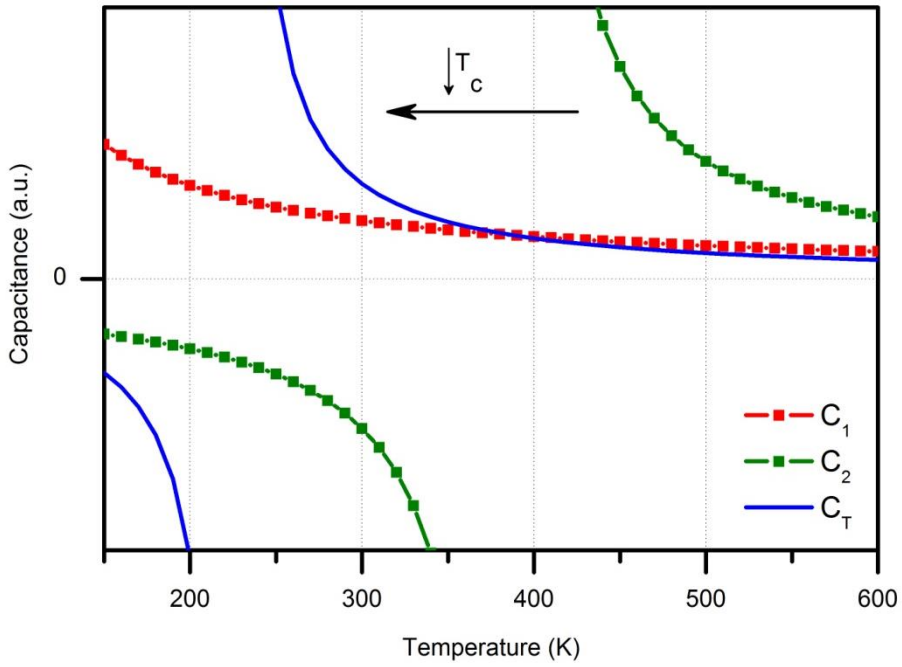

Figure 4.7: Capacitors C_1, C_2 and total capacitance C_T plotted as a function of temperature. At 300 K C_T is greater than C_1 due to negative C_2.

capacitor has the effect of shifting the Curie temperature of the system.

In order to show the influence of temperature on the design of the bilayer, a 25 nm $SrTiO_3$ single layer C_1, 50 nm $BaTiO_3$ single layer C_2 and 25 nm / 50 nm $SrTiO_3$ / $BaTiO_3$ bilayer were simulated at three different temperatures. Figure 4.8 shows both the polarization-bias (PV) and the capacitance taken as the differential of the polarization - bias. For a temperature of 100 K, the bilayer PV shows to be hysteretic (figure 4.8 (a)). Consequently, the capacitance is unstable and the dashed red region is not accessed. The capacitance of C_T as seen in figure 4.8 (b) is lower than C_1, other than at the unphysical infinite slope points shown in the hysteresis loops. The hysteresis seen in figure 4.8 (a), (b), is due to the Curie temperature of the bilayer. Figure 4.7 shows that 100 K is below the Curie temperature of C_2 and C_T, and the bilayer would produce ferroelectric characteristics. The negative capacitance region is unstable in

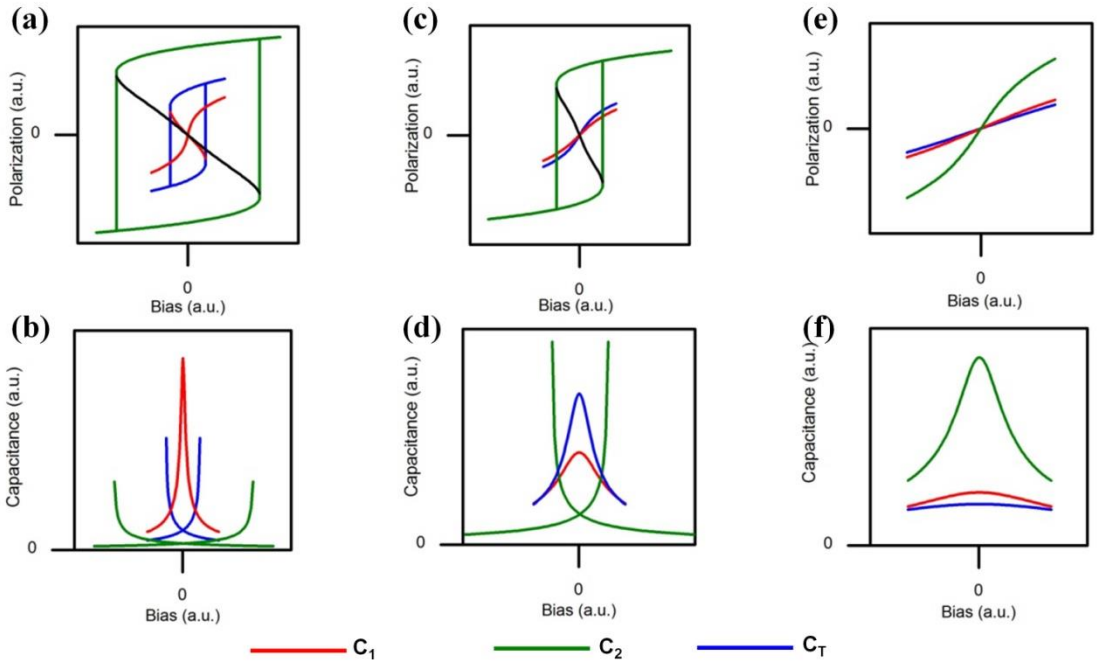

Figure 4.8: Simulated PV and CV at (a) (b) 100 K, (c) (d) 300 K, (e) (f) 500 K. Shown is the single $SrTiO_3$ capacitor C_1 at 25 nm, single $BaTiO_3$ capacitor C_2 at 50 nm, and the bilayer capacitor C_T of $SrTiO_3$ / $BaTiO_3$ at 25 nm / 50 nm.

both C_2 and C_T at this temperature. Increasing the operating temperature to 300 K, figure 4.7 shows that C_T should be greater than C_1. Figure 4.8 (c) shows no hysteresis for C_T, and further, figure 4.8 (d) demonstrates that the bilayer capacitance is greater than the constituent positive capacitor C_1. The lack of hysteresis at this operating temperature is due to the stabilised bilayer, which is functioning at a temperature greater than its shifted Curie temperature shown in figure 4.7. At this temperature the $BaTiO_3$ layer is still ferroelectric. Once the operating temperature is increased past the actual Curie temperature of the $BaTiO_3$ layer, it will transition into its paraelectric phase. When this occurs, the bilayer will be simply two positive capacitances, and the characteristics revert back to standard series capacitance analysis. This is shown in figure 4.8 (f) at 500 K where C_1 and C_2 are now greater than C_T, which is further highlighted in figure 4.5 for the positive region.

The stability issue concerned with ferroelectrics, and hence the bilayer design, can be understood in terms of the energy density function defined in equation 4.6. For each temperature of simulation in figure 4.8, a balancing of the energy functions is needed to produce stabilised capacitance enhancement in C_T. This originates from the broken symmetry of the energy function in a ferroelectric, and its strong dependence on temperature. Figure 4.6 shows energy density functions of both C_1 as $SrTiO_3$ (25 nm), C_2 as $BaTiO_3$ (50 nm) and $SrTiO_3$ / $BaTiO_3$ (25 nm / 50 nm) at each temperature described in figure 4.8. Simulated results are produced from equations 4.6 and 4.8. The critical point at 300 K in figure 4.6 (b) describes when the bilayer energy function transitions from the double minima state, whose characteristic is still shown for the single $BaTiO_3$ capacitor, to a single turning point at zero. The stabilised higher symmetry state of this function in the bilayer at 300 K allows the measured total capacitance C_T to be greater than C_1. This is due to a shallower energy density function for C_T compared with C_1, as equation 4.5 describes that a shallower energy function achieves a greater capacitance. Furthermore, using equation 4.5, the curvature of energy ensures that the capacitance is positive across all bias regions. It is therefore a consequence of the negative energy in the ferroelectric, which is where the negative capacitance region is situated, that allows a shallower total energy function in the bilayer. In turn, this leads to capacitance enhancement when the energy functions of C_1 and C_2 are summed to produce an overall shallower energy density for C_T.

The relationship in energy density shown in figure 4.6 (b) is the region labelled (b) in figure 4.5. In contrast, figure 4.6 (a) still shows double energy minima for the bilayer, a key characteristic of a ferroelectric. An unstable negative energy results that is not accessed in electrical measurements. This is region (a) in figure 4.5. Figure 4.6 (c) is at the 500 K operating temperature that produces two positive energy

densities in the individual $BaTiO_3$ and $SrTiO_3$ layers, and both are now paraelectric. The summation of each of these energy functions, based upon equation 4.8, leads to a total energy function that is sharper than either of the constituent energy functions for C_1 and C_2, i.e. the total capacitance will be less than the smallest of the contributing series capacitances (region (c) in figure 4.5). Equation 4.5 confirms that the sharper energy density for C_T at 500 K in figure 4.6 (c) will result in lower capacitance when compared to the constituent C_1 and C_2 capacitances in the series.

Based upon the preceding simulations, the following experimental section involves investigation of the structures shown in figure 4.9. The series capacitance system, consisting of a negative ferroelectric and positive paraelectric capacitor, is designed due to the instability of negative capacitance. Stabilisation is necessary as the predicted negative capacitance, in accordance with LD theory, cannot be accessed by standard macroscopic measurements. Under the application of an electric field, measurements of single layer ferroelectric films transition between the energy minima operating points (double energy minima for C_2 in figure 4.6 (b)), and the remnant polarization is switched. Thus, the negative capacitance region is not electrically active due to the instability at the origin of energy and polarization. However, the negative capacitance region, originating from the negative energy shown in figure 4.6 (a), (b), allows a total summation of the contributing energy functions of the series capacitors to be shallower than that of the constituent positive capacitance (figure 4.6 (b)). In accordance with equation 4.5, the summation of the energy densities of the contributing capacitors allows a capacitance enhancement effect in a total series capacitance system.

The series capacitor system is such that direct measurement of negative capacitance does not occur. Testing the ferroelectric oxide negative capacitance hypothesis is indirect; capacitance enhancement of the total series capacitance, C_T, over

C_1, will only be observed if there is a contributing negative capacitance (figure 4.5). This explains why a well-studied ferroelectric material, such as $BaTiO_3$, has not demonstrated negative capacitance experimentally before now. Further to this model for testing negative capacitance, the ultimate goal (as previously discussed in section 4.1) is its potential for reducing the subthreshold swing by incorporation into the gate stack of a MOSFET. This opens up further indirect testing methods for proving effective negative capacitance as drain current - gate voltage measurements with SS < 60 mV/decade are consistent with its existence.

The materials of choice for the simulated results, and also for the fabrication of the bilayer, have been $SrTiO_3$ for the positive capacitor C_1 and $BaTiO_3$ for the negative capacitor C_2. $BaTiO_3$ is chosen for its appropriate Curie temperature as it is ferroelectric at room temperature. Therefore, negative capacitance associated with the ferroelectric phase may be stabilised at room temperature. This is highlighted in ref. 8, and whose studies using $Pb(Zr_{0.2}Ti_{0.8})O_3$ showed stabilised C_T at elevated temperatures due to the Curie temperature of this ferroelectric material. The use of the stabilising positive capacitor is a somewhat arbitrary choice at first consideration. Its inclusion is to balance the energy density functions as shown in figure 4.6, where thickness and permittivity influence the energy density. A thinner layer for this positive capacitor may counteract a low permittivity, and vice versa, as a thin layer and/or high permittivity acts to flatten the energy function and increase capacitance. These design choices are important when considering the constraint shown in equation 4.4. However, these parameters for capacitance are not the only influences on the design. The inherent crystallography and composition can affect the stabilisation of the system. LD theory developed here is based upon single crystal, c-axis oriented materials. The use of $SrTiO_3$ as the positive capacitance then becomes pragmatic due to its perovskite nature.

Growth of $BaTiO_3$ upon this template allows superior perovskite/perovskite interfaces, offering epitaxial growth under certain deposition conditions. The technique proves to allow capacitor characteristics as close to LD theory as necessary, such that capacitance enhancement is shown at room temperature in the following experimental section. Further to the positive capacitance choice, the bottom electrode acts as the initial growth template for this capacitor. $SrRuO_3$, a conducting oxide, is chosen in this instance due to the lattice matching between the ensuing $SrTiO_3$ layer, as well as its perovskite nature. In addition, the underlying substrate acts as the main template, and any influence originating from this layer may ultimately alter the stabilisation of the system. $SrTiO_3$, as a single crystal substrate is chosen, as it is for C_1, in order to approach the ideal characteristics simulated in the above figures. Ultimately, in a Si driven nanoelectronics industry, $SrTiO_3$ substrates will have to be substituted for Si. Further work is suggested in chapter 7 regarding the use of Si substrates for displaying effective negative capacitance.

The lattice constants of the materials should also be considered in the design of the bilayer as misfit strain favours particular ferroelectric phases [11]. In order to approach the c phase, where the in-plane polarizations $P_1 = P_2 = 0$ and out of plane polarization $P_3 \neq 0$, a negative misfit strain is required. In this phase, the dipole polarization associated with the ferroelectric phase will be aligned to the applied electric field in the parallel plate MIM capacitor. In-plane lattice constants for the respective materials are, for $SrTiO_3$ a = 3.905 Å [14], $SrRuO_3$ a = 3.93 Å [15] and $BaTiO_3$ a = 3.99 Å [16]. Therefore, as the in-plane lattice constant of the $BaTiO_3$ layer is larger than the underlying $SrRuO_3$ electrode, and $SrTiO_3$ film and substrate, a negative misfit strain will be imposed on this ferroelectric layer, in accordance with equation 3.1. Thus, a further elongation along the c axis will result, and the ferroelectric

c phase will be supported [11]. In this regard, the negative capacitance effect associated with the ferroelectric phase in the $BaTiO_3$ film will be favoured when considering the lattice constants of the chosen materials.

As touched upon, the deposition of the films is also an important factor. Results here present findings using PLD at high temperature such that films are epitaxially grown in a high crystallised phase. Work has been ongoing using sputter deposition as the growth method of choice. However, many issues, such as pin holes and delamination have occurred. This highlights only some of the problems in fabricating high quality perovskite materials for novel applications such as negative capacitance.

4.3 Experiment

Metal-Insulator-Metal (MIM) structures were fabricated on $SrTiO_3$(100) substrates using PLD with a KrF excimer laser from Lambda Physik. Prior to the film deposition, the $SrTiO_3$ substrates were cleaned in acetone, isopropanol and water for 3 minutes each. The bottom electrode of $SrRuO_3$ with thickness 30 nm is lattice matched to the substrate and grown at 750 °C. The insulating layer, grown at 850 °C, comprised 25 nm of $SrTiO_3$, which is paraelectric (calculated due to the lattice constant ratio c/a = 1 from reciprocal lattice mapping of electron diffraction patterns in figure 4.13), and a ferroelectric layer of $BaTiO_3$, having thickness 20 nm, 30 nm or 50 nm. Control samples with either no $BaTiO_3$ or $SrTiO_3$ were also grown. The single $SrTiO_3$ capacitor at 25 nm was used to benchmark capacitance in the bilayer structures, while the single 30 nm $BaTiO_3$ capacitor was tested for ferroelectricity. All layers were deposited at 75 mTorr pressure. Samples were kept under vacuum between the deposition of $SrTiO_3$ and $BaTiO_3$. Finally, a 100 nm thick Pt top electrode was deposited by electron beam evaporation and patterned in a lift-off process. Figure 4.9 shows cross-sections of the samples used for testing the negative capacitance hypothesis.

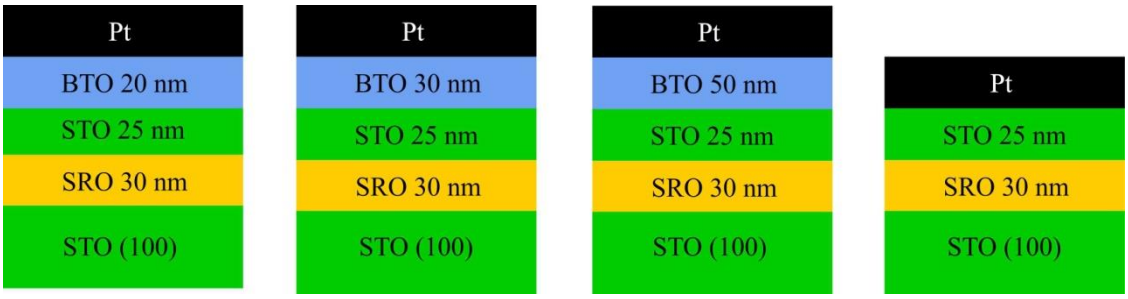

Figure 4.9: Schematic of the bilayers and test structure under investigation for negative capacitance.

During the deposition process, optical images were taken of the substrate and bottom $SrRuO_3$ electrode, as well as resistivity and AFM measurements. After deposition of the $SrTiO_3$ and $BaTiO_3$ films, XRD and TEM images were taken to confirm epitaxial growth of the film, matched to the single crystal substrate. XRD spectra were acquired using Panalytical x'pert Pro with Cu-Kα X-ray radiation having a characteristic wavelength of 1.5418 Å. TEM was conducted on a JEOL-2100F microscope operating a 200 kV Schottky field emitter. Electron diffractions were processed using Fourier transforms in the Gatan DigitalMicrograph software. AFM images were taken to investigate surface smoothness and conducted on a Park Systems XE-150 in non-contact mode.

In order to confirm negative capacitance in the ferroelectric layer, CV results were taken from 10 kHz up to 1 MHz on an Agilent 4294A meter. IV results were taken to investigate leakage current in the films on an Agilent 4155C tester.

4.4 Material Results

XRD spectra were taken on each of the bilayers and single layer $SrTiO_3$ test capacitor in order to verify material quality and microstructure. Figure 4.10 shows the results of both the $SrTiO_3$ capacitor C_1 (25 nm) and bilayer C_T of $SrTiO_3$ / $BaTiO_3$ (25 nm / 50 nm). From the figure, it is evident that the structures are epitaxially grown in (100) orientation, as controlled by the single crystal $SrTiO_3$ (100) substrate, with peak positions indicating the perovskite phase. Figure 4.11 includes spectra of all three bilayers. The results are confirmed in the remaining bilayers, such that epitaxial growth and single phase insulating material has been grown. The results are important when considering the experimental verification of the simulation results given in section 4.2.

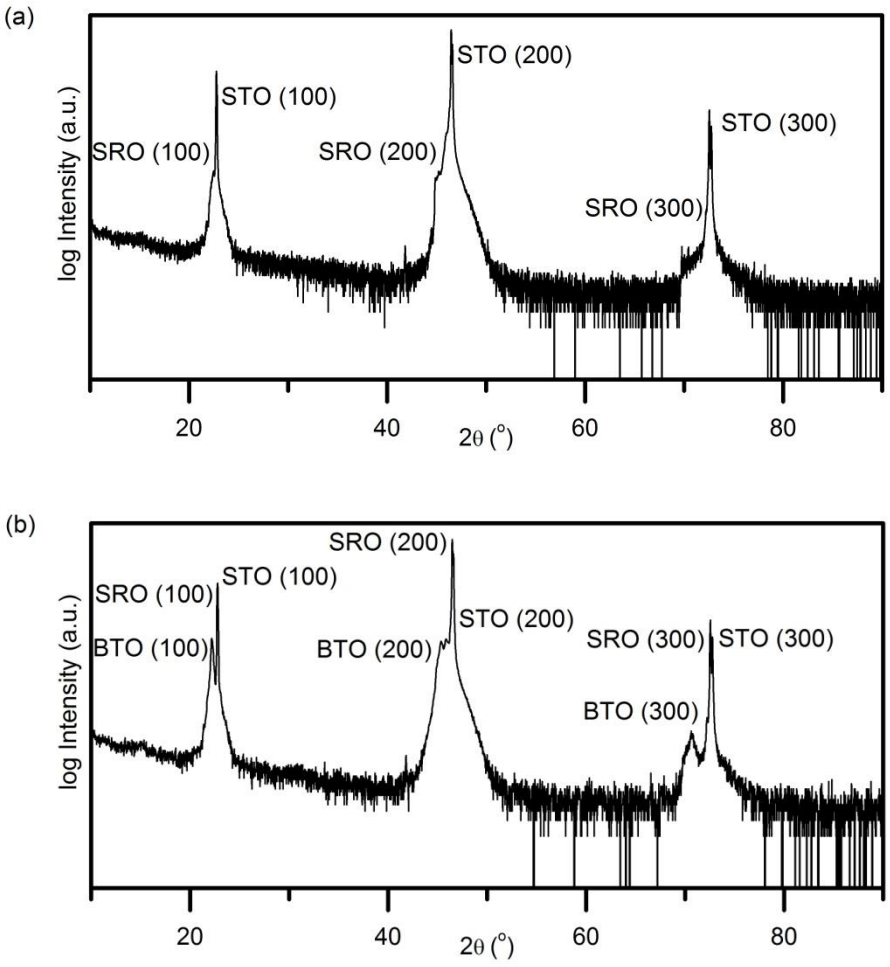

Figure 4.10: XRD spectra of (a) the single $SrTiO_3$ 25 nm and (b) bilayer $SrTiO_3$ / $BaTiO_3$ 25 nm / 50 nm capacitors.

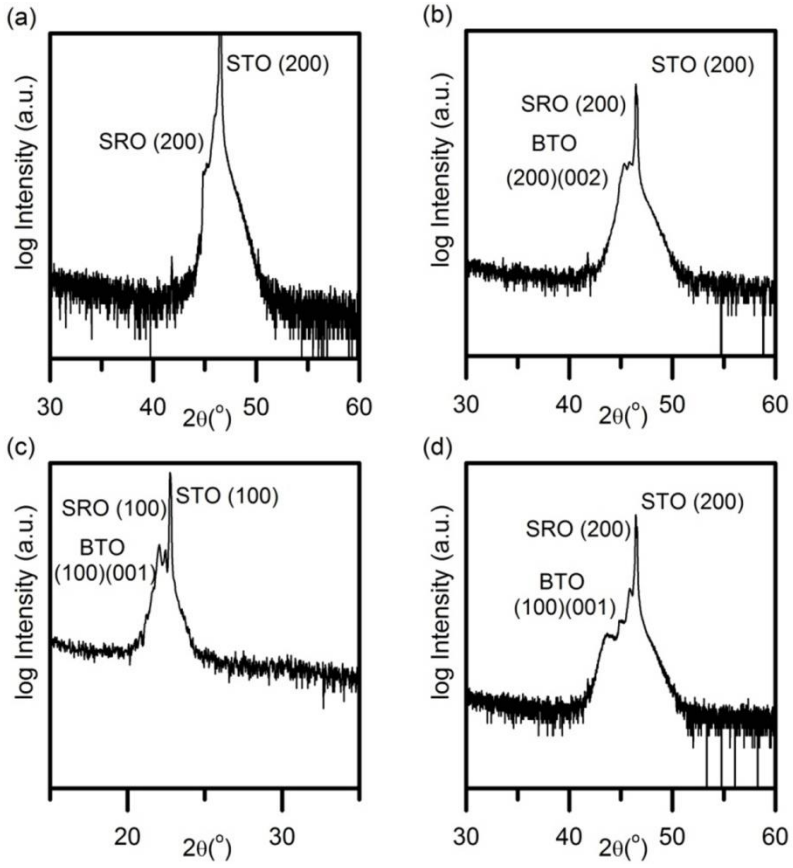

Figure 4.11: XRD spectra of (a) the single $SrTiO_3$ capacitor (25 nm), (b) bilayer $SrTiO_3$ / $BaTiO_3$ (25 nm / 50 nm), (c) bilayer $SrTiO_3$ / $BaTiO_3$ (25 nm / 30 nm) and (d) bilayer $SrTiO_3$ / $BaTiO_3$ (25 nm / 20 nm) capacitors.

The well matched lattice constants allows coherent growth of a full perovskite structure with atomically smooth interfaces.

The previous XRD results showed the epitaxial nature of the films under investigation. Epitaxial films should result in smooth interfaces and top surfaces due to the lack of grain growth and any resulting grain boundaries. AFM imaging is now used to investigate the surface roughness and microstructure. Figure 4.12 shows the results of (10 x 10) μm surface topography scans for the 25 nm $SrTiO_3$ and 25 nm / 50 nm $SrTiO_3$ / $BaTiO_3$ samples. In figure 4.12 (a), the $SrTiO_3$ sample, the surface shows

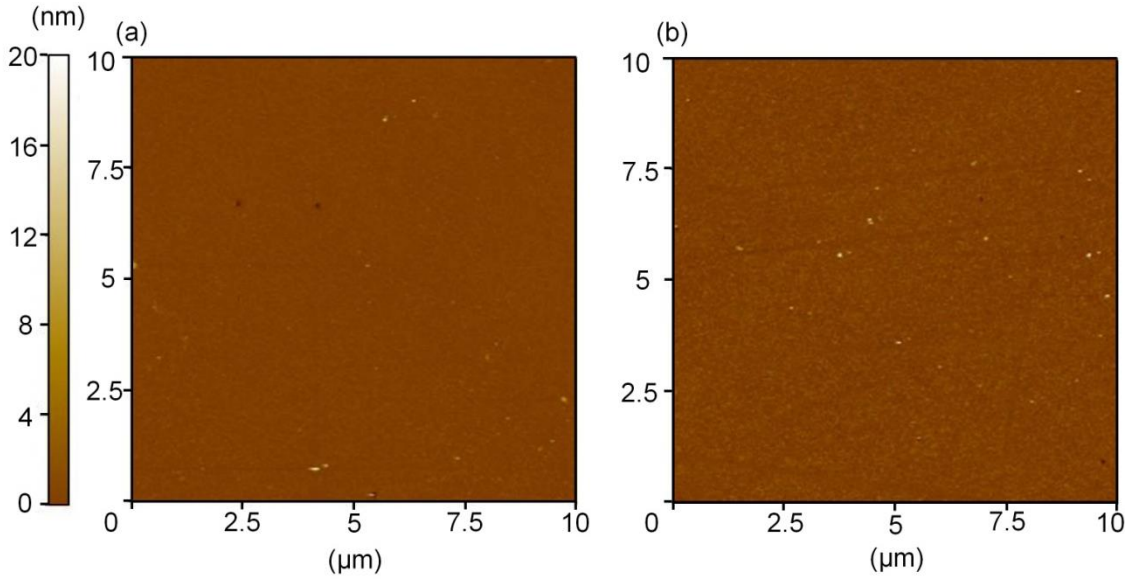

Figure 4.12: AFM topography images of the $SrTiO_3$ (a) and $SrTiO_3$ / $BaTiO_3$ 25 nm / 50 nm capacitors. Probe tip radius < 8 nm.

to be smooth and uniform. The calculated root mean square surface roughness was 0.5 nm. Figure 4.12 (b) shows the matching surface scan for the $SrTiO_3$ / $BaTiO_3$ bilayer. The results are directly comparable to that in the $SrTiO_3$ image shown in figure 4.12 (a) in that the surface is smooth and uniform. Calculated surface roughness for the bilayer was 0.9 nm. Any evidence for grain boundaries would manifest as trenches or valleys surrounding grain surfaces in AFM topographies, and resulting scans would show root mean square surface roughness > 1 nm. Therefore, the AFM results are consistent with the epitaxial nature of the films. The surface smoothness also results from the epitaxial growth of the films.

In order to further confirm the epitaxial growth of the films, cross-sections of each interface of the bilayer capacitor having a $BaTiO_3$ thickness of 20 nm and $SrTiO_3$ thickness of 25 nm are shown in figure 4.13. Each layer is perovskite and grown epitaxially, lattice matched to the $SrTiO_3$ (100) substrate. Electron diffraction (EDX) confirms a single crystal orientation throughout the MIM stack. Reciprocal space mapping of the EDX pattern in figure 4.13 (a) indicates a lattice constant ratio of the

perpendicular and in-plane parameters, c/a = 1.07. An elongation of the c lattice parameter favours the ferroelectric phase in the $BaTiO_3$ film, and is necessary for observing negative capacitance in each structure. The result indicates that the c phase is induced in the ferroelectric $BaTiO_3$ layer, which will be enhanced by negative misfit strain due to the lattice constants of the underlying films and substrate. The remaining $SrTiO_3$ and $SrRuO_3$ films were cubic, and the perpendicular and in-plane lattice constants are calculated from the reciprocal space mapping of the electron diffraction patterns in figure 4.13 (b) and (c) as c/a = 1 ± 0.0001.

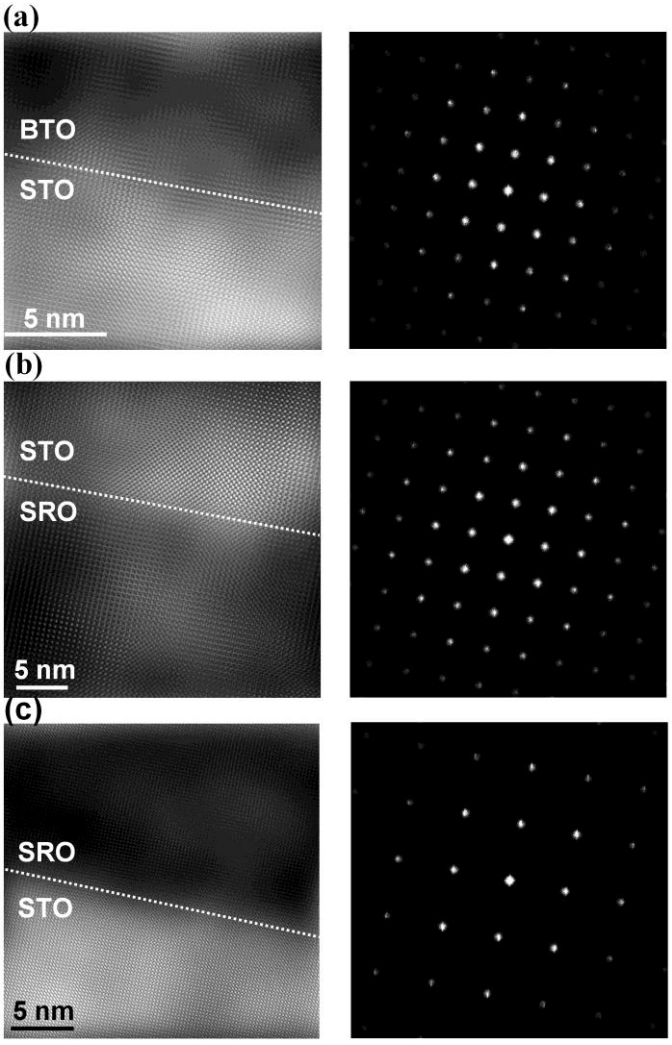

Figure 4.13: Bright field cross section of one the heterostructures under investigation at each interface. $BaTiO_3/SrTiO_3$ film (a), $SrTiO_3/SrRuO_3$ (b) and $SrRuO_3/SrTiO_3$ (100) substrate (c). Dashed line shows interface between each thin film. Corresponding electron diffraction pattern is also shown indicating the single crystal nature.

4.5 Electrical Results

In order to test the negative capacitance hypothesis in ferroelectric oxides, capacitance enhancement has to be measured in a bilayer structure. The technique serves as the indirect measurement of stabilised negative capacitance as shown in section 4.3. Shown in figure 4.14 is capacitance density measured across a voltage range in a single $SrTiO_3$ test structure, as well as three bilayer structures. The bilayer structures include the 25 nm $SrTiO_3$ layer as its stabilising capacitance; therefore, if capacitance in the bilayers is greater than that in the single $SrTiO_3$ structure, capacitance enhancement is apparent. The results in the figure show that, in all three bilayers, capacitance is measured higher than in the $SrTiO_3$ capacitor. This experimentally supports the simulated results which stipulated negative capacitance as

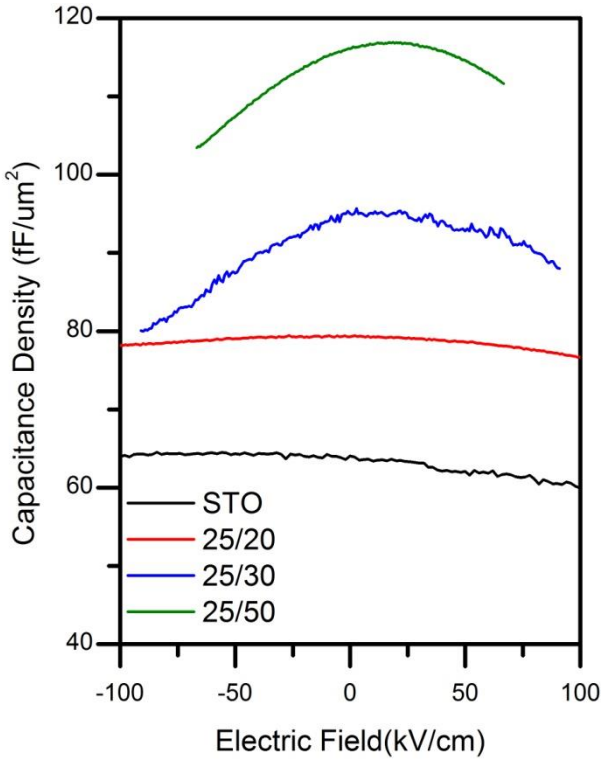

Figure 4.14: Capacitance density measured in a single layer $SrTiO_3$ capacitor at 25 nm thickness and three bilayer structures as a function of applied bias. The bilayers are combinations of $SrTiO_3$ / $BaTiO_3$ at 25 nm / 20 nm, 25 nm / 30 nm, 25 nm / 50 nm thicknesses.

the catalyst for enhancement in the total capacitance, provided the bilayer system was correctly stabilised.

Also shown in figure 4.14 is the tunable nature of the film as capacitance decreases with applied electric field. The result indicates the film is grown in the crystallised perovskite phase, and confirms the XRD spectra and TEM results shown above. The tunable capacitance trends are also shown to increase in figure 4.14 as the thickness of $BaTiO_3$ increases. This is consistent with the insulator becoming dominated with $BaTiO_3$ due to its higher Curie temperature, T_c. Peak capacitance of the layers are also situated at approximately 0 V. This leads to a further observation that the films have been stabilised. Ferroelectric properties in the bilayers should be removed due to the inclusion of the stabilising layer in order to measure capacitance enhancement accurately. Previously shown in figure 4.8 (b) with incorrect stabilisation, the bilayer capacitance peaks are situated at finite voltage and the measurement does not produce capacitance enhancement. However, in figure 4.8 (d), both the bilayer and single $SrTiO_3$ measurements are tunable with no instability in capacitance, originating from remnant polarization switching. Therefore the capacitance measured in figure 4.14 is correctly stabilised, allowing indirect measurement of negative capacitance.

The influence of $BaTiO_3$ thickness is such that it alters the energy function of the overall bilayer in accordance with equation 4.8. Increasing this thickness should increase the total capacitance of the bilayer, up until the point at which negative energy density is induced as the $BaTiO_3$ layer dominates the bilayer. At this threshold, the double energy minima are created and polarization switching occurs, i.e. negative capacitance is no longer accessed and hysteresis ensues. The impact of increasing the thickness of the $BaTiO_3$ layer is shown in figure 4.15. It shows a plot of amplification, defined as C_T / C_1, as a function of $BaTiO_3$ thickness in the bilayer. Also shown is what

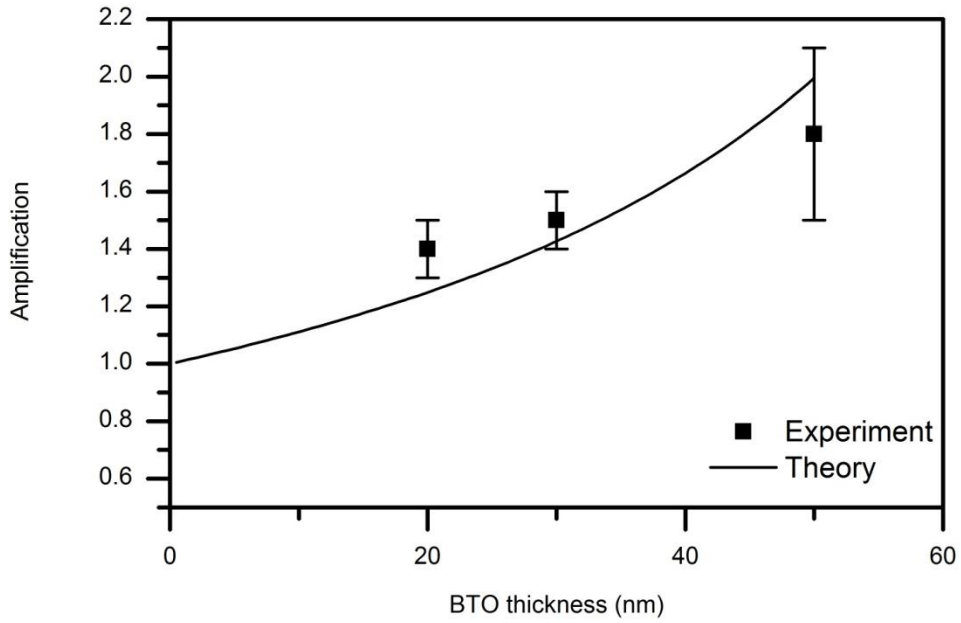

Figure 4.15: Amplification in each bilayer over the constituent $SrTiO_3$ layer. Amplification is defined as C_T/C_1. Theory is simulated from equation 4.9 at room temperature, 25 °C.

is expected theoretically using equation 4.9. The results in the figure do not rule out the possibility of negative capacitance originating in $BaTiO_3$; increasing the thickness of the $BaTiO_3$ film does lead to an increase in the total measured capacitance. However, further data would be needed to accurately compare the experimental measurements with the theoretical curve. Slight film thickness variations, or strain relaxation as film thickness increases could cause variations from theory. Nevertheless, from figure 4.15, increasing the $BaTiO_3$ thickness may be influencing the total energy function of the bilayer. The $BaTiO_3$ thickness couples with polarization (equation 4.8), increasing the negative linear contribution from α around zero bias, and hence negative energy density. The contribution from the fixed $SrTiO_3$ thickness will be unchanged. The overall impact this has is a flattening of the total energy function U_T, and capacitance increases in accordance with equation 4.5. Therefore, figure 4.15 may show evidence of this effect as increasing the $BaTiO_3$ thickness leads to greater capacitance enhancement in the bilayer.

Capacitance enhancement, as previously described, is dependent on the capacitance achieved in the single $SrTiO_3$ capacitor. For this reason, the quality of this capacitor has to be assessed and compared against the bilayer capacitors. Shown in figure 4.16 is the leakage current density as a function of applied bias for the $SrTiO_3$ single layer and $SrTiO_3$ / $BaTiO_3$ bilayer capacitors. The results show that the $SrTiO_3$ capacitor has higher leakage density when compared to the bilayer capacitor. Higher leakage current can compromise the achieved capacitance and lead to overall reductions in the measured capacitance. Therefore, the perceived capacitance enhancement in the bilayer may be leakage mediated, such that the achieved capacitance from the single $SrTiO_3$ capacitor is lower than that what is expected. Comparing the capacitances in the single layer and bilayer capacitors would then not lead to accurate conclusions about negative capacitance being the cause for capacitance enhancement. Also shown in figure 4.16 is the loss tangent, calculated from the imaginary part of the permittivity. The results show that under the full bias range, the charging current is always at least a factor of 2 greater than the leakage current in both samples. The bilayer loss tangent is

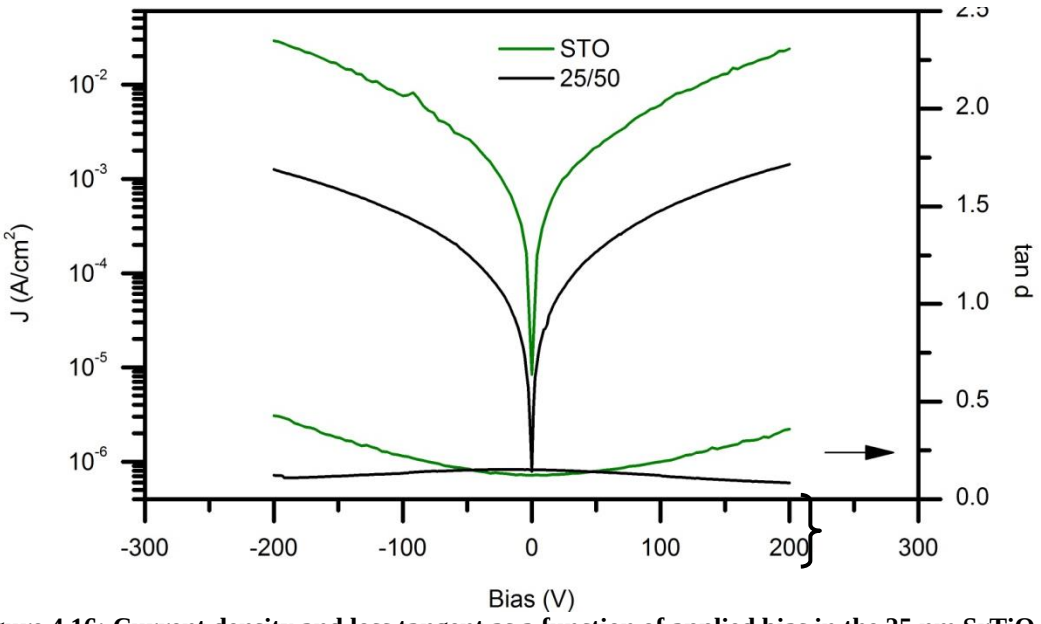

Figure 4.16: Current density and loss tangent as a function of applied bias in the 25 nm $SrTiO_3$ capacitor and the $SrTiO_3$ / $BaTiO_3$ 25 nm / 50 nm bilayer capacitor.

approximately equal to the single $SrTiO_3$ layer between ± 100 kV/cm. The result suggests that the capacitance of the $SrTiO_3$ layer, when measured around zero bias, may be directly compared to the bilayer capacitance due to equal loss tangents around this bias range. Therefore, a direct assessment of measured capacitance in the bilayer and single layer structures is a more realistic comparison when considering the loss tangent results. In addition, the capacitance enhancement is shown to be greatest at zero bias, and is specifically where the loss tangents in the structures are equal.

As well as the leakage current and loss in the single $SrTiO_3$ capacitor, dead layers may be affecting the measured zero bias permittivity. Dead layers cause suppression of the permittivity in such a way that a thinner film will show greater reduction in permittivity than in a thicker film [17-19]. This leads to the assumption that the single $SrTiO_3$ layer should show greater suppression of permittivity than the bilayers, which may lead to an incorrect conclusion about negative capacitance leading to capacitance enhancement. However, the TEM images shown in figure 4.13 do not indicate any physical dead layer at either interface between the insulators. Intrinsic influences originating from incorrect electrode screening and depolarizing fields are likely origins of the permittivity suppression [20, 21], which is further studied in chapter 6 using an effective oxide thickness model.

In order to investigate dead layers impacting the capacitance enhancement, figure 4.17 shows the capacitance density measured in the $SrTiO_3$ test structure and the three bilayers. The relative permittivity for bulk $SrTiO_3$ is widely reported to be around 300 [22], while it is lower for nm scale thin films of $SrTiO_3$ [23] (relative permittivity for 25 nm $SrTiO_3$ capacitor C_1 is 200; equals value reported in ref. 8). Using this bulk value for $SrTiO_3$ permittivity, the capacitance of the 25 nm $SrTiO_3$ layer is included as

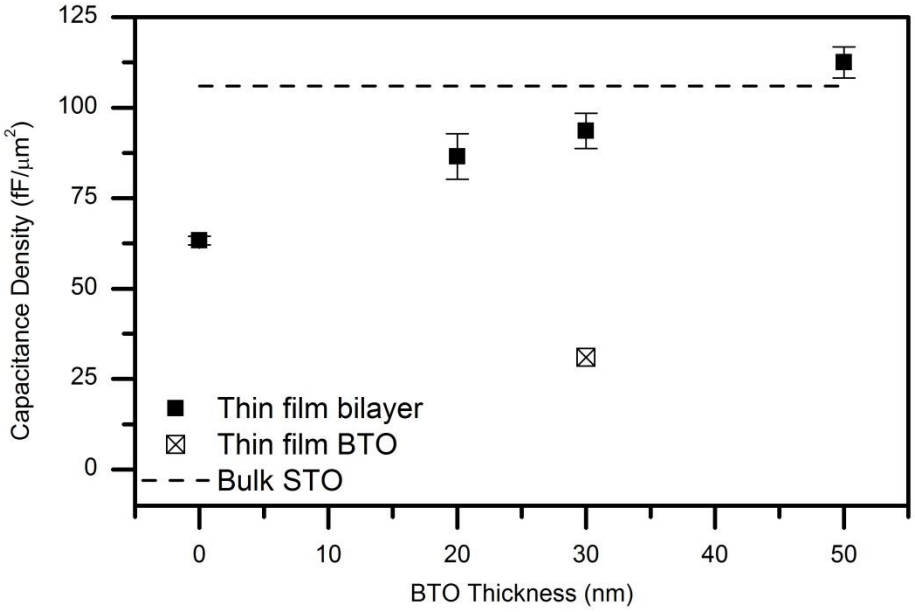

Figure 4.17: Capacitance density in the single 25 nm $SrTiO_3$ capacitor and the three measured bilayers. At 30 nm an additional data point is shown representing the single $BaTiO_3$ capacitor (C_2) without a $SrTiO_3$ layer. Theoretical capacitance density in single $SrTiO_3$ capacitor is also shown.

a dashed line in figure 4.17. Even for this most conservative estimate of $SrTiO_3$ permittivity, the total capacitance for the bilayer stack having a $BaTiO_3$ layer 50 nm thick is larger than with $SrTiO_3$ alone, which indicates an effective negative capacitance for the $BaTiO_3$ layer. This comparison rules out the possibility of the capacitance enhancement resulting from a dead layer effect in the 25 nm $SrTiO_3$ capacitor, which may otherwise lead to incorrect assumptions about the capacitance enhancement [21]. It also further discounts any leakage mediated reductions in capacitance measured on the single layer $SrTiO_3$ capacitor, and points to the increased total capacitance arising from the stabilisation of $BaTiO_3$ negative capacitance.

In figure 4.17 a data point representing the single $BaTiO_3$ capacitor C_2 of thickness 30 nm, without the 25 nm $SrTiO_3$ layer, is also shown for further comparison. At this thickness the $BaTiO_3$ capacitor C_2 displays lower capacitance than in the bilayer. Incorporation of the 25 nm $SrTiO_3$ thickness has led to an increase in total capacitance due to the stabilized negative capacitance layer in the bilayer.

The Maxwell-Wagner effect is known to cause permittivity enhancement in superlattices [24], and evidence of this in $BaTiO_3/SrTiO_3$ heterostructures has been reported previously [25]. But the Maxwell-Wagner effect is known to correlate with the number of heterojunction interfaces, and reduces at low frequency. This explanation is therefore not relevant for the capacitance enhancement reported here, which only has a single interface. Moreover, electrical measurements carried out up to 1 MHz shown in figure 4.18 also demonstrate capacitance enhancement in the bilayer across the whole frequency range. This further rules out Maxwell-Wagner effects.

The $BaTiO_3$ single layer structure is now investigated for ferroelectricity. As the bilayer structure depends on the $BaTiO_3$ layer being ferroelectric in order to show negative capacitance, piezo force microscopy (PFM) was performed on the single 30 nm $BaTiO_3$ capacitor. PFM allows investigation of the ferroelectric nature of the film due to the expansion and contraction of the material under polarization switching. The piezoresponse measured as an amplitude of cantilever deflection allows assessment of the coercive field, which indicates its ferroelectric properties.

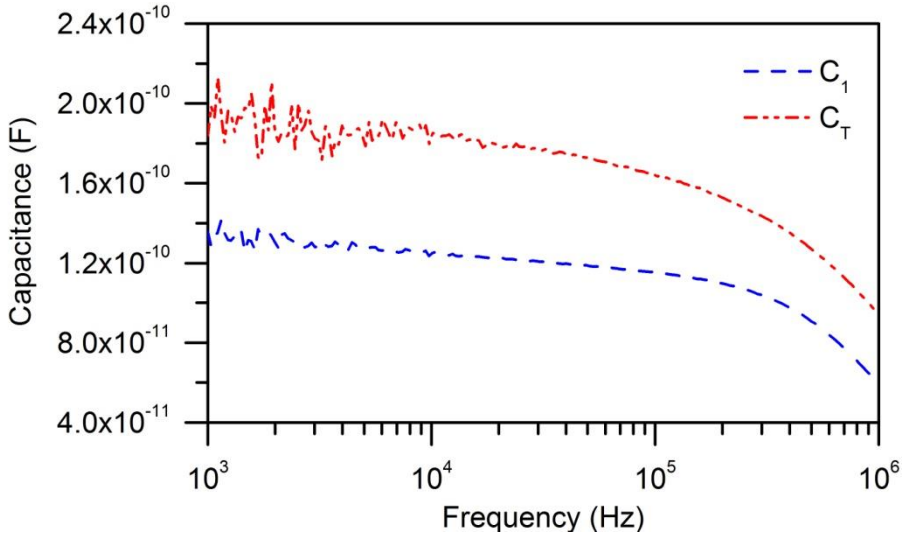

Figure 4.18: Capacitance density measured at a function of frequency. The single 25 nm $SrTiO_3$ capacitor and 25 nm / 20 nm $SrTiO_3$ / $BaTiO_3$ bilayer are shown.

Shown in figure 4.19 is the resulting piezoresponse of the $BaTiO_3$ film under application of an applied electric field. The arrows indicate the direction of the applied field. The results present experimental evidence for ferroelectricity in the $BaTiO_3$ film. Applying a negative electric field and sweeping towards positive field, the piezoresponse initially stays flat (marked region (a)) as the material retains its polarization. Approaching zero field (b), the piezoresponse begins to decrease as the spontaneous polarization transitions into its remnant state. This causes a contraction of the domain, leading to the piezoresponse shown in figure 4.19. The piezoresponse minima are indicative of the coercive field, the point at which the greatest domain contraction occurs when the polarization reverses direction (c, d). The results are archetypal of single crystal and uniform oriented $BaTiO_3$ whose polarization reverses in a 180 ° direction [26]. The PFM measurement further confirms the XRD and TEM results, which showed a single oriented film imposed by the $SrTiO_3$ substrate. It also confirms that the $BaTiO_3$ film is c-axis oriented, which has previously been discussed as desirable for the purpose of reproducing the simulations shown in section 4.3.

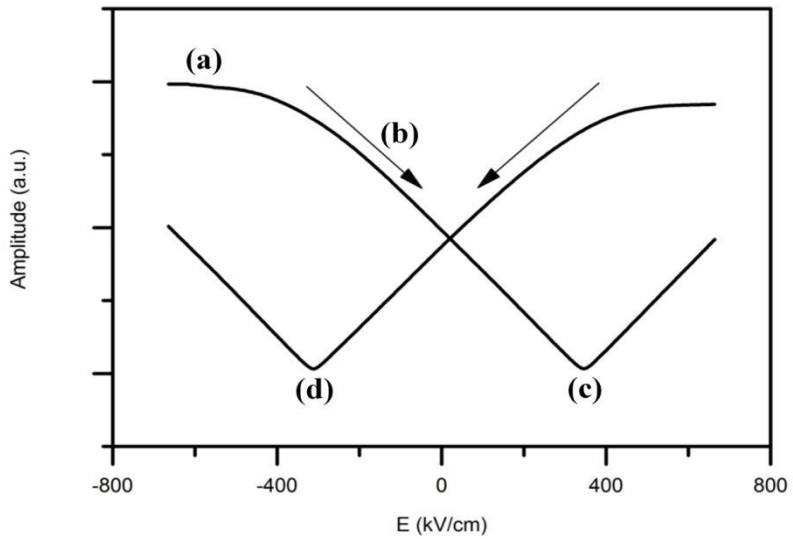

Figure 4.19: Amplitude of piezoresponse as a function of applied electric field. Arrows indicate the direction of applied electric field.

4.6 Summary

In this chapter, the property of negative capacitance was investigated, in particular with $BaTiO_3$, a robust and versatile ferroelectric. Based upon LD theory, predictive negative slopes of polarization in $BaTiO_3$ have been studied in a stabilised series capacitance system. Simulations showed that negative capacitance can be stabilised provided the energy density function in the bilayer is correctly balanced, and achieves a positive turning point at zero polarization. The series configuration allows indirect measurement of negative capacitance as the total capacitance will be measured greater than the constituent positive capacitance if a negative capacitance is in the series. The results show that with a bilayer of $SrTiO_3$ and $BaTiO_3$, where $SrTiO_3$ is positive and $BaTiO_3$ negative, the capacitance of the system is greater than the $SrTiO_3$ capacitance, owed to negative capacitance in the $BaTiO_3$ layer. When the thickness of the $BaTiO_3$ layer is increased, the total capacitance increases. The results were predicted from simulations using LD theory.

The bilayers were measured over a range of frequencies to confirm that the origin of capacitance enhancement is from a negative contribution in the $BaTiO_3$ film. Films were shown to be free from any physical dead layers at the insulating interfaces, such that the reduced permittivity (bulk value 300 to 200 in capacitor C_1) most likely originates from intrinsic effects in thin films. Dead layer analysis further showed that the bilayer with a 50 nm thick $BaTiO_3$ layer still showed capacitance enhancement over that of a bulk single $SrTiO_3$ layer.

The present work demonstrates the feasibility of negative capacitance at room temperature using a lead-free ferroelectric, which can be integrated into CMOS or included as a performance booster within innovative devices such as tunnel field effect transistors [27] in order to realise a future low power technology.

4.7 References

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Chapter 5

Low Temperature Growth of Perovskite Insulators for Tunable High-κ Applications

5.1 Introduction

The properties displayed by perovskite insulators are advantageous as far as the nanoelectronics industry is concerned. They offer desirable electrical properties, such as high-κ for DRAM and tunable capacitance for tunable filter applications, among many others. In order to utilise the aforementioned properties, a key feature of the thin film perovskite is its crystallinity. A crystalline thin film will offer the highest permittivity, and in turn tunability, while an amorphous structure displays low permittivity and tunability, but with the lowest leakage current. Therefore, a trade-off between the properties of the perovskite is required for a specific application. For instance, a low power requirement of in situ hearing aids makes the amorphous, low leakage property desirable, but this will limit the tunable filter aspect of the design.

In order to induce crystal growth in a material a specific crystallisation temperature must be reached. The crystallisation temperature may be given during film deposition, or post-deposition in an annealing process. For FEOL fabrication the temperature may reach > 1000 °C; thus, temperature is not a restricted parameter. However, ensuing metallisation and circuit elements in the BEOL fabrication are ideally not exposed to temperatures exceeding 500 °C. The temperature is restricted in order to limit diffusion of dopants and inhibit formation of undesirable silicide phases. Consequently, any tunable or high-κ capacitor in the BEOL should be crystallised at temperatures of approximately 500 °C or below.

Tunable capacitance is achieved due to a permittivity, or polarization, dependence on the applied electric field. Tunability is shown in equation 5.1

$$n = \frac{\varepsilon(0)}{\varepsilon(E_o)} \tag{5.1}$$

where n describes the tunability achieved in the material at a certain applied electric field E_o and ε is the dielectric permittivity. For a linear dielectric, such as SiO_2, n = 1 and the permittivity is constant across all of the applied electric field. The comparisons between this type of linear dielectric and a tunable perovskite material are highlighted in figure 5.1. In figure 5.1 (a), the polarization begins to saturate when the electric field increases. The capacitance decreases due to the saturating polarization (figure 5.1 (b)), and n > 1 in this instance due to a decrease in permittivity when the electric field increases. In figure 5.1 (c), for the linear dielectric, the polarization does not change as the electric field increases. The result is a constant capacitance, and the permittivity will not change across the applied electric field. Hence, in figure 5.1 (d) n = 1. A review of ferroelectric materials for microwave tunable applications is given in [1].

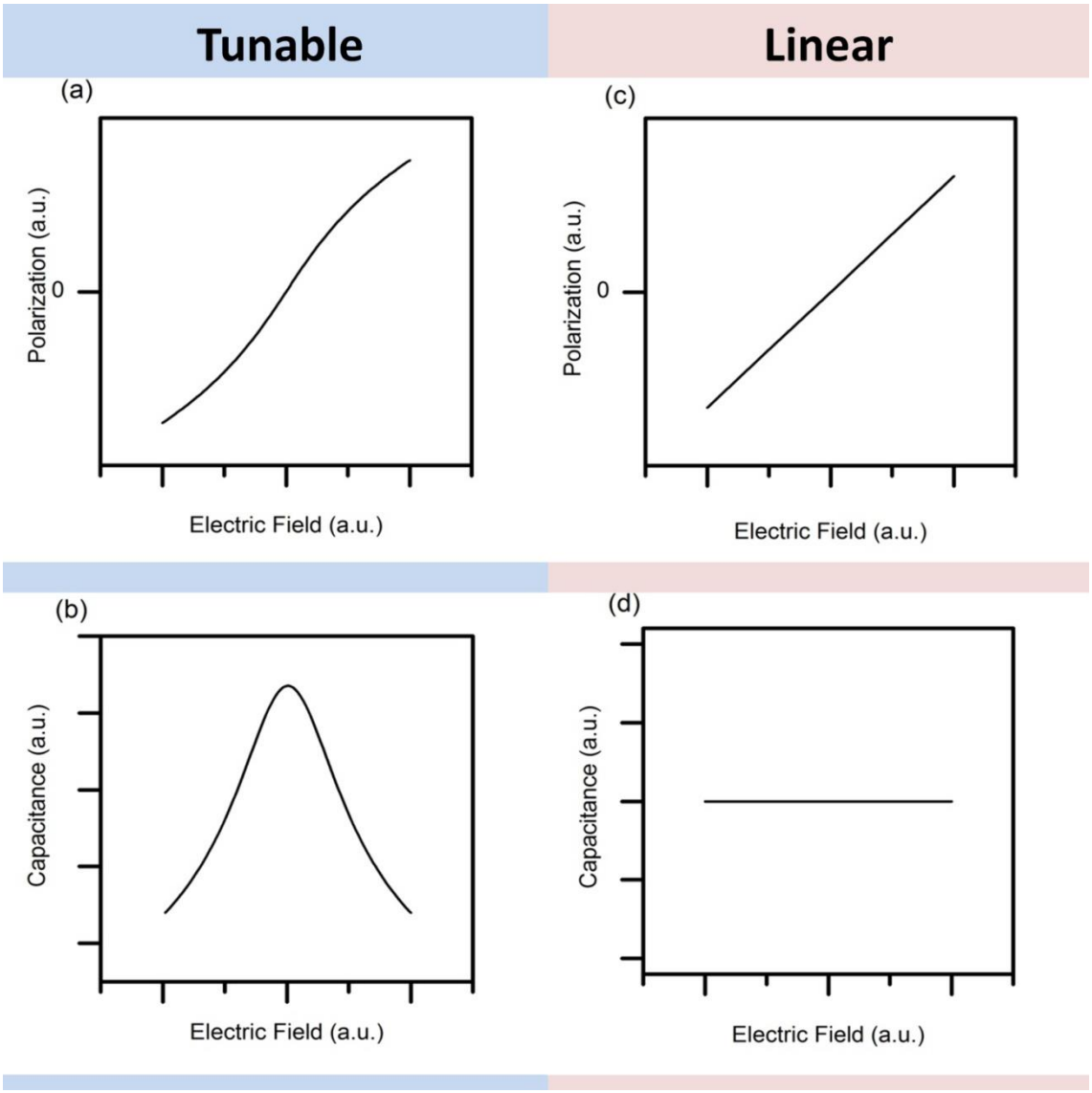


Figure 5.1: Polarization vs electric field curve for a tunable capacitor (a) and its corresponding tunable capacitance taken as dQ/dV (b). Linear polarization vs. bias for a typical dielectric (c) and corresponding bias independent capacitance (d).

The characteristics described in equation 5.1 and figure 5.1 are important benchmarks for fabricating high quality perovskite films. A largely tunable film will produce high zero-bias dielectric permittivity (as highlighted in chapter 6), whereas the linear characteristics in figure 5.1 (c), (d) are more likely to produce the lowest leakage current due to the amorphous nature of the film.

A large number of materials investigated for tunability, including $Ba_{0.5}Sr_{0.5}TiO_3$ [2], $BaTiO_3$ [3], $SrTiO_3$ [4] and also high-*k* properties, ZrO_2 [5], or HfO_2 [6] are based on a range of deposition techniques, substrates and thermal treatments of

the insulators. Studies on $SrTiO_3$ using PLD at 500 °C show evidence of crystallisation, with high relative permittivity at zero-bias of 220 for 0.5 μm film thickness [7] and 190 for 0.55 μm thickness [8]. However, the relatively large thicknesses studied are not suitable for nm scale device integration, and in addition can hide such things as dead layers. Recently, a seed layer approach was conducted using ALD [9]: a thin $SrTiO_3$ seed layer was annealed prior to the remaining 370 °C deposition of $SrTiO_3$ to investigate microstructure. The high temperature anneal needed to crystallize the seed layer may be unsuitable for BEOL integration temperature constraints (≤ 500 °C). Further studies using ALD and post-annealing $SrTiO_3$ have also shown that the crystalline phase is apparent only after reaching a minimum temperature of 650 °C [10].

In chapter 5 the growth of perovskite materials for high-κ tunable characteristics is investigated under the temperature constraint of 500 °C. ALD is used to deposit $SrTiO_3$ films, which are amorphous as-grown. Post-deposition annealing (PDA) is required to crystallise the film, and results show the quality of $SrTiO_3$ having undergone RTP at 500 °C. Influences on the RTP crystallisation temperature from carbon impurities and stoichiometry are explored. PLD is also used to grow $SrTiO_3$ films at 500 °C, in contrast to the ALD films that require RTP in order to crystallise the films. In addition, $Ba_{0.8}Sr_{0.2}TiO_3$ is explored as a possible low temperature solution for high-κ tunable properties, and deposition using PLD at 500 °C is conducted. Results here offer a direct comparison between $SrTiO_3$ and $Ba_{0.8}Sr_{0.2}TiO_3$ for the first time. Alloying the $SrTiO_3$ film with high levels of Ba should increase permittivity and tunability. The results suggest an amorphous phase as the inclusion of Ba has shifted the crystallisation temperature of the $Ba_{0.8}Sr_{0.2}TiO_3$ film. It has been shown recently the impact deposition temperature plays on structural properties, and hence electrical

properties, of $SrTiO_3$ films deposited by sputtering [11]. Further studies in this chapter using $BaTiO_3$ are shown by sputter deposition, which are then compared to the results of the films grown using PLD and ALD. The results presented in this chapter offer comparisons between three established thin film deposition techniques.

5.2 Experiment

$SrTiO_3$ and $Ba_xSr_{x-1}TiO_3$ films were deposited using PLD ranging in thickness from 30 nm – 90 nm on Si(100)/SiO_2/Ti/Pt substrates. The PLD grown films were deposited using a KrF excimer laser from Lambda Physik. The targets were sintered samples of $SrTiO_3$ with 100% purity. Before deposition the substrate was heated up to the deposition temperature of 500 °C. Samples deposited at 700 °C were used as benchmarks for crystallinity to compare against the low temperature deposited samples. The deposition was performed at a repetition rate of 5 Hz in an oxygen pressure of 100 mTorr. The energy density of the focused laser beam on the target was 4 J/cm^2. The number of pulses was determined by the known deposition rate and the desired film thickness of the sample. After deposition the vacuum chamber was flooded with Oxygen up to 500 Torr, and the sample was cooled down to room temperature at a cooling rate of 10 K/min.

$SrTiO_3$ films were deposited using ALD on matching substrates and bottom electrodes to the PLD grown films. The ALD process was performed at 250 °C in an Oxford Instrument FlexAL single wafer reactor using $Sr(iPr_3Cp)_2$ and $Ti(OiPr)_4$ precursors. Film thickness was confirmed by spectroscopic ellipsometry and results showed a growth per cycle rate of 1 Å. The films were subsequently annealed by rapid thermal processing (RTP) in N_2 for 120 s under 500 °C in order to induce crystallization, and compare against the PLD process. An increase in RTP temperature to 600 °C was used as a benchmark for the 500 °C annealed sample.

For the sputter deposition of $BaTiO_3$, substrates were heated from room temperature to 400 °C and film thicknesses were between 30 nm - 150 nm. Ar/O ratio in the sputter chamber ranged from pure Ar, to a ratio of 20/30 under 5 mTorr pressure.

Crystallisation of the $BaTiO_3$ films was done in a post-deposition anneal, either using a furnace or RTP with a temperature of 400 or 500 °C. Time of annealing was varied from 2 minutes to 1 hour.

X-ray photoelectron spectroscopy (XPS) was performed on an AXIS Nova with monochromated Al K_α source. The ALD sample after RTP and PLD samples grown at 500 °C were initially cleaned and etched for 30 s to obtain high resolution spectra for stoichiometry analysis. The transmission electron microscopy (TEM) studies were performed on a JEOL 2010 TEM in bright field mode. The TEM is fitted with a Gatan Multiscan CCD camera below the viewing chamber which makes low-intensity and high-resolution imaging possible. Film crystallinity was assessed in terms of X-ray diffraction (XRD) using Cu K_α radiation. Atomic force microscopy (AFM) in non-contact mode was performed on a Park Systems XE-150 across 1x1 μm^2 to extract grain size and surface roughness as root mean squared values.

In order to probe electrical characteristics of the $SrTiO_3$ films, top electrodes of Pt were deposited by e-beam evaporation and patterned using a lift-off process to create parallel-plate metal-insulator-metal (MIM) structures. Capacitance-voltage (CV) measurements were performed on an Agilent 4294A precision impedance analyser at 1 MHz, while current-voltage (IV) measurements were performed on an Agilent 4155B semiconductor parameter analyser, both at room temperature.

5.3 Low Temperature Growth of $SrTiO_3$

5.3.1 Material properties

The $SrTiO_3$ films deposited using ALD and PLD are investigated. Due to the temperature of growth of ALD, the $SrTiO_3$ film is amorphous as-grown. A PDA at 500 °C is performed in order to crystallise the $SrTiO_3$ film. Therefore, a direct comparison may be given between RTP $SrTiO_3$ at 500 °C after ALD, and $SrTiO_3$ grown at 500 °C using PLD. Assessing the crystallinity of the $SrTiO_3$ films was done using XRD, and the spectra can be seen in figure 5.2 for each growth method and thermal treatment under investigation. $Pt/SrTiO_3$ structures suffer from peak overlapping in XRD spectra which makes analysis difficult. However, the strongest relative intensity peak for $SrTiO_3$ can still be seen if the grains are oriented (110) in a cubic perovskite phase, which is evident in figure 5.2 (a) for the PLD grown $SrTiO_3$. This $SrTiO_3$ film, grown at 500 °C using PLD, shows evidence for crystallinity due to the (110) peak, indicating that 500 °C was sufficient temperature to induce grain growth. The calculated grain size relating to the (110) peak is given below. At this point it is not known if the film is fully crystallised. Electron microscopy experiments are conducted in the following section to investigate the crystallisation further. Remaining peaks are interpreted as Pt due to their intensities, which shows (111) and (200) grain orientations, with possible $SrTiO_3$ peaks being hidden at these positions. XRD results are analysed further in order to extract grain size using the Scherrer equation. In the analysis, peak broadening is attributed to grain size, where a broader peak gives smaller grains [12]. After extracting the contribution from instrumental broadening, grain size estimates based on the (110) peak for the film grown at 500 °C by PLD was 63 nm. The benchmark sample grown by PLD at 700 °C gave a strong (110) peak (not shown), and calculated grain size was 84 nm.

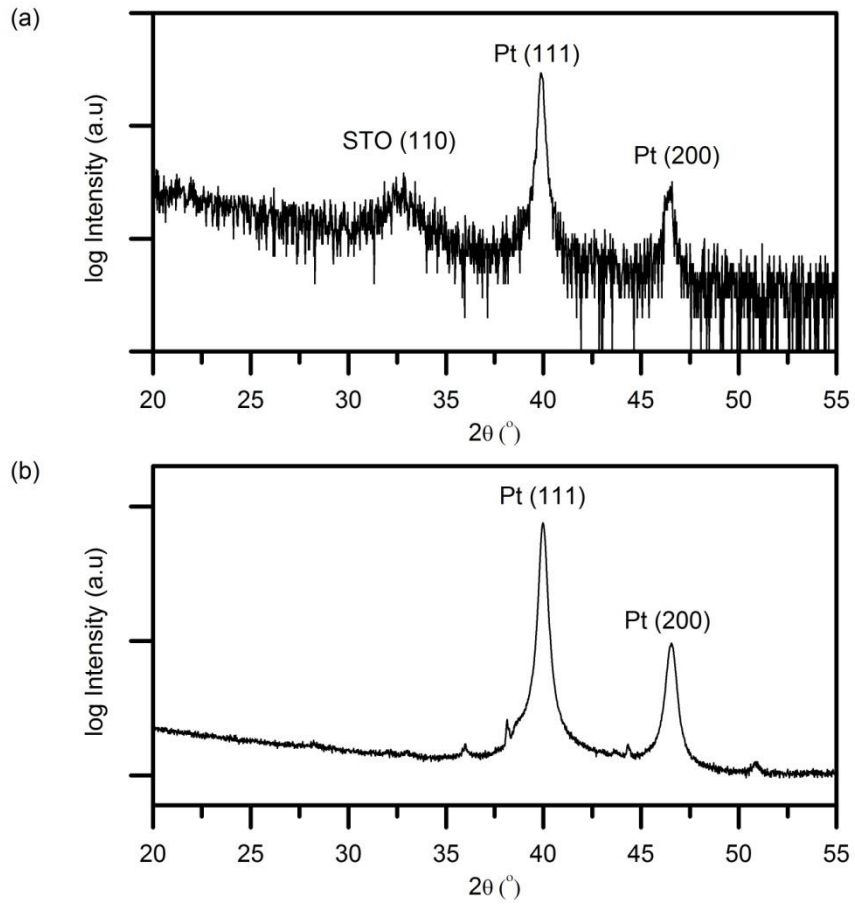


Figure 5.2: XRD spectra of the STO films grown using PLD (a) at 500 °C and using ALD (b) and subsequent PDA at 500 °C.

Turning attention to the ALD film in figure 5.2 (b), there are no changes in the Pt peaks, which still exhibit (111) and (200) grain orientations. However, after RTP at 500 °C, there is no indication of crystallisation in the $SrTiO_3$ film due to the absence of the (110) peak, which was previously observed in the $SrTiO_3$ film grown at 500 °C using PLD. At this stage it is not possible to deduce if the film is amorphous as $SrTiO_3$ peaks may be situated at the Pt peaks as explained previously. The outcome would be a preferred orientation for the grains in the SrTiO3 film which is controlled by the grain orientation of the underlying Pt. The absence of a $SrTiO_3$ peak means Scherrer analysis could not be performed. An XRD spectrum of the 600 °C post-deposition annealed $SrTiO_3$ deposited using ALD was performed (not shown) and a slight (110) peak was visible. It has been shown previously that annealing $SrTiO_3$ by

RTP at 600 °C, which was deposited directly on Si(100) by ALD, produced weak (110) reflections, while increasing the RTP temperature to 650 °C gave strong (100), (110) and (200) peaks [10]. However, the RTP temperature was not increased in this case due to a detrimental effect on leakage current, as shown further into the study. The large increase in leakage current is thought to be due to Pt instability during high temperature anneals, and would otherwise be absent in $SrTiO_3$/Si structures.

The previous XRD results suggested that $SrTiO_3$ films can be crystallised at 500 °C when grown using PLD, while a 500 °C post deposition anneal after ALD

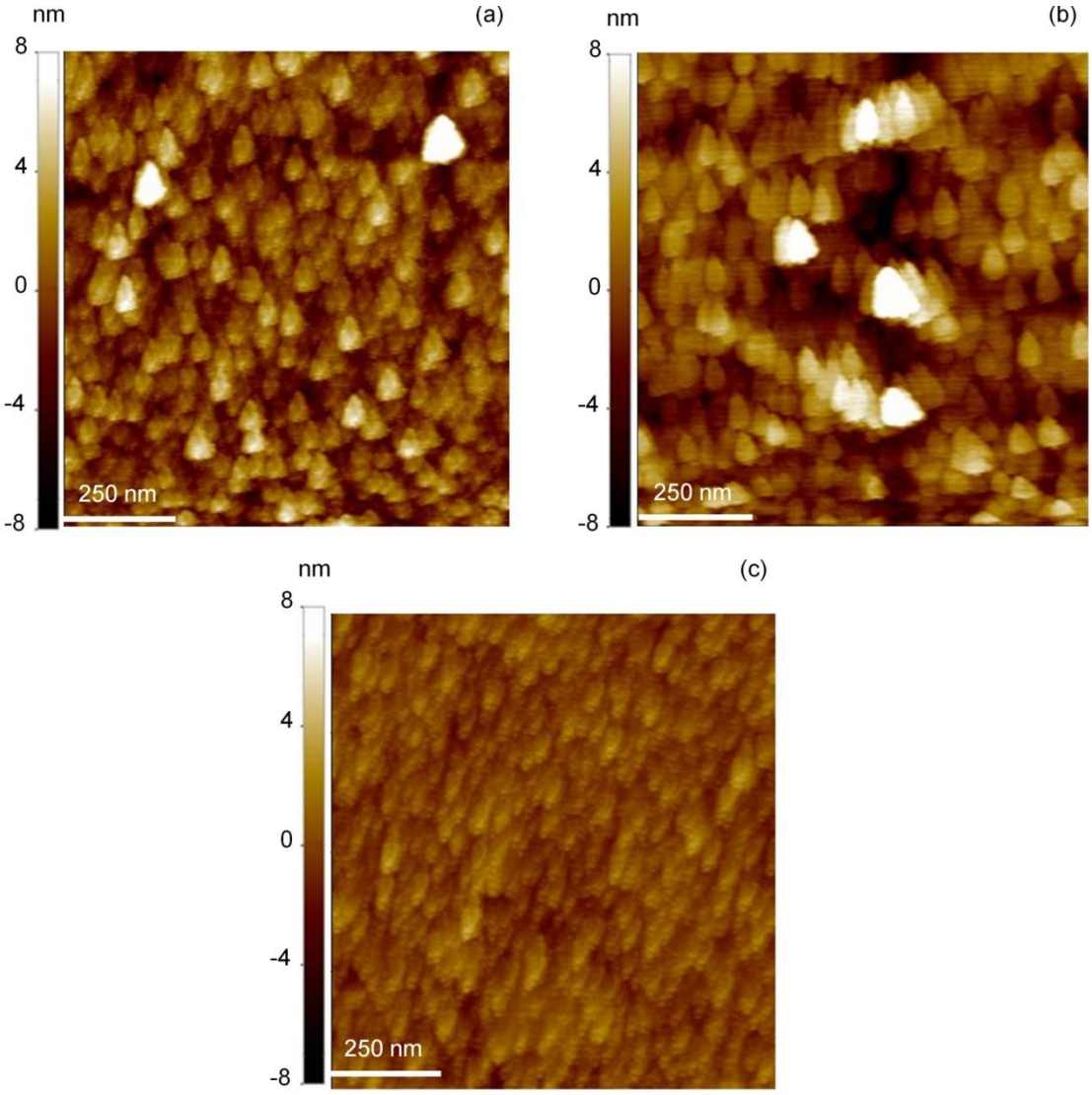


Figure 5.3: AFM images of the STO films grown using PLD at 500 °C (a), PLD at 700 °C (b) and using ALD at 250 °C and subsequently annealed using RTP for 120s in N_2 at 600 °C (c).

did not induce the equivalent (110) grain orientation. AFM images may show the existence of grain structures, and support the XRD results shown above. Figure 5.3 presents topography scans of $SrTiO_3$ grown using PLD and ALD. Figure 5.3 (a) is the PLD film grown at 500 °C. The image shows a possible grain structure, with intersecting grain boundaries. The results are suggestive that 500 °C was sufficient to induce grain growth in this sample. In comparison, a benchmark $SrTiO_3$ film grown at 700 °C using PLD is shown in figure 5.3 (b). It is apparent that figures 5.3 (a), (b) are similar in structure as each sample under investigation shows an equivalent topography. Grain size examination was conducted to verify the Scherrer analysis performed on the XRD spectra, and resulted in 47 nm ± 23 nm grains in the 500 °C film (figure 5.3 (a)) and 55 nm ± 30 nm grains in the 700 °C film (figure 5.3 (b)). The results are close to the grain size estimates using the XRD spectra shown above. Surface roughness was 3 nm for the sample grown at 700 °C and 2 nm for the sample grown at 500 °C. It is likely that increasing the temperature in the PLD process results in slightly larger grains, but at the expense of an increase in the surface roughness of the deposited films.

The AFM topography scan for the ALD film annealed using RTP at 600 °C is shown in figure 5.3 (c). After RTP at 600 °C, the ALD film is smoother than the films grown using PLD and the surface roughness is 0.9 nm. Surface roughness during the annealing process of the ALD film only slightly increased, from 0.4 nm in the as-grown phase, to 0.9 nm in the 600 °C annealed phase. Figure 5.3 (c) is indicating granularity in the $SrTiO_3$ film after RTP at 600 °C, rather than evidence for grain growth shown in figure 5.3 (a) and (b) for the films grown using PLD. The granularity may originate from the underlying Pt during the annealing process. Pt is known to be unstable as the temperature increases to 500 °C and above, where agglomeration [25], structural changes and the onset of hillocks at the insulator/Pt interface have been seen [26, 27].

Therefore, the instability of the Pt may have disturbed the grain growth in the $SrTiO_3$ film during RTP. The result may explain the granular structure for $SrTiO_3$ as evident in figure 5.3 (c). Further evidence of the Pt instability is shown in section 5.3.2 in terms of leakage current analysis.

The AFM images support the previous XRD results: $SrTiO_3$ grown using PLD at 500 °C is sufficient temperature to induce grain growth in the films. In figure 5.2 (a) the XRD spectrum shows evidence of a (110) diffraction peak. Increasing the growth temperature to 700 °C produces slightly larger grains, but concurrently increases the surface roughness (figure 5.4 (a), (b)). However, growth by ALD and post-annealing up to 600 °C does not induce an equivalent grain structure due to the absence of the (110) diffraction peak. It is possible that $SrTiO_3$ peaks are situated at the Pt peak positions in the XRD spectrum shown in figure 5.2 (b). However, AFM imaging shows a granularity of the $SrTiO_3$ surface. It was proposed that the instability of the underlying Pt electrode caused the granularity in the $SrTiO_3$ film as the Pt is known to agglomerate and change in structure at the annealing temperatures used. The Pt may be inhibiting the grain growth of the $SrTiO_3$ film during RTP, which can explain the lack of a diffraction peak in figure 5.2 (b).

The experimentally observed influence of the growth technique and RTP on the film crystallinity is now investigated using TEM. For the $SrTiO_3$ films deposited using PLD, it is apparent that 500 °C is sufficient to crystallise the sample (figure 5.2, 5.3). Bright-field images of $SrTiO_3$ are shown in figure 5.4 for the film grown using PLD at 500 °C, and a film grown at 700 °C is given for direct comparison of the crystallisation. It is clear that the film is crystallised when observing figure 5.4 (a), and the structure of the film is columnar. In the first stages of deposition, material is deposited at various points on the substrate. These initial islands grow upwards as the

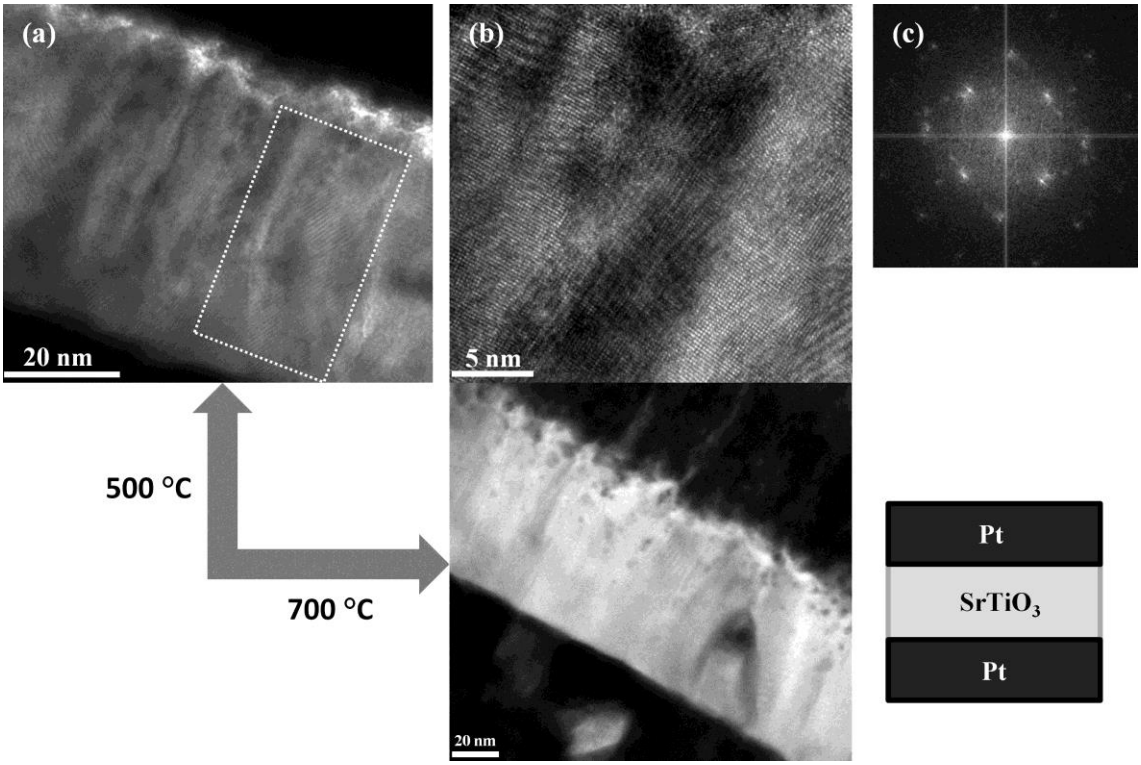


Figure 5.4: Bright-field TEM images of STO films grown using PLD at 500 °C. Cross-section of the STO thickness with example region shown for high resolution imaging (a), high resolution of the STO grains (b) and electron diffraction pattern (c). Also shown is the bright-field TEM image of STO grown at 700 °C indicated by the arrow. The schematic indicates the particular layer contrast in each image.

deposition continues, and the individual columns eventually coalesce towards the top surface. The result is a rougher top interface with the Pt electrode when compared to the bottom Pt/$SrTiO_3$ interface. However, when comparing the top interface between the 500 °C and 700 °C grown $SrTiO_3$ films, the top interface is smoother for the film grown at 500 °C. The previous AFM images (figure 5.3) confirm that when the PLD growth temperature increases to 700 °C, the surface roughness of the $SrTiO_3$ films also increases. Figure 5.4 (b) shows a high resolution image of a typical region highlighted in figure 5.4 (a). Taking into account the influence of Moire fringes, an individual column is a uniform grain orientation. Furthermore, uniform grains are seen to extend across individual columns, showing that a column edge does not necessarily indicate a grain boundary. However, as seen in the electron diffraction pattern in (c), the random arrangement of diffraction points indicates a polycrystalline film. The XRD spectrum in

figure 5.2 (a) gave a single diffraction peak of (110) orientation for perovskite $SrTiO_3$, while Pt diffraction peaks may hide the remaining $SrTiO_3$ peaks. It is therefore probable that $SrTiO_3$ peaks are situated at the Pt peak positions due to the electron diffraction pattern shown in figure 5.4 (c); the random distribution of diffraction points is attributed to numerous grain orientations. The absence of any concentric rings in figure 5.4 (c) shows that the grain size is relatively large with respect to the region of interest.

The XRD spectrum shown in figure 5.2 (b) demonstrated that growing the $SrTiO_3$ film using ALD, and then RTP at 500 °C was not sufficient temperature to induce grain growth. The RTP temperature was then increased to 600 °C, which in turn gave a slight diffraction peak in the XRD spectrum (not shown). The TEM images of the $SrTiO_3$ sample after the 600 °C anneal is shown in figure 5.5. The cross-section in figure 5.5 (a) was taken at various tilt angles to assess the contrasting areas. From the analysis, the sample is deduced to be partially crystallised, with some indication of

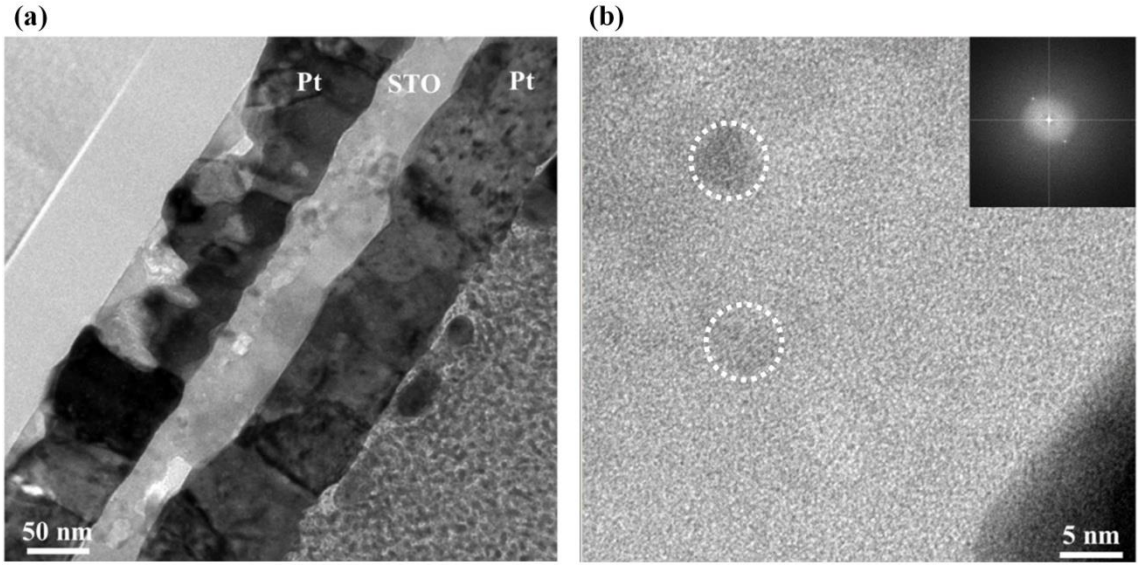


Figure 5.5: Bright-field TEM images of STO films grown using ALD and subsequently annealed at 600 °C. Cross-section of the STO thickness shown in (a) and high resolution image shown in (b). Inset is the electron diffraction pattern. Circled regions are nanocrystallites.

larger crystals. Figure 5.5 (b) is a high resolution image of the sample, where the marked regions also show nanocrystallites. The nanocrystallites are surrounded in an amorphous matrix, which leads to an explanation of the XRD spectrum. It is evident that RTP up to 600 °C was insufficient to fully crystallise the $SrTiO_3$ film and partial crystallisation occurred. The partial crystallisation leads to a weak X-ray diffraction peak and also the electron diffraction points shown in the inset of figure 5.5 (b). In comparison, the $SrTiO_3$ grown at 500 °C using PLD was fully crystallised, as shown in figure 5.4.

After investigating the crystallisation of $SrTiO_3$ thin films using either PLD grown at 500 °C, or ALD and subsequent RTP at 500 °C for 120 s in N_2, the chemical composition and carbon impurities are now discussed in terms of high resolution XPS spectra. A top layer of $SrTiO_3$ was etched on the surface to remove any surface contaminants. The resulting spectra are shown in figure 5.6 for the as-grown ALD film and PLD film grown at 500 °C. The spectra consists of Sr 3p1/2 at 280 eV, Ti 2p1/2 and Ti 2p3/2 at 461 eV and 455 eV, respectively, and O 1s at 530 eV, consistent with ref. 10. It has been reported that $SrTiO_3$ grown using ALD and undergoing a subsequent anneal consisted of crystalline $SrTiO_3$ embedded in various amounts of amorphous $SrCO_3$ [10]. Therefore, the partial crystallisation shown in figure 5.5 for the $SrTiO_3$ film grown using ALD may be due to high amounts of amorphous $SrCO_3$ in the sample. In order to determine the film composition of the $SrTiO_3$ film grown using ALD, the XPS spectra is now studied. A detailed description of $SrCO_3$ in thin film $SrTiO_3$ grown using ALD, and the impact of annealing, is given in [13]. The study shows evidence of slightly higher binding energy, attributed to $SrCO_3$, in the O 1s spectra, and whose intensity decreases from the peak point in the as-grown phase to the

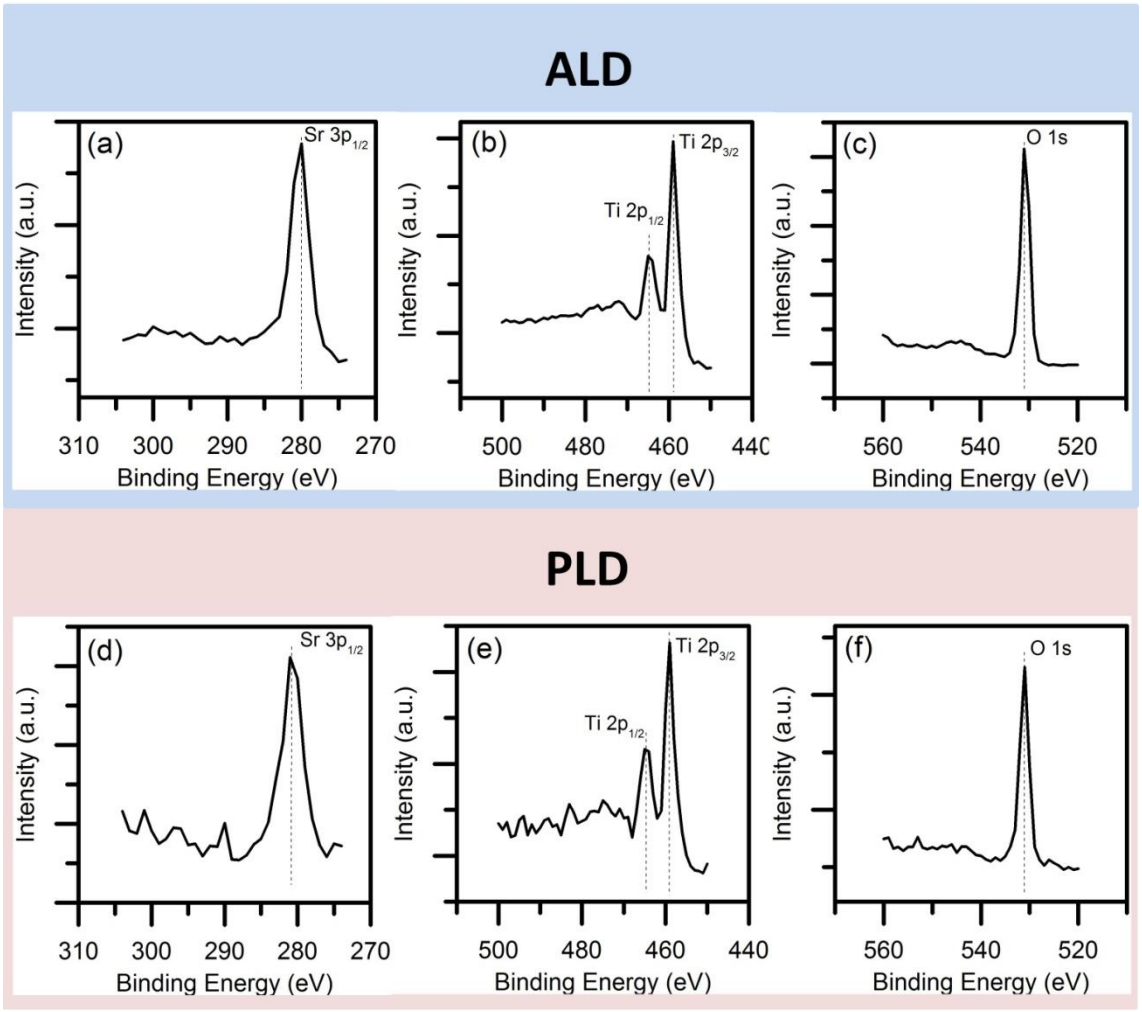


Figure 5.6: High resolution XPS spectra of the ALD STO in an as-grown phase: (a) Sr 3p, (b) Ti 2p, (c) O 1s. XPS spectra of the PLD STO grown at 500 °C: (d) Sr 3p, (e) Ti 2p, (f) O 1s.

annealed crystalline phase. The result in figure 5.6 (c) shows a single peak is evident in the O 1s spectrum for the $SrTiO_3$ film grown using ALD. The absence of any remaining peak suggests that the film is free from any strontium carbonate. In comparison, the O 1s spectrum for the $SrTiO_3$ film grown using PLD is shown in figure 5.6 (f). The spectrum is similar to that shown figure 5.6 (c) for the ALD film in which a single peak is evident. A peak for C 1s may also be seen in Sr 3p spectra. However, figures 5.6 (a), (d), both show a lack of any shoulder region in the Sr 3p peak, also indicating that each film is free from any carbon contamination.

The high resolution XPS spectra in figure 5.6 are now analysed for stoichiometry in the ALD and PLD $SrTiO_3$ films. Further to carbon contamination

affecting the crystallisation of $SrTiO_3$, changes in film composition may also cause a shift in the required temperature for crystallisation. Previous studies [14] have shown an increase in the Ti content increases the crystallisation temperature of $SrTiO_3$, while a Sr-rich film causes a decrease in the required temperature [10, 15]. The variations in binding energy for each of the constituent elements in the ALD and PLD films are shown in figure 5.6. There is minimal variation in binding energy between the ALD and PLD films in the corresponding Sr, Ti and O spectra. Therefore, an approximate film composition is suggested between the samples. Table 5.1 shows the results of the chemical concentrations of the films using quantitative analysis performed on the XPS spectra. From the data, it is apparent that the $SrTiO_3$ film grown using PLD is Sr-rich, with an atomic percentage of 26.6 %. In contrast, the $SrTiO_3$ film grown using ALD shows 19.8 % Sr content. The Ti content in the PLD film is 18.3 %, and 22.9 % in the ALD film. These results confirm that when $SrTiO_3$ is grown using ALD, the film is Ti-rich, while growing $SrTiO_3$ using PLD, the film is Sr-rich. It is apparent that the lack of crystallisation in the $SrTiO_3$ film deposited using ALD is impacted by the film composition, and is confirmed in [10, 14, 15]. Moreover, it has been reported that laser fluence strongly affects the deposition of complex oxides when grown using PLD [16]. Lower laser fluence promotes Sr ablation from the target when compared to Ti, and results in a Sr-rich film. Therefore, this method of controlling laser fluence in a PLD process can lead to desired low temperature crystallisation of $SrTiO_3$ films.

	$SrTiO_3$ Stoichiometric	**$SrTiO_3$ ALD AD**	**$SrTiO_3$ PLD 500 ° C**
Sr (%)	**20**	**19.8**	**26.6**
Ti (%)	**20**	**22.9**	**18.3**
O (%)	**60**	**57.3**	**55.1**

Table 5.1: The calculated atomic percentages of Sr, Ti, O, in the as-grown ALD film and PLD grown film at 500 °C. Values were extracted from the high resolution XPS spectra in figure 5.6.

5.3.2 Electrical properties

Attention is now turned to the electrical properties of the $SrTiO_3$ films. Capacitance measured in perovskite insulators should decrease when the applied electric field increases, as well as yielding high zero-bias permittivity. Figure 5.7 shows the permittivity as a function of applied electric field in the $SrTiO_3$ films deposited by PLD at 500 °C and 700 °C which is the benchmark sample. Also shown in figure 5.7 is the $SrTiO_3$ film deposited by ALD in the as-grown phase and also after RTP at 600 °C. Due to the lack of crystallisation in the $SrTiO_3$ film after a 500 °C anneal (figure 5.2), the 600 °C anneal stage is shown in figure 5.7. For the $SrTiO_3$ film grown using ALD, the calculated permittivity using the parallel-plate capacitance formula $C = \varepsilon/t$ (C = capacitance/area, ε = permittivity, t = thickness), is seen to increase from 25 to 51 after RTP at 600 °C. This is attributed to the more crystallised nature of the sample. However, the permittivity of the PLD film is measured as 160 when the deposition

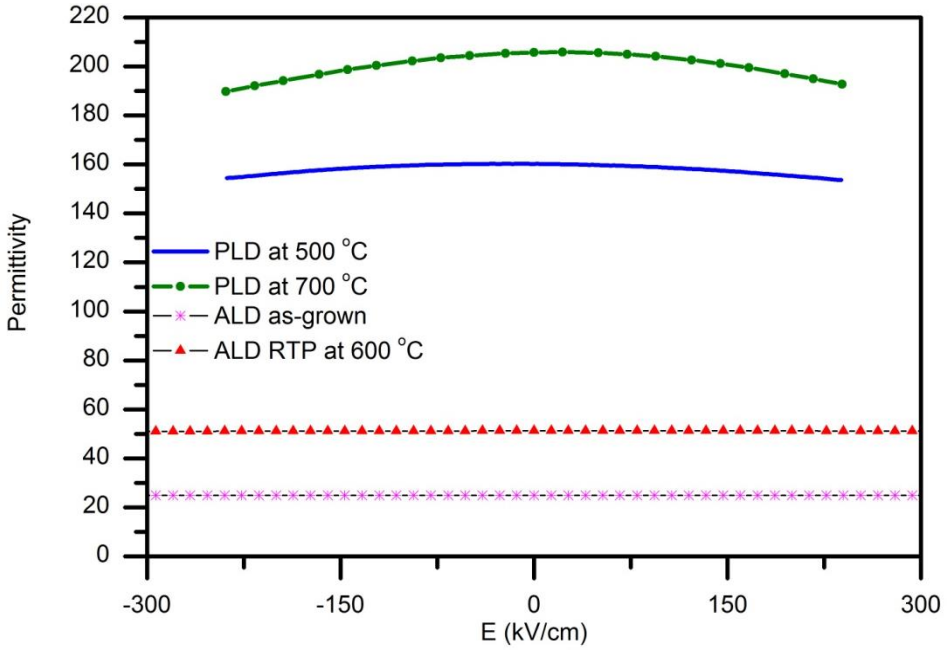


Figure 5.7: Permittivity measured in ALD and PLD $SrTiO_3$ films. The ALD film measured is as-grown and after RTP at 600 °C. The PLD film were grown at 500 °C and 700 °C.

temperature was 500 °C. Once more, the high permittivity is attributed to the crystallisation of the sample, which showed full columnar structures (figure 5.4) and a strong diffraction peak (figure 5.2). The PLD film grown at 700 °C did show higher measured permittivity, which is most likely due to a larger grain size, as calculated in section 5.3.1. The film is also slightly thicker for the film grown at 700 °C (90 nm) compared with the 500 °C film (63 nm), which may impact the permittivity further due to dead layer effects. Chapter 6 explores the impact dead layers have on $SrTiO_3$ films grown using PLD in more detail.

Equation 5.1 is now used to calculate the tunability of the samples under investigation. The $SrTiO_3$ film grown using ALD before RTP shows linear characteristics in figure 5.7 due to the amorphous structure. In fact, there is a slight positive increase in capacitance, which is described by a double layer capacitance caused by oxygen vacancies [17, 18]. This is an important property in high-κ materials in which $dC/dV > 0$, a deleterious characteristic in linear dielectrics such as HfO_2. After RTP, the $SrTiO_3$ film grown using ALD still shows approximately linear characteristics in figure 5.7, and the tunability calculated using equation 5.1 is < 1% ($E_o \rightarrow$ 500 kV/cm). RTP did induce slight tunable properties, but as the TEM image in figure 5.5 shows, the film is dominated by the amorphous phase. In figure 5.7, the $SrTiO_3$ films grown using PLD show the only visible evidence of decreasing permittivity with electric field, with tunability calculated at 4.1 % and 6.3 % for 500 °C and 700 °C growth temperatures, respectively (E_o = 240 kV/cm). It is evident that the increase in growth temperature leads to improvement in the permittivity, as well as the tunable properties of the perovskite. Further studies on the correlation between permittivity and tunability are given in chapter 6.

From figure 5.7, it is clear that the crystallisation impacts the achieved capacitance in each perovskite film. The influence from partial crystallisation is evident due to the increase of permittivity in the $SrTiO_3$ film grown using ALD after RTP; however, this was at a higher temperature than the initial requirement of 500 °C for BEOL applications. Furthermore, the 600 °C anneal only induced slight tunability, shifting the trend from what is expected in a linear insulator, to $n < 1$ %. In figure 5.7 the $SrTiO_3$ film grown using PLD at 500 °C showed clear evidence of tunability. There is also a large increase in permittivity when compared to the film grown using ALD and then annealed at 600 °C. However, the calculated tunability was low (4.1 %), which is less than what is required for tunable capacitors (→40 % at > 100 MHz). The results are explained due to the composition of the film, which contains pure Sr. A pure Sr-based titanate has a low phase transition temperature, where the permittivity and tunability increase with decreasing temperature approaching the phase transition [19]. However, alloying with Ba can shift the phase transition temperature [20], which can lead to increased permittivity and tunability at room temperature. Alloying the $SrTiO_3$ films with Ba in order to increase the tunable characteristics is explored in section 5.4.

The leakage current in the $SrTiO_3$ films is now studied. In figure 5.8 the characteristics of the $SrTiO_3$ film grown using ALD before and after RTP at 600 °C are shown. In addition to the leakage current, a fitted model describing the results is shown [21]. The model describes the leakage current through thin films taking into account the influence from both the interface and bulk of the sample. Current can be inhibited by electron injection and tunnelling at the interface, where the bulk is considered conductive; on the other hand, the interface may allow high electron injection, and the bulk of the sample is therefore the limiting component. Careful consideration of each is required to fully model the leakage current.

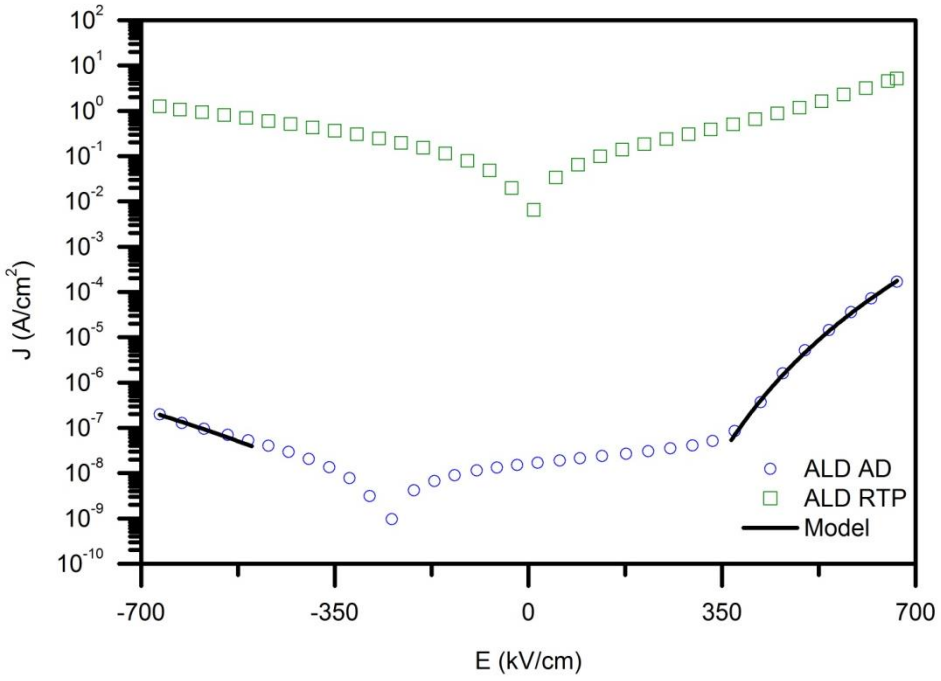


Figure 5.8: Leakage current density measured as a function of electric field in the $SrTiO_3$ film grown using ALD. The fitted model is described in [21].

There is a clear asymmetric trend to the leakage current for the as-grown sample (figure 5.8), with a large increase in the positive region for $E > 350$ kV/cm. Positive charges at the bottom electrode interface is given in [21] as an explanation of the asymmetry. The fixed positive charges play a role in the concentration of deep traps at the interface which promote electron injection, and hence affect leakage current density in the film. An internal electric field is generated at the bottom interface, which repels any mobile electron donors, such as oxygen vacancies, away from the bottom interface. The result is a bigger distance between the trapping sites and the bottom $Pt/SrTiO_3$ interface. Conversely, there is no internal electric field at the top interface, and electron traps are allowed to lie close to the electrode/insulator boundary. The implications on leakage current with applied bias are as follows: in the first instance, a positive voltage on the top electrode will push mobile electron donors towards the bottom interface, offsetting the repulsion from the fixed positive charge. At a certain voltage, the traps are pushed a required distance towards the bottom interface, and

electron tunnelling may ensue from the electrode into the traps. However, applying a negative voltage to the top electrode, the internal electric field is now parallel to the applied field, and mobile traps are pushed close to the top interface, reducing the distance between the traps and the injecting electrons. As such, electron tunnelling may occur at smaller applied negative voltages, which leads to quicker saturating tunnelling current with respect to voltage.

This asymmetry, caused by the fixed positive charge, has implications on the leakage current mechanism that dominates in the film with the applied voltage. For the positive applied voltage, the tunnelling current begins to saturate as the traps are pushed closer to the fixed charge at the bottom interface. The bulk mechanism, controlled by the dielectric quality, will begin to dominate at a specific voltage when the traps are pushed a sufficient distance toward the bottom interface. On the other hand, when negative voltage is applied, the interface traps are no longer inhibited at the top interface, and electron tunnelling is rate-limited at a much lower voltage; therefore, the bulk mechanism controls the leakage much earlier in the process of increasing the negative voltage. In each case, the barrier heights extracted for the films grown using PLD and ALD allow reflection on the dominant leakage mechanism. Further to the perceived leakage asymmetry with bias, the role of electron traps and fixed positive charge with greater density at one electrode is described in terms of resistive switching in [22].

The role of carbon as an impurity has been explored as a possible origin to the fixed positive charge [23]. In addition, a study in [24], which explores the role of carbon contamination in leakage current, states that the carbon most likely originates from the crucible in the electron beam evaporation used for deposition of the bottom Pt

electrode. Leakage current in $BaTiO_3$ with TiN electrodes is investigated in section 5.5, and shows a symmetric leakage trend.

Analysing the results in figure 5.8, the as-grown sample shows the lowest leakage current, and can be attributed to the amorphous nature of the film, in addition to the discussed bulk and interface leakage mechanisms. The fitted model in this circumstance describes an interface blocked current at low positive voltage, where electron tunnelling is the dominating factor, with subsequent thermionic emission through trapping sites in the bulk of the sample as the voltage is increased to approximately 350 kV/cm. At this applied electric field, the electron traps are pushed sufficiently close to the bottom interface such that the tunnelling component of the leakage is no longer rate limited. The negative applied electric field shows a bulk dominated mechanism due to the close arrangement of mobile traps at the top interface, having been pushed by both the fixed positive charge and the applied electric field. The leakage current barriers are shown in table 5.2, and compared with the PLD film in the next section. Nevertheless, as the values show, for the negative applied bias the trap-assisted-tunnelling barrier (Φ_{TAT}) is zero, indicating a high electron injection from the top electrode with no interface limited tunnelling. The bulk mechanism is Poole-Frenkel, where the barrier is Φ_{PF} = 0.58 eV, giving a leakage mechanism that is described solely by electron trap hopping through the insulating film. For the barrier under positive bias, Φ_{TAT} = 0.4 eV, indicating a limitation to electron tunnelling when the electrons are injected from the bottom electrode. However, as the barrier Φ_{PF} = 0.3 eV, it is evident that the leakage is described by both a contributing interface and bulk limited current in this bias region. The model accurately describes the leakage current in the as-grown, amorphous $SrTiO_3$ grown using ALD in both the negative and positive bias regions.

After RTP at 600 °C, the $SrTiO_3$ film shows a large increase in leakage current (figure 5.8). The large increase meant further raising the annealing temperature was not conducted. The asymmetry is no longer evident, and a new mechanism is dictating leakage current through the sample. Previous results confirmed the $SrTiO_3$ film after RTP was only partially crystallised, such that the large leakage current is unlikely to be due to grain boundaries. Surface roughness was also smooth, and lacked any pinholes or microcracks. A possible cause for the increase in leakage is the instability of the Pt electrode during RTP as Pt is known to agglomerate at high temperature [25]. The agglomerating Pt may spike through the insulating film and create electrical shorts. Energy-dispersive X-ray spectroscopy (EDX) has been performed on previous $SrTiO_3$ films grown using ALD after RTP (not shown), and results confirm the hypothesis of Pt shorts. In addition, studies in [26, 27] show that $Pt/Ti/SiO_2/Si$ undergo changes in structure and chemical composition at temperatures ≥ 500 °C. Hillocks were also shown in SEM imaging in the Pt/Ti electrodes [27], which further confirms the instability of the bottom electrode, and is therefore most likely the cause of the large increase in leakage of the ALD film after RTP.

The leakage current in the films grown using PLD is shown in figure 5.9. The model is also fitted to the 700 °C deposited film, which shows a correlation to the fitted model in figure 5.8 for the as-grown $SrTiO_3$ deposited by ALD. Each film shows larger leakage current when compared with the as-grown ALD film from figure 5.8. This may result from the crystallised phase of each of the PLD films, which results in direct leakage paths for electron flow resulting from grain boundaries [28]. As charge traps, such as oxygen vacancies [21], are associated with both the interface injection of electrons and subsequent thermionic hopping through the bulk of the sample, it is likely that the bulk traps have conjugated at the grain boundaries in the bulk. A study on HfO_2

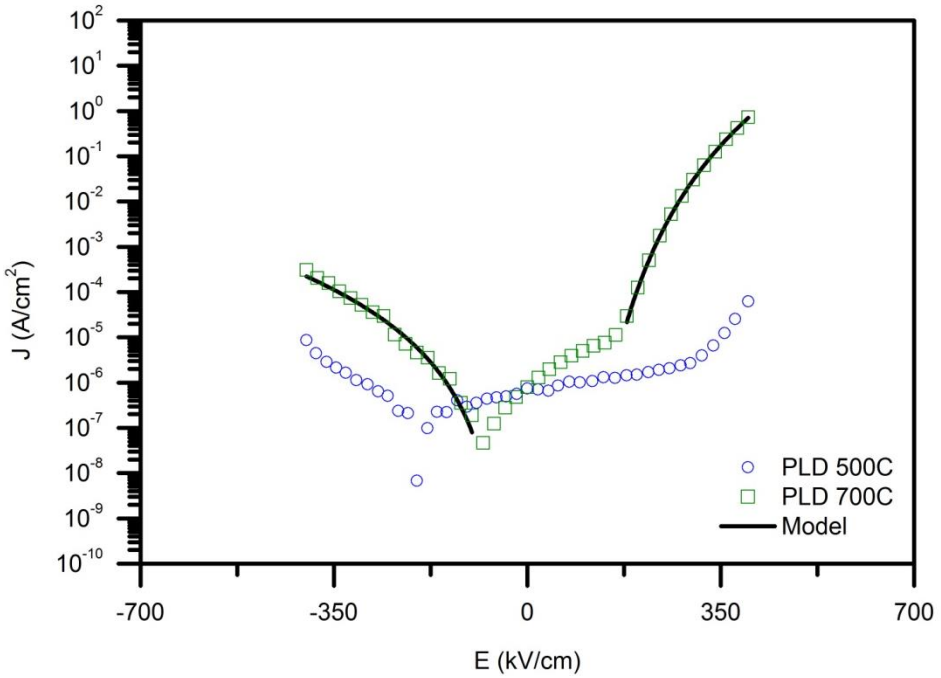


Figure 5.9: Leakage current density measured as a function of electric field in the $SrTiO_3$ films grown using PLD. The fitted model is described in [21].

showed larger oxygen vacancy concentrations at grain boundaries when compared to the concentration in the grains [29]. This would result in more direct paths for current flow through the sample, creating a lower resistive insulator when the film is crystallised. The amorphous $SrTiO_3$ film grown using ALD would therefore have a random distribution of bulk traps. Figure 5.10 shows a schematic of the possible influence on leakage current due to crystallisation when comparing the amorphous $SrTiO_3$ film grown using ALD, to the crystallised phase when grown using PLD.

In figure 5.9, the film grown at 500 °C by PLD shows lower leakage current than the 700 °C growth of $SrTiO_3$ by PLD. However, the TEM images in figure 5.4 demonstrate that each film is fully columnar, with grain size only slightly larger when the film is deposited at 700 °C. What is evident about the leakage current in figure 5.9

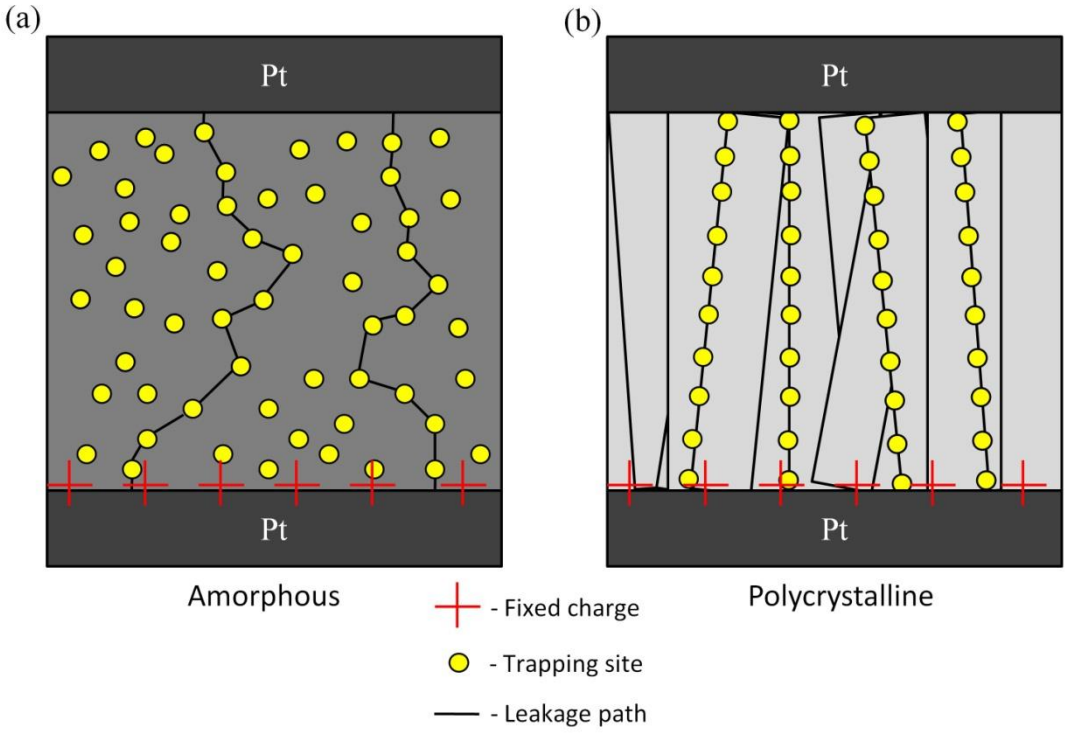


Figure 5.10: Schematic of leakage paths through trapping sites in the amorphous ALD film (a) and polycrystalline PLD film (b).

is that the film grown at 500 °C begins its asymmetric increase in the positive bias region at approximately 350 kV/cm; this is approximately equal to the electric field for the $SrTiO_3$ film grown using ALD at 250 °C (figure 5.8). This region is reached at approximately 125 kV/cm for the $SrTiO_3$ film grown using PLD at 700 °C. As explained previously, this asymmetric increase in leakage current occurs when the bulk leakage mechanism begins to dominate. At this point, the tunnelling current at the interface is no longer rate limited, and the bulk traps control the electron flow through the insulator. Explanation of the rate-limitation of tunnelling current was in terms of the repulsion of the mobile electron donors against the positive fixed charge at the bottom interface. Therefore, when the asymmetric increase in leakage current occurs, the applied electric field is high enough to confine the electron traps close to the electrode interface. For the $SrTiO_3$ film grown using PLD at 700 °C, the applied electric field at the asymmetric leakage region is 125 kV/cm, which is the field considered necessary to

overcome the internal electric field at the bottom interface originating from the fixed positive charge. The amorphous $SrTiO_3$ film grown using ALD, and the film grown using PLD at 500 °C, have electric fields at this asymmetric region of close to 350 kV/cm. The initial assumption, taken from the differing electric fields required for the onset of leakage asymmetry, is that the fixed charge density in the film grown using PLD at 700 °C is lower when compared to the films grown using ALD, and PLD at 500 °C. The difference in the sample properties may originate from growth temperature, where the film grown using ALD is deposited at 250 °C, and the low temperature growth film using PLD is at 500 °C, compared with the high temperature of 700 °C in the benchmark film grown using PLD. Therefore, the temperature during deposition is suggested as impacting the density of the fixed charges at the bottom interface. An explanation due to the influence of growth temperature may arise due to the increased energy in the PLD chamber at 700 °C. If the fixed charge is carbon based, 700 °C may be sufficient energy for reaction with the oxygen content in the PLD chamber, creating CO_x compounds, in turn reducing the density of fixed charges at the interface. Unfortunately, experiments based upon XPS depth profiling were unable to quantify the concentration of carbon at the interface to a suitable resolution. However, the hypothesis currently explains the shift in the applied electric field inducing the leakage asymmetry between films grown at different deposition temperatures.

Further to the influence of growth temperature on the asymmetric leakage current, the $SrTiO_3$ film grown using PLD at 700 °C shows an overall increase in leakage current across the full applied electric field. Expanding on the hypothesis of reacting carbon with oxygen in the PLD chamber at 700 °C, this would lead to an overall reduction in the O content required for titanate deposition, creating greater oxygen vacancies in the sample. This particular defect is considered as the electron

donor traps in the film [21, and references therein], which further impacts both the tunnelling and bulk mediated leakage mechanisms. Therefore, any increase in concentration of oxygen vacancies would supplement an increase in leakage density both when the interface or bulk was the limiting factor, as seen in figure 5.9 (bulk in negative bias region, interface up to 125 kV/cm and bulk thereafter). The XPS data in table 5.1 showed that the film grown using ALD at 250 °C contained greater oxygen content over the equivalent film grown using PLD at 500 °C. The result supports the earlier hypothesis for correlating the reducing leakage current with reduction in oxygen vacancies.

The barrier heights calculated from the model fitted in figure 5.9 for the film grown using PLD at 700 °C is shown in table 5.2, along with the previously discussed leakage barriers in the film grown using ALD. For the film grown using PLD, the negative bias region shows a barrier Φ_{TAT} = 0.1 eV; this barrier in the negative bias region for the film grown using ALD is 0 eV. The calculated barrier highlights the process of electrons that are injected at the top electrode interface and tunnel into deep traps. The barrier is larger for the film grown using PLD, suggesting that the electrons do not tunnel as readily into the traps at the top interface in comparison with the film grown using ALD. Considering a lower density of fixed charges at the bottom interface in the film grown using PLD due to growth temperature, the traps will be pushed less towards the top interface as only the applied electric field is influencing their movement. The film grown using ALD consists of the applied electric field and internal field of fixed positive charges, which would therefore push the traps closer to the top interface. Electrons would tunnel more readily due to the reduced distance, resulting in a lower barrier height. There is a slight change in the contributing bulk barrier, Φ_{PF} = 0.55 eV for the film grown using PLD, and Φ_{PF} = 0.58 eV for the film grown using

	ALD		PLD	
	Φ_{TAT} (eV)	Φ_{PF} (eV)	Φ_{TAT} (eV)	Φ_{PF} (eV)
E > 0	**0.4**	**0.3**	**0.3**	**0.2**
E < 0	**0**	**0.58**	**0.1**	**0.55**

Table 5.2: The calculated barrier heights from the leakage current in the film grown using ALD from figure 5.8 and in the film grown using PLD at 700 °C from figure 5.9.

ALD. The slight change in barrier height suggests that the leakage current flows through the bulk by thermionic emission more readily in the film grown using PLD, which is shown in figure 5.9, compared with figure 5.8 for the film grown using ALD, due to higher leakage current. The increased leakage current may be due to the greater concentrations of oxygen vacancies in the film grown using PLD.

In the positive bias region, the tunnelling barrier is Φ_{TAT} = 0.3 eV for the film grown using PLD, and 0.4 eV for the film grown using ALD. The lower barrier height for the film grown using PLD further implies that electron tunnelling at the bottom interface occurs more readily in this film due to a lower concentration of fixed positive charges. The bulk barrier is Φ_{PF} = 0.2 eV for the film grown using PLD, and 0.3 eV for the film grown using ALD. The calculated bulk barrier heights support the hypothesis of a greater density of oxygen vacancies in the film grown using PLD because a lower barrier describes a greater bulk conduction current.

5.4 Low Temperature Growth of $Ba_xSr_{1-x}TiO_3$

5.4.1 Material properties

The results in the previous section showed that thin film $SrTiO_3$ grown using PLD at 500 °C crystallised the perovskite, and electrical measurements gave high permittivity; however, the tunable capacitance achieved was low at 4.1 %. $SrTiO_3$ is known to have a low phase transition temperature, so room temperature measurements of capacitance and tunability will be reduced in comparison to perovskites with corresponding phase transition temperatures close to 300 K. However, the phase transition temperature can be shifted when the composition of the film is changed. It is known that alloying a pure $SrTiO_3$ perovskite with Ba ions raises the transition temperature to greater values [20]. In this section, the $SrTiO_3$ films investigated above are alloyed with a high concentration of Ba in order to achieve a greater value of permittivity, and most importantly increase the tunability. The Ba content is selected at 80 %, and the film composition is now $Ba_{0.8}Sr_{0.2}TiO_3$.

XRD was performed on the $Ba_{0.8}Sr_{0.2}TiO_3$ film, and results are shown in figure 5.11. The film was grown on $Pt/Ti/SiO_2/Si$ by PLD at 500 °C such that it only

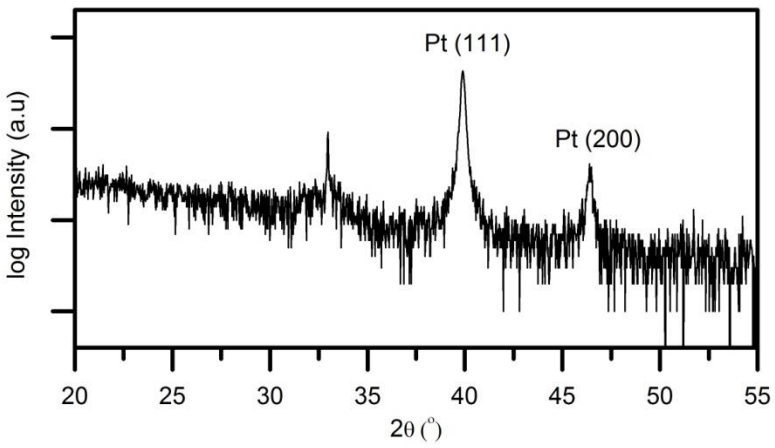


Figure 5.11: XRD spectrum of the BST film grown using PLD at 500 °C.

differs from the $SrTiO_3$ films investigated previously due to the additional Ba content. The spectrum shows a very slight and broad peak at the diffraction angle for $SrTiO_3$ oriented as (110). This peak does not represent a crystallised phase in the film due to its peak position as $Ba_{0.8}Sr_{0.2}TiO_3$ should have a slightly left shifted peak in comparison to $SrTiO_3$. In addition, the broadness of the peak would indicate unphysically small grain sizes using Scherrer analysis. Remaining peaks are attributed to Pt as described in figure 5.2.

The previous XRD results show a lack of evidence for crystallinity in the $Ba_{0.8}Sr_{0.2}TiO_3$ film. TEM imaging was performed in order to confirm the XRD results. Figure 5.12 shows the bright-field high resolution image of a cross-section of $Ba_{0.8}Sr_{0.2}TiO_3$. It is evident from the image that the film is still in an amorphous phase as there is a lack of any long-range ordering between the atoms. There are no visible

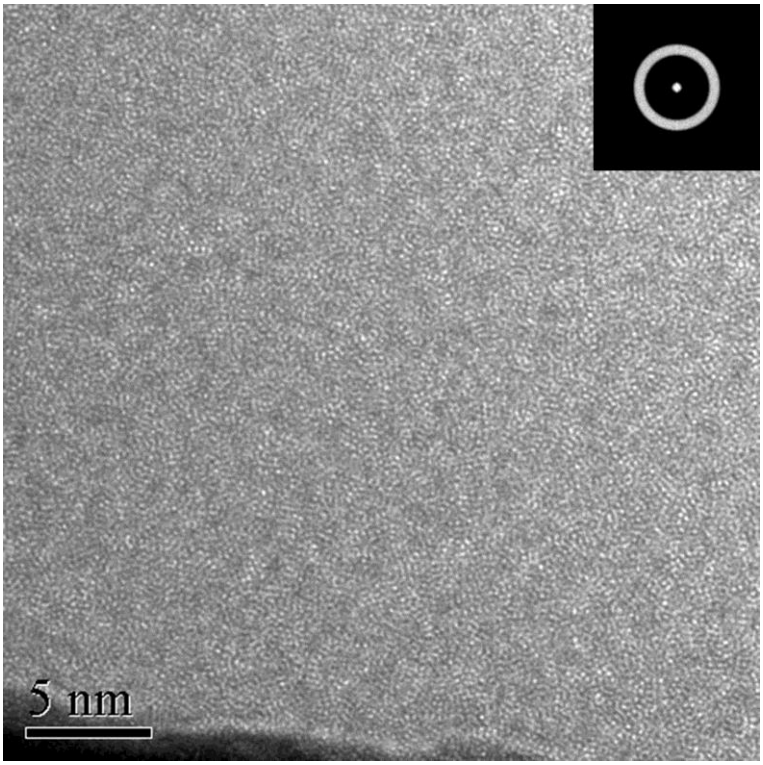
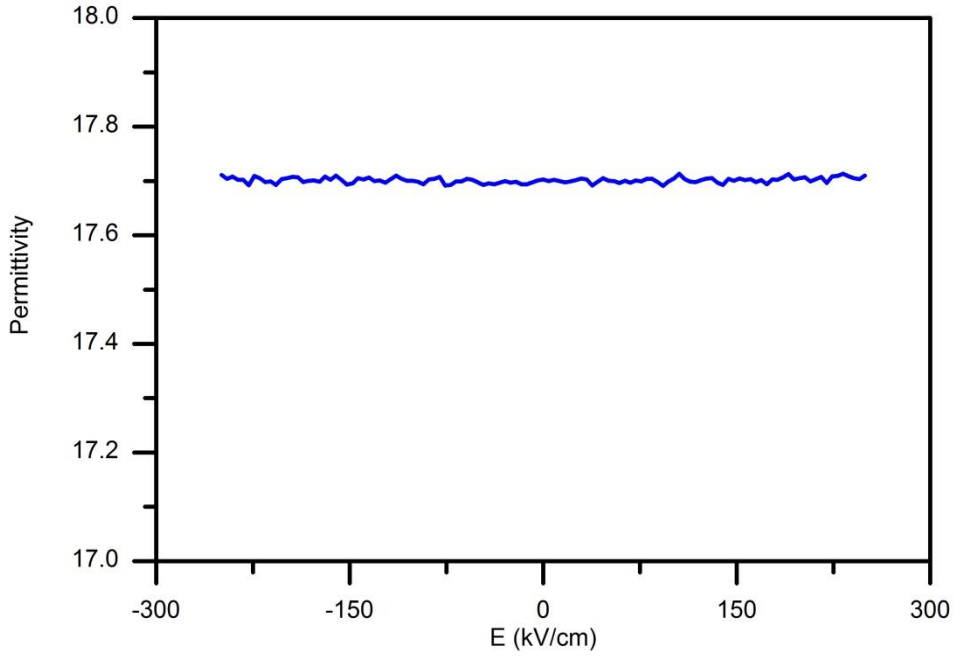


Figure 5.12: Bright-field TEM images of the BST film grown using PLD at 500 °C. Region shows high resolution region of BST. Inset shows the electron diffraction pattern.

grains, and the film has not grown in the previously observed columnar structure (figure 5.4 (a)). The inset in figure 5.12 is the corresponding electron diffraction pattern, and constitutes the direct electron beam and a strong ring of back scattered electrons. This further suggests that the film is not crystallised as there are no diffraction spots shown. From both the XRD and TEM results, $Ba_{0.8}Sr_{0.2}TiO_3$ grown using PLD at 500 °C has not crystallised the film. This is in contrast to the pure $SrTiO_3$ film shown previously with a full columnar structure (figure 5.4), and a strong diffraction peak at (110) (figure 5.2).

5.4.2 Electrical properties

The electrical characteristics of $Ba_{0.8}Sr_{0.2}TiO_3$ are now investigated for permittivity and tunability. The permittivity response to applied electric field is shown in figure 5.13. The permittivity is measured at 17.7, which is low when compared to the $SrTiO_3$ film also grown at 500 °C using PLD. However, this value is close to the measured permittivity in the as-grown $SrTiO_3$ sample deposited using ALD. Therefore, the amorphous phase in the $Ba_{0.8}Sr_{0.2}TiO_3$ film has resulted in the low permittivity. In addition, the $Ba_{0.8}Sr_{0.2}TiO_3$ film also shows no indication of tunability as the permittivity stays constant across the bias range. The fact that the permittivity is linear further highlights that the tunable characteristic of the perovskite crystal does not contribute to the polarization in the $Ba_{0.8}Sr_{0.2}TiO_3$ capacitor, and confirms the amorphous phase of the film.



5.13: Permittivity measured in the $Ba_{0.8}Sr_{0.2}TiO_3$ film grown using PLD at 500 °C. E from ± 250 kV/cm in increments of 5 kV/cm.

The previous results shown for $Ba_{0.8}Sr_{0.2}TiO_3$ indicate that the film is amorphous, which impacts the electrical measurements adversely in terms of low permittivity and zero tunability. XRD results did not show a diffraction peak, and TEM results confirmed the lack of a grain structure. Alloying the $SrTiO_3$ film with Ba was done in order to induce greater permittivity and tunability. However, the major impact of alloying $SrTiO_3$ with 80 % Ba has been on the crystallinity of the $Ba_{0.8}Sr_{0.2}TiO_3$ film. The lack of any tunability and a severely reduced permittivity of 18 (160 in $SrTiO_3$), shows that 80 % Ba content is too high if the films are to be crystallised at 500 °C for BEOL integration. This is due to the crystallisation temperature of the $Ba_{0.8}Sr_{0.2}TiO_3$ film, where the Ba content has increased the required temperature for perovskite crystal growth.

5.5 Low Temperature Growth of $BaTiO_3$

5.5.1 Material properties

Previously shown are the results of $SrTiO_3$ grown using ALD and PLD, as well as $Ba_{0.8}Sr_{0.2}TiO_3$ grown using PLD. In order to study the influence of growth technique and post-annealing further, pure $BaTiO_3$ was also studied for low temperature applications. $BaTiO_3$ thin films were grown using sputter deposition at room temperature, following which an annealing schedule was performed in order to crystallise the samples. The deposition of $BaTiO_3$ was done on either $Pt/Ti/SiO_2/Si$, or $TiN/SiO_2/Si$, such that the impact of the electrode on leakage current can be investigated. The TiN electrodes are fully characterised elsewhere [30].

XRD experiments were first conducted to verify the crystallinity of the samples. Figure 5.15 shows the results of $BaTiO_3$ grown using sputter deposition, after which an anneal was conducted on the films at either 500 °C or 800 °C. 500 °C was chosen to attempt crystallisation at temperatures suitable for BEOL integration. From the figure, there is a lack of any diffraction peak for the 500 °C annealed sample, demonstrating that the film is still amorphous. Increasing the temperature up to 800 °C

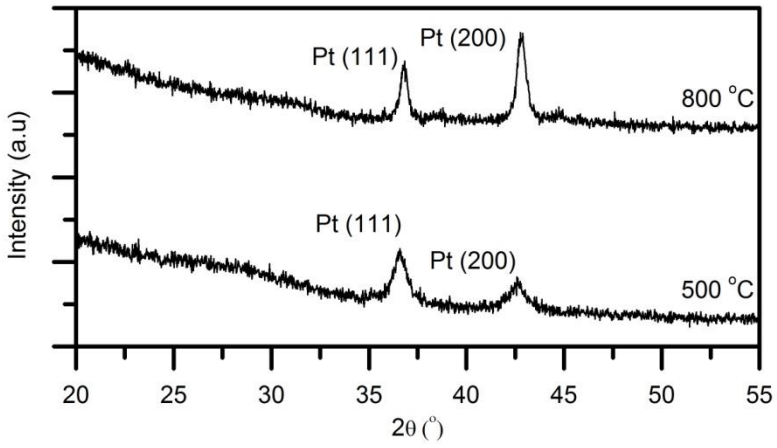


Figure 5.15: XRD spectra of BTO grown using sputter deposition at room temperature and post annealed at either 500 °C or 800 °C.

was intended to induce any degree of crystal growth in the film. The results show that even at temperatures reaching 800 °C, the film stays in its amorphous phase as there is no indication of a diffraction peak. Remaining peaks are attributed to Pt as described previously.

5.5.2 Electrical properties

The previous XRD results suggest that $BaTiO_3$ deposited by sputter at room temperature and post annealed up to 800 °C is not sufficient to crystallise the film. An annealing schedule was conducted on the $BaTiO_3$ film for varying time scales in order to induce crystallisation within the 500 °C temperature constraint. The film was initially annealed at 400 °C for 1 hour, followed by a 500 °C anneal for 2 minutes and then 30 minutes. Capacitance and leakage current was measured at each stage of the process. Permittivity was calculated from capacitance measurements in the sputtered

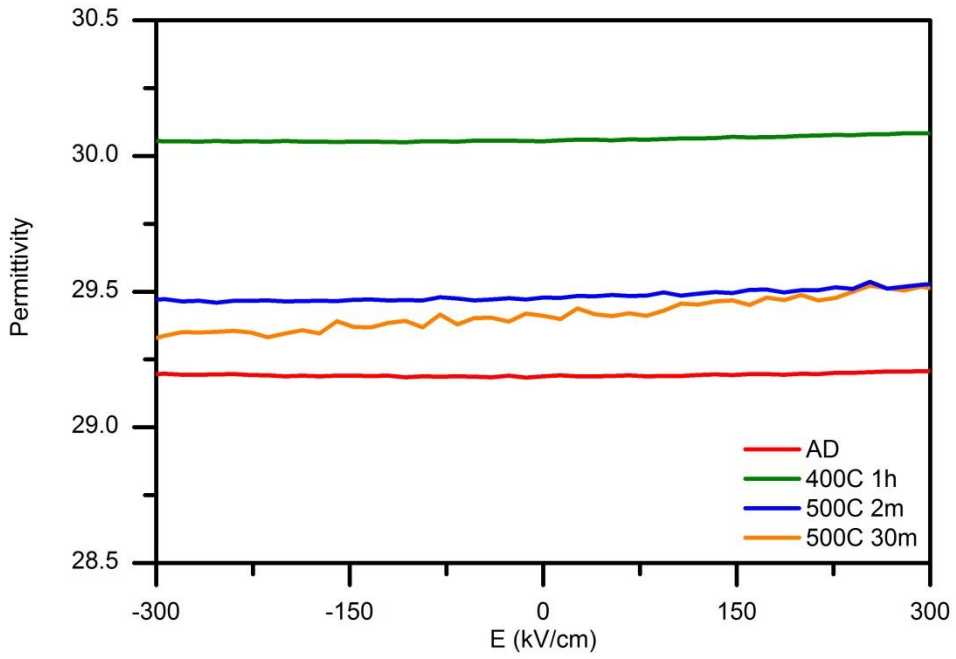


Figure 5.16: Permittivity measured in the sputter deposited $BaTiO_3$ film after different annealing schedules. E from ± 300 kV/cm in increments of 15 kV/cm.

$BaTiO_3$ film, which is shown as a function of electric field in figure 5.16. The high measured permittivity and induced tunability can be used to gauge whether the perovskite film is crystallised.

From figure 5.16, it is evident that the permittivity in the $BaTiO_3$ film is low, with no impact from the length of the anneal. Taking into account the experimental error introduced in the capacitance measurements, the permittivity stays constant across the annealing schedule. There is also a lack of any tunable characteristic in the films, owed to the amorphous structure.

Finally, leakage current measurements were taken on the $BaTiO_3$ film after each stage of the annealing process discussed above. Figure 5.17 shows the results of each measurement. The results show that there is no change in the leakage current at each stage of the anneal schedule. The leakage current results confirm the permittivity calculations in figure 5.16 such that the anneals are insufficient to crystallise the sputtered $BaTiO_3$ film.

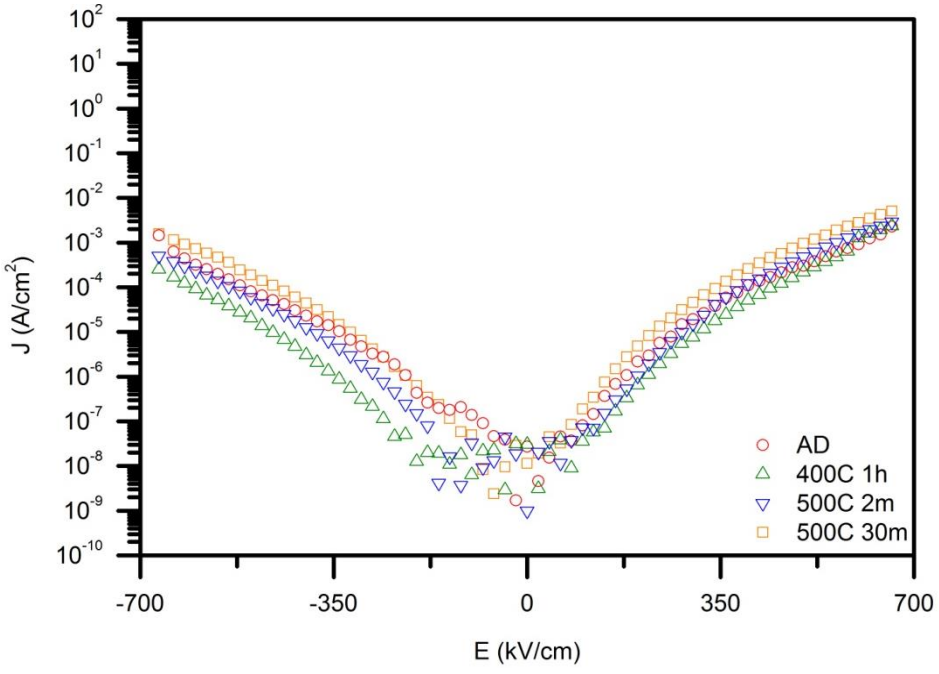


Figure 5.17: Leakage current density measured as a function of electric field in the sputter deposited $BaTiO_3$ film after different annealing schedules.

The leakage current trends in figure 5.17 were measured on $BaTiO_3$ deposited on TiN electrodes. What is apparent in the results is the lack of asymmetry when compared to leakage current measured in $SrTiO_3$ (figure 5.8, 5.9), with each trend in the $BaTiO_3$ film showing symmetric leakage current at the turning point of zero applied electric field. The result supports the hypothesis of fixed positive charge acting on the $Pt/Ti/SiO_2/Si$ substrates, in which the fixed charge is introduced from the crucible in the deposition of Pt [24]. With no positive charge, the leakage current reverses direction at zero bias as there is no longer an internal electric field at the bottom interface. The lack of any fixed positive charge also impacts the movement of the bulk trapping sites in $BaTiO_3$. The absence of a built-in electric field, originating from the fixed positive charge, no longer impedes the movement of the bulk traps towards the bottom $BaTiO_3/TiN$ interface. This is shown in figure 5.17, in which an equal contribution of interface and bulk conduction mechanisms is seen in the positive and negative bias regions. Therefore, the study of leakage current on $BaTiO_3$ deposited on TiN has shown that the asymmetry is eliminated. This is suggestive of a contamination introduced in the deposition of Pt that adversely affects the leakage current in thin films.

The aim of the experiments described here were to determine whether low temperature sputtering of $BaTiO_3$ was a viable solution for BEOL integration. Further studies of depositing $BaTiO_3$ using sputter at low temperature and investigation of high temperature annealing were conducted [31]. A novel multilayer approach was shown to eliminate delamination and pin holes.

5.6 Summary and Conclusion

In this chapter, characteristics of thin film perovskites were investigated for low temperature applications, particularly aimed at BEOL integration. $SrTiO_3$ films were grown using two well-known deposition techniques in ALD and PLD. Further, $Ba_{0.8}Sr_{0.2}TiO_3$ was deposited by PLD in order to compare against the electrical properties of the $SrTiO_3$ films grown at low temperature. $BaTiO_3$ was also grown using sputter deposition at room temperature and then undergoing an annealing process.

Depositing $SrTiO_3$ using PLD at 500 °C, the film was fully crystallised in a columnar structure. Increasing the growth temperature to 700 °C only slightly increased the grain size. However, attempts to reproduce the results using ALD and RTP at 500 °C proved ineffective, and further increasing the annealing temperature to 600 °C was needed to show partial crystallisation. XPS results showed that the bulk of each sample was carbon free. Furthermore, the film grown using ALD was Ti-rich, while the film grown using PLD was Sr-rich. This leads to the conclusion that the lower crystallisation temperature in the film grown using PLD is impacted by film composition. The result may lead to even lower crystallisation temperatures by tuning the Sr content in thin film $SrTiO_3$.

The crystallisation impacted the capacitance properties of the films and the film grown using PLD at 500 °C had a measured permittivity of 160, while the film grown using ALD after RTP at 600 °C achieved only 51. Tunability was also shown at 4.1 % in the film grown using PLD at 500 °C, and approximately linear for the film grown using ALD after RTP at 600 °C.

Growing $Ba_{0.8}Sr_{0.2}TiO_3$ by PLD at 500 °C was done in order to effectively raise the phase transition temperature and induce further tunability in the film. The results showed that the film was still amorphous. Calculated permittivity was low at 18,

and stayed linear when the applied electric field increased. The high content of Ba in the film has increased the crystallisation temperature, in turn making it unsuitable for integration into the BEOL.

Further studies on pure $BaTiO_3$ were conducted on room temperature sputter deposited films and subsequent post-deposition annealing. Results showed that annealing up to 800 °C did not induce crystallisation in the films. An annealing schedule of longer times was performed at 500 °C which proved inefficient at crystallising $BaTiO_3$.

Leakage current characteristics were investigated in the $SrTiO_3$ films, and analysis based upon the model described in [21] was performed. Each film under examination showed asymmetric leakage current. The asymmetric increase in leakage is reached at a lower electric field in the film grown using PLD at 700 °C; therefore, it is hypothesised that a lower density of fixed positive charge is situated at the bottom electrode in this sample. This may be due to the reaction of oxygen in the PLD chamber with carbon contamination on the $Pt/Ti/SiO_2/Si$ substrate. The reaction occurs more readily in the 700 °C deposition due to the higher temperature. Due to this reaction, there will be more oxygen vacancies in the film grown using PLD at 700 °C as oxygen is taken away from the titanate deposition. XPS results support the hypothesis as for the film grown using ALD at 250 °C, a greater oxygen content was shown when compared with the film grown using PLD at 500 °C. The saturating field region in figure 5.8 for the film grown using ALD was also slightly larger (> 350 kV/cm) when compared to the film grown using PLD at 500 °C in figure 5.9 (< 350 kV/cm). Therefore, a higher density of fixed charge would be situated at the bottom interface for the film grown using ALD due to the lowest temperature of deposition. For the sputtered $BaTiO_3$ film on TiN electrodes the leakage current was symmetric across the applied field. This

points to carbon contamination introduced in the Pt deposition as a cause for the leakage asymmetry in the $SrTiO_3$ films.

5.7 References

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Chapter 6

Ferroelectric and Tunable Perovskite Insulators for Integration with Si

6.1 Introduction

Perovskite insulators have attracted particular attention for applications such as ferroelectric random access memories (FeRAM) [1], dynamic RAM [2] and alternative gate materials for metal oxide semiconductor field effect transistors (MOSFETs) [3]. A recent review details their short-term and future prospects for the nanoelectronics industry, further proof of the need to integrate this promising material in next generation devices [4]. A particular region of interest in these materials is the ferroelectric phase, which allows polarization to be retained in the absence of an applied electric field. Ferroelectricity has been the subject of numerous past studies [5 - 8], and is of most relevance in non-volatile memory applications due to its ability to retain its polarisation when power is removed. However, the ferroelectric phase is subject to varying degrees of intrinsic and/or extrinsic influences, ranging from

elemental composition [9], annealing, growth technique [10] and straining [11], among others [12 - 16]. Therefore, it is important to understand the quality of perovskites in terms of their demonstrated ferroelectric properties.

A further region of interest in a perovskite material is the paraelectric phase. Characteristics of the paraelectric phase include ultra-high permittivity, which can be decreased through the application of an increasing electric field, leading to tunable capacitance. Illustrations of the two phases in terms of polarization and derived capacitance as a function of applied bias are given in figure 6.1. The figures are simulated from LD theory given in chapter 2.

The phase of a perovskite is primarily dictated by temperature and described by the Curie-Weiss law, given by

$$\chi = \frac{C}{T - T_c} \tag{6.1}$$

where χ is the dielectric susceptibility, T is the operating temperature, T_c is the Curie temperature and C the Curie constant. The phase of a perovskite will transition at a temperature $T = T_c$; however, in certain materials such as barium titanate ($BaTiO_3$, BTO), the phase transition temperature can be approximately 10 K above T_c [17].

From equation 6.1, it follows that by increasing the operating temperature beyond T_c, the material will show decreasing susceptibility, and in turn permittivity ($\chi = \varepsilon_r - 1$, where ε_r is the relative permittivity of the material). In contrast, operating below T_c should give negative χ, which leads to instability, and hysteretic characteristics ensue. The aforementioned properties are descriptive of the paraelectric phase when $T > T_c$ and the ferroelectric phase in cases when $T < T_c$. The impact of temperature on the crystal structure is depicted in figure 2.5 for both the paraelectric (figure 2.5 (a)) and ferroelectric (figure 2.5 (b)) phase.

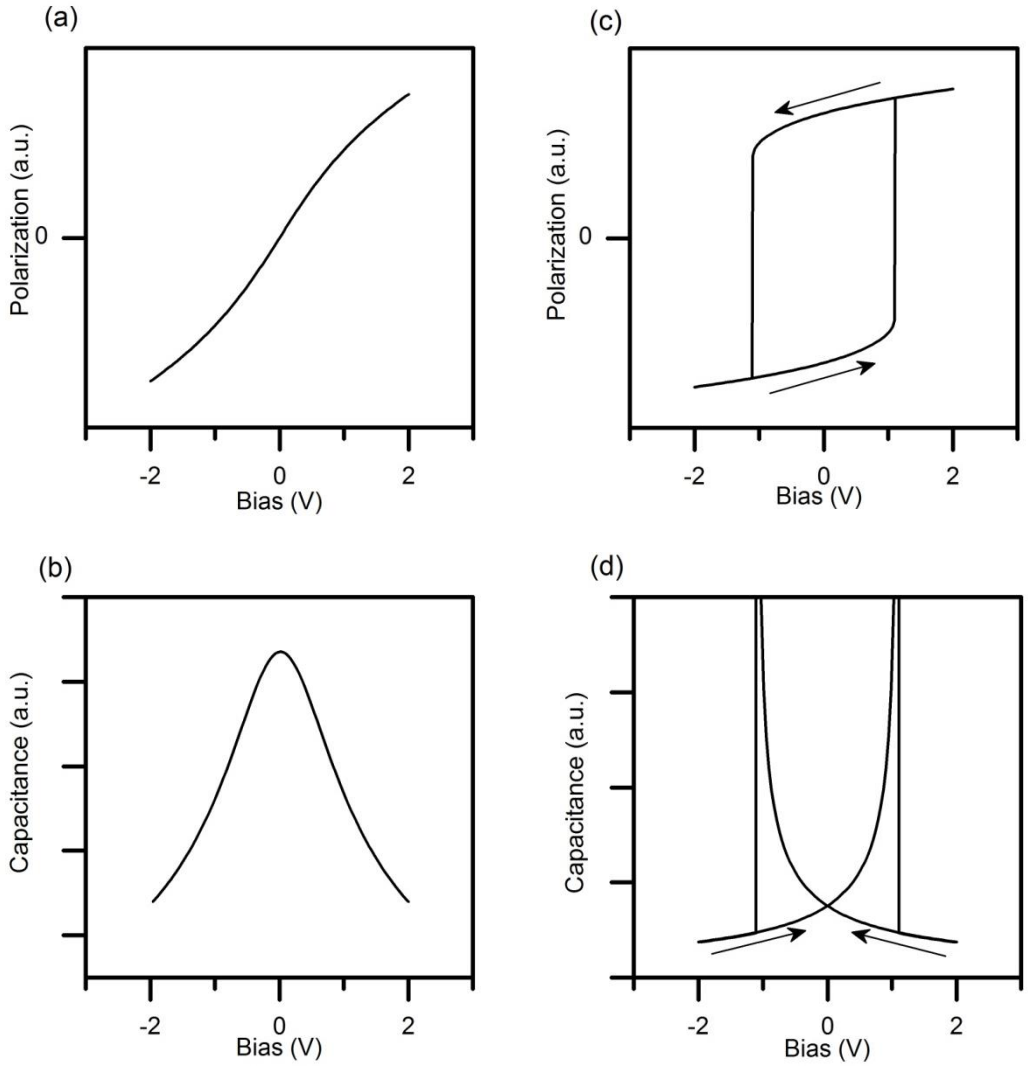

Figure 6.1: Polarization vs bias curve for a paraelectric capacitor (a) and its corresponding tunable capacitance taken as dQ/dV (b). Hysteretic polarization vs. bias for a ferroelectric (c) and corresponding capacitance, showing the instability at the switching field for this ideal case (d).

A key property of a perovskite material is its phase transition temperature, T_c. For the case of $BaTiO_3$ in bulk or powder form, this temperature is approximately 393 K and where the permittivity is a maximum (equation 6.1) [18]. However, experimentally this property is known to change, particularly when dealing with thin film perovskites, and the permittivity peak tends to broaden or shift altogether [19]. In the high temperature phase ($T > T_c$), the perovskite crystal is cubic due to thermal agitation. Decreasing the operating temperature past the phase transition point ($T < T_c$)

the perovskite crystal is tetragonal; long-range coulombic ordering results due to the balance of the thermal and electrostatic forces, allowing an elongation of the crystal c-axis and the creation of a built-in permanent dipole. The tetragonal deformation of a ferroelectric crystal allows alignment and subsequent reorientation of these permanent dipoles through the application of an external electric field.

A so-called "size driven phase transition" has been studied previously, specifically on particles [20] or freestanding films [22] of perovskite material. It places a critical limit on crystal grain size, such that a smaller grain structure shifts the phase transition temperature to lower values. Therefore, the size driven phase transition leads to materials that are paraelectric in phase at operating temperatures previously expected to be in the ferroelectric phase. Numerous studies on $BaTiO_3$ nanoparticles have estimated a critical grain size, below which no ferroelectric properties are seen, to lie between 17 - 190 nm [ref. 20 and references therein]. The grain size dependence has also been incorporated into LD theory in which grain size was varied from 50 - 1200 nm in dense $BaTiO_3$ ceramics [21]. The results showed a progressively reduced distortion of the tetragonal phase with decreasing grain size, in concurrence with a shift in the phase transition temperature to lower values as the grain size reduces. Conversely, a grain size dependence on thin film $PbTiO_3$ was studied, which showed a transition from multidomain to single domain structures at 150 nm grain size or less [22]. The retained tetragonal phase in the single domain structure exhibited a lack of polarization switching under the application of an electric field and low permittivity. The results are attributed to single domain structures in the smaller grains due to the inherent lack of domain walls and their subsequent movement. However, this result was measured on a free-standing film, and hence suffered no influence from the substrate.

For a perovskite in its paraelectric phase, or in fact any high-κ material, an effective way to gauge its permittivity enhancement over a standard insulator is by defining an equivalent thickness; that is, the required thickness of a SiO_2 insulating layer to achieve the same capacitance [23, 24]. Equation 6.2 defines the equivalent oxide thickness, EOT

$$t_{SiO_2} = EOT = \left(\frac{\kappa_{SiO_2}}{\kappa}\right) t_{high-\kappa} \tag{6.2}$$

where *EOT* is the equivalent SiO_2 thickness and κ_{SiO2} its dielectric permittivity, κ is the permittivity of the replacement perovskite insulator and $t_{high\text{-}\kappa}$ its thickness. It is therefore desirable to have a large permittivity, κ, in order to lower the required SiO_2 thickness needed to achieve the same capacitance. The problems regarding exceedingly thin insulating layers of SiO_2 are highlighted in this relationship: for *EOT* < 1 nm, leakage current will be extremely large. High-κ insulators offer equal capacitance density with thicker films, mitigating the issue of leakage current.

However, the relationship highlighted in equation 6.2 assumes a single layer insulator, without any extrinsic surface or interfacial layers. If the linear relationship of equation 6.2 is plotted, further details of the device may be investigated, such as any interfacial layer thicknesses. It is in fact inaccurate to calculate permittivity from the slope of the relationship in equation 6.2 if such interfacial layers are affecting the device characteristics. In addition, a well-known phenomenon known as dead layers impact the characterisation of high-κ insulators [25-27]. Dead layers cause a film thickness dependence on permittivity such that thinner films achieve a lower permittivity, and hence tunability. Therefore, dead layers impact the tunable characteristic of a perovskite material, in addition to their high-κ properties. Chapter 2 of this thesis discusses the possible origin of the dead layer further.

In this chapter, thin films of $BaTiO_3$ deposited by pulsed laser deposition (PLD) are investigated. The films are grown on $Pt/Ti/SiO_2/Si$ substrates, and investigated in terms of ferroelectricity for Si integration applications. The results show that thin films of $BaTiO_3$ are in a mixed phase relationship, consisting of the cubic paraelectric phase (figure 2.5 (a)), in addition to the tetragonal ferroelectric phase (figure 2.5 (b)). Furthermore, it is shown that the cubic phase has a tendency to dominate at room temperature. The dominant cubic phase leads to a measured reduction in the overall remnant polarization, a common occurrence frequently reported in the literature [28] in terms of thin film and grain size dependence. The results confirm a size driven phase transition in thin films clamped to a substrate with columnar structures. The experiments indicate that increasing the heights of the columns by growing thicker films increases the remnant polarization in the thin films. The remnant polarization increase is due to an increase in grain size as the columns grow in height. With an increase in the film thickness, the column widths remain approximately 30 nm in size.

Furthermore, the influence of film thickness is discussed in terms of permittivity and tunability. A new *EOT* model is proposed to take into account interfacial layers, and initial inaccuracies of the model given in equation 6.2 are highlighted. This in turn allows the new model to be applied for cases of dead layers impacting the results of $SrTiO_3$ MIM capacitors. The origins and contributing factors to the dead layer phenomenon are then discussed, and ways of reducing the effect are suggested.

6.2 Experiment

The majority of the sample preparation is explained in section 5.2. However, the $SrTiO_3$ samples grown using PLD are now deposited at 700 °C in order to fully crystallise the material. Thicknesses ranged from 13 nm to 90 nm. Pure $BaTiO_3$ was grown using PLD at 740 °C and film thickness varied between 160 nm to 380 nm. Substrates and bottom electrodes were $Si(100)/SiO_2/Ti/Pt$. Most of the electrical and material characterisation techniques are explained in section 4.2 and 5.2.

For the $BaTiO_3$ capacitors, small-signal capacitance-voltage CV measurements were taken at temperatures ranging from room temperature (300 K) to 420 K. CV measurements consisted of both forward (negative to positive sweep) and reverse (positive to negative sweep) biasing to analyse the $BaTiO_3$ film. All remaining measurements were taken at room temperature. Large-signal hysteresis measurements were taken on a Radiant Precision Premier II. Raman spectra were acquired by a HORIBA scientific LabRam using a 514 nm laser. Electrostatic force microscopy (EFM) images were taken using an NSC 14 Au/Cr cantilever and piezo force microscopy (PFM) images with an NSC-36 Ti/Pt b cantilever. The amplitude and phase of the cantilever oscillation was read using a Stanford Research Systems DSP lock-in amplifier, model SR830.

6.3 The EOT Model

High-κ dielectrics are known to be thermodynamically unstable when in contact with Si [29, 30]. This is undesirable as increasing the capacitance density in MOS devices requires a high-κ material in contact with Si. In the gate stack of a MOS capacitor, where there is an interface of high-κ material with Si, interfacial layers can be created due to inter-diffusion and reaction at high processing temperatures. An interfacial layer in series with the high-κ material can severely degrade the achieved capacitance [31], and possibly create unwanted defect states and/or hopping sites leading to an increasing leakage current density [32 - 34].

In order to gauge the effectiveness of a high-κ material, it is common to state its equivalent oxide thickness (*EOT*), as described in section 6.1. The analysis shows the thickness a SiO_2 insulating capacitor would require to be in order to achieve the same capacitance of a high-κ counterpart; therefore, a lower *EOT* translates to a higher permittivity material. The standard model for *EOT* is achieved by equating the SiO_2 and high-κ capacitance, and is shown in equation 6.3

$$\frac{\varepsilon_0 \varepsilon_r}{t_{ox}} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{EOT} \tag{6.3}$$

where $\varepsilon_o\varepsilon_r$ is the permittivity of the high-κ material, t_{ox} its thickness and $\varepsilon_o\varepsilon_{SiO2}$ the permittivity of the SiO_2 capacitor. Rearranging equation 6.3 gives

$$EOT = \left(\frac{\varepsilon_{SiO_2}}{\varepsilon_r}\right) t_{ox} \tag{6.4}$$

Equation 6.4, as previously shown in equation 6.2, describes the *EOT* as derived from equation 6.3. The relationship in equation 6.4 for *EOT* allows extraction of permittivity in the high-κ material through interpretation of the slope. It also predicts a zero offset term on the y axis of the plot. This method has been conducted in previous studies to

calculate permittivity and investigate dielectric properties of high-κ material [31, 35-37].

However, due to the formation of unwanted interfacial layers, equation 6.3 used to derive the EOT is now incorrect. The actual achieved capacitance of the MOS gate stack under investigation is contributed to by a high-κ and interfacial layer capacitor in a series configuration. The refined model incorporating the interfacial layer contribution to capacitance has implications on the resulting relationship for *EOT*, and differs substantially from that shown in equation 6.4. Furthermore, solely using equation 6.4 masks information about the interfacial layers, and leads to an incorrect determination of permittivity in the high-κ material under investigation. In order to derive the *EOT* relationship correctly, the series capacitance model is presented in equation 6.5

$$\frac{1}{C_m} = \frac{1}{C_B} + \frac{1}{C_i} = \frac{C_B + C_i}{C_B C_i} \tag{6.5}$$

where the measured capacitance C_m is contributed to by a bulk high-*k* capacitance C_B in series with the interfacial layer capacitance C_i. Rearranging equation 6.5

$$\frac{\varepsilon_o A}{C_m} = \frac{t_{ox} - t_i}{\varepsilon_B} + \frac{t_i}{\varepsilon_i} = \frac{t_{ox} - t_i}{\varepsilon_B} + X_i^{-1} \tag{6.6}$$

where A is the area of the electrode, t_i (t_{ox}−t_i) and ε_i (ε_B) is the thickness and permittivity of the interfacial layer (bulk) capacitor, respectively, and $X_i^{-1} = t_i/\varepsilon_i$. Equation 6.6 describes the capacitance of the system as a whole, including the desired bulk high-*k* contribution in series with an unwanted interfacial layer capacitance in a MOS structure. As the interfacial layer thickness reduces to zero, the capacitance approaches that of a single high-*k* layer, and the measured MOS capacitance in accumulation would revert to that shown in equation 6.3. Equation 6.6 is used to plot

data in order to investigate the interfacial capacitance ratio X_i, which is calculated by any non-zero intercept term. It has been used on numerous occasions to investigate dead layer effects in MIM capacitors, where t_i is assumed as a 'dead' interfacial layer in contrast to the expected high-κ material [25 - 27, 38 - 46]. Further analysis on this topic is given in section 6.4.

Using the more thorough model of capacitance in MOS structures with high-κ material, the EOT can be derived with greater accuracy. Equation 6.5 is now incorporated into the derivation of *EOT*. Equation 6.3 is amended by equating a SiO_2 capacitance with the series capacitance of a high-κ material and interfacial layer. Equation 6.7 is used to derive the more accurate model for *EOT*.

$$C_m = \frac{\varepsilon_o \varepsilon_{SiO_2}}{EOT} = \frac{C_B C_i}{C_B + C_i} \tag{6.7}$$

Rearranging for *EOT* and substituting the relationships for C_B and C_i

$$EOT = \left(\frac{\varepsilon_{SiO_2}}{\varepsilon_B}\right) t_{ox} + \varepsilon_{SiO_2}\left(\frac{1}{\varepsilon_i} - \frac{1}{\varepsilon_B}\right) t_i = \left(\frac{\varepsilon_{SiO_2}}{\varepsilon_B}\right) t_{ox} + EOT_i \tag{6.8}$$

where $EOT_i = \varepsilon_{SiO_2}\left(\frac{1}{\varepsilon_i} - \frac{1}{\varepsilon_B}\right) t_i$ and remaining terms are defined previously. Equation 6.8 shows a new model for *EOT* and is used to analyse the bulk high- permittivity in the series capacitance system. The model is also used to study the influence from the interfacial layer capacitance, contributing to an interfacial EOT_i. When the interfacial layer thickness, t_i, approaches zero, equation 6.8 reverts back to the more familiar model shown in equation 6.4. The key difference between equation 6.8 and 6.4 is the prediction of an intercept term EOT_i, which is related to any unwanted interfacial layer capacitance. The influence of the offset term (EOT_i) is briefly discussed in refs. 47, 48, but with no great detail. Studies calculating the permittivity based upon equation 6.4

have omitted the influence of the intercept term. This leads to incorrect assumptions in the achieved permittivity in high-κ material. The use of equation 6.4 to study high-κ material also ignores any thickness dependence on the permittivity, which is discussed in greater detail in section 6.4.

In order to compare the use of equation 6.4 to equation 6.8, and study the influence of the intercept term, EOT_i, results of EOT as a function of dielectric thickness, t_{ox}, from refs. 31 and 49 are presented in figure 6.2. In figure 6.2 (a) the linear relationship between EOT and t_{ox} is shown, and their results using equation 6.4 for calculating permittivity show $\kappa \approx 40$. However, there is a clear intercept of the EOT close to 8.5 Å, and use of equation 6.4 omits this term. Results should be based upon equation 6.8, which includes the offset term EOT_i, and the calculated permittivity, given as 40, is in fact the bulk value ε_B. Setting the permittivity as constant from the slope also ignores the thickness dependence on permittivity. This is due to the perceived interfacial layer, assumed from the EOT_i term, that will cause a reducing permittivity with film thickness. Results based upon $SrTiO_3$ MIM capacitors as a

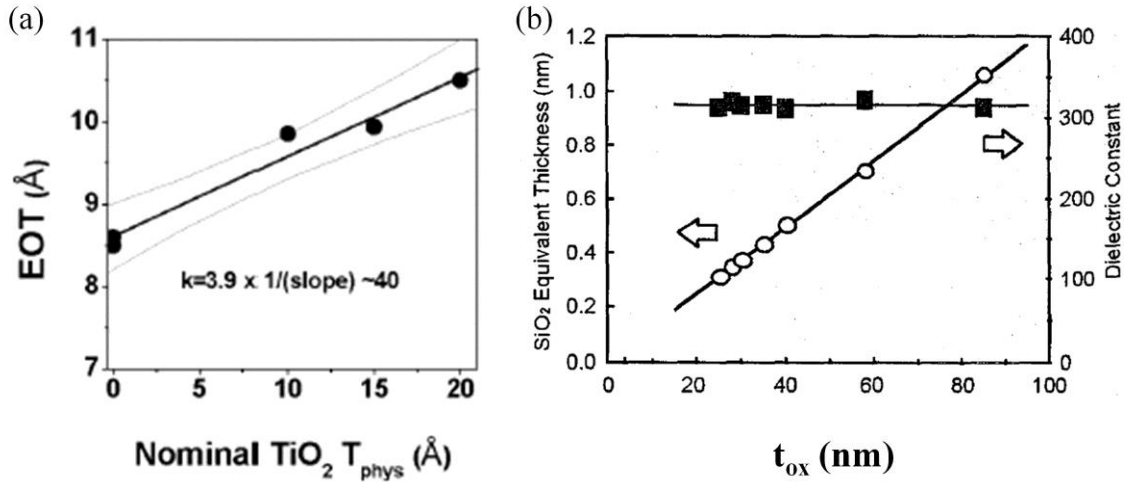

Figure 6.2: *EOT* vs. physical dielectric thickness t_{ox}. Image is taken for (a) from ref. 31 and (b) ref. 49.

function of thickness are explored in section 6.4 in terms of a dead layer. Dead layers affect the permittivity with regards to film thickness in the same way as interfacial layers. It is then an important question to ask whether dead layers are originating from a physical dead layer of material at the interface of the $SrTiO_3$ film and the electrode.

In contrast, figure 6.2 (b) shows *EOT* plotted as a function of t_{ox} using equation 6.8 with zero intercept. Use of equation 6.8 calculates the correct permittivity in each of the varying thicknesses of capacitors under investigation. In addition, with zero intercept (EOT_i = 0), equation 6.8 reduces to the description for *EOT* shown in equation 6.4, and analysis based upon this equation would give correct results. Also shown in figure 6.2 (b) is the permittivity relationship with film thickness. The fact that permittivity stays constant with film thickness confirms the influence of EOT_i, such that, if EOT_i is zero, interpretation of the slope correctly calculates permittivity for each thickness of capacitor electrode separation.

The intercept term, EOT_i, becomes an important indicator of the influence on measured capacitance from any unwanted interfacial layers. Equation 6.9 highlights the relationship between EOT_i and the interfacial capacitance thickness t_i.

$$EOT_i = \varepsilon_{SiO_2}\left(\frac{1}{\varepsilon_i} - \frac{1}{\varepsilon_B}\right)t_i \qquad (6.9)$$

Equation 6.9 states that EOT_i increases proportionally with the interfacial layer thickness. Therefore, if EOT_i is zero, as shown in figure 6.2 (b), there is no contribution to the measured capacitance from any interfacial layers. In this instance the measured capacitor is a single layer, and deriving the EOT is correctly described by equation 6.3.

In order to further study the impact of EOT_i using equations 6.6 and 6.8, the capacitance of $SrTiO_3$ MIM structures is measured as a function of dielectric

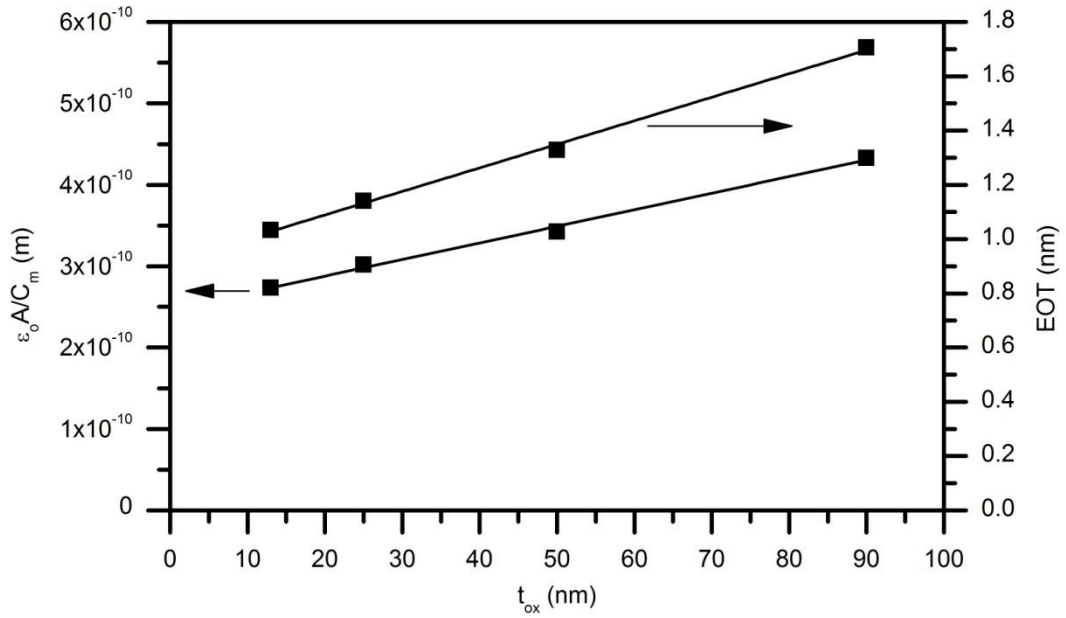

Figure 6.3: Series capacitance model and *EOT* vs. physical dielectric thickness, t_{ox}. Measured data was on STO MIM capacitors deposited using PLD.

thickness. Figure 6.3 shows measured capacitance described by equation 6.6 in the series capacitance system, as well as calculated *EOT* as a function of dielectric thickness between 13 nm and 90 nm. The results presented here are to highlight the modified *EOT* model given in equation 6.8; further analysis on the data for the $SrTiO_3$ capacitors is given in section 6.4. However, the $SrTiO_3$ results are pertinent to the interfacial layer analysis creating a series capacitance configuration due to the non-zero intercepts in figure 6.3.

Analysis based on equation 6.6 and figure 6.3 is done to gauge the impact of the interfacial layer capacitance through calculation of X_i^{-1} (= t_i/ε_i). The intercept gives the inverse interfacial layer capacitance as X_i^{-1} = 0.25 nm. Using equation 6.6, the independent parameters, t_i and ε_i, of the interfacial layer cannot be obtained. From equation 6.6, it is also shown that the slope is used to derive the bulk permittivity with the assumption $t_{ox} >> t_i$, which may not be accurate.

The refined model for *EOT* in equation 6.8 can now be used to analyse the interfacial layer further. From equation 6.8, it is shown that the slope allows extraction of the bulk permittivity without the prior assumption in equation 6.6 of $t_{ox} >> t_i$. The equation also takes into consideration the offset term which gives an interfacial EOT_i at zero physical thickness. This is due to the interfacial layer capacitance described above, which is not considered in standard *EOT* analysis. Using the data extracted from figure 6.3, and rearranging equations 6.6 and 6.8, the interface thickness can be calculated, and conclusions can be drawn as to the origins of the interfacial layer capacitance.

Expanding equation 6.9

$$EOT_i = \varepsilon_{SiO_2}\left(\frac{1}{\varepsilon_i} - \frac{1}{\varepsilon_B}\right)t_i = \varepsilon_{SiO_2}X_i^{-1} - \frac{\varepsilon_{SiO_2}}{\varepsilon_B}t_i \qquad (6.10)$$

From the slope of equation 6.8 and figure 6.3

$$\frac{\delta(EOT)}{\delta t_{ox}} = \frac{\varepsilon_{SiO_2}}{\varepsilon_B}$$

Rearranging equation 6.10 for t_i

$$\frac{\varepsilon_{SiO_2}}{\varepsilon_B}t_i = \varepsilon_{SiO_2}X_i^{-1} - EOT_i$$

$$t_i = (\varepsilon_{SiO_2}X_i^{-1} - EOT_i)\frac{\varepsilon_B}{\varepsilon_{SiO_2}}$$

$$t_i = (\varepsilon_{SiO_2}X_i^{-1} - EOT_i)\left(\frac{\delta(EOT)}{\delta t_{ox}}\right)^{-1} \qquad (6.11)$$

Equation 6.11 shows the interfacial layer thickness in terms of the previously extracted parameters. It can be used to calculate t_i, with previous values of X_i^{-1}, and the slope $\varepsilon_B/\varepsilon_{SiO2}$, both extracted from figure 6.3. This method of interfacial layer thickness

calculation has previously been unattainable when analysis of the *EOT* is solely based upon equation 6.4. Furthermore, calculating the thickness of the interfacial layer allows extraction of its permittivity. In knowing the permittivity of the interfacial layer, conclusions can be drawn as to the origins of this low-κ material formed in series with the bulk high-κ insulator.

In order to confirm the previous analysis, data from ref. 48 is used to calculate the interfacial layer thickness. This is used to confirm the spectroscopic ellipsometry results, which showed an interfacial layer thickness of 2 nm. Using equation 6.11, analysis from the data in ref. 48 calculated an interfacial layer thickness of 1.6 nm, which is in close agreement to the ellipsometry results. Therefore, the new model for *EOT* can be used to gauge the thickness of any interfacial layer that may be created in the fabrication of a high-κ material in series with a Si based material. The permittivity using the calculated thickness of the interfacial layer is ~10. This is close to the permittivity expected of hafnium silicate, and matches the conclusion drawn by the authors in ref. 48. Using the refined *EOT* model, the origin of the interfacial layer has been analysed without the need for ellipsometry measurement of the interfacial layer thickness.

6.4 $SrTiO_3$ MIM Capacitors and Dead Layers

6.4.1 Electrical characteristics

A. Permittivity

Ultra high-κ insulators, such as $SrTiO_3$, suffer from a reduction in maximum permittivity when film thickness decreases due to dead layers. Any dead layer acts in series with the high-κ insulator, which was described in terms of an interfacial layer in a MOS structure in the previous section. From equation 6.5, it is observed that the measured capacitance is always dominated by the smaller of the two series capacitances. With relatively thick dielectrics, C_m provides a good measure of the expected capacitance. However, as the thickness of capacitors required for nanoscale devices is gradually decreased and reaching nanometers in length, the impact of any interfacial capacitance begins to dominate. This is due to the fact that, as dielectrics get thinner, C_B is continuously increasing and gradually becoming comparable to (and in extreme cases, surpassing) C_i. When this happens, the total measured capacitance deviates from what is expected when C_m is calculated using expected bulk value permittivity. This becomes a limiting factor in replacing the standard SiO_2 insulator with a high-κ counterpart as dielectric thickness is now down to nanometer length scales.

In order to investigate any interfacial capacitance on $SrTiO_3$ MIM capacitors, permittivity as a function of film thickness is shown in figure 6.4. Permittivity is extracted using the parallel plate capacitor formula given in equation 2.9. The results in the figure show the well-known phenomenon of reducing permittivity with film thickness. However, figure 6.4 shows the benefit of high-κ insulators as the 90 nm

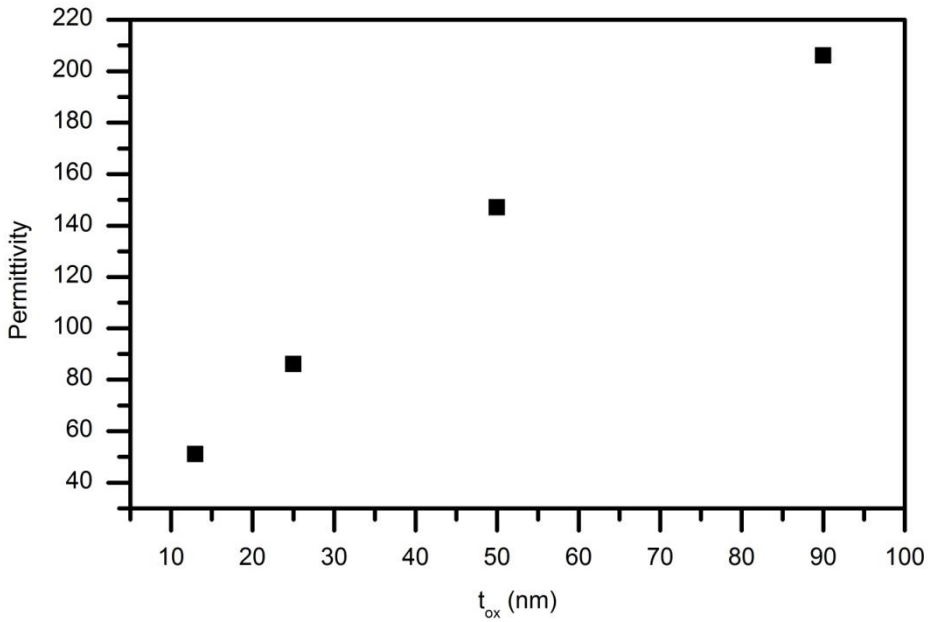

Figure 6.4: Measured permittivity in STO MIM capacitors as a function of dielectric thickness.

thick film displays a peak permittivity of 206. The permittivity in $SrTiO_3$ closely matches that given in ref. 44 for $(Ba,Sr)TiO_3$, in which the series capacitance model in equation 6.6 was applied. The analysis in ref. 44 derived the bulk permittivity using the approximation $t_{ox} >> t_i$, and calculation of the interfacial thickness was not possible due to the inseparability of the intercept term X_i^{-1} ($= t_i/\varepsilon_i$).

The impact of decreasing permittivity with film thickness is known as the dead layer phenomenon, and microscopically, the origin of decreasing permittivity is not well understood. The term dead layer is given to describe the results presented in figures 6.3 and 6.4 in that, the capacitance system can be compared to a series configuration: a high-κ material in series with a low-κ 'dead' layer acting to reduce the total measured permittivity. The results are directly comparable to that discussed for the high-κ and interfacial layer series capacitance system used as the discussion for the EOT model in section 6.3. It is for this reason that equation 6.6 describing the series capacitance model has been used to analyse the dead layer effect in high-κ capacitors in numerous studies [25 - 27, 38 - 46]. Research into this area has resulted in often conflicting explanations as to the origin of the dead layer, some of which include an

extrinsic interfacial layer due to diffusion of Pt [50, 51]; strained interfacial regions [52]; low permittivity space-charge layers [7]; depolarizing fields [8]; electric field penetration into electrodes [53]; and many others [45, 54-58].

Use of equation 6.11 for calculation of the interfacial layer thickness in section 6.3 showed that it was comparable to ellipsometry results given in ref. 48. The interfacial layer causes the intercept term in the *EOT* results in figure 6.2 (a), which leads to a thickness dependent permittivity. Therefore, the previous analysis can be applied to the $SrTiO_3$ MIM structures as figure 6.4 highlights the fact that permittivity is decreasing with film thickness. Based on the structure of the capacitor used in this study, it is possible that the interface capacitance is influenced by two low-κ layers, one at each metal/insulator interface, assuming equal contribution to the overall measured capacitance. This would give $C_i = \varepsilon_o\varepsilon_i/2t_1$, where t_1 and ε_i is the thickness of one low-k region and the permittivity of that region, respectively. However, the proposed model is robust enough that prior knowledge on the number of dead layers in the stack in not necessary and calculates their influence as a sum of the layer(s) combined, C_i. Furthermore, in the subsequent section, TEM images are shown to elucidate the origins of permittivity suppression and to investigate any low-κ 'dead' layer at either interface. In the following analysis, the series capacitance model in equation 6.6, and the new *EOT* model in equation 6.8 is applied to calculate the thickness of a possible interfacial layer, which is otherwise assumed as a dead layer of material.

Analysing figure 6.3 once more, the results show the inverse capacitance of the $SrTiO_3$ films as a function of insulating thickness. Measurements were taken at zero bias where the dead layer effect is most pronounced; this is due to the permittivity being largest at zero bias in tunable films, and hence greater suppression will be apparent. The data lie on a linear best fit and, as an assumption, $t_{ox} >> t_i$, such that the

inverse slope has been previously interpreted as the bulk value permittivity ε_B. The intercept calculates X_i^{-1}, the ratio of interface thickness and permittivity. The derived bulk value permittivity can be overcompensated using equation 6.6 as the assumption $t_{ox} >> t_i$ may not be applicable. The interface capacitance ratio $X_i^{-1} = t_i/\varepsilon_i$ is 0.25 nm and is comparable to other reported values [27]. At this point, only the ratio of t_i/ε_i is known, not t_i and ε_i individually. The linear relationship, and hence constant intercept, implies that the interface capacitance permittivity and thickness is constant and does not depend on the thickness of the film.

The *EOT* data in figure 6.3 is now considered. The results show proportionality between *EOT* and physical thickness of the $SrTiO_3$ capacitors under investigation. The data is close to that shown in figure 6.2 (a) in which an interfacial EOT_i is displayed. If the original equation for *EOT* is used to analyse the results for the $SrTiO_3$ MIM capacitors, the calculated permittivity would be constant in each film thickness from interpretation of the slope. Figure 6.4 shows that the $SrTiO_3$ capacitors have a decreasing permittivity with film thickness, therefore showing that equation 6.4 for *EOT* should not be used for the analysis. This description of *EOT* would also not take into account the visible EOT_i term in figure 6.3, and the value of derived permittivity would be grossly overestimated.

Greater accuracy in the analysis of *EOT* (figure 6.3) is achieved using equation 6.8, which now takes into account EOT_i caused by the dead layer effect in thin films. Furthermore, equation 6.11 allows separation of the interface capacitance parameters t_i and ε_i in order to calculate the perceived interfacial thickness. The y-axis offset gives an interface EOT_i of 0.9 nm taken from figure 6.3. Substituting the interface capacitance ratio X_i^{-1} of 0.25 nm into equation 6.11, along with EOT_i, the interface capacitance thickness and permittivity is 7.5 nm and 30, respectively. As

mentioned previously, the capacitance ratio X_i^{-1} = 0.25 nm is comparable to previous values [27]. The calculated permittivity, ε_i (= 30), is larger than the interfacial layer capacitance permittivity of 10 from section 6.3. This indicates that the origin of the dead layer capacitance is different to the hafnium silicate interfacial layer calculated in the MOS structure. Further comparisons on the interfacial thickness are given at the end of this section.

The inverse slope of EOT in figure 6.3 can also be used to extract a more accurate bulk value permittivity in high-κ material without the assumption $t_{ox} >> t_i$ from equation 6.6. The derived bulk permittivity using equation 6.8 is 450, which would be the assumed permittivity achieved in each high-κ film based solely on equation 6.4. It is shown above that the assumption needed in equation 6.6 is not valid, and an interface thickness of 7.5 nm is comparable to the thinnest film (13 nm) under investigation here. In fact, the bulk value permittivity derived using equation 6.6 is 500, calculating it at 50 greater than using the *EOT* model (ε_B = 450) in equation 6.8.

Figure 6.4 shows evidence of a reducing permittivity with film thickness, and the highest achieved permittivity in the 90 nm film (ε_m = 206) is still grossly under the 450 value calculated using equation 6.8 as the bulk value permittivity. The analysis of the data in figure 6.3 based upon equation 6.8 allows calculation of an interfacial 'dead' layer of thickness 7.5 nm, with low-κ of 30. This interfacial capacitance has the effect of reducing the permittivity in the $SrTiO_3$ MIM capacitors when film thickness is reduced (figure 6.4).

B. Tunability

In addition to ultra-high-κ characteristics, $SrTiO_3$ offers polarization nonlinearity in response to an applied electric field, leading to capacitance tunability. The impact of the interface capacitance on this nonlinearity in $SrTiO_3$ films is now investigated. Figure 6.5 shows the permittivity response to applied electric field for the four thicknesses of $SrTiO_3$ under investigation. The electric field is calculated as V_{app}/t_{ox}, where V_{app} is the applied voltage. The plot also shows the effect the dead layer has on suppressing the maximum permittivity achievable in thin film devices at zero bias. This is clearly illustrated by the fact that increases in the thickness of $SrTiO_3$ results in corresponding increases in the maximum total permittivity. Achievable tunability for a $SrTiO_3$ capacitor can be characterised as shown in equation 6.12 [59]

$$n = \frac{\varepsilon(0) - \varepsilon(E_{app})}{\varepsilon(0)} \tag{6.12}$$

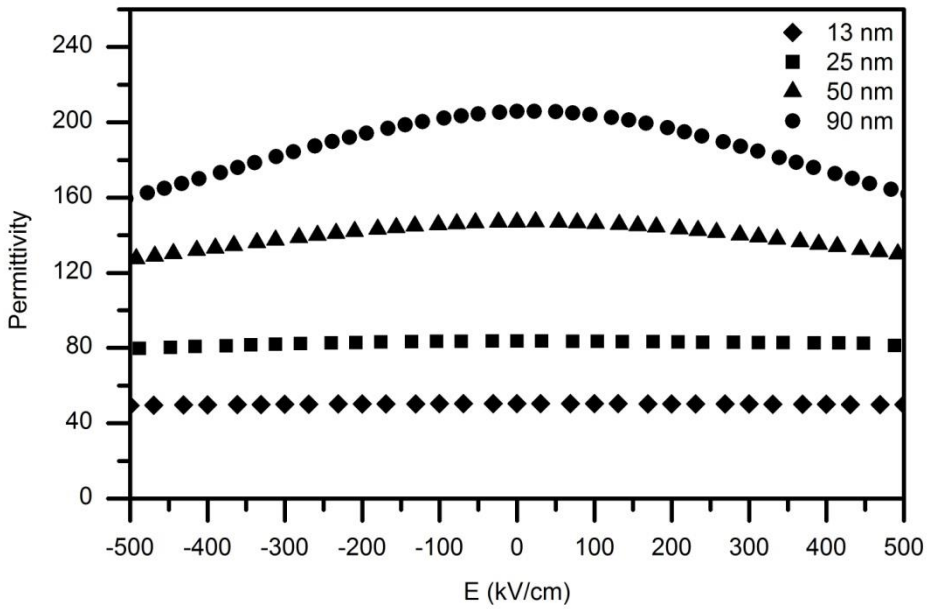

Figure 6.5: Measured permittivity in STO MIM capacitors as a function of applied electric field *E* and thickness of $SrTiO_3$.

where $\varepsilon(0)$ is the permittivity at zero electric field and $\varepsilon(E_{app})$ is the permittivity at an applied electric field, E_{app}. Table 1 shows achievable tunabilities at an electric field of 500 kV/cm, which is inside the breakdown fields of the films. From table 6.1 and figure 6.5, it is clear that, as well as reducing the maximum permittivity, a decreasing film thickness also affects the highest achievable tunability. Fuchs *et al.* [60] discusses this effect in terms of temperature on epitaxially grown $SrTiO_3$, and states that a reduction in the zero bias permittivity also decreases the tunability of the film. $SrTiO_3$ has a temperature dependent permittivity, which decreases with increasing temperature after entering its paraelectric phase at the phase transition temperature T_c; hence, the tunability decreases along with permittivity with increasing temperature. However, for the results reported in figure 6.5, all measurements were taken at room temperature, which is far beyond the phase transition temperature (T_c = 89 K [60]). Permittivity, and hence tunability, has little dependence on temperature at temperatures much greater than T_c. Therefore, the change in permittivity shown in figure 6.5 is more likely the result of interface effects on the overall characterisation of the $SrTiO_3$ thin films.

The series capacitance model can also be used to obtain the actual tunability if the interface capacitance influence is removed. Rearranging equation 6.6 by dividing out the area and taking $C_m = \varepsilon_m / t_{ox}$, the permittivity of the bulk $SrTiO_3$ that achieves a maximum value of 450 from equation 6.8 at zero bias is shown in equation 6.13

t_{ox} (nm)	ε_m	*EOT* (nm)	*n* (%)
13	**51**	**1**	**1**
25	**86**	**1.1**	**9**
50	**147**	**1.3**	**13.5**
90	**206**	**1.7**	**21**

Table 6.1: Average permittivity, measured EOT and tunability across the 4 thicknesses of STO.

$$\varepsilon_{STO} = \frac{\varepsilon_m \varepsilon_i (t_{ox} - t_i)}{t_{ox}\varepsilon_i - t_i \varepsilon_m} \tag{6.13}$$

where ε_m is the permittivity shown in figure 6.5 and ε_{STO} is the achieved permittivity in the bulk $SrTiO_3$ layer. All remaining variables were defined previously.

Dividing the total electric field into its individual components across C_{STO} and C_i, where C_i accounts for both upper and lower interface capacitances, the electric field across the bulk film is shown in equation 6.14

$$E_{STO} = E_{app} \frac{t_{ox}}{\left(\frac{\varepsilon_{STO} t_i}{\varepsilon_i}\right) + (t_{ox} - t_i)} \tag{6.14}$$

where E_{STO} is the field across the bulk layer. Using the interface parameters extracted from equation 6.8, which was t_i = 7.5 nm, ε_i = 30, the actual bulk permittivity can be plotted against bulk electric field using equation 6.13 and 6.14. Figure 6.6 shows the results of bulk permittivity as a function of the bulk electric field. For the 90 nm film, it is clearly observed that the permittivity reaches the maximum 450, and full tunable characteristic curves are now shown, having removed the influence of the interface capacitance. Achieved tunability, *n*, using equation 6.12 for the 90 nm film is now 39%. This approximately doubles the measured tunability for the 90 nm film (table 6.1), and approaches that necessary for tunable capacitor applications (> 40 %). For comparison between bulk and measured results, only the 90 nm curve is shown as similar results were observed across all thicknesses.

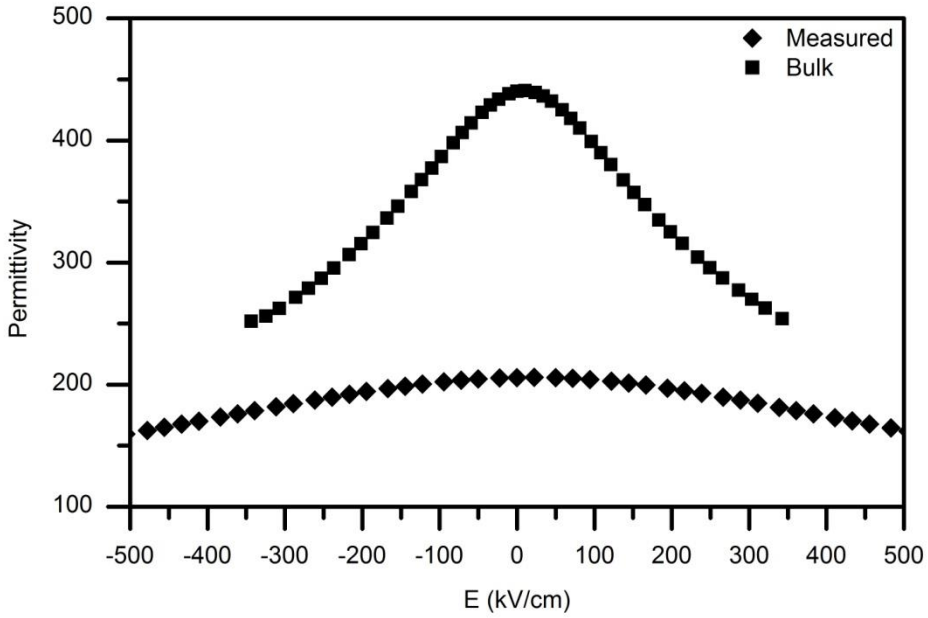

Figure 6.6: Bulk and measured permittivity vs. electric field in the 90 nm STO film, showing the influence of the interfacial layer capacitances.

The nonlinearity of ferroelectric material can be described using LD phenomenological theory, and is discussed in greater detail in chapter 2. Expanding the free energy in terms of an order parameter, in this case polarization (*P*), tunability is related to three material coefficients described below. Equation 2.14 is repeated in equation 6.15 for clarity, where LD theory is taken as a Taylor series expansion

$$\Delta G = \frac{1}{2}\alpha_1 P^2 + \frac{1}{4}\alpha_{11} P^4 + \frac{1}{6}\alpha_{111} P^6 - E_{app} P \qquad (6.15)$$

α_1, α_{11}, α_{111}, are the insulating stiffness coefficients that characterise the permittivity dependence on electric field, G is the Gibbs free energy, which in this case is the energy density stored in the electric field across the capacitor and $E_{app}P$ is the externally applied electrostatic energy term. Shown previously in chapter 2, the material coefficients provide means of describing the characteristics of the perovskite under specific conditions. In addition, they were used to design the negative

capacitance bilayers in chapter 4. In equation 6.15, they relate the energy density of the capacitor to the applied electric field, and hence tunable properties, and will now be discussed in terms of the dielectric thickness dependence.

The applied electric field is always normal to the substrate, and an assumption made that the effect of fringing fields is minimal. Consequently, P is the average polarization from the in-plane polarizations (P_1, P_2) and out-of-plane polarization (P_3) due to the polycrystalline nature of the grown films. Taking the derivative of the free energy in equation 6.15 with respect to P to find the stable operating point where $\delta G/\delta P=0$, the electric field across the $SrTiO_3$ film is expressed in equation 6.16.

$$\frac{\partial G}{\partial P} = E_{app} = \alpha_1 P + \alpha_{11} P^3 \qquad (6.16)$$

In this form, the 6th order term from equation 6.15 has been neglected as it introduces no new physics into the analysis [61]. Inclusion of higher order coefficients only becomes relevant when characterising ferroelectric films of the first-order transition type where α_{11} is negative. Equation 6.16 describes electric field as a function of polarization, which can be inverted to make polarization the subject. The polarization nonlinearity and its dependence on electric field can then be simulated. For linear dielectrics, α_{11} is zero and $\alpha_1 = 1/\varepsilon$; as a result, the tunability of the insulator is dominated by the coefficient α_{11}, while α_1 describes the zero bias permittivity. Immediately it is seen that the interface capacitance has implications on the dielectric stiffness coefficient α_1. Equation 6.16 can be solved as a third order polynomial with E_{app} being cycled through ±500 kV/cm. Solutions to P as E_{app} is cycled are shown in figure 6.7, with bulk value stiffness coefficients for $SrTiO_3$ taken from ref. 62 for the simulated curve. Capacitance tunability can be visualised in figure 6.7 as the slope is not constant, and capacitance is related to polarization using $C \propto \delta P/\delta E$. Figure 6.7

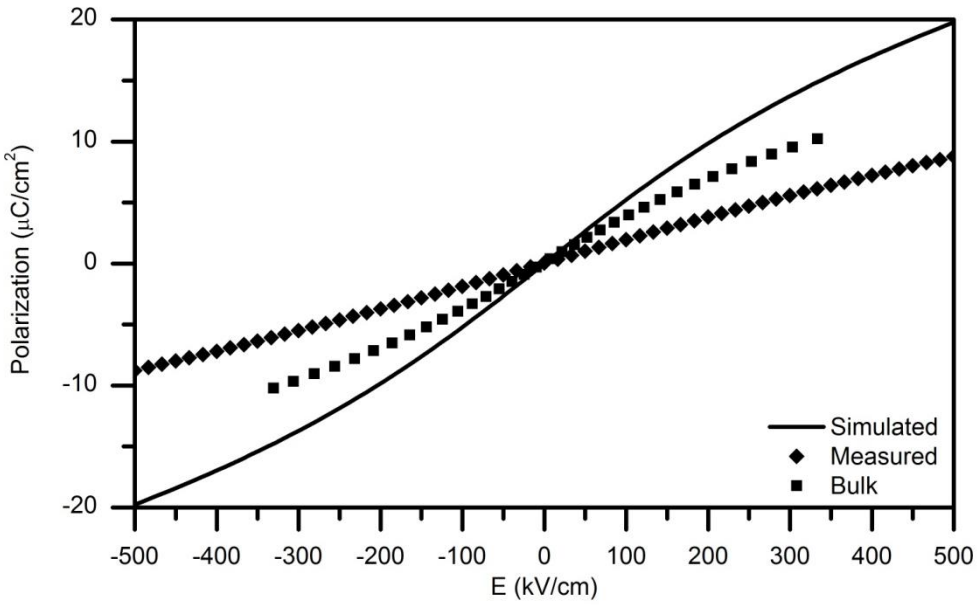

Figure 6.7: Simulated polarization versus applied electric field using bulk values of material coefficients (solid line). Diamond curve is integrated from measured CV data in figure 6.5 for 90 nm film thickness. Square curve is reconstructed polarization integrated from the bulk permittivity shown in figure 6.6.

also shows the reconstructed polarization dependence on applied electric field for the measured (diamond) and bulk (square) curves in the 90 nm film, obtained by integrating the CV characteristics shown in figure 6.6. Only the 90 nm curves are shown for clarity as remaining thicknesses showed similar results.

From figure 6.7, it is observed that the measured (diamond) polarization depends on the electric field approximately linearly. Also shown is the bulk (square) polarization dependence on electric field. This is integrated from the bulk capacitance trend shown in figure 6.6, which was previously shown by removing the influence of t_i and ε_i using equation 6.13 and 6.14. It is apparent that removing the influence of the interface capacitance increases the achievable tunability of the $SrTiO_3$ film, as well as permittivity, which is related to the slope around zero electric field. When the applied electric field increases, the nonlinear α_{11} term begins to dominate.

Attention is now turned to investigating the influence of insulating thickness on the material coefficients defined above. The insulating stiffness coefficients are extracted using best fits to the measured curves (diamond) in figure 6.7 and equation 6.16. Permittivity suppression as film thickness is reduced translates into $\alpha_1 \propto t^{-1}$ ($\alpha_1 = \varepsilon_o\varepsilon_r(o)^{-1}$ where $\varepsilon_r(o)$ is the zero bias permittivity) [59] due to the linear decrease in permittivity with decreasing film thickness (figure 6.8). However, the nonlinear term also displays the same relationship, $\alpha_{11} \propto t^{-1}$, which is shown in figure 6.9. Also shown in figure 6.8 is the bulk value for α_1 using $\varepsilon_{STO} = 450$, and in figure 6.9 the bulk value of α_{11} taken from ref. 62. Figure 6.8 shows an increase in the linear coefficient with decreasing film thickness, and hence decreasing permittivity, resulting in a divergence from the bulk value shown, which is thickness independent. Figure 6.9 also shows the same trend, and the nonlinear α_{11} coefficient increases over the bulk value with decreasing film thickness. When considering equation 6.16, it is desirable to have a large α_{11} coefficient to dominate over the linear part of the equation, and in turn achieve a greater tunability. It is shown in figure 6.5 that this is not the case, and tunability is actually decreasing with film thickness, regardless of the enhancement in the nonlinear α_{11} coefficient. Best fits were also performed on the bulk curve (figure 6.7, square). This resulted in the extracted coefficients approaching expected bulk values taken from ref. 62 (α_1=2.5x10^8, α_{11}=6.9x10^9 for this work, compared to α_1=1.87x10^8, α_{11}=1.7x10^9 for ref. 62).

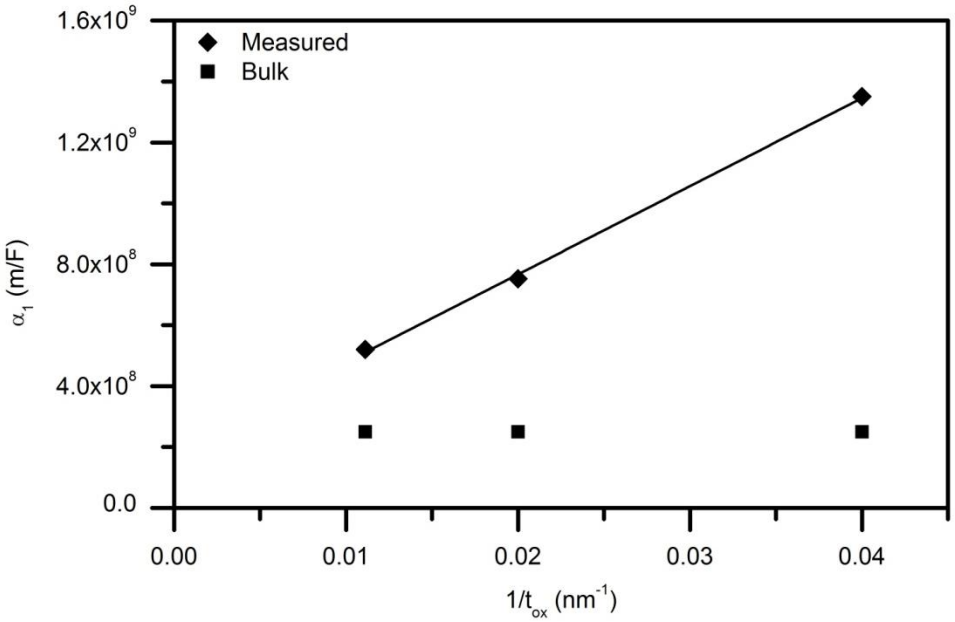

Figure 6.8: Linear dielectric stiffness coefficient extracted using a best fit of equation 6.16 in figure 6.7 of the measured polarization (diamond) and expected bulk value of linear coefficient using $\alpha=1/\varepsilon$ (square).

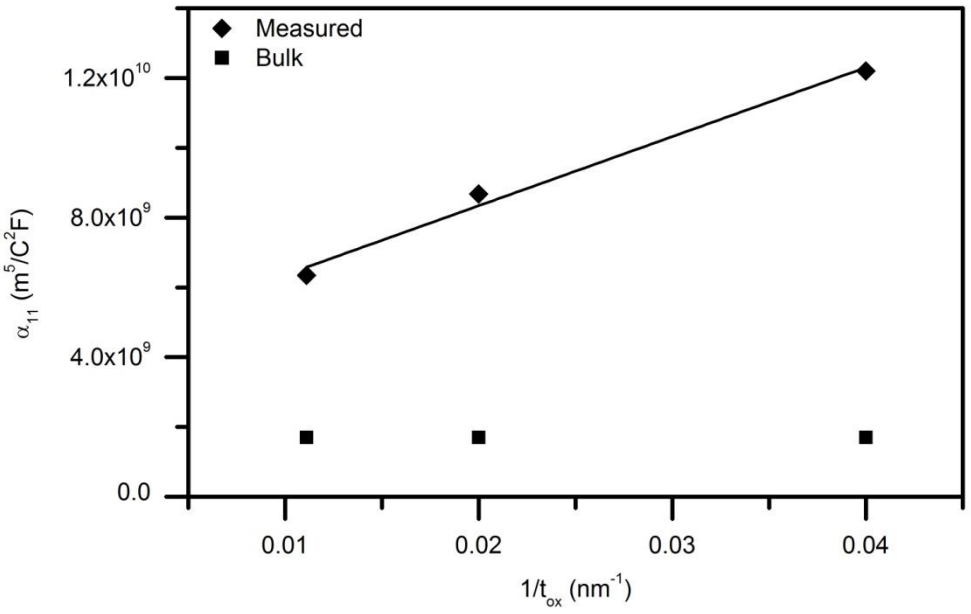

Figure 6.9: Nonlinear dielectric stiffness coefficient extracted using a best fit of equation 6.16 in figure 6.7 of the measured polarization (diamond) and expected bulk value of nonlinear coefficient taken from ref. 62 (square).

Under ideal circumstances, α_1 and α_{11} are constant with film thickness; the bulk permittivity response of the film with electric field, E_B, should show no thickness dependence. However, inclusion of the series capacitor in figure 6.5 shows a thickness dependent permittivity response with E_{app}. Due to the constant interface capacitance, as described in the inverse capacitance model in figure 6.3, a decrease to the total film thickness will reduce the thickness of the bulk of the film, and E_{app} will differ from E_B. The model then requires an increasing E_{app} to reach a given polarization due to the increasing voltage drop across the interface capacitance.

This voltage partition problem can be solved analytically [27]. With appropriate boundary conditions for two dielectrics in contact, $P_{app} = P_i = P_B$, and assuming no free charge ($\chi = \kappa$), the electric field across the bulk and interfacial capacitance can be represented in LD formulation in equation 6.17 and 6.18.

$$E_B = \frac{V_B}{t_B} = \alpha_1^B P + \alpha_{11}^B P^3 \tag{6.17}$$

$$E_i = \frac{V_i}{t_i} = \alpha_1^i P + \alpha_{11}^i P^3 \tag{6.18}$$

The stiffness coefficients are split into bulk, α^B and interfacial, α^i, components representing the linear (α_1) and nonlinear (α_{11}) effects. Adhering to Kirchhoff's voltage law such that, in equation 6.19, the applied voltage is the sum of the two voltage drops across the capacitor.

$$V_{app} = V_B + V_i = t_B(\alpha_1^B P + \alpha_{11}^B P^3) + t_i(\alpha_1^i P + \alpha_{11}^i P^3) \tag{6.19}$$

Using the relationship $t_B = t_{ox} - t_i$, equation 6.19 is rearranged for the series voltage partition across the bulk and dead layer capacitance using LD theory, shown in equation 6.20.

$$E_{app} = \left[\alpha_1^B + \frac{t_i}{t_{ox}}(\alpha_1^i - \alpha_1^B)\right] P + \left[\alpha_{11}^B + \frac{t_i}{t_{ox}}(\alpha_{11}^i - \alpha_{11}^B)\right] P^3 \qquad (6.20)$$

Equation 6.20 shows the effective linear stiffness coefficient α_1 is increased proportional to t_{ox}^{-1} and also due to $\alpha_1^i > \alpha_1^B$ as the interfacial capacitance has a smaller permittivity. There is also a linear correlation between the nonlinear stiffness coefficient α_{11} and t_{ox}^{-1}, which is seen in figure 6.9. This is in contrast to the results in ref. 26 in which only α_1 shows the linear proportionality with t_{ox}^{-1}. For the nonlinear term to increase, the interfacial and bulk coefficients must not be equal, such that $\alpha_{11}^i > \alpha_{11}^B$. For the nonlinear α_{11} coefficients to differ for the interface and bulk, a compositional gradient may exist due to small amounts of Ti diffusion from the adhesion layer through Pt grain boundaries [68]. The diffusion would result in a Ti-rich interface region compared to the bulk sample which has previously been seen in XPS depth profiling (not shown).

It is clear from the results presented so far that the dead layer phenomenon is observable electrically. However, there are some discrepancies as to the origin of this layer, as discussed previously. The following section will discuss the pertinent question in whether a dead region of material is physically observable at the interface of the $SrTiO_3$ and Pt electrode.

6.4.2 Material characteristics

In order to assess the material quality of the $SrTiO_3$ capacitors, the crystallinity of the films is investigated. The XRD spectrum of the 90 nm film is shown in figure 6.10. The results indicate a strong (110) peak, attributed to the $SrTiO_3$ perovskite phase, and presents evidence for the crystalline nature of the film. Remaining peaks are attributed to (111) and (200) Pt orientations. $SrTiO_3$ and Pt thin film heterostructures suffer from peak overlapping in characterisation using XRD. It is therefore likely that $SrTiO_3$ peaks are hidden under the Pt peaks due to the high temperature of growth (700 °C). Further analysis of XRD spectra for $SrTiO_3$ films is given in chapter 5.

It is shown that film thickness plays an important role in the characteristics of the devices. The observed results show that a decreasing film thickness is detrimental not only to the maximum permittivity achievable, but also the tunability of the material. The dead layer interfacial capacitance, thought to be the cause of the electrical

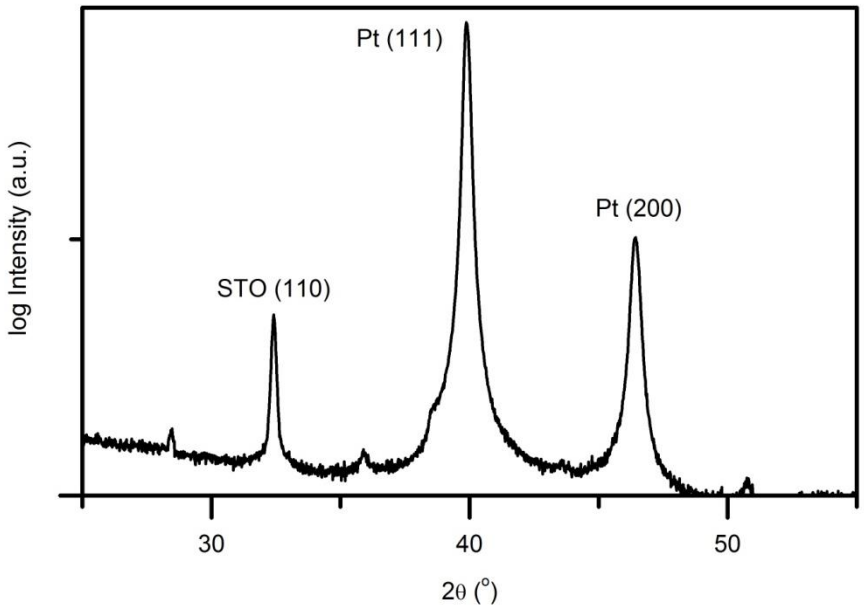

Figure 6.10: XRD spectrum of the 90 nm STO film. Peaks shown are attributed to the (110) perovskite phase for STO and (111), (200) of the Pt layer.

dependence on thickness, is calculated to have a total thickness of 7.5 nm, assumed to be approximately 4 nm at each interface due to the symmetric structure of the MIM capacitors used in this study.

In order to investigate the origins of the interface capacitance, TEM imaging is conducted. Figure 6.11 shows images of the 90 nm structure. The dark contrasting areas in figure 6.11 (a) were analysed at different tilts, and shifted at different tilt angles. Therefore, they are the facets of the individual growth columns, commonly observed for samples deposited using PLD, and not from diffusing Pt. Figure 6.11 (b) shows the bottom Pt/$SrTiO_3$ interface, which is smooth. No evidence of contrasting regions or distinct secondary phases, such as TiO_x due to Ti out-diffusion through the Pt bottom electrode, is shown. In figure 6.11 (c) the top $SrTiO_3$/Pt interface is somewhat rougher due to the upward growth and coalescence of the individual $SrTiO_3$ columns. The images in figure 6.11 show no indication of 4 nm thick interfacial regions, and hence the reduction in permittivity and tunability cannot be attributed to a physical observable material in series with a bulk $SrTiO_3$ film. The interfacial capacitances in the series capacitance model are, however, electrically active, and describe the apparent size effects on the electrical characteristics in thin-film high-κ capacitors as described in

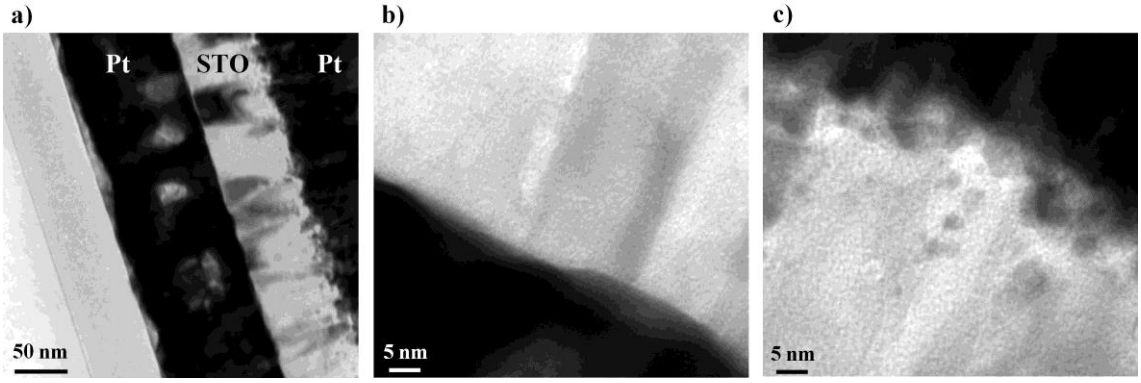

Figure 6.11: TEM a) 90 nm MIM capacitor. From the left of the image: Si/SiO_2/Ti/Pt/STO/Pt. Dark contrasts are the facets of the individual growth columns of $SrTiO_3$. b) Bottom Pt/ STO interface. c) Top STO/Pt interface.

section 6.4.1. Intrinsic effects, such as incorrect electrode screening and depolarizing fields [63, 64], are likely causes for the dead layer effect, which would not be visible in TEM images. Extrinsic factors, such as interfaces that are not atomically smooth and defect states should act to enhance the effect [63].

Figure 6.11 (c) shows evidence of an imperfect metal/insulator interface due to the polycrystalline film imposed by the substrate and growth method used. This can create a finite separation between the free charge in the electrode and polarization bound charge in the insulator, leading to a contribution to the interface capacitance. Techniques using atomic layer deposition to achieve atomically smooth metal/insulator interfaces should act towards minimising the reduction in permittivity and reduced tunability, which is evident in this chapter.

In order to validate equation 6.8, data from ref. 24 for $Ba_xSr_{1-x}TiO_3$ (BST, x = 0.7) and $SrTiO_3$ films are taken and shown in figure 6.12. Figure 6.12 shows the extracted interface thickness, t_i, calculated using equation 6.8 and the interface EOT_i for both $SrTiO_3$ and $Ba_{0.7}Sr_{0.3}TiO_3$ films grown using metal organic chemical vapour deposition (MOCVD) on platinized silicon wafers. The correlation with EOT_i and t_i is shown for both films as a larger EOT_i gives a greater interface capacitance thickness, which would lead to further decreasing permittivity with film thickness. Also shown in figure 6.12 is the elemental composition, taken as a Group (Gr) II/Ti ratio. It is shown that film composition is an important factor on the interface capacitance, and can explain why figure 6.12 does not show a linear relationship between t_i and EOT_i. The stoichiometric $Ba_{0.7}Sr_{0.3}TiO_3$ film (Gr II/Ti = 0.97-1.03) shows the greatest interface capacitance thickness, with an increasing or decreasing ratio leading to a decrease in t_i. Comparing the interface capacitance thickness of the MOCVD $SrTiO_3$ film and the PLD grown $SrTiO_3$ film studied here, t_i = 0.7 nm for the MOCVD film and t_i = 7.5 nm

for the PLD film. The large increase of the interfacial thickness may be attributed to the rougher top interface of the PLD film (figure 6.11 (c)), as any charge separation between the insulator and electrode can lead to additional capacitive terms. The PLD process is a physical deposition method (PVD), which will result in films with rougher interfaces due to the inherent deposition method. In contrast, the $SrTiO_3$ film grown using MOCVD, which showed a much smaller interface capacitance thickness, will have smoother interfaces due to the conformal deposition. It is apparent that atomically smooth interfaces and increases in Gr II or Ti ions leading to small deviations in film composition, can act to lower the interface capacitance thickness.

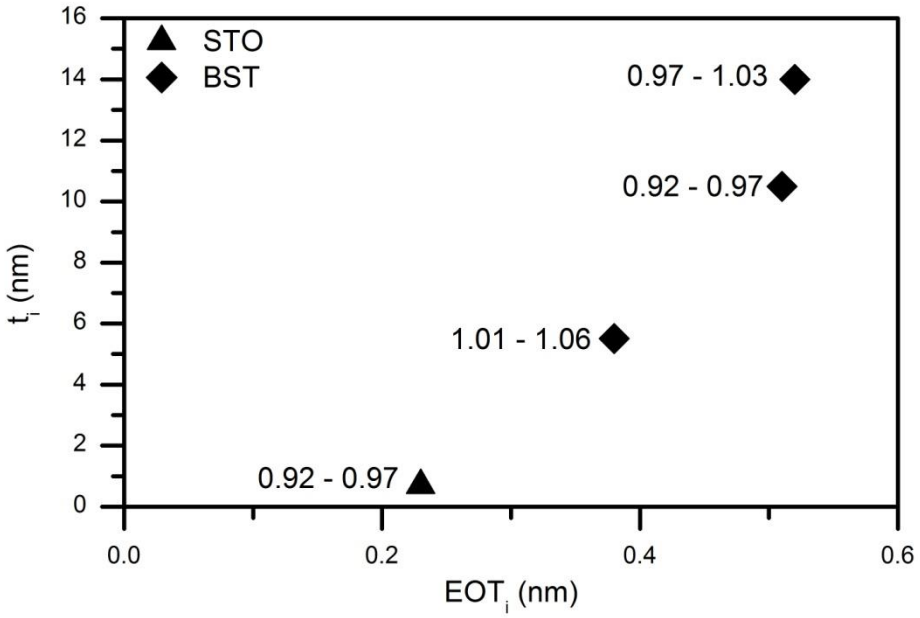

Figure 6.12: Extracted interface thickness as a function of interface EOT_i using equation 6.7 with data taken from ref. 24. Diamonds are $Ba_xSr_{1-x}TiO_3$, x=0.7 and triangle indicates STO. Numbers indicate elemental composition as Gr II/Ti ratio.

6.5 Mixed Phase $BaTiO_3$ MIM Capacitors

6.5.1 Results

A. Electrical

Figure 6.13 shows the CV characteristics for a MIM capacitor with a BTO insulating layer 160 nm thick performed at two different temperatures, 300 K and 420 K. Measurements performed at both temperatures should exhibit ferroelectric and paraelectric characteristics, respectively, since the phase transition temperature T_c = 393 °K. At 300 K, measurements show two distinct curves, with the applied forward and reverse bias direction shown by the arrows. The curves indicate a two peak ("butterfly") trend in the measurement, and this is attributed to the polarization switching in a ferroelectric, i.e. the material displays directionally dependent characteristics with applied bias through its hysteretic polarization ($P \neq 0$ at $V = 0$). These results are indicative of ferroelectricity in BTO measured at 300 K.

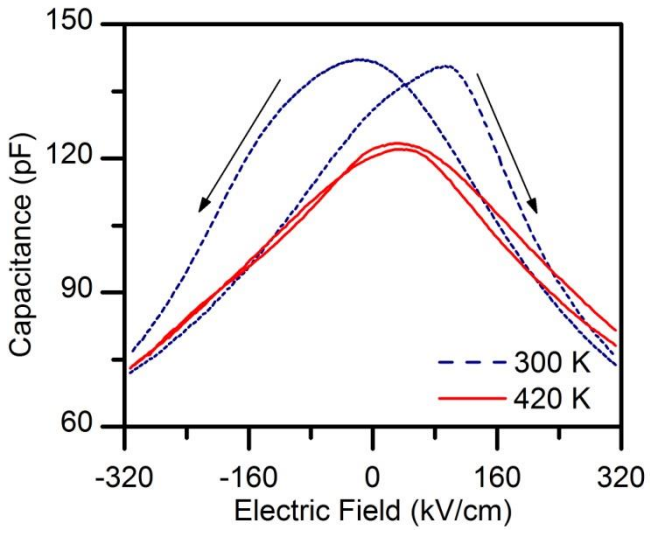

Figure 6.13: Capacitance-voltage measured on the Pt/$BaTiO_3$ (160 nm)/Pt capacitor at 300 K and 420 K. Electric field is taken as V/t_{ox}, where t_{ox} is the thickness of the $BaTiO_3$ film.

The 160 nm thick BTO capacitor was measured at 420 K in order to induce a phase transition. The CV characteristics shift as the measurement temperature increases past the bulk value of T_c (figure 6.13). The intermediate measurements (not shown) between temperatures 300 K and 420 K evolve gradually with increasing temperature towards the characteristics seen at 420 K. The double capacitance peaks observed at 300 K converge to a single peak and the butterfly trend is lost. The high temperature measurement is indicative that a phase transition has taken place in the BTO film such that each unit cell is now cubic (figure 2.5 (a)) and no longer retains any polarization.

Permittivity is determined for the 160 nm thick BTO capacitor using the parallel-plate capacitor relationship of the MIM structure. The permittivity response in a perovskite may show evidence of a phase transition in accordance with equation 6.1. When the ferroelectric transitions into the paraelectric phase (figure 2.5 (b) → (a)), the permittivity will increase, reaching a maximum at the phase transition temperature, 393 K [18]. From the capacitance measurements shown in figure 6.13, it is expected that a peak permittivity will be seen at approximately 400 K. This would suggest a phase transition in the 160 nm thick BTO film.

Figure 6.14 shows the extracted permittivity variation with temperature from capacitance measurements using the parallel-plate relationship. Increasing the temperature towards 400 K, there is an absence of any peak in the permittivity. In contrast, measurements on freestanding BTO showed permittivity increasing sharply from approximately 380 K, and reaching a peak Curie anomaly at 400 K, demonstrating its ferroelectric nature [19]. The trend shown here is indicating a paraelectric characteristic where the permittivity is decreasing with increasing temperature, as described by equation 6.1. The result suggests that the phase transition has shifted to a lower temperature, whereby the paraelectric phase is induced at $T < T_c = 393$ K. The

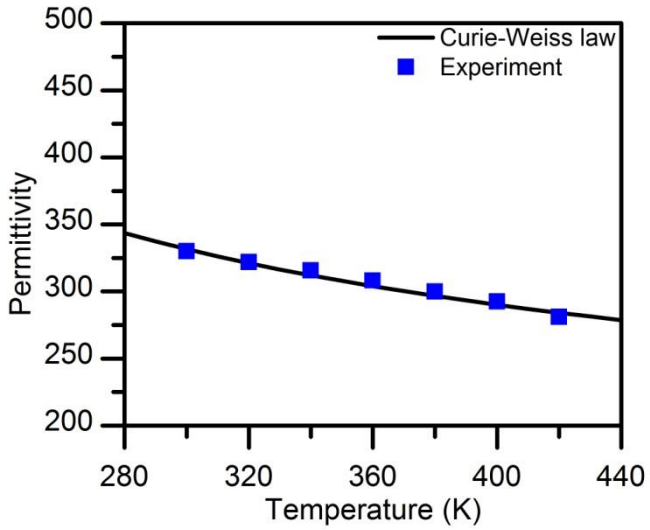

Figure 6.14: Permittivity measured on the Pt/$BaTiO_3$ (160 nm)/Pt capacitor as a function of increasing temperature. Permittivity is extracted from the parallel-plate capacitor relationship. The Curie-Weiss law in equation 6.1 is fitted to the experimental data.

Curie-Weiss law in equation 6.1 is fitted to the experimental data in figure 6.14 in order to confirm the paraelectric nature of the BTO film. The extracted Curie constant is equal to 0.5 x 10^5, and is comparable with values of 10^5 calculated in previous studies on polycrystalline BTO from A.C. measurements [65]. However, the permittivity analysis contradicts the CV measurements in figure 6.13 which shows a convergence of the peak capacitance points when the temperature is increased to 420 K.

The electrical results for the 160 nm thick BTO capacitor disagree in terms of the properties displayed: the butterfly CV trend in figure 6.13 shows evidence for the tetragonal phase, while the permittivity response with temperature in figure 6.14 can be fitted to the Curie-Weiss law in the paraelectric phase. The results lead to a conclusion that the film is in a mixed phase condition. The tetragonal part is responsible for the butterfly CV measurements, while the cubic phase dictates the permittivity response with temperature. The cubic phase is thought to be the dominating contribution due to the overriding paraelectric response to permittivity when the temperature increases.

High concentrations of the cubic phase will manifest as minimal remnant polarization, which is apparent in a number of studies [28]. Minimal remnant polarization in the BTO capacitors is investigated with large-signal hysteresis measurements in section 6.5.2.

B. Material

In order to investigate the material characteristics and mixed phase properties of the BTO film, EFM, XRD and Raman spectra were taken at room temperature. Before the EFM images were taken, in order to polarize the BTO, -5 V was applied to the bottom Pt electrode and a 4 μm x 4 μm area was scanned in contact mode. The EFM images were taken across a 6 μm x 6 μm area which covers the previously polarized area. The alternating modulation applied to the tip had an amplitude of 0.8 V and a frequency of 20 kHz.

XRD spectra (figure 6.15) of the 160 nm thick film is performed to investigate the crystallinity and to determine growth orientation. Results from the 280 and 380 nm thick BTO films are also shown and discussed in section 6.5.2. From the results, it can be concluded that the BTO film is polycrystalline with random orientation, as evident from the numerous diffraction peaks in the spectrum. Therefore, the BTO film consists of randomly oriented grains with intersecting grain boundaries. Peak splitting in XRD spectra may show evidence for the tetragonal phase in a perovskite crystal. The data presented in figure 6.15 does not signify any peak splitting; however, this is likely to be due to the resolution of the XRD measurement and as such the results do not factor into the conclusion about the phase of the BTO.

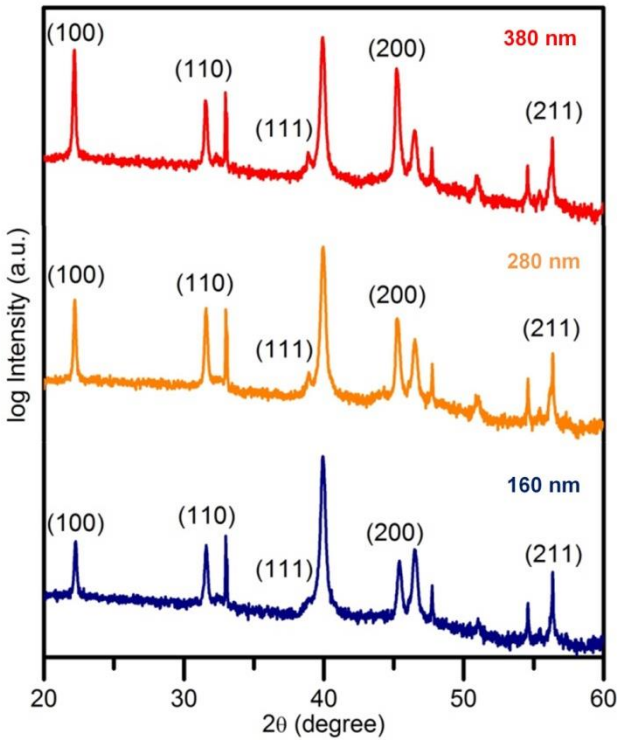

Figure 6.15: XRD spectra of the BTO films with varying film thickness. Orientations of BTO are labelled with remaining contributions originating from Si or Pt.

Further understanding of the structure of the BTO film can be gained using the TEM imaging in figure 6.16 for the 160 nm thick sample. The image in figure 6.16 (a) shows the full BTO film thickness situated between the dark contrasting Pt electrodes. It is apparent that the film has grown in a columnar structure, originating from the initial bottom Pt electrode. Each column spans the full film thickness and they coalesce towards the top Pt electrode; therefore, each column height is the full thickness of the given film. From 6.16 (a), each column width is estimated at 30 nm. Also shown in 6.16 (b) are high resolution TEM images of the individual BTO columns. The results show that, taking into account the influence of Moiré fringes, each column is a uniform grain of single orientation, leading to grain boundaries at the column edges.

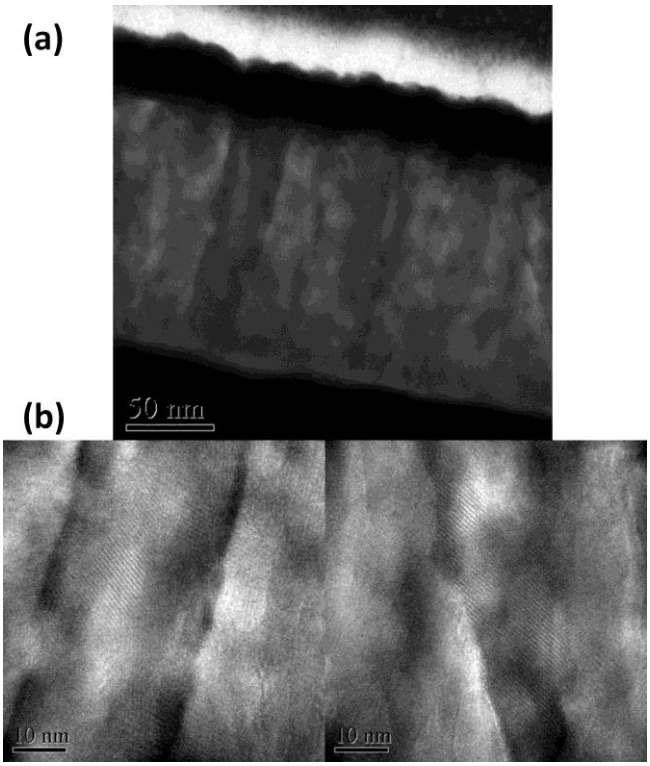

Figure 6.16: TEM imagine of the 160 nm thick BTO sample. (a) Image shows the cross section of the full film thickness situated between the dark contrasting Pt electrodes. (b) Images show high resolution TEM highlighting individual columns.

The EFM technique is applied to study any remnant polarization and domain structure in the BTO film. Figure 6.17 shows the EFM scan of 6 μm x 6 μm area on the surface of the 160 nm thick BTO film. The polarized 4 μm x 4 μm region appears as a bright square, in sharp contrast with the outer un-polarized area. Colour variation in the polarized region as shown in Figure 6.17 also indicates that the film is non-uniformly polarized. The result is further highlighted by a magnified scan of 1 μm x 1 μm on the polarised area, clearly showing highly contrasted regions. The dark regions indicate non-polarizable domains whereas white regions show the polarized domains. The cubic phase in BTO does not retain the spontaneous polarization upon the removal of an external field whereas in the ferroelectric tetragonal phase it does. The co-existence of

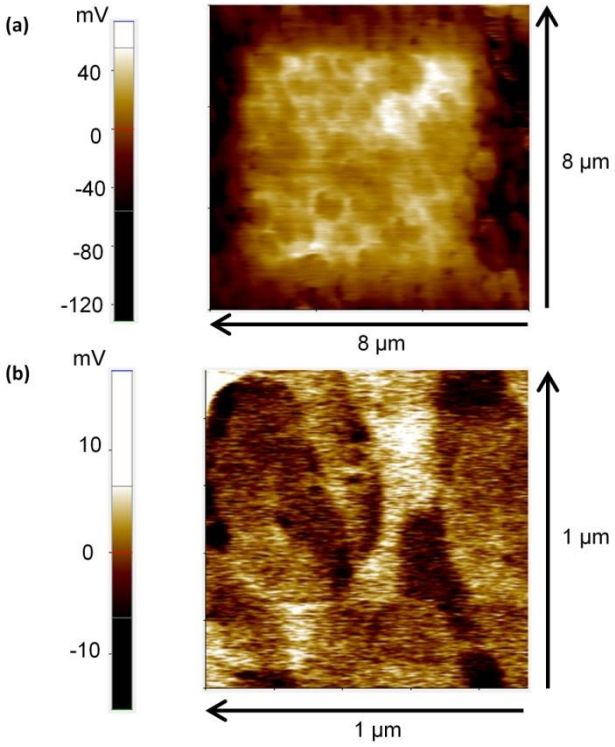

Figure 6.17: EFM image of polycrystalline BTO at 160 nm thick (a). BTO is non-uniformly polarized. High resolution scan shows that it is a mixture of polarizable and non-polarizable domains (b).

polarizable and non-polarizable domains confirms the presence of both cubic phase and tetragonal phase in polycrystalline BTO, in adherence with the previous results.

Raman spectra of thin film $BaTiO_3$ from 100 cm^{-1} to 800 cm^{-1} at room temperature is given in figure 6.18. Raman active phonons for tetragonal $BaTiO_3$ are represented by $3A_1 + B_1 + 4E$ [66]. Long-range electrostatic forces cause a splitting of the transverse and longitudinal phonons. These Raman active bands are situated around 250 cm^{-1} (A_1(2TO)), 306 cm^{-1} (E(3TO) + E(2LO) + B_1), 520 cm^{-1} (E(4TO) + A_1(3TO)) and 720 cm^{-1} (E(4TO) + A_1(3LO)). A sharp peak at approximately 300 cm^{-1} is a characteristic of tetragonal $BaTiO_3$. The 300 cm^{-1} peak disappears as the phase changes from tetragonal to cubic [20]. Data for the 160 nm thick $BaTiO_3$ film presented here

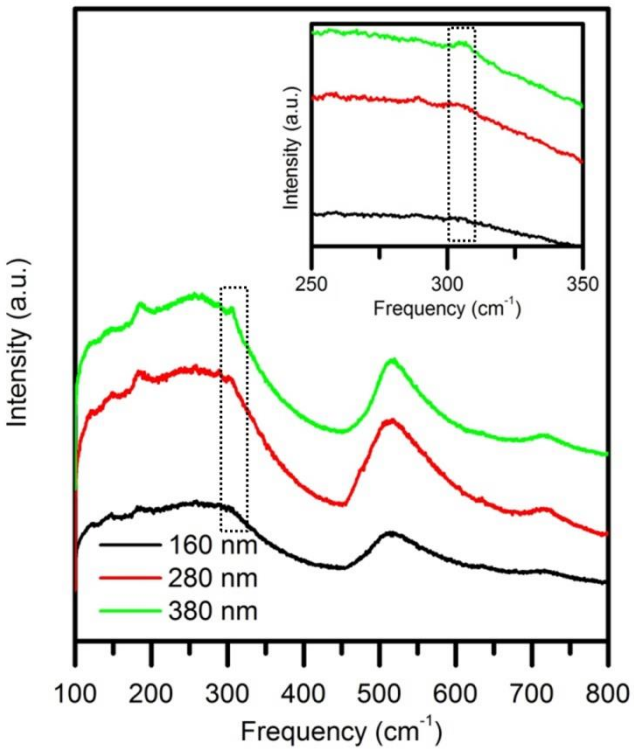

Figure 6.18: Raman spectra of polycrystalline BTO as a function of increasing thickness. Dashed region shows BTO has a reduced peak intensity around 300 cm^{-1} indicating presence of both cubic and tetragonal phases. Inset highlights that the peak intensity at 300 cm^{-1} increases with increasing film thickness.

shows a reduced intensity peak around 300 cm^{-1} compared to a bulk ceramic. The result suggests that the 160 nm thick film largely consists of the cubic phase due to the reduced peak intensity at 300 cm^{-1}. Analysis of the Raman spectra of all $BaTiO_3$ thicknesses studied here is given in section 6.5.2.

6.5.2 Discussion

Based on the previous results, thin film BTO is observed to be in a mixed phase condition comprising cubic and tetragonal parts. The butterfly CV trend and bright contrasting regions in EFM confirms the existence of the tetragonal phase. The permittivity response with temperature, dark contrasts in EFM and lack of any Raman peak at 300 cm^{-1} shows evidence for the cubic phase. The studies discussed were for the

160 nm film thickness, which showed polycrystalline, randomly oriented grains in a columnar structure. The discussion will now turn to the thickness dependence of the films and 280 nm and 380 nm thick films will be compared with the results of the 160 nm thick film.

The remaining XRD spectra for the 280 nm and 380 nm thick films are presented in figure 6.15. The results are unchanged to those described previously for the 160 nm thick film. Each film thickness shows a polycrystalline and randomly oriented grain structure. Therefore, an increasing film thickness does not impact the texture or crystallinity of the BTO films.

The Raman spectra for the 280 nm and 380 nm thick films are studied, particularly the sharp peak at 300 cm^{-1} indicative of the tetragonal phase. Figure 6.18 shows the evolution of each spectrum for the Raman scattering bands 250, 520 and 720 cm^{-1} explained previously. There is also an indication of a sharp peak at 300 cm^{-1}. The inset reflects the magnified region of the peak of interest at 300 cm^{-1}. As the film thickness is increased, the 300 cm^{-1} peak is seen to increase in intensity. The intensity of the Raman peaks may be affected by different crystallographic orientations. However, the XRD spectra in figure 6.15 show that each film is polycrystalline with no change in the crystallographic orientations. Therefore, the reduction in the intensity of the Raman peak at 300 cm^{-1} with film thickness is not due to different crystallographic orientations in the films. This corresponding reduction of peak intensity suggests that a phase transition occurs towards the cubic phase as the film thickness is reduced. Consequently, an increasing film thickness should lead to an increase in remnant polarization.

Figure 6.19 shows a large-signal hysteresis measurement on the 380 nm thick sample. The inset in figure 6.19 also shows the remnant polarization measured in each sample to corroborate the thickness dependent Raman results discussed above. From the results a clear thickness dependence is evident on the remnant polarization, which increases with BTO film thickness, leading to a confirmation of the Raman results. Therefore, it is initially inferred that an increase in the film thickness has increased the grain size of the film. In accordance with the size driven phase transition, the larger grains in the thicker films will be tetragonal and contribute to the increased remnant polarization. Thus, the concentration of the cubic phase in these mixed phase films will be reduced in thicker films.

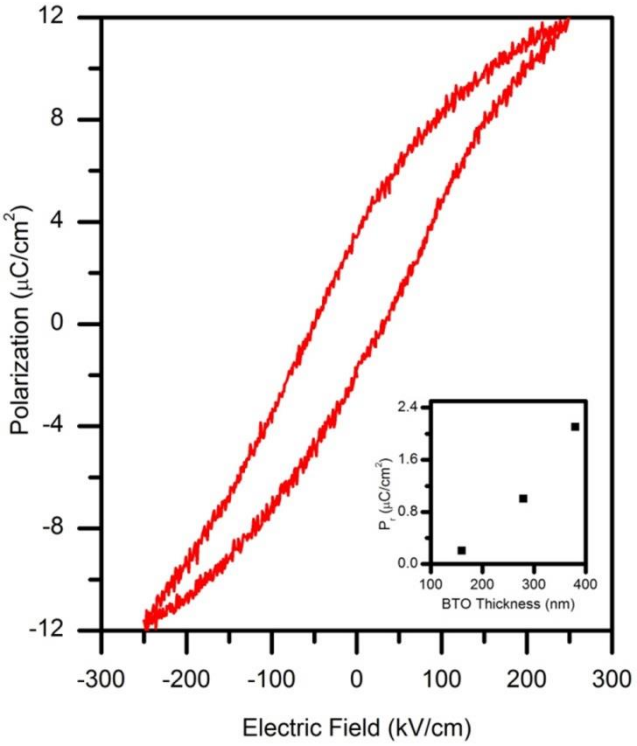

Figure 6.19: Large signal hysteresis measurements of the 380 nm thick BTO film. Inset shows the measured remnant polarization as a function of film thickness.

In order to verify any changes in the grain structure of the films, AFM topography scans are conducted and shown in figure 6.20. Each image shows an unchanged topography, which demonstrates an unchanging grain diameter as the film thickness is increased. However, from the TEM images of the 160 nm thick film in figure 6.16, BTO is known to grow in a columnar structure. Therefore, as the film thickness is increased the height of each individual column increases, while the diameter of each column stays constant as measured in the AFM scans. The increasing remnant polarization with film thickness is therefore due to an increase in the volume of each individual column as they grow in height. The increase in volume will favour the tetragonal phase whereby a larger number of dipoles are allowed to align along the polar axis, leading to the increase in remnant polarization. Ferroelectricity as a cooperative phenomenon favours an increase in the number of dipoles available for interaction, leading to an energetically stable ferroelectric phase. Previous studies discuss the number of required dipoles in terms of a correlation volume [67]. In the polycrystalline films with no preferred orientation, a similar effect should be seen if the diameter of the columns increase, which would be reflected in a changing topography in AFM scans.

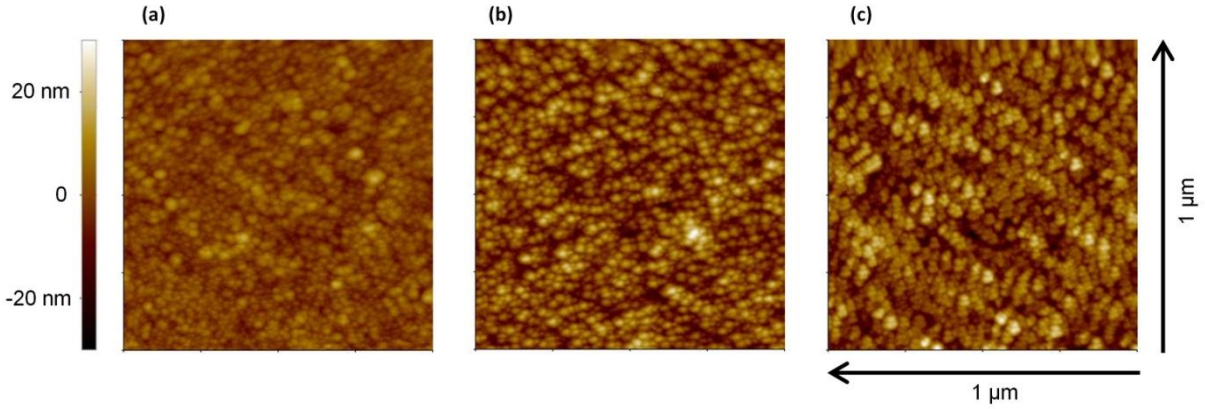

Figure 6.20: AFM topography scans of the 160 nm (a), 280 nm (b) and 380 nm (c) thick films.

6.6 Summary and Conclusion

Using high-κ material in contact with Si in MOS devices may lead to unwanted interfacial layers, resulting in a series of capacitances. Characterising the devices using the standard *EOT* equation leads to incorrect assumptions about the permittivity of the high-κ material, and does not incorporate the interfacial layer influence. A new *EOT* model was proposed, in conjunction with the series capacitance model, in order to acquire a method of estimating the interfacial layer thickness, as well as obtain a more accurate value of bulk permittivity in the high-κ insulator. Due to the similarities between series capacitances of high-κ / interfacial layers, and high-κ / dead layers, the *EOT* model may be used to analyse the effective dead layers that impact the electrical results in MIM devices. The *EOT* model was used to separate the interfacial capacitance parameters ε_i and t_i to describe the electrical results.

$SrTiO_3$ films of four different thicknesses were characterised as a function of film thickness in terms of an effective dead layer. As film thickness is reduced, it is shown that the maximum achievable permittivity and tunability is also lowered. Using TEM imaging, the dead layer capacitance within this model is shown to only be an effective capacitance, not a physical capacitance in series with a bulk-like $SrTiO_3$ film in a MIM structure. This supports the hypothesis of intrinsic influences causing the dead layer effect, such as incorrect electrode screening and depolarizing fields.

Investigation of the tunable properties of $SrTiO_3$ was done as a function of film thickness using the coefficients in LD theory. Each coefficient shows a thickness dependence, proportional to t_{ox}^{-1}, which is explained through a voltage partition of the series capacitance incorporated into LD theory. The fact that the α_1 term increases when compared to bulk values is a direct consequence of the effective dead layer causing

permittivity suppression as $\varepsilon_r \propto \alpha_1^{-1}$. However, the nonlinear α_{11} also increases, which indicated that the interfacial region is not 'dead' material with linear dielectric properties such as a TiO_x layer. This supports the results shown in TEM imaging in which $SrTiO_3$ is shown up until the electrode boundary. An increase in the nonlinear term should give an increase in the tunability, which is not the case when the film thickness is reduced. The increased α_1 term with decreasing film thickness masks this effect and dominates the free energy contribution to the capacitance system when considering equation 6.15. This has the effect of pinning the achievable permittivity beneath a given value, allowing less tunability with increasing bias.

Analysis of thin film $BaTiO_3$ integrated with Si on $Pt/Ti/SiO_2/Si$ substrates showed evidence of a mixed phase property in the films. The mixed phase film explains the low remnant polarization in thin film BTO as reported in the literature [28]. Large-signal measurements showed that increasing the film thickness led to an increase in the remnant polarization. The Raman spectra also confirmed that an increase in the film thickness correlated with increasing peak intensities at 300 cm^{-1} which is indicative of the tetragonal phase. XRD results showed that the crystallinity and texture stay constant with increasing film thickness. Furthermore, AFM and TEM imaging showed that the films grow in a columnar structure in which an individual column stays at a constant diameter as the film thickness increases. The results are such that as the films are grown with increasing thicknesses, the variable in terms of film structure is the increase in the height of each individual column.

The size driven phase transition sets a critical grain size in order for a material to display ferroelectric properties. In dense BTO ceramics the tetragonal phase was shown to be progressively less prominent [21]. Here, it is shown that for a thin film BTO grown in a columnar structure, the height of the individual column acts to increase

the remnant polarization due to the increasing contribution from the tetragonal phase. In each film the diameter of the columns stay at an approximate 30 nm in size.

6.7 References

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Chapter 7

Summary and Conclusion and Future Work

7.1 Summary and Conclusion

In this thesis, the electrical and material properties of perovskite insulators have been investigated for the nanoelectronics industry. Perovskite insulators have the potential to fulfil both the 'more Moore' and 'more than Moore' technology track agendas. For 'more Moore', where attention is turned to increasing the density of digital logic, an elusive negative capacitance property in ferroelectric perovskites may reduce the subthreshold swing. This in turn will lead to lower power dissipation and reduced voltages levels, which will aid in the pursuit for greater transistor packing density. For 'more than Moore', in which greater circuit functionality is important, the tunable capacitance and ultra-high-κ properties of perovskites can be used.

Chapter 4 shows compelling evidence for negative capacitance in $BaTiO_3$ at room temperature for the first time. The stabilised negative capacitance effect is shown over a large voltage range in a series capacitance system. The MIM bilayer capacitance

design is comparable to a MOSFET gate stack in which a series of capacitors is situated. The simulated results in figure 4.8 highlight that, if a negative capacitance layer, such as $BaTiO_3$, is placed in series with a positive capacitance, the total capacitance of the series is larger than the constituent positive capacitance. This result can only occur if a negative capacitance layer is stabilised in the series (figure 4.5). Experimental evidence for stabilised negative capacitance in the bilayer showing capacitance enhancement is given in figure 4.14. Furthermore, figure 4.17 shows a comparison between a single $BaTiO_3$ capacitor of 30 nm thickness, single $SrTiO_3$ capacitor of 25 nm thickness and a bilayer consisting of 25 nm $SrTiO_3$ and 30 nm $BaTiO_3$. Even with a total thickness of 55 nm, the bilayer shows larger measured capacitance than the single 25 nm $SrTiO_3$ capacitance and the single 30 nm $BaTiO_3$ capacitance, owed to a stabilised negative capacitance layer. The results show that $BaTiO_3$ displays effective negative capacitance if the perovskite is stabilised in a series capacitance configuration.

In chapter 5, perovskites are studied for the purpose of 'more than Moore', where high permittivity and tunable capacitance can be utilised. Low temperature growth of $SrTiO_3$ using PLD showed that 500 °C is sufficient temperature to crystallise the films when grown on a Si substrate. However, when films of $SrTiO_3$ are grown using ALD and post deposition annealed at equivalent temperatures, the films only partially crystallised (figures 5.4 and 5.5). Film composition was shown to be an important factor in achieving crystallisation, and Sr rich films may crystallise at lower temperatures. The finding may lead to lower crystallisation temperatures for films that are to be incorporated in the back-end-of-line where temperature must be kept low. Furthermore, alloying samples with high concentrations of Ba proved ineffective in order to improve the electrical properties of the films. The resulting $Ba_{0.8}Sr_{0.2}TiO_3$ films

deposited at 500 °C using PLD increased the crystallisation temperature such that all high permittivity and tunable properties were lost. Therefore, $SrTiO_3$ is the likely candidate for incorporating perovskites into the back-end of integrated circuitry. $BaTiO_3$ was also investigated using sputter deposition, which suffered from the same high crystallisation temperatures required for the $Ba_{0.8}Sr_{0.2}TiO_3$ films grown using PLD. The results show that perovskite insulators can be crystallised at 500 °C for the purpose of back-end integrated circuitry, provided the film composition is well controlled.

Chapter 6 investigates the properties of ferroelectric and tunable characteristics for integration with Si. An *EOT* model is used and adapted for the purpose of characterising high-κ material. It was found that the standard *EOT* equation is unsuitable for series capacitance systems in which either interfacial layers, or dead layers, act upon the achieved electrical results. The amended *EOT* model may be used to calculate the layer thicknesses. The *EOT* model is applied to $SrTiO_3$ thin films grown using PLD on Si substrates, which suffer from a dead layer effect. The thickness of the dead layer was calculated at 7.5 nm, but evidence for a physical layer of 'dead' material in TEM imaging in figure 6.11 was absent. The results show that the dead layer effect is only electrically active and physical series capacitances are not apparent. This suggests that dead layers may not be used as the stabilising positive capacitance for negative capacitance bilayers. Negative capacitance stabilisation requires a positive energy function to be summed to the negative curvature of the ferroelectric layer. Therefore, as the dead layer is not a physical layer, the summation of a positive layer to the total bilayer energy function would be absent.

$BaTiO_3$ was also investigated for its ferroelectric properties when it is integrated with Si substrates. The results showed that thin film $BaTiO_3$ deposited using

PLD exists in a mixed phase constitution. At room temperature, the films were dominated by its cubic phase, responsible for paraelectricity, due to its permittivity response to temperature (figure 6.14); however, capacitance-voltage measurements suggested a tetragonal phase, which is responsible for ferroelectricity (figure 6.13). Thicker films achieve a larger grain size, which is further shown to correlate with an increase in remnant polarization. The results confirm the size driven phase transition in films of ferroelectric material integrated with Si. Furthermore, due to the small achieved remnant polarization, reaching a maximum 1.8 $\mu C/cm^2$ in the 380 nm thick film, the $BaTiO_3$ film grown on Si was unsuitable for use in the bilayer capacitors for the purpose of investigating negative capacitance. A large remnant polarization, and hence large hysteresis window, is most desirable as the negative slope associated with negative capacitance is situated around the origin [1].

7.2 Future Work

The current bilayer designs used for the experimental confirmation of negative capacitance are based upon single-crystal $SrTiO_3$ substrates. From the discussion in chapter 3, the reasons for the choice of $SrTiO_3$ substrates are due to the lattice matching between the ensuing perovskite films, preferred straining and ensuring epitaxial growth. All the aforementioned properties are desired such that the simulated characteristics of perovskites shown in section 4.2 can be reproduced experimentally. However, in a Si-driven electronics industry, experimental evidence of negative capacitance on a Si substrate is important. Therefore, replacing the $SrTiO_3$ substrate with an equivalent Si substrate would be required. Problems arising due to lattice mismatching between the perovskite and Si and differing thermal expansion coefficients, may lead to bilayers of inferior properties to the ones studied in this thesis. For example, a polycrystalline grown film inherently introduces grain boundaries into the insulator, whose properties are unpredictable.

One solution as an immediate step towards Si integration is the use of a yttria-stabilised zirconia buffer layer, previously discussed in section 2.3.6. The application of such a layer would be to promote epitaxial growth of the ensuing perovskite films, and therefore reproduce the characteristics of the bilayers when grown on $SrTiO_3$ substrates. The buffer layer would be grown on the Si substrate, and following a CeO_2 and either a $LaNiO_3$ or $SrRuO_3$ bottom electrode would be grown. The layers are chosen such that the large lattice mismatching between the eventual $BaTiO_3$ or $SrTiO_3$ films and the Si substrate can be accommodated. The structures have been investigated with single layers of $BaTiO_3$, which showed large increases in the out-of-plane polarization [2]. A cross-section of the proposed bilayers in order to test the negative capacitance hypothesis for integration with Si is shown in figure 7.1. The proposed

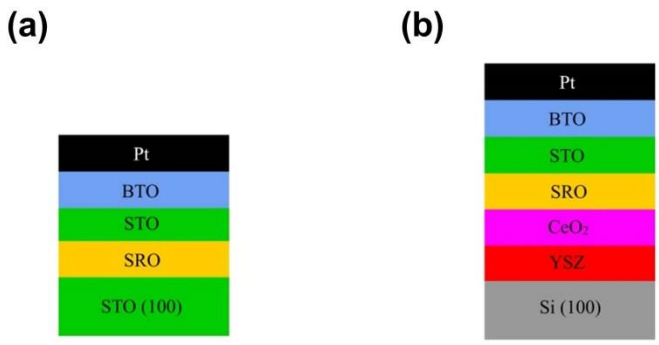

Figure 7.1: (a) Cross-section of the MIM bilayer from chapter 4. (b) The proposed bilayer with a Si substrate. An additional yttria-stabilised zirconia layer is incorporated into the design in order to epitaxially grow perovskite films on Si substrates [2].

designs would lead to a route towards negative capacitive layers being incorporated with Si devices, such as the MOS capacitor, or MOS transistor.

The ultimate aim for negative capacitance is to incorporate the technology into a MOSFET gate stack. The technology will see $BaTiO_3$ replace a now well established high-κ oxide material, for example HfO_2. In order to reproduce the results shown in chapter 4 in a MOS capacitor, the stabilising positive capacitance will have to be replaced by the underlying semiconductor capacitance, C_s. This capacitance is associated with the underlying Si and depletion layer. However, there will also need to be a thin SiO_2 layer in between the $BaTiO_3$ and Si channel, which introduces a third capacitance in the series. The reason for this is because of the high quality of the Si/SiO_2 interface in terms of reduced interface states compared with other Si/dielectric interfaces. In fact, the success of the Si transistor is largely due to the superior SiO_2 layer in the gate stack.

Equation 2.20 and 2.21 are now used to design the framework for negative capacitance in a MOS capacitor. Equation 2.20 and 2.21 are repeated below

$$SS = \frac{\delta V_G}{\delta(\log_{10} I_D)} = \frac{\delta V_G}{\delta \Psi_s} \cdot \frac{\delta \Psi_s}{\delta(\log_{10} I_D)} = 2.3\frac{kT}{q}\left(1 + \frac{C_S}{C_{ox}}\right) \quad (2.20)$$

$$\frac{\delta V_G}{\delta \Psi_s} = m = \left(1 + \frac{C_S}{C_{ox}}\right) \quad (2.21)$$

where the *SS* should be lower than 60 mV/decade by making $m < 1$. In order to make m < 1, a negative term should be introduced into C_{ox}, which is the capacitance associated with the gate stack. Equation 2.21 is now written with the contribution from the $BaTiO_3$ and SiO_2 layers

$$m = 1 + \frac{C_S}{\left(\frac{C_{BTO}C_{SiO2}}{C_{BTO}+C_{SiO2}}\right)} \quad (7.1)$$

C_{ox} is now a series configuration of C_{BTO} and C_{SiO2}, which is the contribution from the $BaTiO_3$ and SiO_2 layers, respectively. Two limits are placed on *m*: for a *SS* < 60 mV/decade $m < 1$ and for stability reasons $m > 0$. Therefore, equation 7.1 is rewritten as

$$0 < m = 1 + \frac{C_s}{\frac{C_{BTO}C_{SiO2}}{C_{BTO}+C_{SiO2}}} < 1 \quad (7.2)$$

Equation 7.2 is now rearranged to establish design constraints for the negative capacitance layer.

$$\frac{C_s C_{SiO2}}{C_s+C_{SiO2}} < -C_{BTO} < C_{SiO2} \quad (7.3)$$

where $-C_{BTO}$ is effectively $|C_{BTO}|$ as C_{BTO} is negative. The upper limit, $-C_{BTO} < C_{SiO2}$, is the condition for a *SS* < 60 mV/decade and is when $m < 1$. This limit ensures that the total capacitance associated with the gate stack, C_{ox}, is negative, and is operating in region (a) from figure 4.5. If a negative C_{ox} is substituted into equation 2.21 then $m < 1$. The stabilising positive capacitance is now C_s. In this regard, the total series

capacitance of C_{ox} and C_s will now be greater than the constituent positive capacitance C_s. The result is in direct comparison to the MIM bilayer design in chapter 4, however an additional capacitance C_{SiO2} is introduced, and the positive stabilising capacitance from $SrTiO_3$ is supplanted by C_s.

Figure 7.2 shows the body factor, *m*, calculated as the thickness of the $BaTiO_3$ layer increases. The body factor is calculated from equation 7.1, and equation 4.7 is used to calculate the capacitance of the $BaTiO_3$ layer using the LD coefficient for α_1 described in chapter 4. The SiO_2 capacitor is calculated using a 1 nm thickness, and for permittivity equal to 3.9. The semiconductor capacitance is calculated using a doping density of 10^{17} cm^{-3} and at an applied gate voltage above the flat-band voltage.

In figure 7.2, there exists a region where $m > 1$. Within this region, the total capacitance, C_{ox}, associated with C_{BTO} and C_{SiO2}, is positive. This positive scapacitance

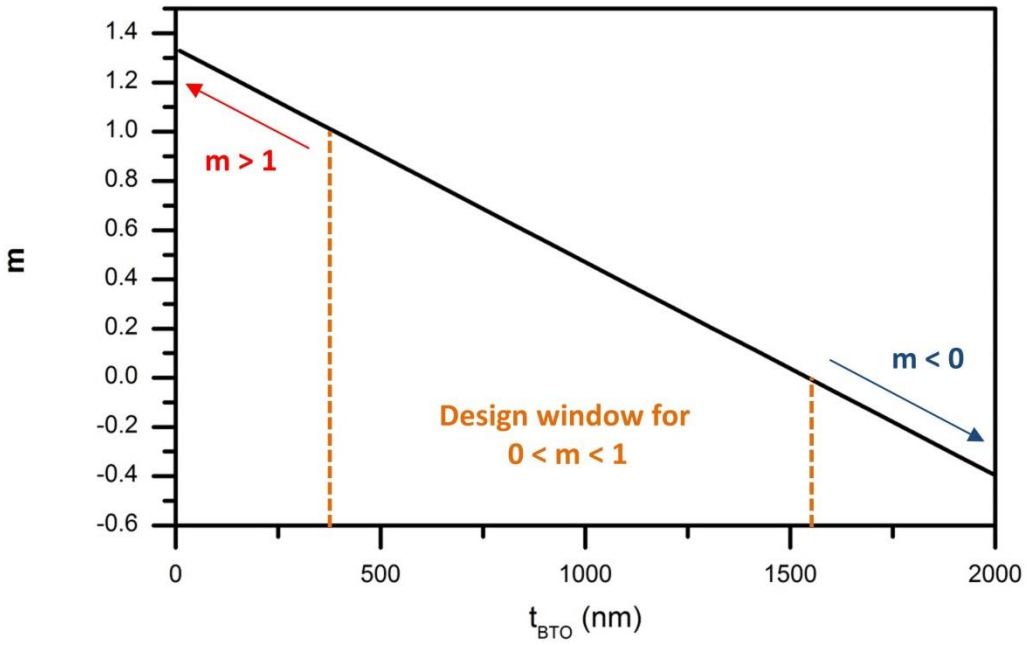

Figure 7.2: The body factor, *m*, calculated using equation 2.21. A design window is shown for certain thicknesses of the $BaTiO_3$ layer.

originates from $|C_{BTO}| > C_{SiO2}$, and therefore would operate in region (b) in figure 4.5 for total positive capacitance enhancement. Substituting a positive C_{ox} into equation 2.21 would result in $m > 1$. In the design window for $0 < m < 1$, the capacitance C_{ox} is now negative and $|C_{BTO}| < C_{SiO2}$. The stabilising positive capacitance is now C_s, and the total series capacitance of C_{BTO}, C_{SiO2} and C_s, would be greater than the capacitance C_s. Finally, when $m < 0$, the lower limit imposed from equation 7.3 is not satisfied. The total series capacitance of all three capacitors would be negative, and hysteretic characteristics would ensue.

Figure 7.2 shows that the thickness of the $BaTiO_3$ layer has to be correctly designed for the purpose of achieving $0 < m < 1$. If the thickness of the $BaTiO_3$ layer is too large, stability issues arise, where $m < 0$, and hysteretic characteristics would result. However, if the $BaTiO_3$ layer is too thin, $m > 1$ and the *SS* is > 60 mV/decade. The addition of a thin layer of SiO_2 introduces a low capacitance into the design. For this reason, the $BaTiO_3$ needs to be relatively thick in order to compensate for the low capacitance. This is due to the balancing of the energy density functions of the system. The overall energy density of the $BaTiO_3$ and SiO_2 layers should show double well minima. The additional contribution from the positive capacitance, C_s, will then act to stabilise the system, creating the single minimum energy function at zero polarization. Conversely, increasing the $BaTiO_3$ thickness too much would result in the overall energy function showing double well energy minima. The outcome is an unstable state, and the MOS capacitor would operate in region (a) from figure 4.5.

Figure 7.2 is calculated using the LD coefficient for $BaTiO_3$ from chapter 4. In this chapter, the MIM bilayer was based upon a full perovskite stack that was epitaxially grown. The reason for this was to approach the ideal characteristics shown in the simulations in section 4.2. However, in the gate stack of the MOSFET, the structure of the films will differ when compared to the MIM capacitor. For example, the growth of a $BaTiO_3$ film on an amorphous SiO_2 layer will not be epitaxial, and the resulting $BaTiO_3$ structure will be polycrystalline. Grain boundaries and further random grain orientations, will therefore impact the characteristics of the $BaTiO_3$ film. Consequently, the $BaTiO_3$ film in the gate stack should show an increase in the LD coefficient α_1. This can be understood by assuming that the permittivity will reduce if the $BaTiO_3$ is polycrystalline (equation 2.15). In this regard, the upper limit of equation 7.3 shows that the capacitance of C_{BTO} should be less than C_{SiO2}; therefore, the required film thickness may be lower than what is shown in figure 7.2 if the permittivity is reduced. In fact, using an estimated permittivity for C_{BTO} of -100, the required thickness to ensure $0 < m < 1$ is 28 nm to 94 nm. Thus, the achieved quality of the $BaTiO_3$ film is critical for operating in the design window shown in figure 7.2. The overall capacitance of C_{BTO} must be designed accurately using equation 7.3 if the SS is to be lower than 60 mV/decade.

The results in chapter 5 showed that $SrTiO_3$ thin films are crystallised when grown using PLD at 500 °C. However, the tunability was low, and alloying the films with Ba increased the crystallisation temperature above 500 °C. The reason for the increase in the crystallisation temperature was the high concentration of Ba, which was 80 % of the A-cation contribution in the perovskite. Further studies on $Ba_xSr_{1-x}TiO_3$, where $x < 0.8$, are proposed for the purpose of keeping the crystallisation temperature

below 500 °C. If the crystallisation temperature is kept low, the advantages of introducing Ba, such as greater tunability, may be obtainable.

7.3 References

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