Low frequency noise in silicon carbide & graphene electronics

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Dedicated to

Chan family

Declaration

I certify that all material in this thesis which is not my own work has been identified and that no material has previously been submitted and approved for the award of a degree by this or any other university.

Hua Khee Chan
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Abstract

The electrical noise phenomenon in semiconductor devices has been an on-going research topic throughout the evolution of semiconductors, having been discovered in the characteristics of a vacuum tube [1]. Being a naturally occurring phenomenon, due to the microscopic interaction of conducting carriers with defects in the lattice structure, electrical noise can never be eliminated completely. Instead the degree of current/voltage fluctuations can only be reduced if the noise origin is known and well-understood. Amongst the types of electrical noise identified, the low frequency or $1/f$ noise is the most studied phenomenon, owing to the valuable insight that it gives in relation to the degree of crystal perfection, structural quality of fabricated devices and device reliability; as well as its impact and disturbance on circuit operation. In this thesis, the focus is on exploring the characteristics of low frequency noise on electronic devices made using silicon carbide, in particular, a high temperature signal-level junction field effect transistor (JFET), and 2D graphene film utilising an epitaxially grown graphene field effect transistor (GFET).

One of the advantages of using SiC electronics is its ability to operate at higher temperatures than conventional Si and SOI technologies, where theoretical predictions of operation above 800°C and practical device operation up to 600°C have been demonstrated [2]–[5]. The realisation of high temperature devices opens up a new opportunity for functional electronic systems in hostile environment applications, such as in space exploration, geothermal/geo-exploration plus monitoring capability and thermal/nuclear reactor inspection. As one of the key design considerations in analogue circuits, the low frequency noise defines the minimal recoverable input signal of an amplifier, limits the down-scaling of signal level & transistor sizes, and affects the RF circuit operation in the form of phase noise. In the effort to facilitate the transistor optimisation process in enabling functional SiC electronics in extreme environment, the electrical noise origins of JFET with 9μm and 21μm gate length with multiple gate width dimensions were investigated. The noise behaviours of the transistor variants are each dominated by the generation-recombination (G-R) process and contribution of resistive noise components. Furthermore, the temperature dependence of the JFETs noise characteristics measured from 300K to 700K can be distinctively correlated to each JFET variants, where the trap assisted G-R mechanism and the low-field mobility-temperature dependence can be used to describe the acquired results correspondingly.

In the effort to deploy SiC electronics in extreme environment, it is imperative to first understand the electrical performance and lifetime of SiC devices, when subjected to prolonged operating conditions. This is useful to pinpoint the expected operational lifetime and ensure the reliability of these critical electronic components. Whilst, the DC and AC characteristics may offer a restricted amount of information on the level of device degradation, any abnormality in device operation can be better detected by low frequency noise measurements, where the degree of noise deviation between the good and damaged devices often exceeds those observed using DC and AC parameters. The reliability of SiC JFETs subjected to 1000 hours of high temperature stressing was examined utilising both current-voltage and low frequency noise behaviour. The degraded device structures of the stressed SiC JFETs can be successfully segregated by comparing the low frequency noise and current-voltage characteristics between the aged and as-fabricated samples. It was found that the degradation of contact metallisation governed the transistor noise properties at drain-source voltages ≤1.25V and the enhanced multi level G-R process from traps generated in the active transistor structures dominate the noise at drain-source voltages >1.25V.

Graphene has gained a significant amount of research attention in recent years, owing to its superlative material properties. The ultra high carrier mobility, large surface to volume ratio, and potentially ultra low noise property, position graphene as an attractive candidate in fabricating remarkable switching devices and sensor nodes that surpass current state-of-the-art technology. Whilst, the ideal graphene characteristics may seem extraordinary, in practice the actual device properties do not match theoretical predictions, due to the material synthesis and device fabrication processes, which introduce unintentional defects into the system. The influence of gate dielectric formation is investigated by correlating noise measurements with conventional DC and AC parametric testing. The obtained noise results illustrate that the normalised current noise magnitude shows a power dependency with the channel resistance. An enhanced hysteresis effect is also observed for epitaxial GFETs that can be correlated to the quality of the graphene/oxide interface formed during gate dielectric formation. The Hall Effect mobility and noise properties of these GFETs were mapped on wafer scale (16mm×16mm) to examine the material and device reproducibility and repeatability for large scale manufacturing. The inverse relation between the GFETs low frequency noise and the Hall Effect mobility and the weak sheet resistance dependence on the sheet electron concentration, implies a short-range mobility scattering related noise origin.

Contents

List of publications

D.K. Gaskill, **H.K. Chan**, V.D. Wheeler, V.K. Nagareddy, L.O. Nyakiti, A. Nath, R.L. Myers-Ward, Z.R. Robinson, N.Y. Graces, M.V. Rao, J.P. Goss, N.G. Wright, C.R.Eddy, Jr, and A.B. Horsfall, *"The low-frequency noise spectrum in gated epitaxial graphene field-effect-transistors"* APS March Meeting, Denver, Virginia, March 3–7, (2014), Oral presentation.

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Chapter 1: Introduction

1.1 Background

　　With the ever increasing demand for functionality and performance of consumer based electronic devices, as well as the expansion and development of novel electronics market such as those requiring high temperature, radiation hardened and high power-to-density-ratio operability, it is imperative to continuously optimise and improve existing semiconductor technology. Strategies may include the miniaturisation of device physical dimensions to increase the transistor density; adaptation of system on chip (SoC) design to create a single multi-function integrated circuit (IC); development of novel transistor technology for faster switching speeds; and introduction of wafer stacking technology to enable multi-wafer integration. Nevertheless, when the conventional state-of-the-art semiconductor technology is incapable of delivering the required performance, notably due to the constraints in material properties and the limitation in device dimensional scaling, an alternative method such as the utilisation of novel semiconductors with superior electrical properties is a more feasible approach to tackle these challenges.

　　In the case of extreme (high temperature and/or irradiated) environment applications (eg. aerospace, oil and gas and electrical vehicles), where operating temperature is beyond ICs made of conventional materials (for example a maximum 225°C for silicon on insulator (SOI) technology), the electronics can be replaced by wide band-gap materials such as the silicon carbide, where the highest operating temperatures were predicted and demonstrated at 900°C and 600°C respectively [2]–[5]. For RF applications, although current communication modules are widely made of compound III-V material, the rapid evolution in telecommunication technology that requires faster data rate based on the use of a higher & broader frequency band as well as increased power density of the base station to support the growing network, will render current III-V solutions obsolete or uneconomical. Projections predicts that III-V materials will reach an intrinsic maximum cut-off frequency at 850GHz and an oscillation frequency of 1.2THz by 2021 [6]. Therefore a replacement technology needs to be fully deployable by then.

　　The design and development of device technology on novel materials usually begins with the adaptation of existing transistor design and fabrication process before

prototypes are redesigned to meet industrial standards. Being a pioneer in semiconductor device design, it is necessary to thoroughly understand the distinct material characteristics, impact of novel device structure and corresponding fabrication techniques on transistor performance. One of the key challenges in new device design is the presence of electrical noise originating from the microscopic interaction between carriers and high defects/traps densities, which are induced intrinsically by material imperfections and/or unintentionally generated, due to device structure or fabrication techniques. The manifestation of noise in electronic devices is nothing new. It is a naturally occurring phenomenon that is widely recognised and imposes disturbances in the physical, astronomical, biological, psychological, musical and electronic systems [7]–[12]. In electronic systems, the presence of electrical noise can never be fully eliminated, especially for noise generated within the device; however by studying the characteristics of these disturbances, the noise generation source can be identified and suppressed.

Because of the close correlation between electrical noise and microscopic events in semiconductor devices, noise data provides a useful insight and diagnostic tool for the physical operation that can be used to gauge the quality of the wafer as well as assessing the structural perfectness of a fabricated device. Similarly, the comparison of noise results between the as-fabricated devices and those which have undergone reliability stressing can help identify the failure modes, to consequently improve device design and fabrication process, ultimately extending the device operating lifetime. From a circuit perspective, the electrical noise is a limiting factor on the minimum input signal that needs to be fed into an amplifier to maintain the integrity of valuable information. The figure of merit for this performance is classified as the signal to noise ratio (single level system) or the noise figure (cascaded system), which is one of the critical considerations in analogue circuit design. Furthermore, electrical noise in particular the low frequency or $1/f$ kind that can be up-converted in the form of phase noise whilst interacting with the inductive-capacitive-resistive (LCR) components, deteriorating the high frequency operation of an RF circuit [13], [14].

1.2 Motivation

The focus of this thesis resides in the application of low frequency noise (LFN) investigation on the characteristics of high temperature signal-level SiC junction field effect transistor (JFET) and epitaxially grown (on SiC substrate) top-gated graphene field effect transistors (TG-EGFET or more generally GFET). These SiC JFETs are

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intended for extreme environment applications, where the transistors serve as the active components for signal conditioning and communication systems. Hence it is important to understand the low frequency noise performance under different operating conditions to facilitate circuit design and device optimisation. In addition, the assessment of device reliability using LFN under long term exposure to extreme environment conditions is useful to predict the device lifetime for decommissioning or scheduled replacement of these SiC electronic systems. Furthermore the low frequency noise results are useful to pin-point the device failure mechanism as the transistor may undergo structural deformation. Although previous literature has reported LFN characteristics on buried gate vertical JFET using 4H and 6H SiC, as this JFET structure is uniquely design for power electronics application, the LFN results may not be relevant to the signal-level lateral SiC JFETs investigated in this work.

Due to the unique epitaxial graphene synthesis process that leads to distinctive material properties, the LFN characteristics of our TG-EGFETs can be used to verify theoretical predictions of graphene material properties as well as establishing a fundamental understanding of LFN characteristics, such as the area and atomic thickness scalability, impact of SiC surface properties, correlation of transport properties, and influence of extrinsically fabricated structure (e.g. contact metallisation, gate dielectric material, photolithography) and ultimately the noise generation sources. At the present time there is no standard fabrication practice established for graphene device fabrication, therefore these results are important to help formulate a series of processes that can serve as exemplary practice to manufacture graphene devices with best electrical performance. Furthermore, the acquired LFN characteristics are also important for the high frequency and RF system design.

1.3 Chapter outline

Chapter 2 begins with the presentation of the existing literature relating to type of electrical noise and the basic mathematical expressions in describing the noise power, before the discussion is focussed on the material properties of both SiC and graphene. Next, the different SiC transistor structures are illustrated with the justifications on why the SiC JFET is the most suitable structure for extreme environment applications. The different gate configurations for the graphene field effect transistor are also briefly discussed in section. Chapter 2 is concluded by introducing a small signal equivalent noise model for the JFET and GFET structure.

Chapter 3 discuss the current-voltage (I-V), capacitance-voltage (C-V), LFN and Hall Effect characterisation techniques used in this work and the corresponding instrumentation setup. The mathematical expressions used to produce each parameter are illustrated. In addition, this chapter also briefly outlines the best practise techniques used in the measurements

Chapter 4 present the LFN results of the 4H-SiC epitaxial JFETs, starting with the influence of transistor gate geometry on the I-V and noise characteristics, in an effort to identify and correlate the transistors LFN source based on existing models. The impact of high temperature operation, up to 400°C, on the transistor noise properties is also investigated. Whilst, this outcome provides useful insight into the noise behaviour under high temperature operation, it also serves as an evaluation tool to validate the proposed noise source/modelling for the different JFET variants. Finally, the LFN properties and DC characteristics of the transistors are used to justify which JFET design is the most suited for high temperature switching components.

Chapter 5 investigates the reliability of 4H-SiC epitaxial JFETs that have undergone 1000 hours of 400°C and 500°C high temperature aging. The post current-voltage and low frequency noise characteristics at different gate-source voltages from the stressed JFETs samples are acquired and compared against as-fabricated samples to assess the overall deteriorated characteristics. Utilising the transistor drain-source channel, transmission-line-model (TLM) structure and the JFET P+NN+ or the gate junction, the cause of excess noise is identified. The proposed hypothesis is verified by comparing the LFN behaviour under a high temperature sweep, amongst the three investigated samples.

Chapter 6 explores the LFN properties of the atomic layer deposited high-κ top-gated epitaxially grown junction field effect transistors. The chapter begins by examining the influence of the gate dielectric formation process, using current-voltage and LFN characteristics, followed by electrical and noise comparison between Al_2O_3 and HfO_2 gated GFETs. The observed hysteresis effect on the two TG-EGFET variants is further inspected utilising capacitance-voltage properties and a hysteresis model, proposed to correlate the noise and C-V characteristics with the charges interaction between gate dielectric and graphene channel. Next, the sheet resistance, LFN, and Hall Effect properties are mapped on the 16mm×16mm substrate for the two dielectric

samples. Finally, scaling of LFN against the sheet resistance, mobility and Hooge parameter are examined alongside with a proposed noise generation mechanism.

Chapter 7 presents the conclusion and the proposed future work for this thesis.

Chapter 2: Silicon carbide and graphene electronics: electrical noise, material properties and device technology.

2.1 Electrical noise

Following the definition provided by Oxford English dictionary [15], the term "noise" (in particularly electrical noise) can be described as follows:

Noise •*n* **Pronunciation:** /nɔɪz/
2. Technical irregular fluctuations that accompany a transmitted electrical signal but are not part of it and tend to obscure it

In a broad sense, noise phenomenon can be perceived as the unwanted disturbance superimposed onto a useful signal or information. For instance, if we try to reach out to another person in a packed pub, the effort of conveying the message will be much greater in comparison to a quiet empty room. The situation is exacerbated if we decided to speak normally without raising our voice in such a noisy environment, which may lead to the failure in delivering our content to the targeted person. Similarly, the electrical disturbances in electronic circuitry can obstruct the desirable electrical signal when the noise magnitude is in excess of the signal power, masking the useful signal and ultimately hampering the intended operation or functionality of the system.

The electrical noise in an electronic system may originate from external sources including AC power line (50Hz), cross-talk or interference from adjacent circuits, electromagnetic coupling, electrostatics, vibration, radiation and lighting. Nevertheless, these disturbances can be eradicated with cautious PCB layout design, proper electromagnetic shielding, electrical isolation and line filtering. On the other hand, the naturally occurring electrical noise arising from semiconductor devices via random perturbation of the device physical parameters, disrupts or alters the inherent electrical signal and cannot be eliminated completely. Such interference limits the accuracy of a sensory system, lowers the input signal level that can be processed for signal conditioning circuitry as well as distorting the high frequency component of an RF or oscillator circuit in the form of phase noise. Fortunately, the study of noise behaviour under different operating conditions helps pinpoint the origin. Such information can be utilised to improve the device fabrication process and revise the structure of electronic

devices and optimise the material growth processes that serve as one of the critical factors in minimising the noise manifestation.

2.2 Mathematical quantification of electrical noise

There are generally two processes that can be used to describe the electrical noise generated in a semiconductor device. Whilst, the quantification of equivalent averaged electrical noise manifests from the stochastic processes can be defined in terms of mean value, variance, autocorrelation function and power density, the corresponding noise magnitude for a stationary process is a mean value over a finite time period and is the most widely considered fluctuation process in the reported electrical noise experiments [16]. Due to the nature of the measurement techniques employed in this investigation, where the voltage/current fluctuation is measured and averaged over a fixed period, a stationary process is adopted for the noise analysis in this work.

When an electrical perturbation is superimposed onto an electrical signal (denoted as A), the summation of both parameters at a particular instance can be expressed as:

$$A(t) = \overline{A} + \Delta A(t) - (2.1)$$

where $\overline{A}$ is the intended electrical signal averaged over a long time interval and $\Delta A(t)$ is the instantaneous electrical noise at time (t). The average square of $\Delta A(t)$ over a very long time or $\overline{\Delta A(t)^2}$ is a quoted as a constant value for stationary noise. $\Delta A(t)$ can be further described in a Fourier form as [16]:

$$\Delta A(t) = \sum a_i \exp(i2\pi f_t t) + a_i^* \exp(-i2\pi f_t t) - (2.2)$$

here a_i and a_i^* are the coefficient of amplitude of fluctuation for the time and frequency domain respectively. The noise component acquired at a specific frequency, f_t can be expressed as [16]:

$$\overline{\Delta A(t)} = 0 - (2.3)$$

$$\overline{\Delta A(t)^2} = 2\overline{a_i a_i^*} - (2.4)$$

whereby the average of fluctuation signal with an opposite Fourier domain (f_t & t) will nullify each other out (analogous to a sinusoidal wave with opposite phases) resulting in zero noise magnitude, whilst the square mean of these noise fluctuation functions is equal to the sum of Fourier coefficients (a_i and a_i^*) illustrated in Equation 2.2.

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If the electrical noise is measured in a unit bandwidth, $\overline{\Delta A(t)^2}$ can be expressed in the form $\overline{\Delta A(t)^2}/\Delta f$, where the resulting parameter is known as the noise power spectral density, $S_A(f)$. It can be noted that this is a general form of the power spectral density and the parameter can be written in different equivalence such as current, voltage, and conductance. Furthermore, it is worth mentioning that the Fourier components of $S_A(f)$ acquired within this bandwidth are summed quadratically. Following the prediction of Wiener-Khintchine theorem, $S_A(f)$ can be closely associated with an autocorrelation function denoted as $C(t)$, where the term signifies the average rate of decay for a deviation in $\Delta A(t_0)$ and can be described as [16]:

$$C(t) = \overline{\Delta A(t_0)\Delta A(t_0 + t)} = \lim_{T \to 0} \frac{1}{2T} \int_{-T}^{T} \Delta A(t_0)\Delta A(t_0 + t)\, dt \quad - (2.5)$$

Both the $C(t)$ and $S_A(f)$ expressions are transposable and can be expressed as:

$$S_A(f) = 4 \int_{0}^{\infty} C(t) \cos(2\pi f t)\, dt \quad - (2.6)$$

$$C(t) = \int_{0}^{\infty} S_A(f) \cos(2\pi f t)\, df \quad - (2.7)$$

Equations 2.6 and 2.7 based on the Wiener-Khintchine theorem are the essential building blocks needed to construct a physical model to describe the observed electrical noise in a semiconductor device. The noise properties predicted using Equations 2.6 and 2.7 are theoretically comparable with the observed electrical noise spectrum in both shape and magnitude. An example of electrical noise spectrum acquired from a field effect transistor is illustrated in Figure 2.1.
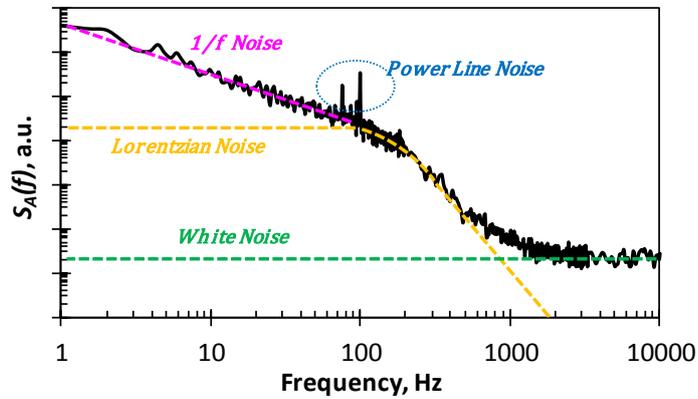
Figure 2.1: An example of electrical noise spectrum, with the corresponding noise components, measured from a field effect transistor.

There are several distinct noise components that can be observed from the data in Figure 2.1. Starting from the low frequency regime, a pink noise component commonly known as the low frequency noise (LFN) or $1/f$ noise due to the inverse frequency dependence of the noise power spectral density is dominating the power spectrum. The multiple noise peaks observed between 50Hz and 100Hz are the harmonics originating from the 50Hz line frequency, which is denoted as the power line noise. This component can be typically suppressed with either numerical post processing techniques or cautious electrical isolation during experimental setup. In the higher frequency range (between 100Hz and 1kHz), a unique Lorentzian component of generation-recombination noise fluctuation is observed before the noise power spectral density becomes dominated by a white noise component that is independent of frequency. The white noise element is commonly contributed by the intrinsic thermal and/or shot noise (to be discussed in the next section) or is due to the extrinsic influence from the background noise from the instrumentation. The cut-off frequency between the frequency dependent and white noise components varies between devices, and typically lies between a few hundred Hertz and up to the range of mega Hertz. In this thesis, the investigation effort is focused solely on the frequency dependent noise component notably the LFN due to the immense physical data it represent such as quality of semiconductor material, structural defects/imperfections electron devices, device failure indication etc; nevertheless the origin and mathematical expression for the other most observed electrical noise of intrinsic nature are discussed in the next section.

2.3 Type of electrical noise

The electrical noise phenomenon in semiconductors has been extensively studied over the past six decades [1], [17], generating numerous empirical and physical models that explicitly describe a specific noise type [16], [18]–[25]. Most of these observed electrical noise components are very well defined and understood, for instance the thermal noise, shot noise, generation-recombination noise and random telegraph noise. However, there is one particular noise component that seems to be inconclusive to describe or even to agree upon its origin; that is the infamous LFN or $1/f$ noise. In this section, a brief description and mathematical model for the aforementioned electrical noise types are covered and then the discussion is focused on the different origins of the LFN source with a corresponding noise model.

(a) **(b)**
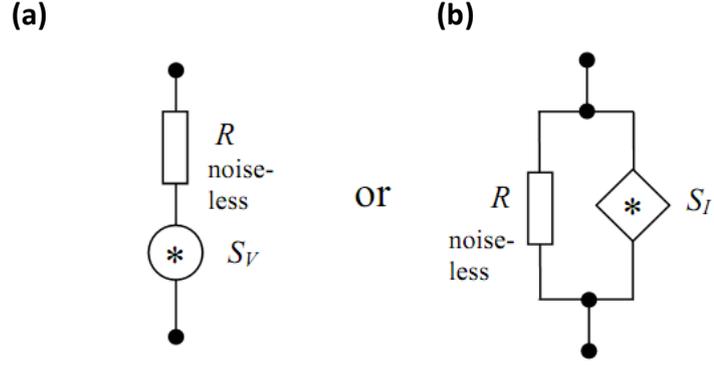
Figure 2.2: Equivalent electrical noise model in the a) Thévenin and b) Norton configuration.

Two general small signal circuit equivalents are usually employed to model electrical noise. The investigated samples are assumed to comprise a noiseless resistor denoted as $R_{noiseless}$ and the generated electrical perturbations are either considered as a voltage source superimposed on $R_{noiseless}$ in series configuration for the Thévenin notation or a current source place in parallel with the $R_{noiseless}$ for the Norton equivalent. The schematic presentations of the two conventions are presented in Figure 2.2.

2.3.1 Thermal Noise

Thermal noise, first predicted by Albert Einstein [7], describes a fluctuation of the electromotive force induced by Brownian motion of free electrons within a material under thermal equilibrium. The phenomenon was later demonstrated experimentally by J.B. Johnson [26] and the power spectral density was calculated by H.T Nyquist [27]. Therefore, thermal noise is also known as the Johnson, Nyquist, diffusion (due to the nature of mechanism) or velocity fluctuation noise.

Thermal noise is generated by a carrier scattering process, where the corresponding velocity of the carrier involved is randomised, inducing a form of velocity gradient within the material. The generated gradient causes the surrounding carriers to drift in a specific direction, resulting in a small net current flow that is measurable as the noise power spectral density. Under equilibrium conditions, the average energy of this motion is expressed as $k_BT/2$ and demonstrates an ultra fast relaxation time of $\tau \approx 10^{-12}s$. Hence, the observed noise spectrum is independent of frequency, where $S_A(f)$ is constant throughout the frequency range investigated. The voltage and current notation for the noise power spectral density are conventionally expressed as:

$$S_V = 4k_B TR - (2.8)$$

$$S_I = 4k_B T/R - (2.9)$$

where k_B is the Boltzmann constant, T the device temperature and R the effective resistance of the device investigated.

2.3.2 Shot Noise

Shot noise is described as the random tunnelling of a free carrier (electron) through a potential barrier, which is commonly found in devices with a space-charge region formed by a p-n junction or a Schottky contact. It is a non-continuous process, where the noise current is discretely generated as the electrons travel across a potential barrier randomly and independently. The fluctuation mechanism for shot noise is closely correlated to that of thermal noise, except that the resulting noise current only flows in one direction; hence the resultant $S_A(f)$ has a value which is half of the thermal noise. Similar to thermal noise, shot noise is independent of frequency due to short electron transition process and current power spectral density can be expressed as:

$$S_I = 2eI - (2.10)$$

here e is the elementary charge and I the corresponding leakage current flowing through the potential barrier.

2.3.3 Generation-Recombination Noise

Generation-recombination (G-R) noise arises from the random emission and capture of free carriers via defect structures or traps in a semiconductor, leading to the fluctuation of total carrier number or population. The G-R process can indirectly cause perturbations in mobility, diffusion coefficient, electric field, barrier height and space charge region volume, affecting the current conduction mechanism in the form of electrical noise. The simplest form of G-R noise is a band to band transition, which involves direct carrier hopping between the conduction and valence bands. In practice however, a fabricated electron device possesses inherent defects such as those related to the imperfect crystal growth, oxide interface, compound material interface, surface states, fabrication error or contamination. Therefore, these generated defects or impurities act as transitional point to facilitate the carrier G-R process between bands. The schematic representation of these mechanisms is presented in Figure 2.3.
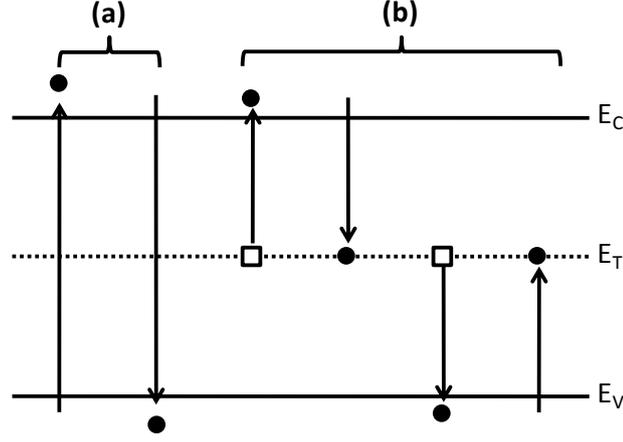
Figure 2.3: Generation-recombination mechanism for the a) direct band to band and b) four possible types of trap assisted carrier transition.

Whilst a practical trap assisted carrier transition may involve hopping through multiple energy trap levels, most G-R models only consider a single level transition for ease of explanation and mathematical representation. Unlike the thermal and shot noise, the interaction between the free carrier and a specific trap centre demonstrate a unique time constant, which defines the very characteristic of the observed noise spectrum such as the upper and lower cut-off frequency, frequency dependence of $S_A(f)$ (or the λ in the $1/f^\lambda$ noise function) and the presence of $S_A(f)$ in a specific frequency range. There are two distinct approaches that can be used to describe the noise spectrum of the generation-recombination mechanism. In the case of Langevin's method, the fluctuation in free carrier number as a function of time can be expressed as:

$$\frac{d(\Delta N)}{dt} = -\frac{\Delta N}{\tau_t} + H(t) - \quad (2.11)$$

where ΔN is the fluctuation in number of free carriers, τ_t the time constant of the corresponding trap species, and $H(t)$ the function of random noise fluctuation. The noise power spectral density can be derived based on the Langevin equation, which gives [28]:

$$S_{N_t} = \frac{4\tau_t}{1 + (2\pi f \tau_t)^2} \overline{\Delta N_t^2} - \quad (2.12)$$

here S_{N_t} is the carrier number noise power spectral density, f the frequency and $\overline{\Delta N_t^2}$ is average mean square of the carrier fluctuation magnitude. The noise components shown in Equation 2.12 is a representation of trap assisted carrier trapping and de-trapping from a single trapping state, known as a Lorentzian spectra. However the actual

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measured $S_A(f)$ is usually a sum of several discrete processes that are superimposed to form the distinctive noise spectrum throughout the frequency range investigated. It is worth highlighting that G-R mechanisms are also used to explain the manifestation of $1/f$ noise driven by number fluctuation and so it is ambiguous to define the G-R noise as an independent noise mechanism without linking it to LFN. This topic will be further discussed in the Section 2.3.5.

2.3.4 Random Telegraph (RTS) Noise

Random telegraph noise is caused by the random emission and capture of free carriers, similar to the fluctuation mechanism of generation-recombination noise. This electrical noise is also known as popcorn or burst noise due to the frequency signature that resemblances the bursting of popcorn. Unlike the G-R fluctuation caused by the carriers interaction with one or several trap species that share the same time constant, RTS noise is commonly due to a single carrier trapping and de-trapping action that leads to a large fluctuation in current conduction.

The random carrier G-R mechanism via a single (or multiple) trap energy induces a dual $(or\ 1 + no. of\ levels)$ of state transition, which causes the conductivity or resistance to switch between one level and another. Hence, the RTS noise is also an insightful technique to study the properties of a single trap species. Moreover, RTS noise is usually depicted as a fluctuation current or ΔI as a function of time (t), opposing the noise power spectral density versus frequency plot in G-R noise, where the typical RTS noise representation is analogous to a digital signal with random rise/fall time and period. An example of a typical RTS noise spectrum measured from a deep sub-micron MOSFET is illustrated in Figure 2.4. Based on the $\Delta I - t$ diagram in the figure, the $S_A(f)$ of the RTS noise can be derived and modelled as [29]:

$$S_{RTS}(f) \ = \frac{4(\Delta I)^2}{(\overline{\tau_h} + \overline{\tau_l})[(1/\overline{\tau_h} + 1/\overline{\tau_l})^2 + (2\pi f)^2]} - \ (2.13)$$

where $\overline{\tau_h}$ and $\overline{\tau_l}$ are the duration of the high and low states respectively. Similar to the previous noise mechanisms, Equation 2.13 only describes two state fluctuations to illustrate the characteristics.
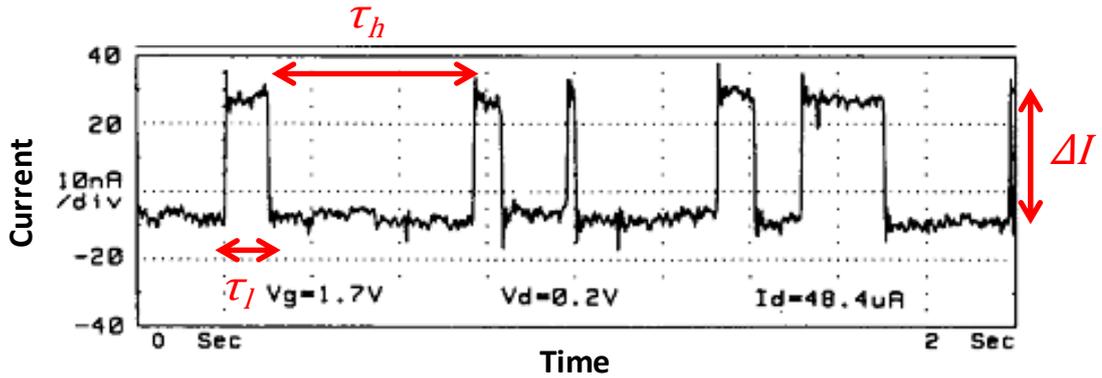
Figure 2.4: RTS noise as a function of time measured from a deep sub-micrometer MOSFET [30]**.**

2.3.5 Low Frequency Noise (LFN)

Low frequency noise, flicker noise or $1/f$ noise (due to the inverse frequency dependence) has been assumed as the fluctuation of conductance since its discovery until the phenomenon was finally verified by the Voss and Clarkes' experiment in 1976 [31]. This experiment demonstrated that the measured LFN shows a I^2 dependency if the driving current is kept constant and similarly the noise power spectral density follows a function of V^2 for fixed bias voltage. The square current/voltage function of $S_A(f)$ (Note that $S_A(f) \propto I^2\ or\ V^2$ since it is a power unit, following the P= $I^2R\ or\ V^2/R$ notation) implies that the applied external bias does not contribute to the measured voltage/current fluctuation; instead it enables the conductance perturbation in the device to be recorded.

Knowing the manifestation of LFN is due to conductance fluctuation of the material investigated, the parameter for n-type semiconductor can be described using:

$$\sigma = n\mu_0 e - (2.14)$$

here n is the electron concentration and μ_0 the mobility (Note that a similar P-type notation exist with a variation change in symbols). The next important question to ask is which parameter causes the LFN, whether that is a variation of carrier population or the fluctuation in the carrier mobility. The dispute between the number and mobility fluctuation theory has sparked a significant debate amongst the noise community, generating numerous research papers and numerical/empirical modelling each formulated specifically to encapsulate and theorise the different experimental findings. Hence, to date there is no universal model or mechanism that can be used to explain the observation of LFN, contrasting the standardised and well-established fluctuation

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mechanism and modelling for the other noise components. By comparing the results in the literature, it seems that the physical mechanisms that governed the LFN manifestation are somewhat unique to that particular experimental setup.

Although there were other hypotheses proposed to explain the fluctuation of LFN such as the quantum noise [18] and enthalpy variation (thermodynamics related) [11], only the classical number and mobility fluctuation mechanism are discussed in this section. Based on the number fluctuation theory, the LFN manifestation can be further described by the general G-R model for carrier trapping and de-trapping process via traps located in the mid-gap as well as surface state fluctuations that utilise the McWhorter model in metal-oxide-semiconductor (MOS) devices. In the case of mobility variation, there is the local interference fluctuation, where the electrons are scattered through mobile defects and the quantum based scattering that excite photons resulting in an unwanted perturbation when a charge carrier collides with the lattice. In most cases, there is a distinct numerical/empirical formula that models the observed noise power spectral density caused by these fluctuation mechanisms, which will be discussed in the following sub-section. As a general rule, the measured $S_A(f)$ can be described in a universal empirical formula, as shown in Equation 2.15, where such an expression is the fundamental noise model used in SPICE modelling, although there is very little physical representation of the actual fluctuation mechanism.

$$S_I = \frac{KF\,I^{AF}}{f^\lambda} - \ (2.15)$$

here KF is the magnitude of measured noise power spectral density, AF the current exponent, λ the frequency exponent typical found to be 1.0±0.1.

I. **Number Fluctuation**

The number fluctuation mechanism describes the variation of total carrier number in a material, which results in fluctuation of the current $\Delta I \propto (\Delta n)\mu_0 e$, leading to the observation of low frequency noise. This fluctuation mechanism is analogous to the G-R noise model, except all Lorentzian spectra produced by the carrier interaction with a single trap species is summed and the carrier time constant (lifetime) is evenly distributed across a logarithmical frequency spectrum, forming the distinctive $1/f$ dependence of $S_A(f)$. Given a Lorentzian spectra with a carrier lifetime between τ_1 and τ_2 as well as a statistical weight proportional to τ^{-1}, the density distribution of lifetimes or $g(\tau)$ for the generation-recombination (G-R) process can be expressed as [32], [33]:

$$g(\tau) = \frac{1}{ln(\tau_2/\tau_1)\tau} \ , for \ \tau_1 < \ \tau \ < \tau_2 - \ (2.16)$$

$$g(\tau) = 0 \ , in \ other \ case - \ (2.17)$$

The $ln(\tau_2/\tau_1)$ term is used as a normalisation function. By introducing $g(\tau)$ in Equation 2.12, S_{N_t} can be expressed as:

$$S_{N_t} = \overline{4\Delta N_t^2} \int_{\tau_1}^{\tau_2} g(\tau_t) \frac{\tau_t}{1 + (2\pi f \tau_t)^2} d\tau_t \ - \ (2.18)$$

Integration of Equation 2.18 yields:

$$S_{N_t} = \frac{1}{ln(\tau_2/\tau_1)} \frac{\overline{4\Delta N_t^2}}{2\pi f} (tan^{-1} 2\pi f \tau_2 - tan^{-1} 2\pi f \tau_1) \ - \ (2.19)$$

Based the lower, upper and band pass cut-off frequency conditions, S_{N_t} can be further estimated as follows:

$$f < 1/2\pi\tau_2 \, , \qquad S_{N_t} = \frac{\overline{4\Delta N_t^2}\tau_2}{ln(\tau_2/\tau_1)} \ - \ (2.20)$$

$$1/2\pi\tau_2 < f < 1/2\pi\tau_1 \, , \qquad S_{N_t} = \frac{\overline{\Delta N_t^2}}{ln(\tau_2/\tau_1)f} \ - \ (2.21)$$

$$f > 1/2\pi\tau_1 \, , \qquad S_{N_t} = \frac{\overline{\Delta N_t^2}\tau_1}{ln(\tau_2/\tau_1)\pi^2\tau_1 f^2} \ - \ (2.22)$$

The formation of $1/f$ noise spectrum through the contribution of multiple Lorentzian spectra is only possible if the carrier interaction with a specific trap species is separated among the other carrier generation-recombination process, where the different carrier hopping from one trap species to another is minimal. An example of the LFN spectrum produced by the summation of several discrete Lorentzian spectra of different traps energy/species, illustrated in Figure 2.5a. In the case where certain trap species dominate the conductance fluctuation process, the Lorentzian spectra generated by such process will be superimposed on the LFN spectrum, causing a distinct G-R bulge that disrupts the $1/f$ dependency of $S_A(f)$. An illustration this phenomenon is shown in Figure 2.5b.
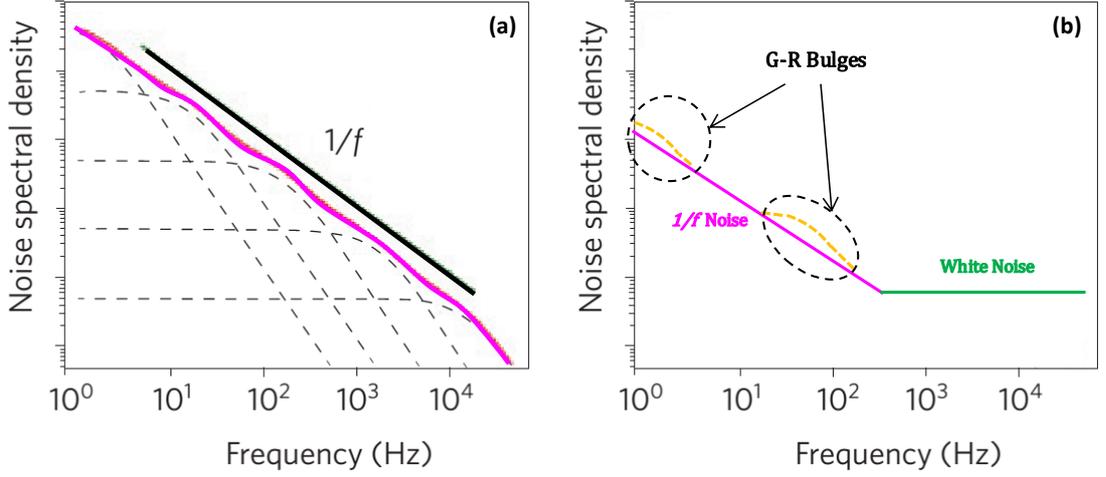
Figure 2.5: a) $1/f$ like low frequency noise spectrum composed of several Lorentzian spectral with evenly distribution carrier lifetime b) Example of generation-recombination (G-R) bulge when the Lorentzian spectrums of G-R origin is superimposed onto another $1/f$ noise component.

II. Mobility Fluctuation

The number fluctuation theory describes the variation in carrier mobility due to different scattering mechanisms or other indirect processes that leads to the scattering of carriers. Amongst all the mechanisms proposed in the literature, the Hooge empirical model is the most frequently used to describe the observed LFN spectrum for a wide variety of semiconductor devices, as well as the noise properties of an intrinsic material. Based on Hooge's original proposal, the measured current noise power spectral density (S_I) can be depicted as:

$$S_I = \frac{\alpha_H I^2}{N_0 f^\lambda} - \quad (2.23)$$

where α_H is the dimensionless Hooge parameter, which was initially presumed to be a constant, with a value of 2×10^{-3} but was later found to show a strong dependency with the crystal quality (inversely proportional to the defect density), I the driving current through the test structure, N_0 the total carrier number/population and λ the frequency exponent bearing a value of 1.0±0.1.

The LFN manifestation described by the Hooge model is considered to be the fluctuation of conductance arising from the lattice scattering of carriers and is strictly a bulk mechanism. Nevertheless, most reports published in the recent years utilise the Hooge parameter as a means of comparing noise performance for different processing techniques across a huge variety of materials. In some cases, the fluctuation mechanism

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that induces the observed LFN may not be related to the carrier scattering process and the analysis contradicts the noise results and properties reported previously. A discussion relating to the paradox and difficulty in direct application of such a model on a 2D material such as the graphene devices will form part of Chapter 6.

The other noise mechanism that falls in this category is the scattering cross-section variation due to the fluctuation of a single defect centre between two states based on the so-called "soft potentials" model [34], [35]. This type of fluctuation is related to the migration of individual or small groups of atoms between two-well potentials, and was initially thought to be only practical in low temperature systems, but the model was later expanded without temperature constraint [34]. The changes in this scattering cross-section arise from the capture and/or release process of charge carriers. Following the fluctuation theory proposed in this context, the current noise power spectral density can be described as:

$$S_I \approx \frac{N_{0i}(1 - N_{0i})I^2}{A^2} \frac{\tau_i}{1 + (2\pi f \tau_i)^2} (\sigma_a - \sigma_b)^2 - \quad (2.24)$$

where N_{0i} & $1 - N_{0i}$ is the equilibrium occupation number at the a & b defect states, $\sigma_{a,b}$ the effective scattering cross-sections for the a & b defect states, τ_i the relaxation time of the N_i trap occupancy and A the effective area for the test sample. Due to the nature of this fluctuation process, the τ_i term hence the formula given in Equation 2.24 is highly sensitivity with the sample temperature.

2.4 Impact of electrical noise

Electrical noise is one of the critical metrics in RF and analogue design, hence it is essential to study and understand such a phenomenon to reduce noise at the device level, as well as decoupling its effects from the corresponding on-circuit components. As semiconductor technology advances towards the miniaturisation of the active chipset dimension, operating voltage supply, power consumption and signal level, the presence of electrical noise that was once deemed to be non-detrimental to the circuit operation is becoming a critical issue that needs to be addressed. For instance, the demand in better sensing precision and the up-scaling of digital resolutions (even on the scale of the 4 bits to 8 bits transition), possess a technical challenge to accurately determine the deviations of the measurement with the further shrinkage of signal level, which is highly susceptible to electrical noise disturbances. To demonstrate the impact of electrical noise over functionality and performance of an electronic system, consider a

remote sensory system that has a sensor element, signal conditioning circuitry and a wireless communication module as shown by the schematic diagram in Figure 2.6.

Starting from the sensor node, the device associated electrical noise limits the accuracy and sensitivity of the sensor, where the white noise sources (thermal and shot noise) define the fundamental noise floor that restrict the down-scaling of the signal level and further refinement in the sensor resolutions. In an effort to maintain the signal quality, the raw sensor output is stringently required to be pre-amplified for further post signal processing or conditioning. Nevertheless, if the intrinsic noise of the signal processing module is not properly optimised, it will degrade the signal to noise ratio (SNR) of the amplified signal, which may affect the signal integrity and credibility of output results. Furthermore, the SNR of the module governs the minimum input signal level that can be recovered from the system noise [36]. Therefore it is imperative to design a preamplifier stage with small intrinsic noise, where such effort can be achieved by the careful selection of transistors and other components coupled with an impedance matching network.
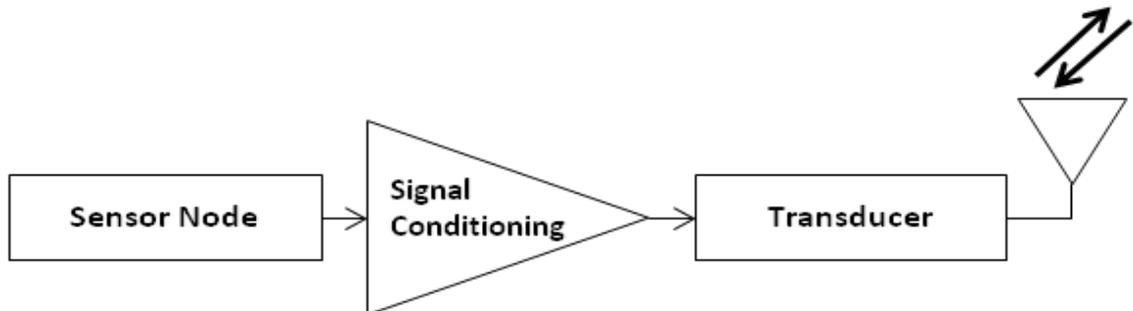
Figure 2.6: Schematic block diagram of a simplified remote sensory system.
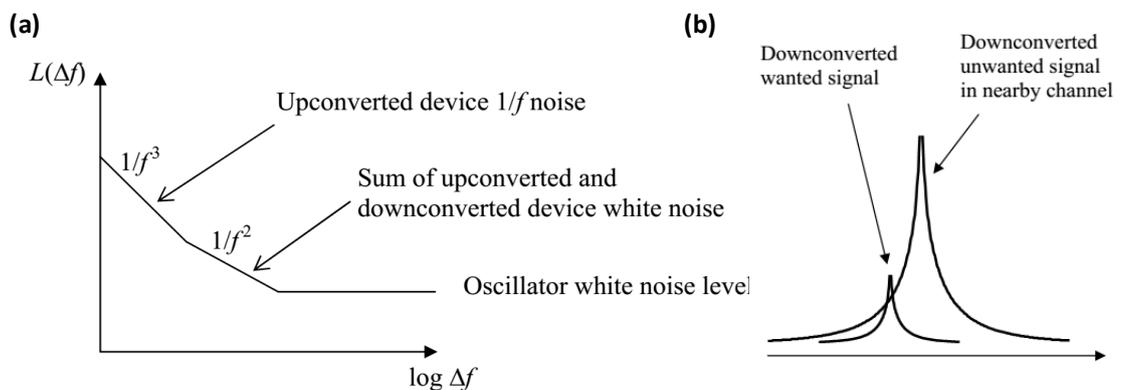
Figure 2.7: a) Schematic representation of the low frequency noise (LFN) up-conversion for the oscillator circuit. b) Impact of down-converted LFN in the form of phase noise in a receiver [32]**.**

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An assumption can be made that the sensor output is successfully amplified with excellent SNR and minimal distortion. This signal is then fed into a transducer for broadcasting of information to a remote monitoring system. A typical transducer has a voltage controlled oscillator that is composed of discrete transistors and an LC (inductor and capacitor) tank. Whilst, the LFN may seem to only dominate in the low frequency region, it can also affect the high frequency performance of transistor circuitry such as an oscillator. Figure 2.7b illustrates a schematic representation of the up and down conversion of an electrical noise (LFN and white noise components) and useful signal, where the phase noise is superposed close to the desired signal. The up/down conversion of $1/f$ and white noise elements will distort the output signal, manifesting in the of form phase noise [14], [17], which ultimately degrades the overall system SNR. The issue is exacerbated if both the receiving and transmitting end of the communication module has an inherent electrical noise performance that will further distort the transmitted/broadcasted sensor signal on the receiving ends. Hence, it is critical to ensure that the modulation channels are placed further apart from each other to lower the phase noise with a trade-off limiting capacity of transmitted information.

In a broad sense, the manifestation of electrical noise can only be reduced not completely eliminated, therefore it will always coexist with the useful electrical signal. Furthermore, the effect of electrical noise can be cascaded together especially in a multiple stage analogue module, thus further deteriorating the overall system performance. To illustrate the effect of cascading electrical noise in an analogue circuit, a multiple stage system analogous to those shown in Figure 2.6 is considered. The noise figure (NF) of the generalised single stage module can be expressed as:

$$NF(dB) = 10 \log F = 10 \log \left(\frac{SNR_{in}}{SNR_{out}} \right) - \quad (2.25)$$

where F is the noise factor, $SNR_{in,out}$ the input and output signal to noise ratio for the stage and the SNR is described as the ratio of signal power (P_s) divided by the noise power (P_n).

Considering a cascaded system, the noise factor of a particular n-th stage system denoted as F_n can be described as:

$$F_n = \frac{(P_s/P_n)_{n-1}}{(P_s/P_n)_n} = \frac{(P_s/P_n)_{n-1}}{G_n(P_s)_{n-1}/[G_n(P_n)_{n-1} + (P_n)_n]} = \frac{G_n(P_n)_{n-1} + (P_n)_n}{G_n(P_n)_{n-1}} - \quad (2.26)$$

here the terms with the n and n-1 subscript are the electrical parameters, which correspond to the current and previous stage respectively, and G_n, $(P_n)_n$ are the gain and the intrinsic noise power. By applying Equation 2.26 to a multiple cascaded system with a total number x stages, the effective system noise figure (NF_{sys}) can be described as:

$$NF_{sys} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_x - 1}{G_1 G_2 \dots G_{x-1}} - \quad (2.27)$$

2.5 Material and electrical properties of silicon carbide

Silicon carbide (SiC) has undergone a long history of development since the first accidental synthesis in 1824 by Jons Jacob Berzelius [37], where its applications range from the substitute of diamond abrasives tools [38] to the fabrication of the first light emitting diode (LED) in 1907 [39]. Nevertheless, the appraisal of SiC as a practical material for electronic switching devices has only begun to materialise in the past three decades, owing to the capability of synthesising wafers in large quantities with reduced crystalline defects. Because of the superior stability of the carbon–silicon bond, silicon carbide has been demonstrated as a suitable semiconductor material for the realization of electronics in conditions beyond those possible using conventional silicon technologies. The superlative material properties of SiC are especially useful in fabricating power electronics with improved switching capability, higher temperature operation and greater reverse voltage blockage, yet managing all these features on a 20 times smaller active device dimension in contrast to the conventional Si technology [40]. Although the SiC market share is mainly dominated by power electronics applications, the other prospective application of SiC electronics is the in the field of extreme environments such as space exploration, geothermal monitoring, oil and gas exploration or thermal/chemical reactor inspection, which require functional electronics at an elevated temperature and high radiation conditions.

2.5.1 Atomic structure and the different polytypes of SiC

SiC has a tetrahedral based configuration where the polyhedron is built on four triangular shaped planes formed by the four neighbouring carbon atoms with respect to a silicon atom. A schematic illustration of the example crystal lattice is shown in Figure 2.8. As the SiC unit cell is arranged with the adjacent SiC cells, it forms different atomic layer stacking, known configurations as the polytypes, which demonstrate distinctive material and electronics properties respectively, because of the unique

atomic configuration. To date more than 250 polytypes of SiC have been discovered [41], nevertheless only three are reproducible in large area wafers with acceptable defect densities for potential electronic applications. These are the 3C, 4H and 6H SiC, in which the 4H and 6H SiC polytypes are commercially and widely available. Hence, they are the most commonly used polytypes in SiC electronics fabrication.

The schematic cross sections in Figure 2.8a and b illustrate the typical crystalline structure of 4H and 6H SiC respectively. The changes in the stacking sequence of the Si–C bilayers (as highlighted by the dotted box in Figure 2.8) produce the variety in polytypes in the SiC material. Within the same bilayer sheet, each atom has a covalent bonding that is shared amongst other atoms in the same stack, while a single atom is bonded covalently with an adjacent (top/bottom) Si–C bilayer. In the case of the 4H-SiC polytypes, four stacking sequences known as the C-A-B-A bilayer configuration form a unit cell that is repeated in the <0001> c-axis stacking direction. Whereas, the C-A-B-C-B-A bilayer stacks that is reproducible in the c-axis direction define the fundamental structure of the 6H-SiC. These Si–C bilayers are also known as the basal plane and bilayer sheets with similar configuration (eg. A-A or B-B etc.) can never stack on top of each other. Due to the nature of a polar based material, SiC has an opposing surface termination along the c-axis. For instance, if the top surface is terminated by the Si atom known as the Si-face, the surface termination of the flip-side will always be the C atom denoted as the C-face or vice versa.
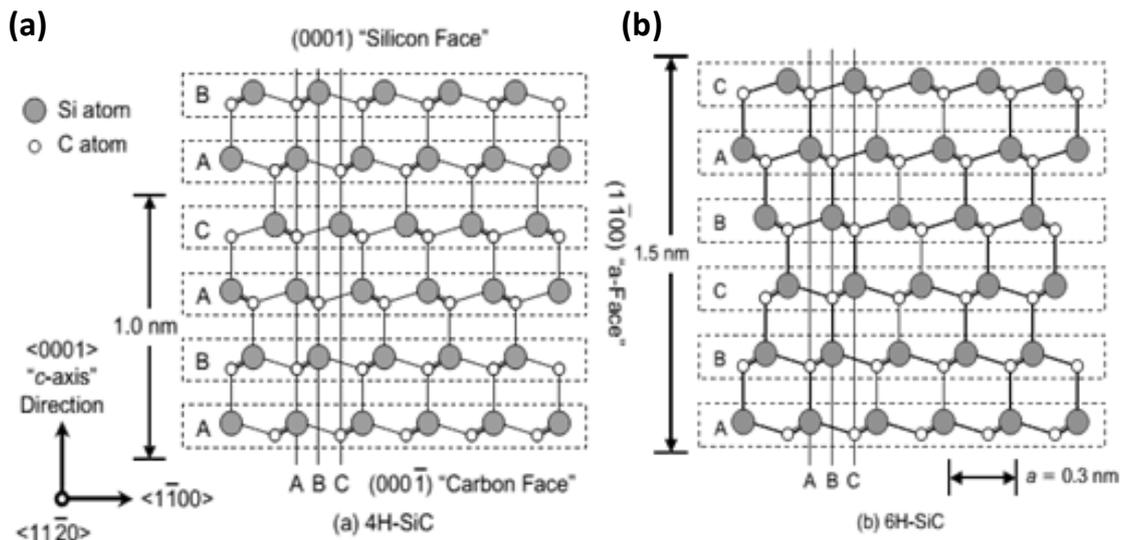
Figure 2.8: Schematic cross-section illustration of the a) 4H-SiC and b) 6H-SiC bilayer stacking sequence [40]**.**

2.5.2 Electrical properties of SiC

One of the deterministic factors that stimulate the extensive research and ensure the success in broad applications of a novel material is the superior properties it possesses over the existing Si and III-V semiconductors. Because of the unique Si and C bonding and the different stacking sequence of the Si–C bilayers, each SiC polytype demonstrates distinctive material properties that are useful in a specific field of application. A detailed comparison of the 3C, 4H and 6H SiC material properties in contrast to the other widely used semiconductor materials are shown in Table 2.1.

In comparison to conventional Si technology, SiC has 3 times greater energy gap, 3 times greater thermal conductivity, 10 times higher critical electric field and 16 orders of magnitude lower intrinsic carrier concentration at room temperature. These properties enable far higher operating temperatures than Si devices (a maximum 225°C of operation temperature of SOI technology [42], [43]), excellent susceptibility in radiation bombardment [44], [45] and high current density and blocking voltage for power electronics [46]. The electrical advantages of SiC offer opportunities for new design schematic design and circuit innovation in field of power electronic, extreme environments and high power communication system. Nevertheless, due to the nature of this research, only the applications in extreme environments are discussed in the following section.

Table 2.1: Comparison of electrical properties between 4H, 6H and 3C SiC against the industrial standard, Si, GaAs, Ge & GaN at room temperature [32], [40], [47]**.**

Properties	4H-SiC	6H-SiC	3C-SiC	Si	GaAs	Ge	GaN
Energy Gap (eV)	3.26	3.02	2.4	1.12	1.43	0.66	3.4
Critical Electric Field $N_D = 10^{17}cm^{-3}(MVcm^{-1})$	//c-axis: 3.0 $\perp$c-axis:2.5	//c-axis: 3.2 $\perp$c-axis:>1	1.8	0.6	0.6	0.2	2-3
Intrinsic Carrier Concentration (cm^{-3})	10^{-8}	$\sim10^{-6}$	~10	10^{10}	1.8×10^6	10^{13}	$\sim10^{-10}$
Electron Drift Mobility $N_D = 10^{16}cm^{-3}$ $(cmV^{-1}s^{-1})$	//c-axis: 800 $\perp$c-axis:800	//c-axis: 60 $\perp$c-axis:400	750	1400	6500	~3000	900
Holes Drift Mobility $N_A = 10^{16}cm^{-3}$ $(cmV^{-1}s^{-1})$	115	90	40	71	320	~2100	200
Saturated electron Velocity $(10^7\ cms^{-1})$	2	2	2.5	1.0	1.2	0.7	2.5
Dielectric Constant	9.7	9.7	9.7	11.9	0.5	16.2	9.5
Thermal Conductivity $(Wcm^{-1}K^{-1})$	3-5	3-5	3-5	1.5	0.46	1.6	1.3

2.5.3 Advantages of SiC in extreme environment applications

Owing to its wide band-gap and low intrinsic carrier concentration, SiC electronic devices are able to withstand a far higher operating temperatures than conventional Si devices and even outperform the temperature threshold of state of the art silicon on insulator (SOI) technology by twofold. These unique electrical properties enable SiC electronics to operate over an extended temperature range by preserving semiconducting behaviour, in contrast to other mainstream semiconductors where the intrinsic carrier concentration dominants the device conductivity over the intentionally engineered doping profile.

Whilst, theoretical prediction suggests a maximum operating temperature in excess of 900°C, analogue and digital circuit operation is limited to temperatures closer to 500°C in experimental demonstration [2]–[5]. This extended temperature capability enables the usage of SiC electronics in new engineering frontiers such geothermal well monitoring (>300**°C**), high temperature power electronics control (>350**°C**), high temperature sensing system (technology limited), passive/non-cooled high temperature electronics and so on, where the conventional Si and SOI technology is incapable.

Furthermore, the strong Si and C bonding of SiC make it a prospective candidate in radiation hardened electronics. The large displacement threshold energy of SiC results in 8 to 10 times more radiation resistance than Silicon and Gallium Arsenide, where a total 97eV of irradiation energy is required to knock out an atom from the crystal lattice [48]. This feature allows the engineering of radiation detectors with a better operating lifespan and fabrication of radiation hardened electronics for application in cosmic exploration, nuclear reactor monitoring and electronics system in satellites.

2.6 Graphene as an emerging material

Since its first discovery, graphene has generated enormous research interest in the field of material science, theoretical physics, chemistry and engineering because of its unique material properties that open up new frontiers of prospective applications. The distinct honeycomb configuration of carbon atoms, position graphene as the stiffest and strongest material known to man by its strength to weight ratio, demonstrating a Young's modulus of 1TPa and intrinsic strength of 130 GPa; yet it is the only crystal that can be elastically stretched up to 20% without breaking [49]. As a two dimensional material, graphene has an enormous surface to weight ratio that stands at 2630 m^2/g [50]

and illustrates an optical transparency of 97.7% [51]. Moreover, the electrical conductivity of graphene (1×10^6 S-cm) is superior to the best industrial standard such as Gold (0.45×10^6 S-cm) and Silver (0.63×10^6 S-cm) as well as having a thermal conductivity of 50 $Wcm^{-1}K^{-1}$. The record electron mobility in a graphene sheet, up to 200,000 $cm^2V^{-1}s^{-1}$ at room temperature is by far the best result currently known to man that is threefold better than the InSb at room temperature, with an electron mobility of 77,000 $cm^2V^{-1}s^{-1}$ [52]. By just considering the application of graphene in the field of electronics, these superlative properties have generated numerous reports in the literature such as novel transistor technology [53], next generation high electron mobility transistor (HEMT) [6], [54], ultra low noise transistor [55], [56], high selectivity sensing array [57], [58], part per billion grade sensor [59], [60], stackable 2D hetero-structure [61], THz grade detector and generator [62]–[65], resistance and quantum hall measurement standards [6], [66], [67] etc.

2.6.1 Atomic structure and electronics properties of Graphene

Carbon is known to have several allotropes due to the different form of hybridization of its valence orbital in the outer shell that resulted in the unique forms of carbon-carbon bonding. These carbon allotropes were sequentially found throughout the millennial starting from the 3D based Graphite in the 15th century, then the Fullerene as a 0D allotrope in 1985 prior to the discovery of the 1D carbon nanotubes in 1991. It was not until 2004 where the final form of 2D carbon allotrope known as graphene was synthesized successfully, completing the whole set of carbon allotropes in all known dimensionalities. The discovery of 2D graphene is not only worth investigating by itself due to the superlative properties, the material serves as a template to examine and understand the material properties of other carbon allotropes. Being the universal form of all carbon allotropes, when the graphene sheet is curled up systematically with introduction of pentagons forms the 0D Fullerene; while the sequential stacking (on top of each other) and rolling over of a single layer graphene creates 3D graphite and the 1D carbon nano-tube.

Graphene is a single atom thick material arranged in a basic hexagonal structure, where three out of the four valence electrons of the carbon atom are bonded with the neighbouring atoms in plane, forming the strong σ bond under the *sp²* hybridization and the other valence electron create a π bonding perpendicular to the plane. Two carbon atoms referred to as A and B are the basic building block that forms the graphene unit cell as illustrated in Figure 2.9a. The in-plane σ bonding between carbon atoms does not

contribute to the electron transport properties of the graphene sheet; instead it defines the remarkably strong and stiff mechanical properties of the material. On the other hand, the distinct electronic properties of graphene sheet are given by the π bonded valence electrons, and the delocalisation of electron π bands, where such bonding is formed as a consequence of the free electron oscillation perpendicular to the graphene plane, creating a P_z orbital that overlaps with other P_z orbital from the neighbouring carbon atoms. Utilising the tight-binding approximation, the electronic properties of the π band structure can be computed, as seen in Figure 2.9b.

The electronic properties of graphene are described by the distinct band structure shown in Figure 2.9b. As can be observed the results in the figure, the lower conduction (π) and the upper valence (π*) band illustrate a rather unusual pattern, where both the π and π* band converges at the K and K' point known as the Dirac point. The crossing of these 6 K and K' point pairs leads to the smooth overlying of the conduction and valence, exhibiting linear dispersion characteristics without creating an energy band-gap. In case of pristine graphene that is undoped, the Fermi level lies exactly at the Dirac point. It can be up (n type) or down (p type) shifted depending on the dopant species. Owing to the zero band-gap characteristics graphene demonstrates an ambipolar behaviour, where its charge carriers can be electro-statically modulated between electron and holes.
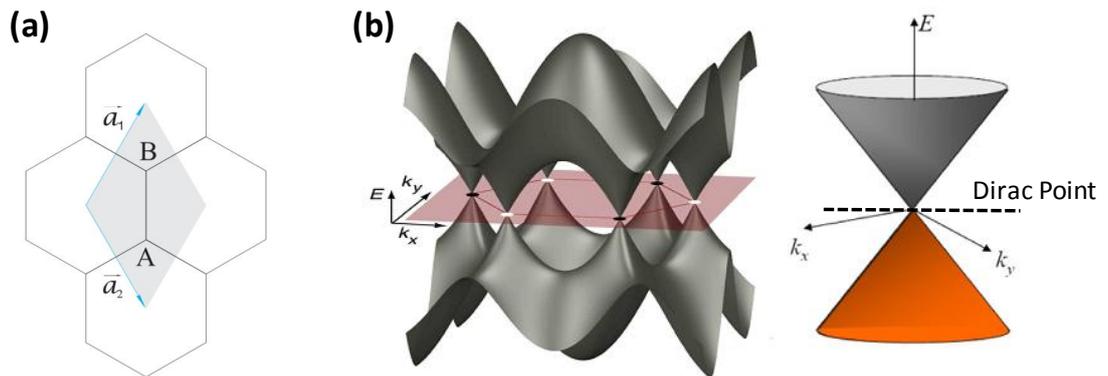
Figure 2.9: a) Basic building block of the graphene unit cell (shaded area) with unit vectors [68]. b) Electronic band structure of graphene computed using tight-binding approximation [69].

2.6.2 Graphene synthesis

Whilst, the material properties of graphene are superior to any known material to man, the triumph of graphene in the real world applications is heavily dependent on the ability to manufacture the material in large scale quantity with acceptable material quality. Many synthesis methods have been proposed to produce graphene film that can be potentially scaled up, such as liquid-phase exfoliation [70], [71], laser irradiated reduced graphite oxide [72], chemical vapour deposition (CVD) on metal [73], epitaxial growth (EG) from SiC substrates [74], [75], and molecular assembly etc [76]. Amidst of the vast number of proposed technique in the literature, only the graphene produced via mechanical exfoliation, CVD and EG are discussed in the following section, considering their scientific importance in graphene technology development and the maturity of the synthesis method in producing large format and good quality graphene sheets.

I. <u>Mechanical exfoliation</u>

Mechanical exfoliation is the most simplistic and ultra low budget method in producing a graphene flake that can be easily implemented in any clean room environment with the help of sticky tape and highly ordered pyrolytic graphite (HOPG). The method involves repeatedly exfoliating the graphite flakes that are peeled off from the HOPG before it is transferred over to a Si substrate with grown SiO_2 layer. Despite the crudeness in the synthesis process, ME graphene had generated the vast majority of valuable experimental studies ranging from elucidating and verifying the material properties to proof-of-concept for novel devices architecture. Although, the graphene flakes produced from this process are limited in dimension (up to a millimetre at best), irregularly shaped, uneven thickness (multiple atomic thickness may be produced) and their azimuthal orientation not controllable; however its unprecedented material quality is among the best and outperforms any other synthesis method to date. The record mobility up to 200,000 $cm^2V^{-1}s^{-1}$ and 20,000 $cm^2V^{-1}s^{-1}$ respectively were demonstrated at room temperature for single layer suspended graphene with current annealing [77]–[79] and regular graphene on a Si substrate [80]. Therefore, the combined features of low-cost production, high quality material, and rapid prototyping, position ME graphene as a suitable method for research activities but impractical for large scale industrial applications.

II. **Chemical vapour deposition**

Chemical vapour deposition is a promising method to produce a large format graphene film that can be up scaled indefinitely depending on the available dimension of the compatible catalytic metal substrate. Graphene synthesized through this method generally involves the deposition of carbon atoms from C containing gases (usually with the presence of methane and hydrogen carrier gases) onto the catalytic metal surface before the produced graphene sheet is transfer to another substrate via a complicated process. This involves spin-coating a layer of polymer (PMMA) to support the graphene sheet, then the catalytic metal is etch away and the graphene-polymer layer is transfer to an arbitrary substrate before the polymer is remove with a respective solvent.

Reports in the literature have shown that the catalytic metals used for CVD graphene growth include Pt, Cu, Au, Rh, Ir, Ni, Co, Ru, Ti, Hf, Zr and Ta [81]–[84]. However, either the quality of synthesized graphene are degraded due to the huge lattice mismatch between the catalytic metal and graphene [81]–[83] or the process is economically unviable owing to the non-reusable seeding substrate that is made of precious metal [6], [82], [84]. Cu is the most favourable catalytic metal amongst the investigated material because of the minimal solubility of C in Cu, showing >0.0001 atom% in contrast to Ni with 1.3 atom% at 1000°C [84], [85]. This contribute to the self-limiting feature on graphene grown on copper substrate, where the growth process is halted when the Cu substrate is fully covered, resulting in the synthesis of a conformal single layer graphene [85]. The first successful growth of large area (centimetre range) CVD graphene was demonstrated in 2009 on polycrystalline Cu foils by Ruoff group [73] and only after a year later a 30" roll to roll graphene production was reported [86]. The mobility for the CVD grown graphene is typically in the range of 1000 to 7000 $cm^2V^{-1}s^{-1}$ measured at room temperature.

Whilst, the CVD method can potentially be used to synthesised very large area graphene sheets with a comparatively cheap production cost and acceptable material quality for industrial usage, there are plenty of underlying issues that need to be addressed before this technology can be widely industrialised. For example, the wrinkling of graphene film due to the large thermal expansion coefficient between graphene and Cu [87], the requirement of transferring the grown film to arbitrary substrates [6], [73], [82], [84], the photo-resist contamination from the supporting polymer [88] as well as the mechanical damage induced during the transfer process [84]

can potentially hamper the electrical characteristics of the final transferred graphene sheet. In addition, the non-reusable catalytic metal and the stringent growth conditions with complicated transfer process may strain the production cost for graphene sheet synthesized via this method. Nevertheless, if these problems are rectified, the CVD grown graphene can serve as a prospective industrial standard for large format, cost effective and high quality graphene product for practical applications.

III. <u>Epitaxial growth from SiC substrate</u>

Epitaxially grown graphene on SiC substrate is another promising means to produce a high quality graphene sheet on a wafer scale that has a natural supporting substrate for in-situ fabrication without the need of film transfer. The up-scaling of the epitaxial graphene dimension is completely dependable on the availability of SiC substrate, where up to 6" of graphene substrate can be produced from the commercially obtainable SiC substrate at this instance [89]. Synthesis of the epitaxial graphene involves pre-growth surface reconditioning by etching off the polishing damage of SiC substrate in high temperature H_2 filled environment before the Si atom is sublimated from the SiC surface in ultra-high vacuum (UHV) or N_2/Ar_2 filled environment, where the graphitised SiC surface undergo some form of surface reconstruction, forming the graphene layer [74], [84], [90].

Graphene can be epitaxial grown on both the C- and Si- faces of SiC substrate with different polytypes, which results in diverse physical and electronic properties of produced graphene sheet. Moreover, the off-cut angle of the SiC substrate from the grown ingot was recently demonstrated to significantly affect the surface morphology of synthesized graphene, and thus the material and electrical properties of EG due to different surface profile such as terrace width and channel orientation that disrupts the carrier mean free path of the device channel [91]. Although, the first epitaxial graphene was grown on the C-face of SiC, due to higher reactivity of sublimation process, then leads to the least controllable grown graphene layer and randomly oriented polycrystalline layers [84]; EG synthesized on the Si-face SiC substrate has becoming more favourable over the years. Nevertheless, the electrical properties of EG synthesized from the C-face SiC wafer illustrate unprecedented characteristics, where mobility in the range of 10,000 to 30,000 $cm^2V^{-1}s^{-1}$ (approximately 15 fold higher than the graphene sample grown on Si-face) with $\sim 0.5 \times 10^{13} cm^{-2}$ of p-type carrier concentration was achieved. The choice of SiC polytype has a significant impact on the characteristics of resultant EG. In the case of 4H-SiC (0001) 60% of the wafer surface is

cover in monolayer, while the remaining surface is composed of bi-layer and tri-layer graphene. For the 6H-SiC (0001) and the 3C-SiC (111), the surface coverage of monolayer increases progressively from 92% to an astonishing 98%, illustrating the high compatibility of 3C-SiC for good quality EG production [92].

Unlike the EG grown on C-face, the Si-face EG has some fundamental differences on the stacking properties and the graphene to SiC interface. During the high temperature sublimation process, the residue carbon atoms left over from the sublimated Si undergo a $(6\sqrt{3} \times 6\sqrt{3})R30$ surface reconstruction, forming the very first C atomic layer subsequent to SiC stacking known as the "buffer layer" or "interfacial layer". These reorganised C atoms exhibit an isostructural similarity to graphene except the characteristic sp^2 bonding and are covalently bonded to the underlying SiC stacking. Hence, it does not illustrate any electronic characteristics of graphene. With further sublimation of Si atoms, new buffer layer is formed underneath the original buffer layer, leading to the simultaneous conversion of this initial $(6\sqrt{3} \times 6\sqrt{3})R30$ C layer into a monolayer graphene. A schematic illustration of the graphene atomic arrangement with increasing layer thickness and the corresponding TEM imaging is illustrated in Figure 2.10.

Careful regulation, formation and conversion of these buffer layers enables a precise control of the intended graphene thickness. However, the sublimation rate of the Si atoms drastically reduces with subsequent formation of each additional graphene layer, owing to the increasing resistance of Si atoms out-diffusion where free atoms can only escape through the defects in graphene, the SiC terrace edge and/or the sample edge. Despite the capability in regulating grown graphene layers, the buffer layer of the EG grown on Si-face SiC has unintentionally n doped the graphene film [93] as well as inducing a strong temperature dependency of film mobility [94]. The typical sheet carrier concentration of the single layer graphene sheet grown on Si-face of SiC is in the range of $8 \times 10^{11} \text{cm}^{-2}$ to $1 \times 10^{13} \text{cm}^{-2}$, demonstrating a room temperature mobility between 700 to 2000 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for EG grown in an Ar environment. The interface between the buffer layer and SiC substrate also was demonstrated to be breakable with 700°C thermal annealing in H_2 environment repeatedly, significantly decoupling the characteristics induced by this interface layer, where the carrier mobility is improved significantly with the removal of SiC/graphene interface that act as additional scattering sites [90].
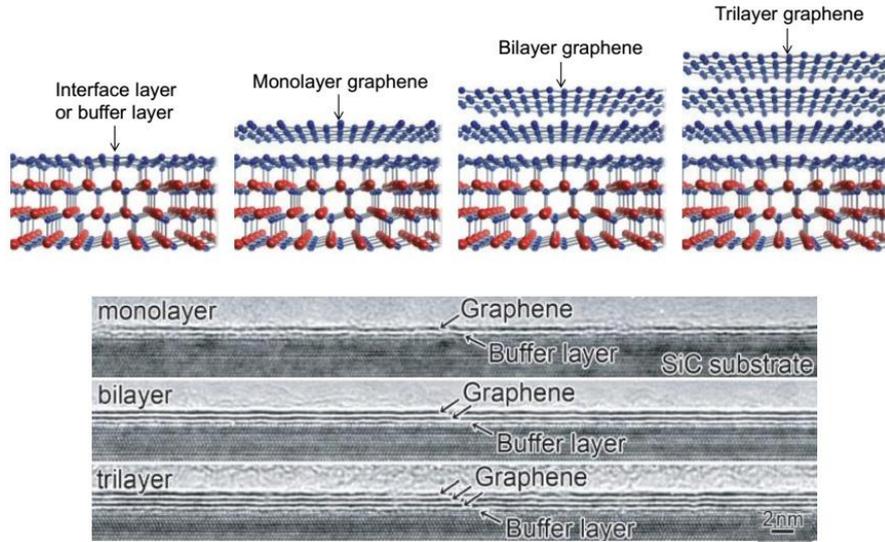
Figure 2.10: Schematic illustration of graphene-SiC interfacial layer, monolayer, bilayer and trilayer graphene sheet grown on the Si-face of 6H-SiC wafer with different atomic thickness and the corresponding TEM imaging [95]**.**

Although, the EG sheet synthesized from the SiC substrate exhibits plenty of remarkable properties in comparison to the other growth techniques, for example the excellent film quality, conformal graphene layer, wafer scale production with excellent run to run reproducibility and repeatability and in-situ readiness for device fabrication without the requirement for material transfer. The high substrate cost and stringent growth environment at high temperature may limit its application to only the niche market, thus undermining the EG potential in large scale consumer grade electronics production. Although the formulation of new solutions such as the reuse of the SiC substrate for graphene synthesis, graphene grown on compound SiC epitaxy on Si, fall of SiC substrate price and/or availability of larger SiC substrate will enable wider adaptation of EG in commercial grade or general purpose electronics application. The current EG technology still triumphs in the field of highly specialised electronics (eg: Terahertz grade and ultra low noise transistor, Terahertz detector/generator etc.), where the unique material characteristics outweigh the production costing. In this thesis, the investigated graphene transistors were fabricated using single layer EG grown the Si-face of 6H-SiC.

2.7 Device technology for SiC and graphene

In this section, the variety of transistor technologies developed for the SiC and graphene material are discussed. Fundamentally, most transistor technology on these materials is derived from the conventional Si technology, owing to the compatibility in fabrication processes as well as good understanding of the device physics and operation.

For SiC technology, the discussion is focussed on the device for hostile environment system, where the advantages and drawbacks of a particular SiC transistor technology are presented. In the case of graphene devices, although there are newly proposed transistor structures such as the tunnelling field effect transistor [96], only metal oxide gated transistors are considered due to the relative maturity in the transistor technology and extensive coverage in devices physics and operation.

2.7.1 MOSFET

The metal-oxide-semiconductor field effect transistor (MOSFET) is perhaps one of the most widely recognised transistor technologies in the field of electronic engineering because of its vast influence and application in the modern semiconductor industry. The voltage-controlled conduction, high switching speed, low standby power and superior integrated function are the attractive features for the MOS transistor technology, that has fuelled its wide spread industrial application. The MOSFET works on the principle of creating/diminishing a conduction channel by inverting the polarity of a doped semiconductor to allow/prevent carrier conduction between the two ends of the channel electrodes (drain and source).

The U-shaped groove MOSFET (UMOSFET) and the Double-diffusion MOSFET (DMOSFET) structures were commonly found in SiC technology (See Figure 2.11); where the former suffers from an irregular gate oxide layer (uneven oxide thickness on side wall and lateral channel) and field crowding at the gate corner, while the latter eliminates the concern of oxide growth issue but requires additional ion-implantation process to define the active device structures that may damage the implanted area and the high activation annealing temperature may exceed the fabrication thermal budget [97]. Despite of all the aforementioned electrical advantages, the thermal oxide grown on SiC exhibits an inherent poor oxide quality, with large interface trap density. The situation is further compounded when the transistor is required to operate at high temperature. This phenomenon resulted in threshold voltage (V_T) instability, where a -14mV/°C of degradation in V_T is demonstrated [98]. Unless new, better dielectric deposition or growth techniques are devised, the usage of SiC MOSFET for hostile environments will remain out of reach in the short to medium term.
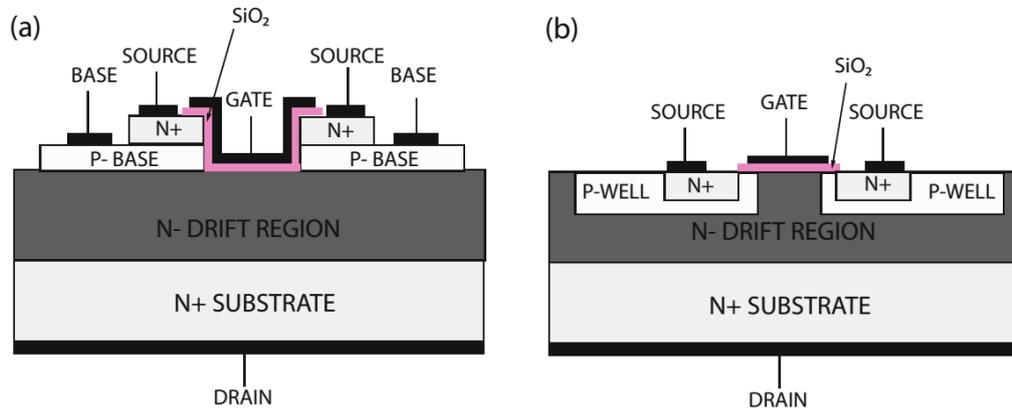
Figure 2.11: Schematic illustration of the a) U shaped (U) and b) double-diffusion (D) metal oxide semiconductor field effect transistor (MOSFETs) [97]**.**

2.7.2 MESFET

The metal semiconductor field effect transistor (MESFET) is renowned for its fast switching capability, where it is commonly found in RF and high frequency applications. The MESFET operation utilising a similar principle to the PN junction, where the depletion region is transposed perpendicularly to the conducting channel for current regulation and the PN junction is replaced with a Schottky barrier. A schematic representation of a MESFET is illustrated in Figure 2.12. The SiC MESFET is highly desirable for the ever increasing demand in power RF devices, owing to its fast switching speed, high current density and does not require the aid of active cooling mechanisms as opposed to conventional III-V and Si devices that are limited at 300°C. Whilst, device operation up to 500°C was reported on the SiC MESFET, the relatively low barrier height of the Schottky contact causes a large gate to channel leakage current [4], [97], restricting the application of this transistor technology in high temperature environments (no more than 400°C).
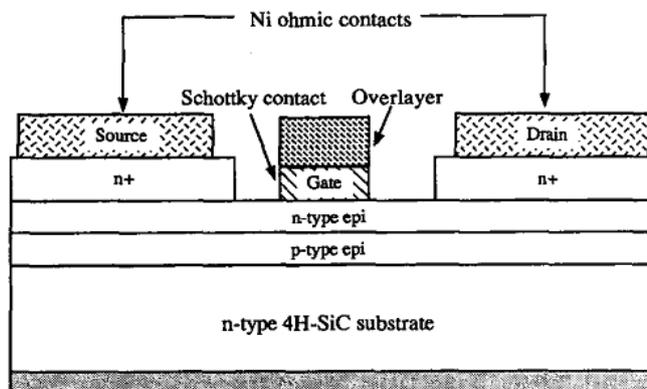
Figure 2.12: Schematic cross-section of a 4H-SiC epitaxial metal semiconductor field effect transistor [99]**.**

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2.7.3 BJT

The bipolar junction transistor (BJT) is one of the earliest forms of transistor technology proposed during the dawn of the semiconductor era. Because of the operating nature of the BJT, that involves minority and majority carriers, it is a relatively slow switching device where up to 20kHz of switching speed was demonstrated [97]. A schematic representation of vertical BJTs derived from using implanted and epitaxial fabrication techniques are shown in Figure 2.13. As a power electronic device, the SiC BJT shows an excellent tolerance in breakdown voltage and is typically considered for beyond 3kV operation. In the case of high temperature applications, the on-state performance of a BJT is considered to be better than other transistor technology [100], which minimise the turn-on losses hence the overall switching losses. Nevertheless, the low lifetime of minority carriers at elevated temperature, strenuous reproducibility in device characteristics, stringent requirement for high quality ohmic metal contact and the twofold degradation in current gain between room temperature and 250°C operation, rule out the practicality of SiC BJT in high temperature applications.
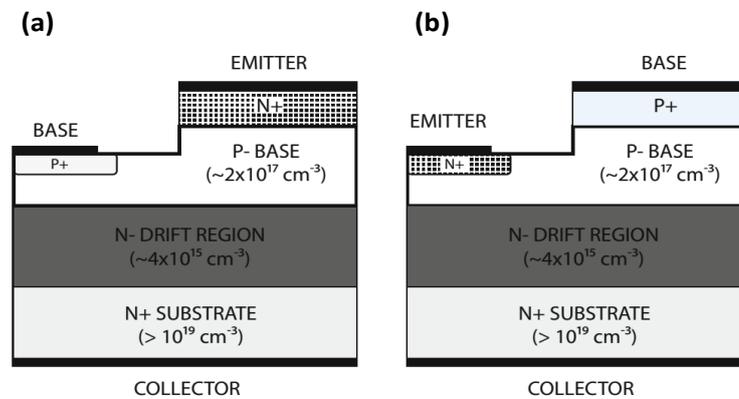
Figure 2.13: Schematic illustration of the a) implanted and b) epitaxial (right) bipolar junction transistor (BJTs) [97]**.**

2.7.4 JFET

The junction field effect transistor (JFET) is widely used in analogue circuit design, owing to the high input impedance, voltage controlled operation and low intrinsic noise nature. The transistor operation is analogous to a MESFET but instead of using Schottky barrier as a means of channel modulation it is replaced with the space charge region of a PN junction. (See Figure 2.14 for the schematic representations of JFETs) This implementation removes the need of high quality gate dielectric oxide for stable device operation and the enhanced built-in potential elevates the maximum

operational temperature of the transistor with minimal gate leakage effects. Amongst all the device technology discussed previously, the SiC JFET is the most promising transistor structure to be implemented as the fundamental switching component in extreme environment applications.

Apart from the high stability in device operation, that offers a better predictability in high temperature transistor behaviour; the low intrinsic noise behaviour of the transistor, even at an elevated temperature, improves the overall system performance of the signal conditioning circuitry and reduces the manifestation of phase noises in RF based circuitry. In addition, the high energy band-gap of SiC material and the absence of an oxide gate dielectric suggest the operability of SiC JFET in an irradiated environment. Reports in the past have demonstrated that Si based JFETs exposed to a neutron fluence of $>3\times10^{15}$ cm^{-2} at room temperature are severely degraded; whilst owing to the wide-band gap and large breakdown properties of SiC, the combination of neutron fluence and 300°C operation on the SiC JFET illustrate almost zero variation in the device characteristics [101]. These findings imply an excellent resilience and suitability of the SiC JFET application in elevated temperature and highly radiated environments.
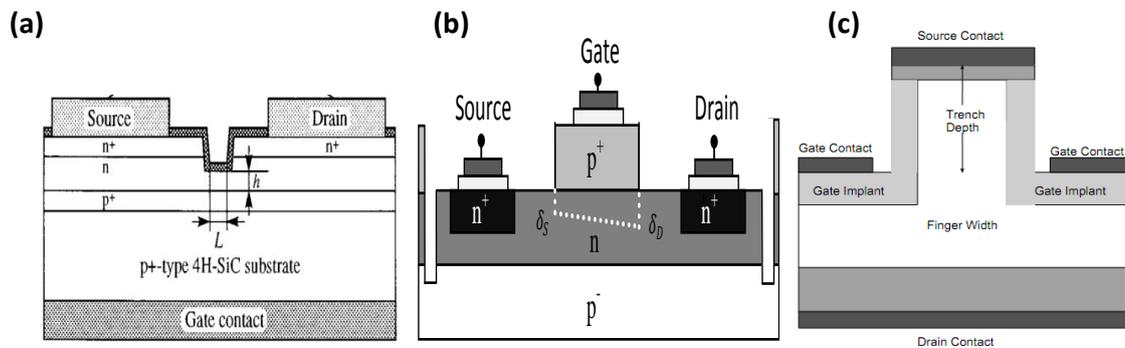
Figure 2.14: Schematic illustration of the a) planar with buried gate [102]**, b) epitaxial and c) vertical variances** [103] **of junction field effect transistors (JFETs).**

2.7.5 GFET

The graphene field effect transistor (GFET) is based on the adaption of the conventional MOS structure onto the recently discovered graphene sheet/flakes. The fundamental building components of a GFET are no different from any field effect transistor, which consists of the drain and source terminals, conducting channel (graphene sheet/flakes) and gate dielectrics for current regulation. The schematic illustrations of two GFET variant are shown in Figure 2.15. Following the different

synthesis method, the GFET may have an inherent back gate structure if the graphene sheet/flakes are transferred over to an arbitrary substrate or an additional top-gating structure is required to be deposited for the epitaxially grown graphene on SiC substrate. Whilst, the in-built back gated structure may offer a good level of current modulation, the relatively large gate regulation voltage (tens to hundreds of volts) render the incompatibility of this control scheme with modern electronics. Hence, the top-gate dielectric is usually integrated for enhanced transistor performance.

There are wide ranges of prospective applications proposed for the GFET, harnessing its superior intrinsic material properties such as the high frequency or RF transistor, transparent and/or flexible electronics, optical detector/generator and THz grade oscillator etc. Although the GFET is recommended as a means of replacement for CMOS technology, due to the zero or ultra narrow band-gap nature as well as the trade-off between the opening of band-gap and degradation in carrier mobility [6], the inherently low on/off ratio of this device can be an obstructive factor for the succession of the GFET in logic circuitry application. Nevertheless, the GFET triumphs in the case of high frequency and RF applications that do not mandate the total switch off of the transistor, turning into a potential substitution devices for next generation RF HEMTs.
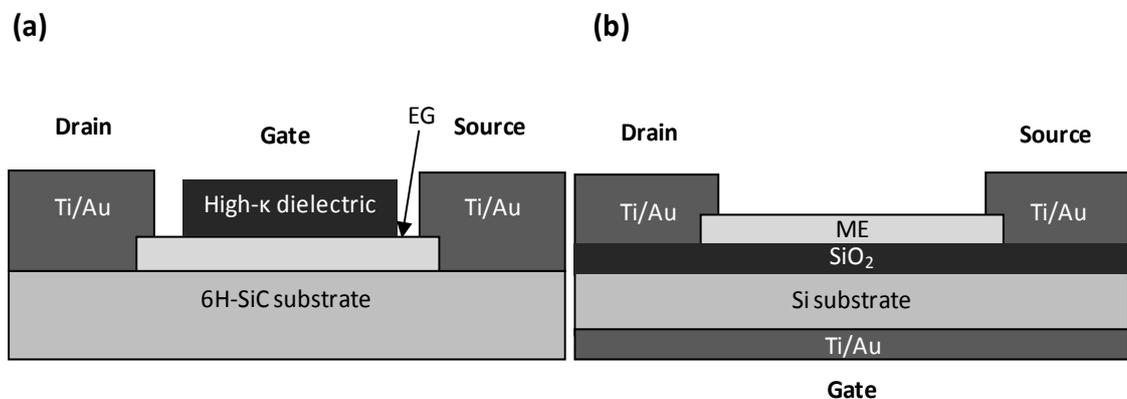
Figure 2.15: Schematic cross-section of the a) top gated epitaxial grown and b) bottom gated mechanical exfoliated graphene field effect transistor.

2.8 Electrical noise in SiC JFETs and graphene based FETs

The overall electrical noise of the transistor can be derived based on its small signal equivalent circuit. This analysis enables the detailed breakdown of each electrical noise component relating to its origin, where the influence of these noise sources can be individually summed. This can then be translated into the device equivalent current or voltage noise power spectral density based on the Thévenin or Norton configuration. In

this section, the noise components of the discrete SiC JFET and GFET are briefly introduced.

2.8.1 JFETs

Figure 2.16 shows the schematic illustration of the JFET small signal equivalent circuit coupled with the typical noise sources under the common-source configuration. As can be observed in the figure, $R_{D_{con}}$, $R_{S_{con}}$ and $R_{G_{con}}$ are the contact resistance of the drain, source and gate terminals correspondingly; while total drain-source channel resistance($R_{DS_{TOTAL}}$) is the sum of the resistivity component governed by the PN junction and the passive channel resistance (channel epitaxy) free from the influence of SCR, denoted as $R_{DS_{SCR}}$ and $R_{DS_{epi}}$respectively.

Whilst, these resistivity components are generally perceived to be governed by thermal noise, where the equivalent current noise power spectral density can be described by replacing the R term in Equation 2.9 with the respective resistance; An additional $1/f$ like behaviour is commonly superimposed onto the noise spectrum of these resistors as reported for thin film, intrinsic or doped semiconductor and metal contact structure etc when these components are characterised independently [12]. For ease of illustration and the fact that the device low frequency noise is usually dominated by the active resistance/conductance component, which in this case, is $R_{DS_{SCR}}$. The modelling of the $1/f$ component is embedded in the noise expression of $R_{DS_{SCR}}$ and the corresponding S_I can be described in Equation 2.28.
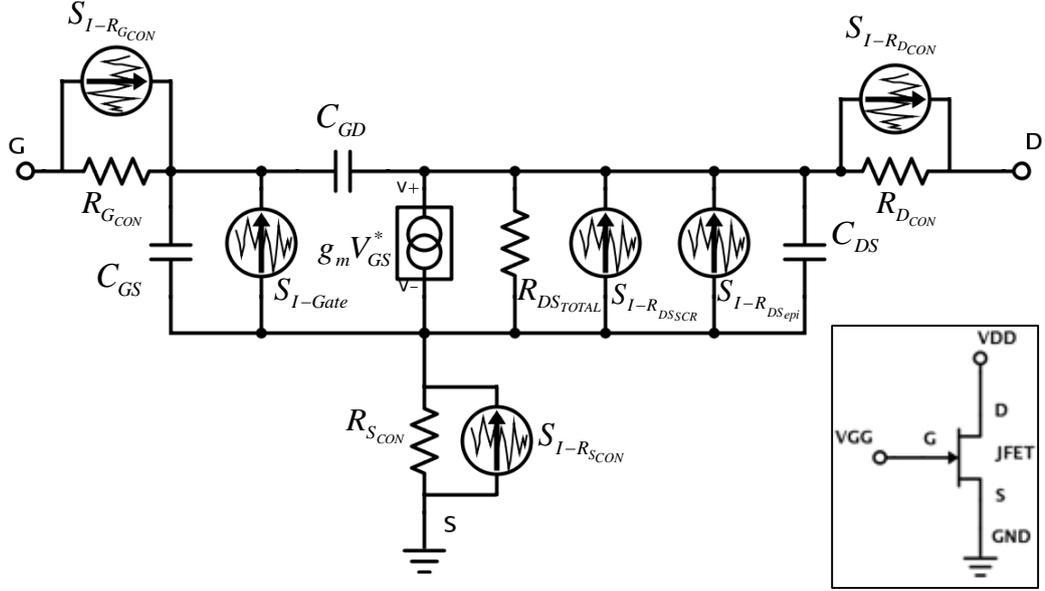
Figure 2.16: Small signal equivalent circuit and typical device level noise sources (excluding external biases and components coupled to the transistor) for the junction field effect transistor (JFET) under common-source configuration. Inset in the figure illustrates the JFET bias configuration.

$$S_{I-R_{DS_{SCR}}} = \frac{4k_B T}{R_{DS_{SCR}}} + \frac{\alpha_H I^2}{N_0 f^\lambda} - \quad (2.28)$$

here the 1st term on the right describes the thermal noise of the $R_{DS_{SCR}}$,while the 2nd term demonstrates the overall $1/f$ noise component that dominates the JFETs. Although the Hooge expression was used to represent the low frequency noise component in this example, in practice however it can be any noise sources that causes the $1/f$ or Lorentzian like behaviour and maybe even an unique model that is explicitly tied to a certain transistor technology (eg. McWhorter for Si MOSFET or Generation-recombination for GaAs HEMT).

In the vicinity of the transistor gate and source terminal, a shot noise component may also be present due to the random tunnelling of electrons within the SCR formed by the gate-source PN junction as denoted by the S_{I-Gate} term in Figure 2.16. In reality, although the influence of this noise component is minimal due to direct correlation of S_I with the leakage current, it may dominate the transistor noise behaviour under certain bias conditions and must not be neglected. Furthermore, the inherent noise sources from the external gate biasing circuit or any previous electronics stage can be superimposed onto the gate terminal, degrading the overall transistor performances as discussed in Section 2.4.
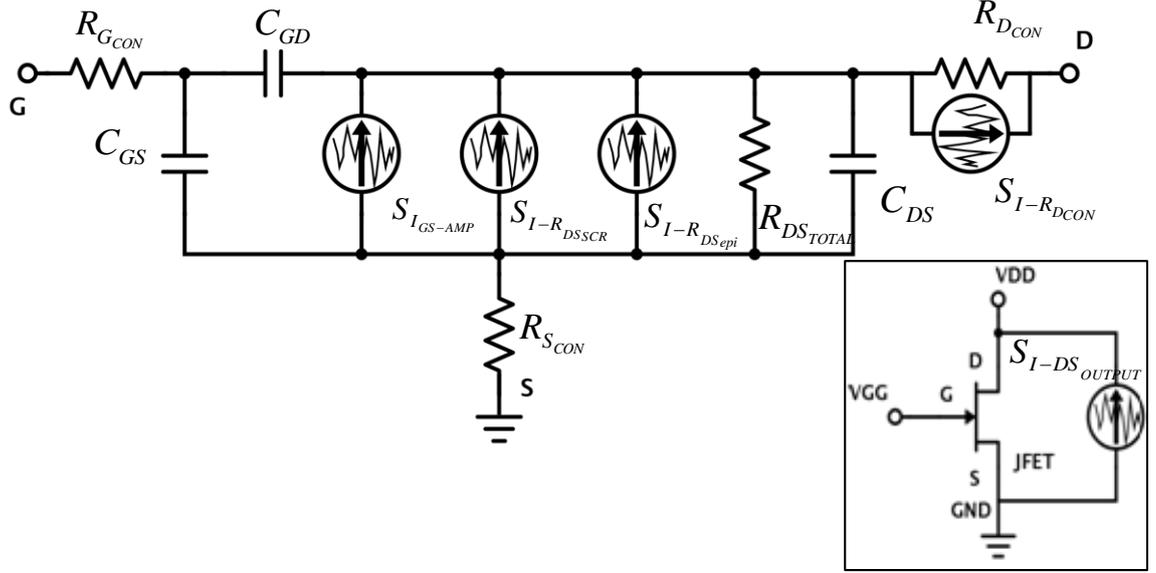
Figure 2.17: The modified small signal equivalent circuit with the corresponding noise modelling for the junction field effect transistor (JFET). Inset in the figure illustrates a noiseless JFETs and the effective current noise generator.

Based on the small signal equivalent circuit, the noise components from the gate terminal can be transposed to the drain-source branch by assuming the effective gate-source voltage (V_{GS}^*) is equal to the sum of V_{GS} and the gate-source voltage noise ($S_{V_{GS-Total}}$), where $S_{V_{GS-Total}}$ can be expressed as:

$$S_{V_{GS-Total}} = S_{V-R_{G_{CON}}} + S_{V-R_{S_{CON}}} + S_{I-GATE}|Z_{GATE}|^2 - (2.29)$$

here Z_{GATE} is the effective gate-source impedance of the JFET. By considering only the noise components of the effective gate-source voltage, $V_{GS}g_m^*$ can be rewritten as the amplified current noise power spectral density, given by:

$$S_{I_{GS-AMP}} = V_{GS}g_m^* = S_{V_{GS-Total}}g_m - (2.30)$$

Following Kirchhoff's current law, the total output current noise power spectral density on the drain-source terminal can be described as the sum of the current noise generators on the drain-source node as shown in Figure 2.17, including the newly found $S_{I_{GS-AMP}}$ in Equation 2.30 which produces:

$$S_{I_{DS-OUTPUT}} = S_{I_{GS-AMP}} + S_{I-RDS_{SCR}} + S_{I-RDS_{epi}} + S_{I-R_{D_{CON}}} - (2.31)$$

The resulting small signal equivalent circuit and the noise modelling of a JFET are illustrated in Figure 2.17.

2.8.2 GFETs

The noise modelling of the GFET is identical to the JFET equivalent circuit with the exception of the shot noise component notably due to the MOS gate configuration and its homogenous active channel (non PN structure). Although there are two generally accepted low frequency noise behaviours identified in the GFET, here denoted as the V/Λ and W shape noise, nevertheless there is a lack of universal explanation or even an accurate noise model to encapsulate these characteristics. The authors of each noise report had formulated a distinctive noise model for explaining their own findings, for example Hooge's model is utilised to elucidate the V and Λ shape noise in monolayer and bilayer graphene, ʍ shape noise is described by the spatial charges inhomogeneity, V and ʍ shape transformation is related to the interchangeable long and short range scattering etc. We shall explore the low frequency noise properties of the GFET in the Chapter 6.

2.9 Summary

In summary, this chapter has presented the fundamental mathematical expression for quantising the electrical noise, before exploring the different variety of electrical noise sources that exist in an electronic device, where each source can be uniquely related to the transistor device structure. Two distinctive low frequency noise generation mechanisms, notably the mobility and number fluctuation theory with its associated noise models were then discussed along with the impact of electrical noise on the electronics system.

Next, the material properties and electronics structure of SiC and the advantages of SiC electronics for hostile environments were briefly covered. The material and electrical properties for single atomic layer graphene, which fuelled its emergence as a prospective material for countless of applications were discussed. Three commonly reported graphene synthesis methods, particularly mechanical exfoliation, chemical vapour deposition and epitaxial growth on SiC substrate were also presented.

The pros and cons of different SiC transistor technology as well as the rationale behind the choice of the JFET as a promising switching device in hostile environments were briefly explained in Section 2.7. The device structure of the MOS gated graphene field effect transistor was also presented. Finally, this chapter is wrapped up with the introduction of a small signal equivalent circuit coupled with the corresponding device level noise models for the JFET and GFET.

Chapter 3: Experimental

3.1 Current-voltage

The current-voltage (I-V) measurements were performed using a Keithley (Model 4200-SCS) semiconductor characterisation system denoted as Keithley 4200 hereafter with a pair of remote amplifier/switch (Model 4225-RPM) to allow the interchange of I-V and C-V measurements without physically rewiring the instrument. Kite ver.8.2 was used as the automated interface for hardware control and data acquisition. All DUTs (devices under test) were probed using a Cascade Microtech probing station (Model Summit 12000B-AP) attached to a DCP-HTR High-performance DC Parametric probe to enable high temperature characterisation (rated up to 300°C). The Cascade Microtech probing station was supported on an active air anti-vibration table.

The built-in I-V test routine for the specific device configuration (PN, JFET, MOSFET etc) from the Keithley Kite library were used for all current-voltage related measurements. In all cases, the I-V results presented in this thesis are an average from at least 2 consecutive measurements. In the event where the acquired I-V characteristics fail to meet the expected behaviour, the probe is usually repositioned onto another contact area and at least 3 appended data were obtained to verify the consistency before the I-V characteristics finally recorded. To enhance the accuracy of the acquired results, the acquisition mode of the Kite software is typically set to the "Quiet mode" (30% improved settling time between DUTs biases and parametric measurements to reduce the impact of parasitic capacitance) with 20 times of data sampling for each bias. For a detailed instruction and operating manual of the Kite software see the Keithley application guide [104], [105].

3.2 Capacitance-voltage

The instrumentation setup and test routine for the capacitance-voltage (C-V) measurements is identical to the I-V characterisation. A similar maintenance routine was performed on the Keithley 4200 with an additional measurement correction under the open and close circuit configuration executed at the beginning of each C-V measurement. Once the correction is completed, a confidence check was then performed to verify the rectified parameters before acquiring the C-V characteristics of the DUTs. These calibration routines are a built-in function of the Keithley Kite software package.

Refer to the application note and white paper release by Keithley for further characterisation tips and C-V corrections [106], [107].

3.3 Low frequency noise

The low frequency noise measurement were performed using an in-house designed, assembled and coded acquisition system inspired by the Agilent's $1/f$ noise system. The two-port noise power spectral density was acquired by first amplifying the electrical signal of the DUTs using a battery powered Standard Research SR570 low noise current amplifier (LNA), where the noise signal of the DUTs is elevated significantly above the system noise to prevent it from mixing into the background noise. Then, the amplified noise signal is fed into a SR760 fast Fourier transform (FFT) analyser to interpret the AC components of the fluctuating signal. The two terminal DUTs is powered by the SR570 programmable in-built voltage source, while the third terminal (usually the gate) is biased using a Keithley 2611 SMU coupled with a low pass filter for the noise isolation from mains. The on-wafer probing setup for the low frequency noise measurement is identical to the C-V and I-V characterisation. A schematic block diagram of the low frequency noise measuring system is provided in Figure 3.1.

The instrumental control and data acquisition for the LFN noise system is a semi-automated process performed by using a custom made code created using the National Instruments LabVIEW software package. For each noise measurement, the biasing conditions and the LNA setups were required to be configured individually using the custom made software. The sensitivity or gain (denoted as A/V) of the LNA has to be equal or less than the DUTs conductance in order to selectively amplify the noise signal of the DUTs above the system noise without saturating the amplifier. In addition, the built-in offset current on the amplifiers must be also equivalent or smaller than the DUTs driving current. This compensation current enhances the amplifier performance by minimising the feedback current that can create a virtual null at the amplifier input if it flows into the DUTs through the feedback resistance of the LNA [108]. For this application, the LNA is configured under the low noise mode and the band pass filter was used to eliminate any AC components outside of the 1 Hz to 100 kHz range.

The noise power spectral density of the DUTs is acquired between 0.97Hz to 100 kHz, comprising of 1600 data points acquired separately from 4 measurements each with 400 data points obtained at different frequency spans (eg. 195 Hz, 3150Hz and

50kHz) to improve the noise data resolution. Each of the acquired noise spectra was averaged at least 12 times (typically 15 times) with 0% of overlapping. The Hanning window function was selected as the signal processing method, which is the best available analysis scheme for the low frequency noise measurement in this configuration, exhibiting a better frequency resolution and spectral leakage. These parameters were the typical configuration for the FFT analyser used for all noise measurement in this thesis.

During the data acquisition routine, the background noise was first acquired by probing onto the unbiased DUTs prior to the actual noise measurement at the intended operating conditions to create a reference spectrum for comparison. Figure 3.2 illustrates the contrast of the noise power spectral density between the actual and amplified noise signal with reference to the background noise at room temperature. To enhance the signal integrity of the measured noise spectrum, the general rule of thumb is to ensure the amplified noise signal is several orders higher than the background noise as demonstrated in Figure 3.2a. In addition, a second noise spectrum is also acquired consecutively and compared against the first spectrum to identify any transient based abnormalities. These noise spectra should be identical and highly reproducible if the measuring conditions are optimum.

The acquired noise data is post-process using Excel spreadsheets with embedded formulas such as the correction of the amplified noise to its actual magnitude with respect to the LNA A/V, noise unit conversion (dB and A/Hz), mathematical manipulation and model fitting. The acquired voltage noise power spectral density from the FFT analyser is expressed as:

$$S_{V_{FFT-OUT}} = S_{I_{DUT}} * (V/A)^2, (V^2/Hz \text{ or } A^2/Hz) - (3.1)$$

where $S_{I_{DUT}}$ is the current noise power spectral density of the DUTs and A/V is the sensitivity of the LNA. Note that the sensitivity is squared as $S_{I/V}$ is a power unit. The inter-conversion of the dB and V^2/Hz or A^2/Hz unit can be achieved using:

$$S_{V/I - dB/Hz} = 10 \log(S_{V/I - V^2/Hz \text{ or } A^2/Hz}) - (3.2)$$

$$S_{V/I - V^2/Hz \text{ or } A^2/Hz} = 10^{(S_{V/I - dB/Hz})/10} - (3.3)$$

here $S_{V/I - dB/Hz}$ and $S_{V/I - V^2/Hz \text{ or } A^2/Hz}$ are the noise power spectral density in decibel and voltage/current unit correspondingly. To enable current or voltage normalisation, a

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separate set of *I-V* characteristics is usually obtained using the method described in Section 3.1 prior the low frequency noise measurement. This procedure also served as verification and screening process to remove any defective devices from the low frequency noise measurement due to fabrication errors.

In effort to reduce the uncertainty or magnitude span of the acquired noise power spectral density such as those shown on Figure 3.2, the measured LFN spectra requires to be averaged as many times as possible. Nevertheless, this implementation is impractical, time consuming and ineffective in practice, where the measuring time can totalled up to ten of minutes for a single measurement on a 100 averaging count. Therefore, a post fitting scheme on $1/f$ noise spectrum is introduced instead, where the noise spectrum between 0.1 Hz to 200 Hz is fitted using the least-squared method and all noise data reported in this thesis were based on the modelled results unless stated.
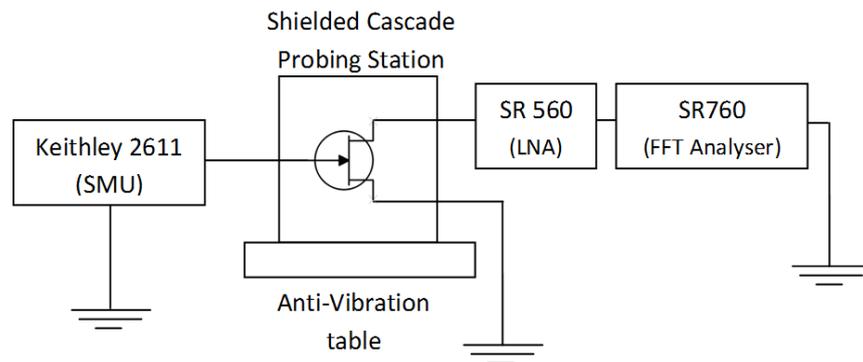
Figure 3.1: Schematic diagram of the low frequency noise measurement system.
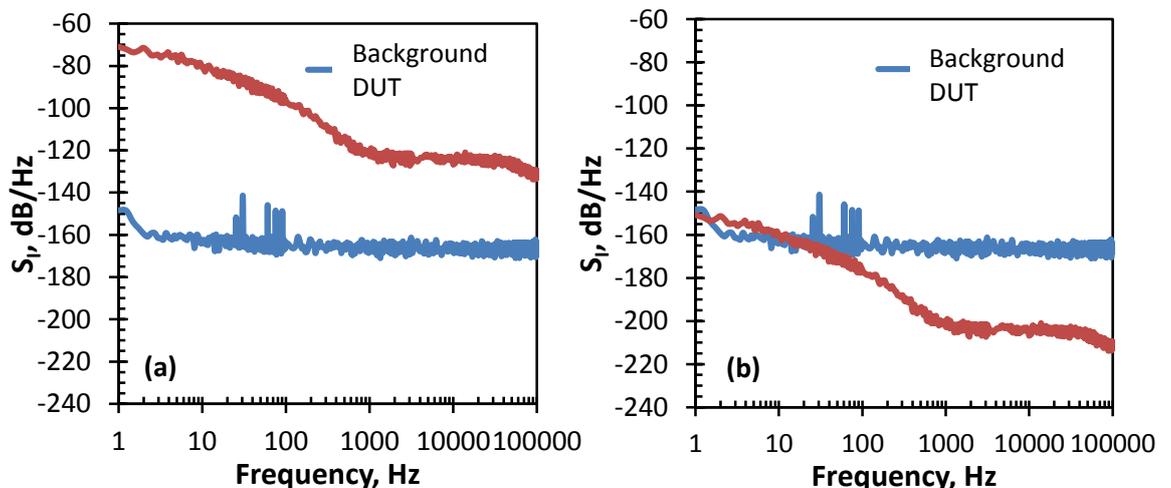
Figure 3.2: Noise power spectral density as a function of frequency for the a) amplified and b) actual low frequency noise spectrum of a representative device under test (DUT) with respect to the background noise at room temperature.

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3.4 Hall Effect

The hardware setup of the Hall Effect measurement was based on the commercially available MMR Variable Temperature Hall System with a custom measurement system assembled using a Keithley (Model 2000) Multi-meter and Keithley (Model 2611) single channel SMU. The on-chip DUTs prober was a home-made movable platform for sample loading and on/off field measurement with 4 sets of 20μm resolution manipulators made by Everbeing International Corp. using Tungsten tips. A reversible 5000 Gauss electromagnet (Model MK50) driven by a Kepco (Model BOP 50-8D) bipolar operational power supply was used to generate the required magnetic field for Hall Effect characterisation. All hardware control and data acquisition was achieved by custom coded programs, created using the National Instruments LabVIEW software package.

The Hall Effect measuring scheme was the adaption of the published procedure by the US National Institute of Standards and Technology and ASTM International ASTM F76-08 standard test method with some minor alteration [109], [110]. In a nut shell, the Hall Effect mobility can be extracted from the changes in Hall voltage with respect to the different degree of magnetic field (usually in opposite polarity) and the sheet resistivity (no field) of the corresponding DUTs. The operating principle of the Hall Effect is based on the Lorentz force as illustrated in Figure 3.3, where the electron moving along an electric field with an applied magnetic field perpendicular to its flow direction can experience a magnetic force normal to both directions. Assuming a constant current flow in the x-axis, the effective magnetic force applied (on the z-axis) on the DUTs can causes the drifting of the electron concentration to one side of the sample (y-axis) that can be determined using the right hand rule convention. This temporarily creates an excess positive surface charge on the opposite y-direction that results as the Hall voltage.

Conventionally, by knowing the effective sample current (I_{Bias}) and Hall voltage (V_{Hall}) under different applied magnetic fields with a unique 4 ports biasing configuration, the sheet concentration can be computed using:

$$n_{sh} = I_{Bias}\Delta B/e|V_{Hall}| - \quad (3.4)$$

where e is the elementary charge, ΔV_{Hall} the deviation of Hall voltage under different magnetic fields and ΔB the magnetic field difference. Nevertheless, the limited data point is highly susceptible to measurement error in practice that will result in exorbitant

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errors in the extracted Hall Effect parameters. To enhance the accuracy of the computed Hall Effect mobility, at least 5 sets of V_{Hall} are obtained between 2000G and -2000G of magnetic field strength to construct the $V_{Hall} - B$ gradient. This procedure was based on the assumption that the V_{Hall} of the investigated sample demonstrates a linear function with respect to the B within the 2000G range. This is commonly accepted for Si, SiC and graphene devices. Furthermore, the V_{Hall} were acquired under different source/measure configurations (typically 13/24, 31/24, 24/13 and 24/31, see illustration in Figure 3.4a. Note that the accuracy of the measured results may improve with increasing source/measure configuration matrix) based on 4/6 terminal van der Pauw structures. A typical example of van der Pauw variants were illustrated in Figure 3.4. Based on these assumptions, Equation 3.4 can be written as:

$$n_{sh} = \frac{I_{Bias}}{e} \frac{1}{n} \sum_{i=1}^{n} mHall_{ab,cd} - (3.5)$$

here n is the total number of source and measure configurations and $mHall_{ab,cd}$ the $B - V_{Hall}$ gradient under different source/measure configurations. Utilising the sheet resistivity (r_{sh}) of the DUTs extracted following the van der Pauw expression, $\exp(-\pi r_{sh} V_{43}/I_{12}) + \exp(-\pi r_{sh} V_{14}/I_{23}) = 1$ using the 4 terminal test structures, the Hall Effect mobility is given by:

$$\mu_H = (1/er_{sh}n_{sh})^{-1} - (3.6)$$
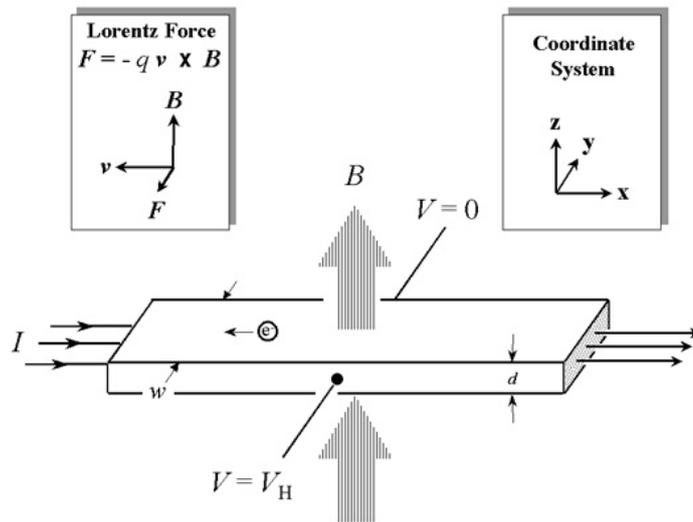
Figure 3.3: Schematic illustration of Hall Effect mechanism with its corresponding measuring parameter on a slab of semiconductor [109].
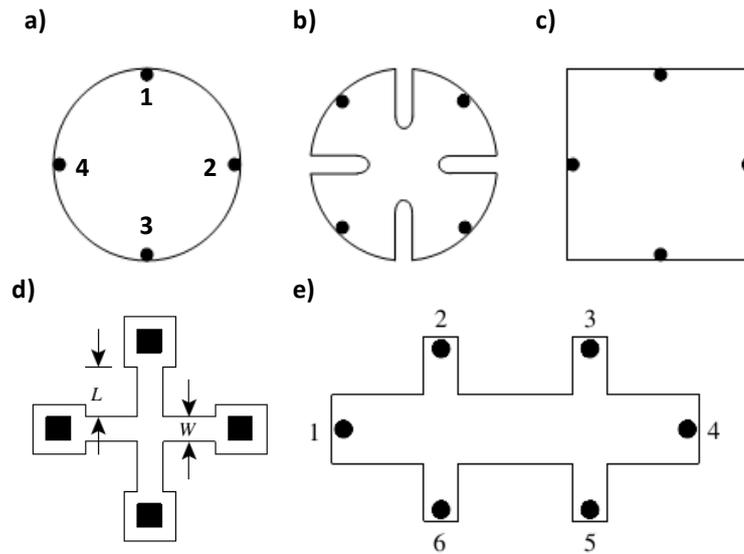
Figure 3.4: Schematic illustration of the a) symmetrical circular, b) cloverleaf, c) square/rectangle, d) Hall cross, and e) Hall bar/spider/bridge variants of Van der Pauw structure [111]**.**

For an improved user experience, the LabVIEW program was written to accommodate both 2D and 3D materials and the Hall Effect parameters were generated in-situ alongside the raw data for manual mathematical manipulation.

3.5 Summary

In summary, this chapter covers the instrumentation setups for all the measuring techniques such as current-voltage, capacitance-voltage, low frequency noise and Hall Effect characterisation, employed in this thesis. The measuring procedures were also briefly discussed in the chapter.

Chapter 4: Low Frequency Noise in 4H-SiC Epitaxial Junction Field Effect Transistor

4.1 Introduction

Silicon carbide has been demonstrated as a suitable semiconductor material for the realisation of electronics in conditions beyond those possible using conventional silicon technologies. Because of their unique material properties, SiC devices are highly desirable for high temperature, high power, high frequency and radiation hard environments. In theory, the intrinsic carrier concentration suggests a maximum operating temperature in excess of 800°C, while operation beyond 500°C has been demonstrated experimentally [2]–[5]. In addition, the radiation hardness of SiC devices has been shown to be significantly higher than Si devices [112], where only a minor degradation in the *I-V* characteristic of SiC FET was demonstrated at 600K in a neutron fluence of $1 \times 10^{15} n/cm^2$ [101]. The high thermal conductivity and superior breakdown electric field also make SiC suitable for use in power electronic applications [113]–[115]. Due to this combination of properties, SiC is becoming the material of choice for the realisation of electronic circuits in extreme environments such as space exploration, pollution monitoring, and aerospace [116]–[118].

In silicon-based technology, typical amplifier circuits are built using bipolar transistors, metal semiconductor field effect transistors (MESFETs), and metal oxide semiconductor field effect transistors (MOSFETs) as the active component. However, due to the high electronic trap density at the SiC-oxide interface of SiC-MOSFETs, the device threshold voltage (V_T) is unstable, where the trapping states lead to a significant drift in V_T as the bias conditions are cycled at elevated or even room temperature [119]–[121]. In SiC-MESFETs, the Schottky-barrier gate junction has a high leakage current during high temperature operation because of to the relatively low barrier height [4], [97]. Bipolar-transistor based amplifiers suffer from low input impedance in comparison to FET devices, as well as high intrinsic noise attributed to the current conduction mechanism.

Among the field effect transistor technologies, the junction field effect transistor (JFET) offers a viable solution to the challenges posed by other device structures. The current modulation mechanism, which is based on the evolution of a space charge region (SCR) of a p-n junction, improves the transistor built-in potential stability at high

temperature, resulting in a huge reduction in gate leakage current relative to MESFETs. Furthermore, the lack of an oxide interface layer removes the source of the threshold voltage instability, where a threshold-voltage shift of only 50 mV and a decrease in drain current of 7% has been observed for a device subjected to a thermal soak at 500°C for 1000 hours [122]. In circuit design, JFETs are well known in analogue applications because of their high input impedance and inherently low intrinsic noise, even operating at high temperatures [102], [123], [124]. All these unique characteristics make the JFET transistor highly favoured for the realisation of high performance analogue circuits, such as in front-end amplifiers/preamplifiers and oscillator circuitry for use in hostile environments.

Besides the excellent stability in DC characteristics, low frequency noise (LFN), also known as $1/f$ noise due to its inverse relation with frequency, is one of the critical design metrics for analogue circuits. Whilst, this type of electrical noise may seem to only dominate in the low frequency region, it can affect the high frequency performance of JFET circuitry. For oscillator circuits, LFN is up-converted to high frequency elements, distorting the output signal in the form of phase noise [14], [17]. In the case of operational amplifiers, the noise characteristics determine the signal-to-noise ratio of the transistor, which governs the minimum input signal that can be recovered without being buried into the system noise [36]. Therefore, it is important to study the low frequency noise characteristics of an electron device to understand the operational limitation as well as to optimise the transistor design.

Previous reports in the literature have reported the low frequency noise characteristics of SiC JFETs under different operational conditions [102], [125]–[128]. However, the noise investigations are solely based a homogenous transistor structure with identical gate geometry using high power buried gate JFETs, manufactured by Cree Inc. In addition, the low frequency noise origin in these reports is dominated by the carrier fluctuation process from the structure specific SiC-SiO$_2$ interface, which cannot be regarded as a generalised noise model for all SiC JFET, especially for those without a SiO$_2$ passivation layer in close proximity with the conduction channel. In this chapter, the low frequency noise behaviour of top-gated epitaxial signal-level JFETs, designed by the SiC electronic team (Dr. Konstantin Vasilleiky and Dr. Rupert Steves) in Newcastle University, were examined. The comparison matrices include the impact of transistor gate geometry and operating temperature on the JFET low frequency noise characteristics.

4.2 Experimental

Lateral JFETs were fabricated on the Si face of a 3" production grade 4H-SiC wafer purchased from CREE Inc. The wafer comprised three epitaxial layers, p^- (2×10^{15} cm^{-3}, 5 μm thick), n (1×10^{17} cm^{-3}, 0.3 μm thick), and p^+ (2×10^{19} cm^{-3}, 0.2 μm thick), as shown in Figure 4.1. Reactive ion etching was used to define the isolation cell between devices and a second etch step formed the lateral extent of the gate region. Nitrogen was implanted to a total dose of 1×10^{19} cm^{-2} in the n epitaxy to form the n+ source and drain region, followed by 1600°C activation anneal with graphite cap protection to prevent step bunching and dopant-out diffusion from the implanted region [129]. This enables the formation of low-resistivity ohmic contacts to the source and drain. A SiO$_2$ layer was grown at 1150°C under dry oxygen for surface passivation, and contact windows were opened by BHF etching. Ni/Si (n-type) and Al/Ti (p-type) metallisation was deposited and subsequently annealed using a Rapid Thermal Annealing process to form the ohmic contacts on the source, drain, and gate regions, respectively [130]. Au was then deposited on the surface and patterned using a lift off process, to facilitate wire bonding. The JFETs used in this study have gate lengths (L) of 9μm and 21μm with different gate widths (W) (perpendicular to diagram) of 200μm, 150μm, 100μm and 50μm.
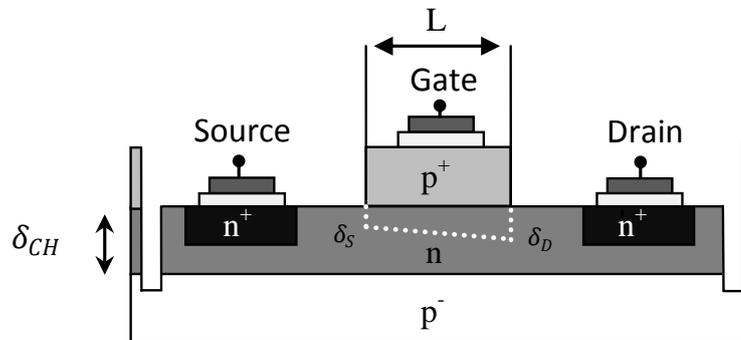
Figure 4.1: Schematic cross-section diagram of 4H-SiC epitaxial junction field effect transistor (JFET).

4.3 Results and Discussion

4.3.1 The influence of gate geometry on 4H-SiC JFETs

I. <u>Electrical Characterisation</u>

To investigate the influence of gate geometry on the JFET DC characteristics, the drain-source current (I_{DS}) of the investigated devices was normalised with the corresponding gate geometry (W/L) ratio. The *I-V* characteristics of these devices were presumed to follow the constant mobility model as described by the following equation [131]:

$$I_D = \frac{We\mu N_D \delta_{CH}}{L}\left\{V_{DS} - \frac{2}{3\sqrt{\Psi_P}}\left[(\Psi_{bi} + V_{DS} - V_{GS})^{3/2} - (\Psi_{bi} - V_{GS})^{3/2}\right]\right\} - (4.1)$$

here *e* the elementary charge, μ the carrier drift mobility, N_D the n-channel doping concentration, δ_{CH} the channel depth, Ψ_P the pinch-off voltage and Ψ_{bi} the built in voltage of the p-n junction.

The *I-V* data in Figure 4.2 shows the comparison of gate geometry normalised drain-source current ($I_{DS} L / W$) as a function of drain-source voltage (V_{DS}) between transistors with a gate length, *L*, of 9μm (filled line) and 21μm (dotted line) under three different gate width, *W*, configuration of a) 200μm, b) 150μm and c) 50μm. The gate-source voltage (V_{GS}) of the devices was biased from -3.0V to 1.0V with 1.0V increments. As can be observed from the *I-V* curve in Figure 4.2, there are some mixed results amongst the investigated JFETs. For transistors with *W* of 150μm, the $I_{DS} L / W$ characteristics of the two devices with different *L* coincide perfectly, while the normalised *I-V* data for transistors with 200μm *W* are slightly deviated from each other. In the case of 50μm gate width JFETs, the two transistors under comparison demonstrate a large variation in the *I-V* characteristic, notably on the 9μm gate length transistor where the current capability is significantly lower relative to all investigated devices. One possible scenario that may cause the discrepancy in the JFETs normalised *I-V* characteristic is due to the variation of the doping concentration and channel thickness (denoted as δ_{CH} in Figure 4.1) across the acquired 4H-SiC epitaxial layers, owing to the material growth and production tolerance.
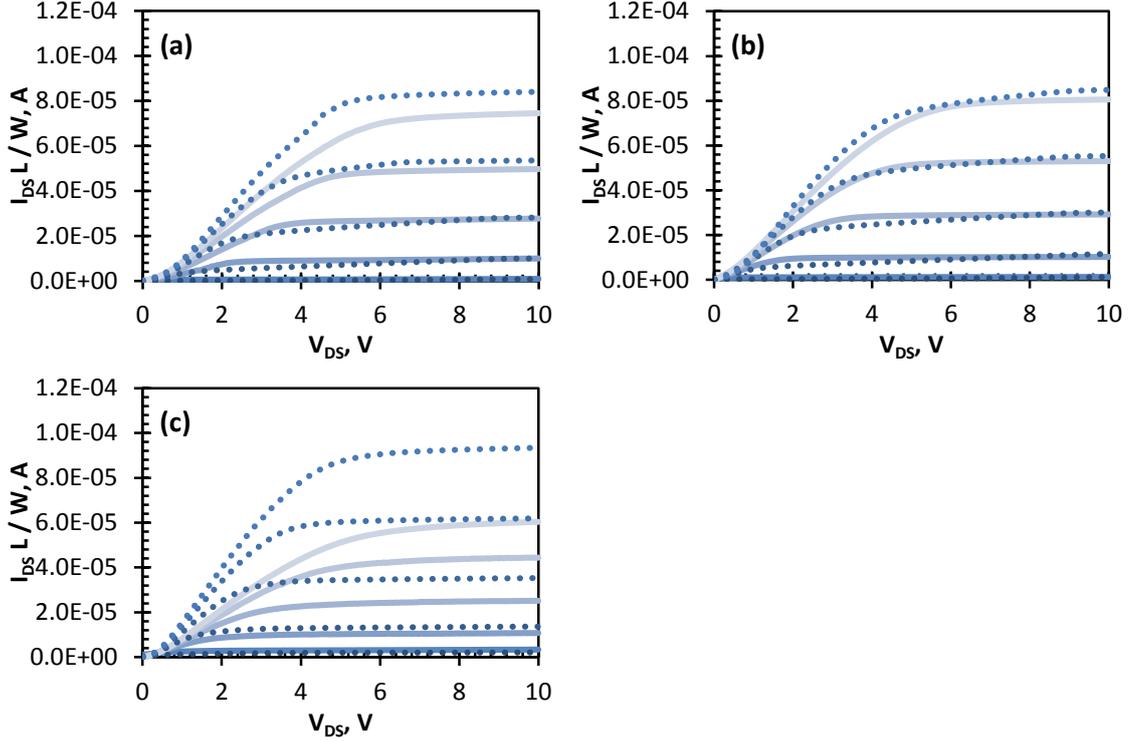
Figure 4.2: Comparison of gate geometry normalised current characteristics ($I_{DS} L / W$) as a function of drain-source voltage (V_{DS}) between junction field effect transistors (JFETs) with gate length (L) of 9µm (filled) and 21µm (dotted) on an identical gate width (W) of a) 200µm, b) 150µm and c) 50µm. The gate-source voltage (V_{GS}) of the investigated transistors were swept from -3.0V to 1.0V with a 1.0V steps.

To examine the influence of wafer tolerance on these observations, the normalised I-V curves for all investigated devices biased at $V_{GS} = 0.0V$ are plotted in Figure 4.3 alongside the maximum and minimum deviation of $I_{DS} L / W$ (dashed line), estimated using the two extreme cases of tolerance based on Cree's epitaxial specification [89]. The rated tolerance of the doping concentration and channel thickness on the n epitaxy is ±25% and ±10% respectively[*1]. The results in Figure 4.3 show that the normalised I_{DS} of all investigated devices fall within the calculated I_{DS} boundary using Equation 4.1 with the rated N_D and δ_{CH} tolerance. In the case of the 21µm gate length variants, the $I_{DS} L / W$ characteristics show a close agreement with the sample average (as shown by the dotted line), with an exception on the 50µm/21µm transistor where the normalised I_{DS} is relatively larger than the average $I_{DS} L / W$. On the other hand, the I-V characteristics of the transistors with 9µm gate length are deviated between devices and exhibit a lower $I_{DS} L / W$ relative to the sample average. Based on these results, the

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[*1] Note that the 4H-SiC epitaxial wafer used for the transistor fabrication was the early batch of 4" wafer hence the material quality is comparatively inferior

tolerance of the SiC wafer properties is not likely to be the prime reason that causes the $I_{DS} L / W$ discrepancy among the investigated devices. Since the 9μm gate length JFETs are the only variant that demonstrate large variation in the $I_{DS} L / W$ characteristic, either these transistors have different device physics inherently or they may suffer from fabrication errors such as under/over etching and photolithograph misalignment, where the variation of W/L ratio on the 9μm L transistors is two-fold more susceptible than the 21μm L transistors.
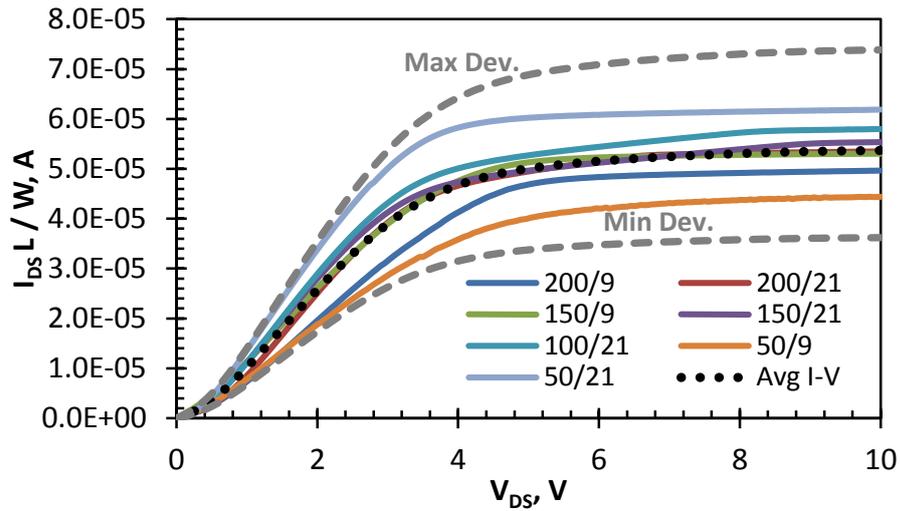
Figure 4.3: Gate geometry normalised current ($I_{DS} L / W$) as a function of drain-source voltage (V_{DS}) measured at 0.0V gate-source bias (V_{GS}) for all investigated junction field effect transistors (JFETs). The corresponding computed maximum and minimum deviation as well as the sample average of the $I_{DS} L / W$ are illustrated by the dashed and dotted lines respectively.
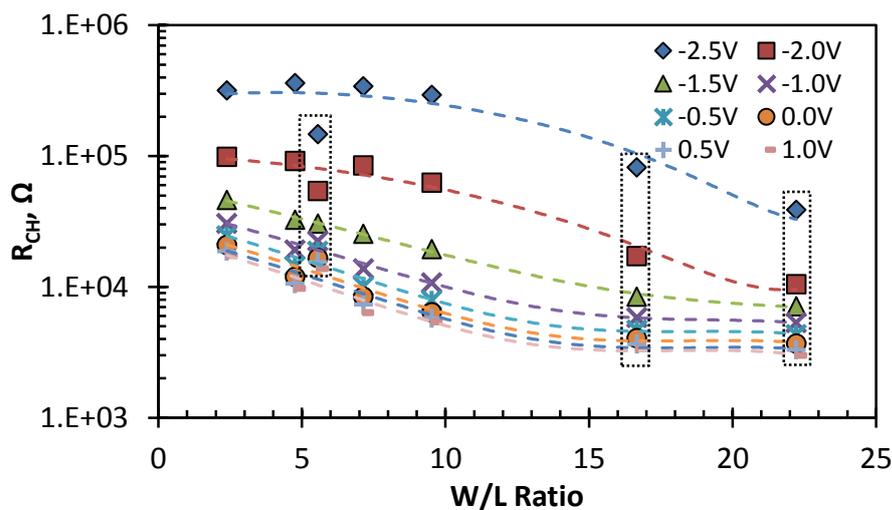
Figure 4.4: Total channel resistance (R_{CH}) of the junction field effect transistors (JFETs) extracted from the linear operating regime as a function of gate geometry (W/L) ratio for gate-source voltage (V_{GS}) biased from -2.5V to 1.0V. The dashed lines are the corresponding polynomial fitting for each V_{GS}.

The total channel resistance (R_{CH}) of a JFET biased in the linear operating regime can be described by the sum of passive and active resistive components as shown in the following expression:

$$R_{CH} = 2R_{con} + R_{epi} + R_{DS} = \frac{2\rho_c}{A_{con}} + \frac{2\rho_{epi}l}{W\delta_{CH}} + \frac{2\Psi_P L}{We\mu N_D\delta_{CH}V_G} \quad - (4.2)$$

here R_{con} is the contact resistance, R_{epi} the n-epitaxy resistance between the gate structure and n+ region and R_{DS} the drain-source resistance, ρ_c the specific contact resistance, A_{con} the area of contact pad, ρ_{epi} the resistivity of n-epitaxy, l the length of the spacing between the drain/source N+ region and P+N junction, V_G the effective gate voltage $V_G = V_{GS} - V_{TH}$, V_{TH} the transistor on/off voltage.

The results in Figure 4.4 illustrate the scaling of R_{CH} as a function of the W/L ratio biased at V_{GS} between -2.5V and 1.0V with 0.5V steps. As can be observed from the data in the figure, the R_{CH} for gate bias from -1.5V to 1.0V demonstrates a monotonic decrease with increasing W/L ratio and begins to saturate as the gate geometry ratio exceeds 15. For V_{GS} between -2.0V and -2.5V, the channel resistance shows a very weak dependence with the gate geometry ratio, notably for the transistors with low W/L ratio (<10) where the observed R_{CH} is almost independent of the gate geometry scaling. Furthermore, it can be observed that the influence of the gate bias on R_{CH} is significantly reduced as the conduction channel widens with increasing V_{GS}, leading to the domination of the R_{CH} by the passive components.

Based on Equation 4.2, R_{DS} is predicted to scale linearly with the W/L ratio without exhibiting any form of saturation when $V_{GS} > V_{TH}$. The data in Figure 4.4 indicates that some transistor variants do not follow the constant mobility model, causing the $R_{CH} - W/L$ relation to diverge from the predicted behaviour. In addition, the distinct R_{CH} behaviour such as those transistors with R_{CH} value lower than the sample average when $R_{CH} \approx R_{DS}$ at $V_{GS} =$ -2.0V and -2.5V, indicate limitations in the applicability of the constant mobility model in describing the devices *I-V* characteristics. These transistors are identified as the 9μm gate length variant as highlighted by the dotted box in the Figure 4.4. Conspicuously, there may be some fundamental differences in operation between the 9μm and 15μm *L* transistors such the short channel effect, which lead to such discrepancies in the DC characteristics.

II. <u>Low Frequency Noise Characterisation</u>

The results in Figure 4.5 illustrate the typical current noise power spectral density ($S_{I_{CH}}$) as a function of frequency for the 4H-SiC epitaxial JFET with a) 9μm and b) 21μm gate length. The transistors were biased at V_{GS} from -3.0V to 1.0V with 1.0V increments with V_{DS} maintained at 3.0V for all gate geometry investigation unless otherwise stated. As can be observed from the data in Figure 4.5a, the $S_{I_{CH}}$ of the 9μm device exhibits a monotonic decay in magnitude with increasing V_{GS} and the trend is reversed as the gate junction is forward biased. The change in noise behaviour is presumed to be caused by the contribution of gate leakage. The data shows that the frequency exponent (λ) of the noise spectrum has transformed from -2.0 to -1.0 during the widening of the conduction channel and a saturated noise component highlighted by the dashed line can be clearly observed at the low frequency region (<10 Hz) for V_{GS} between -3.0V and -1.0V. The large frequency exponent and saturated noise component is inferred as the superposition of Lorentzian spectra manifested from generation-recombination (G-R) fluctuations as seen in previous reports [19], [125], [132].

In contrast, the $S_{I_{CH}}$ of the 21μm transistor increases monotonically with increasing V_{GS} and the frequency exponent of the spectrum exhibits a pure $1/f$ behaviour at frequencies $< 200 Hz$ for all biases investigated. For both transistor variants, the noise spectrum eventually decayed into a white noise component at $> 500 Hz$, which can be easily misinterpreted as the thermal noise of the devices. Nevertheless, due to the homogeneity of the white noise magnitude despite of the differences in gate geometry and biasing conditions as well as the significant discrepancy with the thermal noise level (computed thermal noise $S_I \approx 1 \times 10^{-24} A/Hz$), implies that the white noise element is dominated by the background noise contributed by the measuring instruments. Based on the noise spectrum in Figure 4.5, it can be clearly observed that the noise behaviours of the 9μm and 21μm gate length transistors are governed by two distinct noise mechanisms. To examine the validity and the origin of these noise sources, the low frequency noise characteristics of other on-chip JFET variants with identical L but different W are thoroughly investigated.
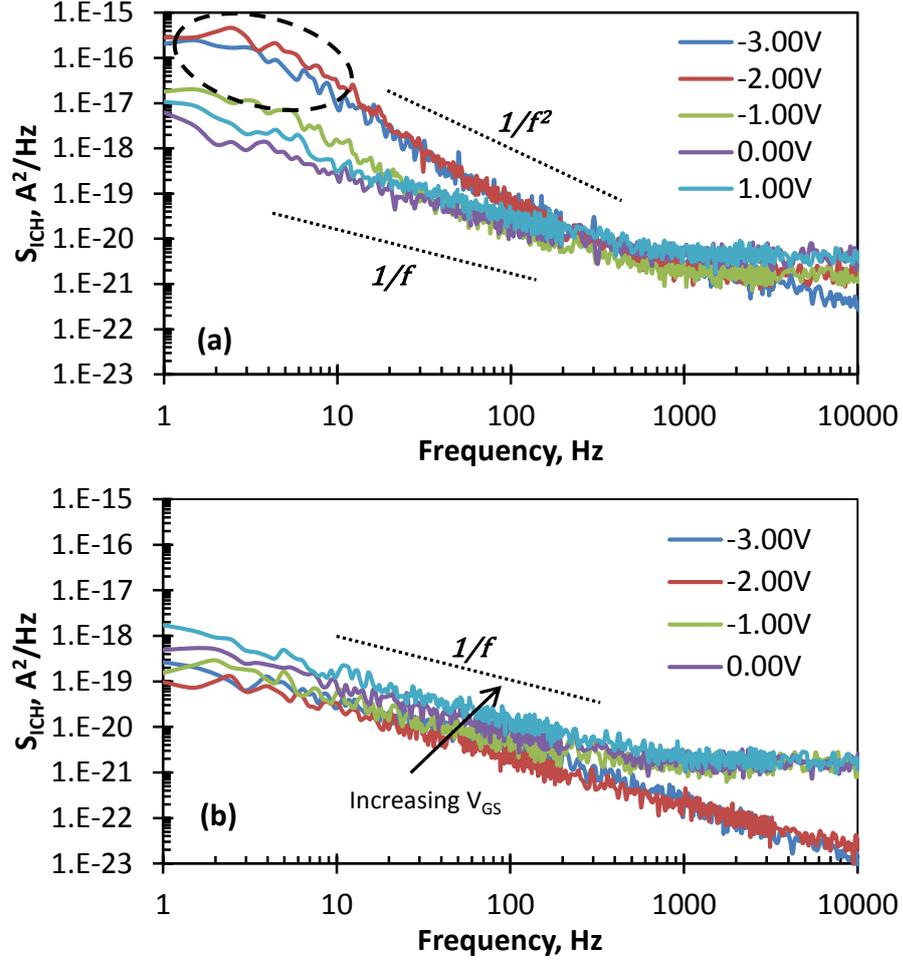
Figure 4.5: Channel current noise power spectral density ($S_{I_{CH}}$) as a function of frequency for the junction field effect transistor (JFET) with a) 9μm and b) 21μm gate length (L) biased at gate-source voltage (V_{GS}) between -3.0V and 1.0V.

The $S_{I_{CH}}$ measured at 10Hz are plotted as a function of I_{DS} in Figure 4.6 for transistors with L of **a)** 9μm and **b)** 21μm under different W. All investigated devices were biased in the linear operating regime and the V_{GS} was swept from -3.0V to 1.0V with 0.5V increments. The dashed lines are the polynomial fit to the results and serve as a guide to the eye. As can be observed from the data in Figure 4.6a, the $S_{I_{CH}}$ for all 9μm devices demonstrate a gradual increment in $S_{I_{CH}}$ with increasing I_{DS} as the conduction channel widens, until a sample specific critical point, where the noise magnitude decreases dramatically. As V_{GS} is increased further (until the gate junction is forward biased) the $S_{I_{CH}}$ behaviour shows a monotonic increase due to the superposition of gate junction leakage noise. In contrast, two distinct trends are observed on the 21μm L transistors. While the 50/21μm device demonstrates a similar $S_{I_{CH}} - I_{DS}$ behaviour to the 9μm L transistors, the noise behaviour of the other 21μm gate length variants exhibit weak I_{DS} dependence at low V_{GS} before $S_{I_{CH}}$ increases proportionally to I_{DS}^2.

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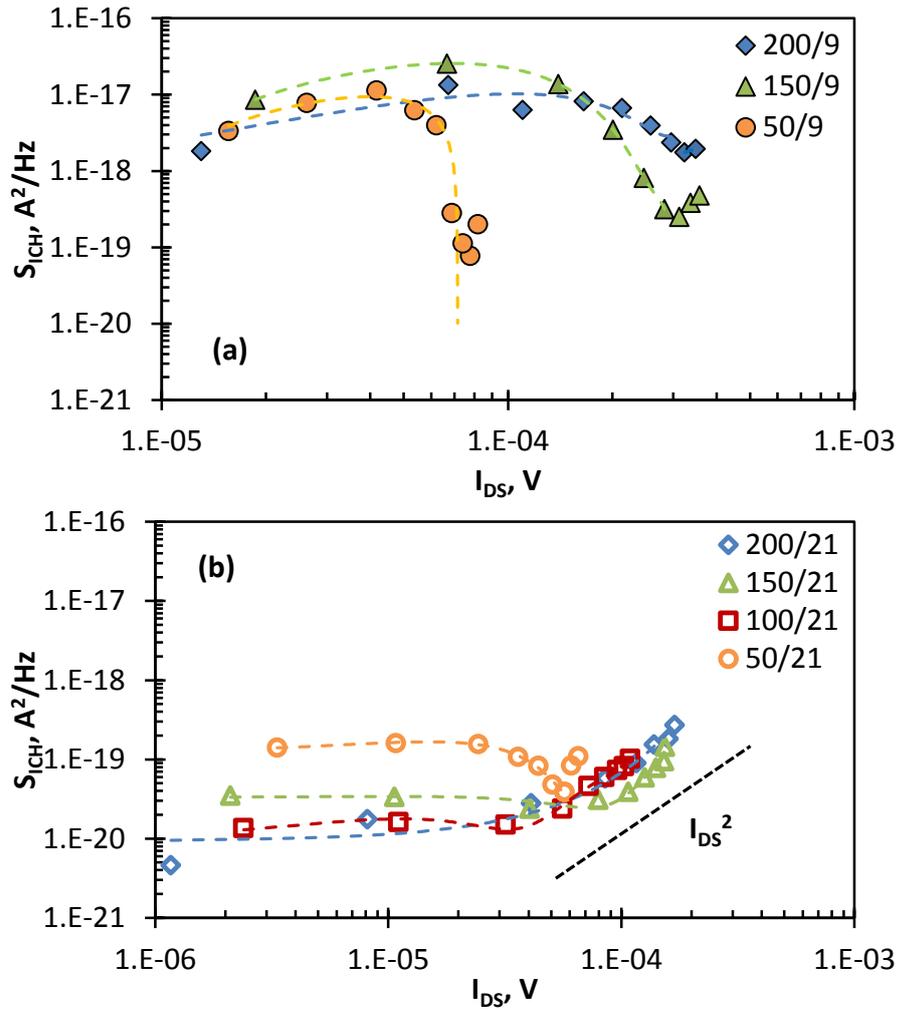
Figure 4.6: Channel current noise power spectral density ($S_{I_{CH}}$) as a function of drain-source current (I_{DS}) measured at 10Hz for junction field effect transistor (JFET) with a) 9µm and b) 21µm gate length (L) and different gate width (W). The gate-source voltage (V_{GS}) of the JFETs is biased from -3.0V to 1.0V with 0.5V steps.
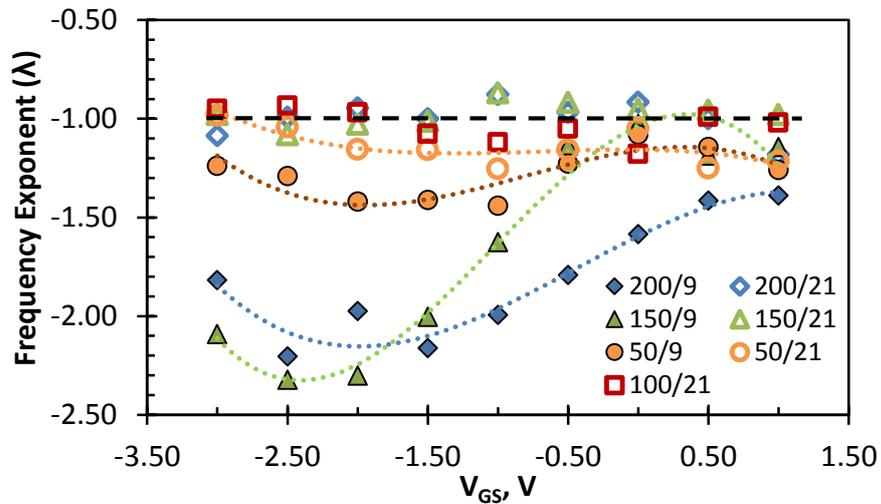
Figure 4.7: Frequency exponents (λ) as a function of gate-source voltage (V_{GS}) for the noise spectrum of each corresponding junction field effect transistors (JFETs) in Figure 4.6.

The data in Figure 4.7 illustrates the frequency exponent of the noise spectrum for the corresponding devices shown in Figure 4.6. The dotted and dashed lines are the guide to the eye for $\lambda - V_{GS}$ relation to highlight the polynomial like and constant frequency exponent respectively. Similarly, the exponent data exhibit two distinct characteristics that can be explicitly associated with the 9μm and 21μm devices with the exception of the 50/21μm variant, where it shows a comparable behaviour with the 9μm devices. As observed in the figure, the frequency exponents of 9μm gate length transistors have an oscillating characteristic. At low V_{GS}, the λ of the noise spectrum decreases monotonically before it starts to escalate exponentially at a device specific bias, then the exponent starts to decrease again at high V_{GS} (the value of which varies between transistors) as a result of an increasing gate leakage current, similar to the turning-point of the $S_{I_{CH}} - I_{DS}$ relation. Conversely, the λ of the 21μm L variants exhibit a constant value of -1.0 ± 0.1 throughout the investigated biases.

Based on the $S_{I_{CH}} - I_{DS}$ and $\lambda - V_{GS}$ relations, the two distinctive LFN characteristics observed in Figure 4.5 may be verified. While, the noise behaviours of 9μm gate length devices and the 50/21μm transistor demonstrate a strong correlation with the evolution of the channel space charge region (SCR) because of the strong dependency of $S_{I_{CH}}$ and λ against V_{GS}, the LFN of the 21μm gate length devices are dominated by resistor-like behaviour similar to the past report [12], owing to semi-linear behaviour between $S_{I_{CH}}$ and V_{GS}. By comparing these results with the models published in the literature, the LFN origin for each JFETs variant is elucidated.

A. *Trap assisted Generation-Recombination Model*
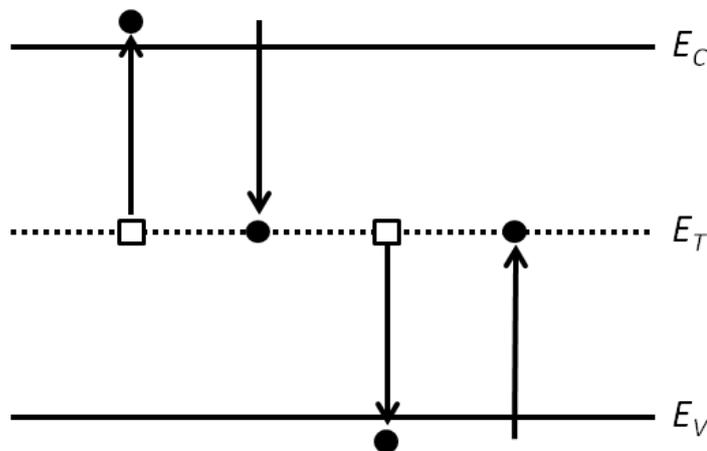
Figure 4.8: The electron and hole capture and emission process at the trap centres.

Results in the literature have proposed numerous low frequency noise models for the JFET utilising the Generation-Recombination (G-R) mechanism, built upon the number fluctuation theory. Amongst these models, G-R fluctuation via Shockley-Hall-Reed (SRH) centre [19], [132]–[135], and oxide interface traps [102], [127], [136] are the most widely reported mechanisms. Sah [132], Lauritzen [19] and Kandiah [135] proposed the origin of low frequency noise manifestations in JFET are due to the trapping and de-trapping of free electrons within the gate junction SCR region through mid-gap defects, while Liou [136], Flatresse [127] and Levinshtein [102] demonstrate that the origin of JFET electrical noise is caused by the electron exchange with the surface states in the native oxide. Despite the similarity in fluctuation mechanism, the nature of each trapping centre defines the unique properties of the transistor noise behaviour, thus enabling the identification of the corresponding fluctuation sources.

Fluctuation in carrier number can be ascribed by the four electron/hole emission and capture processes shown Figure 4.8. For conceptual illustration, the following model only considers carrier fluctuation from a single level trap energy located in the SCR region. In practice, the derived model can be more generally applied to any two level G-R mechanism. Furthermore, fluctuation arising from multiple energy levels may also be present in semiconductor devices. Based on the low frequency noise model proposed by Sah and Lauritzen, the fluctuation rate of trapped carriers under the four processes in Figure 4.8 can be described using:

$$N_t \partial f_t / \partial t = U_{cn} - U_{cp} = N_t \big[(c_n f_{tp} n - e_n f_t) - (c_p f_t p - e_p f_{tp}) \big] - \quad (4.3)$$

where $\partial f_t / \partial t$ is the fluctuation rate of carrier via trap centre, N_t the trap centre concentration per unit volume, U_{cn} and U_{cp} the net capture rate by the trap centres for electron and hole respectively, c_n , c_p, e_n and e_p the capture (c) and emission (e) probability of the trap centre for electron (n) and hole (p) correspondingly, f_t the fraction of trap centres occupied by electrons, f_{tp} the fraction of empty trap centres, n and p the free electron and hole concentration per unit volume.

Within the part of the channel forming the SCR, the carrier generation processes are the dominant mechanism as the electrons and holes in this region are depleted by the high electric field, rendering the recombination process to be non-existent. Equation 4.3 can be further expanded, by assuming that the emission and capture probability ratios for electrons (n_1) and holes (p_1) at equilibrium ($U_{cn} = 0$ and $U_{cp} = 0$) are equivalent

to the non-equilibrium state, such as in the case of a reverse biased p-n junction. The corresponding expansions of Equation 4.3 based on these assumptions are expressed as:

$$e_n/c_n = n_1 = n_i \exp(E_t - E_i)/k_B T - (4.4)$$

$$e_p/c_p = p_1 = n_i \exp(E_i - E_t)/k_B T - (4.5)$$

$$\partial n_t/\partial t = -n_t[c_p(p + p_1) + c_n(n + n_1)] + N_t(c_p p_1 + c_n n) - (4.6)$$

here n_i is the intrinsic carrier concentration, E_t the Fermi energy of trap centres, E_i the intrinsic Fermi energy, k_B the Boltzmann constant,T the temperature in Kelvin and n_t the trapped electrons concentration at the trap centres..

By expanding the electron and hole concentrations around the steady state value, we obtain the expression below:

$$\partial(\delta n_t)/\partial t = -\delta n_t[c_p(p_0 + p_1) + c_n(n_0 + n_1)] + \delta n c_n(N_t - n_{t0}) - c_p n_{t0}\delta p - (4.7)$$

where p_0 and n_0 are the steady-state concentration per unit volume of holes and electrons respectively, δn and δp the deviation in electron and hole concentration and n_{t0} the trapped electron concentration at steady state.

Equation 4.7 alone is insufficient to determine the general solution for the trap time constant, requiring the use of two other differential equations computed from the continuity of current and charge for holes and electrons, which require solving of three coupled nonlinear partial differential equation. Fortunately, there is another solution for the nearly depleted region in the JFET structures, by considering only the long-time constant or the low frequency components. Based on this assumption, the time constant can be expressed as:

$$\tau_t = \frac{1}{[c_p(p_0 + p_1) + c_n(n_0 + n_1)]} - (4.8)$$

The variation in the carrier fluctuation required to model the degree of noise manifestation can be determined using analysis based on statistical mechanisms [137]:

$$\overline{\Delta\Lambda\delta N_t^2} = k_B T\partial(n_t\Delta\Lambda)/\partial F_t = N_t f_t f_{tp}\Delta\Lambda - (4.9)$$

$$f_t = 1 - f_{tp} = \frac{1}{1 + \exp[E_{FN} - E_T)/k_B T]} = \frac{c_n c_0 + c_p p_1}{[c_p(p_0 + p_1) + c_n(n_0 + n_1)]} - (4.10)$$

by dividing both side by the square of the elemental volume increment ($\Delta\Lambda^2$) in Equation 4.9 gives:

$$\overline{\delta N_t^2} = \frac{N_t f_t f_{tp}}{\Delta\Lambda} - (4.11)$$

here E_{FN} and E_T are the quasi-Fermi energy and trap energy responsible for the carrier fluctuation respectively. Utilising expressions 4.8 and 4.11, the typical noise power spectral density can be represented as:

$$S_{N_t} = \frac{4\tau_t}{1+(\omega\tau_t)^2}\frac{N_t f_t f_{tp}}{\Delta\Lambda} - (4.12)$$

In practice however the noise power spectral density based on carrier numbers as seen above may not be attainable due to the availability and setup of measuring instruments, where the fluctuation of conductance (G), voltage (V) and current (I) are conventionally measured. Nevertheless the equivalence of S_{N_t} in these notations can be expressed as:

$$\frac{S_{G_{CH}}}{G_{CH}^2} = \frac{S_{V_{CH}}}{V_{CH}^2} = \frac{S_{I_{CH}}}{I_{DS}^2} = \frac{S_{N_t}}{N_0^2} = \frac{4\tau_t}{1+(\omega\tau_t)^2}\frac{\overline{\delta N_t^2}}{N_0^2} = \frac{4\tau_t}{1+(\omega\tau_t)^2}\frac{N_t f_t f_{tp}}{N_0^2\Delta\Lambda} - (4.13)$$

where the four ratios on the left are the relative or normalised noise power spectral density, $S_{G_{CH}}$, $S_{V_{CH}}$, $S_{I_{CH}}$, S_{N_t} for conductance, voltage, current and carrier number respectively and N_0 the total number of free carriers.
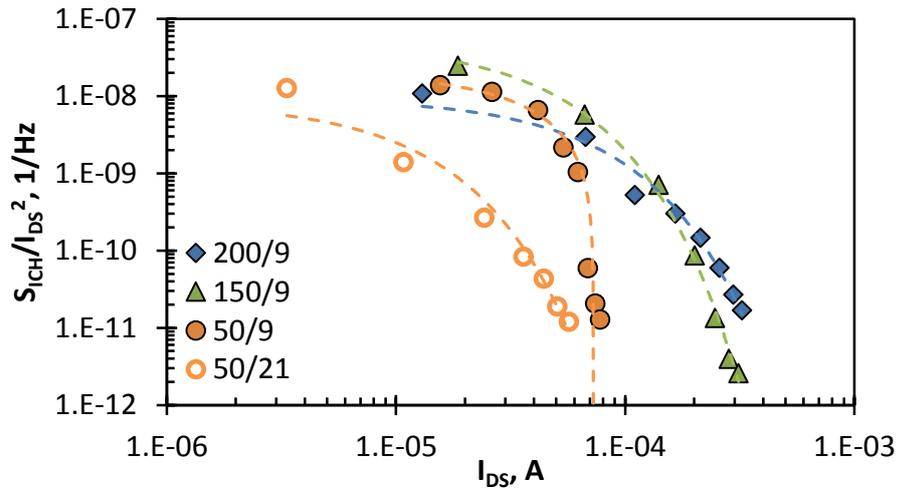
Figure 4.9: Normalised channel current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) measured at 10Hz as a function of drain-source current (I_{DS}) for the 9μm gate length junction field effect transistors (JFETs) and the 50/21μm variant. The gate-source voltage (V_{GS}) are biased from -3.0V to 0.0V with 0.5V steps.

To facilitate a direct comparison between the measured low frequency noise and the G-R model, $S_{I_{CH}}$ data are normalised against I_{DS}^2 to produce the S_{N_t}/N_0^2 equivalent and are plotted in Figure 4.9 as a function of I_{DS}. These devices were measured at 10 Hz with V_{GS} biased from -3.0V to 0.0V with 0.5V increment. The $S_{I_{CH}}/I_{DS}^2$ data in the figure demonstrates an exponential decay in magnitude with increasing I_{DS}, which deviates from the $S_{I_{CH}} - I_{DS}$ data shown in Figure 4.6a, where dual current dependencies were observed under different gate bias operations. Based on the expression given as Equation 4.13, the $S_{I_{CH}}/I_{DS}^2 - I_{CH}$ relation suggests that the $(N_t f_t f_{tp})/(N_0^2 \Delta \Lambda)$ term shows a strong dependence on $e^{-I_{DS}}$ and the data can be interpreted as a correlation of $S_{I_{CH}}/I_{DS}^2$ behaviour to the variation of the SCR volume or conduction channel thickness under the influence of V_{GS}.

Figure 4.10 shows the $S_{I_{CH}}/I_{DS}^2$ data re-plotted as a function of the two-dimensional SCR area (A_{SCR}) computed using the gradual channel approximation, to examine the contribution of SCR on the observed low frequency noise. The inset to the figure illustrates the A_{SCR} as a function of V_{GS}. As observed from the data in Figure 4.10, the $S_{I_{CH}}/I_{DS}^2$ is at a minimum and shows a weak dependence with A_{SCR} at high V_{GS} until a device specific critical point (typically ~2.2×10⁻⁸1/Hz), where the noise magnitude increases exponentially relative to a small change of A_{SCR}. Indeed, the $S_{I_{CH}}/I_{DS}^2 - A_{SCR}$ relation provides further evidence that the $S_{I_{CH}}/I_{DS}^2$ behaviour is correlated to the evolution of the SCR. Nevertheless, following the noise expression in Equation 4.13, the $S_{I_{CH}}/I_{DS}^2$ term is still heavily influenced by the N_0^2 term that is V_{GS} dependent, which may causes the semi-linear increment of $S_{I_{CH}}/I_{DS}^2$ with A_{SCR} in Figure 4.10. Considering a fixed $\overline{\delta N_t^2}$ term, the rapid escalation of the $S_{I_{CH}}/I_{DS}^2$ behaviour with increasing A_{SCR} can be translated into an increase in the $\overline{\delta N_t^2}/N_0^2$ term as N_0^2 decays under the influence of V_{GS}, where the total number of free carriers in the JFET channel is gradually depleted with expanding SCR volume. Therefore, it is important to nullify the influence of the N_0^2 term to reveal the true dependency of $\overline{\delta N_t^2}$ with A_{SCR}. This can be achieved by multiplying the $S_{I_{CH}}/I_{DS}^2$ term by N_0^2 to produce a new expression ($S_{I_{CH}} N_0^2/I_{DS}^2$) that is proportional to $\overline{\delta N_t^2}$.

The data in Figure 4.11 shows the $S_{I_{CH}} N_0^2/I_{DS}^2$ as a function of A_{SCR}. As can be observed from the figure, the $S_{I_{CH}} N_0^2/I_{DS}^2$ data increases monotonically with increasing

A_{SCR} (negative gate bias), demonstrating a similar trend as the $S_{I_{CH}}/I_{DS}^2 - A_{SCR}$ behaviour in Figure 4.10. However, $S_{I_{CH}}N_0^2/I_{DS}^2$ exhibits an inverse behaviour in the high gate leakage regime($V_{GS} \geq 0.0V$), where the noise magnitude increases monotonically with decreasing A_{SCR}. The latter noise characteristic can be elucidated by the influence of gate leakage current as the junction is forward biased, while the former verifies the strong correlation of $N_t f_t f_{tp}/\Delta\Lambda$ with the evolution of the SCR, where the carrier fluctuation probability is improved with increasing A_{SCR}.

Based on the observed $S_{I_{CH}}N_0^2/I_{DS}^2 - A_{SCR}$ and $\lambda - V_{GS}$ characteristics, it can be inferred that the low frequency noise characteristics observed on the 9μm gate length and the 50/21μm JFETs originates from the SCR formed by the gate junction. The observed noise behaviours are presumably induced by the transformation of SCR modulated by V_{GS}, where the increase in A_{SCR} under negative V_{GS} causes the quasi-Fermi level to be in close proximity with the energy level of the trap. Utilising Equation 4.10, the proximity of E_{FN} to E_T under the influence of V_{GS}, enhances the $f_t f_{tp}$ term, hence increasing the likelihood of carrier fluctuation, which results in a higher observed noise magnitude. Conventionally, the experimental noise results obtained by Sah and Lauritzen were based on gold doped Si JFET [19], [132], where the trap centres were well-defined and controlled. However, the relative immaturity of SiC technology compared to Si has resulted in the generation of multiple trapping states of both intrinsic and extrinsic origin during the crystal growth and/or fabrication process that may potentially act as a G-R centre. Therefore, some of the investigated JFETs may appear to have inherently different $S_{I_{CH}}N_0^2/I_{DS}^2 - A_{SCR}$ and $\lambda - V_{GS}$ characteristics due to the interaction of carriers with specific trap species. This would also explain the contrary results between the findings in this investigation and those presented by Sah [132], where the c_n, c_p, e_n and e_p parameters are not constant with electric field, instead it is closely correlated to the trap species involved in the carrier fluctuation mechanism.
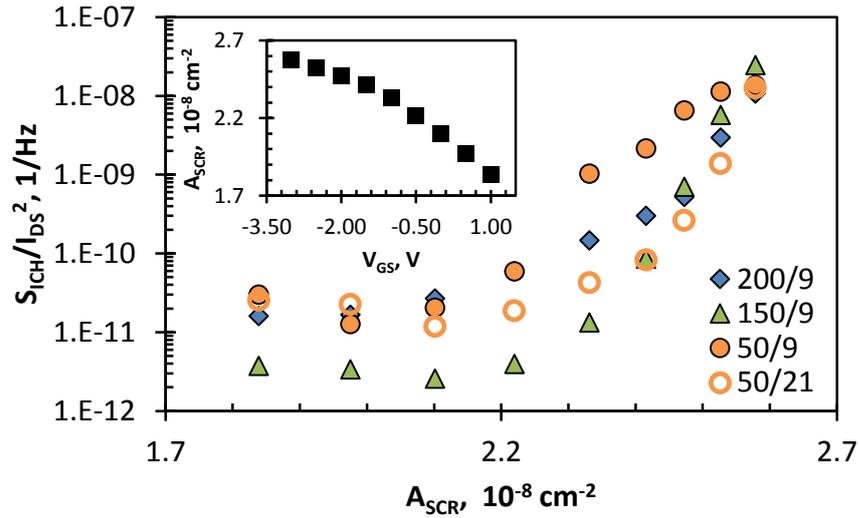
Figure 4.10: Normalised channel current noise power spectral density $(S_{I_{CH}}/I_{DS}^2)$ **measured at 10Hz as a function of space charge region area** (A_{SCR}) **for the 9μm gate length junction field effect transistors (JFETs) and the 50/21μm variant. The gate-source voltage** (V_{GS}) **are biased from -3.0V to 1.0V with 0.5V steps. Inset shows the corresponding** A_{SCR} **as a function of** V_{GS}.
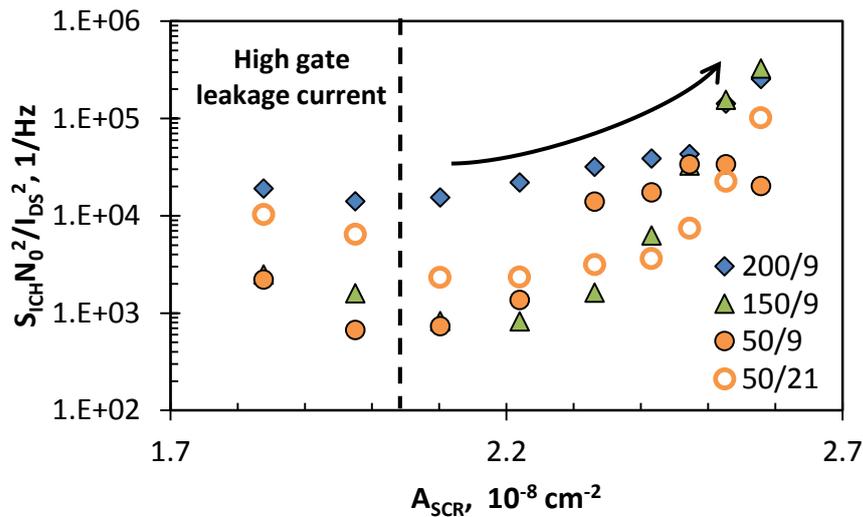
Figure 4.11: Normalised channel current noise power spectral density multiply by the respective square of total number of carrier $(S_{I_{CH}}N_0^2/I_{DS}^2)$ **as a function of space charge region area** (A_{SCR}) **for the 9μm gate length junction field effect transistors (JFETs) and the 50/21μm variant. The gate-source voltage** (V_{GS}) **are biased from -3.0V to 1.0V with 0.5V steps.**

B. *Series Resistor Model*

Following Equation 4.2, the typical channel resistance (R_{CH}) of a JFET biased in the linear operation regime is a summation of three resistive components R_{con}, R_{n-epi} and R_{DS}, each of which originates from different parts of the transistor. These components can be further categorised as:

$$R_{CH} = R_{DS} + R_{passive} - (4.13)$$

where $R_{passive}$ is the sum of $2R_{con}$ and $2R_{n-epi}$.

Each of these components dominates R_{CH} under different drain-source bias conditions. At high negative gate bias, the channel resistance is mainly governed by R_{DS} (where the conduction channel is highly depleted). As the SCR volume reduces, $R_{passive}$ becomes the dominant component of the channel resistance. As can be observed in the $R_{CH} - V_{GS}$ plot in Figure 4.12, the data clearly distinguishes the regions of dominance for both resistances as V_{GS} is swept from -3.0V to 1.0V. Whilst $R_{passive}$ dominates the channel resistance at $V_{GS} \geq -1.5V$ (where R_{CH} is weakly dependent on V_{GS} and shows the sign of saturation with increasing V_{GS}), the observed R_{CH} is governed by R_{DS} at $V_{GS} < -1.5V$, where the R_{CH} increases monotonically with decreasing V_{GS}.

Based on the JFET channel resistance model, the measured channel LFN ($S_{R_{CH}}$) of the transistor can be separated into three distinctive noise sources each correlating to the resistive components in Equation 4.2 as shown below:

$$S_{R_{CH}} = S_{R_{DS}} + S_{R_{n-epi}} + S_{R_{con}} - (4.14)$$

where $S_{R_{DS}}$, $S_{R_{n-epi}}$ and $S_{R_{con}}$ are the low frequency noise source of R_{DS}, R_{n-epi} and R_{con} respectively. Following Hooge's formula [138] the channel noise expression can be further expanded as below:

$$\frac{S_{I_{CH}}}{I_{DS}{}^2} = \frac{S_{R_{CH}}}{R_{CH}{}^2} = \frac{\alpha_{DS}}{f^\lambda N_{PN}} + \frac{\alpha_{n-epi}}{f^\lambda N_D} + \frac{\alpha_{con}}{f^\lambda N_{con}} - (4.15)$$

here $S_{R_{CH}}/R_{CH}{}^2$ is the relative or normalised resistance noise power spectral density, α_{DS}, α_{n-epi} and α_{con} are the Hooge's parameter for the active drain-source (governed by the gate junction), n-epitaxy and contact resistance correspondingly, N_{PN}, N_D and N_{con} the total carrier number of the channel region under the gate junction, n-epitaxy and contact resistance respectively.
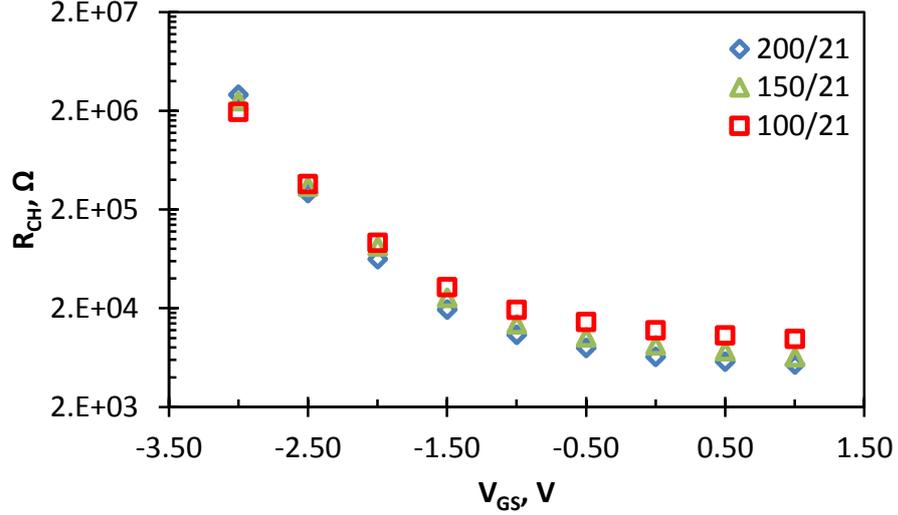
Figure 4.12: Total channel resistance (R_{CH}) extracted from the linear operating regime as a function of gate-source voltage (V_{GS}) of the junction field effect transistors (JFETs) with 21µm gate length (L).

In this particular case, we presumed that the μ and α_{DS} are constant (without pinch-off effect) throughout the applied V_{GS} as the V_{DS} were maintained at the linear operation regime. Furthermore, the specific fluctuation mechanism relating to Hooge model may not be necessarily governing the low frequency noise of the investigated JFETs due to the fundamental difference in fluctuation theory between G-R and Hooge models. Hence, Equation 4.15 can only be used as a demonstration of the concept for the interchangeable resistance noise that dominates the JFET structures studied here.

The results in Figure 4.13 illustrates $S_{I_{CH}}/I_{DS}^2$ as a function of R_{CH} measured at 10 Hz with V_{GS} biased between -3.0V to 0.5V in increments of 0.5V. The inset to the figure shows the variation of α_{DS} as a function of R_{CH}, where $\alpha_{DS} \propto R_{CH}^{1.5}$. As predicted by Equation 4.15, the $S_{I_{CH}}/I_{DS}^2 - R_{CH}$ plot clearly shows two distinctive noise dependencies for all investigated devices, corresponding to the $R_{CH} - V_{GS}$ relation in Figure 4.12. At low R_{CH} ($V_{GS} \geq -1.5V$), the observed $S_{I_{CH}}/I_{DS}^2$ is virtually independent of the R_{CH}, exhibiting a typical resistor or contact noise behaviour where $S_{I_{CH}} \propto I_{DS}^2$ [12]. In the case of high R_{CH} ($V_{GS} < -1.5V$), the $S_{I_{CH}}/I_{DS}^2$ increases monotonically with $R_{CH}^{1.5}$, which is comparable to those LFN behaviour observed on the 9µm L transistors if $S_{I_{CH}}/I_{DS}^2$ is re-plotted as a function of total channel resistance. Such phenomenon implies a strong correlation of G-R related LFN manifestation in the 21µm L JFET at $V_{GS} < -1.5V$.
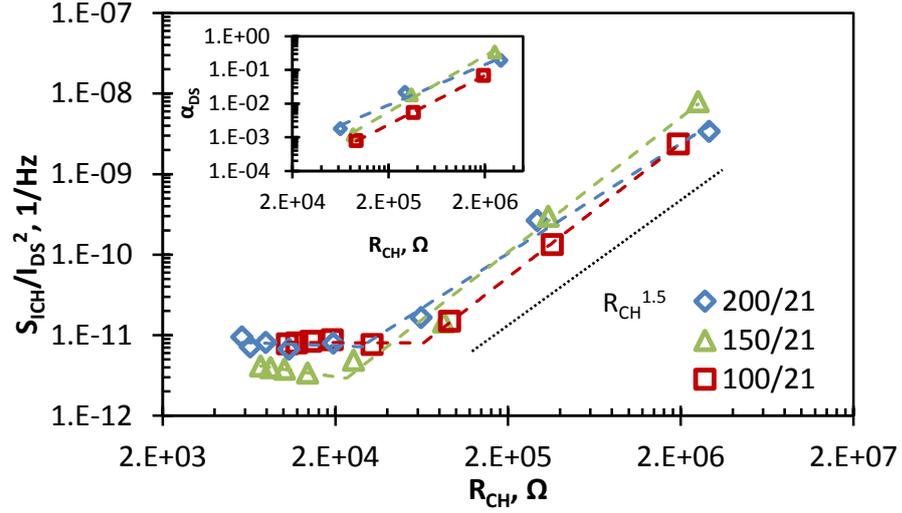
Figure 4.13: Normalised channel current noise power spectral density $(S_{I_{CH}}/I_{DS}^2)$ **measured at 10Hz as a function of total channel resistance** (R_{CH}) **for the 21μm gate length junction field effect transistors (JFETs). Inset shows the Hooge's parameter of the drain-source resistance** (α_{DS}) **as a function of** R_{CH} **extracted using the** $S_{I_{CH}}/I_{DS}^2$ **data under the strong influence of drain-source resistance** (R_{DS})**.**

These findings contradict those reported in the literature, where the transistors with fluctuation origin related to conducting channel demonstrates noise dependence of $S_{I_{CH}}/I_{DS}^2 \propto R_{CH}$ [126]. Furthermore, the typical α_{DS} that was shown to be independent of V_{GS} in the literature is not reflected in the $\alpha_{DS} - R_{CH}$ data presented here, where α_{DS} demonstrate a strong V_{GS} dependence. All these observations lead to the implication that the Hooge model cannot fully describe the $S_{I_{CH}}/I_{DS}^2 - R_{DS}$ relation on the 21μm L JFETs. Based on the data shown in Figure 4.13, the low frequency noise source of the 21μm L devices arises from two distinct origins. While the noise behaviour of the JFETs biased at $V_{GS} \geq -1.5V$ is due to the conductance fluctuation of passive resistivity components, the behaviour at $V_{GS} < -1.5V$ is associated with the evolution of the SCR, possibly due to the similar G-R fluctuation presented in Section 4.3.1.II.A. Although the exact reasoning that leads to a unity frequency exponent is unknown for these 21μm transistors, the low frequency noise behaviours at $V_{GS} < -1.5V$ may be an indirect fluctuation mechanism which is observed as a form of resistance noise. Therefore, the characteristic time constant of the carrier trapping and de-trapping process is not reflected in the frequency exponent of the noise spectrum. By employing the series resistance model, the low frequency noise origin of the 21μm gate length variants can be described by the interplay of the active and passive resistivity components, leading to

the observation of unique $S_{I_{CH}} - I_{DS}$ behaviour in comparison to that observed in the 9μm L JFETs.

4.3.2 The influence of high temperature operation on 4H-SiC JFETs

I. Electrical Characterisation

The data in Figure 4.14 illustrates the variation in R_{CH} as a function of operating temperature (T) for the 21μm and 9μm L transistors with gate widths of 200μm, 150μm and 50μm. The devices are biased in the linear operation regime at $V_{DS} = 3.0V$ with V_{GS} floating. As can be seen from the data, R_{CH} increases monotonically with a $T^{\sim\beta}$ dependence, where β lies in the range of 1.60 to 1.82. These values are similar to but not identical with the temperature exponents of the low-field mobility (β_μ), where the predicted β_μ is between 1.87 and 2.00 utilising the Caughey-Thomas approximation [139] and the fitting parameters reported in the literature [140], [141]. The findings demonstrate that the $R_{CH} - T$ results are closely correlated to the temperature dependence of bulk 4H-SiC mobility, implying the domination of bulk resistivity components such R_{DS} and R_{n-epi} over the R_{CH} at elevated temperatures.
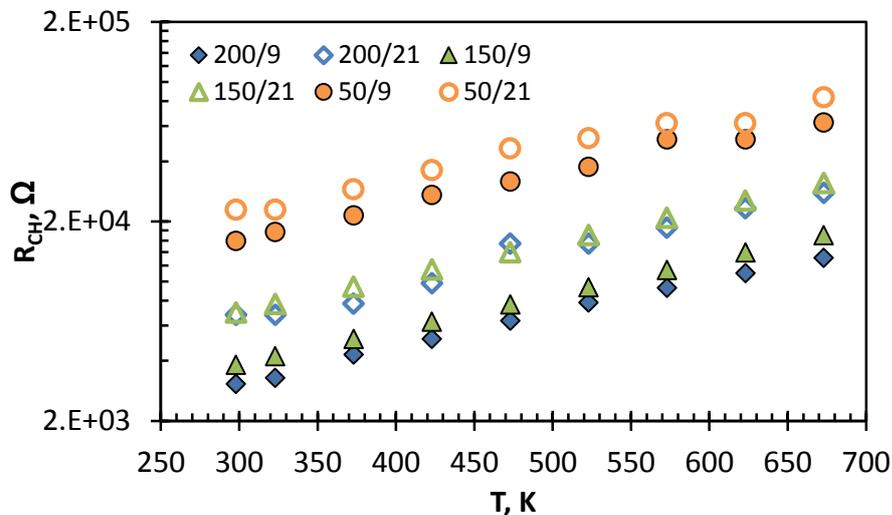
Figure 4.14: Total channel resistance (R_{CH}) as a function of operating temperature (T) for junction field effect transistors (JFETs) with gate geometry (W/L) of 200/9μm, 200/21μm, 150/9μm, 150/9μm, 50/21μm and 50/9μm. The drain-source voltage (V_{DS}) is biased at 3.0V while the gate-source voltage (V_{GS}) is left floating.

II. Low Frequency Noise Characterisation

Figure 4.15 shows $S_{I_{CH}}/I_{DS}^2$ plotted as a function of frequency for different operating temperature from 298K to 673K for the a) 21μm and b) 9μm gate length JFETs with gate width of 200μm. As can be observed from the data in the figure, the

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noise spectrum of the 21μm gate length transistor is a superposition of multiple Lorentzian components at T between 298K and 473K. At 523K, the low frequency component ($f \leq 200Hz$) of $S_{I_{CH}}/I_{DS}^2$ shows evidence of a white noise plateau, before the spectrum is transformed into a pure $1/f$ dependence at $T > 523K$. In contrast, $S_{I_{CH}}/I_{DS}^2$ of the 21μm L devices demonstrate a $1/f$ dependence up to 500Hz before the spectrum is decay into the system noise over the entire temperature range studied.
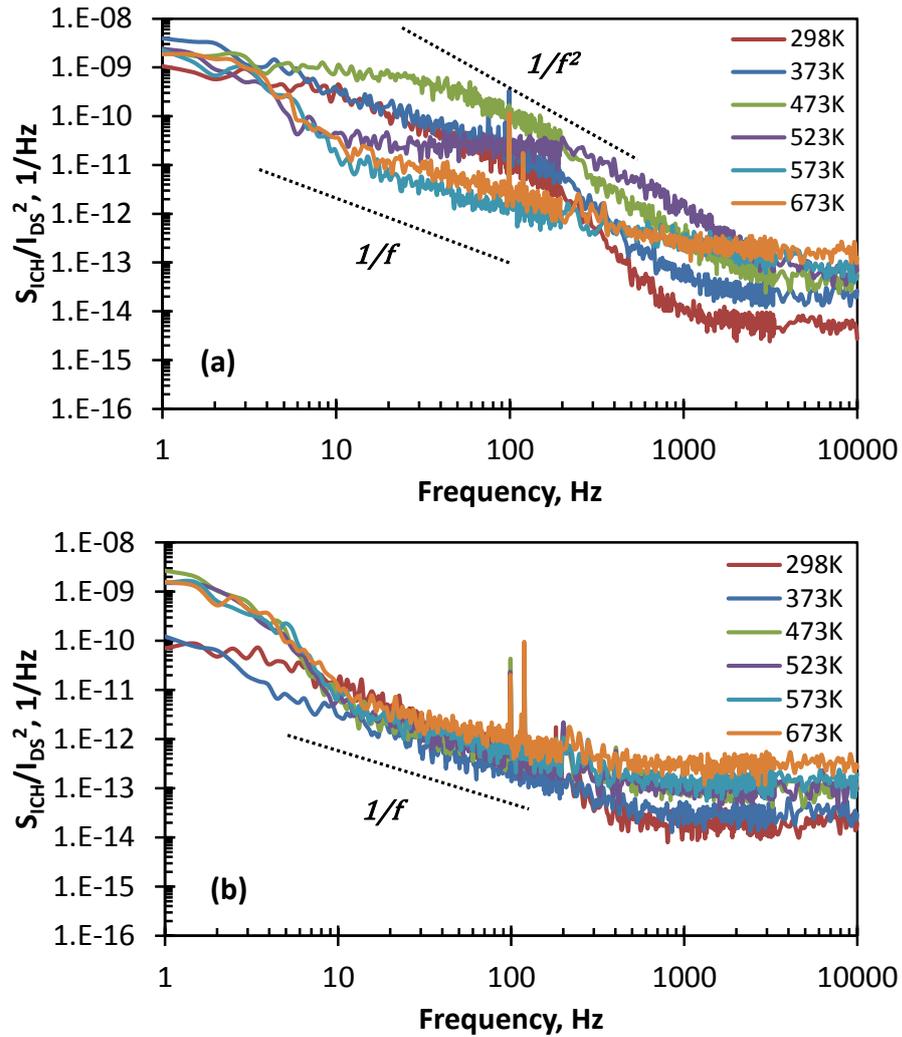
Figure 4.15: Normalised channel current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) as a function of frequency for a) 9μm and b) 21μm gate length (L) junction field effect transistor (JFET) with 200μm gate width (W) operating from 298K to 673K. The drain-source voltage (V_{DS}) is biased at 3.0V with floating gate-source voltage (V_{GS}).
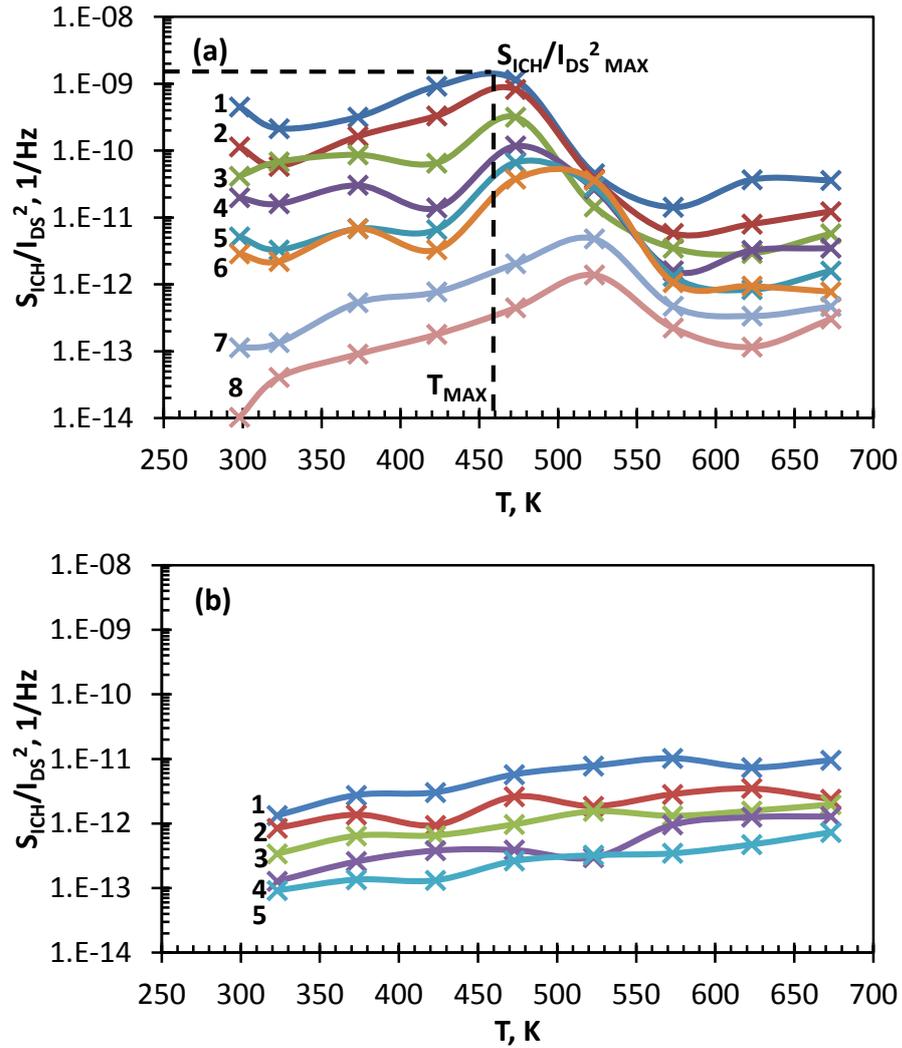
Figure 4.16: Normalised channel current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) as a function of operating temperature (T) for the a) 9μm and b) 21μm gate length (L) junction field effect transistor (JFET) with 200μm gate width (W). $S_{I_{CH}}/I_{DS}^2$ is measured at frequency: 1–10Hz, 2–20Hz, 3–40Hz, 4–80Hz, 5–160Hz, 6–200Hz, 7–420Hz and 8–850Hz. The drain-source voltage (V_{DS}) of the devices is biased at 3.0V and the gate-source voltage (V_{GS}) is left floating.

Alternatively, these $S_{I_{CH}}/I_{DS}^2$ results can be transformed into the temperature function measured at different frequencies to clearly demonstrate the temperature dependence of LFN as shown in Figure 4.16. As can be observed from the data in Figure 4.16b, the $S_{I_{CH}}/I_{DS}^2$ of the 21μm JFET increases monotonically with operating temperature for all frequency components investigated. In contrast, the 9μm gate length device demonstrates a gradual increment in $S_{I_{CH}}/I_{DS}^2$, reaching a frequency dependent maximum point followed by a significant decrease before converging to give a $S_{I_{CH}}/I_{DS}^2$ behaviour similar to that observed with the 21μm transistor. In addition, $S_{I_{CH}}/I_{DS}^2$ for the 9μm device is at least 3 orders of magnitude higher than the 21μm transistor at room

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temperature. Conventionally, the $S_{I_{CH}}/I_{DS}^2 - T$ relation dominated by the G-R mechanisms was considered as an interaction between the temperature dependent quasi-Fermi energy and the responsible trap levels, and the methods of trap species extraction in the literature were developed based on such an assumption [142]–[144].

As reported in [142]–[145], the trap levels responsible for manifestation of low frequency noise can be extracted based on either the $S_{I_{CH}}/I_{DS}^2 - f$ relation for different T (Figure 4.15) or the $S_{I_{CH}}/I_{DS}^2$ behaviour as a function of T measured at different f (Figure 4.16). Although the extraction method for both cases is basically dissimilar, the ultimate outcomes of these methods are theoretically equivalent. In practice, however the latter case was reported to be less susceptible to measurement interference [142], since the maxima characteristics of $S_{I_{CH}}/I_{DS}^2$ can be traced conspicuously, while the $S_{I_{CH}}/I_{DS}^2 - f$ gradient where the noise level is 3dB less than the white noise plateau, as observed in Figure 4.15a can be rather ambiguous to determine.

A. *Generation-Recombination trap extraction based the low frequency noise spectrum*

In this approach, the improvised model devised by Levinshtein and Rumyantsev [145] was employed, which utilises the $S_{I_{CH}}/I_{DS}^2 - T$ dataset measured at different f. Based on this model, new assumptions and resulting mathematical expressions are imposed on the fundamental G-R model described using Equation 4.13. First, the free carrier concentrations are assumed to be fully depleted in the SCR ($n_0 = p_0 = 0$) and the electron capture rate dominates the generation-recombination process ($c_n n_1 \gg c_p n_p$) [143], [145]. Hence, the time constant given in Equation 4.8 can be rearranged as:

$$\tau_t = \tau_c f_t - (4.16)$$

where τ_c is the carrier time constant.

Next, the carrier capture cross-section (σ) is assigned to be exponentially dependent on the operating temperature, where $\sigma = \sigma_0 \exp(-E_\sigma/kT)$, which enables τ_c to be expressed as:

$$\tau_c = \tau_{c0}\exp(E_\sigma/kT), \tau_{c0} = (\sigma_0 v_{T0} n_0)^{-1} - (4.17)$$

here σ_0, v_{T0} and n_0 are the carrier capture cross-section, thermal velocity and electron concentration at 0K respectively and E_σ is the characteristic energy level for the capture cross-section.

In contrast to traditional approaches, the temperature dependence of the trap capture cross-section is introduced to this extraction method as an enhanced feature, which was demonstrated to minimise the errors of extracted parameters [145]. By incorporating Equations 4.16 and 4.17 into Equation 4.12, $S_{I_{CH}}/I_{DS}^2$ can be described using:

$$\frac{S_{I_{CH}}}{I_{DS}^2} = \frac{4N_t}{N_{D-Ion}^2 \Delta \Lambda} \frac{\tau_{c0} \exp(E_\sigma/kT) f_t^2 f_{tp}}{1 + \omega^2 \tau_{c0}^2 \exp(2E_\sigma/kT)} - \quad (4.18)$$

(Note that the square of ionised doping concentration N_{D-Ion}^2 is used instead of N_0^2 to accurately model the SiC JFET behaviour at high temperature, improving the accuracy of predicted LFN value)

Two general limiting boundary conditions were utilised in the original manuscript where E_T was considered to be above or below the E_{FN} relative to the bottom of conduction band. In this investigation, only formulas based on the condition that E_{FN} lies above E_T for all investigated temperatures are described. Under this condition, f_t^2 can be approximated as 1 (since the trap levels are mostly occupied as $E_{FN} > E_T$) while $1 - f_t$ is given as:

$$1 - f_{tp} \cong \exp[(E_{FN} - E_T)/kT] \cong \frac{N_c}{N_D} exp\left(-\frac{E_T}{kT}\right) - \quad (4.19)$$

here N_c is the effective number of states for conduction band. By substituting f_t and $1 - f_{tp}$ into Equation 4.18 produces,

$$\frac{S_{I_{CH}}}{I_{DS}^2} = \frac{4N_t}{N_{D-Ion}^2 \Delta \Lambda} \frac{\tau_{c0} \exp[(E_\sigma - E_T)/kT]}{1 + \omega^2 \tau_{c0}^2 \exp(2E_\sigma/kT)} - \quad (4.20)$$

The corresponding temperature where the maximum $S_{I_{CH}}/I_{DS}^2$ is observed as a function of ω can be acquired by differentiating Equation 4.18 with respective to $1/T$ and by setting the derivative to zero:

$$\frac{1}{kT_{max}} = -\left(\frac{1}{2E_\sigma}\right) ln\left(\frac{E_\sigma - E_T}{E_T \tau_{c0}}\right) - \frac{1}{E_\sigma} \ln(2\pi f) - \quad (4.21)$$

here T_{max} is the operating temperature when $S_{I_{CH}}/I_{DS}^2$ is at maximum and τ_o is the time constant of the spectrum at 0K. By extracting the gradient of the $1/kT_{max}$ term as a function of $\ln(2\pi f)$ (denoted as ∇T) yields $-1/E_\sigma$. Utilising Equation 4.21, the expression in 4.20 can be reorganised in the form of $S_{I_{CH}}/I_{DS\,MAX}^2$ as function of $1/kT_{max}$ described by:

$$\frac{S_{I_{CH}}}{I_{DS\;MAX}^2} = \frac{4N_t}{N_{D-Ion}^2 \Delta\Lambda} \frac{N_c}{N_D} \frac{(a/\omega^2\tau_{c0}^2)^{\frac{E_\sigma - E_T}{2E_\sigma}}}{1 + a} - \quad (4.22)$$

where $a = (E_\sigma - E_T)/(E_T - E_\sigma)$. Likewise, the gradient of the $\ln S_{I_{CH}}/I_{DS\,MAX}^2$ as a function of $2\pi f$ (denoted as ∇S) gives $(E_\sigma - E_T)/E_\sigma$. Based on the $kT_{max} - \ln(2\pi f)$ and $\ln S_{I_{CH}}/I_{DS\,MAX}^2 - \ln(2\pi f)$ relations, E_σ and E_T can be extracted using:

$$E_\sigma = \frac{1}{\nabla T} - \quad (4.23a) \qquad E_T = \frac{1 - \nabla S}{\nabla T} - \quad (4.23b)$$

With E_σ and E_T known, τ_{c0} can be computed using:

$$\tau_{c0} = \frac{1}{\omega}\left(\frac{E_\sigma - E_T}{E_\sigma + E_T}\right)^{0.5} \exp\left(\frac{-E_\sigma}{kT_{max}}\right) - \quad (4.24)$$

The results in Figure 4.17 illustrate the $S_{I_{CH}}/I_{DS}^2$ behaviour measured at 10Hz as a function of operating temperature for the a) 9μm and b) 21μm gate length JFETs with the gate width variants of 200μm, 150μm and 50μm. Despite the fact that only the $S_{I_{CH}}/I_{DS}^2$ behaviours at 10Hz were shown, the noise spectrum for all JFET variants with similar L have a comparable trend to the data shown in Figure 4.16. As can be observed in Figure 4.17a, the noise data for the 9μm L JFETs demonstrate an identical behaviour to the data shown in Figure 4.16, except the position of the maxima is different between devices. In contrast, all 21μm gate length transistors illustrate a monotonic increase in $S_{I_{CH}}/I_{DS}^2$ with the increment of operating temperature. It is interesting to highlight that at $T > 550K$, the $S_{I_{CH}}/I_{DS}^2$ behaviour for JFETs with gate geometry of 150/9μm, 150/21μm and 50/21μm begins to increase rapidly with T.
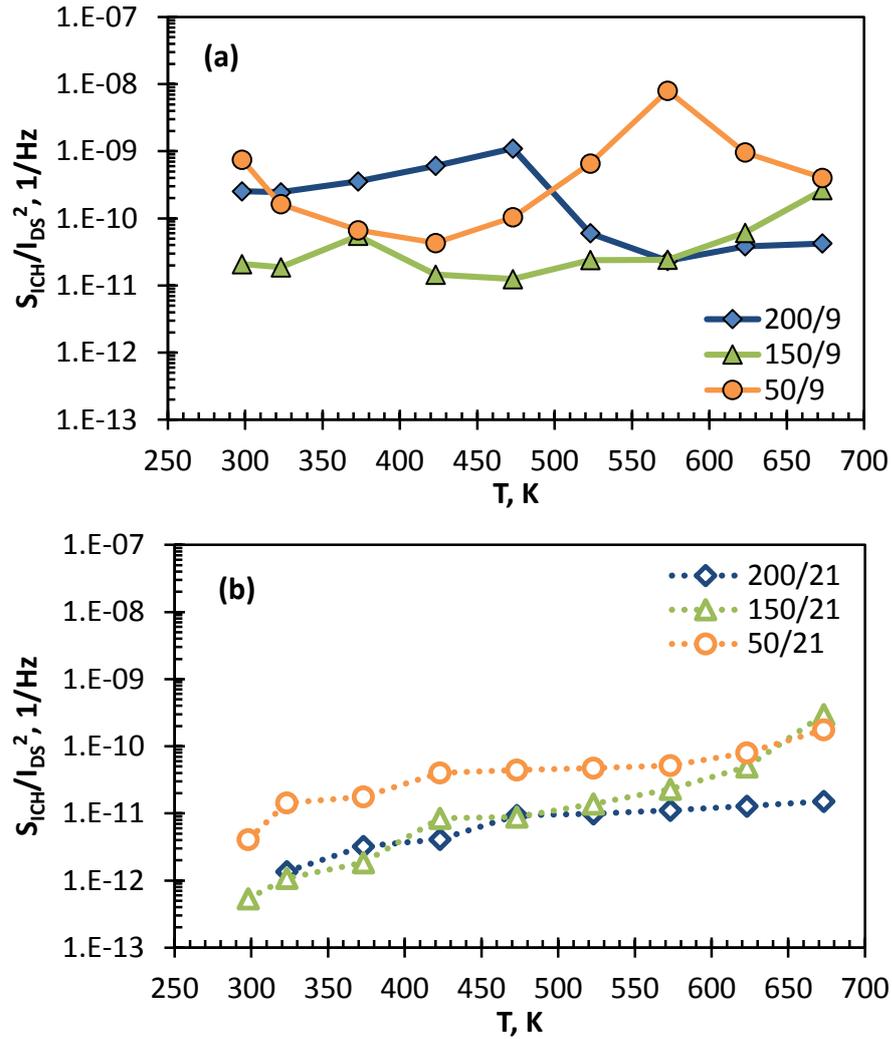
Figure 4.17: Normalised current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) measured at 10Hz as a function of operating temperature (T) for the a) 9µm and b) 21µm gate length (L) junction field effect transistors (JFETs) with the gate width (W) variants of 200µm, 150µm and 50µm. The drain-source voltage (V_{DS}) of the devices is biased at 3.0V and the gate-source voltage (V_{GS}) is left floating.

Based on the model described in Section 4.3.2.II.A., only the transistors demonstrating the characteristics noise maxima at different frequencies can be used for trap extraction. In the case of the 21µm gate width JFETs, the observed increase in $S_{I_{CH}}/I_{DS}^2$ with temperature can be explained either by the weak temperature dependence of σ, where $E_\sigma < E_T$ or the JFET channel is dominated by another form of noise, such as the series resistor model in Section 4.3.1.II.B.. The significant and rapid increase in $S_{I_{CH}}/I_{DS}^2$ on the 150/9µm, 150/21µm and 50/21µm transistor variants at $T > 550K$ may be due to the contribution of thermally activated traps with deeper energy levels to the G-R fluctuation mechanism. Since the Arrhenius plot yields higher activation energies at escalated temperatures, it is logical to correlate the observation of $S_{I_{CH}}/I_{DS_{MAX}}^2$ at

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higher temperature as resulting from traps with deeper energy levels. Nevertheless, such a relation only holds if the σ of corresponding trapping states show exponential dependence of T, which is illustrated in the following results. Utilising the trap extraction method, the corresponding trap properties for 9μm L JFETs were extracted and the results are shown in Table 4.1.

Table 4.1: Properties of the G-R traps involved in low frequency noise generation.

Device	200/9μm		150/9μm	50/9μm
Trap	T1a	T1b	T2	T3
E_σ,eV	-2.42	-1.31	-0.57	-0.37
E_T, eV	-0.57	-0.96	-0.26	-0.16
N_t, cm^{-3}	1.26E+09	7.56E+04	6.99E+09	1.98E+11
$\sigma_{@298K}$, cm^2	7.62E-09	1.37E-13	1.08E-20	9.10E-22
$\sigma_{@523K}$, cm^2	1.86E-26	4.75E-23	7.71E-25	1.85E-24
$\sigma_{@723K}$, cm^2	6.56E-33	1.62E-26	2.33E-26	1.90E-25

As can be observed in Table 4.1, the extracted trap species in these JFETs are unique between devices and demonstrate the existence of a shallow energy level relative to the literature in [102], where a trap energy of $E_C - E_T$ of -2.7eV was obtained. Although the extracted trap energy properties may not be identical to those values acquired using the deep-level transient spectroscopy (DLTS) technique, owing to the possible discrepancy in the ∇T and ∇S curve fitting and the comparatively lower $S_{I_{CH}}/I_{DS}^2 - T$ data resolution. Nevertheless, the proximity of these trap energy level in reference to the reported DLTS data can be used to approximate the responsible noise generating defects in these transistors, where the $Z_{1/2}$ [146], SiC-SiO$_2$ related trapping states [147] and single plane stacking fault related trap [148], [149] may be associated to the E_T of T1a, T1b and T2 respectively. In the case of 50/9μm JFET, the extracted E_T does not correspond to the value of T_{max}, where the predicted E_{FN} is approximately twofold higher than the extracted E_T. Moreover, the measured $S_{I_{CH}}/I_{DS}^2{}_{MAX}$ of the 50/9μm JFET demonstrate a same T_{max} throughout the frequencies used in the trap properties extractions, indicating a weak dependence of σ with T. These scenarios render the unsuitability of the extraction method proposed by Levinshtein and Rumyantsev, hence the validity of the extracted E_T for the 50/9μm transistor variant is questionable [145].

Following the findings detailed Sections 4.31 and 4.3.2, the temperature dependent noise behaviour demonstrates a strong correlation with the two hypothesised LFN origins for each corresponding transistor variant. In the case of the 9μm gate length JFETs, the proposed generation-recombination noise mechanism is verified by the temperature dependence of the observed noise behaviour, where the LFN magnitude is heavily dependent on the proximity of temperature modulated E_{FN} with respect to the E_T of the G-R trap centre, resulting in the unique noise peak shown in Figure 4.17a. In contrast, the gradual increment of $S_{I_{CH}}/I_{DS}^2$ with T on the 21μm gate length JFETs supports the series resistance model, where the $S_{I_{CH}}/I_{DS}^2 - T$ relation can be correlated to the temperature dependency of the resistivity components.

4.4 Summary

The *I-V* and low frequency noise behaviour of 4H-SiC epitaxial signal-level JFETs with different gate geometries were investigated. Significant differences in DC characteristics between the 9μm and 21μm gate length JFETs were observed. In the case of 21μm gate length variants, the transistor *I-V* characteristics demonstrate a close correlation to the constant mobility model. Whilst, the 9μm gate length devices failed to follow the current scaling factor possibly due to the inherently different mode of operation or the fabrication related errors such as under/over etching issue. At room temperature, the low frequency noise behaviours of the 21μm gate length JFETs exhibit a rather peculiar $S_{I_{CH}}/I_{DS}^2 - I_{DS}$ trend, where the channel noise is dominated by the passive resistivity components at $V_{GS} \geq -1.5V$ and the noise becomes dominated by G-R fluctuations as the SCR volume increases. For the 9μm gate length transistors and the 50/21μm gate geometry variants, the low frequency noise behaviour can be described by the trap-assisted generation-recombination mechanism that occurs within the SCR of the p-n junction.

The JFETs channel resistance and low frequency noise characteristics were also examined between 298K and 673K. The total channel resistance for all the transistors investigated demonstrates a scaling factor of approximately 1.8 with the operating temperature, coinciding with low-field mobility-temperature relation predicted based on Caughey-Thomas model. This indicates that the measured total channel resistance comprises a significant contribution from the intrinsic resistance of the n-epitaxial layer. Similarly, two different temperature dependent low frequency noise behaviours were obtained that can be explicitly linked to the gate length of the transistor. For the

investigated 9μm gate length devices, the low frequency noise demonstrates a distinctive $S_{I_{CH}}/I_{DS}^2$ maximum at a temperature that is unique to each transistor all for all frequencies investigated (20Hz to 850 Hz) . In the case of 21μm gate length JFETs, the $S_{I_{CH}}/I_{DS}^2$ increases monotonically with operating temperature through the investigated temperature range. Utilising the trap extraction method reported previously, the trap levels responsible for the G-R fluctuation were extracted for the 9μm gate length devices. Although the trap species are different among devices where E_T is in the range of -0.26eV to -0.96eV, the noise causing G-R centres have relatively shallower trap energy, contrasting to those typically reported on SiC buried gate JFET. Nevertheless, to verify the actual trapping species that is responsible for the observed noise behaviour, an alternative trap extraction technique such as the DLTS is required.

Chapter 5: Reliability Evaluation of Thermally Stressed 4H-SiC Lateral Junction Field Effect Transistor

5.1 Introduction

Apart from gauging the performance of analogue devices, low frequency noise (LFN) is an important evaluation parameter for material quality and structural integrity monitoring, notably for novel semiconductor technology and new device design. Many reports in the literature have demonstrated the possibility of using LFN for the identification of defective structures in semiconductor devices, whereby these findings can be used to optimise the device design and material growth processes [56], [102], [126], [134], [150]–[152]. For example, the excess noise caused by the precipitated oxygen/dislocation complexes in silicon diodes fabricated using the Czochralski grown substrates can be passivated through appropriate thermal treatment [150]. Additionally, the excess noise originating from the native oxide/semiconductor interface on JFETs can be reduced by minority carrier injection through the forward-biased gate junction or a thermal annealing process with the transistor biased in the linear operating regime [124], [125].

Due to the high sensitivity of LFN measurements, the measured noise results for devices that experienced abnormality in operation often demonstrate a significant increase in the noise magnitude, contrasting to the minimal deviation in the DC and AC characteristics [153]. Therefore, the LFN measurement can be utilised as an effective and non-invasive screening process to evaluate the reliability of devices. Such measurements are particularly useful to monitor, examine, and identify structural and intrinsic degradation for devices that have been subjected to thermal, electrical and irradiation stress tests. For semiconductor devices that have undergone aging processes, the physical characteristics of the devices usually suffer from multiple degradations, causing conventional I-V and C-V characterisation techniques to be inconclusive. By acquiring and comparing the LFN characteristics between the as-fabricated and stressed devices under different bias conditions, the mechanism responsible for the observed degradation can be identified [153]–[158].

To date, research has focused solely on using the changes in current-voltage (I-V) characteristics to evaluate the lifetime and reliability of SiC electronics operating at high

temperatures [3], [4]. However, there are no reports on utilising LFN as a quality parameter or diagnostic tool to examine the degradation of SiC transistors under these conditions. This is extremely important for devices that are required to operate for long periods in the temperature range of 400°C to 800°C, which may experience multiple structural degradations, ultimately leading to device failure. Even when the transistor is still functional, the overall device performance is affected as the *I-V* characteristics may show evidence of degradation of ohmic contacts. The situation is exacerbated by further deterioration of the intrinsic noise characteristics, leading to degradation of the overall circuit performance.

Here, the LFN behaviour of two thermally stressed 4H-SiC lateral JFETs at 400°C and 500°C for 1000 hours under different bias conditions were investigated. In the process of identifying the origin of excess noise in these systems, the LFN of the transistor drain-source channel, gate junctions and transmission-line model (TLM) structures from each respective sample were examined thoroughly.

5.2 Experimental

Two batches of JFETs described in Chapter 4 were thermally aged in furnaces open to air for 1000 hours at 400°C and 500°C (denoted by TS-400 and TS-500, respectively). No electrical stress was applied to the devices during the high temperature aging process to prevent hot electron induced degradation under an external electric field [158]. *I-V* and LFN measurements were then performed after the aging period, and the results are compared to the as-fabricated devices (denoted as Non-TS). For ease of comparison, only the JFET variants with 15µm and 21µm gate length were investigated (unless stated otherwise). Despite the difference in gate length dimension, the 15µm gate length variant demonstrated identical similar LFN behaviour to the 21µm gate length transistor, matching the results presented in Section 4.3.1.II.B.

5.3 Results and Discussion

5.3.1 The influence of thermal degradation on the drain-source channel of 4H-SiC lateral JFETs

I. Electrical Characterisation

The data in Figure 5.1 show typical *I-V* characteristics of the Non-TS, TS-400, and TS-500 samples measured at room temperature. To enhance the electrical isolation between the SiC back-substrate and chuck of the probing station, these samples were placed on a 1mm thick ceramic plate during the LFN and *I-V* measurements. As can be observed from the data in Figure 5.1, the *I-V* curve of the thermally stressed sample demonstrates a monotonic decrease in both linear ($I_{DS_{lin}}$) and saturated ($I_{DS_{sat}}$) current with increasing aging temperature. The specific contact resistance for Non-TS sample is extracted as $3.18 \times 10^{-2} \Omega cm^2$ and the total channel resistance (R_{CH}) at zero gate-source voltage (V_{GS}) is 6.5kΩ. In the case of thermally stressed samples, R_{CH} shows an average increment of 4% and 120% relative to the Non-TS sample for TS-400 and TS-500 respectively. Furthermore, the $I_{DS_{lin}}$ characteristics of the thermally aged devices have been shifted by approximately 1.5V along the drain-source voltage (V_{DS}) axis (see the inset to Figure 5.1). The observed *I-V* characteristics imply that the JFET contact metallisation may undergo some form of degradation during the thermal cycle, possibly the evolution of the Ni_xSi_y alloy phases as well as oxidation of the metal stack [159], leading to the increase in contact resistances and formation of potential barriers.
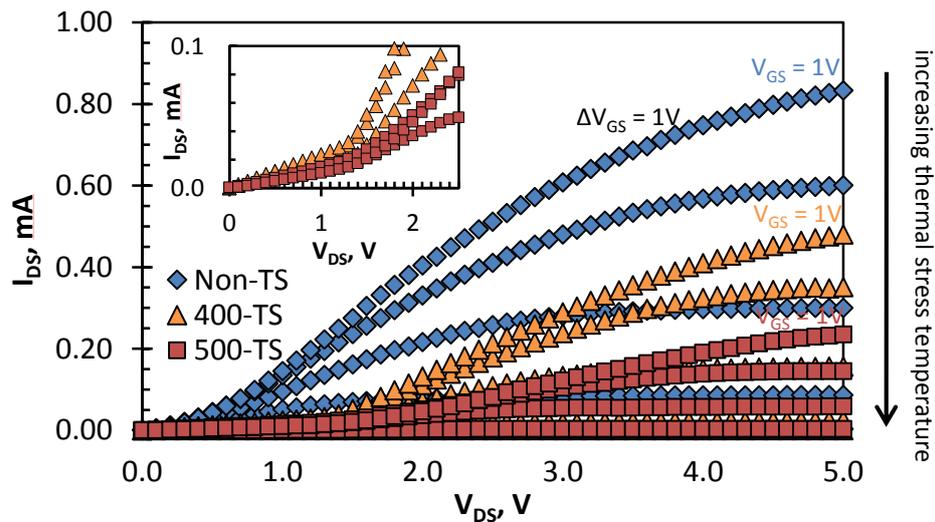
Figure 5.1: *I-V* characteristics for junction field effect transistor (JFET) with gate geometry (W/L) ratio of 200μm/21μm on Non-TS (RT), TS-400 (400°C) and TS-500 (500°C) samples. The gate-source voltage (V_{GS}) of the devices is vary from -3.0V to 1.0V with 1.0V of increment. Inset shows the zoom in on the shifted $I_{DS_{lin}}$ behavior for TS-400 and TS-500.

II. <u>Low Frequency Noise Characterisation</u>

To further examine the effect of thermal stress on the transistor characteristics, LFN measurements were performed on the drain-source channel of the devices. The data in Figure 5.2 show the channel current noise power spectral density ($S_{I_{CH}}$) for a) Non-TS and b) TS-400 and TS-500 samples as a function of frequency. The V_{GS} of the transistors were swept from −1.0V to 1.0V, while the V_{DS} were fixed within the $I_{DS_{lin}}$ region, where $V_{DS} = 2.0V$ for both thermally aged samples to compensate the shifted $I_{DS_{lin}}$-V_{DS} characteristics and the Non-TS sample was biased at $V_{DS} = 1.5$ V. There are several distinctive properties that can be observed in the data shown in Figure 5.2. First, the noise spectra of TS-400 and Non-TS samples demonstrate $1/f^{\lambda}$ behaviour for frequencies below 100Hz where the frequency exponent (λ) is equal to 1.0±0.2, before the spectrum decays into system noise at frequencies above 1 kHz. Furthermore, in spite of the superposition of a Lorentzian spectrum on the TS-400 sample, the S_{ICH} magnitude for both Non-TS and TS-400 sample are identical for all studied gate bias values. In the case of TS-500, the transistor noise spectrum demonstrates a pure $1/f^{\lambda}$ (with λ between 1.00 and 1.14) dependence up to 100 kHz without any sign of merging with the system noise. In addition, the measured S_I of the TS-500 sample is some 3 orders of magnitude higher than the TS-400 and Non-TS equivalents despite the significant reduction in drain-source current capability.

Reports in the literature describe two possible scenarios that can lead to thermal degradation of LFN in semiconductor devices: either the magnitude of the existing noise sources have increased due to the generation of crystalline defects/traps concentration [153], [154], [160], or additional noise sources have been generated due to physical degradation of components of the transistor structure, such as the contact metallisation[159], [161] or the pn-structures [154], [160]. To identify the scenario that causes the observed excess noise in the TS-500 sample, the influence of V_{GS} on the transistors LFN behaviour was investigated. Any form of deviation on the V_{GS} noise dependence between these samples can be used as an indication to discriminate between the two cases.
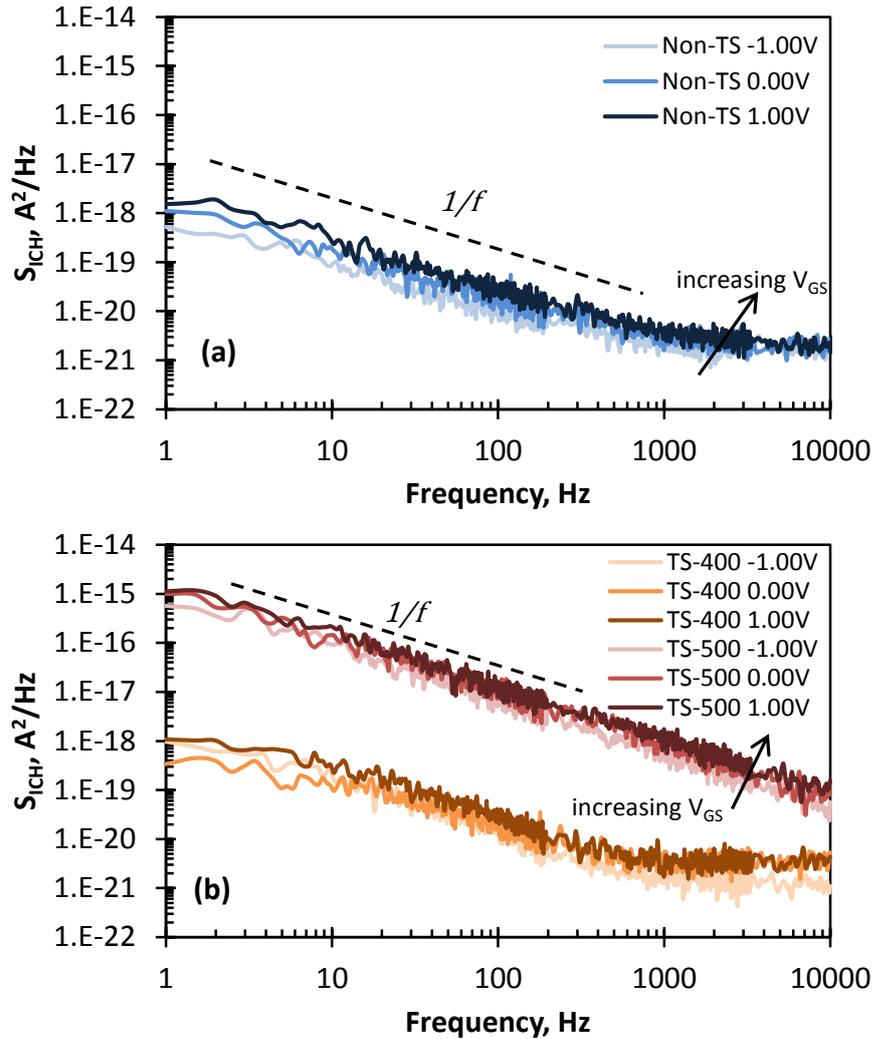
Figure 5.2: Channel current noise power spectral density (S_{ICH}) as a function of frequency on a) Non-TS and b) TS-400 & TS-500 junction field effect transistor (JFET) with gate-geometry (W/L) ratio of 200μm/21μm. Both thermally stressed and Non-TS devices were biased at drain-source voltage (V_{DS}) equals to 2.0V and 1.5V respectively, while gate-source voltage (V_{GS}) was swept from -1.0V to 1.0V with 1.0V increment.

The data in Figure 5.3 show the normalised current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) as a function of R_{CH} for all samples measured at 20Hz, 80Hz and 160Hz. The $S_{I_{CH}}/I_{DS}^2$ were acquired in the linear operating regime where $V_{DS} = 1.5V$ and 2.0V for the Non-TS and thermally stressed samples respectively, while the V_{GS} of all studied transistors was varied from -2.0V to 0.5V in 0.5V steps. The corresponding $R_{CH} - V_{GS}$ characteristics for each transistor are shown in the inset of Figure 5.3. In a broad sense, the $S_{I_{CH}}/I_{DS}^2 - R_{CH}$ behaviour of all investigated samples illustrates the typical characteristic of the 21μm gate length JFET variants, where the transistors LFN behaviour are governed by the interplay of passive and active resistivity noise components as presented in Chapter 4. In the case of the Non-TS sample, the LFN

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behaviour shows a very weak dependence with R_{CH} within the investigated V_{GS} range identical to the findings in Section 4.3.1.II.B., where the $S_{I_{CH}}/I_{DS}^2 \propto R_{CH}^{1.5}$ dependence only occurred for $V_{GS} \leq -2.0V$. In contrast, the $S_{I_{CH}}/I_{DS}^2$ behaviour of both thermally stressed samples exhibits a greater influence of the active resistivity component, as illustrated by the shift of noise transition V_{GS} from the typical -2.0V on the as-fabricated sample to -1.0V and -0.5V for TS-500 and TS-400 sample respectively. Furthermore, the observed $S_{I_{CH}}/I_{DS}^2 - R_{CH}$ dependence where the active resistive component dominates at low V_{GS} has doubled for the thermally stressed samples, where the $S_{I_{CH}}/I_{DS}^2$ for TS-500 and TS-400 samples exhibits a monotonic increase with R_{CH}^3 and $R_{CH}^{3.6}$ respectively.

Following the Series Resistor Model method described in Section 4.3.1.II.B., the observed $S_{I_{CH}}/I_{DS}^2 - R_{CH}$ behaviours on the stressed transistors contradict the observed changes on the devices DC characteristic. Theoretically, one would predict that the channel LFN is dominated by the expected degradation of the contact resistance (R_{con}) especially in the case of TS-500 sample, owing to the twofold escalation of R_{CH} due to the evolution of Ni$_x$Si$_y$ contact-alloy. Based on these assumptions and the findings in Section 4.3.1.II.B., the LFN generated by the passive resistivity components would have dominated the channel LFN behaviour, causing the extension or at least maintaining the zero R_{CH} dependence on the $S_{I_{CH}}/I_{DS}^2$ characteristics for the gate biases investigated. Nevertheless, the strong influence of the drain-source resistance (R_{DS}) regulated by the device PN junction over the $S_{I_{CH}}/I_{DS}^2$ characteristics implies that the channel LFN of the stressed JFETs are dominated by the active noise component from the channel space charge region (SCR), possibly due to the generation of additional traps/scattering centres in the n⁻ epitaxial layer.

There is however an inconsistency with this explanation, as the normalised noise magnitude of the TS-400 is almost identical to the Non-TS, while the $S_{I_{CH}}/I_{DS}^2$ of the TS-500 sample is still 3 orders higher in magnitude relative to the as-fabricated sample. Such observations complicate the situation, as one may relate the 4% and 120% of increment in R_{CH} to the small increment and 3 orders of escalation in the transistors $S_{I_{CH}}/I_{DS}^2$ magnitude observed on the TS-400 and TS-500 sample correspondingly. Therefore, it is inconclusive to determine the mechanism that leads to the observation of excess noise on the TS-500 sample based on these data alone. To examine the influence of thermally degraded R_{con} on the devices LFN behaviour, the LFN of the transmission

line model structure and the JFETs channel noise under the influence of V_{DS} are investigated in following sections.
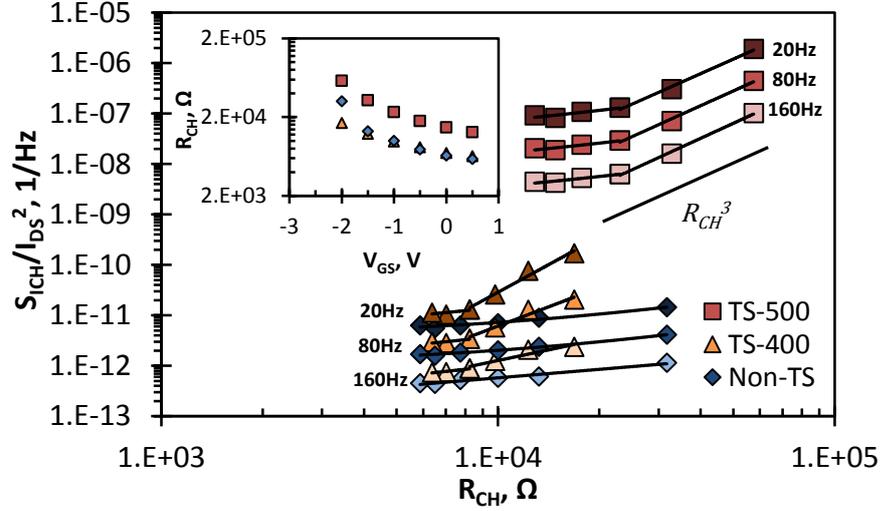
Figure 5.3: Normalised channel current noise power spectral destiny $(S_{I_{CH}}/I_{DS}^2)$ as a function of total channel resistance (R_{CH}) for all junction field effect transistor (JFET) samples with gate geometry (W/L) ratio of 200µm/21µm measured at 20Hz, 80Hz, and 160Hz. The devices were biased at fixed drain-source voltage (V_{DS}) (1.5V for Non-TS and 2.0V for TS-400 and TS-500) while gate-source voltage (V_{GS}) was stepped from -2.0V to 0.5V with 0.5V increments. Inset illustrates the corresponding R_{CH} for each respective V_{GS}.

5.3.2 The low frequency noise characteristics of thermally degraded contact metallisation on the 4H-SiC n-type resistor using Transmission Line Model (TLM) structure

The LFN of n-type transmission line model structures (denoted as TLM herein) for all investigated samples were acquired in the ohmic current regime where the devices were biased above the contact potential barrier. Since the TLM is only comprised of contact metallisation and n-epitaxy, it enables the investigation of thermal degradation on the passive resistivity components without the influence of the SCR. The data in Figure 5.4 shows the comparison of normalised TLM current noise power spectral density $(S_{I_{TLM}}/I_{TLM}^2)$ as a function of TLM current (I_{TLM}) for a) Non-TS & TS-400 and b) TS-500 samples measured at 20 Hz. The investigated contact spacing (δ_{TLM}) for these devices is 10µm and 20µm.
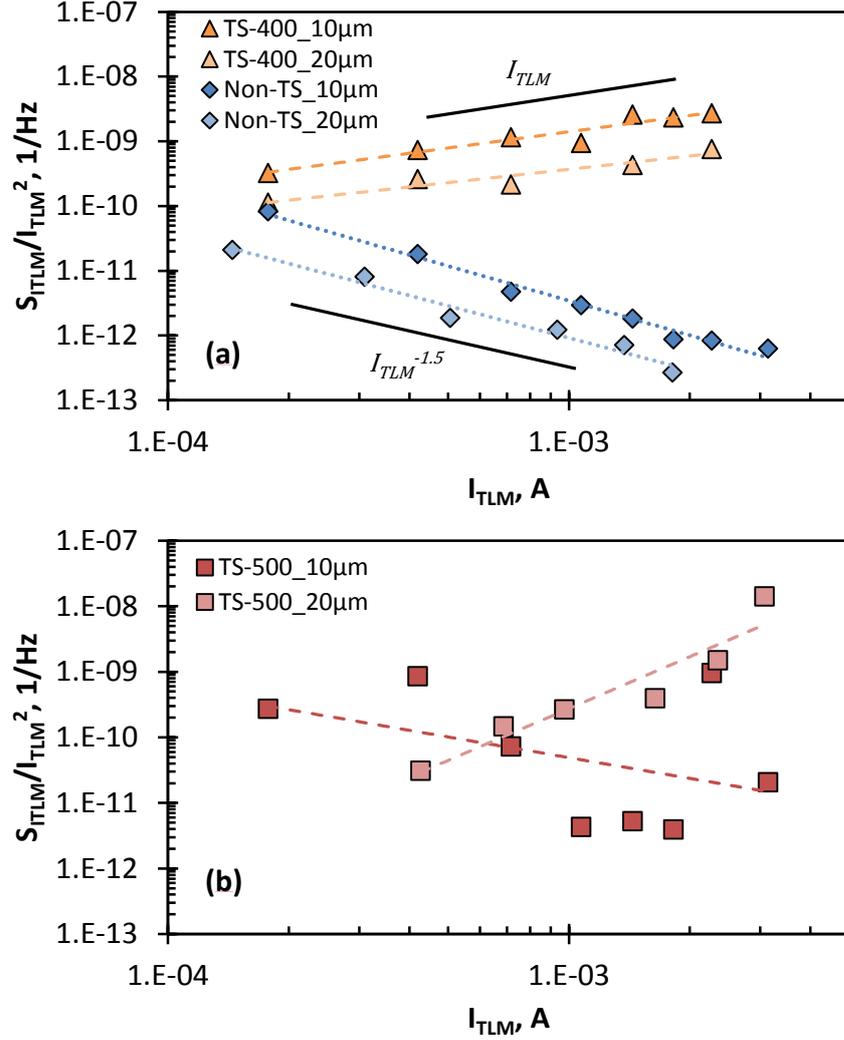
Figure 5.4: Normalised current noise power spectral density of the Transmission Line Model structure (denoted as TLM) ($S_{I_{TLM}}/I_{TLM}^2$) as a function of current (I_{TLM}) for a) Non-TS & TS-400 and b) TS-500 with contact spacing (δ_{TLM}) of 10μm and 20μm. The TLM were biased in the ohmic region from 1.0V to 5.0V.

As can be observed from the data in Figure 5.4a, both TLM structures from each sample exhibit a similar current dependence, where $S_{I_{TLM}}/I_{TLM}^2 \propto I_{TLM}^{-1.7}$ and $S_{I_{TLM}}/I_{TLM}^2 \propto I_{TLM}$ for Non-TS and TS-400 respectively. Furthermore, the normalised LFN magnitude decreases monotonically with increasing δ_{TLM} in accordance with the noise-volume scaling rule [12], [162]. On the other hand, the LFN characteristics of the TS-500 TLM data in Figure 5.4b show a unique current dependency for each δ_{TLM}. For devices with 10μm δ_{TLM}, the $S_{I_{TLM}}/I_{TLM}^2$ illustrates a random behaviour against I_{TLM}, while $S_{I_{TLM}}/I_{TLM}^2$ for the 20μm TLM increases monotonically with I_{TLM}^2.

The LFN for the Non-TS samples is non-comparable to the typical noise results reported for a bulk resistor that $S_{I_{TLM}}/I_{TLM}^2$ is weakly dependent on I_{TLM}. This may be

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due to the influence from other noise sources; including native oxide interface fluctuation, and Schottky contact like behaviour (oxidation of ohmic metallisation). Nevertheless, the $S_{I_{TLM}}/I^2_{TLM} - \delta_{TLM}$ dependence indicates that the measured LFN is still dominated by the characteristics of the bulk SiC. In the case of thermally aged samples, the TLM LFN characteristics are severely affected by the degradation of contact metallisation as seen by the escalation of noise magnitude as well as the alteration on the $S_{I_{TLM}}/I^2_{TLM}$ dependence with I_{TLM}. Despite the influence from the deteriorated Ni_xSi_y alloy stack, the TS-400 $S_{I_{TLM}}/I^2_{TLM}$ still preserves the typical noise-volume scaling characteristics indicating those originating as bulk effects. In contrast, the random noise behaviour observed in the TS-500 TLM data signifies the existence of additional contributions from other noise sources than can be explained by the effect of degraded contact noise.

Based on these findings, the degraded contact metallisation on both thermally aged samples was shown to affect the LFN performance equally, which is contradictory to the findings in Section 5.3.1. II., where only the TS-500 sample exhibits a substantial deterioration in LFN performance. In addition, the deviation of TLM $S_{I_{TLM}}/I^2_{TLM}$ magnitude between TS-500 and Non-TS sample is non-equivalent to the degree of noise escalation for the transistor channel. Therefore, the observed channel excess noise on the TS-500 sample is not caused by the superposition of series resistance noise from the evolved Ni_xSi_y metal alloy.

5.3.3 The effect of thermally degraded contact metallisation on the 4H-SiC lateral JFETs channel low frequency noise characteristics

To examine the influence of R_{con} on the JFETs LFN characteristic, the channel low frequency noise under the influence of V_{DS} was investigated. The data in Figure 5.5 shows $S_{I_{CH}}/I^2_{DS}$ as a function of I_{DS} measured at 20Hz for the three investigated samples. These transistors are biased at V_{DS} between 0.1V and 5.0V with floating V_{GS}. The corresponding I-V characteristics of the devices are plotted in Figure 5.6 on a semi-logarithmic scale with lines showing the frequency exponents as a function of V_{DS}. Utilising this configuration not only eliminates the influence of gate leakage current on the measured noise [20], it also provides a good understanding of the contact noise $(S_{R_{con}})$ contribution to the overall LFN performance as R_{CH} is mainly contributed by the contact resistance (R_{con}) component at $V_{GS} = 0.0V$. (See results in Section 4.3.1.II.B.)

As can be observed from the LFN results in Figure 5.5, the $S_{I_{CH}}/I_{DS}^2$ of the TS-500 transistor demonstrates a weak I_{DS} dependence at low V_{DS}, then the noise magnitude increases significantly, peaking at 1.5V before decreasing proportionally to I_{DS}^{-1}. On the other hand, a similar trend is observed for both TS-400 and Non-TS samples at low V_{DS}, except the $S_{I_{CH}}/I_{DS}^2$ data demonstrate a decaying nature with $I_{DS}^{-1.5}$ above 100μA. Despite the complex $S_{I_{CH}}/I_{DS}^2$ dependence with I_{DS}, the frequency exponent of the TS-500 sample demonstrates a constant λ value of -1.10 for all the biases investigated as shown by the data in Figure 5.6. In contrast, the frequency exponent of the Non-TS sample exhibits a polynomial function with V_{DS} and settles at approximately -1.06 for $V_{DS} > 3.0V$. The TS-400 LFN spectrum at $V_{DS} \leq 1.25$ V exhibits a relatively large exponent up to -1.40 and decreases monotonically with V_{DS}, before coinciding with the Non-TS polynomial behaviour for $V_{DS} > 1.25$ V.

The data in Figures 5.5 and 5.6 illustrates that $S_{I_{CH}}/I_{DS}^2 - I_{DS}$ and $\lambda - V_{DS}$ relations show a strong correlation between the channel LFN behaviour and the I-V characteristics in both thermally aged JFETs. At $V_{DS} \leq 1.25$ V, the lack of a current dependence in the $S_{I_{CH}}/I_{DS}^2$ data indicates that the observed LFN is of resistance origin, possibly due to the contact metallisation [12] (See Section 2.3.5 for the explanations). Furthermore, the effect of degraded contact metallisation can be clearly observed in the $\lambda - V_{DS}$ relation, most notably in the TS-400 data, exhibiting a relatively large exponent at low V_{DS}. Such behaviour can be elucidated by the trapping and de-trapping of carriers via the poor oxide interface formed by the oxidised Ti layer in the contact alloy [163], similar to the fluctuation mechanism in MOS-devices [160]. In contrast, the TS-500 sample solely illustrates a unity value of λ for all V_{DS} investigated, in spite of the $S_{I_{CH}} \propto I_{DS}^2$ dependence at low V_{DS}. In most cases since the LFN components are additive, the observed TS-500 noise characteristics may be due to the superposition of a higher magnitude noise mechanism originating in the SCR on top of the noisy contact alloy, resulting in the observed excess noise and distinctive $1/f$ spectrum.
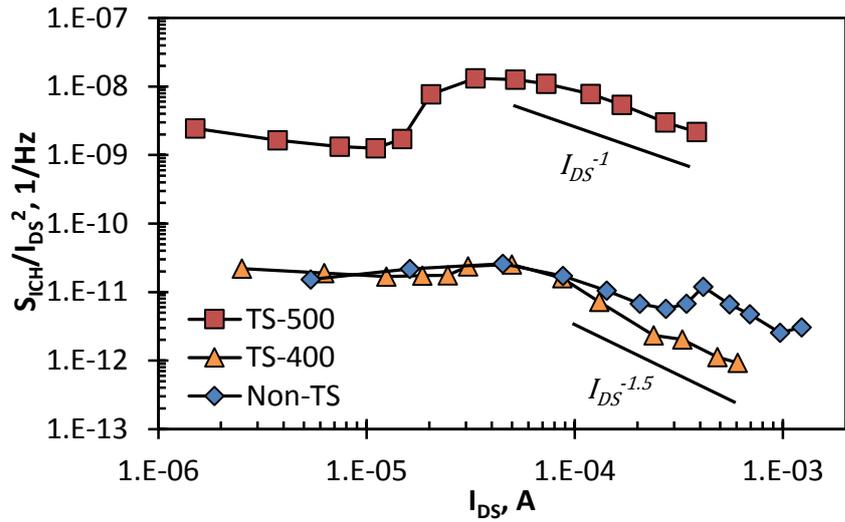
Figure 5.5: Channel normalised current noise power spectral density $(S_{I_{CH}}/I_{DS}^2)$ as a function of drain-source current (I_{DS}) for the junction field effect transistors (JFETs) with gate geometry (W/L) ratio of 200μm/15μm measured at 20 Hz for the three samples measured at 300K. The drain-source voltage (V_{DS}) of these transistor was swept from 0.1V to 5.0V while floating gate-source voltage (V_{GS}).
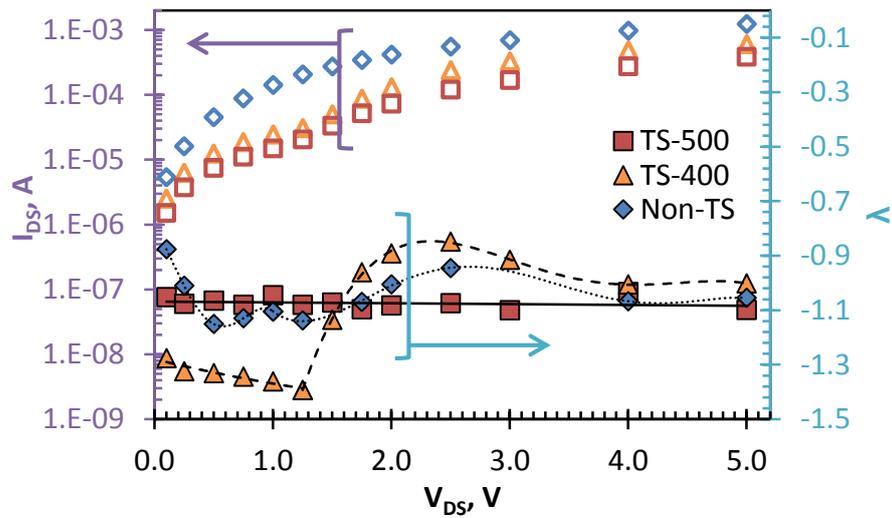
Figure 5.6: I-V characteristics and the frequency exponent (λ) as a function of drain-source voltage (V_{DS}) for the three investigated samples correspond to the LFN results in Figure 5.5.

Although the actual fluctuation mechanism for JFETs under the influence of V_{DS} is not comprehensively discussed in the literature, one would generally relate the LFN behaviour to the pinch-off process of the space charge region (SCR). For transistors biased at $V_{DS} > 1.25$ V, the measured noise characteristic is presumably caused by the transformation of channel SCR under the influence of the drain-source electric field. Hence, any changes in the $S_{I_{CH}}/I_{DS}^2 - I_{DS}$ dependency between samples would suggest some form of alteration to the fluctuation process. Following the

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expression in Equation 4.13 and assuming a similar SCR width for all investigated devices; the slower decay rate of the TS-500 $S_{I_{CH}}/I_{DS}^2 - I_{DS}$ relation in comparison to the Non-TS and TS-400 LFN behaviour indicates that the degree of carrier fluctuation $\overline{(\delta N_t^2)}$ is comparatively higher than the evolution of N_0^2 under channel pinch-off conditions. This observation further supports the likelihood of thermal stress activated trapping centres within the SCR of the n-epitaxy, enhancing the $N_t f_t f_{tp}$ term in Equation 4.13, leading to the observed excess noise in the TS-500 sample. To verify this hypothesis, two approaches were implemented. First, the LFN behaviour of the P+NN+ junction in the JFET structures under different bias conditions was investigated. Secondly, the temperature dependence of $S_{I_{CH}}/I_{DS}^2$ for the TS-500 and Non-TS with different gate geometry ratio were examined.

5.3.4 Low frequency noise characteristics of the P+NN+ gate junction on the thermally aged 4H-SiC lateral JFETs

I-V and LFN characterisation of the transistor P+NN+ junction was performed. For ease data presentation, only the results from the gate-drain P+NN+ (denoted as PN herein) structure were shown in this section. Nevertheless, the LFN and *I-V* characteristics of the gate-source junction are identical; as expected from the symmetric structure. The data in Figure 5.7 shows the semi-logarithmic plot of the absolute junction current (I_{GD}) as a function of gate-drain junction voltage (V_{GD}) for all samples. Three distinctive conduction regions can be assigned to the *I-V* curves as (i) reverse leakage, (ii) generation-combination and (iii) series resistance, corresponding to the numerical labels in Figure 5.7. When the PN structures are biased beyond the junction threshold voltage (V_{JTH}), the SCR diminishes and the junction current is regulated by the series contact resistance as illustrated by region iii in the figure. Under reverse bias conditions, the conduction mechanism in regions i and ii is modulated by the generation and recombination of electron-hole pairs in the SCR. Due to the dominance of different conduction mechanisms in these regions, the corresponding LFN characteristics can be used to verify the origin of the excess noise in the JFET channel.

As can be observed from the results in Figure 5.7, the reverse bias current for both thermally aged samples is approximately 4 orders of magnitude lower than the Non-TS device. Although the reason for this finding is unclear, it is unlikely to be caused by the superposition of series resistance from the deteriorated gate-drain contact metallisation since only the TS-500 devices suffers from major degradation in R_{Total}; instead the

shift in this *I-V* behaviour may be caused by the physical degradation of the PN structure or the intrinsic properties of the JFET channel. At low forward bias, the junction ideality factor (n) is extracted as 1.66, 1.64 and 1.27 respectively for Non-TS, TS-400 and TS-500, by means of Shockley's empirical formula for PN diode [131]. The decrement of n in TS-500 in comparison to the Non-TS and TS-400 counterparts may be explained by the carrier recombination mechanism via multilevel centres, which indicates the generation of shallow traps in the SCR based on the expression:

$$n = \frac{(s + 2d)}{(s + d)} - (5.1)$$

here s and d are the total number of shallow and deep traps in the SCR respectively [164], [165]. Following the expression in Equation 5.1, the extracted n for the Non-TS and TS-400 junctions is analogous to multi-level G-R process via 2 deep and 1 shallow traps, which resulted in $n = 5/3 \, or \, 1.67$. The reduced ideality factor in the TS-500 sample requires the generation of additional 4 to 5 numbers of shallow trapping states that produce the range of ideality factor between 1.25 and 1.29, where the corresponding n ratio is equivalent to $10/8$ or $9/7$.

The results in Figure 5.8 show $S_{I_{GD}}$ as a function of I_{GD} biased in region ii (filled) and iii (unfilled). Under forward bias conditions (shown by region iii), $S_{I_{GD}}$ exhibits a progressive increase in magnitude with increasing thermal aging temperature. In addition, the $S_{I_{GD}}$ of both thermally aged samples have transformed from a weak current dependence to $S_{I_{GD}} \propto I_{GD}$ and $S_{I_{GD}} \propto I_{GD}^{1.5}$ respectively for the TS-400 and TS-500 sample. These observations are expected as the forward junction current is heavily influenced by the superposition of Schottky like behaviour caused by the oxidation of contact metallisation stacks [166], where the $S_{I_{GD}}$ dependence in the function of I_{GD} for both thermally stressed devices exhibit a close correlation to Si based Schottky diodes [167]. Based on the report, the $S_{I_{GD}} \propto I_{GD}$ relation was described by the mobility and diffusivity fluctuation origin and the $S_{I_{GD}} \propto I_{GD}^{1.5}$ characteristic may be caused by the random walk of carriers via interface states [167]. In addition, $S_{I_{GD}}$ under forward bias for thermal stressed samples appears to scale proportionally with R_{CH}, where $S_{I_{GD}}$ is enhanced by an order of magnitude for TS-500, while a small increment in $S_{I_{GD}}$ was observed on TS-400 at the transition point between regions ii and iii. As can be observed from the $S_{I_{GD}}$ behaviour in region ii, the noise results can be correlated to the

junction ideality factor. For the PN structures that share an identical n, the $S_{I_{GD}}$ of Non-TS and TS-400 samples shows a current dependency of 1.5 similar to the results reported in asymmetrical P+N junction [150]. Whilst, the degraded TS-500 sample demonstrates an enhanced dependence with $S_{IGD} \propto I_{GD}^{1.7}$. Furthermore, the S_{IGD} of TS-500 is at least an order higher than that observed in the Non-TS sample, which indicates that the carrier fluctuation parameters ($N_t f_t f_{tp}$) given by Equation 4.13 have increased.
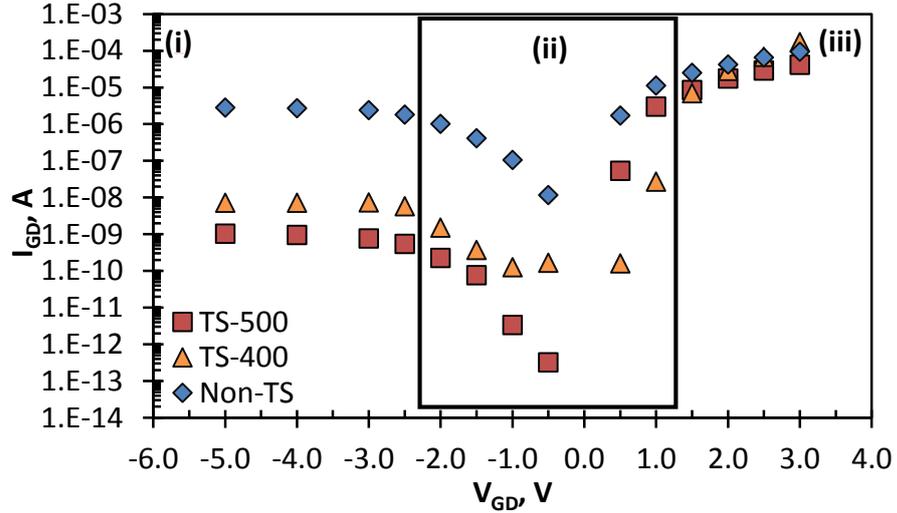
Figure 5.7: *I-V* **characteristics of the gate-drain P+NN+ junction with** W/L **ratio of 200μm/15μm for Non-TS, TS-400 and TS-500 sample. The gate-drain junction voltage (V_{GD}) is varied from -5.0V to 3.0V. The numerical labels highlight the three distinctive current conduction mechanisms: i) reverse leakage, ii) generation-combination and iii) series resistance effect.**
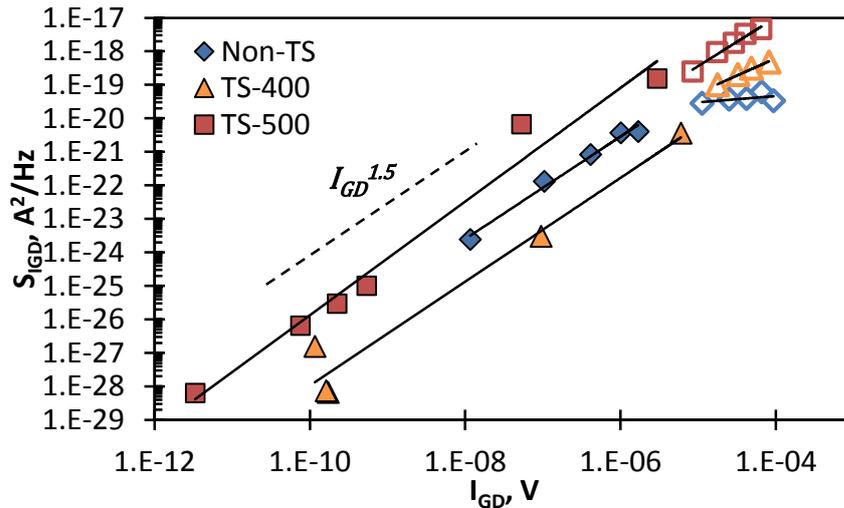
Figure 5.8: Current noise power spectral density of the gate-drain junction ($S_{I_{GD}}$) as a function of I_{GD} on junction field effect transistor (JFET) with 200μm/15μm gate geometry (W/L) ratio for all investigated samples measured at 20Hz. The PN structures were biased in region ii (filled) and iii (unfilled) corresponding to the *I-V* characteristics in Figure 5.7.
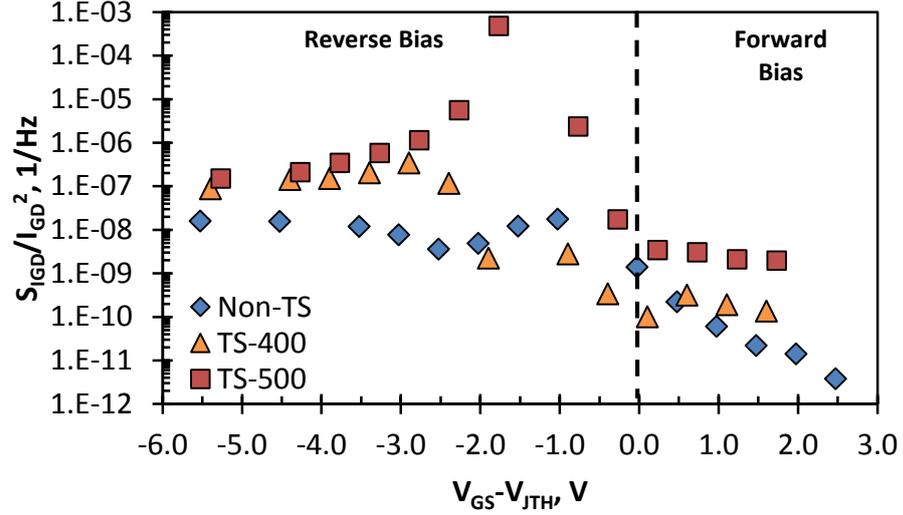
Figure 5.9: Normalised current noise power spectral density of the gate-drain junction ($S_{I_{GD}}/I_{GD}^2$) as a function of junction potential ($V_{GD} - V_{JTH}$) on junction field effect transistor (JFET) with 200μm/15μm gate geometry (W/L) ratio for all investigated sample measured at 20Hz.

The evolution of $N_t f_t f_{tp}$ under the influence of V_{GD} was investigated by plotting $S_{I_{GD}}/I_{GD}^2$ measured at 20 Hz against the junction potential ($V_{GD} - V_{JTH}$) as shown by the data in Figure 5.9. The junction turn-on voltage (V_{JTH}) was extracted utilising the standard mathematical method based on the forward bias $I_{GD} - V_{GD}$ relation in region ii and the V_{JTH} for each PN structure are computed as 0.53V, 1.40V and 0.69V respectively for Non-TS, TS-400 and TS-500. As can be observed from the data in Figure 5.9, $S_{I_{GD}}/I_{GD}^2$ increases monotonically for $V_{GD} - V_{JTH} < 0V$ (i.e. when the SCR is formed for all investigated samples), before it reaches a device specific maxima and subsequently decays. As the junction potential becomes more negative, the $S_{I_{GD}}/I_{GD}^2$ of the Non-TS sample rises gradually until $V_{GD} - V_{JTH} = -2.5V$ before settling at 1.6×10^{-8} 1/Hz, whereas the $S_{I_{GD}}/I_{GD}^2$ of TS-400 shows a weak $V_{GD} - V_{JTH}$ dependence and converges with the noise behaviour of TS-500 at $V_{GD} - V_{JTH} \leq -3.0V$. The LFN results in Figure 5.9 clearly demonstrate the abnormality in the TS-500 LFN behaviour, where the maximum value of $S_{I_{GD}}/I_{GD}^2$ is at least 4 orders of magnitude greater than in either Non-TS or TS-400.

The observed LFN behaviour in Figure 5.9 can be elucidated by the trap assisted G-R processes occurring in the SCR, as reported previously [132], [150], [168]. Due to the nature of device physics of a PN junction, this version of the G-R model differs slightly from that presented in Section 4.3.1 II. A. The G-R fluctuation in a PN junction

is an indirect mechanism that leads to the manifestation of LFN and may be described by means of a carrier fluctuation that alters the electric field within the PN junction, resulting in electrostatic potential difference across the SCR. Following Equations (4.10) and (4.13), the features in the $S_{I_{GD}}/I_{GD}^2 - V_{GD}$-$V_{JTH}$ data shown in Figure 5.9 may be explained by the alignment of the quasi-Fermi energy with the corresponding trap energy as the SCR evolves under the application of an external electric field. In the case of the TS-500 data, the observed increment in the $S_{I_{GD}}/I_{GD}^2$ magnitude is a consequence of the enhanced generation-recombination mechanism via the additional trapping centres generated during the thermal aging process.

5.3.5 Temperature dependent of low frequency noise of the 500°C aged 4H-SiC lateral JFETs

To examine and verify the extensive generation of trapping centres throughout the SiC die subjected to 500°C aging, the LFN behaviours of JFETs with different gate dimension were acquired. The results in Figure 5.10 illustrate $S_{I_{CH}}/I_{DS}^2$ as a function of operating temperature (T) for the TS-500 JFETs with gate geometry (W/L) ratio of a) 200/21µm, b) 50/21µm, c) 200/9µm and d) 50/9µm. These devices were biased at a fixed V_{DS} of 3.0V while V_{GS} is left floating. The dashed lines in these figures highlight the temperatures at which the $S_{I_{CH}}/I_{DS}^2$ maxima are observed on the spectrum.

As can be observed from the data in Figure 5.10a and b, the $S_{I_{CH}}/I_{DS}^2$ characteristic of the 21µm gate length JFETs has transformed from a monotonic dependence as was demonstrated by the data in Section 4.3.2 II. to a more complex behaviour. In the case of the 200/21µm devices, the $S_{I_{CH}}/I_{DS}^2$ data shows a weak T dependence at low temperatures then the noise magnitude escalates rapidly at approximately 480K, peaking at 540K before it decrease with further increases in temperature. While, the $S_{I_{CH}}/I_{DS}^2$ data for the 50/21µm variant shows an identical trend with the 200/21µm transistor at temperatures below $430K$, the observed $S_{I_{CH}}/I_{DS}^2$ decays monotonically with further increase in operating temperature.
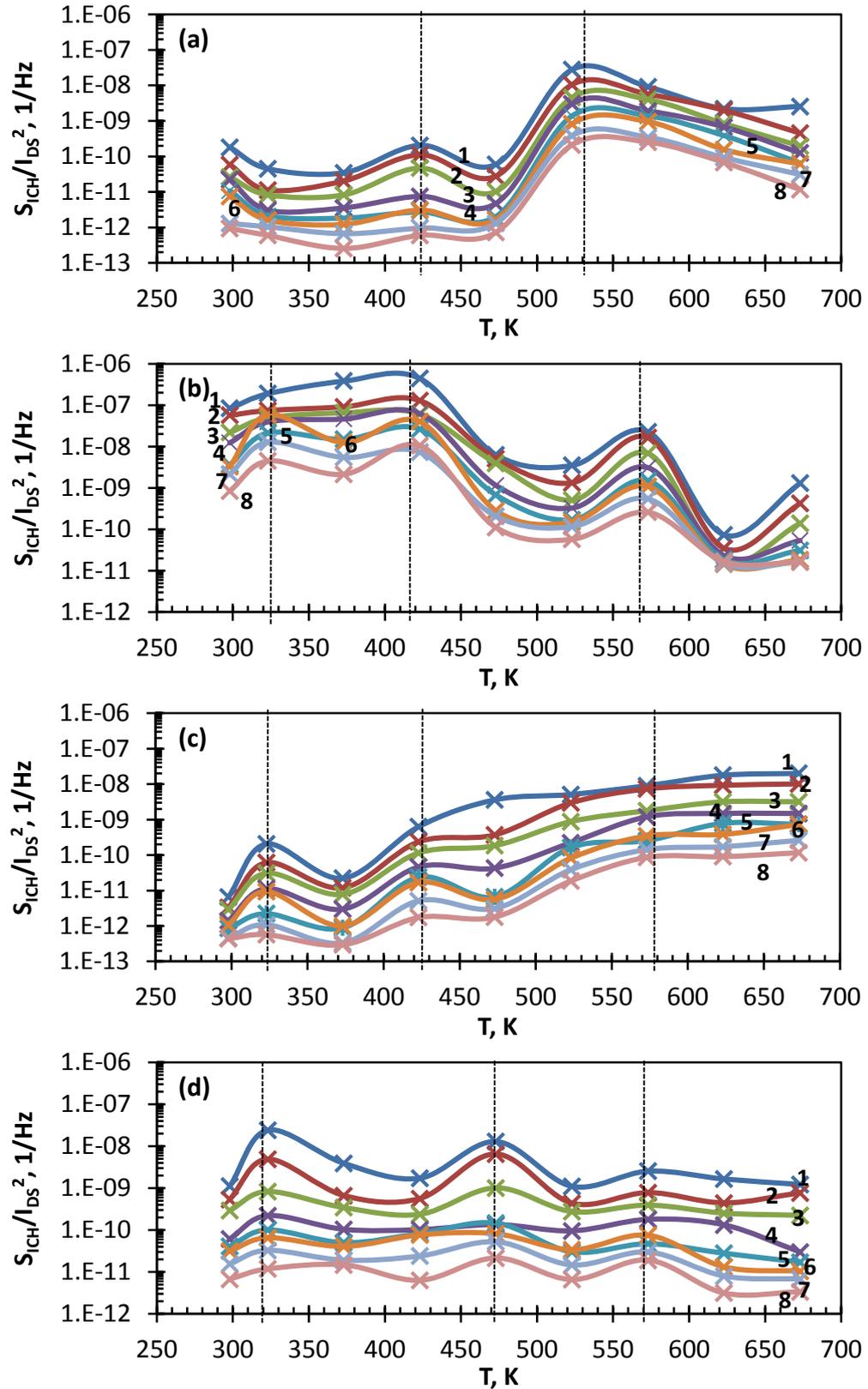
Figure 5.10: Normalised channel current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) as a function of operating temperature (T) for the TS-500 transistors with gate geometry (W/L) ratio of a) 200/21µm, b) 50/21µm, c) 200/9µm and d) 50/9µm. $S_{I_{CH}}/I_{DS}^2$ is measured at frequency: 1–10Hz, 2–20Hz, 3–40Hz, 4–80Hz, 5–160Hz, 6–200Hz, 7–420Hz and 8–850Hz. The drain-source voltage (V_{DS}) of the transistors is biased at 3.0V while floating the gate-source voltage (V_{GS}).

Aside from the changes in the $S_{I_{CH}}/I_{DS}^2 - T$ behaviour, the $S_{I_{CH}}/I_{DS}^2$ for the 21μm gate length variants demonstrate multiple noise maxima throughout the investigated temperature range. In contrast, the LFN characteristics in Figure 5.10c and d show the typical $S_{I_{CH}}/I_{DS}^2$ behaviour for the 9μm L JFETs. It is noteworthy to highlight that the $S_{I_{CH}}/I_{DS}^2$ magnitude for some transistors at 298K does not match with the level of excess noise obtained in Section 5.3.1.II. Such variations may be due to the fixed drain-source bias, leading to the measurement of unique LFN sources that dominate the different operating regime of the $I_{DS} - V_{DS}$ relation, similar to those $S_{I_{CH}}/I_{DS}^2 - I_{DS}$ data observed in Figure 5.5.

Following the models published in the literature [143], [145], the unique $S_{I_{CH}}/I_{DS}^2 - T$ behaviour is caused by the temperature dependence of the capture cross-section of trapping centres (σ) and the temperature modulated empty/electron filled trap level occupancy fraction (f_t/f_{tp}), which gives the distinct time constant of noise spectrum (T_t) and the $S_{I_{CH}}/I_{DS}^2$ maxima characteristics. Nevertheless, the noise maxima temperature (T_{MAX}) as illustrated by the dashed lines in Figure 5.10 are rather similar among the frequencies investigated, which implies a weak dependence of the capture cross-section (σ) with T, indicating the method described in [31] and [32] cannot be used to extract E_T from these results.

The observed $S_{I_{CH}}/I_{DS}^2 - T$ results in Figure 5.10 enable a qualitative study on the trap centres responsible for the noise manifestation in TS-500. Since the $S_{I_{CH}}/I_{DS}^2 - T$ relation is equivalent to the Arrhenius behaviour, the observation of $S_{I_{CH}}/I_{DS}^2$ maxima at an elevated T yields a higher activation energy for the generation-combination centres, corresponding to a deeper energy trap. Based on this assumption, the observed $S_{I_{CH}}/I_{DS}^2$ maxima at the specific operating temperature can be associated with the alignment of quasi-Fermi energy (E_{FN}) with the respective energy level of defect centres (E_T) as E_{FN} is increased by changes in operating temperature. The E_{FN} value can be approximated as:

$$E_{FN} \cong \frac{kT}{e} ln\left(\frac{N_{C_T}}{N_D}\right) - \quad (5.2)$$

here k is the Boltzmann constant, e the elementary charge and N_{C_T} the effective density of states for 4H-SiC as a function of T and is expressed as $N_{C_T} \cong 3.25 \times 10^{15} T^{1.5}$.

As seen from the data shown in Figure 5.10, a number of T_{MAX} values can be observed as occurring regularly amongst the investigated devices at 325K, 430K and 520K, which can be translated into a trap energy level with respect to E_C of -0.14eV, -0.21eV and -0.26eV. The trap species responsible for these energy levels may be related to Titanium [146], [148], [149] and/or Chromium [146] impurities, as well as the single plane stacking fault [148], [149]. The correlation of excess noise with the additional G-R centres created by the Ti based impurities is more likely and is in agreement with the observed Ti incorporation into the SiC as illustrated by second ion mass spectrometry (SIMS) analysis [169]. This is thought to be due to thermal migration during the 500°C stressing period. Based on these results, the excess $S_{I_{CH}}/I_{DS}^2$ observed on the TS-500 devices is considered to arise from the generation of additional shallow energy trapping states that enhance the carrier fluctuation process. These findings are in agreement with the alternation of the $S_{I_{CH}}/I_{DS}^2 - I_{DS}$ dependence of the drain-source channel under the influence of V_{DS}, the reduced ideality factor and the excess $S_{I_{GD}}/I_{GD}^2$ peak of the P+NN+ structures.

5.4 Summary

The *I-V* characteristics of both thermally aged samples illustrate an increase in the contact resistance and formation of a potential barrier at $V_{DS} \leq 1.25$ V due to the changes in of the contact metallisation. The channel resistance for TS-400 and TS-500 samples were discovered to have increased by 4% and 120% respectively relative to the as-fabricated devices (Non-TS). In addition, the LFN characteristics of the TS-500 devices were found to be significantly deteriorated, where the channel noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) is elevated by at least 2 orders in comparison relative to the Non-TS sample. In contrast, the TS-400 sample exhibits a slight increment in $S_{I_{CH}}/I_{DS}^2$. Moreover, the V_{GS} modulated $S_{I_{CH}}/I_{DS}^2 - I_{DS}$ relation demonstrates that the channel LFN of both thermally stressed transistor samples is dominated by the active resistance component of the JFETs PN junction, instead of the channel passive resistances as observed on the 21μm gate length JFET variants in Chapter 4.

The investigation of the LFN characteristics reveals that the P+NN+ junction current noise power spectral density ($S_{I_{GD}}$) for the TS-500 sample biased in the generation-recombination (G-R) current dominated operating regime follows a $S_{I_{GD}} \propto I_{GD}^{1.7}$ behaviour, which deviated from the $S_{I_{GD}} \propto I_{GD}^{1.5}$ dependence observed on the Non-

TS and TS-400 samples. Such findings coincide with the decrease in ideality factor observed on the TS-500 P+NN+ structure, which indicates that the junction current is dominated by an enhanced multi-level generation-recombination (G-R) process due to the presence of additional shallow traps. Furthermore, the $S_{I_{GD}}/I_{GD}^2$ plot as a function of junction potential $(V_{GD} - V_{JTH})$ for TS-500 P+NN+ structure illustrates a 6 order of magnitude increase in $S_{I_{GD}}/I_{GD}^2$ for $V_{GD} - V_{JTH}$ between 0.0V and -3.0V, which suggests the elevation of carrier fluctuation on the 500°C stressed sample.

The examination of the $S_{I_{CH}}/I_{DS}^2$ behaviour with the operating temperature on the TS-500 transistors, with different gate geometry ratios validates the hypothesis that there is a generation of additional shallow trapping centres in the JFETs SCR for the TS-500 devices. As observed from the $S_{I_{CH}}/I_{DS}^2 - T$ results, the temperature dependence of $S_{I_{CH}}/I_{DS}^2$ for both 9μm and 21μm gate length variants has been transformed from a conventional $S_{I_{CH}}/I_{DS}^2 - T$ behaviour unique to each respective gate length to the observation of multiple $S_{I_{CH}}/I_{DS}^2$ maxima within the investigated temperature range. These $S_{I_{CH}}/I_{DS}^2$ maxima were consistently observed in the data, which can be linked to the existence of additional trapping states. Such findings are consistent with the changes in the $S_{I_{CH}}/I_{DS}^2$ behaviour of the JFETs under the influence of V_{GS} and V_{DS} as well as the modification of the P+NN+ junction ideality factor and the $S_{I_{GD}}/I_{GD}^2$ trend biased in the generation-recombination dominated operating regime on the TS-500 sample.

Chapter 6: Low Frequency Noise in Atomic Layer Deposited High-κ Top-Gated Epitaxial Graphene Field Effect Transistors

6.1 Introduction

The high carrier mobility, Fermi velocity and thermal conductivity position graphene as a prospective candidate for the realisation of terahertz grade transistors with broad band capability [170], [171]. Whilst the zero-band gap behaviour of as-grown graphene is not suitable for conventional CMOS circuitry, its electrical properties are highly compatible with RF applications as the circuit operation does not mandate the transistor to switch off completely. Due to its unique and superlative transport properties [6], graphene may well be the potential alternative or replacement for existing III-V technology in the coming decade as III-V device capabilities are capped at a cut-off frequency of 850GHz and a maximum oscillation frequency of 1.2THz [6].

The existence of wafer scale production and fabrication process steps compatible with existing Si technology are the stringent requirements to enable the commercial realisation of such transistor technology. Among all graphene synthesis process, epitaxially grown graphene through low pressure sublimation of SiC substrate (denoted as epitaxial graphene or EG) not only fulfils the criteria of large scale manufacturing; also the electrical and material properties of synthesized graphene are far superior to the other wafer scale counterparts. For example, mechanically exfoliated (ME) or chemical vapour deposition (CVD) has an inherent back gated structure owing to the material synthesis process, which involves transferring the grown graphene sheet/flake onto a host material, commonly a Silicon substrate with SiO_2 layer. The lack of native oxide on epitaxial graphene requires the integration of alternative materials as a top-gate structure to construct transistors.

Results reported in the literature have described attempts of direct oxide formation on graphene films based on using physical vapour deposition (PVD) [172]–[174], atomic layer deposition (ALD) [175]–[178], pulsed laser deposition (PLD) [179] and a physical assembly process [172], [180]. ALD is currently the preferred technique amongst these options because of the low processing temperature and precise regulation of both the oxide thickness and the chemical composition, leading to the formation of conformal, high quality, and ultrathin dielectric films. However, the nature of ALD

process requires a reactive species on the targeted surface to initiate the nucleation process and enhance the oxide-semiconductor adhesion. The hydrophobic nature and chemical inertness of graphene hampers the fabrication of high quality dielectric layers with uniform coverage. Therefore, an optimum surface modification with minimal deterioration to the transport properties on the as-grown graphene is required to facilitate the bonding of oxide precursors.

Techniques for graphene surface modification in the effort to enable gate oxide formation have been proposed and demonstrated based on ozone and NO_2 pre-treatment [177], [181], [182], formation of a seed layer via electron beam deposited oxide [182], [183], oxidation of electron beam deposited metal [176], [182], [184], spin-coating of buffered low-κ polymer [182], [185], [186], hydrogen and fluorine surface functionalisation [176], [182], [187], and wet chemical surface treatment [188]. Although some of these methods illustrate good figures of merit in oxide coverage on the targeted graphene surface, the treated graphene sheet/flake shows evidence of degradation in structural and/or electronic properties. Among these options, the Fluorine functionalisation technique was demonstrated as a feasible surface preparation process in forming conformal and thin oxide layers without degrading the transport properties [187]. Reports have previously shown that by regulating the functionalised graphene surface to 6%-7% Fluorine coverage creates an optimum level of the ALD reaction site, leading to a better adhesion of the oxide precursor and subsequently uniform growth of high quality oxide thin films. In addition, the post ALD graphene film exhibits a 15%-25% improvement in Hall mobility relative to the as-grown graphene sheet [187].

Following the discussion in previous chapters, it is well known that in analogue and high frequency transistor design, the naturally occurring low frequency noise (LFN) caused by the random fluctuation of conductance serves as a critical metric in limiting device operability. In the case of RF applications, the LFN can be up-converted and observed as a form of phase noise in the output signal, distorting a broad frequency range [17]. Additionally, the LFN performance has tremendous impact in governing the signal to noise ratio (SNR) of the system, restricting the minimum input signal that can be amplified above the system noise floor. The inverse function of LFN magnitude with the device volume (or area for 2D material) defines the intrinsic limitation on how small a transistor can be miniaturized before the device signal is comparable to the generated noise current [189]. Therefore, investigating the LFN characteristics of top-gated epitaxially grown graphene field effect transistors (TG-EGFET) offers a better

understanding on the physics of noise manifestation in EG devices as well as facilitating the optimisation and realisation of THz grade transistors.

In this chapter, the LFN performance of fluorine pre-treated ALD gated graphene field effect transistors is investigated. These samples were grown, designed and fabricated by Dr. Virginia Wheeler and Dr. Nelson Graces in the Naval Research Laboratory in Washington DC, United States. The influence of the gate dielectric material, device operation, gate hysteresis effect, wafer mapping and LFN noise scaling of TG-EGFET were explored and discussed in a comprehensive manner.

6.2 Experimental

The EG samples investigated in this chapter are grown on a 16mm×16mm semi-insulating 6H-SiC (0001) substrate with an off-cut angle of 0.03° via the synthesis method described in [74]. The grown EG samples have a "screw" like surface morphology with spiral hexagonal steps around the threading screw dislocation pits. The representative scanning electron microscopy (SEM) and atomic force microscopy (AFM) imaging on a section of the surface morphology of EG sample is illustrated in Figure 6.1a and b respectively. Drain-source structures of the transistors were patterned via standard photolithography technique using LOR/S1811 photo-resist, followed by the deposition of Ti/Au (10nm/100nm) using e-beam evaporation. These samples then underwent lift-off process in warm acetone. The corresponding Raman, AFM and XPS results for these samples were published elsewhere [187].

I. Fluorine Functionalisation

To facilitate the formation of top-gated dielectric layer, the graphene surface is treated with XeF_2 using Xactix X3 etcher prior to the deposition of Al_2O_3 and HfO_2 via ALD. An accumulative 120s fluorination period is performed on the graphene samples through 6 individual pulses with duration of 20s each, while maintaining the XeF_2 and N_2 carrier gas at constant partial pressures of 1 and 35 torr respectively. Any residual gases not reacted with the graphene surface were purged by performing 10s of chamber evacuation at the end of each pulse cycle. This fluorination recipe produces an optimum Fluorine density of ~6.5% on the graphene surface whilst preserving the intrinsic transport properties of the synthesized graphene [190].

II. Atomic Layer Deposition

The Al_2O_3 and HfO_2 dielectrics were deposited utilising thermal ALD in a Cambridge Nano-Tech Savannah 200 system operating at 225°C on two fluorinated EG

samples. Trimethyl-aluminum (TMA) and tetrakis-ethylmethylamido-hafnium (TEMAH) precursors were used to form the Al_2O_3 and HfO_2 dielectric with deionised (DI) water acting as the oxygen source. The two high-κ dielectric materials were deposited at a growth rate of ~1.2Å/cycle; following an in-situ initial DI water pulse sequence consisting of 20 consecutive pulses to initialise the ALD. Measurement on a separate Si witness/control sample indicates that the deposited Al_2O_3 and HfO_2 dielectrics have thicknesses of approximately 18.3nm and 17.1nm respectively.

I-V, *C-V*, Hall Effect and LFN measurement were performed on these samples after 12 months of storage period in N_2 filled container. All measurements were performed at room temperature. The investigated device structure includes hall cross and hall bar configuration, each with a critical graphene area of 80μm^2 (20μm×4μm each channel) and 1200μm^2 (120μm×10μm). Figure 6.1c and d show optical microscopic-graphs of the gated hall cross and hall cross structures as well as the device schematic cross-section. Each sample has a total 12 identical dies processed using the same photolithography mask, which are arranged evenly across the 16mm×16mm substrate. The corresponding wafer map and the labels denoting the position of the test devices are illustrated in the inset of Figure 6.1e.
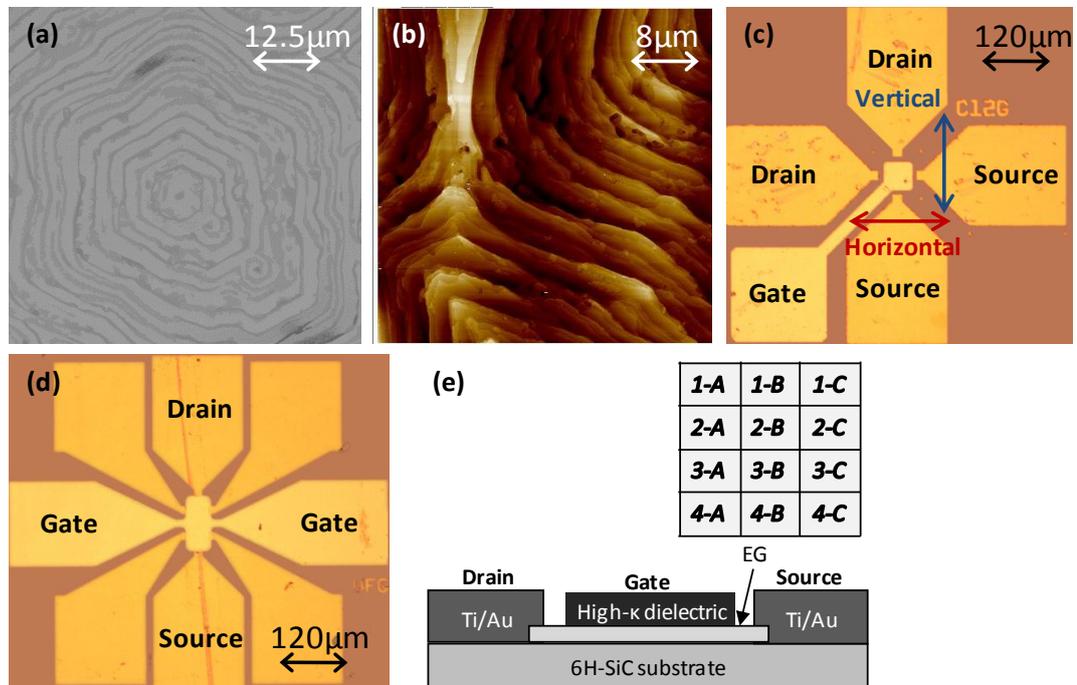
Figure 6.1: a) Scanning electron microscopy (SEM) and b) atomic force microscopy (AFM) imaging for the surface morphology of as-grown epitaxial graphene (EG). Microscopic imaging of the top-gated graphene field effect transistors (EG-EGFET) on the c) hall cross and d) hall bar device structure. e) Schematic cross-section of the EG-EGFET and the inset illustrates the die location.

6.3 Results and Discussion

6.3.1 Influence of the atomic layer deposited high-κ dielectric layer on epitaxially grown graphene.

The comparison of *I-V* characteristics between bare (ungated) and gated EG devices taken using the hall cross configuration is illustrated in Figure 6.2 a and b for the 1) Al_2O_3 and 2) HfO_2 gate dielectrics respectively. *I-V* characteristics were measured by varying the drain-source voltage (V_{DS}) of the horizontal channel (See the inset in Figure 6.1c and e) from -3.0V to 3.0V while floating the gate-source voltage (V_{GS}) to minimise the influence of oxide charge interaction with the graphene channel*[2]. For ease of comparison, only the electrical characteristics for the horizontal channel are presented in this section. Due to the circular surface morphology of the SiC substrate, the active channel of the graphene devices is intrinsically perpendicular to the SiC steps, with multiple steps being located within the active device, regardless of the channel orientation. Hence, it is worth mentioning that both horizontal and vertical channel device exhibits similar electrical properties, due to the surface morphology of the SiC substrate, contrary to previous reports [191].

As can be seen from the results in Figure 6.2, the *I-V* curves of the bare EG devices from the Al_2O_3 sample demonstrate a large variation in drain-source current (I_{DS}) among the 5 investigated devices. The total channel resistance (R_{CH}) in average of this dataset is $1.75 \times 10^4 \Omega$ with a relative maximum and minimum deviation (denoted as Δmax and Δmin) of 48.9% and 47.2% respectively. In contrast, the Al_2O_3 gated hall cross structures show highly reproducible *I-V* characteristics with an averaged R_{CH} at $1.12 \times 10^4 \Omega$. As anticipated from the observed uniform DC behaviour, the I_{DS} deviation for the Al_2O_3 gated devices are significantly smaller than the bare devices, resulting in an uncertainty of 12.5% and 8.7% of Δmax and Δmin. Furthermore, the *I-V* curve for the hall structure devices for the gated Al_2O_3 sample shows evidence of I_{DS} saturation for the gated hall cross at high bias, whereas the bare graphene devices exhibit an excellent ohmic behaviour throughout the investigated V_{DS} range. This observation may be related to the influence of the top oxide gate, possibility due to the interaction of trapped charges in the graphene-oxide interface.

[*2] A similar I-V measurement with grounded gate terminal exhibits an enhanced current saturation effect, where the drain-source current (I_{DS}) starts to saturate at a lower channel voltage (V_{DS}) than those observed in Figure 6.2. Furthermore, the total channel resistances (R_{CH}) were affected for both investigated samples. This observation is more pronounced in the HfO_2 dielectric possibly due to the presence of mobile charge in the oxide-graphene interface.
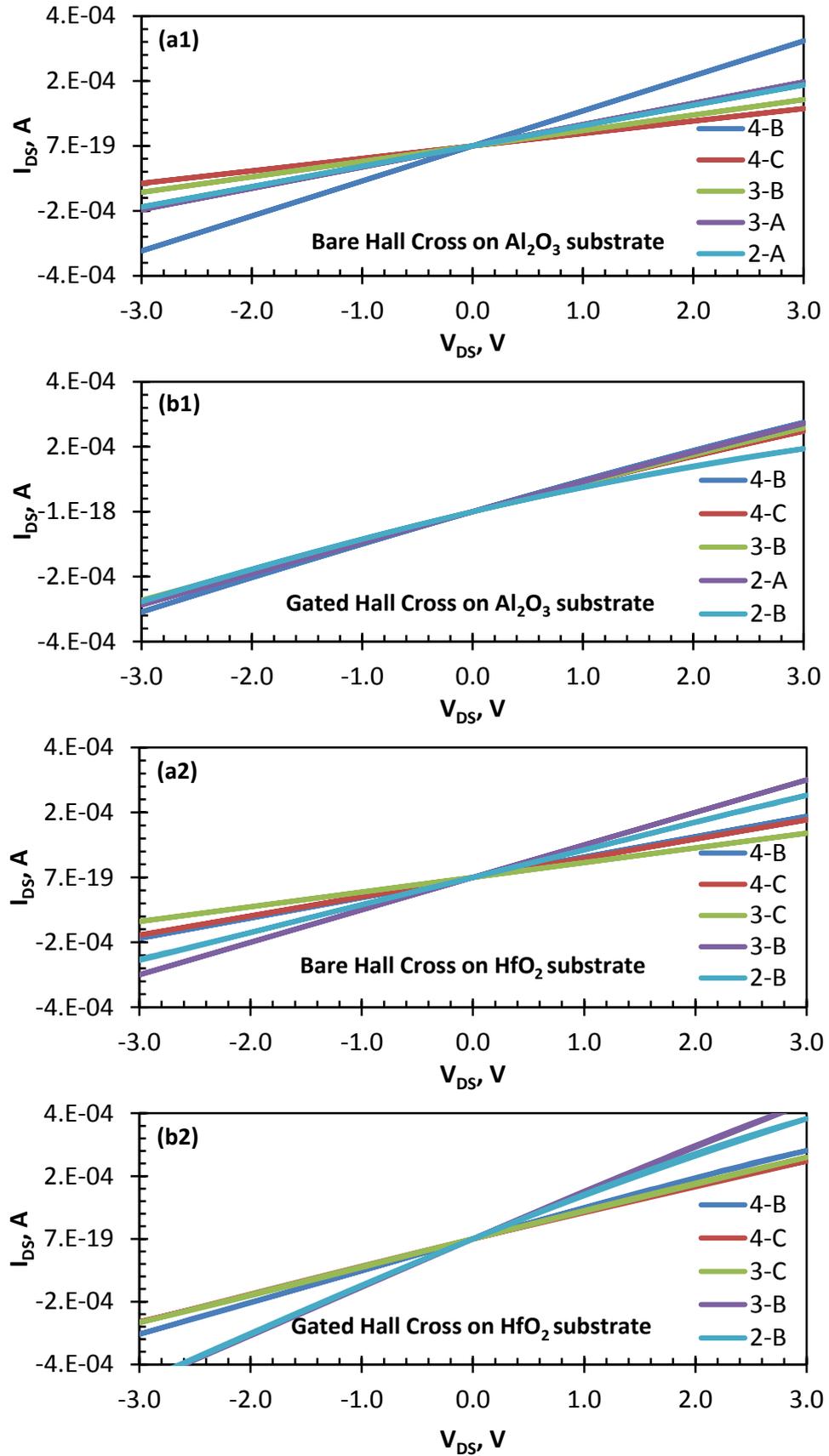
Figure 6.2: *I-V* **characteristics for the graphene hall cross structures with 1) bare and 2) gated configuration on the a) Al₂O₃ and b) HfO₂ gate dielectric sample. The devices gate-source voltage (V_{GS}) is left floating and the drain-source voltage (V_{DS}) is varied from -1.0V to 1.0V.**

In the case of the HfO_2 sample, the *I-V* trend on the non-gated hall cross structure illustrates an identical data trend to its non-gated Al_2O_3 samples, where the devices demonstrate a significant spread in R_{CH}. This dataset yields an average R_{CH} of $1.54 \times 10^4 \Omega$ with $\Delta max = 43.6\%$ and $\Delta min = 34.9\%$. In contrast to the Al_2O_3 devices, the *I-V* curve of the HfO_2 gated transistors demonstrates a larger variation in I_{DS}, exhibiting a non-ohmic behaviour at a much lower V_{DS}, which is 1.0V for some devices. The averaged R_{CH} for these transistors is $1.92 \times 10^4 \Omega$ while the Δmax and Δmin is 22.6% and 27.1% respectively.

From the data shown in Figure 6.2, it can be clearly observed that the *I-V* characteristics for all the bare graphene devices investigated demonstrate a huge variation in comparison to the gated graphene devices. Although the reason behind this phenomenon is unclear, it may be in part due to the prolonged storage duration and the exposure to different ambient environment during test routine. The un-gated graphene film may undergo some degree of atmospheric aging, leading to the doping of the graphene film and hence the modification on the observed R_{CH}. This issue is commonly reported in the literature and may be rectified utilising the in-vacuo or forming gas thermal and/or current annealing process [192], [193]. Conversely, the excellent consistency in the *I-V* characteristics for the gated hall-cross devices under investigation implies that the atomic layer deposited gate dielectric offers a good level of protection from the doping caused by foreign absorbates. These features are ideal to electro-statically regulate the electronic properties of the graphene channel, as well as shielding it from foreign contamination, a key step to enable practical circuit applications. It is questionable if the increased variations in R_{CH} and low I_{DS} saturation voltage for the HfO_2 gated samples relates to process deformities arising from the material synthesis and/or the gate dielectric deposition, nevertheless the changes in the channel *I-V* characteristics induced by grounding the gate-source terminal suggest that the oxide-graphene interface may have a greater role in defining such phenomenon.

To further investigate the impact of the top-gate structure on the electrical properties, the LFN behaviour of the hall cross structures was obtained by floating the gate contact and stepping the V_{DS} from -1.0V to 1.0V for the structure shown in Figure 6.2. The advantages of using LFN characterisation are that the technique is easy to employ and offers a highly sensitive macroscopic overview of the microscopic anomalies of the intrinsic material. Hence, any structural deformities due to the ALD

process can be easily differentiated by comparing the LFN behaviour of bare and gated hall cross devices. The data in Figure 6.3 illustrates the channel normalised current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) as function of V_{DS} for the bare and gated hall cross structures for the a) Al₂O₃ and b) HfO₂ dielectrics respectively. The data were obtained at 10Hz and $S_{I_{CH}}/I_{DS}^2$ were averaged between 5 sets of devices. The corresponding error bars represent the absolute maximum and minimum of the measured LFN noise and the horizontal dashed lines are fitting of the $S_{I_{CH}}/I_{DS}^2 - V_{DS}$ characteristics for each device structure. Insets to both figures illustrate the $S_{I_{CH}}/I_{DS}^2$ behaviour as function of frequency for a pair of similar hall cross devices with gated and un-gated configuration obtained from the same sample die.

Figure 6.3: Channel normalised current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) as a function of drain-source voltage (V_{DS}) measured at 10Hz for the a) Al₂O₃ and b) HfO₂ top-gated graphene field effect transistor (TG-EGFET). The drain-source voltage (V_{DS}) of the TG-EGFET were biased from -1.0V to 1.0V while the gate terminal is left floating. Insets show the LFN spectrum for both bare and gated configuration biased at $V_{DS} = 1.0$V.

As can be observed in Figure 6.3, the average $S_{I_{CH}}/I_{DS}^2$ for the Al₂O₃ gated hall cross devices shows a slight increase in noise magnitude relative the bare graphene devices, while the LFN magnitude on the HfO₂ substrate are comparable for both gated & non-gated structures. Moreover, the $S_{I_{CH}}/I_{DS}^2$ exhibits a weak V_{DS} dependency on all structures investigated, suggesting a resistor like LFN behaviour, similar to the observation described in Section 5.3.3. Under this scenario, the observed conductance fluctuation on the graphene channel is not driven by the applied V_{DS}, instead I_{DS} allows $S_{I_{CH}}$ to be measurable, analogous to the resistance concept in Ohm's law [12]. Furthermore, the LFN spectrum for the hall cross devices with the Al₂O₃ dielectric illustrates a $1/f$ behaviour throughout the entire frequency range (up to 100kHz). A similar noise spectrum is observed on the HfO₂ substrate, except a Lorentzian component with a dependency of $1/f^{1.5}$ is superimposed onto the $1/f$ spectrum at $f <$ 20Hz. While, the $1/f$ observations are found to be consistent among the other examined devices on the Al₂O₃ sample, only a limited number of HfO₂ gated hall crosses exhibit the unique $1/f^{1.5}$ characteristics at the low frequency regime similar to that demonstrated in the inset. Therefore, the $1/f^{1.5}$ trend observed on the HfO₂ gated devices may be induced by the 'slow' carrier generation-recombination process via the defective graphene/oxide interface, corresponding to results in past literature [194].

The LFN results in Figure 6.3 reveal some interesting features of the TG-EGFET fabricated using fluorine functionalisation prior to ALD. Literature in the past have reported that the LFN of oxide incorporated devices in graphene and other semiconductor materials usually suffer from at least 1 order of magnitude degradation in noise performance [102], [195], [196]. In contrast to previous observations, the LFN results of the investigated TG-EGFETs demonstrated only an equivalent ~2.5dB/Hz (quarter of an order) increase in the observed $S_{I_{CH}}/I_{DS}^2$. This suggests that the oxide deposition process forms a graphene/oxide interface with minimal noise generation sites and does not considerably damage the underlying graphene. These oxide properties are highly desirable and promising in fabricating ultra low noise graphene based electronics. In addition, the noise spectrum of the gated structures are generally free from the $1/f^{2-3}$ bulges at the low frequency regime observed in previous reports [194], which implies the gated devices are not affected by the generation-recombination fluctuation due to "slow" traps. It is inconclusive to determine the cause of the $1/f^{1.5}$ noise observations on the HfO₂ samples, however since the phenomenon is solely

observed on the HfO₂ gated devices; this may well be a unique feature of the gating dielectric and may be linked to the peculiar *I-V* characteristics.

6.3.2 Comparison of Al2O3 and HfO2 top-gated epitaxial graphene field effect transistor (TG-EGFET)

I. <u>Electrical Characterisation</u>

The data in Figure 6.4 illustrates the typical *I-V* characteristics of the TG-EGFET on a hall cross structure for the a) Al_2O_3 and b) HfO_2 gated devices. These transistors were measured by sweeping the V_{GS} from -3.0V to 2.0V with 0.5V steps. The bias conditions are limited within this voltage range to minimise the gate leakage current (up to a maximum 10pA at $V_{GS} = -3.0V$), which may damage the dielectric layer and eventually cause oxide breakdown. The corresponding R_{CH} for each gate bias is shown in the inset to the figure. As can be observed from the results, the *I-V* curve for the Al_2O_3 transistor demonstrates a gradual increase in I_{DS} with rising V_{GS}. In addition, the transistor I_{DS} shows only a weak current saturation behaviour under positive V_{GS} and the non-ohmic behaviour becomes significantly more noticeable with decreasing V_{GS}. A similar behaviour is observed for the $I_{DS} - V_{DS}$ dependence of the HfO_2 gated TG-EGFET, except that the *I-V* characteristic exhibits a more noticeable I_{DS} saturation in the measured I_{DS} at a lower V_{DS} and the situation is progressively aggravated with increasing negative V_{GS}.

The *I-V* results for both investigated gate dielectrics illustrate some interesting features that can be uniquely associated with the dielectric. Whilst, the extended ohmic behaviour in the I_{DS} characteristics for the Al_2O_3 gated transistor is ideal for analogue circuit operation, the relatively low channel modulation can be a significant challenge for RF circuit design. In contrast, the HfO_2 dielectric demonstrates a slight improvement in the I_{DS} modulation, where the on/off current ratio ($I_{DS_{on/off}}$) within the investigated V_{GS} is 2.35 in comparison to 1.38 for the Al_2O_3 transistor. Despite such improvement, the HfO_2 transistor suffers from a substantial I_{DS} saturation at a lower V_{DS}. Furthermore, no carrier type transformation was observed within the investigated V_{GS} as shown by the $R_{CH} - V_{GS}$ plot in the insets. Nevertheless, the continuous increment in R_{CH} with decreasing V_{GS} indicates that the Dirac voltage (V_{dirac}) is located at $V_{GS} < -3.0V$ for both dielectrics. The reason for the large V_{dirac} shift on these transistors samples is unknown and requires further investigation.
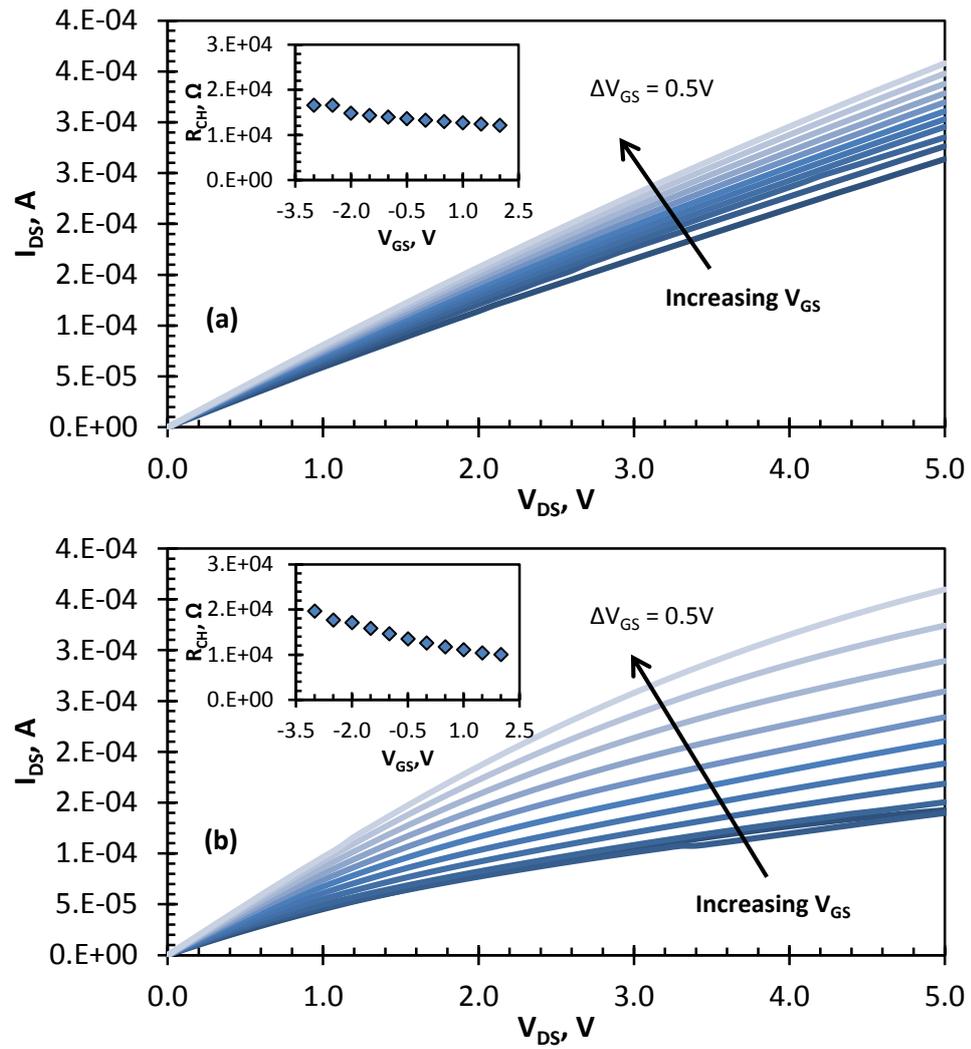
Figure 6.4: *I-V* **characteristics for the a) Al₂O₃ and b) HfO₂ top-gated epitaxial graphene field effect transistor. The transistor gate-source voltage (V_{GS}) is varied from -3.0V to 2.0V with 0.5V increments. The insets show the corresponding total channel resistance (R_{CH}) as a function of V_{GS}.**

II. Low frequency noise characterisation

To investigate the influence of Al_2O_3 and HfO_2 dielectric gating on the transistor LFN performances, $S_{I_{CH}}/I_{DS}^2$ was acquired as function of V_{GS}. The results in Figures 6.5 and 6.6 show the $S_{I_{CH}}/I_{DS}^2$ of Al_2O_3 and HfO_2 gated transistors respectively from devices of identical dimensions measured under the same bias conditions on two separate occasions. The data in both Figures a. and b. illustrate the results of the initial and latter measurement obtained after the transistor is subjected to several non-destructive electrical test routines. LFN measurements were performed by holding V_{DS} at 1.0V in the ohmic regime, while V_{GS} is stepped between -3.0V and 2.0V (red curve) and then from 2.0V to -3.0V (blue curve) with 0.5V interval, which are designated as forward and reverse V_{GS} measurements respectively. The insets to the figures illustrate the $I_{DS} - V_{GS}$ curve for each corresponding LFN measurement. It is worth highlighting that the illustrated I-V and $S_{I_{CH}}/I_{DS}^2$ characteristics are typical of those observed on the EG-GFET in hall cross configuration across the 16mm×16mm samples.

As can be seen from the results in Figure 6.5, the $S_{I_{CH}}/I_{DS}^2$ characteristics of the Al_2O_3 TG-EGFET for both forward and reverse V_{GS} operation exhibits a very weak gate dependence at positive V_{GS} before the $S_{I_{CH}}/I_{DS}^2$ starts to increase gradually with decreasing V_{GS}. On the other hand, the I_{DS} reduces monotonically with rising R_{CH} as V_{GS} is swept negatively towards V_{dirac}. The I-V and LFN characteristics for the forward and reverse V_{GS} measurements demonstrate minimal hysteresis, where the $I_{DS} - V_{GS}$ curve shows a maximum variation of 4.7% in I_{DS}. In addition, the $S_{I_{CH}}/I_{DS}^2$ and $I_{DS} - V_{GS}$ results are consistent between the initial and latter measurement, even though the hysteresis loop on the latter measurement may have noticeably escalated, showing a deviation of up to 10.7% of I_{DS}. The excellent electrical stability of the sample utilising the Al_2O_3 dielectric implies the formation of high quality oxide-graphene interface with minimal extrinsic charge contribution from the foreign absorbates and/or dielectric layer, contrary to the observations in the literatures [197]–[200], where a large hysteresis shift in V_{dirac} were commonly observed on the reported GFETs between forward and reverse V_{GS} sweep and the $I_{DS} - V_{GS}$ characteristics is highly dependent on the V_{GS} sweep rate.
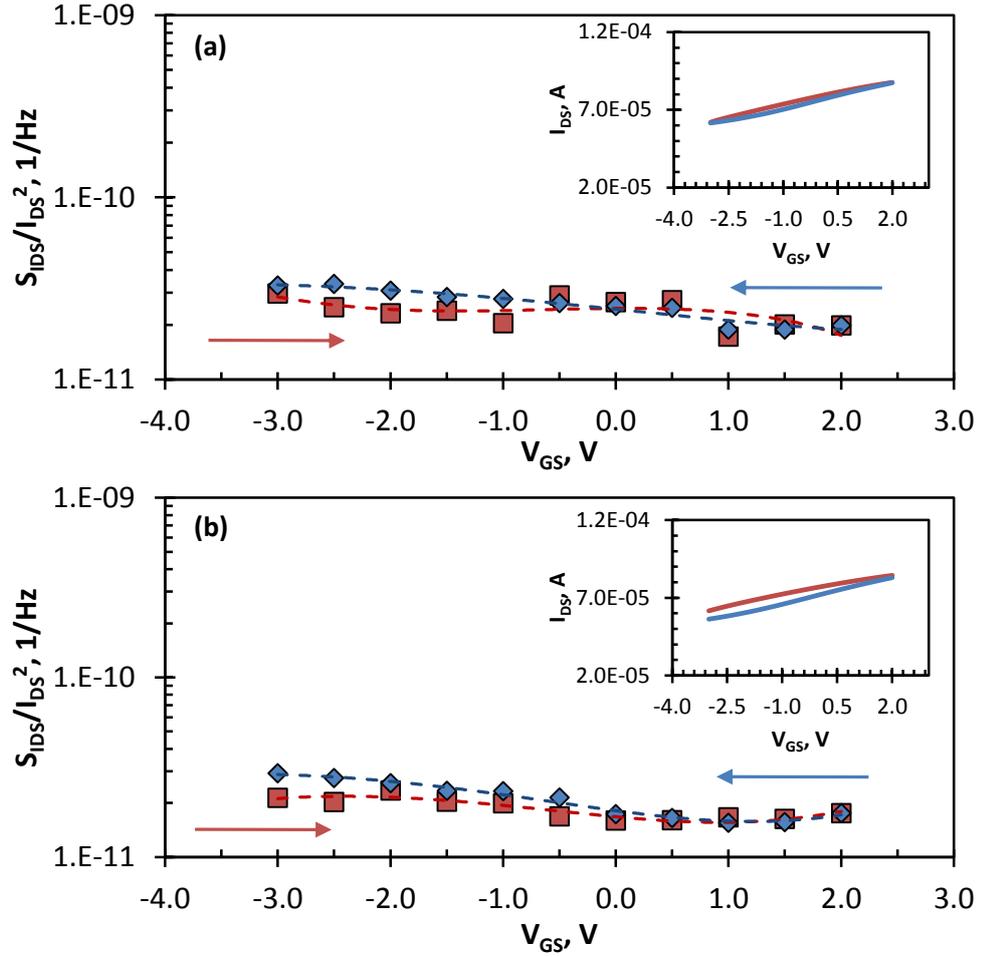
Figure 6.5: Channel normalised current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) as a function of gate-source voltage (V_{GS}) measured at 10Hz on the a) before and b) after repeated electrical measurements on the Al₂O₃ top-gated graphene field effect transistor (TG-EGFET). The drain-source voltage (V_{DS}) of the TG-EGFET was fixed at 1.0V while V_{GS} was biased from -3.0V to 2.0V and back to -3.0V with 0.5V steps. Insets show the $I_{DS} - V_{GS}$ curve for each corresponding measurement.

In contrast, the LFN behaviour of the HfO₂ TG-EGFET as shown in Figure 6.6 is strongly modulated by V_{GS} where the observed $S_{I_{CH}}/I_{DS}^2$ increases significantly with reducing V_{GS}, demonstrating almost an order of magnitude change across the examined V_{GS} range. While the $I_{DS} - V_{GS}$ trend is comparable to that observed in the Al₂O₃ devices, the forward and reverse sweep exhibits up to a 15.1% deviation in I_{DS} compared to the initial test. Moreover, the hysteresis effect dominates the LFN results as shown by the changes in the slope of the $S_{I_{CH}}/I_{DS}^2 - V_{GS}$ data, as well as the alteration in the $S_{I_{CH}}/I_{DS}^2$ characteristics between the forward and reverse V_{GS} sweep from a semi-linear behaviour to showing a strong V_{GS} dependence.
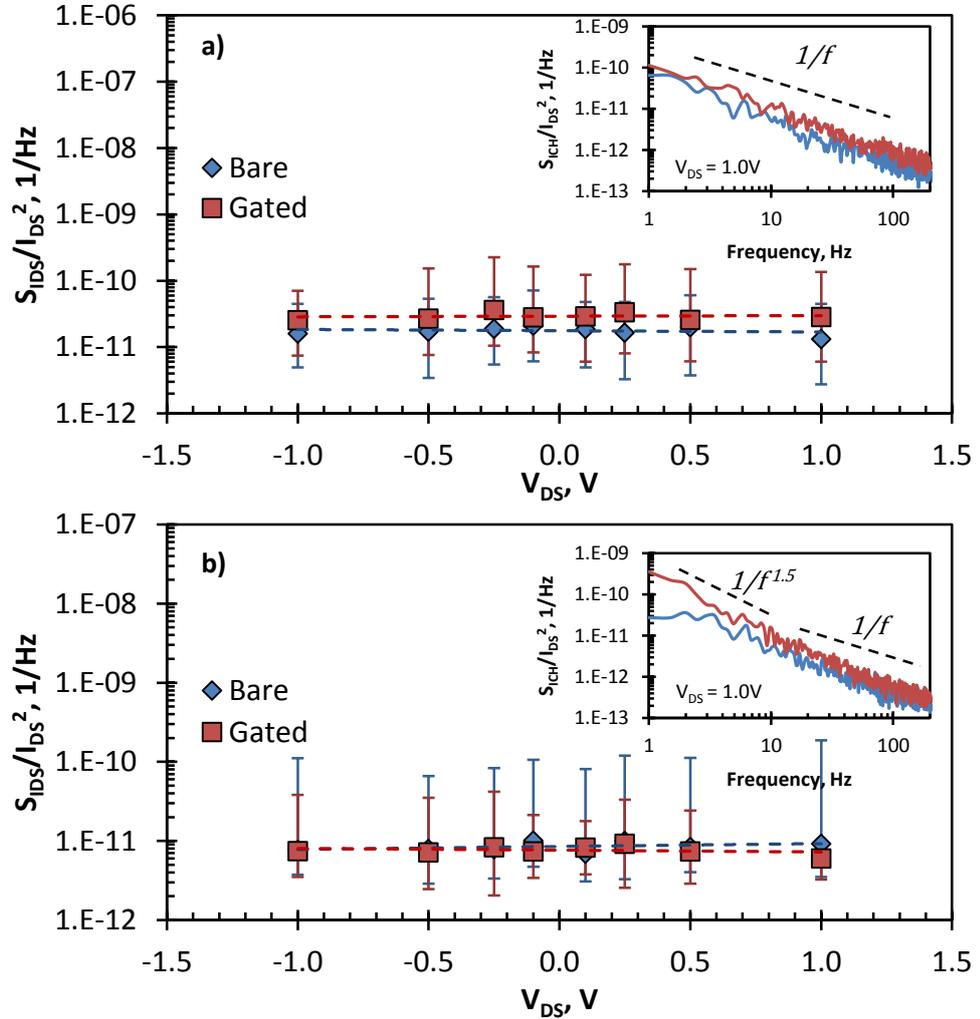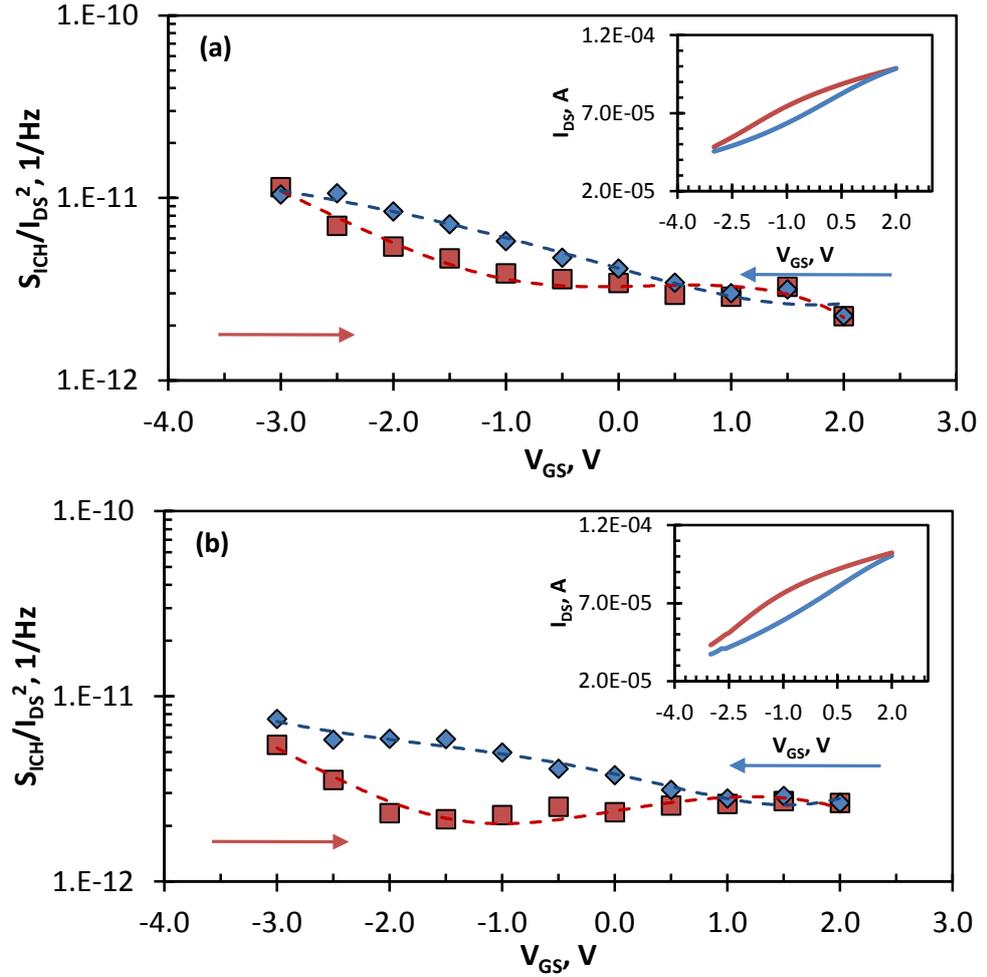
Figure 6.6: Channel normalised current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) as a function of gate-source voltage (V_{GS}) measured at 10Hz on the a) before and b) after repeated electrical measurements on the HfO2 top-gated graphene field effect transistor (TG-EGFET). The drain-source voltage (V_{DS}) of the TG-EGFET was fixed at 1.0V while the V_{GS} were biased from -3.0V to 2.0V and back to -3.0V with 0.5V steps. Insets show the $I_{DS} - V_{GS}$ curve for each corresponding measurement.

Furthermore, the LFN and *I-V* results of the HfO2 TG-EGFET have evolved significantly as a result of being exposed to multiple electrical test routines. As can be seen from the LFN data in Figure 6.6b, the noise transition voltage for the forward V_{GS} (red) has shifted further into the negative regime at $V_{GS} = -2.0$V compared to -0.5V for the initial dataset, demonstrating a weak gate bias dependence on the $S_{I_{CH}}/I_{DS}^2$ behaviour. For the $I_{DS} - V_{GS}$ characteristics, the hysteresis loop between the forward and reverse V_{GS} has increased to a maximum of 23.7%, which is double that of the Al2O3 equivalent. Such an observation is consistent for both investigated dielectrics, which implies an increase of trapped charge in the graphene-oxide interface. Despite the hysteresis effect and modification of the LFN and *I-V* characteristics, the magnitude of the $S_{I_{CH}}/I_{DS}^2$ characteristics for the latter measurement is still within the range of 1×10-

^{12} 1/Hz and 1×10^{-13} 1/Hz. In addition, it is noteworthy to mention that the $S_{I_{CH}}/I_{DS}^2$ behaviour of the reverse V_{GS} characteristics, denoted by the blue lines in Figure 6.6, appear to overlap onto each other, despite the dissimilar forward V_{GS} characteristics. This observation suggests the interface states that govern the $S_{I_{CH}}/I_{DS}^2$ and $I_{DS} - V_{GS}$ hysteresis loops are strong influenced by the application of positive gate biases, possibly due to a trap recharging process [124], [201].

Whilst V_{dirac} is unattainable for the investigated V_{GS} range, the inverse relation of $S_{I_{CH}}/I_{DS}^2$ with I_{DS} in both transistor samples demonstrates a strong resemblance of single layer graphene (SLG) transistors reported previously [202], despite of the SLG (terraces) and BLG (step edges) like network formed on the conducting channel of these investigated samples [74]. Based on the findings in these reports, the LFN behaviour of SLG transistor structures was described to demonstrate a Λ-shape characteristics, where $S_{I_{CH}}/I_{DS}^2$ increases as V_{GS} approaches V_{dirac}, prior to reaching the maximum value at $V_{GS} = V_{dirac}$. This noise characteristic is considered to follow Hooge's relation, where $S_{I_{CH}}/I_{DS}^2 = \alpha_H/N_{CH}f^{\lambda}$. Here α_H is the Hooge's parameter, which is shown to reduce with improved material quality [162], N_{CH} the total number of carriers in the graphene channel and λ the frequency exponent of the noise spectrum commonly reported as ~1.0 [56], [200], [202]–[204].

Since the original Hooge model is conventionally used to describe the conductance fluctuation in bulk semiconductors [24], [162], it does not fully consider the contribution of surface effects in LFN manifestation [138] that is evidently dominating both the transport and LFN behaviour [205]–[210] of graphene transistors. Therefore, despite the apparent similarity between the observed $S_{I_{CH}}/I_{DS}^2 - R_{CH}$ behaviour and that predicted from Hooge's model, the actual physical mechanism that leads the LFN fluctuations in TG-EGFET could be a coincidence and the observed $S_{I_{CH}}/I_{DS}^2$ trend may not necessarily be caused by the proposed lattice scattering process [162]. There are other hypotheses for the observed LFN fluctuation in graphene transistors associated with the unique $S_{I_{CH}}/I_{DS}^2 - V_{GS}$ behaviour, including energy band dispersion [211], long/short range scattering [212] and spatial charge in homogeneity [213]. Our observations strongly imply the correlation of the observed $S_{I_{CH}}/I_{DS}^2$ behaviour with the properties of the graphene-oxide interface, which may result in an inherently different fluctuation mechanism from those reported previously. The measured LFN in these TG-EGFETs can be either caused by mobility scattering

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resulting from the interaction of trapped charge with the graphene channel, or the carrier population fluctuation by generation-recombination mechanism. However since the observed LFN spectrum shows a combination of a pure $1/f$ behaviour and the superposition of $1/f^{1.5}$ components in the low frequency regime, it is inconclusive to determine the dominant conductance fluctuation mechanism over the entire frequency range studied. Nevertheless, the roles of interface traps should not be ignored when considering the formulation of a LFN model to describe the TG-EGFET characteristics or even the conventional back-gated graphene devices based on the unique LFN results among the Al₂O₃ and HfO₂ gated transistors.

The influence of graphene-oxide interface traps is clearly evident in the data taken after a number of measurements, as seen in Figure 6.6b, where the dielectric charge state of the HfO₂ TG-EGFET modified by the previous test routines has caused the shift of V_{dirac}, due to the interaction of the graphene channel and charge in the dielectric [198]. Such phenomena have resulted in the distinctions among the LFN results between the two test routines. In addition, the interfacial traps may have also enhanced the modulation of $S_{I_{CH}}/I_{DS}^2$, where the noise magnitude deviations between the maximum and minimum R_{CH} is considerably larger than those observed in the Al₂O₃ devices and other reported graphene transistors in the literature [194], [196], [202], [214]. In contrast, the weak $S_{I_{CH}}/I_{DS}^2$ dependence on V_{GS} and small hysteresis effect in the Al₂O₃ sample implies that either the deposited oxide layer has minimal dielectric trap concentration or the trapping/de-trapping centres are located deep within the energy level and these are inaccessible under the operating conditions used in this study.

Based on the data shown in Figures 6.5 and 6.6, it is premature to elucidate the dielectric charge characteristics and its influence on the TG-EGFET electrical properties. To further investigate the mechanism of gate hysteresis, the capacitance-voltage (C-V) characteristics were correlated with the LFN data extracted from these transistors.

6.3.3 Hysteresis effect on the Al2O3 and HfO2 top-gated epitaxial graphene field effect transistor (TG-EGFET)

I. Capacitance-voltage measurement

The results in Figure 6.7 illustrate the total gate-source capacitance (C_{GS}) as a function of V_{GS} on the TG-EGFET with a) Al₂O₃ and b) HfO₂ dielectrics. The data were acquired by first stressing the dielectric by holding V_{GS} at -3.5V for an accumulative

hold time (τ_{hold}) up to 400s, followed by C-V measurement at 1MHz from -3.5V to 3.5V for each 100s interval. At the end of the 400s cycle, a post recovery C-V characteristic was obtained after stressing the V_{GS} at 3.5V for 100s. The inset in Figure 6.7a shows a schematic of the equivalent capacitance for the TG-EGFET, where C_{TG}, C_Q and C_{para} are the top-gated oxide, quantum and parasitic capacitance respectively. The equivalent C_{GS} can be computed as $C_{GS}^{-1} = (C_{TG}^{-1} + C_Q^{-1})^{-1}$.

Based on the data in Figure 6.7a, it can be seen that the C_{GS} of the Al₂O₃ gated transistors has a weak V_{GS} dependence throughout the investigated biases. This phenomenon may be caused by two possible scenarios. First, the measured capacitance results could be dominated by C_{TG}, which is independent of the graphene electronic structure, opposing the typical C_Q dominated C-V characteristics, where C_{GS} decays to a minimum value as V_{GS} approaches V_{dirac}. Alternatively, the V_{dirac} of TG-EGFET is beyond the investigated V_{GS} range, leading to a weak C_Q correlation with C_{GS}. Judging from the I-V results of the Al₂O₃ TG-EGFET in Section 6.3.2 I., the former scenario is more likely to be valid as the R_{CH} shows a good degree of V_{GS} modulation, although $I_{DS_{on/off}}$ for Al₂O₃ gated transistors are comparatively small. Nevertheless, despite the prolonged negative V_{GS} stressing, the observed C-V characteristics are maintained throughout the test routine. These observations justify the hypothesis in the previous section that the Al₂O₃ dielectric layer is weakly influenced by the extrinsic charge interaction, leading to the minimal hysteresis on the I-V characteristics and LFN manifestation.

On the other hand, the C-V characteristics of the HfO₂ TG-EGFET is heavily influenced by V_{GS}, which implies the dominance of C_Q on C_{GS}. The results shown in Figure 6.7b indicate that C_{GS} decreases exponentially as V_{GS} is swept further into the negative regime. This situation is exacerbated with increasing τ_{hold} under negative V_{GS}, where the C_{GS} is significantly reduced, probably due to the V_{dirac} shift toward the positive direction along the V_{GS} axis. The displacement of the C-V characteristics is rather substantial for the first 100s interval, showing a maximum shift of 32.3%. However, with increasing τ_{hold} under negative V_{GS} stress, the shift in the characteristics slows down progressively and eventually saturates at $\tau_{hold} > 400s$. In addition, the distorted C-V characteristics of the HfO₂ TG-EGFET can be effectively reverted to its initial behaviour by stressing the V_{GS} at 3.5V for 100s, as illustrated by the red dashed

line in Figure 6.7b. These observations are most likely due to the carrier interaction between graphene film and trapping states within the dielectric; where the negative V_{GS} stress enhances the electron trapping process that leads to the positive V_{dirac} shift, while the situation is reversed as the oxide trap is refilled by stressing the dielectric with positive V_{GS}.
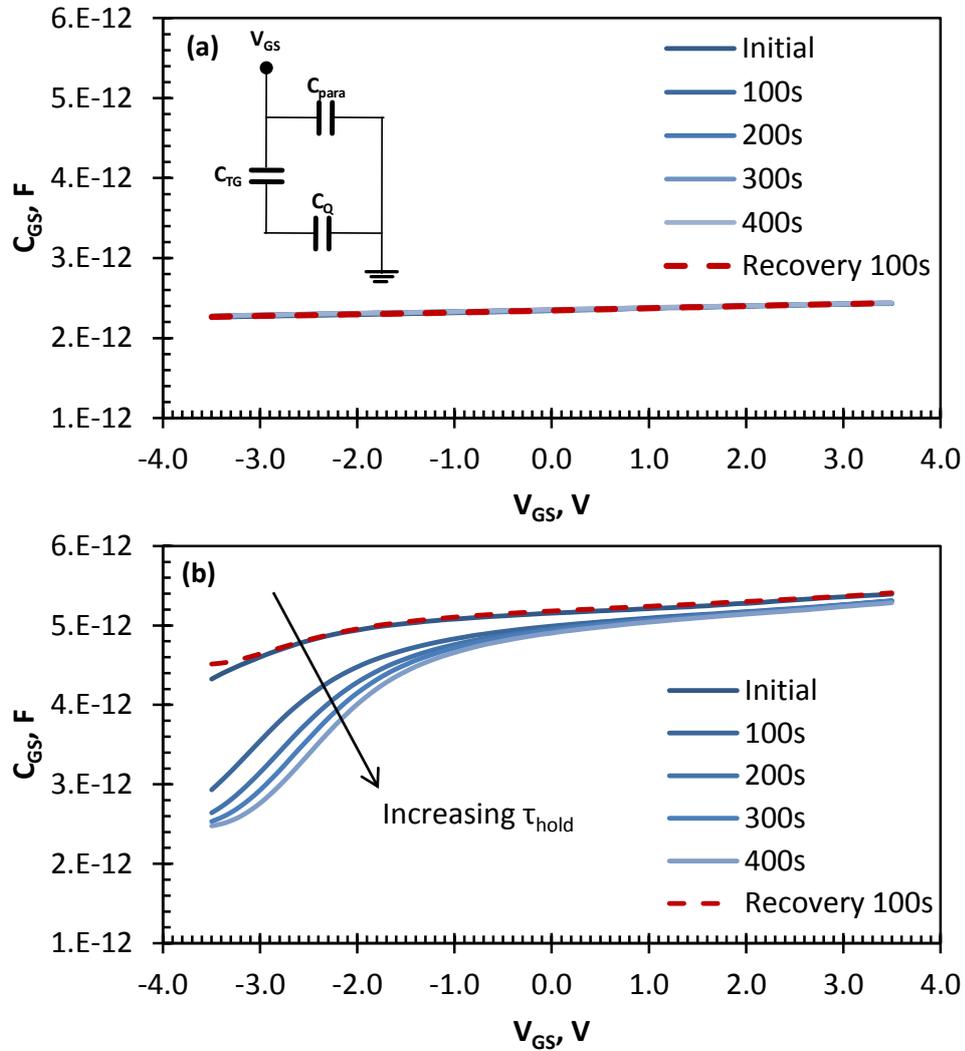
Figure 6.7: Total gate-source capacitance (C_{GS}) measured at 1MHz as a function of gate-source voltage (V_{GS}) for the a) Al₂O₃ and b) HfO₂ top-gated epitaxial graphene field effect transistor (TG-EGFET). The measurement was performed by first stressing the transistor V_{GS} at -3.5V up to 400s of accumulative hold time, while the C_{GS} is measured from V_{GS} = -3.5V to 3.5V on each 100s interval. The post recovery C-V relation by holding the V_{GS} at 3.5V for 100s is also demonstrated in the figures. Inset in a) illustrates the equivalent capacitance model for the TG-EGFET.
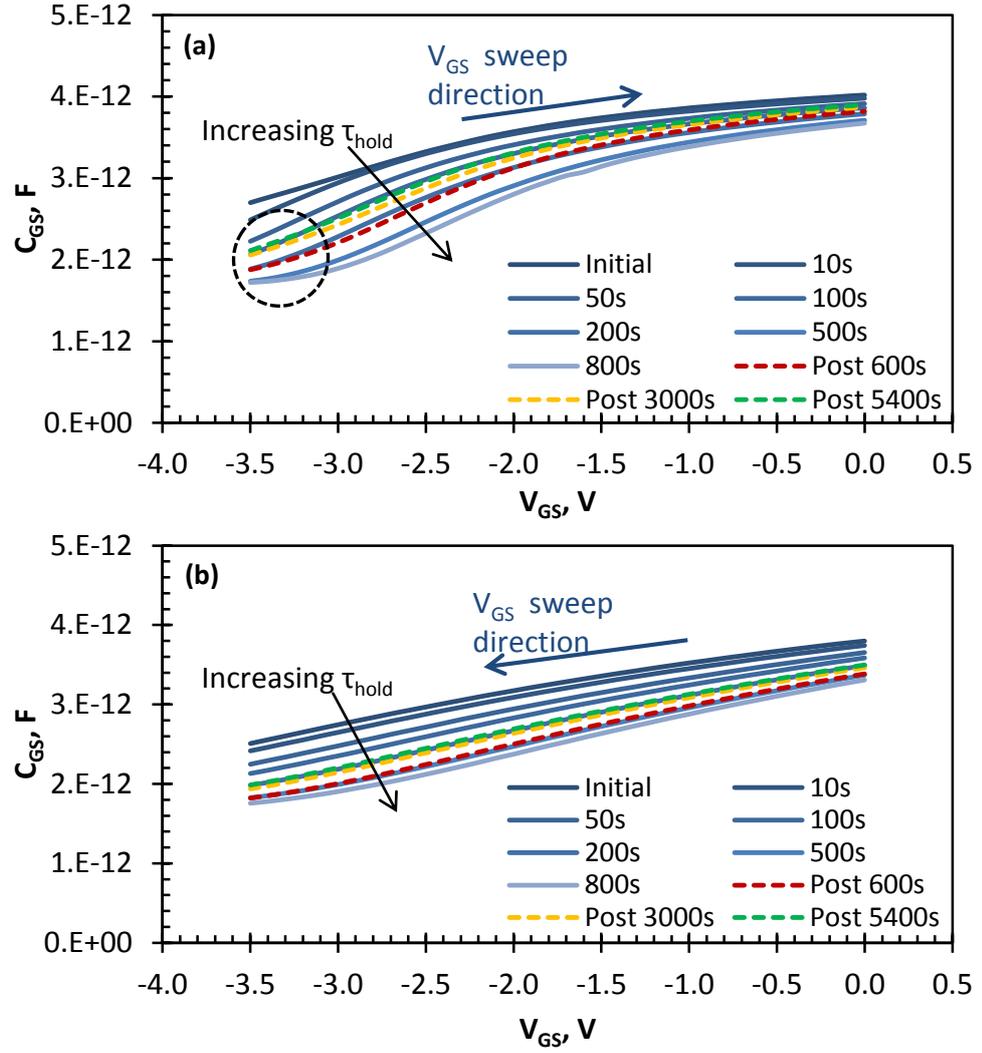
Figure 6.8: Total gate-source capacitance (C_{GS}) measured at 3MHz as a function of a) forward and b) reverse gate-source bias (V_{GS}) for the HfO₂ top-gated epitaxial graphene field effect transistor (TG-EGFET). The measurement was performed by first stressing the transistor V_{GS} at -3.5V up to 800s of accumulative hold time, while the C_{GS} is measured by sweeping the V_{GS} from -3.5V to 3.5V and back to -3.5V continuously on the selected interval. The C-V characteristics were subsequently measured at 600s (red), 3000s (yellow) and 5400s (green) after the transistor is subjected to the V_{GS} stress routine.

To further study the influence of V_{GS} on the graphene-oxide interaction, a similar test routine was performed on the HfO₂ TG-EGFET by sweeping the V_{GS} from -3.5V to 3.5V (forward) and back from 3.5V to -3.5V (reverse) continuously up to 800s of τ_{hold}. To illustrate the drift in the characteristics, the capacitance for values of V_{GS} between -3.5V and 0.0V are shown in Figure 6.8. However, it should be noted that the $C_{GS} - V_{GS}$ behaviour for $V_{GS} > 0.0V$ is identical to those demonstrated in Figure 6.7. In addition, the $C_{GS} - V_{GS}$ relation after the negative V_{GS} stress routine was also acquired to examine

the graphene-oxide behaviour at steady state condition without the influence of positive gate bias stress.

In general, the C_{GS} results for both the forward and reverse V_{GS} sweep direction shown in Figure 6.8 illustrate a negative exponential reduction with rising τ_{hold} similar to the observations in Figure 6.8. Moreover, the shift in the capacitance characteristics with respect to gate-source voltage (dC_{GS}/dV_{GS}) reveals that V_{dirac} is moved positively with increasing τ_{hold}. Contrasting this observation with results reported in the literature [197]–[199], [214], the C-V characteristics for the forward and reverse V_{GS} are extremely asymmetrical, where the dC_{GS}/dV_{GS} of the forward V_{GS} is significantly higher than the value for reverse V_{GS} operation. For the forward V_{GS} characteristics, the typical inverted bell-curve of the C-V behaviour in proximity of V_{dirac} can be clearly observed with increasing τ_{hold} at negative V_{GS}, where the C_{GS} is distorted in the vicinity of V_{dirac}. In contrast, the $C_{GS} - V_{GS}$ relation for the reverse V_{GS} sweep appears to result in a linear reduction in C_{GS} with decreasing V_{GS}. The post $C_{GS} - V_{GS}$ characteristics taken without recovery gate bias, appear to be settling at the stressed C-V behaviour with a minimal level of restoration. The transistor C-V characteristics acquired 5 minutes after the test routine has completed, appears to show an equivalent $C_{GS} - V_{GS}$ behaviour to that obtained after 200s of τ_{hold} stressing. However, the recovery process is saturated after 50 minutes, settling at a comparable C_{GS} trend of 100s and 200s of negative V_{GS} stressing for the forward and reverse V_{GS} operation respectively.

From the data presented in Figures 6.7 and 6.8, a model is proposed to elucidate the influence of V_{GS} on the graphene-oxide interaction. During a prolonged negative V_{GS} stress on the gate dielectric of the TG-EGFET, holes are injected into the dielectric trapping centres, gradually replacing any trapped electrons. The charge screening between the trapped oxide charges and the underlying graphene channel effectively moves the Dirac point causing a temporary p doping of the graphene transistor, which results in the observed positive drift on the transistor V_{dirac}. As the trap populations in the dielectric layer are completely filled, the displacement of the Dirac point is halted, leading to the saturation of V_{dirac} and the C-V behaviour.

In contrast, the positive V_{GS} stress changes the occupancy of the dielectric trap states by repelling the captured holes and the injecting electrons to the trapping centres. This mechanism returns the Dirac point to its initial position, leading to the full

restoration of the initial C-V characteristics. The interaction between the graphene and traps in the dielectric under the influence of V_{GS} can be easily identified by the data in Figures 6.7 and 6.8, where the positive gate stress managed to achieve complete recovery of the C-V characteristics, while the TG-EGFET that does not undergo the recovery stress routine maintains the altered C-V behaviour induced by the dielectric stress at negative V_{GS}. The slight restoration of the $C_{GS} - V_{GS}$ characteristics observed in Figure 6.8 may have resulted from the reverse V_{GS} sweeping during the C-V measurement, as electrons are injected back into a shallower energy levels. A schematic presentation of the hysteresis model is presented in Figure 6.9a.

The asymmetry of the forward and reverse C-V characteristics is influenced by the interaction of the graphene and trapped charge. Under forward gate bias, the charge screening effect on the graphene-oxide interface leads to the creation of an additional parasitic capacitance superimposed onto the C_{GS}, causing to the distinctive curvature of the C-V characteristics near V_{dirac}. As the trapping centres are filled under reverse V_{GS} conditions, the observed characteristic curvature of the $C_{GS} - V_{GS}$ behaviour as highlighted by the green circle in Figure 6.9b diminishes, showing a linear decrement of C_{GS} as V_{GS} approaches V_{dirac}. Similarly, the differences in $dC_{GS}/dV_{GS} - V_{GS}$ behaviour for forward and reverse bias is due to the dominant charge species in the graphene-oxide interface, where the electron recombination rate of the oxide trap is significantly faster than the rate of electron generation. The corresponding relation of C_{GS} and dC_{GS}/dV_{GS} as a function of V_{GS} is illustrated in Figure 6.9b and c respectively. It is noteworthy to mention that the restoration of the $C_{GS} - V_{GS}$ characteristics as shown in Figure 6.7 is achieved under a comparatively shorter gate recovery stress duration in contrast the negative gate stress period, possibly due to the considerably higher gate leakage current at $V_{GS} = 3.5$V in comparison to $V_{GS} = -3.5$V.
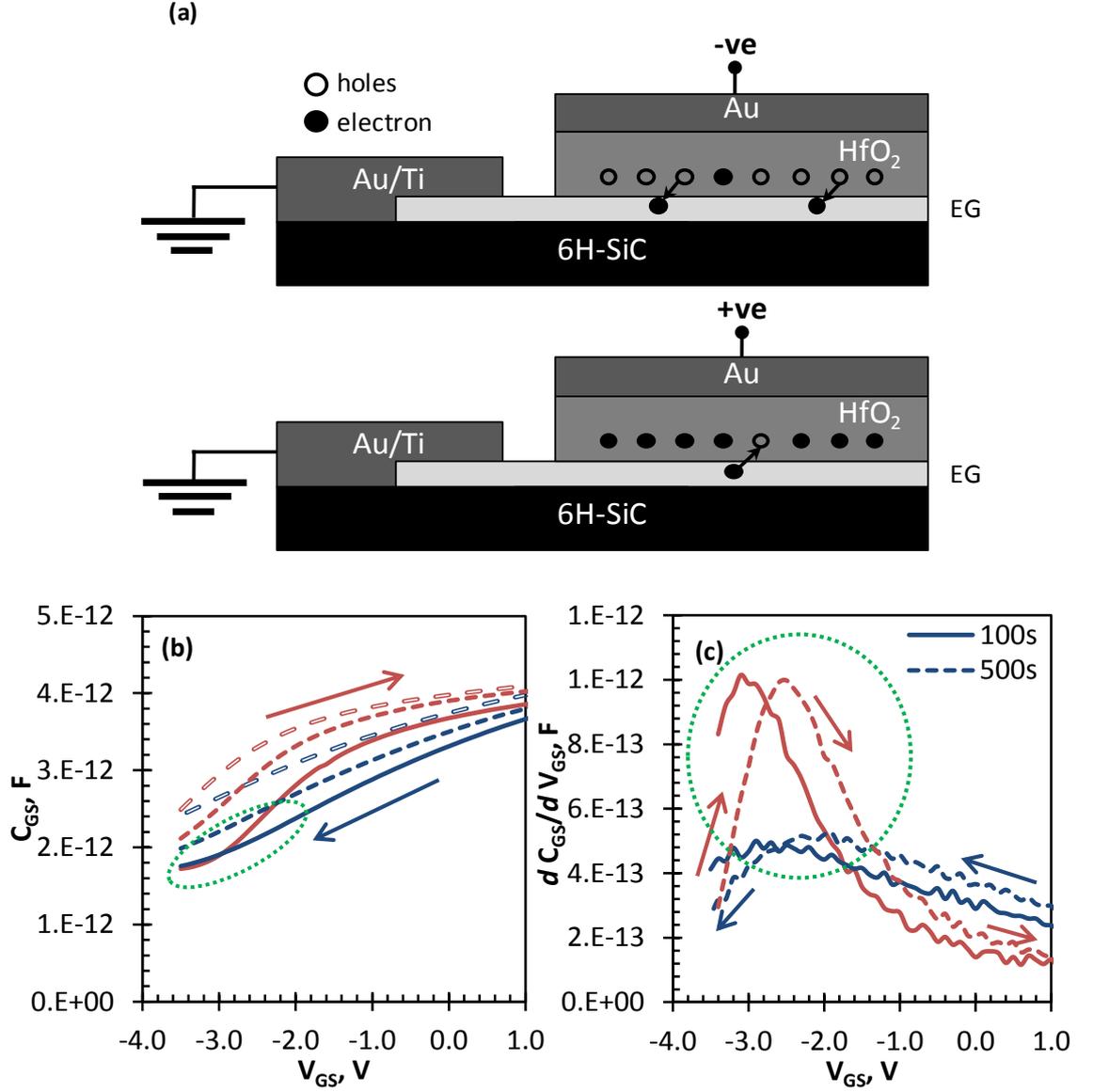
Figure 6.9: a) Hysteresis model for the top-gated epitaxial graphene field effect transistor (TG-EGFET) subjected to positive and negative gate-source voltage (V_{GS}) stress routine. b) Comparison of total gate-source capacitance (C_{GS}) measured at 3MHz as V_{GS}function for the HfO₂ TG-EGFET under forward and reverse V_{GS} operation. The data illustrated are measured after 10s & 800s of accumulative hold time (τ_{hold}) under negative V_{GS} stress alongside with the post 90 minutes recovery results. c) Capacitance rate of change with gate-source voltage (dC_{GS}/dV_{GS}) as a function of V_{GS} of the HfO₂ TG-EGFET subjected to 100s and 500s of τ_{hold} negative V_{GS} stress routine.

II. Low frequency noise correlation with hysteresis model

To examine the effect of gate hysteresis on the transistor low frequency noise, the data in Figure 6.10a to d shows the $S_{I_{CH}}/I_{DS}^2$ plot as a function of R_{CH} from two representative HfO₂ TG-EGFETs measured under identical operating conditions, each on two separate occasions. The LFN results were acquired by varying V_{GS} from -3.0V to 2.0V (red curve) and from 2.0V to -3.0V (blue curve) in 0.5V steps with V_{DS} held at

1.0V. As can be observed from the data shown in Figure 6.10, the LFN results of the transistors during the initial measurement illustrates a monotonic increase in $S_{I_{CH}}/I_{DS}^2$ with R_{CH} in both forward and reverse V_{GS} sweeps. The $S_{I_{CH}}/I_{DS}^2$ characteristics consistently show a R_{CH}^2 dependence with the exception of the forward V_{GS} data for Sample I, where $S_{I_{CH}}/I_{DS}^2$ saturates at $R_{CH} \approx 14k\Omega$, before decreasing with further increases to V_{GS}.
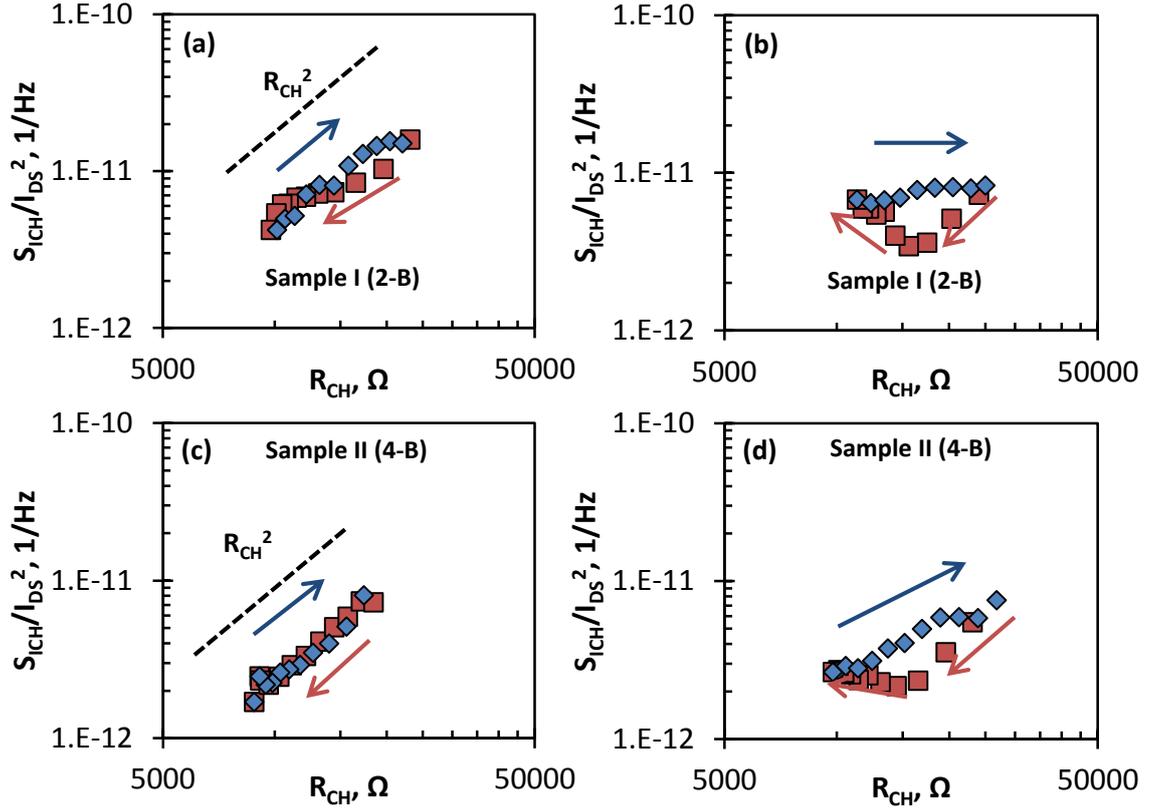
Figure 6.10: Channel normalised current noise power spectral density $(S_{I_{CH}}/I_{DS}^2)$ as a function of total channel resistance (R_{CH}) measured at 10Hz for the HfO₂ top-gated graphene field effect transistor (TG-EGFET). The results in the plots illustrate the initial (a,c) and latter (b,d) measuring attempt after subjected to multiple electrical test routine for two TG-EGFETs with identical devices configuration. The drain-source voltage (V_{DS}) of the transistors was fixed at 1.0V while the gate-source voltage (V_{GS}) was biased from -3.0V to 2.0V (red) and back from 2.0V to -3.0V (blue) continuously with 0.5V steps.

On the other hand, the $S_{I_{CH}}/I_{DS}^2$ behaviour obtained from subsequent measurements on the same transistors has evolved significantly, illustrating a distinctive linear dependence of $S_{I_{CH}}/I_{DS}^2$ on R_{CH} for each TG-EGFET. In the case of Sample I, $S_{I_{CH}}/I_{DS}^2$ decreases gradually with reducing R_{CH} as V_{GS} becomes more positive, before the trend in $S_{I_{CH}}/I_{DS}^2$ is reversed at a device specific bias, showing a systematic increase with reducing R_{CH} before saturating at $V_{GS} > 0.0V$. For reverse V_{GS}, the $S_{I_{CH}}/I_{DS}^2$ shows

a weak R_{CH} dependence, demonstrating a constant noise magnitude for all V_{GS} investigated. A similar $S_{I_{CH}}/I_{DS}^2$ data is observed in the noise characteristics of Sample II, except that the observed $S_{I_{CH}}/I_{DS}^2$ increases with R_{CH} during the reverse V_{GS} sweep.

Following the results shown in Figure 6.10, the LFN behaviour acquired between the initial and subsequent measurements clearly demonstrates a distinctive difference as expected from the observed hysteresis loop in the I-V and C-V characteristics. These results are consistent with those obtained from other HfO₂ TG-EGFET measurements and may signify a strong correlation between charge in the dielectric and on the conductance fluctuation of the carriers in the channel of the TG-EGFET. In contrast, the $S_{I_{CH}}/I_{DS}^2 - R_{CH}$ relations of three identical Al₂O₃ gated transistors were measured on different wafer sites to verify this hypothesis. As can be observed from the results in the Figure 6.11, the $S_{I_{CH}}/I_{DS}^2$ of all the measured Al₂O₃ TG-EGFET exhibit a R_{CH}^2 dependence regardless of the V_{GS} sweep direction or previous biasing conditions. Although these measurements were taken after several electrical test routines, the noise hysteresis loop is virtually non-existent in comparison to the HfO₂ results presented in Figure 6.10. Furthermore, these results are in agreement with the $S_{I_{CH}}/I_{DS}^2 - R_{CH}$ relation of the initial measurement on the HfO₂ TG-EGFET, which implies that this is observation of the intrinsic LFN behaviour of the transistors.
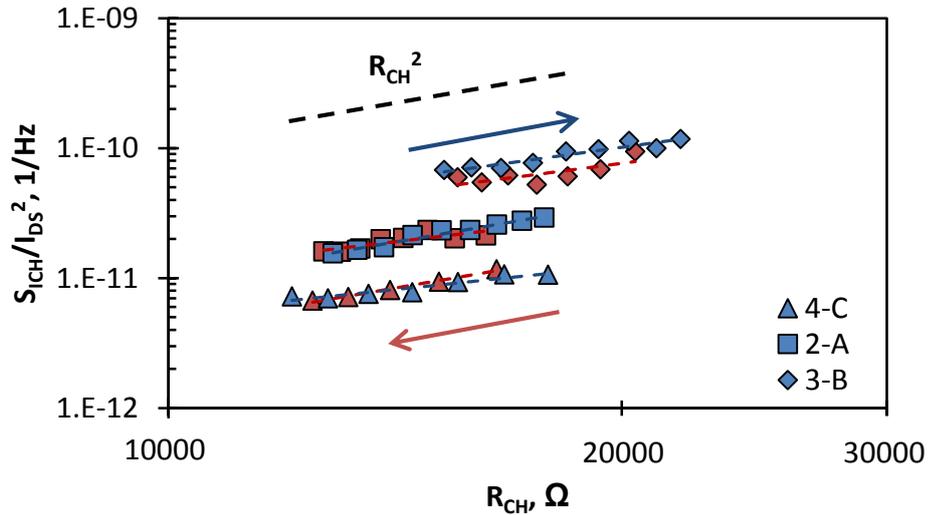
Figure 6.11: Channel normalised current noise power spectral density $(S_{I_{CH}}/I_{DS}^2)$ as a function of total channel resistance (R_{CH}) measured at 10Hz for the three Al₂O₃ top-gated graphene field effect transistors (TG-EGFET) with identical devices configuration. The drain-source voltage (V_{DS}) of the transistors was fixed at 1.0V while the gate-source voltage (V_{GS}) was biased from -3.0V to 2.0V (red) and back from 2.0V to -3.0V (blue) continuously with 0.5V steps.

Based on these phenomena, it can be deduced that the trapped oxide charge dominates the TG-EGFET LFN behaviour notably in the case of HfO$_2$ top-gated transistors. This outcome is thought to be caused by the poor oxide quality of the first few atomic layers of the HfO$_2$ dielectric and so the deposition process requires further optimisation. Apart from modifying the position of the Dirac point, the $C_{GS} - V_{GS}$ and $I_{DS} - V_{GS}$ characteristics, the interaction of the charges with the graphene channel is disruptive to the observed TG-EGFET LFN characteristics. Even though the identification of the actual physical mechanism responsible is not possible, the carrier fluctuation due to hole injection processes under gate-source bias may potentially lead to such observations. Therefore, the distinctive $S_{I_{CH}}/I_{DS}^2$ characteristics observed in Figures 6.6 and 6.10 can be explained by the superposition of the carrier generation-recombination process via graphene-oxide interface traps onto the intrinsic gate modulated conductance fluctuations of these transistors.

6.3.4 The comparison of wafer mapped Hall Effect, sheet resistance and low frequency noise between top-gated epitaxial graphene field effect transistor (TG-EGFET)

In the effort to examine the feasibility of industrial scale electronic device fabrication for ALD TG-EGFET structures, the $S_{I_{CH}}/I_{DS}^2$, Hall Effect mobility (μ_H), sheet carrier density (n_{ch}) and sheet resistance (R_{sh}) were mapped across the 16mm×16mm substrate for both Al$_2$O$_3$ and HfO$_2$ samples utilising the top-gated hall bar structures. (See the schematic in Figure 6.1d) The LFN measurements were performed by floating V_{GS}, while $S_{I_{CH}}$ were acquired and averaged at $V_{DS} = \pm 1.0$V. The μ_H and n_{ch} were averaged between the magnetic field strength of ~500G and ~2000G (individual measurements showing a variation of up to $\pm 5\%$) and the hall bar current was limited to a maximum 5mW of power dissipation. R_{sh} were also obtained under similar current constraints, without the influence of magnetic field. The $S_{I_{CH}}/I_{DS}^2$, μ_H, n_{ch} and R_{sh} data of all the investigated devices were plotted with respect to the die location on the SiC substrate (See inset in Figure 6.1e for the site details) in Figures 6.12 and 6.13 corresponding to the Al$_2$O$_3$ and HfO$_2$ gated samples. Each horizontal dashed line in the figures represents the mean value of measured parameters.
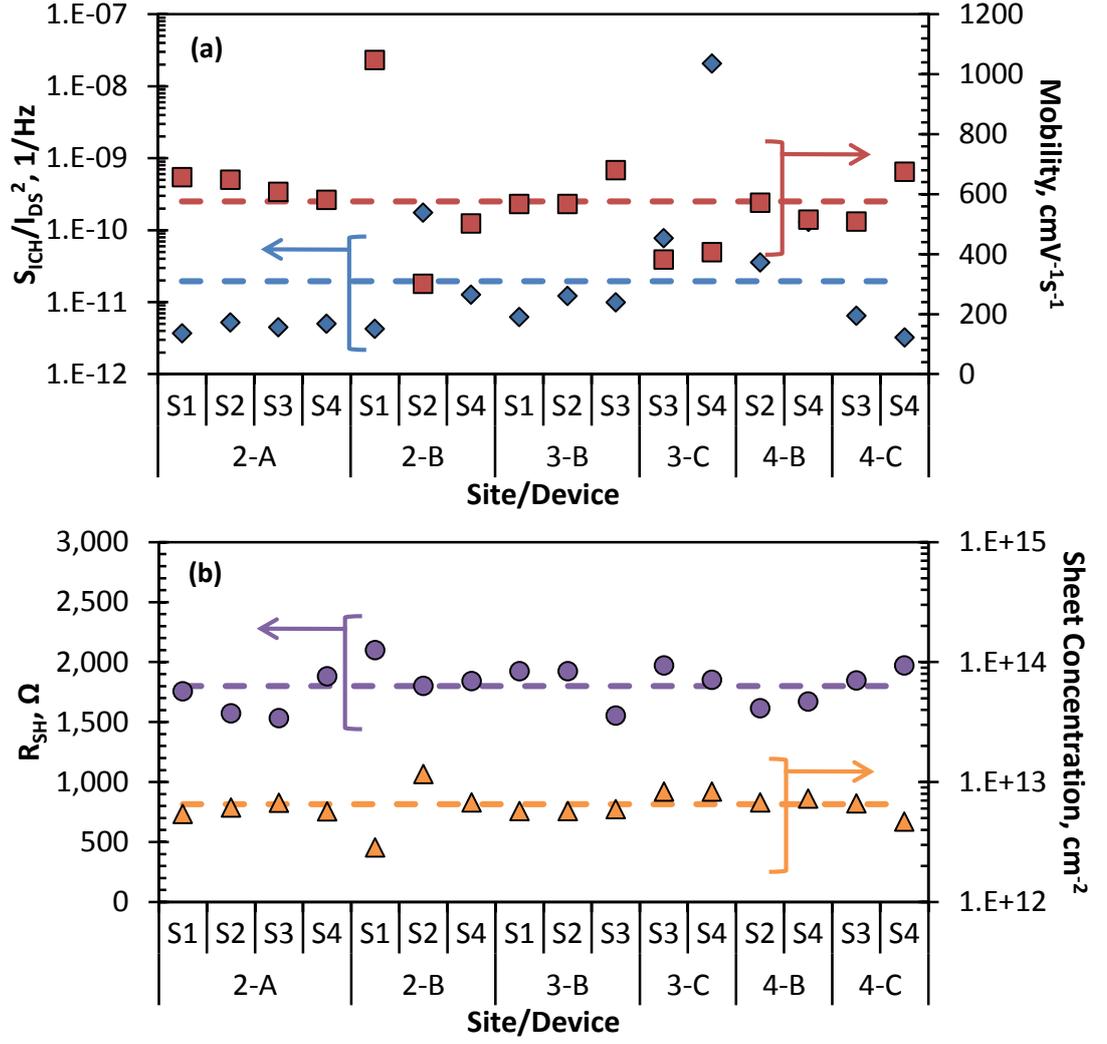
Figure 6.12: Wafer mapping results for the channel normalised current noise power spectral density $(S_{I_{CH}}/I_{DS}^2)$, Hall Effect mobility (μ_H), sheet carrier density (n_{ch}) and sheet resistance (R_{sh}) with respect to the die location on the SiC substrates for the Al₂O₃ gated hall bar configuration.

As can be observed from the data presented in Figure 6.12a, the LFN of the Al₂O₃ gated hall bar is rather consistent across the SiC substrate, demonstrating a mean $S_{I_{CH}}/I_{DS}^2$ of 2.0×10^{-11}Hz^{-1} with a few exceptions where the noise magnitude of a limited number of devices are significantly larger than the typical 10^{-11}Hz^{-1} and 10^{-12}Hz^{-1} range. Furthermore, the average hall mobility is slightly lower than 600cm²V⁻¹s⁻¹ with a maximum and minimum μ_H of 1100cm²V⁻¹s⁻¹ and 300cm²V⁻¹s⁻¹ respectively. The $S_{I_{CH}}/I_{DS}^2$ and μ_H results both illustrate a relative standard deviation (standard deviation divided by the mean of dataset, %RDS) of 9.2% and 28.8%. Similarly, the n_{ch} and R_{sh} results shown in Figure 6.12b are highly consistent for the examined Al₂O₃ gated hall bar structures. Whilst the n_{ch} of this dataset lies within the range of between 10^{12}cm⁻²

and 10^{13}cm^{-2}, the average R_{sh} was 1.8kΩcm^{-2}. The %RDS for the R_{sh} and n_{ch} dataset were computed as 9.4% and 29.0% respectively.

On the other hand, the measured $S_{I_{CH}}/I_{DS}^2$ and Hall Effect results of the HfO$_2$ gated hall bar illustrate a significant scatter across the 16mm×16mm substrate, as shown by the data in Figure 6.13a. In the case of the LFN results, the average noise magnitude is equal to $3.3×10^{-11}$Hz^{-1} and the value of $S_{I_{CH}}/I_{DS}^2$ spans 4 orders of magnitude. The average μ_H of this sample set is slightly higher than its Al$_2$O$_3$ counterpart, showing a mean value of approximately 800cm^{2}V^{-1}s^{-1} however the %RDS of the HfO$_2$ devices is 49.8%. For the R_{sh} and n_{ch} parameters, the results in Figure 6.13b illustrate an average value of 1.6kΩcm^{-2} and $7.6×10^{12}$cm^{-2} respectively. Following the data trend in Figure 6.13b, the measured R_{sh} and n_{ch} for these gated hall bar structures shows a significant variation, demonstrating a fourfold increase in %RDS for the R_{sh} at 39.5% and a 7 fold enhancement of %RDS for the n_{ch} results in comparison to the Al$_2$O$_3$ dataset.

Based on the wafer mapping results for the Al$_2$O$_3$ and HfO$_2$ devices, a number of distinct characteristics can be identified. First, the Hall Effect properties for both investigated samples show a significantly larger variation in the results when compared against either the $S_{I_{CH}}/I_{DS}^2$ or R_{sh} parameters. This observation is likely to arise from the intrinsic surface morphology of the SiC substrate used for the EG growth, where each of the investigated hall bar structures were fabricated on a unique surface profile. Previous reports in the literature have shown that the diversification of the SiC surface properties such the step profile (terrace width, step height, SiC off-cut angle, surface roughness etc.) [91], [205], [207], [215], [216], graphene layer variation [206], step orientation with respect to device channel (channel fabricated in parallel or perpendicular to the terrace) [217], the film contamination due foreign absorbates/contaminants [77], [209], [216], [218] and graphene interfacial properties [182] have a significant effect on the transport properties of the graphene channel. In this scenario, the device channel was constructed on a SiC surface with circular step which results in an active channel that orientated perpendicularly to terrace with high steps count, irregular terrace width, and varying step height; as well as increased non-uniformity of graphene thickness. [91], [207], [217]. Such surface characteristics result in lower Hall mobility, as the carriers have higher tendency to be scattered via the non-homogeneous carbon lattice, consequentially contribute toward the variation in transport properties across the SiC wafer.
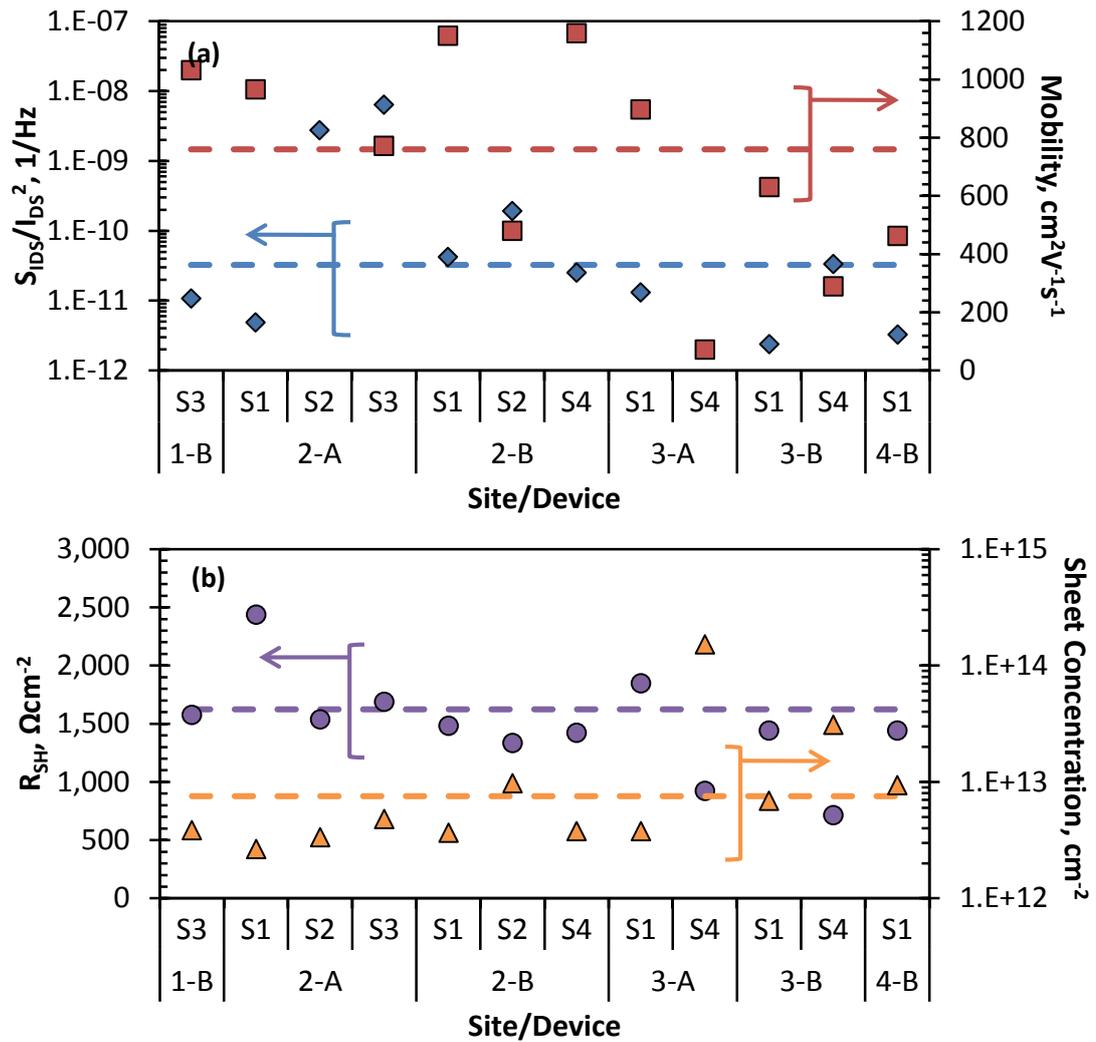
Figure 6.13: Wafer mapping results for the channel normalised current noise power spectral density $(S_{I_{CH}}/I_{DS}^2)$, Hall Effect mobility (μ_H), sheet carrier density (n_{ch}) and sheet resistance (R_{sh}) with respect to the die location on the SiC substrates for the HfO₂ gated hall bar configuration.

Next, by contrasting the mapped results between the Al₂O₃ and HfO₂ gated hall bar devices, the enhanced LFN and Hall Effect variation across the HfO₂ gated sample can be identified. Even though the larger discrepancies in electrical characteristics on these mapped devices can be correlated to the tolerance in graphene growth and device fabrication process, since the two EG samples were grown and fabricated using the same procedure under the same run with an exception for the deposited top gating material; therefore the observed increase of %RDS for the $S_{I_{CH}}/I_{DS}^2$, μ_H, n_{ch} and R_{sh} data on the HfO₂ sample can be deduced as a contribution from the poor graphene-oxide interface, in agreement with the enhanced hysteresis effect, as shown in Figures 6.6 to 6.9. Following the observations in Section 6.3.3, the carrier trapping and de-trapping mechanism between the graphene and the gate dielectric, especially the ability to retain

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the trapping states may be the cause of the significant variation in sheet carrier density, resulting in a comparatively larger $\%RDS$ on the μ_H and R_{sh} properties than those on the Al_2O_3 sample.

Nevertheless, despite the huge variations in the Hall Effect parameters, the low $S_{I_{CH}}/I_{DS}^2$ observed on the Al_2O_3 sample suggests that the fabricated graphene devices have a relatively small density of noise generation sites. Based on the Hooge model, α_H for the Al_2O_3 gated devices is calculated to be $\sim 10^{-3}$, while the HfO_2 gated devices illustrate a typical α_H range from 10^{-3} to 10^0. The lower boundaries of the α_H results was found to be equivalent at $\sim 1 \times 10^{-3}$ for both investigated samples, which may be considered as the intrinsic noise limitation for these circular step samples. By comparing the LFN results from the literature, the calculated α_H for this sample is among the best reported on a production level SLG graphene with excellent reproducibility across a large area [56], [211], [219], [220]. Nevertheless, these results are still 2 orders of magnitude higher when compared to the recorded low α_H at 10^{-5}, which was achieved using exfoliated graphene flakes. Hence, this raises the ultimate question on the lowest intrinsic LFN that can be achieved for wafer scale graphene synthesis.

In the effort to enhance the LFN performance of graphene devices, it is essential to first identify the origin of the noise within the EG. By studying the correlation between the noise behaviour, transport properties and the material characteristics of the graphene sheet, a good indication of the sources responsible in LFN manifestation of the epitaxially grown material can be identified. Such implications are useful to optimise the material synthesis and device fabrication processes, leading to the realization of ultra low noise devices. The LFN scaling of the Al_2O_3 graphene devices was examined in the following section owing to the better consistency in electrical characteristics in comparison to the HfO_2 devices. It is noteworthy to highlight that the outcomes of this inspection can served as an intrinsic LFN characteristics of the TG-EGFET that is free from the influence of poor graphene-oxide interface.

6.3.5 Low frequency noise scaling in top-gated epitaxially grown graphene field effect transistors (TG-EGFET)

Previous literature has unveiled many unique LFN characteristics of graphene based field effect transistors derived from the mechanically exfoliated flakes [194], [196], [202], [204], [214], [221]–[223], chemical vapour deposited [55], [200] and

epitaxially grown films.[56], [224] For example, the discovery of distinctive LFN behaviour of single layer and bi-layer (BLG) graphene transistors under V_{GS} modulation was one of the initial findings this field [202]. The results show that while the SLG can be described using the classical Hooge relation, the LFN behaviour the BLG exhibits a monotonic increase with increasing carrier density. Furthermore, there are several models proposed to describe the observed noise data that is based on the V and M shape like $S_{I_{CH}}/I_{DS}^2$ dependency with respect to gate biases [204], [212], [214]. The demonstration of $S_{I_{CH}}/I_{DS}^2$ scaling with the graphene thickness demystified the century old question on LFN manifestation, which shows that graphene devices with 1-7 atomic layers are dominated by surface effects, whereas devices with >7 graphene layer behave like a bulk semiconductor [223].

Among the LFN literature, there is a lack of a comprehensive study on the LFN scaling on epitaxial graphene sheets. Owing to the fundamental differences in the physical properties of graphene films grown on Si-face of the SiC substrate, such as the active graphene channel being composed of a lumped network of SLG on the SiC terrace coupled with BLG on the intersection between SiC steps and terrace [74] and the unique contribution from the graphene-SiC interfacial layer [90]. The low frequency noise scaling on these EG devices can be inherently dissimilar to those characteristics reported in flakes and CVD graphene. In this section, we focus on the dependence of $S_{I_{CH}}/I_{DS}^2$ under the influence of V_{GS} and the scaling of LFN magnitude with transport characteristics measured under floating gate conditions.

To examine the V_{GS} modulated LFN behaviour of the TG-EGFET, $S_{I_{CH}}/I_{DS}^2$ of the Al$_2$O$_3$ and HfO$_2$ gated transistors with Hall cross configurations are plotted as a function of R_{CH} in Figure 6.14. The dashed lines in the figure are the power fitting of the $S_{I_{CH}}/I_{DS}^2$ for each corresponding transistor. These results were acquired by first stressing the V_{GS} of the devices at 3.5V for 100s prior measuring the $S_{I_{CH}}/I_{DS}^2$ from 2.0V to -3.0V under reverse V_{GS} mode with 0.5V steps to minimise the contribution of graphene-oxide interface charge. As can be observed from the data in the figure, the $S_{I_{CH}}/I_{DS}^2$ of all the TG-EGFETs investigated illustrate a monotonic increase with $R_{CH}{}^{\beta}$, where β varied between 1.7 and 2.0. Furthermore, both the Al$_2$O$_3$ and HfO$_2$ data show a common $S_{I_{CH}}/I_{DS}^2 - R_{CH}$ behaviour, in contrast to the peculiar R_{CH} dependence in Figure 6.10. Such phenomenon indicates that the $S_{I_{CH}}/I_{DS}^2 - R_{CH}$ characteristics

observed in this data are the inherent gate modulated LFN behaviour of the TG-EGFETs, which is free from the influence of the interfacial-trapped charges.

By comparing the results with those in the literature, the $S_{I_{CH}}/I_{DS}^2 - R_{CH}$ characteristics of the TG-EGFETs show some similarities with back-gated single layer graphene flakes [202] and single wall carbon Nano-tube devices [225], notably on the linear escalation of $S_{I_{CH}}/I_{DS}^2$ as a function of R_{CH}. It is uncertain why the R_{CH} dependence deviates between these graphene configurations; nevertheless the observed R_{CH}^2 dependence of the LFN characteristics on these TG-EGFETs demonstrates a close resemblance to the LFN behaviour of SiC junction field effect transistors (JFETs) that is induced by the carrier interaction between the passivation oxide and channel [102]. This electrical noise manifestation can be usually associated with the carrier trapping and de-trapping process, where the generation-recombination (G-R) and the McWhorter models are conventionally used to describe the gate dependency of LFN in both JFETs [19], [132] and metal oxide field effect transistors (MOSFETs) [22] respectively.
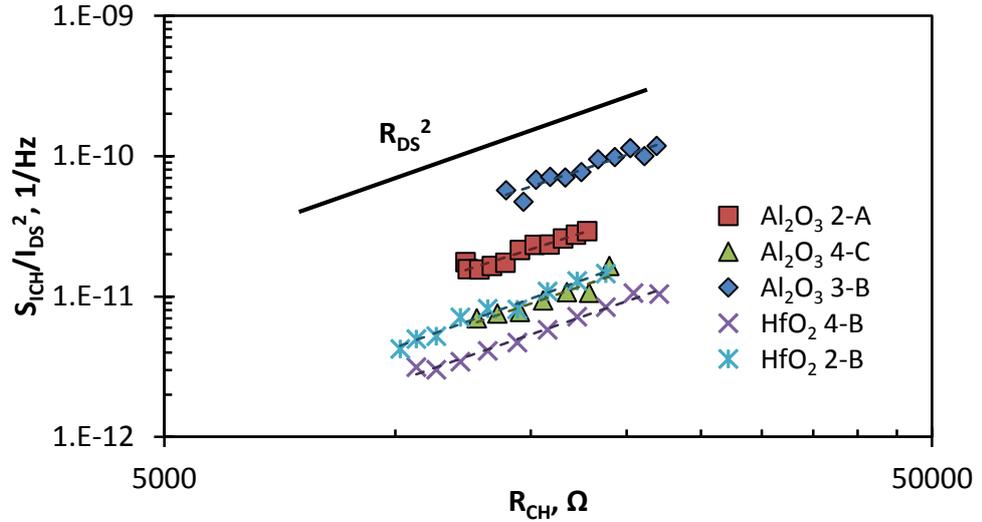
Figure 6.14: Channel normalised current noise power spectral density $(S_{I_{CH}}/I_{DS}^2)$ as a function of total channel resistance (R_{CH}) measured at 10Hz for the all top-gated graphene field effect transistors (TG-EGFET) with hall-cross configuration. The gate-source voltage (V_{GS}) of the transistors was first stressed at 3.5V for 100s, before stepping V_{GS} from 2.0V to -3.0V continuously with 0.5V steps and fixing the drain-source voltage (V_{DS}) at 1.0V.

There is however an incompatibility issue in correlating these models to the TG-EGFET results. While the gate modulated $S_{I_{CH}}/I_{DS}^2$ behaviour of the TG-EGFET may be in close agreement with the noise behaviour predicted by these two models, the fundamental differences in transistor operation between the 2D based TG-EGFET and the bulk semiconductor transistor technology (MOSFET/JFET), render the incorrect modelling/projection of the physical fluctuation mechanism. For example, the observed LFN spectrum of the GFET samples demonstrates a pure $1/f$ noise spectrum instead of the characteristic traits which shows a composition of multiple Lorentzian components for the conventional MOSFET/JFET results. One may argue that this phenomenon is either caused by the superposition of several single G-R sources with evenly distributed carrier lifetime on a logarithmically wide timescale or the G-R mechanism may be indirectly inducing a long-range Coulomb scattering that has a large time constant [203]. Nevertheless, further experiments are imperative to fully understand the roles of graphene-oxide interface and the corresponding trapped charge species that dominate the LFN manifestation in these TG-EGFETs.

In a broad sense, the observed $S_{I_{CH}}/I_{DS}^2$ behaviour may have an altered V_{GS} dependence depending on the different type of carrier interaction with the trapping/scattering centre such as those relating to water vapour [212], gate dielectric [56], surface absorbates/contamination, [203], [210], [226], or the interaction of multiple layers such as that found in bilayer graphene [202]. Whilst, some of these trapping/scattering centres can be minimised or eliminated through an optimised clean room fabrication process, the introduction of channel protective layers, the deposition of high quality gate oxide layer and the careful regulation of grown material thickness on the SiC and CVD graphene is critical. The $S_{I_{CH}}/I_{DS}^2 - V_{GS}$ dependence show less than an order of magnitude difference between the maximum and minimum R_{CH}, in spite of contribution of additional interfacial trapping states. Even though it is unknown if the $S_{I_{CH}}/I_{DS}^2$ magnitude span has a direct proportionality with $I_{DS_{on/off}}$, nevertheless the carrier interaction between the graphene and trapping/scattering centre results in a minor influence on defining the $S_{I_{CH}}/I_{DS}^2$ limitations in graphene based transistors. Instead, the substrate properties and the graphene-SiC interface are likely to be the dominant effect in the LFN performance of EG devices.

The scaling of LFN data for TG-EGFET against the surface properties of the SiC wafer was investigated by correlating the observed $S_{I_{CH}}/I_{DS}^2$ with carrier transport

characteristics. The $S_{I_{CH}}/I_{DS}^2$ of the Al₂O₃ gated hall bar devices are re-plotted as a function of a) n_{ch}, and b) R_{sh} in Figure 6.15 utilising the wafer mapping results in Figure 6.12. As can be observed from the data in Figure 6.15a, the $S_{I_{CH}}/I_{DS}^2$ of the Al₂O₃ gated devices exhibits an exponential increase with n_{ch}, in contrast to the prediction of Hooge's relation, which supposes an inverse relation between $S_{I_{CH}}/I_{DS}^2$ and n_{ch}. Furthermore, the LFN data in Figure 6.15b shows a weak R_{sh} dependence on $S_{I_{CH}}/I_{DS}^2$, opposing the square law behaviour observed in Figure 6.14. These phenomena implicate the existence of more than one fluctuation mechanism that is unique to the device operation of TG-EGFET. Whilst the V_{GS} regulated $S_{I_{CH}}/I_{DS}^2$ can be associated with the G-R process via the graphene-oxide interface, the contrary direct scaling of $S_{I_{CH}}/I_{DS}^2$ with the sheet concentration may be affiliated with the scattering process in EG.

To examine this hypothesis, the $\mu_H - n_{ch}$ relation of the Al₂O₃ gated hall cross transistors is plotted in Figure 6.16a. The data in the figure demonstrate a power law decrease of μ_H with the sheet carrier density, illustrating a $\mu_H \propto n_{ch}^{-1}$ dependence. Furthermore, as the $\mu_H - n_{ch}$ relation is extrapolated toward the intrinsic sheet carrier density (n_i) at $(8.5\pm0.5)\times10^{10}$cm^{-2} in room temperature [191], [227], [228]; μ_H is expected to increase to ~24,000cm²V⁻¹s⁻¹. The intrinsic sheet carrier density can be computed using the notation $n_i = (\pi/6)/(kT/\hbar v_F)$ [228], where k is the Boltzmann constant, T the temperature, $\hbar$ the reduced Planck constant and v_F the Fermi velocity.
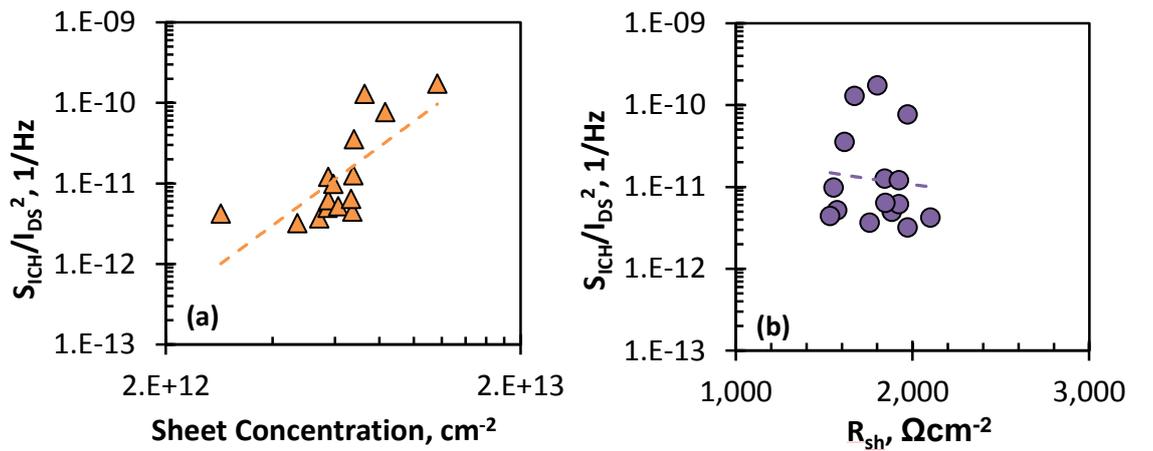
Figure 6.15: Channel normalised current noise power spectral density ($S_{I_{CH}}/I_{DS}^2$) of the Al₂O₃ gated hall-bar devices measured at 10Hz as a function of a) sheet concentration (n_{ch}) and b) sheet resistance (R_{sh}). The noise results were acquired by averaging the $S_{I_{CH}}/I_{DS}^2$ at drain-source voltage (V_{DS}) equals to ±1.0V while floating the gate-source voltage (V_{GS}).
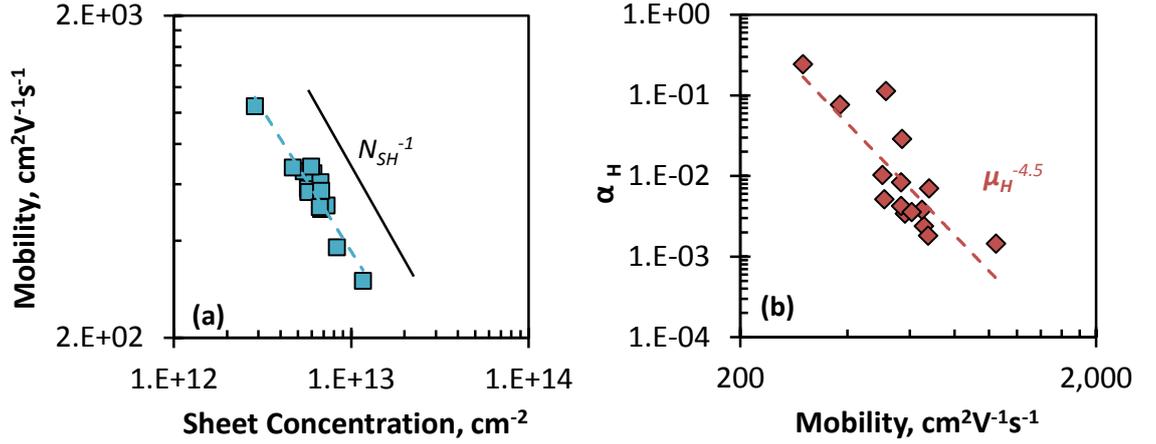
Figure 6.16: a) Hall Effect mobility (μ_H) as a function of sheet carrier density (n_{ch}) b) Extracted Hooge's parameter (α_H) as a function of Hall Effect mobility (μ_H) for the Al₂O₃ gated hall-bar devices.

As expected from the irregular surface morphology as well as the interaction between graphene and SiC interface that give rise to the interfacial and scattering point defects respectively, the predicted μ_H at n_i is 8 times lower based on the reported results from exfoliated [229] and suspended [218], [230] graphene devices, which give μ_H values of ~200,000cm^{2}V^{-1}s^{-1}. Nevertheless, in comparison to the past findings on un-gated Si-face EG devices [191], the predicted μ_H at n_i is at least 4 times higher, whilst preserving the $\mu_H - n_{ch}$ dependence. The increase of μ_H at n_i may be due to the suppression of additional scattering centres introduced on to the graphene channel via atmospheric doping or foreign absorbates contamination resulting from the top-gated structure. Such $\mu_H - n_{ch}$ behaviour is in close agreement with reports in the literature, where the $\mu_H - n_{ch}$ characteristics can be correlated to the short-range and 'ripple' scattering mechanisms [215] due to the unique physical properties EG grown on the Si-face of SiC substrate.

The results in Figure 6.16b show the α_H parameter extracted from empirical formula, as a function of μ_H for the Al₂O₃ gated hall bar devices. As can be observed from the data, the value of α_H shows a monotonic decrease with rising μ_H, where a scaling factor of -4.5 is observed. The inverse function of α_H against μ_H indicates that the scattering processes that limits the channel μ_H is also responsible for the electrical noise manifestation in these EG devices. Since the mobility scattering process is heavily influenced by the physical properties of the graphene and the underlying SiC substrate, instead having a constant α_H value regardless of the device physical conditions, the structural perfection of graphene lattice and the variability of the channel mobility

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scattering process has a strong influence on the α_H magnitude. This observation implies that Hooge's model is not relevant in describing the scaling of LFN with carrier transport properties, which results in the distinctive LFN observations shown by the data in Figure 6.15.

Based on these results, the scaling of intrinsic (none V_{GS} modulated) $S_{I_{CH}}/I_{DS}^2$ is dominated by the carrier scattering process of epitaxial graphene, where the LFN behaviour can be depicted as $S_{I_{CH}}/I_{DS}^2 \propto \mu_H^{\gamma+1}$ or $\alpha_H \propto \mu_H^\gamma$ in Hooge notation. Here γ was found to be approximately -4.5, however γ has been reported to vary between -1 and -3 depending on the device structure and physical layout of the GFET [204]. The actual mobility scattering mechanism may not be determined based on these results, however the $\mu_H \propto n_{ch}^{-1}$ dependency has narrowed down the prospective origin to short-range and/or ripple scattering processes. Assuming the mechanism of LFN fluctuation remains identical up to the intrinsic carrier concentration; the $\alpha_H - \mu_H$ dependence can be extrapolated, demonstrating potentially record breaking low noise behaviour where $\alpha_H \approx 3 \times 10^{-10}$ at room temperature.

Figure 6.17 illustrates the comparison between the area normalised current noise power spectral density $(S_{I_{CH}}WL/I_{DS}^2)$ of the GFETs fabricated on different device geometry and material synthesis process relative to the high electron mobility transistor (HEMT) structures produced from the conventional semiconducting materials. As can be observed from the data in the figure, the $S_{I_{CH}}WL/I_{DS}^2$ of the EG is comparable if not better than those reported for mechanical exfoliated graphene, considering the relatively low mobility value on these samples in contrast to the typical ~3,000cm^{2}V^{-1}s^{-1} for those reported ME sample. Nevertheless, when the graphene data is compared to that from HEMT structures fabricated using bulk semiconductors, the $S_{I_{CH}}WL/I_{DS}^2$ is at least 2 orders lower than that measured on the investigated GFETs. This phenomenon is probably contributed by the inverse proportionally of $S_{I_{CH}}/I_{DS}^2$ against the total carrier population in the case of bulk semiconductor, where the 3D materials have significantly larger channel volume as supposed to a 2D graphene. Furthermore, the advances in bulk crystal growth and device fabrication technique for the HEMT are extremely well-understood, which contributes to the further optimisation of the HEMT LFN performance. Judging from crudeness and relative immaturity of the current graphene growth and device fabrication process, the continuous effort in technology development and process optimisation will propel the noise performance of GFET to be on par with

the current state-of-art device, and will no doubt eventually surpass existing semiconductors as a prospective material for ultra low noise application.
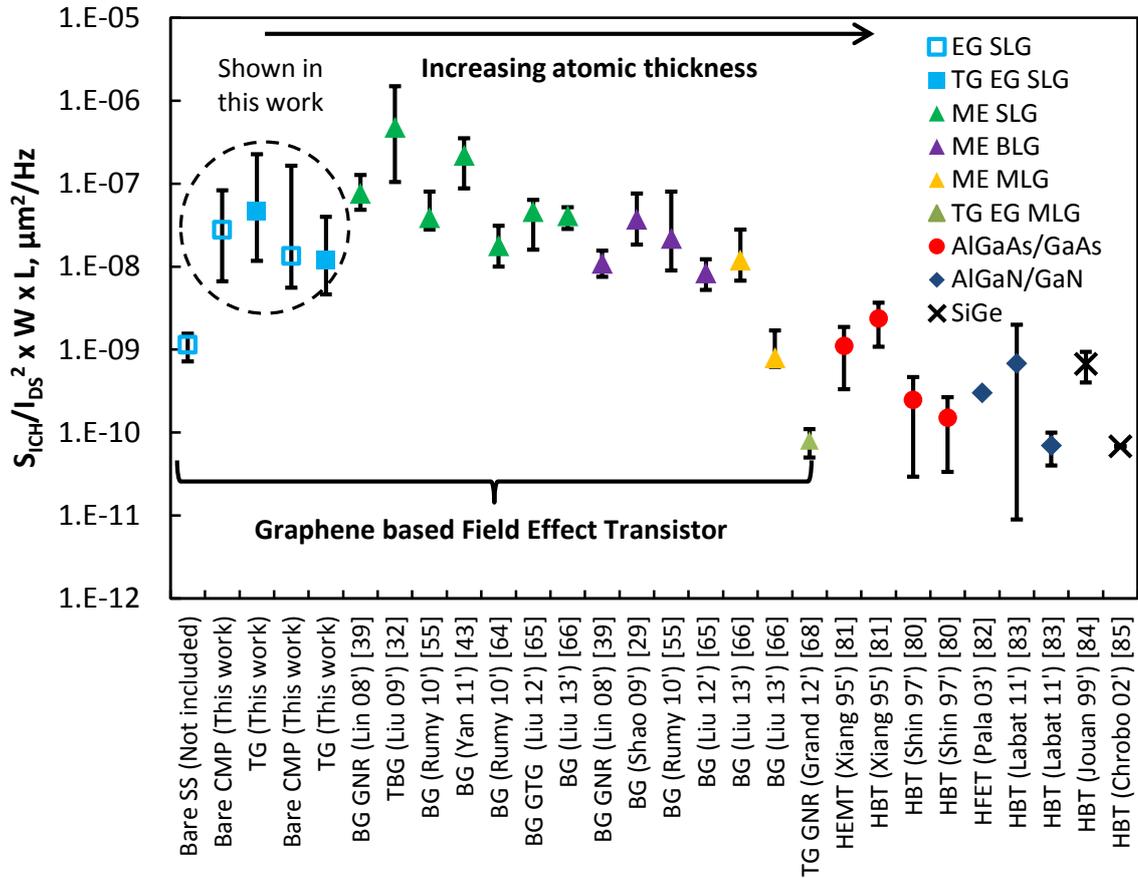
Figure 6.17: Comparison of the area normalised current noise power spectral density $(S_{I_{CH}}WL/I_{DS}^2)$ of epitaxial (EG) and mechanical exfoliated (ME) single with layer (SLG), bilayer (BLG) and multilayer (MLG) graphene transistors with the high electron mobility transistors (HEMT) and heterojunction bipolar transistor (HBT) made from conventional semiconductors. (Note: TG = top-gated)

6.4 Summary

A comprehensive investigation on the electrical and low frequency noise characteristics of the pre-fluorinated atomic layer deposited high-κ top-gating epitaxial grown graphene field effect transistors were performed on wafer scale 16mm×16mm samples. The comparison of the *I-V* results between the 5 different pairs of gated and bare graphene devices with identical device configurations demonstrate a good level of uniformity in both Al$_2$O$_3$ and HfO$_2$ gated transistors. In contrast, the *I-V* data of bare graphene devices acquired from the two substrates were hugely scattered, exhibiting up to 48.9% and 47.2% of relative maximum and minimum deviation respectively as expected from the atmospheric ageing effect. Furthermore, the LFN behaviour of the

gated and bare graphene devices show a close resemblance in the LFN spectrum with a slight elevation in the $S_{I_{CH}}/I_{DS}^2$ magnitude for both gated devices relative to its bare counterparts. These observations implicate the formation of high quality top-gating structure with minimal noise generation sites that has an extended unique feature in preventing the doping of the graphene channel by foreign absorbates.

The device DC operations and LFN characteristics of these TG-EGFETs are further examined by modulating the V_{GS} from -3.0V to 2.0V. The transistors $I_{DS} - V_{DS}$ results illustrate good ohmic behaviour through the investigated V_{DS} for the Al₂O₃ gated devices, while the I_{DS} of HfO₂ TG-EGFET begins to saturate a 1.5V. $I_{DS_{on/off}}$ of these transistors were found as 2.35 and 1.38 for the HfO₂ and Al₂O₃ gated devices correspondingly and no sign of carrier type transformation were observed within the investigated V_{GS} range. Results from the LFN behaviour and gate hysteresis effect under the V_{GS} modulation suggests that the Al₂O₃ gated transistors are weakly influenced by interfacial trap charges as the I-V and $S_{I_{CH}}/I_{DS}^2 - V_{GS}$ illustrate an excellent consistency between run to run measurements; whilst the LFN and DC gate dependency of the HfO₂ gated GFETs were highly deviated between test routines. Furthermore, there is also an obvious V_{dirac} displacement for the Al₂O₃ and HfO₂ between the forward and reverse V_{GS}, which is similar to the findings in past reports as well as an enhanced hysteresis loop among the acquired results from initial and latter test routines.

The observed transistor hysteresis effect were investigated and verified utilising C-V characterisation. To study the interaction between the trapped interface charges and graphene channel, the TG-EGFETs were subjected to different duration of V_{GS} stress time before C_{GS} is measured from $V_{GS} =$ -3.0V to 2.0V and back to -3.0V. This biasing condition is presumably causing the population and de-population of the trapped charges in the graphene/oxide interface. In the case of the HfO₂ devices that illustrate a severe hysteresis loop, the V_{dirac} of the transistor is shifted positively along the V_{GS} axis with increasing V_{GS} stress duration at -3.5V. Whilst the shifted $C_{GS} - V_{GS}$ on the HfO₂ devices can be successfully restored by stressing the gate-source terminal in forward bias at 3.5V for 100s; the altered C-V characteristics fails to revert back to its initial value if the transistor is left in idle (unbiased) states. On the contrary, the $C_{GS} - V_{GS}$ relation of the Al₂O₃ devices remains unchanged throughout the test routine. In addition, the $dC_{GS}/dV_{GS} - V_{GS}$ and asymmetrical C-V behaviour between the forward and reverse V_{GS} operation further reveals the influence of interfacial traps on the TG-

EGFET operation, which significantly altered on the R_{CH} dependency of the $S_{I_{CH}}/I_{DS}^2$ characteristics.

The mapped results of the μ_H, n_{ch}, R_{sh} and $S_{I_{CH}}/I_{DS}^2$ on the Al$_2$O$_3$ TG-EGFETs in hall-bar configuration throughout the 16mm×16mm substrate demonstrate a high consistency among the acquired parameters, in contrast to the massive electrical and noise properties variations on the HfO$_2$ gated sample. This finding is most likely to be arising from defective graphene/oxide interface due to the diverse trapped state induced by the V_{GS} operation, coinciding with the anomalous LFN characteristics and hysteresis effect. By plotting the $S_{I_{CH}}/I_{DS}^2$ results against its electrical noise and Hall Effect properties based the wafer mapped and V_{GS} regulated data unveil two unique LFN scaling of different noise manifestation origin. In the case of the electro-statically modified electrical behaviour, the $S_{I_{CH}}/I_{DS}^2$ data demonstrate a close resemblance to those SLG devices reported on graphene flakes and bulk SiC JFET, where $S_{I_{CH}}/I_{DS}^2 \propto R_{CH}^2$. Despite of the similarity with Hooge's model, the actual V_{GS} modulated noise manifestation can be inherently different due to the distinctive differentiation between 2D and bulk transistor operation. We presumed such LFN manifestation is due to the carrier generation-recombination process via the graphene-oxide interfacial layer. For the intrinsic EG LFN characteristics, the $S_{I_{CH}}/I_{DS}^2$ was found to oppose the infamous Hooge's model, where the LFN behaviour can be described as $S_{I_{CH}}/I_{DS}^2 \propto \mu_H^{\gamma+1}$ or $\alpha_H \propto \mu_H^{\gamma}$, here $\gamma =$-3.5. It is inconclusive to determine the actual LFN manifestation for this setup, nevertheless the correlation of the $S_{I_{CH}}/I_{DS}^2/\alpha_H$ to the Hall Effect mobility suggest that the LFN source may be of short-range and/or ripple scattering origin.

Chapter 7: Concluding remarks and future work

7.1 Summary

This thesis presents electrical noise investigations, in particular the low frequency kind or $1/f$ like noise, of 4H-SiC epitaxial junction field effect transistor (JFET) and top-gated epitaxially grown graphene field effect transistor (TG-EGFET). Due to of the relative immaturity of both SiC and graphene technology in comparison to conventional Si, Ge and III-V compound semiconductors, the material quality and current device production methods may introduce unintentional defects that can interact with the device conduction mechanism, inducing unwanted disturbance in the electrical signal. By utilising the ultra-sensitive and non-destructive low frequency noise measurement as a complementary technique to conventional electrical characterisation methods, the cause of these perturbations can be identified and reduced by the means of optimising the structural design and fabrication/synthesis process. Therefore, the study of low frequency noise properties is critical for the device development cycle to produce an optimal device performance intended for the specific field of application. In addition, the noise performance of discrete devices is extremely important at the system level, which defines constraints in analogue circuit design. The detailed outcomes of the low frequency noise investigation on the SiC JFET and TG-EGFET are summarised as follows.

7.1.1 Low Frequency Noise in 4H-SiC Epitaxial Junction Field Effect Transistor

The SiC epitaxial JFETs studied here are intended as the active switching component for signal conditioning and RF communication circuits in extreme environment. Therefore, it is of the utmost important to study the electrical and low frequency noise characteristics of these SiC JFETs, especially when they are operated under these conditions to identify a practical transistor design. The noise characteristics of 9μm and 21μm gate length JFETs exhibit distinct $1/f$ noise behaviours, which can described by trap assisted generation-recombination processes within the space-charge region and interplay of the noise origin of the active or passive channel resistance.

Due to the nature of the fluctuation mechanism, the 9μm gate length transistors are more sensitive to operating conditions, which resulted in an exponential relation between $S_{I_{CH}}/I_{DS}^2$ and V_{GS}. Similarly, generation-recombination fluctuation attributed to

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the distinct temperature dependence of $S_{I_{CH}}/I_{DS}^2$, where the proximity the temperature dependent E_{FN} to E_T, led to the observation of a unique or multiple $S_{I_{CH}}/I_{DS}^2$ peaks throughout the investigated temperature range. In contrast, the low frequency noise characteristic of the 21μm gate length devices demonstrates a semi-linear function with R_{CH}, in which the constant and linear $S_{I_{CH}}/I_{DS}^2$ behaviour is regulated by the $R_{PASSIVE}$ and R_{DS} components respectively. $S_{I_{CH}}/I_{DS}^2$ shows only a monotonic increase with rising temperature, owing to the observed $R_{CH} \propto T^{1.8-2.0}$ dependence, which relates to the bulk carrier mobility. The low frequency noise behaviours acquired under different V_{GS} conditions and operating temperatures for the 9μm and 21μm gate length JFETs are in accordance to the proposed noise modelling.

Following the results in Chapter 4, it can be observed that 21μm gate length design produces more scalable and predictable DC characteristic, which is fully described by existing models in the literature. Furthermore, the larger gate length/width ratio is also more resistant to process tolerance, where the effect of over/under etching or misalignment (typically 1-2μm) generates a smaller variation in characteristic than observed for the 9μm variant. In terms of low frequency noise performance, the 21μm gate length transistor has a more predictable and superior characteristics in comparison to the 9μm variants. Whilst, the constant $S_{I_{CH}}/I_{DS}^2$ behaviour generated by the passive resistances at high V_{GS} was unintentional, the resulting noise characteristics enable a stable noise performance when the devices are operated in that regime. During high temperature operation, the systematic increases in $S_{I_{CH}}/I_{DS}^2$ with T for the 21μm design is more favourable than the noise maxima observed at random temperature in the 9μm device, so that the as the circuit designer can incorporate necessarily compensation or adjustment at the corresponding operating temperature.

7.1.2 Reliability Evaluation of Thermally Stressed 4H-SiC Lateral Junction Field Effect Transistor

One of the key metrics in hostile environment electronics is the reliability of circuit components under a prolonged deployment in these conditions, where the thermal and radiation fluence can damage active device structure, possibly causing an alteration to the alloy composition of the ohmic contact. Low frequency noise and *I-V* characteristics have been utilised to examine the reliability of 4H-SiC epitaxial JFETs subjected to 2 different temperature stress conditions, 400°C and 500°C for 1000 hours. Following the $1/f$ noise and DC characteristic presented in chapter 5, the origins of the

degradation in the *I-V* and LFN characteristics for both thermally stressed samples were identified. Whilst the thermally evolved alloy composition of the n-type ohmic contact stacks dominates the LFN behaviour of the JFET channel at $V_{DS} \leq 1.25$ V for the stressed samples; only the TS-500 transistors illustrate an enhanced LFN magnitude throughout the range of investigated biases. This leads to the debate whether the observed degradation of the contact metallisation or the non-deliberately generated material defects is responsible for the observed excess noise on these TS-500 transistors.

A comparison was made between the noise and DC behaviours of the on-chip transmission-line-model (TLM) structure, transistor channel as a function of V_{DS}, the P+NN+ junction (including the ideality factor) and $S_{I_{CH}}/I_{DS}^2 - T$ for both stressed with the as-fabricated JFET samples. The degradation in the TS-500 noise performance can be described by as the enhanced the generation-recombination mechanism dominated by additional generated shallow trapping states in the SCR. Although the corresponding trap species are not able to be explicitly identified based on these results, there are strong implications that they are originated from the shallow trapping states such the foreign metal impurities and/or the activation of intrinsic SiC defects within the $E_C - 0.26eV$ regime.

The findings in Chapter 5 provide some critical insights into the possible device failure mechanisms in 4H-SiC epitaxial JFETs stressed at high temperatures. In the case of the contact metallisation, further optimisation work and/or the introduction of protective barriers are required to enhance the integrity of the ohmic contact under high temperature operation. The migration of Ti and Cr into the SiC structure can be prevented through the incorporation of additional diffusive barriers, which may potentially eliminate the origin of the excess noise. Otherwise, the operating temperature of these 4H-SiC JFETs should be limited to a maximum 400°C to extend the device operating lifetime or an alternative JFET structures are required to enable the deployment of these SiC devices in extreme environment.

7.1.3 Low Frequency Noise in Atomic Layer Deposited High-κ Top-Gated Epitaxially Grown Graphene Field Effect Transistors

Epitaxial growth is currently the most feasible technique to enable the wafer production of commercial grade graphene devices. The study of low frequency noise behaviour of the epitaxial graphene helps establish a fundamental understanding of

material properties, which is critical for the realisation of next generation transistors. One of the underlying problems for graphene transistors is the formation of a gating structure with excellent trans-conductance, without overly degrading the superior material transport properties. The investigation of low frequency noise characteristics between bare and high-κ top-gated graphene devices demonstrates that an optimum level of fluorination on the graphene film, not only leads to the formation of conformal and coverage of dielectric layer using the ALD technique, but also preserves the LFN performance, in contrast to the orders of magnitude degradation observed with other techniques. Furthermore, the deposited gate dielectric provides a good protective feature for the graphene channel that is highly susceptible to foreign absorbates, shielding the transistor from post fabrication contamination and atmospheric ageing.

The comparison of the I-V and $1/f$ noise characteristics on the Al_2O_3 and HfO_2 top-gated devices reveals some distinct differences, which are material dependent and correlated to the quality of oxide-graphene interface. Although the extracted $I_{DS_{on/off}}$ of the HfO_2 gated transistors at 2.38 is slightly better than to the Al_2O_3 of 1.38, the device suffer from a prominent hysteresis effect in both I-V and noise characteristics, where the shift in V_{dirac} between each $I_{DS}-V_{GS}$ sweep is contributing to variation of R_{CH} and the drift in $S_{I_{CH}}/I_{DS}^2 - V_{GS}$ behaviour from run to run. In addition, the observed $S_{I_{CH}}/I_{DS}^2$ of the HfO_2 gated transistor exhibits a larger difference in the $S_{I_{CH}}/I_{DS}^2$ behaviour between the on and off state than the Al_2O_3 devices. Further investigation of the hysteresis effect using C-V characterisation under different V_{GS} pre-stressing conditions, shows that V_{dirac} of the HfO_2 transistors can be electrically modulated, implying the presence of dielectric traps. The influence of these trapping centres on the DC and noise characteristics are examined and validated by deliberately populating and depopulating the traps by applying a stressing bias to V_{GS}. A model based on the charge trapping mechanism in these interface states is proposed to describe the observed characteristics and hence the correlation to the I-V and $1/f$ noise characteristics.

The impact of these interface charges can be observed in the variation of the resistivity, low frequency noise and Hall Effect properties across the wafer. For the Al_2O_3 gated sample shows a small hysteresis, the observed transistor properties are highly consistent, demonstrating minimal variation between devices across the 16mm×16mm substrate. In contrast, the transistor properties of HfO_2 device are widely scattered. The presence of these interface states is an underlying fabrication issue that

needs to be addressed to enable wafer scale production of high quality graphene transistors. Another interesting aspect in graphene material is to understand the noise scaling or the fluctuation mechanism, to enable the production of devices with the lowest achievable noise magnitude. By studying the relation of the mapped $S_{I_{CH}}/I_{DS}^2$ with respect to n_i, R_{sh}, and α_H, the $1/f$ noise behaviour of the epitaxial graphene exhibits a strong correlation with μ_H, where $S_{I_{CH}}/I_{DS}^2 \propto 1/\mu_H^{3.5}$. The $\mu_H - n_{ch}$ characteristic of these transistors suggests that the $1/f$ noise manifestation may be related to short-range and 'ripple' scattering process because of the unique surface properties of the SiC substrate used for the growth.

Based on the outcomes of Chapter 6, the fundamentals of low frequency noise in TG-EGFET have been comprehensively investigated. The noise comparison between bare and gate EG devices validates the feasibility of fluorine pre-treated graphene surface in producing high quality oxide layer without deteriorating the graphene transport properties. Although the investigated EG is composed of a single layer on the (terrace/Basal plane) and bilayer (at the steps), the V_{GS} dependency of $S_{I_{CH}}/I_{DS}^2$ demonstrates a Λ behaviour, similar to observations in single layer graphene, which is claimed to follow the Hooge relation. Nevertheless, the observed $S_{I_{CH}}/I_{DS}^2 - V_{GS}$ characteristics on these TG-EGFETs would imply the interaction between trapping states in the gate oxide and carriers in the channel is dominating the V_{GS} modulated noise. The acquired $S_{I_{CH}}/I_{DS}^2 \propto \mu_H^{\gamma+1}$ on samples free from the gate electrostatic influence, where γ is approximately -4.5 and may vary between -1 and -3 opens up the a new prospective on the possible low frequency noise manifestation in EG graphene. These suggest that there are two unique fluctuation mechanisms that governed low frequency noise of EG. Whilst, noise properties of the TG-EGFET under different bias conditions are influenced by the graphene-gate electrostatic interaction, the surface properties of SiC/graphene substrate determine the overall intrinsic noise limit.

7.2 Future outlook

The outcomes in Chapter 4 and 5 demonstrate the presence of different trapping states that is responsible for manifestation of low frequency noise. Although the low frequency noise technique is unable to pin-point the exact trap species, these results provide a complementary outlook to those findings from the deep-level transient spectrometry that can be used to identify the defect location. Furthermore, the thermal stressing process can be repeated on the optimised JFET structure with an additional on

the fly monitoring feature at a fixed time interval to obtain the evolution of the JFETs DC and noise characteristics. It is also beneficial to examine the transistor reliability for an extended thermal aging period beyond the 1000 hours to identify the true device lifetime and other associated failure mechanisms.

In Chapter 6, the low frequency noise investigation in these TG-EGFETs revealed many interesting noise properties that are unique to the epitaxially grown graphene and the subsequent device fabrication processing. The validity of $S_{I_{CH}}/I_{DS}^2 \propto \mu_H^{\gamma+1}$ requires further investigation using the EG with different surface properties such as material grown on different off-cut angle of the SiC wafer, variation of terrace width and step height, steps orientation with respect to the device channel as well as sample with an enhanced Hall Effect mobility.

The other interesting areas that are important to fuel the development of practical graphene applications includes the study of photo resist contamination (shown to affect the channel sheet resistance) on the device noise performance, low frequency noise investigation of the interaction between different foreign absorbates and graphene channel for graphene based sensors, effect of intercalation (demonstrated to significantly improve the channel mobility) on the device noise performance and the fundamental low frequency noise behaviour on the EG grown on the C-face (overall improvement in mobility) of SiC substrate.

In a broader sense, the study of graphene low frequency noise will served as the foundation work for the other uprising 2D based materials such as the chalcogenide family (eg. MOS_2, WS_2), atomic thickness of sliced up conventional material (eg. germanene, silicene) and their hybrid hetero-structures. There are endless of research opportunity using the low frequency noise technique in the field of novel 2D material.

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