Silicon Nanowire: Fabrication, Characterisation and Application

Sami Ramadan

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Abstract

This thesis focuses on the fabrication considerations and the characterisation of silicon nanowires and their integration into chemical sensors. One aim is to optimize a top-down fabrication process for silicon nanowires, in particular the methods that use optical lithography, wet etching and thermal oxidation. The main concerns here are to achieve a reproducible and high yield fabrication process and to obtain a controllable structure. Extensive work was carried out to study the parameters that affect the repeatability of the process. The properties of silicon nitride films, the oxidation method and the characteristics of the anisotropic etchant were found to be key parameters affecting the reproducibility of the process. Several silicon nitride films were deposited under various conditions and their optical properties were tested before and after thermal oxidation. It was found that the oxynitride thickness depends on the refractive index of the nitride film: the lower the refractive index, the thinner the oxynitride. Then an etching process was developed to selectively etch the oxidised silicon nitride over silicon dioxide. The etching process included two steps: firstly ion milling to remove the oxynitride film and secondly using boiling phosphoric acid to strip the silicon nitride film. Nitride-rich silicon nitride films exhibited higher etching selectivity over silicon dioxide compared with silicon-rich silicon nitride. Based on the etch selectivity, oxynitride thickness, and silicon dioxide thickness the maximum thickness of silicon nitride film that can be used to act as a mask during the fabrication of silicon nanowires was determined. The impact of oxidation method on the reliability of the process was studied, and SOI and bulk silicon samples were oxidised at the same temperature and time using lamp-based RTP radiation and also a furnace with resistive heating. The results showed that the SOI sample is colder than the bare silicon sample when both were heated using the lamp-based RTP. This effect was considered during the fabrication of silicon nanowires to obtain a reliable process. Comprehensive experimental measurements were carried out to compare the characteristics of Tetra-Methyl Ammonium Hydroxide (TMAH) and Potassium Hydroxide (KOH) etching to optimise the fabrication process. The use of TMAH was found to lead to a more reliable process.

Another aim of the project was to characterise the fabricated devices, and for this the contact properties and the electrical properties of the silicon nanowires needed to be evaluated. Extensive electrical measurements were carried out to study the thermal stability and ohmic contact formation for the silicon nanowire. Three metallization schemes were studied: Al/Ti, Al/W/Ti and Al/Ti/AlO_x. All these exhibited ohmic contact to the nanowires. However, Al/Ti/Si and Al/W/Ti/Si were found to be unstable after 425 °C RTP annealing. Al/Ti/AlO_x/Si withstood this level of temperature but the contact resistance was about ten times higher than that of Al/W/Ti. The electrical resistivity of the silicon nanowires was then studied; it was found that the measured electrical resistivity decreases with the nanowire thickness. Several models were then developed to explain the apparent increase in resistivity. It was suggested it can be largely attributed to the reduction of the conductive area of the nanowire due to interface traps.

Finally, a silicon nanowire sensor was designed and fabricated, and this sensor was used to detect the changes in pH. The preliminary results showed that the sensor detected the change of pH in the buffer solution. However, reliability and yield were low, which was assumed to be due to the large parasitic current between the source/drain and the buffer solution.

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Abbreviations

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BHF	Buffered Hydrofluoric Acid
BOX	Buried Oxide
HF	Hydrofluoric Acid
IPA	Isopropyl Alcohol
IR	Infrared Radiation
ISFET	Ion Selective Field-Effect Transistor
KOH	Potassium Hydroxide
LPCVD	Low Pressure Chemical Vapour Deposition
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NMP	N-Methylpyrrolidone
PECVD	Plasma Enhanced Chemical Vapour Deposition
PVD	Physical Vapour Deposition
RIE	Reactive Ion Etching
RMS	Root Mean Square
SEM	Scanning Electron Microscope
SOI	Silicon on Insulator
TEM	Transmission Electron Microscope
TLM	Transfer Length Method
TMAH	Tetra-Methyl Ammonium Hydroxide
VLS	Vapour Liquid Solid

Contents

Abstract…… i
Acknowledgements……. iii
Abbreviations……..……...…….…… v
Contents…….…….. vi
Chapter 1 Introduction ……..……...……...… 1
1.1 Background…… 1
1.2 Thesis overview……... 2
Chapter 2 Silicon Nanowire Background ……..……...……. 4
2.1 Fabrication methods…… 4
2.1.1 Bottom-up approaches…… 4
2.1.2 Top-down approaches…… 5
2.2 Physics of semiconductor nanowires…… 10
2.2.1 Quantum confinement…….…… 10
2.2.2 Size effect…… 11
2.2.3 Ionization energy……...…….. 11
2.2.4 Mobility……...…… 12
2.3 Applications of silicon nanowire…….. 13
2.3.1 Nanowire thermoelectrics…… 13
2.3.2 Piezoresistive silicon nanowire…… 13
2.3.3 Silicon nanowire-bio interface……..…… 13
2.3.4 Biosensing application……..……..…… 14
2.4 Summary……16
References……..……... 16
Chapter 3 Fabrication of Silicon Nanowire …….…….....…… 21
3.1 Introduction…….. 20
3.2 Spin-on-doping SOD…… 21
3.2.1 Doping background…… 21
3.2.2 SOD process…… 22
3.2.3 SOD removal…… 22
3.2.4 Doping Profile…… 23
3.3 Fabrication of silicon nanowires…….. 27
3.3.1 Fabrication process steps…….…… 27
3.3.2 Nanowires profiles……...…….…… 29
3.3.2.1 AFM basics…….. 29
3.3.2.2 Modelling the tip effect on nanowire width……. 30
3.3.2.3 AFM images……..…….….. 32
3.3.3 Silicon nitride mask……...……. 33
3.3.4 Size reduction of nanowires…… 34
3.3.4.1 In situ size reduction……..…… 34
3.3.4.2 Size reduction by thermal oxidation…… 36
3.4 Fabrication considerations of silicon nanowires…….. 39

3.4.1 Characterisation of silicon nitride films…….. 39
3.4.1.1 Deposition rate and etch rate…….. 41
3.4.1.2 Optical properties of silicon nitride…… 41
3.4.1.3 Film behaviour during thermal oxidation…… 42
3.4.1.4 Etching of thermally oxidised silicon nitride…… 47
3.4.1.5 Silicon Nitride Selection for nanowire process…….. 50
3.4.2 Characteristics of thermal oxidation…… 52
3.4.2.1 RTP vs Furnace…….. 52
3.4.2.2 The robustness of sidewall oxide…… 56
3.4.3 Characteristics of TMAH and KOH for nanowire fabrication…… 57
3.4.3.1 Etch rate and surface morphology……... 59
3.4.3.2 Silicon dioxide and silicon nitride etch rates…….. 61
3.4.3.3 Undercut rate……... 62
3.4.3.4 Anisotropic etching on fabrication of nanowires…… 62
3.4.3.5 First anisotropic etching step…….. 62
3.4.3.6 2nd anisotropic etching step…… 64
3.5 Null results……..….. 67
3.6 Summary…… 70
3.7 Future work……...…… 71
References…… 73
Chapter 4 Electrical Transport in Silicon Nanowire ..……..... **77**
4.1 Introduction…….……..…… 77
4.2 Electrical contacts……..77
4.2.1 Energy level alignment and band bending……..….. 78
4.2.2 Charge transport mechanism for metal/semiconductor interface……. 79
4.2.3 Ohmic contact……... 80
4.2.4 Choice of material for ohmic contacts…….. 81
4.2.5 Electrical characterisation of contacts……..… 81
4.2.5.1 Experimental results: microwires……... 84
4.2.5.2 Experimental results: nanowires……..…… 89
4.3 Electrical characterisations of silicon nanowire……..….. 92
4.3.1 Effective electrical resistivity of a nanowire…….…..... 92
4.3.2 Nonlinearity behaviour of current-voltage curves in four probe measurements…….. 94
4.4 Summary…… 99
4.5 Future work……..……100
References……..……101
Chapter 5 Analytical Modelling of Resistivity in Triangular Silicon Nanowires …...104
5.1 Introduction……..…… 104
5.2 Effect of dopant distribution…….…...……107
5.3 Surface-depletion due to interface traps…….....** 109
5.3.1 Calculation of the potential inside the neutral region ψ_0…….....…. 114
5.3.2 Calculation of depletion region r_{qdep}……..…….…. 116
5.3.3 Calculation of the potential inside the depletion region ψ_r…… 118
5.3.4 Calculation of effective carrier density n_{eff} and effective resistivity..... 119
5.3.5 Effective resistivity in silicon nanowire: fitting the experimental data….. ……
…. 121

5.4 Effect of surface scattering …… 122
5.5 Effect of surface roughness…… 126
5.6 Summary…… 128
5.7 Future work…… 129
References…… 130
Chapter 6 Silicon Nanowire Field-Effect Transistors in Aqueous Media …… 132
6.1 The ion-sensitive field-effect transistor (ISFET)…… 132
6.2 Sample design and fabrication…… 134
6.3 pH measurements…… 137
6.3.1 Measurement set-up…… 137
6.3.2 Dry test…… 138
6.3.3 pH response…… 139
6.3.4 pH dynamic measurements…… 139
6.4 Null results…… 140
6.4.1 Parasitic leakage current between the source/drain and buffer solution… 140
6.4.2 Voids in the metal electrodes…… 141
6.5 Summary…… 142
6.6 Future work…… 142
References…… 143
Chapter 7 Thesis Review…… 145
7.1 Concerning the optimization of the fabrication process of silicon nanowire…… 145
7.1.1 Reproducibility and yield…… 145
7.1.2 Controllability of the nanowire…… 146
7.2 Characterisation of devices…… 147
7.3 Models of device properties…… 148
7.4 Nanowire integration for chemical sensing…… 148
7.5 Recommendations for future research…… 148
Appendix A …… 150
Appendix B …… 151

List of Tables

Chapter 3 20
Table 3.1: Oxide thickness ratios, regions A, B, C and D. Regions are defined in Figure 3.11(b)..... 37
Table 3.2: Silicon nitride deposition conditions, deposition rates, thicknesses and etch rates in BHF and boiling phosphoric acid (H3PO4)..... 42
Table 3.3: The refractive indexes of silicon nitride films..... 42
Table 3.4: Films compassions and refractive indexes of oxidised silicon nitride as a function of depth..... 45
Table 3.5: The oxynitride and oxide ratios on oxidised silicon nitride to the silicon dioxide thickness on bare silicon..... 47
Table 3.6: Etch rates of silicon nitride films in boiling H3PO4 after the removal of oxynitride layers..... 48
Table 3.7: Etch selectivity of oxidised silicon nitride over silicon dioxide in boiling H3PO4 and oxide thickness ratios consumed during the removal of oxide and oxynitride layers..... 51
Table 3.8: Ellipsometry thicknesses results for SOI and Bulk Si samples..... 54
Table 3.9: AFM thicknesses results for SOI and Bulk Si samples (RTP 1000 °C, 11 min)..... 54
Table 3.10: Average etch rates of <100> silicon, surface roughness of <100> and <111> after TMAH and KOH etching..... 59
Table 3.11: Etch rates of thermal silicon dioxide and silicon nitride in TMAH and KOH..... 61
Table 3.12: Average undercut values..... 62
Table 3.13: Average nanowire width as a function of 1st KOH etching time (2nd KOH adjusted for 4 min at 56 °C)..... 63
Table 3.14: Averages etch rates of <111>..... 65
Appendix A 150
Table A.1: Deposition rate, etch rate and optical property..... 150
Table A.2: Etching of thermally oxidised silicon nitride..... 150
Appendix B 151
Table B.1: Nanowires with Al/Ti and Al/W/Ti contact structures..... 151
Table B.2: Nanowires with Al/AlOx/Ti contact structure..... 153

List of Figures

Chapter 2 ..…….……...……...…..4
Figure 2.1: Vapour-liquid-solid growth mechanism of silicon nanowire: (a) gold nanodroplet on clean surface; (b) eutectic droplet; (c) nucleation; (d) nanowire growth; (e) FESEM image of silicon nanowire grown via a VLS mechanism [5]……..5
Figure 2.2: Schematic of nanoimprint lithography process steps……...…7
Figure 2.3: Schematic diagram of key fabrication steps of sidewall lithography: (a) deposition of sacrificial layer; (b) conformal deposition of low temperature oxide; (c) selective anisotropic dry etching; (d) subsequent selective anisotropic dry etching……8
Figure 2.4: Two examples of crystal orientation dependent etching techniques…..... 10
Figure 2.5: Scale bar of the size of nanowire compared to biological objects……... 14
Figure 2.6: Basic structure of silicon nanowire biosensor: (a) schematic of a p-type silicon nanowire sensor with receptors and a plot of conductance as a function of time; (b) the nanowires response when negative ligands are attached to the receptors and the change in conductance as a function of time……15
Figure 2.7: Silicon nanowire pH sensor: (a) schematic of silicon nanowire surface modified with a 3-aminopropyltriethoxysilane; (b) changes in nanowire conductance as a function of the pH in the solution [58, 59]……15
Chapter 3 ..…….……...……..20
Figure 3.1: Schematic of four probe configuration technique…… 23
Figure 3.2: Average impurity concentrations as a function of RTP pyrometer set point temperature; diffusion time 5 min……. 25
Figure 3.3: Impurity concentrations as a function of depth at pyrometer temperature of 975 °C for 120 sec (blue circle); 300 sec (red triangle); 120 sec calculated (blue line) and 300 sec (red line)…… ….…….. 27
Figure 3.4: Process steps for the fabrication of silicon nanowire: (a) Doped SOI; (b) Oxidation; (c) Oxide opening; (d) Deposition of SiNx ; (e) SiNx pattern; (f) 1st ODE etching; (g) Sidewall oxidation; (h) SiNx removal; (i) 2nd ODE etching step; (j) Sidewall oxide removal; (k) Nanowire isolation; (l) Metal pattern for nanowire characterisation (with 3D schematic); (m) Metal pattern for nanowires FET characterisation (with 3D)…….…..... 29
Figure 3.5: (a) A basic block diagram of an AFM; (b) the forces between the tip and the surface……...…….……... 30
Figure 3.6: The convolution effect on the width of nanowire (a) an AFM tip with a radius larger than the thickness of nanowire (left), AFM trajectory (right);

(b) an AFM tip with a radius smaller than the thickness of nanowire (left), AFM trajectory (right); (c) the critical dimension of nanowire hc= R-Y 31
Figure 3.7: (a) 3D images of silicon nanowires with a trapezoidal cross-section; (b) 3D images of silicon nanowires with a triangular cross-section; (c) SEM image of a Si nanowire with a triangular cross-section [1] ..…… 32
Figure 3.8: The refractive index of oxidised RF sputtered silicon nitride as a function of depth (The process gas is nitrogen and the as-deposited refractive index is 1.9)……..….……..….. 34
Figure 3.9: Schematic of the process steps involved during in situ size reduction of nanowires……. 35
Figure 3.10: The vertical etch rate of vertical <111> as a function of doping level…. 35
Figure 3.11: Size reduction of silicon nanowire by using thermal oxidation (a) experimental results before and after 930 °C in RTP and 20 sec in BHF; (b) simulated structure: (c) after 30 min oxidation; (d) af.ter 60 min ; (e) after 120 min…….…..……..…… 38
Figure 3.12: Schematic diagram of: (a) RF sputter; (b) PECVD; (c) ellipsometry experiment……. 40
Figure 3.13: The etch behaviour of oxidised silicon nitride and silicon dioxide in BHF (N_2, mixed $_{N2}$/Ar and Ar are the process gases)…….….. 48
Figure 3.14: The etch behaviour of oxidised silicon nitride and silicon dioxide after etching in boiling H3PO4 followed 4 sec BHF (N_2 and Ar are the process gases)…… 49
Figure 3.15: The etch behaviour of oxidised silicon nitride and silicon dioxide in ion milling with argon at DC=530 V, P=12 mtorr…….. 49
Figure 3.16: The maximum thickness of silicon nitride mask for different types of silicon nitride films as a function of sidewall oxide……. 51
Figure 3.17: Optical microscopy image shows that an insufficient nitride mask causes a change of etch direction during ODE etching which is seen as curvature and discontinues at the corners……..……..… 52
Figure 3.18: Schematic of (a) RTP configuration; (b) thermal oxidation furnace……..53
Figure 3.19: Schematic of incident and reflected radiations through (a) bulk Si wafer; (b) SOI wafer…….....…….. 55
Figure 3.20: Optical microscopic image shows a cut at the corner of nanowire……....56
Figure 3.21: 3D image of <111> silicon surface after KOH etching (left) and 2D image of the same surface before and after rotation (Rq=3.2 nm)……... 60
Figure 3.22: 3D image of <111> silicon surface after TMAH etching (left) and 2D image of the same surface before and after rotation (Rq= 2.4 nm)……..… 61
Figure 3.23: The fabrication steps that involved in the undercut measurements…….. 62
Figure 3.24: The effect of short etching time on the angle between <100> and <111> planes…… 63
Figure 3.25: Schematic shows the impact of the position of nitride film on lateral oxidation [51]…… 64
Figure 3.26: Silicon nanowires after 5 min (left) and 8 min (right) in 2nd KOH……. 65
Figure 3.27: The minimum thickness of nanowires (Ymin) that can be obtained with KOH; Kt_tot=0.7t_tot, t_c=5 nm calculated for 27 nm nitride thickness..66

Figure 3.28: Different sizes nanowires formation by using in situ size reduction. (Sub 10 nm is obtained)… ……..….. 67
Figure 3.29: Schematic of nanowire profile after 2nd ODE etching; (a) and (b) should have the same height after AFM scan…...…… 68
Figure 3.30: Sheet resistance measurements before (BWC) and after (AWC) pyrometer window cleaning…….....…… 69
Figure 3.31: Run to run variation of oxide thickness using RTP (the trend does not represent the real order).Figure 3.32: 3D schematic of the nanowires after 2nd ODE; oxide remains on the bulk source and drain (useful for selective doping of nanowires)……. 72
Figure 3.32: 3D schematic of the nanowires after 2nd ODE; oxide remains on the bulk source and drain (useful for selective doping of nanowires)…… 72
Figure 3.33: Deposition-Etching technique……..…… 72
Chapter 4 ...…….……...……..77
Figure 4.1: (a) Energy band diagram of a metal and semiconductor before contact; (b) energy band diagram for ohmic contact of metal/n-type semiconductor; (c) energy band diagram for Schottky contact of metal/n-type semiconductor, (w is the depletion region width)…… 78
Figure 4.2: Conduction mechanism at metal-semiconductor contacts (a) thermionic emission; (b) tunnelling; (c) thermionic-tunnelling emission……79
Figure 4.3: (a) Schematic of multiwire test method; (b) plot of total resistance as a function of wire length for multiwire structure; (c) schematic of four probe method……84
Figure 4.4: Current-voltage characteristics of as-deposited silicon microwires with contacts of different metallization structures (l=30 μm, w=2 μm, h=90 nm)……85
Figure 4.5: The effect of various annealing temperatures on the current-voltage characteristics of different contact systems: (a) Al/Ti/Si (Note that the current-voltage after 425℃ is after current is multiplied by 10(orange colour)); (b) Al/W/Ti/Si; (c) Al/Ti/AlOx; (d) the effect of annealing temperature on linearity and performance of Al/Ti /Si (the as-deposited graph is after multiplying the current by 10)… ……..…….....86
Figure 4.6: (a) Current-voltage characteristics of microwire devices with different lengths; (b) total contact resistance as a function of microwire length (Al/Ti/Si contact system, w=2 μm, doping >3.5 X 10^{18} cm-3)….…… 87
Figure 4.7: Specific contact resistivity as a function of annealing after various annealing temperatures…….……..…… 88
Figure 4.8: The total resistance as a function of nanowire length……..……. 90
Figure 4.9: (a) Histogram of measured contact resistance of silicon nanowire using four probe method (b) histogram of measured specific contact resistivity of silicon nanowire using four probe method (Al/Ti/SiNWs, Ac= 360 nm, doping >3.5 X 10^{18} cm-3)……. ……..……..... 91
Figure 4.10: Measured contact resistance as a function of nanowire cross section, inset: histogram of measured contact resistance at A=5200 nm^2…… 91
Figure 4.11: (a) The measured resistivity of silicon nanowires as a function of its thickness (the inset: the function that fits the measured resistivity when the thickness of nanowire is less than 60 nm) (b) Histogram of measured resistivity of silicon nanowire with different thicknesses……..92

Figure 4.12: The effective carrier concentration in silicon nanowire as a function of nanowire thickness (this average calculated data is based on the measured resistivity in Figure 4.11)……...93
Figure 4.13: Nonlinearity examples of four probe current-voltage characteristics in four probe measurements (a) heavily doped nanowire n > 3.5 X 10^{18} cm-3, t= 65 nm (b) moderately doped nanowire 1x 10^{17}cm-3 < n < 1X 10^{18} cm-3, t= 45 nm…….……. 94
Figure 4.14: (a) Four contact current-voltage characteristics of a heavily doped silicon nanowire: (b) power fits to the nonlinear regime in (a), (c) linear fits to the ohmic regime in (a)……95
Figure 4.15: Temperature dependent four probe current-voltage characteristics of a heavily doped nanowire (the inset: power fits to the nonlinear regime at 125℃)……96
Figure 4.16: The four probe current-voltage characteristics of a heavily doped nanowire before and after annealing (b) the power fits to the nonlinear regime of the nanowire after post-metallization annealing (c) the linear fits to the linear regime of the device after post-metallization annealing……97
Figure 4.17: (a) A linear four probe current-voltage characteristics of silicon nanowire after annealing (b) and (c) are the nonlinear and linear regimes of the curve before annealing respectively…… 97
Figure 4.18: The power law fits to the nonlinear regime of the device in Figure 4.13(b) (the inset: the linear fits to the ohmic regime for the same device)…...…98
Figure 4.19: Temperature dependent four probe current-voltage characteristics of a moderately doped nanowire (Vc is the crossover voltage)……99
Chapter 5...……..……...……..104
Figure 5.1: (a) The measured resistivity of silicon nanowire as a function of its thickness (inset: the function that fits the measured resistivity when the thickness of nanowire is less than 60 nm); (b) Histogram of measured resistivity of silicon nanowire with different thicknesses…… 106
Figure 5.2: Modelling results for impurity concentration as a function of silicon depth……108
Figure 5.3: Resistivity as a function of the thickness of silicon nanowire before (WD) and after (ED) eliminating the effect of non-uniformity in impurity concentration (inset: the function that fits the measured resistivity after eliminating the doping effect for thicknesses of nanowire larger than 65 nm)……... 109
Figure 5.4: Charges associated with the silicon-silicon dioxide interface…… 110
Figure 5.5: TCAD simulation of the electrostatic potential and current density distributions inside triangular silicon nanowire: (a) electrostatic potential for fully depleted nanowire with doping 1 X 10^{17} cm-3; (b) electrostatic potential for partially depleted with doping 1 X 10^{18} cm-3; (c) current density for fully depleted nanowire with 1 X 10^{17} cm^{-3}; (d) current density for partially depleted nanowire with 1 X 10^{18} cm-3……112
Figure 5.6: TCAD simulation of the electrostatic potential and current density distribution inside circular and triangular cross sections: (a) electrostatic potential inside circular cross section; (b) electrostatic potential inside triangular cross section; (c) current density inside circular cross section; (d)

current density inside triangular cross section (doping 1 X 1018 cm-3 for all simulated devices)……...…….. ……...113
Figure 5.7: Electrostatic potential in the centre of the nanowire as a function of carrier concentration……116
Figure 5.8: (a) Effect of nanowire thickness on depletion region width, Dit= 5 X 1012 cm-2eV-1, ND= 4 X 10^{18} cm-3 and 5.3 X 1018 cm-3; (b) effect of carrier concentration on depletion region width, Dit= 5 X 10^{12} cm^{-2}eV-1, t= 37 nm, 51 nm and 102 nm; (c) effect of interface trap density on depletion region width, ND= 5.3 X 10^{18} cm-3, t= 37 nm, 51 nm and 102 nm….. 117
Figure 5.9: (a) The effect of carrier concentration on electrostatic potential inside depletion region, Dit= 5 X 10^{12} cm^{-2}eV-1, t= 37 nm, 51 nm and 102 nm, (b) the effect of interface trap density on electrostatic potential inside depletion region, ND= 5.3 X 10^{18} cm-3, t= 37 nm, 51 nm and 102 nm. 118
Figure 5.10: (a) Effective carrier density as a function of carrier concentration, Dit= 5 X 10^{12} cm^{-2}eV-1, t= 37 nm, 51 nm and 102 nm; (b) effective carrier density as a function of interface trap density on the depletion region width, ND= 5.3 X 10^{18} cm-3, t= 37 nm, 51 nm and 102 nm; (c) effective carrier density as a function of nanowire thickness, Dit= 5 X 10^{12} cm-2eV-1, ND= 4 X 10^{18} cm-3 and 5.3 X 10^{18} cm-3……..…….. 120
Figure 5.11: The effective resistivity as a function of nanowire thickness (Dit= 5 X 1012 cm-2eV-1, ND= 4 X 10^{18} cm-3 and 5.3 X 10^{18} cm-3)……. 121
Figure 5.12: Fitting the surface depletion effect to the measured electrical resistivity of silicon nanowire for $D_{it} = 5.9 \text{ X } 10^{12} cm^{-2} eV^{-1}$. ……..… 122
Figure 5.13: Schematic used to calculate the effect of surface scattering on the electrical resistivity in triangular nanowire……..124
Figure 5.14: Calculated relative resistivity of nanowire to bulk resistivity as a function of nanowire thickness with different values of the specularity parameter (mean free path of 15 nm)…… 125
Figure 5.15: The effect of surface roughness on the electrical resistance of nanowire as a function of nanowire width (inset: relative resistance as a function of nanowire thickness)……..127
Figure 5.16: All possible modelled affects the increase of resistivity in the nanowire compared with measured one (measured (red dots); the effect of doping distribution (cyan); the effect of surface depletion for $D_{it} = 5.9 \text{ X } 10^{12} cm^{-2} eV^{-1}, N_D = 4 \text{ X } 10^{18} cm^{-3}$(green); the effect of surface depletion effect for $D_{it} = 5.9 \text{ X } 10^{12} cm^{-2} eV^{-1}, N_D = 5.3 \text{ X } 10^{18} cm^{-3}$(blue); the effect of surface roughness (orange); scattering effect (purple). ……..……127
Chapter 6 ..……..……... 132
Figure 6.1: (a) Schematic diagram of basic structure of ISFET; (b) dielectric/electrolyte interface……..…… 134
Figure 6.2: Mask layout of the nanowires where the expanded views show the distance between the electrodes in the case of a single nanowire (bottom left) and bundles of five nanowires (bottom right)…… …. 135
Figure 6.3: Main process steps for the fabrication of silicon nanowire field effect sensor: (a) Printing the alignment marks; (b) doping the source and drain; (c) fabrication of the silicon nanowire (see Figure 3.4 for full fabrication process of the nanowire); (d) deposition of the aluminium oxide to act as an

active sensing layer; (e) deposition of the source/drain contacts; (f) deposition of the silicon nitride layer to act as a passivation layer. The cross-sections A-A' and B-B' are views of the layout. ……... 136
Figure 6.4: (a) An AFM image of the nanowire used as a sensor; (b) and (c) microscopic images showing the two types of structures of a bundle of five and a single nanowire; (d) and (e) histograms showing uniformity in thickness and width for 23 nanowires…….. 137
Figure 6.5: Back-gate measurements of silicon nanowire field effect transistor: (a) linear scale; (b) logarithmic scale…… 138
Figure 6.6: Transfer characteristics of source-drain current for different pH solution buffers, Vsd=0.4 V: (a) linear scale; (b) logarithmic scale……. 139
Figure 6.7: Transfer characteristics of source-drain current for different pH solution buffers, Vsd=0.7 V and Vfg = 0.3 V……140
Figure 6.8: Transfer characteristics of a nanosensor in the buffer solution and the leakage current between the front gate (Vfg) and the source/drain……. 141
Figure 6.9: (a) Microscopic image of an as-deposited Al/Ti metal; (b) microscopic image of metal electrode after a long period of exposure to air……...142

Chapter 1

Introduction

1.1 Background

In his 1959 lecture,''There is plenty of room at the bottom'', physicist Richard Feynman discussed the possibility of obtaining devices which would be very small in size, and he claimed that "the wires should be 10 or 100 atoms in diameter, and the circuits should be a few thousand angstroms across". More than fifty years after Feynman's prediction, nanotechnology has become one of the most attractive subjects in science, medicine and engineering. Tens of thousands of research papers are published every year investigating novel techniques to make objects a few nanometres in diameter, studying their characteristics, understanding their fundamental properties and pushing them into exciting areas of application.

In this field of research, silicon nanowires are one of the most suitable objects for investigation, for many reasons. Silicon is an abundant element and practical material, and it forms an oxide which is chemically stable at the interface with silicon. Moreover, it is at the heart of CMOS technology. A nanowire can be defined as a nanostructure that has a high length to thickness ratio with a typical diameter of less than one hundred nanometres.

Silicon nanowires can be realized using bottom-up and top-down methods. The bottom-up methods are inspired by the beauty of nature's method in constructing charming objects from the bottom-up. Silicon nanowires formed from the bottom-up have high quality with controlled diameter. These methods are both simple and cheap. However, there is still a major challenge in controlling the doping level and growth positions of these nanowires, and these main drawbacks considerably limit the use of bottom-up methods. For decades top-down methods have dominated the area of IC manufacturing. Their application is still superior for achieving nanometre scale array structures with high control of doping, position and feature sizes. However, further scaling using top-down methods requires complex and often expensive equipment. Over the last decade, new fabrication techniques have been introduced to fabricate nanostructures using top-down methods without the need

for high lithography techniques. However, it has become clear that achieving reliability and reproducibility with many of these new methods is problematic.

Accessing the nanoscale regime is associated with the appearance of new fundamental properties. Electrical, optical, electronic and mechanical properties become size-dependent. The nature of the surface plays an important role in a material's properties. Surface states, the nanowire's surroundings and scattering all have a large influence on the properties of nanowires. Understanding these effects is essential in order to integrate nanowires into device applications.

Silicon nanowires can have a significant impact in various fields of application, including electronics, biology, energy devices and sensing. Among the above-mentioned applications, silicon nanowire-based sensors offer low-cost, label free and real time sensing applications.

1.2 Thesis overview

This thesis investigates the fabrication of silicon nanowire-based devices for electronics and sensing applications. This thesis addresses the challenges in fabricating silicon nanowires using indirect top-down methods, and in particular the methods that use optical lithography, wet etching and thermal oxidation. The issues involved in each fabrication step that affects the reproducibility of the process are addressed, and attempts are made to find solutions so as to obtain a reliable fabrication process. The thesis also addresses the issues related to the contacts for nanowires and characterises several important properties of nanowires such as resistance, resistivity and doping. This study attempts to offer insights into the effect of scaling on the electrical properties of nanowires, and also attempts to integrate silicon nanowires into functional devices for a chemical sensor.

There are four main objectives of this thesis:

- Optimization of the fabrication process of silicon nanowires using an indirect top-down method based on optical lithography, anisotropic wet etching and thermal oxidation, along with investigations of the key factors to obtain a reproducible process with high yields and a controllable structure.
- Characterisation of the fabricated devices and an investigation of the key issues that affect their performance.
- Development of models and simulation to understand the properties of fabricated nanowires in mesoscopic systems.
- Design, fabrication, and characterisation of a silicon nanowire-based chemical sensor.

This thesis is organised as follows:

Chapter two provides the background and a review of silicon nanowire fabrication by top-down and bottom-up methods. The effect of size and surface to volume ratio on the electrical and electronic properties of a silicon nanowire is discussed. Some applications of silicon nanowires in thermoelectrics, mechanical and biological applications are presented, with a special focus on the principles and applications of silicon nanowire biosensor.

Chapter three considers the fabrication of silicon nanowire field effect transistors, and reports on the optimization of the fabrication process of silicon nanowires using optical lithography, anisotropic wet etching and thermal oxidation, and investigates the key factors that affect the reproducibility and reliability of the process, such as properties of the silicon nitride film during thermal oxidation, the behaviour of Si and SOI substrates during oxidation using radiant and resistive heating sources, the robustness of a sidewall mask, and the etching characteristics of Trimethyl Ammonium Hydroxide (TMAH) and Potasium Hydroxide (KOH).

Chapter four concerns electrical transport in silicon nanowires, and discusses the issues related to contacts for nanowires in addition to the electrical properties of the nanowire itself. The electrical properties of three metallisation schemes are investigated, which are Al/Ti/Si, Al/W/Ti/Si and Al/Ti/AlO_x/Si, and their stability at different elevated temperatures is determined. The key properties of electrical transport in silicon nanowires such as electrical resistivity, electrical resistance and impurity concentration, are also investigated.

Chapter five presents the analytical modelling of resistivity in triangular silicon nanowires. Several models are developed to explain the apparent increase in measured electrical resistivity with decreasing thickness of the silicon nanowire. The features described in this chapter include doping distribution, surface depletion, surface scattering due to boundary conditions, and sidewall surface roughness. The 3D Sentaurus Device simulator is used to support the analytical modelling of the effects of surface depletion effects on the electrical characteristics of a triangular silicon nanowire.

Chapter six considers silicon nanowires in aqueous media, and the theoretical background of the ionic-sensitive field-effect transistor (ISFET) and its pH sensitivity is discussed in this chapter. Experimental data for silicon nanowires in aqueous media are presented concerning the sensitivity of the nanowire to changes in pH value.

Chapter seven provides the general conclusions for the major work presented in this thesis. It also recommends further directions for research into the fabrication of nanowires, especially in the fields of selective ionic sensing, drug delivery, biosensing and thermoelectrics.

Chapter 2

Silicon Nanowire Background

In this chapter, the most successful techniques developed to fabricate silicon nanowires are reviewed. Some of the fundamental electrical and electronic properties of silicon nanowires are also introduced. Finally, a review of the major applications of silicon nanowires is presented, including thermoelectrics, mechanical and biological applications.

2.1 Fabrication methods

Two main approaches have been developed to fabricate nanostructures. These are the top-down, and the bottom-up methods. Bottom-up approaches involve assembly processes where small functional units are joined to form more complex structures. The top-down approaches start with a complex structure and reduce its size to a very fine structure and mostly use the same techniques as used in CMOS processing.

2.1.1 Bottom-up approach

Vapour-liquid-solid (VLS)

The vapour-liquid-solid process can be used to grow silicon nanowires [1-4]. In this method, a catalyst of nanoparticles of a transition metal, usually gold, is deposited on a clean and defect free substrate which can be silicon or glass (Figure 2.1(a)). Then the nanoparticle catalyst is heated to a temperature higher than the eutectic temperature for the chosen metal-semiconductor, which is Au-Si in this case, in the presence of a vapour phase source of semiconductor. The vapour can be generated through chemical vapour deposition (CVD) [3, 5], the laser ablation technique [6] or by molecular-beam-epitaxy (MBE) [7, 8]. This results in the formation of a droplet of metal-semiconductor, Au-Si, on the substrate surface (Figure 2.1(b)). The mixture will have a melting point much lower than that of the components, 360 °C in the case of Au-Si. Through the continuous introduction of gas precursor, the eutectic droplet absorbs more silicon until the eutectic supersaturates, and

the semiconductor starts to nucleate due to the precipitation of Si out of the supersaturated droplet (Figure 2.1(c)). Continually, the nanowire is formed (Figure 2.1(d)). For SINWs, Silane SiH_4 is used as a reactant source, and diborane (B_2H_6) and phosphine (PH_3) respectively are the *p*-type and *n*-type dopants.

Nanowires grown using the vapour-liquid-solid (VLS) technique can have a diameter of 15 nm with tens of micrometres in length. Vapour-liquid-solid (VLS) method is cheap and can be used to fabricate a wide range of materials with a diameter of 10 nm and tens of micrometres in length [2, 5]. However, it is still incompatible with conventional CMOS devices due to the lack of control of growth positions and the numbers of the nanowires, in addition to the incorporation of metal impurities into the nanowire during the growth [9].

2.1.2 Top-down approaches

The main methods that can be used to release SiNWs using top-down approaches are electron beam or nanoimprint lithography, and indirect methods.

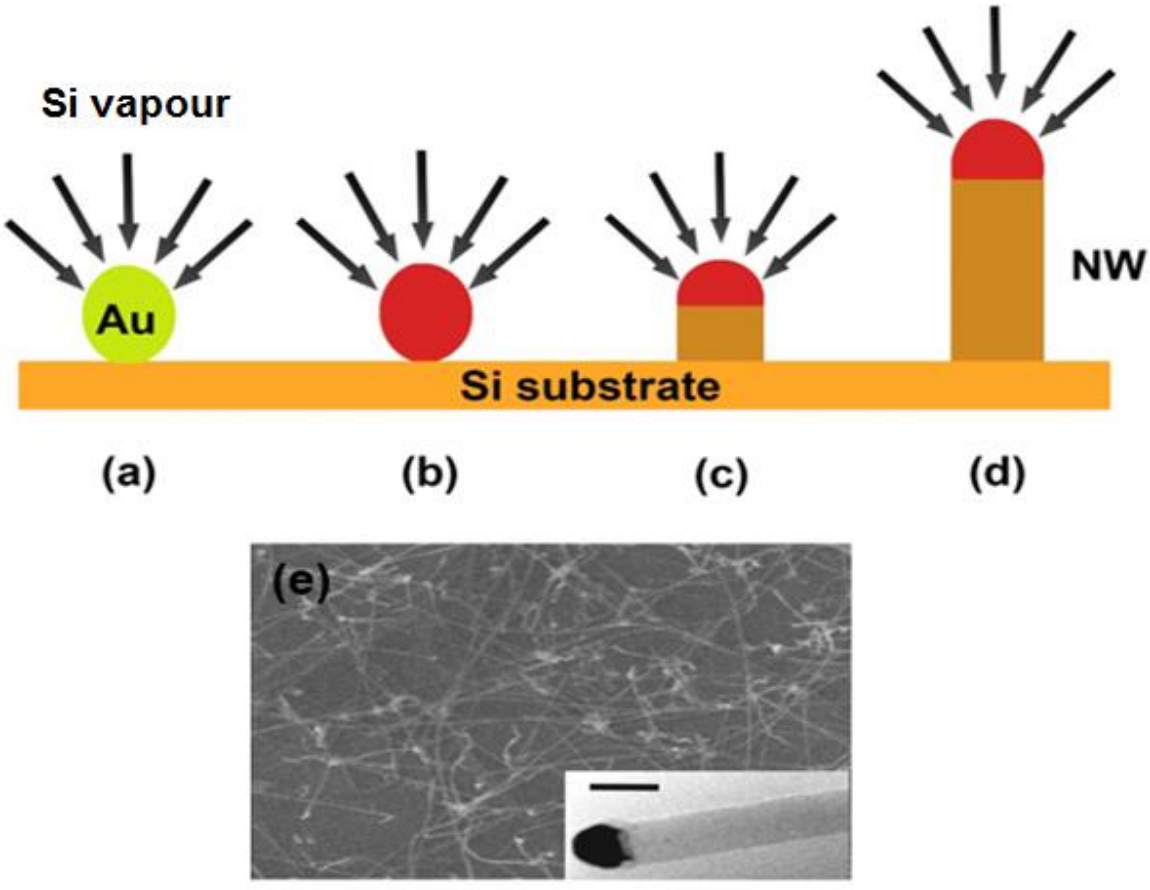


Figure 2.1: Vapour-liquid-solid growth mechanism of silicon nanowire: (a) gold nanodroplet on a clean surface; (b) eutectic droplet; (c) nucleation; (d) nanowire growth; (e) FESEM image of silicon nanowire grown via a VLS mechanism (scale bar 20 nm) [5].

Electron beam lithography

In this method, a focused beam of electrons is used to define the fundamental device structure on a layer of photoresist; etching is then performed to transfer the pattern onto the substrate. This method has much higher resolution compared with optical lithography because of the short electron wavelength that can be obtained [10], which is given by:

$$\lambda = \frac{h}{\sqrt{2qVm_e}} \tag{2.1}$$

where λ is the electron wavelength, h is Planck's constant, V is the accelerated voltage, q is the elementary charge, and m_e is the mass of the electron. This technique does not require a mask and features with less than 10 nm have been reported using this technique [10-12]. However, it is a slow and expensive technique.

Nanoimprint lithography

The concept and the main development in nanoprimrint lithography (NIL) were proposed by Chou's group in mid-1990s [13, 14]. Since that time this method has attracted considerable research effort and wide application due to its ability to fabricate small features for mass production with low cost [15-17].

There are three main process steps involved in the nanoimprint lithography technique [13, 15], as shown in Figure 2.2. Firstly, Nanostructures are formed on the mould using materials with good mechanical properties and with superior corrosion resistance, generally using electron beam lithography. Secondly, a thin layer of resist with low viscosity and good adhesion is coated on a substrate. The mould along with its pattern is then brought into contact with the substrate, patterning the resist surface in contrast to the pattern in the mould, followed by releasing the mould. Thirdly, subsequent anisotropic etching steps are required to remove the resist residual and transfer the pattern into the substrate. However, the high defect density and the accuracy overlay for multilayer imprinting processes are still problematic with regards to commercial productions [4].

Indirect techniques

In the aforementioned techniques, the dimensions of the obtained nanostructure are the same as the patterned structure. Thus those techniques can be considered to be direct methods. However, the dimensions of the nanostructure are limited by the resolution of the pattern technique. Over the last decade many methods have been reported for the fabrication of very fine nanostructures with no need to use high resolution techniques. Basically, they start with the patterning of wide structures, mostly using any lithography technique available in the cleanroom. This is followed by other process steps such as etching, deposition or thermal oxidation, to obtain small nanostructures. These techniques are cost-effective and can be categorised as indirect methods because the final nanostructure is not identical to the patterned one.

Below are some of the methods that can be classified as indirect top-down techniques:

i- Sidewall lithography

The main fabrication steps here are as follows [18, 19]: Firstly, a supporting microstructure is defined and transferred into the substrate. Secondly, a material with high selectivity for etching to the supporting material is conformable to the surface. Thirdly, reactive ion etching (RIE) steps are performed to form the final structure. In this technique, the width of the final structure depends on the thickness of the coated film rather than the patterned structure as shown in the schematic in Figure 2.3.

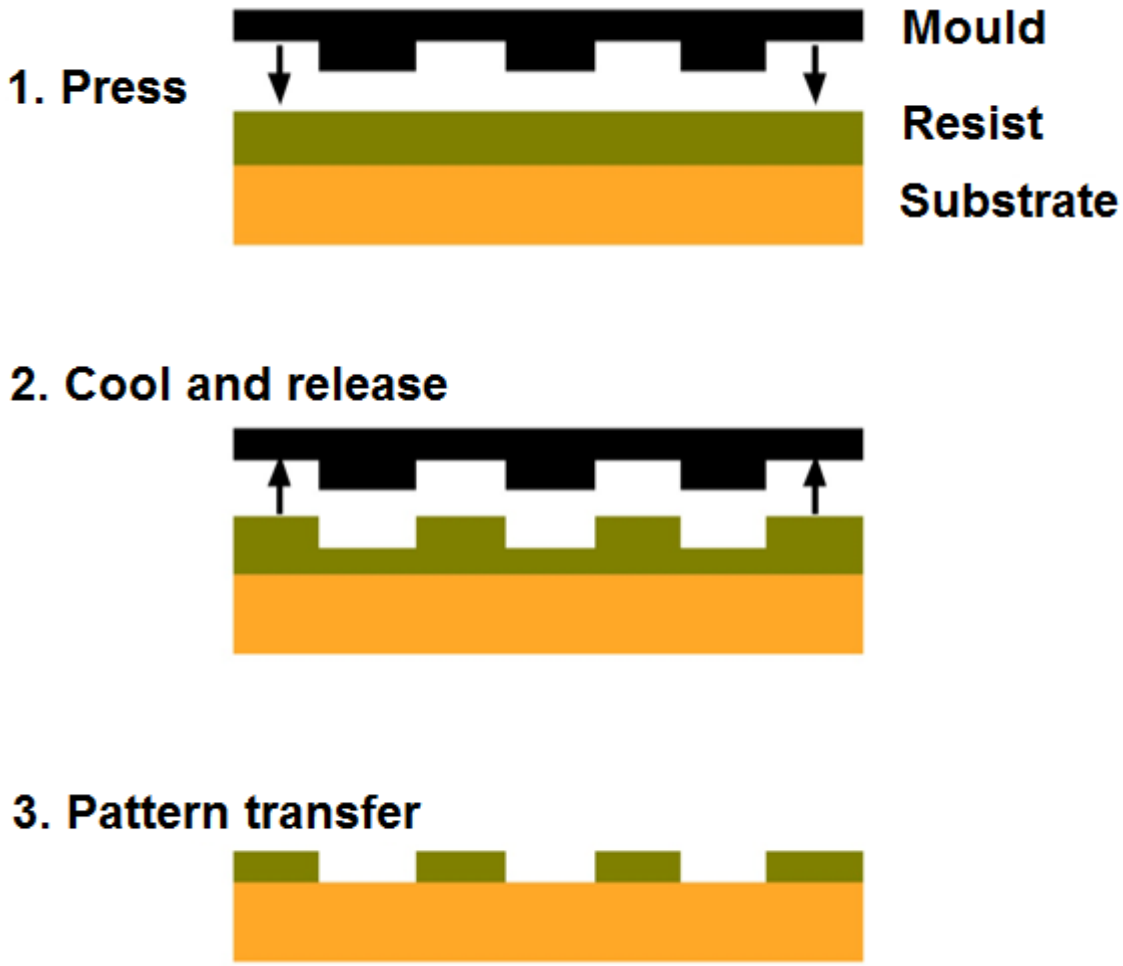


Figure 2.2: Schematic of nanoimprint lithography process, (a) Orient substrate and imprint the mould, (b) separate the mould from substrate, (c) remove resist and etch using RIE

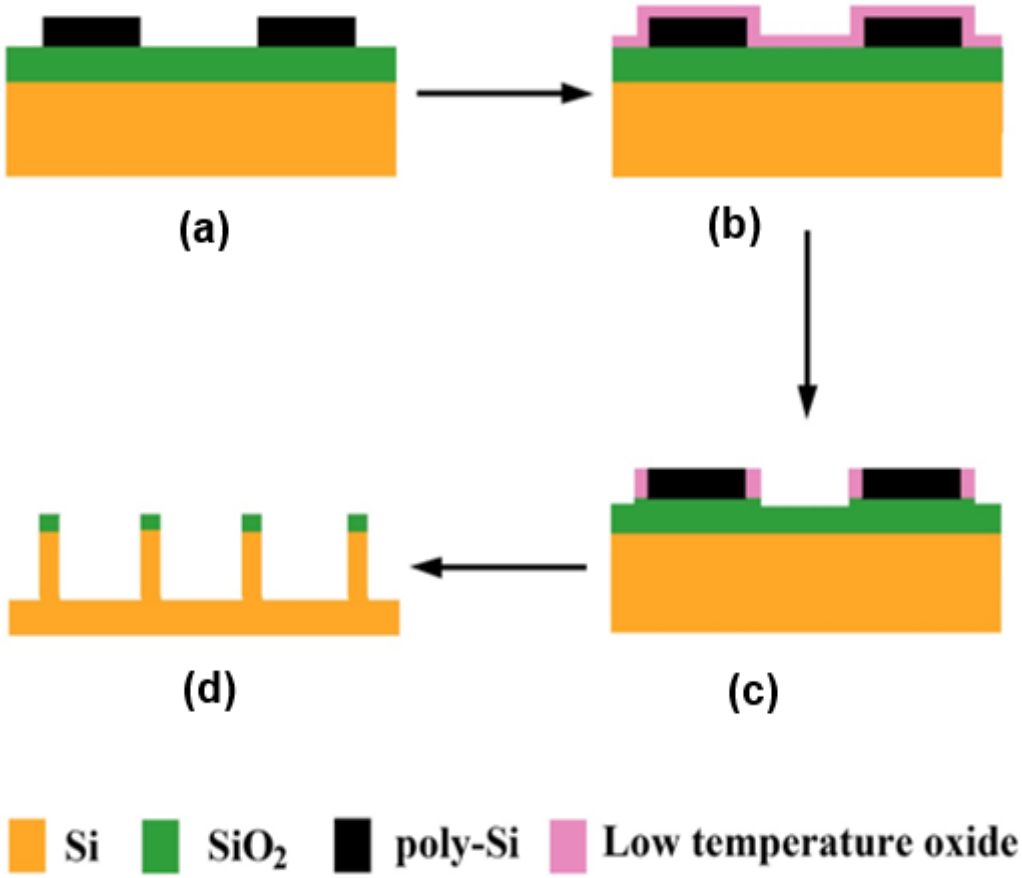
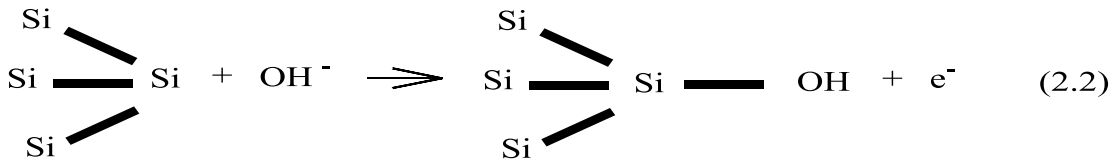


Figure 2.3: Schematic diagram of key fabrication steps of sidewall lithography: (a) deposition of sacrificial layer; (b) conformal deposition of low temperature oxide; (c) selective anisotropic dry etching; (d) subsequent selective anisotropic dry etching.

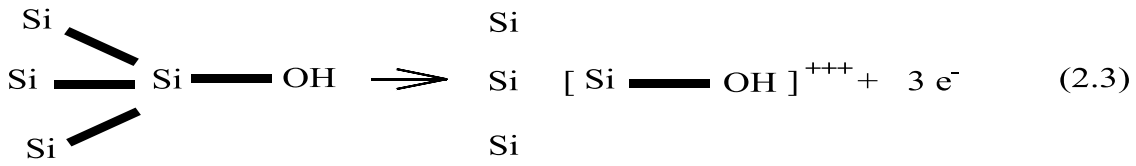
ii- Crystal orientation dependent etching techniques

The final nanostructures using these techniques are defined by anisotropic wet etchants such as Potasium Hydroxide (KOH), Trimethyl Ammonium Hydroxide (TMAH), and Ethylenediamine Pyrocatechol (EDP), instead of patterned lithography. The principle involved is based on those etchants that can etch single crystalline silicon with different rates for different crystalline orientations, e.g. where the etch rates in the <100> and <110> directions are much faster than in the <111> direction [20, 21]. The nature of the anisotropic action of these etchants is not fully understood. However, one of the commonly accepted explanations attributes the selectivity in etching between different planes to the difference in the density of the area of the dangling bonds and the strength of back-bonds [22]. For example, in the case of the (111) surface, an atom has one dangling bond and three back-bonds, whereas, in the first step, one hydroxide ion can bind to the atom as shown in equation (2.2):



(2.2)

In the second step, the three Si-Si back-bonds near the Si(OH) have to be broken to form a soluble Si complex as shown in equation (2.3):



(2.3)

whereas an atom on the (100) surface has two dangling bonds and two back-bonds. Therefore, during the reaction, two hydroxide ions are available to bind with two dangling bonds of a silicon atom on the (100) surface in comparison to one on the (111) surface. In addition, the silicon atom has to break two back-bonds in the case of the (100) surface in comparison to one on the (111) surface. Therefore, it is assumed that the energy required to break three back-bonds is higher than that required to break two back-bonds [22].

Two main techniques have been developed to fabricate nanowires benefiting from the anisotropic etching of silicon. The first technique starts with the deposition on or growth out of scarified material such as silicon dioxide on top of a thin silicon layer. Then a microstructure is patterned and defined using lithography and etching, and this is followed by a controllable anisotropic etching step to define the final nanostructure [23, 24]. The final structure obtained normally has a trapezoidal cross section with two <111> planes and one <100> plane [25]. (Figure 2.4(a))

The second technique is not limited by lithography, but uses a sidewall to make the fine nanostructure. In this method, after patterning a microstructure, a step of anisotropic etching is performed along the <111> plane. Then the <111> plane is protected by another sacrificial material. After that the first sacrificial layer is removed followed by a second anisotropic etching step. The final structure has a triangular cross-section [26, 27] (Figure 2.4(b)). These methods are cost-effective and the diameter can be reduced to below 30 nm.

Only a single step of anisotropic wet etching is applied in the first technique, while two-steps, in addition to a thermal oxidation step are required in the second one. Nonetheless, a post-thermal oxidation step is required to reduce the size of the structure in the first technique, whereas the second wet etching stage can be applied to reduce the size of the structure in the second technique. This makes the second technique more appropriate for size reduction. Therefore, this technique is further investigated in this research.

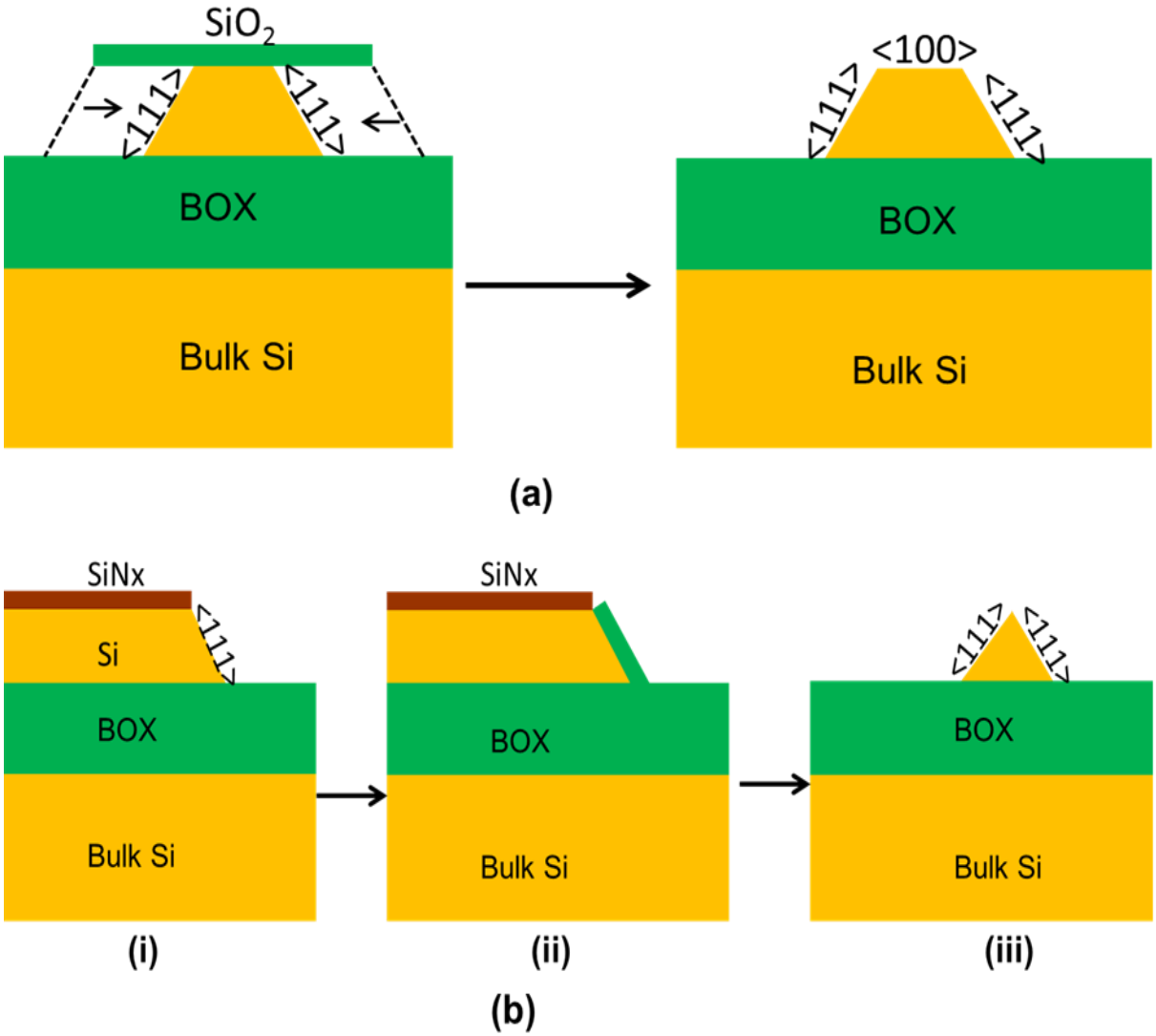


Figure 2.4: Two examples of crystal orientation dependent etching techniques: (a) a microstructure is patterned first then the nanostructure is formed after employing the anisotropic wet etching step; (b) a microstructure is patterned and formed using the anisotropic wet etching step followed by thermal oxidation and a second wet etching step.

2.2 Physics of semiconductor nanowires

The properties of nanowire are different from their bulk counterparts. Hence, due to the decreased dimensions, properties such as the band gap, ionization energy, doping and mobility become size dependent. Understanding these properties is essential in order to successfully integrate the nanowire into reliable applications. Some of the important properties of nanowires are described below:

2.2.1 Quantum confinement

The quantum confinement effect is one of the most direct effects of reducing the size of material to the nanostructure regime. It is observed when the size of the nanostructure is comparable to the wavelength of the electron. The confinement effect can change the shape of the density of states and the band gap of the material [11, 28]. Therefore, the optical and electronic properties of the material become dependent on its size [29].

Band gap

In crystalline structures, the energy levels broaden into "bands" which depend on the distance between the atoms in the material. Each band contains many allowed energy levels, and the allowed bands are separated by regions of energy that cannot be occupied by electrons. These are called band gaps. The electrical properties of materials are primarily determined by the nature of the energy bands. As the size decreases to the quantum confinement regime, this decrease leads the energy levels to become discrete which widens the band gap; and, ultimately, the band gap energy also increases.

The quantum confinement effect is observed when the size of a nanostructure becomes smaller than 5 nm [30-33]; therefore, this effect is considered insignificant in this thesis.

2.2.2 Size effect

The effect of size becomes prominent when the carrier mean free path is comparable to the size of the nanowire. In this regime, the properties of the nanowire, such as electrical and thermal properties depend on the surface conditions [34-36]. For example, a reduction in the thermal conductivity of silicon nanowires is observed with decreases of its size [37], and this reduction is larger in nanowires with rough surfaces compared with smooth surfaces due to the increase of surface scattering [38]. A reduction in the electrical conductivity of metallic nanowires compared to the bulk conductivity is also observed when the diameter of the nanowires is in the range of, or smaller, than the mean free path of the electrons [39].

2.2.3 Ionization energy

When impurities are added to the semiconductor, the impurity donor electrons (in case of *n*-type) will fill in certain impurity levels that usually lie close to the bottom of the conduction band. The energy necessary to move the donor electron from the donor level to the conduction band is called the ionization energy. The ionization energy is an important parameter in semiconductors because it determines the efficiency of doping. The ionization energy depends on the screened electrostatic potential [40-42]. In bulk silicon doped with phosphorous, the ionization energy is about 45 meV, and in heavily doped semiconductors

the screening effect is stronger due to the large number of electrons that shield the Coulomb potential. The ionization energy is expressed as [43, 44]:

$$E_D = \frac{E_{D0}}{1 + (1 + \frac{N_D}{N_{ref}})^2} \tag{2.4}$$

where E_{D0} is the ionization energy of the bulk semiconductor, which is 45 meV for phosphorous in silicon. $N_{ref} = 2.2\ X\ 10^{18} cm^{-3}$, and N_D is the donor concentration.

In silicon nanowires, however, as the volume reduces the number of the electrons shielding the ionized impurity also declines. This leads to a reduction of the screened Coulomb potential and an increase in ionization energy. This effect could increase if the nanowire is coated with a material that has a different dielectric constant. Diarra et al, reported an increase in ionization energy in nanowires due to dielectric discontinuity. They found that the ionization energy is theoretically inversely proportional to the radius of the nanowire, and this increases in the ionization energy due to dielectric mismatch and is given by [45]:

$$E_r = E_{DO} + \frac{2q^2}{\varepsilon_s r \varepsilon_d} \frac{\varepsilon_s - \varepsilon_d}{\varepsilon_s + \varepsilon_d} F\left(\frac{\varepsilon_s}{\varepsilon_d}\right) \tag{2.5}$$

where E_r is the radius-dependent ionization energy, ε_s is the dielectric constant of silicon, ε_d is the dielectric constant of the surrounding material, r is the radius of the nanowire, E_{DO} is the bulk ionization energy, and $F\left(\frac{\varepsilon_s}{\varepsilon_d}\right)$ is a positive function of the ratio of the dielectric constant of the nanowire to the dielectric constant of its outer surface material.

The increase in ionization energy causes a reduction in effective carrier density and consequently an increase in the effective resistivity of the nanowire [44-46].

2.2.4 Mobility

From the microscopic point of view, mobility can be expressed by the following expression [42]:

$$\mu = \frac{ql}{v_e m^*} \tag{2.6}$$

where q is the elementary charge, l is the electron mean free path, m^* is the effective mass of the carrier, and v_e is the drift velocity of the electron. In bulk silicon, mobility depends on carrier type and concentration. When the size of the nanowire decreases to be comparable to or smaller than the electronic mean free path (MFP), the mean free path will be affected by the surface and, thereafter, mobility becomes size-dependent. Mobility is also affected by quantum confinement due to the change in effective mass, and this effect becomes important at sizes less than 5 nm as mentioned previously.

2.3 Applications of silicon nanowire

2.3.1 Nanowire thermoelectrics

In the field of thermoelectric materials, silicon nanowires have superior properties compared with their counterpart in bulk silicon [36, 47, 48]. This superiority stems from the fact that the size of the nanowire is usually comparable to or smaller than the phonon mean free path. The efficiency of thermoelectric material is related to the dimensionless figure of merit parameter ZT, which is given by [38]:

$$ZT = \frac{S^2 \sigma T}{k} \tag{2.7}$$

where S is the Seebeck coefficient, k is thermal conductivity, σ is electrical conductivity, and T is the absolute temperature. Good thermal to electrical conversion efficiency depends on the value of ZT, which typically should be > 1. This can be obtained by increasing the electrical conductivity and minimizing the thermal conductivity of the material. Heavily doped bulk silicon devices have relatively good electrical conductivity as well as high thermal conductivity which make them poor thermoelectric materials. Due to strong phonon-boundary scattering at sizes less than the phonon mean free path, the thermal conductivity of silicon nanowires can be reduced without affecting the electrical conductivity of the nanowire [49]. An amorphous like value of thermal conductivity has been demonstrated in silicon nanowires of diameter 50 nm [38].

2.3.2 Piezoresistive silicon nanowire

The piezoresistance effect in semiconductors refers to the change in the conductivity of the material with applied stress. The piezoresistance effect has been widely studied and used in mechanical sensors [50-52]. Silicon nanowires are observed to have an unusually large piezoresistance effect (called “giant piezoresistance”), with an increase of almost two orders of magnitude compared with bulk silicon in the <111> direction [53]. This effect can be used to improve the speed of nanoelectronic devices, as well as in mechanical and biological sensing applications [49, 53].

2.3.3 Silicon nanowire-bio interface

Nanowires have a size much smaller than the typical biological cell size. They also have high surface-to-volume ratios and can be fabricated with high aspect ratios. These properties make them appropriate for communication with living cells for various purposes, such as extracellular and intracellular action potential recording [54-56], measuring the electrical and mechanical changes inside and outside the cell, or directing stem cell differentiation without causing damage to the cell [57]. Figure 2.5 shows a comparison of scales between nanowire size and the sizes of various biological objects.

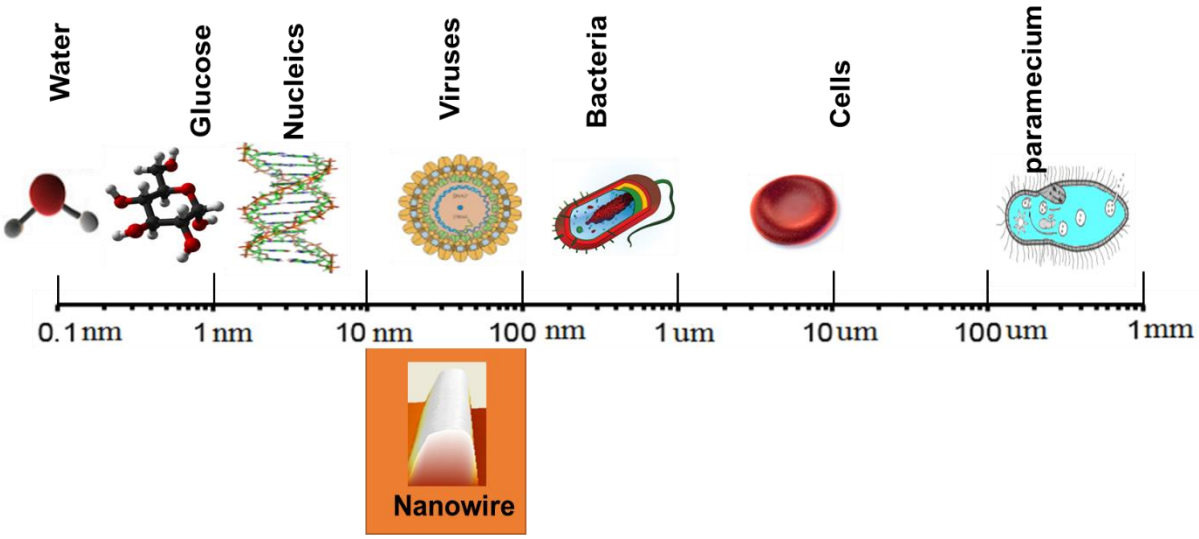


Figure 2.5: Scale bar of the size of nanowire compared to biological objects.

2.3.4 Biosensing application

Silicon nanowire biosensors are considered as real-time, label-free, multiplexing detection, high sensitivity tools for pH sensing, protein sensing, virus detection, ion sensing and nucleic acids detection. The basic principle of a silicon nanowire biosensor and its pH application are described below:

Nanowire biosensor

Figure 2.6 illustrates the basic structure of a nanowire biosensor. A p-type nanowire is rested on buried oxide (BOX) and connected to a source and drain. The electrical conductance of the silicon nanowire between the source and drain does not change with time (Figure 2.6(a)). By attaching charged species to the chemically modified silicon nanowire, the electrical conductance does change [58-60]. If the species are negatively charged, an accommulation region is created which leads to an increase in conductance in the case of the p-type NW (Figure 2.6(b)). If the species are positively charged, a depletion region is created which leads to a decrease in conductance. Therefore, the charged species at the nanowire surface work in a way similar to the gate in a field effect transistor.

pH sensing

pH sensing has been utilized as a characterisation model for the ability of a nanowire used as a chemical sensor. The first silicon nanowire pH sensor was reported in 2001 using the vapour-liquid-solid method [58].

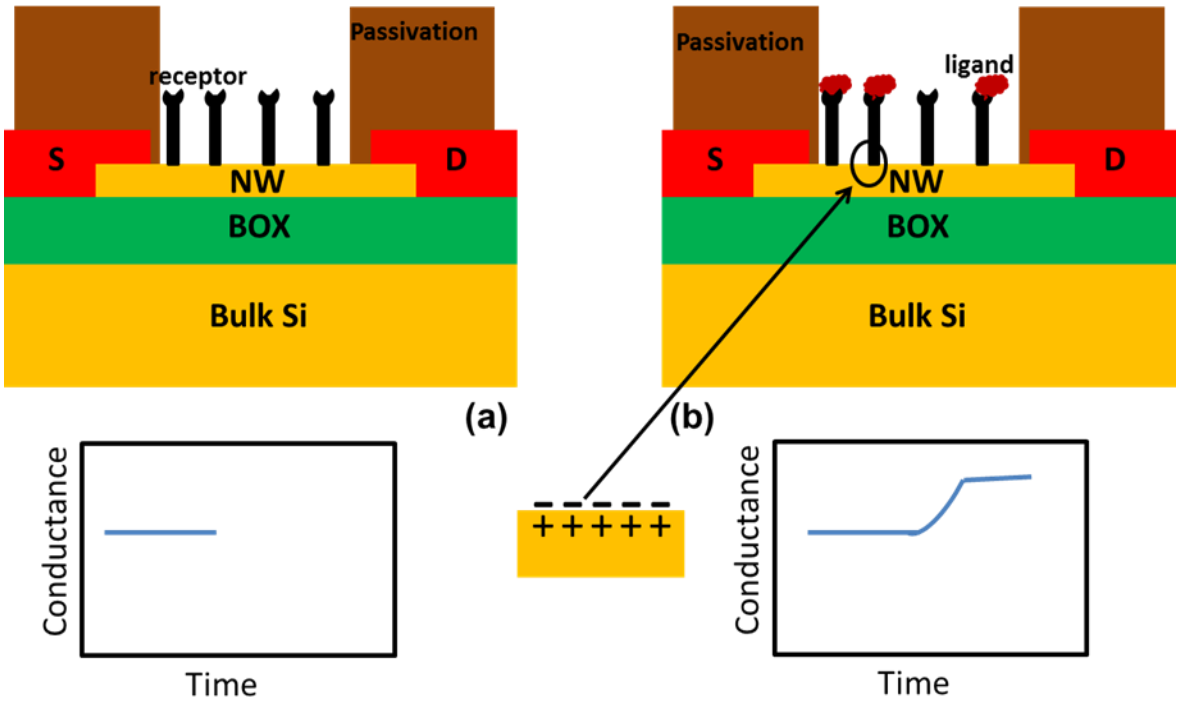


Figure 2.6: Basic structure of silicon nanowire biosensor: (a) schematic of a p-type silicon nanowire sensor with receptors and a plot of conductance as a function of time; (b) the nanowire response when negative ligands are attached to the receptors and the change in conductance as a function of time.

The surface of a silicon nanowire oxide was modified with 3-aminopropyltriethoxysilane, which leaves amino and silanol groups at the surface. The amino and silanol groups at the surface can exchange protons in the solution, and the nature of the surface can be determined by the value of pH. At a low pH value the surface charge is positive, and at middle and higher pH values the surface charge is neutral and negative respectively. Figure 2.7 shows a linear relationship between the conductance of the nanowire and the value of pH.

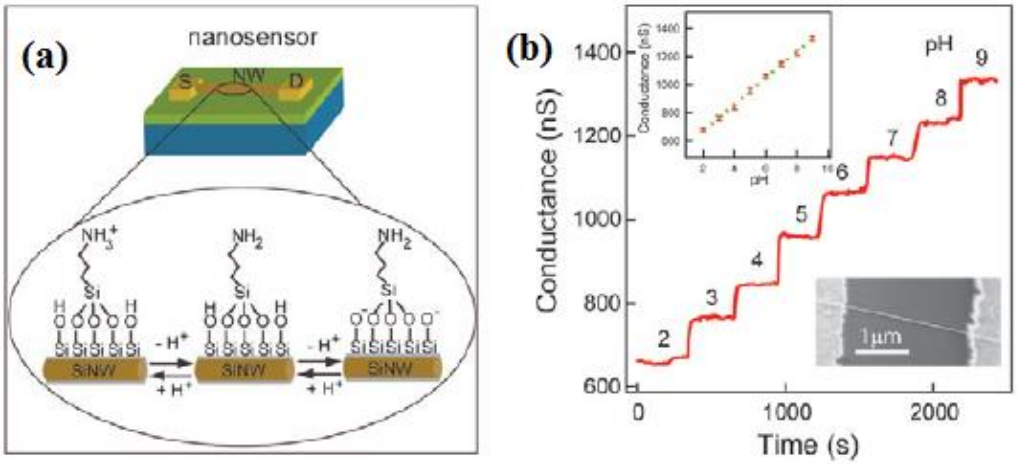


Figure 2.7: Silicon nanowire pH sensor: (a) schematic of silicon nanowire surface modified with a 3-aminopropyltriethoxysilane; (b) changes in nanowire conductance as a function of the pH in the solution [58, 59].

2.4 Summary

This chapter describes some of the essential aspects of silicon nanowire fabrication, and their electronic properties and applications. It reviews the top-down and bottom-up approaches which are the two main types of method used for fabricating silicon nanowires. The effects of quantum confinement, size effect and ionization energy on the electrical properties of silicon nanowires were described. With their unique properties compared to bulk silicon, silicon nanowires can be used in a wide range of applications including thermoelectrics, mechanical and biological applications. In the next chapter, the fabrication process of silicon nanowires using an indirect top-down method is described and optimised.

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Chapter 3

Fabrication of Silicon Nanowires

3.1 Introduction

Low dimensional nanomaterials have received increasing attention in the last two decades because of their unique physical and chemical properties for various ranges of applications. A large number of studies demonstrated nanowires as building blocks in applications, such as Fin FET, biosensor, thermoelectric and optoelectronic devices. In this field of research, silicon nanowires are the most fascinating objects for many reasons. First of all, silicon is a versatile and practical material, and it has a stable oxide at the interface. Moreover, a significant number of reliable silicon device designs are based on CMOS technology. There are two kinds of method developed to fabricate silicon nanowires: bottom-up and top-down. The former methods can produce nanowires of high quality, with controlled diameter. These remarkable methods are both simple and cheap. However, there is still a lot of concern over the doping level and growth positions of the nanowires, as these main drawbacks considerably limit the use of the bottom up methods. The latter, top down methods, such as optical and electron beam lithography have dominated the area of IC manufacturing for decades. Their applications for achieving nanometer array structures with high control of doping, position and feature sizes are still superior. However, further scaling using these techniques requires either additional tools or conditions, such as in Extreme UV (EUV) or slow and expensive ones, such as in electron beam lithography (EBL). Many top-down methods have been suggested to produce low cost sub-10 nanostructures such as patterning by using mechanical lithography nanoimprinting lithography (NIL) or AFM lithography. However, the high defect density and the complexity of nanoimprinting lithography NIL in addition to the low throughput in AFM lithography are still problematic. In recent years, a number of indirect top-down methods have been developed to extend the limit of standard lithography. In these interesting methods, wide features are patterned first, then certain process steps such as etching and thermal oxidation can be used to produce very small features. The indirect techniques are promising. However, the reliability and reproducibility still cause concerns.

Recently, an indirect top-down method based on optical lithography, anisotropic etching and thermal oxidation has been demonstrated [1]. However, this technique was not reproducible and required further optimisation before it could be used in device applications. This chapter reports optimization of the fabrication process of this technique and investigates the effects of many key steps, such as spin-on doping, thermal oxidation and anisotropic wet etching, on the reliability and reproducibility of the fabrication process.

This chapter will also describe the stages of optimised fabrication process for this technique. It begins by describing the spin-on-doping method (SOD) used to introduce the dopants into a silicon substrate. Then the fabrication process of silicon nanowires is illustrated. The key aspects that affect the reproducibility and reliability of the process, such as properties of the silicon nitride film during thermal oxidation, the behaviour of Si and SOI substrates during the oxidation using radiant and resistive heating sources, the robustness of a sidewall mask and the etching characteristics of Tetra-Methyl Ammonium Hydroxide (TMAH) and Potassium Hydroxide (KOH) etchants are then investigated. The chapter will also include some null results which might be beneficial for other research fellows.

3.2 Spin-on-doping SOD

3.2.1 Doping background

Nanowire based nanodevices, such as biosensors or nanoelectronic devices require precise control of doping level over the diameter and uniformity over large areas with high yield, and it is important that no lattice damage should be produced.

There are two main conventional methods to introduce doping in semiconductors, ion implantation and spin-on-doping (SOD). The former one injects ions into Si under accelerated electric field. This process can obtain controllable and precise doping concentration over large areas of the wafer. The process requires a low temperature and can work with a variety of masks and it does not require high cleaning procedures. However, ion implantation can cause displacements of the atoms and cause damage to the lattice [2].

The latter, Spin-on-doping (SOD), method is based on diffusion. In the most used technique, the dopant solution is deposited first using spinning, and then the solution is dried at low temperature to remove the excess solvent. The dopants diffuse into the film by subjecting the wafer to high temperature. The doping level and depth can be controlled by varying the temperature and time. This technique has no implantation defects, gives high yield with good uniformity and shallow junctions can be obtained [3]. However, this technique has drawbacks, as it can leave organic residual after thermal diffusion which is difficult to remove and may cause surface damage and degradation of device performance; in addition this technique does not have uniformity along the wafer [4, 5].

3.2.2 SOD process

In the current research, spin-on-dopants were used as dopant sources. The SOI samples were firstly cleaned prior to applying SOD sols. The cleaning procedures were carried out as follows:

a- General cleaning: the organic contaminants were removed with the use of NMP and IPA in an ultrasonic bath at 70 - 80 °C for 10 min, which was followed by rinsing with DI water.
b- Organic residues and metal particles were removed using Piranha solution 3:1 H_2SO_4: H_2O_2 in an ultrasonic bath for 10 min at 70-80 °C, which was followed by rinsing in DI water.
c- RCA1 cleaning: The insoluble organic contaminants as well as metallic particles were removed using 5:1.5:0.5 DIH_2O: H_2O_2: NH_4OH in an ultrasonic bath for 8 min at 70 - 80 °C.
d- The samples were dipped for 3 seconds in BHF to remove the oxide formed during the RCA1 process.
e- RCA2 cleaning: the remaining ionic metal contaminants were removed using 5:1:1 DIH_2O: H_2O_2: HCL 5:1:1 in an ultrasonic bath for 10 min at 70-80 °C.

In the typical cleaning, another BHF step to leave the surface of silicon hydrophobic should also have been included. However, in this process the step was skipped as it had been reported that keeping the hydrophilic surface could improve the uniformity of dopants [6]. Also, a faster dopant removal in the case of a hydrophilic structure than in the case of a hydrophobic one was also observed in this research.

The cleaned samples were then coated with SOD solution (being a mixture of silica, solvent and P_2O_5, in case of phosphorus) and spun at 3000 rpm for 20 sec, and then heated in the oven for 30 min at a temperature > 130 °C, while typically the solution is baked at a fixed temperature 150 °C, for solvent evaporation and forming the porous structure [7]. The dopants were then diffused into the silicon by using rapid thermal processing (RTP) or furnace with temperature ranging from 850 °C to 1100 °C. The diffusion reaction of phosphorous into silicon is ideally given as $2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2$. The furnace was then cooled down to room temperature before removing the wafers.

The SOD thickness was then measured by using optical ellipsometry; the measured thickness was between 70-85 nm and refractive index ranged from 1.47-1.49.

3.2.3 SOD removal

One of the most difficult steps in the SOD process is removing the SOD layer, which is due to the formation of a thin organic layer on the silicon surface after coating that could decompose into carbon and diffuse into silicon during the diffusion of dopants at high temperature [8]. This layer is difficult to remove and leaves damage on the surface, as well

as causes degradation in device performance. The typical SOD cleaning procedure includes a 45 sec BHF step to remove the glass layer first, oxidising the silicon surface, prior to removing the oxide layer using another step of BHF.

In this experiment, the cooling temperature was the most critical step in obtaining reproducible results. Thus, a series of treatment steps was carried out consisting of two sets of samples one after leaving the furnace to be cooled down to temperature between 300-400 °C and the other set after cooling to room temperature, which was then followed by certain SOD removal procedures. These procedures included a sequence of BHF etching and oxidation steps, using acetone. It was observed that a damage free surface was, interestingly, obtained only on the samples cooled to room temperature. This could be noticed easily as a hydrophobic surface was left after removing the dopants from BHF. This procedure was repeated by using different oxidants, such as HCL at 70 °C, 5:1.5:0.5 DIH_2O: H_2O_2: NH_4OH at 70 °C or by doing a short oxidation step at a temperature of 800 °C. However, reproducible results were only obtained on the samples cooled to room temperature in nitrogen (N_2) after dopant diffusion. The reliability of this method was confirmed after repeating it for tens of times during the fabrication of the nanowires. However, the other procedures were only repeated three times each.

Recently, it was reported that performing an oxidation step at a relatively low temperature prior to dopant diffusion into the substrate can reduce carbon contamination in the dopant source and improve solar cell device performance [4]. This step could be looked into future experimental work for process optimisation.

3.2.4 Doping Profile

The doping profile and film resistivity were obtained from the measured sheet resistance. The sheet resistance was measured by using a dual configuration method, as shown in Figure 3.1.

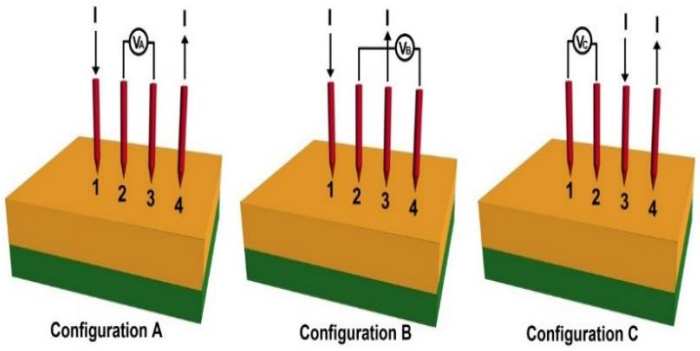

Figure 3.1: Schematic of four probe configuration technique.

This technique followed the procedure in which four probes were placed on the substrate in a straight line; then two separate resistances were measured using configuration A, B or A, C and sheet resistance R_S then was calculated by using [9, 10]:

$$exp\left(\frac{2\pi R_A}{R_S}\right) - exp\left(\frac{2\pi R_B}{R_S}\right) = 1 \qquad (3.1.a)$$

or

$$exp\left(\frac{2\pi R_A}{R_S}\right) - exp\left(\frac{2\pi R_C}{R_S}\right) = 1 \qquad (3.1.b)$$

where R_A, R_B and R_C are the resistances for configuration A, B and C respectively. The measured sheet resistance was used to calculate the resistivity of thin film as:

$$\rho = R_S \times t \qquad (3.2)$$

where *t* is the thickness of the silicon film.

The impurity concentration in the silicon film was determined as a function of resistivity from [11].

Equation 3.2 assumes that the electrical resistivity of the film is vertically uniform. However, in the diffusion process used to form the doped region, the doping and therefore electrical resistivity varies with the film depth. The silicon layer thickness in this study is about 150 nm. Consequently, this thickness is thin enough to make the change of resistivity less an order of magnitude, so Equation 3.2 is approximately valid.

The probe penetration can increase the bulk contribution in the measured current. Conversely, this contribution affects the accuracy of the measurements in shallow junctions (sub-20 nm) and lightly doped structures [10]. Given that the samples in this study are thick enough, and moreover are heavily doped, the effect of probe penetration can be neglected.

Equation 3.2 does not take into account surface absorption and scattering effects. When the thickness of the film is comparable to the mean free path of electrons the electrical properties become size dependent. However, Equation 3.2 is still valid provided that the thickness is larger than 20 nm, as discussed in section 5.4.

The effect of the surface states on the dopant activations can be significant; therefore, this effect is comprehensively studied in section 5.3. On the contrary, it is expected that the effect of surface states on the dopant activation is lower than the values reported in section 5.3. This is due to that the sheet resistance measured on carefully cleaned surface immediately after the BHF treatment. Moreover, the silicon layer is bounded by one interface, while in the case of nanowires, the silicon nanowire is coated all around, which means that the traps contribute more to the measured resistivity.

The above measurements were performed to give an initial idea of the impurity concentration inside the silicon film. Nevertheless, there are several steps and measurements used in this research to accurately define the sheet resistance and bulk resistivity of the silicon layer. This includes the measurements of sheet resistance with depth (next paragraph) annealing to obtain uniformity profile (section 3.3), and measurements of sheet resistance using a defined test structure (section 4.3.1).

Figure 3.2 shows the average impurity concentration level at different RTP pyrometer set point temperatures for 5 min. The data indicates that the electrically active doping level can be controlled by annealing temperature. While in case of furnace diffusion at 1100 °C for 15 min, the impurity concentration was in the 2.8 X 10^{18}- 5 X 10^{18} cm^{-3} range (not shown in Figure 3.2).

It is worth noting that the dual configuration technique does not extract carrier concentration but instead it measures the impurity concentration. In order to estimate the activated carrier density, temperature measurements of resistivity are required. The measured resistivity as a function temperature can subsequently be used to extract the carrier density versus temperature according to the following formula $n(T) \propto \frac{1}{\rho(T)\mu(T)}$. The extracted carrier density can be used to determine the ionization energy $n(T) \propto \exp(-{}^{E_D}/_{2KT})$. The ionization energy is an important parameter to calculate the effective carrier density. However, these measurements are not performed in this study and require further investigation.

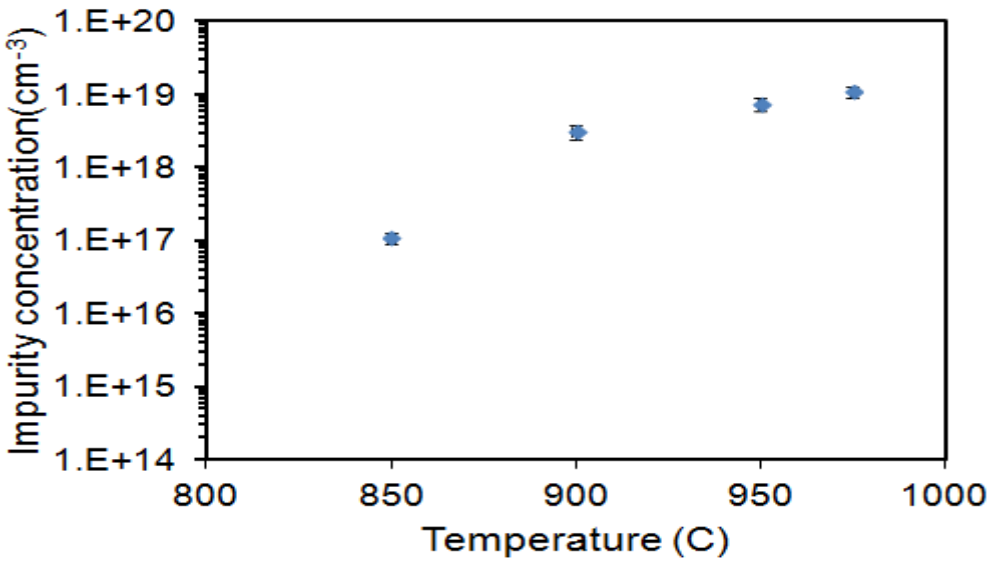

Figure 3.2: Average impurity concentrations as a function of RTP pyrometer set point temperature; diffusion time 5 min (each of these measurements were repeated three times). (N.B. Error bars are present in each data point, although some are not visible).

In order to obtain a better understanding of bulk resistivity and dopant density as a function of depth, a differential sheet resistance measurement was performed. In this measurement, the sheet resistance was obtained by considering the film as multiple thin films stacked on top of each other. The thickness of each layer is $(t - x)$ where x is the coordinate from the surface into the film.

The procedures to obtain these measurements were performed after a consecutive number of etching steps using reactive ion etching (RIE). In each step, a portion of silicon was etched using SF_6/O_2 followed by measuring sheet resistance with the application of the dual configuration technique; subsequently, the impurity concentration in silicon was calculated, as referred to above.

Figure 3.3 shows the phosphorus distributions in SOI as a function of silicon depth at two durations of annealing times 120 sec (the blue circle) and 300 sec (the red triangle). The results show the ability to control the dopant distribution in the SOD process through the optimization of annealing time in RTP. It is worth noting that these measurements were repeated four times.

To further link these experimental data with the theoretical models, the doping profile was calculated as a function of depth and time. Since the dopants were introduced by a constant source of dopants, the doping profile would follow a complementary error function *erfc* which is given by [11, 12]:

$$N(x,t,T) = N_s erfc\left(\frac{x}{2\sqrt{D(T)t}}\right) \tag{3.3}$$

where *Ns* represents dopant atom concentration at the surface, x is the junction depth, t is diffusion time, and $D(T)$ is diffusivity coefficient. The calculated doping profile is shown in Figure 3.3 for t = 120 sec (blue line) and t = 300 sec (red line) where $D(T)$ was chosen to be $D(T) = 9.2\ X10^{-14}$ cm^2/sec to fit the experimental data. This value of diffusivity coefficient (D) corresponds to $T = 1050$ ℃ [11, 13] while the RTP process was performed at a pyrometer temperature of 975 °C. The mismatch between these two values could be due to the error of reading the temperature by pyrometer, as will be discussed later in section 3.5.

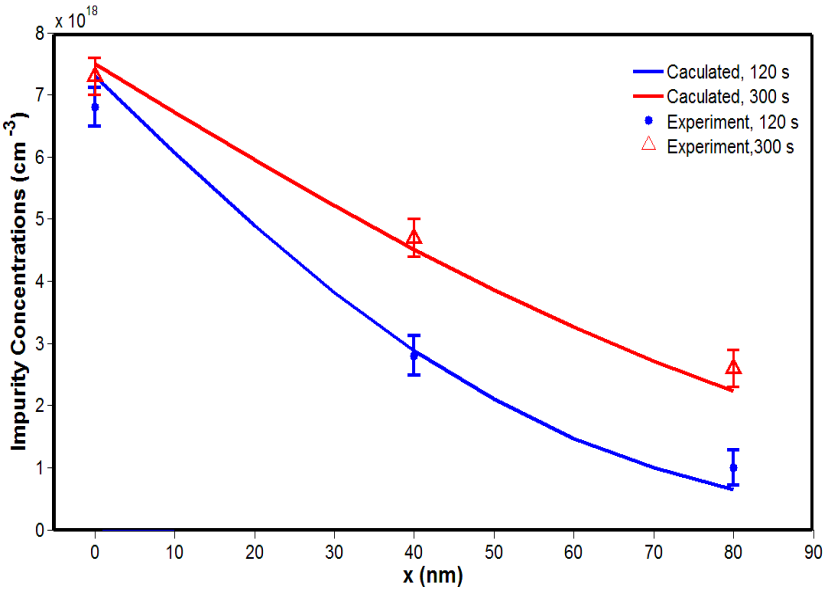

Figure 3.3: Impurity concentrations as a function of depth at pyrometer temperature of 975 °C for 120 sec (blue circle); 300 sec (red triangle); 120 sec calculated (blue line) and 300 sec (red line).

3.3 Fabrication of silicon nanowires

3.3.1 Fabrication process steps

The fabrication process was performed on a doped <100> SOI substrate sample, the doping process is described in the previous section; the whole fabrication, based on the method reported in [1], proceeded as follows:

3.3.1.1 Oxide opening: a 30-50 nm oxide was grown on the SOI substrate, a lithography step was used to define the area of the formation of nanowires. Then, a BHF step was performed to open a window through the oxide. The width of the window would determine the length of the nanowires, as will be demonstrated later. (Figures 3.4(a), (b), (c)).

3.3.1.2 Silicon nitride deposition and patterning: a layer of silicon nitride with 30 nm thickness was deposited by using RF sputter in pure N_2 at 90 °C. Then, the nitride film was patterned by another lithography step where the exposed silicon nitride was etched by using BHF. (Figures 3.4(d), (e))

3.3.1.3 First Orientation dependent etching (ODE): the samples were then etched, by using 25%wt TMAH solution with added 7.5% IPA at 56±1 °C to etch the exposed silicon. Due to the anisotropic characteristics of TMAH etching, the etch stops at the <111> plane. The etching time should be sufficient enough to expose the <111> plane and not too long to avoid wide undercut of the masked silicon nitride. (Figure 3.4(f))

3.3.1.4 Sidewall oxidation: the samples were oxidised to protect the exposed <111> plane for the next ODE etching step. Oxidation was performed by furnace or RTP to obtain a thickness of silicon dioxide between 15-18 nm. (Figure 3.4(g))

3.3.1.5 Removal of oxynitride and nitride layers: during sidewall oxidation not only silicon was oxidised, but also the silicon nitride was partially oxidised. The oxynitride thickness formed on top of silicon nitride, for samples deposited in pure nitrogen (N_2), was between 20-30% of the oxide thickness grown on bare silicon sample. Thus, the oxynitride was removed first by using an RIE step in pure argon (Ar), which was followed by a step of boiling phosphoric acid to remove the silicon nitride layer. (Figure 3.4(h))

3.3.1.6 Second Orientation dependent etching: another step of 25%wt TMAH solution with added 7.5% IPA at 56±1 °C was performed to define the nanowires. (Figure 3.4(i))

3.3.1.7 Sidewall oxide removal: the nanowires were then immersed in BHF for a few seconds in order to remove the sidewall oxide. (Figure 3.4(j))

3.3.1.8 Device isolation: The nanowires with their S/D contact regions were then patterned using a lithography step to isolate devices from one another. The isolation patterns were transferred by using an RIE step in SF_6/O_2. The Photoresist was then removed by immersing the samples for 10 min in NMP, which was followed by Piranha cleaning for 10 min; then the samples were placed in a plasma Asher for 2 min in order to remove organic residual. (Figure 3.4(k))

3.3.1.9 Nanowires oxide coating: the samples were cleaned twice in Piranha, RCA1, and RCA 2 for 5 min each at 80 °C. This was followed by dipping the samples in BHF for 3 sec in order to remove native oxide and then the samples were placed for 1 min in plasma Asher in order to remove any residual organic layer. Then they were placed in the furnace under nitrogen (N_2) conditions and annealed up to 930 °C. Once the temperature reached this level, the nitrogen (N_2) was turned off and oxygen (O_2) was purged into the chamber for 12 min and was switched off and N_2 purged again for similar time in order to remove fixed oxide.

3.3.1.10 Contact opening: the area of contact was then patterned and defined by using lithography and BHF etching. (Figure 3.4(l))

3.3.1.11 Metallisation: another lithography step was performed to pattern the contact pads. Then the electron beam evaporator was used to deposit a 60/100 nm of Ti/Al, which was followed by lift-off step in acetone in order to remove the photoresist. (Figure 3.4(l))

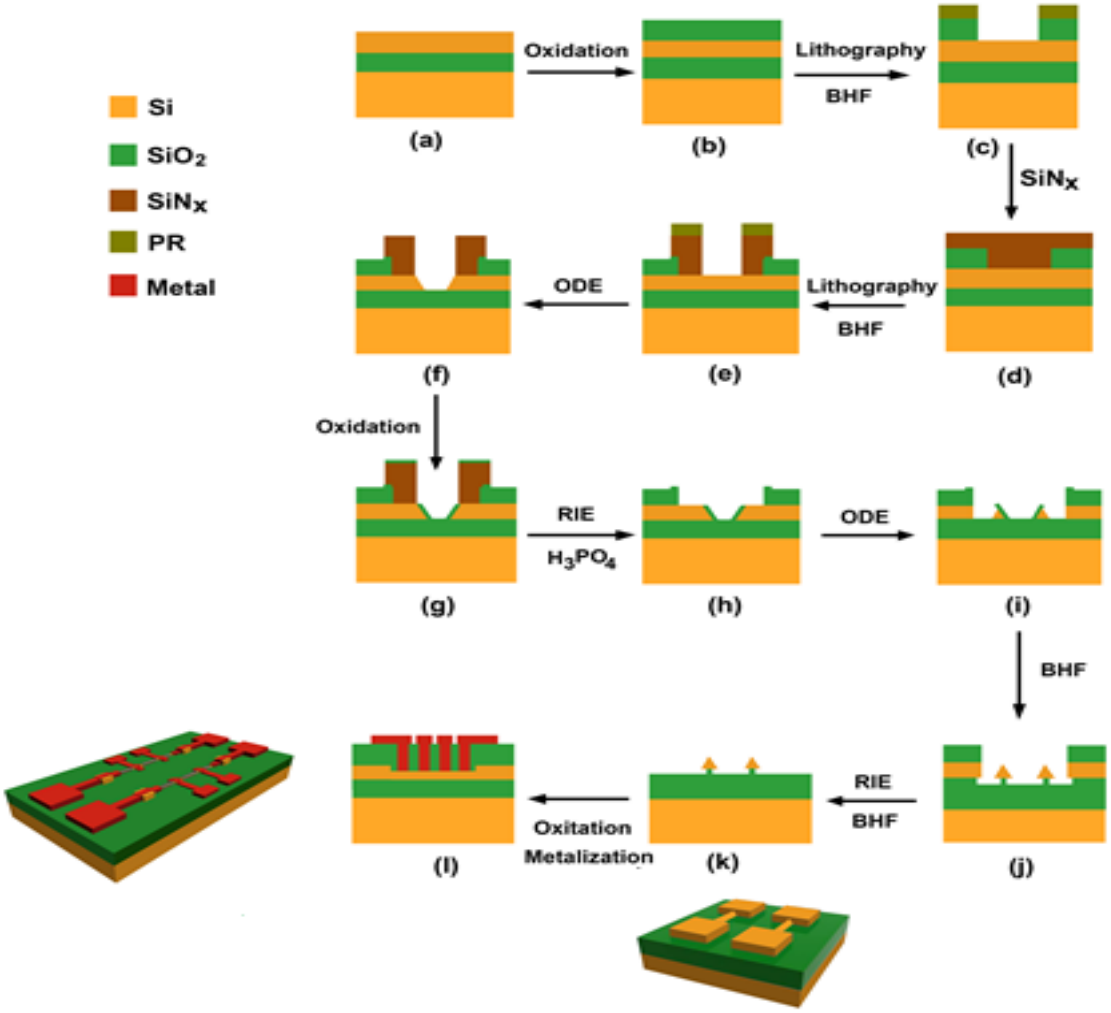

Figure 3.4: Process steps for the fabrication of silicon nanowire: (a) Doped SOI; (b) Oxidation; (c) Oxide opening; (d) Deposition of SiN_x; (e) SiN_x pattern; (f) 1st ODE etching; (g) Sidewall oxidation; (h) SiN_x removal; (i) 2nd ODE etching step; (j) Sidewall oxide removal; (k) Nanowire isolation; (l) Metal pattern for nanowire characterisation (with 3D schematic).

3.3.2 Nanowires profiles

The silicon nanowire profiles were obtained by using Atomic Force Microscopic (AFM). Therefore, a very simple explanation of the working principle of AFM is presented first.

3.3.2.1 AFM basics

Figure 3.5 (a) is a basic block diagram of an AFM. AFM uses a cantilever with a sharp tip to detect the topography of the surface, where the forces between atoms at the end of the tip and the surface of the sample lead to deflection in the cantilever. This deflection is detected by a laser beam and reflected onto a photodiode. The cantilever is attached to a piezoelectric scanner maintaining a constant distance between the tip and the sample. The

forces between the tip and the surface of the sample strongly depend on the distance between them. When the tip is brought to a few nanometres from the sample the attractive van der Waals forces appear, which increase to reach a maximum at shorter distances. Next, the forces gradually decrease to be replaced by repulsive forces when the the distance between the atoms is smaller than the van der Waals radii due to Pauli repulsion. The forces between the tip and the surface are shown in Figure 3.5(b). The AFM can operate in different modes, such as static mode, when the tip physically contacts the sample and dynamic modes such as tapping mode and non-contact mode, depending on the tip-sample distance and the oscillation amplitude. High resolution surface features can be detected using AFM [14, 15].

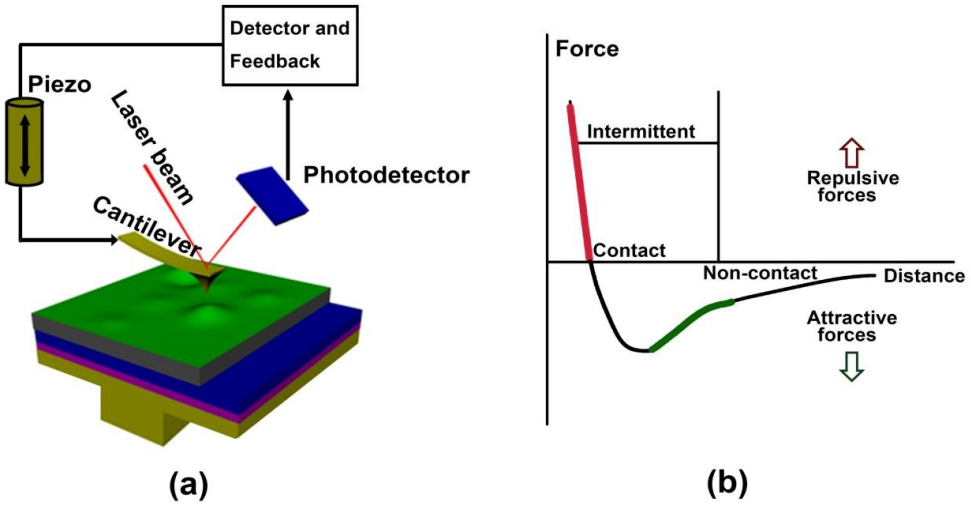

Figure 3.5: (a) A basic block diagram of an AFM; (b) the forces between the tip and the surface.

3.3.2.2 Modelling the tip effect on nanowire width

The limitation of an AFM is that its lateral resolution depends on the size and shape of the tip which makes the measured lateral AFM image wider than the actual structure. This is referred to as a convolution effect, as shown in Figure 3.6(a). The increase in width should be taken into consideration to accurately determine the geometry of the structures. Therefore, the increase in the width due to the convolution effect was estimated by using a simple model that takes into account the diameter of the tip, the thickness and the sidewall angle of the nanowire. Two cases were considered in this model, as follows:

Case 1: The radius of the tip R is larger than the thickness of a nanowire; this case is shown in Figure 3.6(a), the increase in the width $i = x1 - x$ where $x1 = \sqrt{R^2 - (R-h)^2}$ and $x = h\cot\beta$ where R is the tip radius, h is the thickness of nanowire and β is the sidewall angle of silicon.

Case 2: The radius of the tip is smaller than the thickness of nanowire. This case is shown in Figure 3.6 (b); the increase in the width, $i = R\ \cos\ (90 - \beta)$.

The critical thickness of nanowire h_c that determines which case should be used to calculate the value of the increase in the nanowire width can be extracted from Figure 3.6 (c) and given by:

$$h_c = R - Y = R(1 - \cos\beta) \tag{3.4}$$

Therefore, the actual width of nanowire w as a function of measured value w_m and geometry of nanowire and tip radius can be rewritten as:

$$w = w_m - 2i = \begin{cases} w_m - 2(\sqrt{R^2 - (R-h)^2} - h\cot\beta), & h_c \le R(1-\cos\beta) \\ w_m - 2(R\cos(90-\beta)) & , \; h_c > R(1-\cos\beta) \end{cases} \tag{3.5}$$

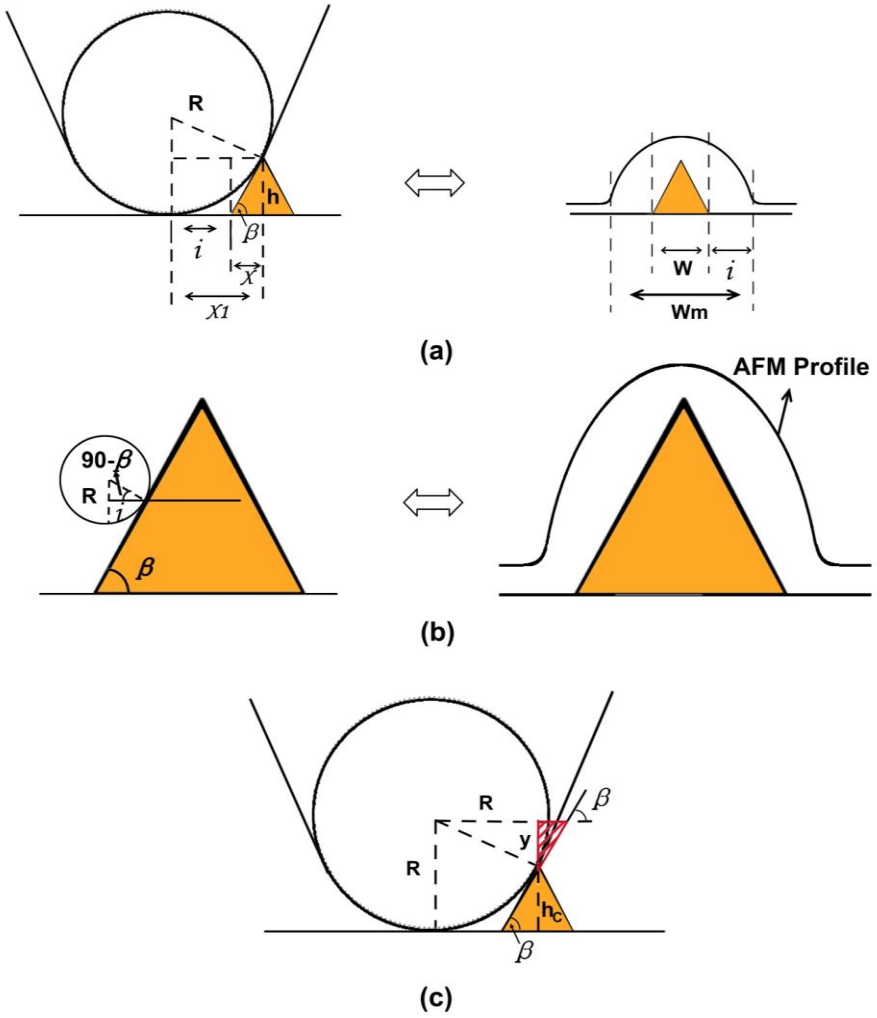

Figure 3.6: The convolution effect on the width of nanowire (a) an AFM tip with a radius larger than the thickness of nanowire (left), AFM trajectory (right); (b) an AFM tip with a radius smaller than the thickness of nanowire (left), AFM trajectory (right); (c) the critical dimension of nanowire h_c= R- Y.

3.3.2.3 AFM images

Turning to the experimental procedure, the geometries of the fabricated nanowires were analysed by using two types of non-contact AFM tips, very sharp SSS-NCHR tips with typical tip radius <5 nm and aspect ratio 4:1 at 200 nm and commercial ACTA tips with typical tip radius <20 nm and aspect ratio 1.5-3:1. The AFM profiles for different nanowires with different thicknesses are shown in Figures 3.7(a), (b). It should be noted that more than 20 AFM scans were performed on each sample with one or two locations along each nanowire.
As shown in the AFM images, the process can produce nanowires with either trapezoidal or triangle cross-section depending on duration of time in 2nd ODE solution.

The trapezoidal cross-section was formed due to the growth of a silicon dioxide layer under the edge of silicon nitride due to the lateral diffusion of oxygen under the edge of silicon nitride layer during sidewall oxidation resulting in a so-called bird's beak structure [16, 17]. The lateral length of oxide could be three times the sidewall oxide thickness and it increased as the nitride thickness decreased [17, 18].

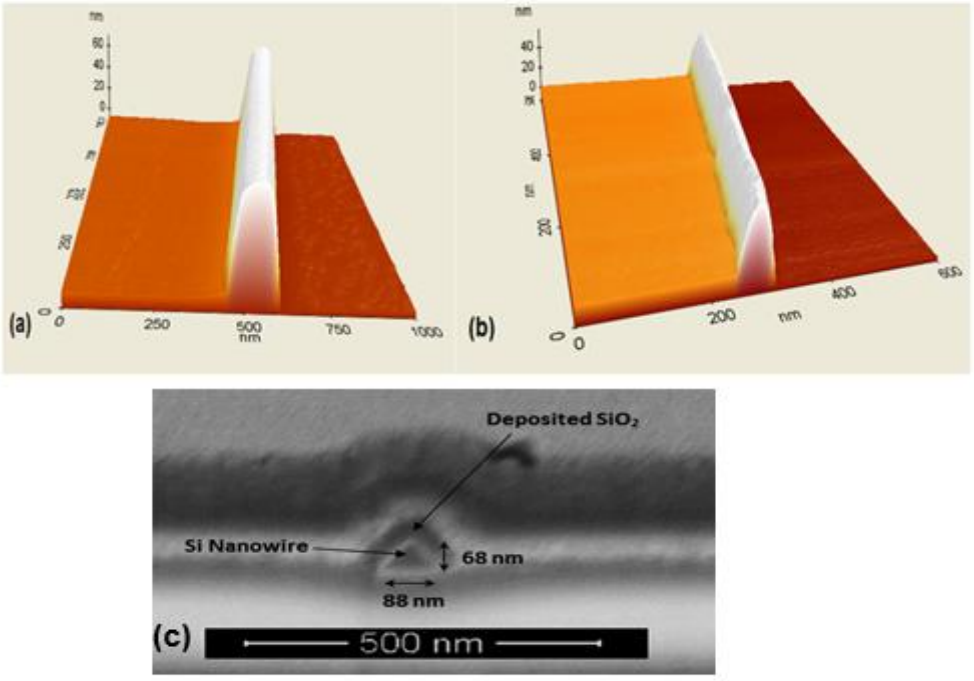

Figure 3.7: (a) 3D images of silicon nanowires with a trapezoidal cross-section; (b) 3D images of silicon nanowires with a triangular cross-section; (c) SEM image of a Si nanowire with a triangular cross-section [1].

3.3.3 Silicon nitride mask

During the oxidation of the <111> plane in section 3.3.1.4, both sidewall silicon and silicon nitride were oxidised where the top layer of silicon nitride was converted into oxynitride. The oxidised silicon nitride, SiNx / SiNxOy, has a much lower etch rate in boiling phosphoric acid in comparison with deposited silicon nitride and lower selectivity compared with silicon dioxide. As a result, when the sample was placed in boiling H_3PO_4 to strip the SiOxNy / SiNx layers, a portion of sidewall oxide was also removed. Furthermore, if the oxynitride layer is too thick it could result in complete removal of sidewall oxide and failure in the formation of nanowires.

For the reasons mentioned above, in order to obtain a reliable process, two conditions have to be fulfilled: the silicon nitride film should have low oxidation rate; and also a high selectivity etching process of oxidised silicon nitride over silicon dioxide is required.

Therefore, extensive studies focusing on the effect of thermal oxidation on different kinds of silicon nitride under different deposition methods and conditions were conducted in this research. The silicon nitride film with the highest resistance to thermal oxidation was optimised to be used as a mask to obtain a reliable fabrication process. Detailed experimental work and discussion will follow later in this chapter, while here the focus is on a discussion of the properties of the silicon nitride film that was used as a mask in device fabrication.

In this fabrication process, the silicon nitride was deposited by using Oxford Instruments Plasmalab System 400 RF Sputter in pure nitrogen (N_2) at 90 °C with RF power of 150 W. The deposition rate was 2.5 nm/ min; the refractive index was between 1.81-1.94.

When this silicon nitride was oxidised at a temperature of 930 °C (the silicon dioxide thickness grown on the silicon substrate by this process was 18 nm) a portion of silicon nitride was converted into oxynitride. The ratio of converted oxynitride thickness to the total oxide thickness on silicon substrate was between 0.2-0.3. This ratio was determined by measuring the change of effective refractive index as a function of depth, by using optical ellipsometry after performing RIE etching in argon (Ar). As shown in Figure 3.8 the refractive index recovers after etching 5-7 nm from the top of the film.

Etching this oxynitride layer in normal silicon nitride etchant (boiling H_3PO_4) is very slow, and even slower than the etch rate of silicon dioxide. The etching process, therefore, required two etching steps: the first step of etching was used to remove oxynitride by using RIE in pure argon (Ar); the second step of etching was used after the removal of oxynitride layer and involved etching in boiling H_3PO_4 which is the main etchant of silicon nitride. The selectivity of silicon nitride over thermally grown oxide was approximately 4.3. It should be noted that the measurements were performed three times.

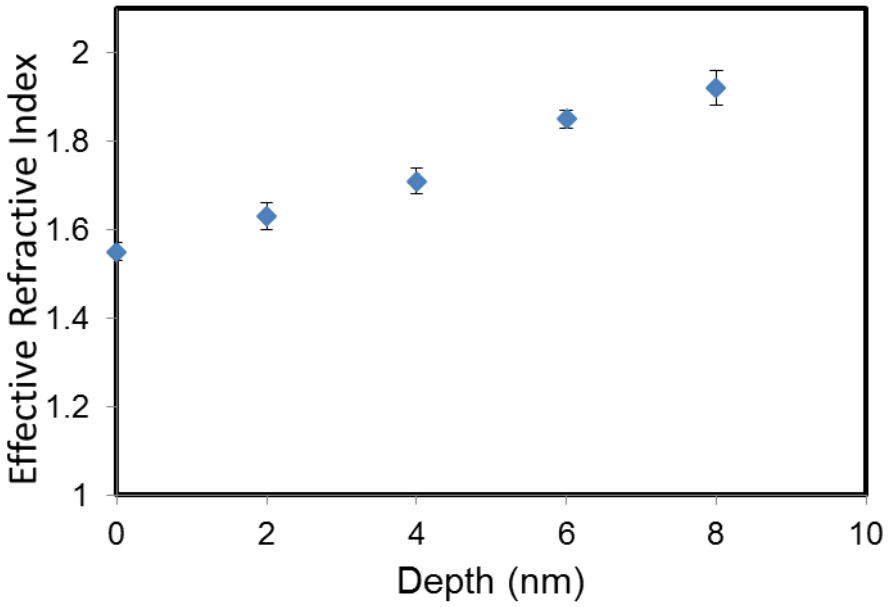

Figure 3.8: The refractive index of oxidised RF sputtered silicon nitride as a function of depth (the process gas is nitrogen and the as-deposited refractive index is 1.9).

3.3.4 Size reduction of nanowires

A number of methods can be utilised to reduce the size of nanowires. One of these methods applies etching steps using ion milling of the nanowires while masking the silicon pads. This method requires strict control of pressure and power to avoid damage to the structure and to reduce sidewall roughness occurring during the process. It is also possible to scale down the size by performing a sequence of thermal oxidation steps [19, 20]. The size can also be reduced easily by placing the samples for a longer time in the KOH or TMAH during the 2nd anisotropic wet etching step [21, 22], and this may be referred to as an *in situ* size reduction method. The latter two methods were investigated here to reduce the dimensions of the nanowires, as they are easier to apply than the former one.

3.3.4.1 *In situ* size reduction

The non-zero etch rate of the <111> silicon plane leading to anisotropic wet etching of silicon offers another advantage of using wet etchants such as TMAH and KOH to reduce the size of a silicon nanowire. Lateral and vertical size reduction of nanostructures by using anisotropic etching was reported earlier in many studies [21, 23]. However, more research is needed to investigate the concentration, temperature, and doping and solution type on the vertical and lateral size reduction of nanowires. In this fabrication 25 % wt. TMAH was used, with added 7.5% IPA at 56 ± 1 °C as an etchant to form the nanowires. The study will demonstrate size reduction under these conditions, which will further be developed in great detail, focusing on size reduction under previously mentioned conditions. The size reduction rate was defined by the lateral and vertical etch rate of the <111> plane. The

average lateral reduction was measured to be 20 ± 2 nm/min while the vertical etch rate was measured to be 12.8 ± 1 nm. This approximately equals $l = 2x = \frac{2y}{\tan\beta}$, where l and y are the lateral and vertical size reduction rates and β is the sidewall angle (refer to the schematic in Figure 3.9). Based on the measurements obtained the etch rate ratio of <111>/<100> was found to be between 0.12-0.13.

The etch rate with doping level was also measured and a lower <111> etch rate was observed, consequently with lower size reduction when the doping level increases, and it drops down by 25 % ,when the doping level is about 1.5 x 10^{19} cm^{-3}. The results are shown in Figure 3.10. (Note the <111>/<100> ratio measurements with doping level were not performed). More data and work will be presented later in this chapter.

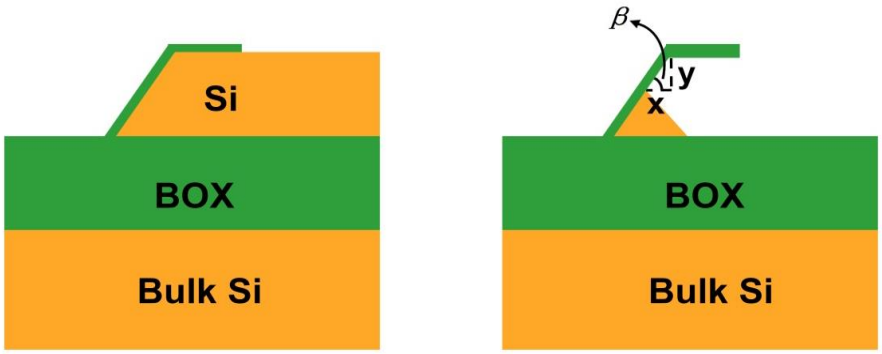

Figure 3.9: Schematic of the process steps involved during *in situ* size reduction of nanowires.

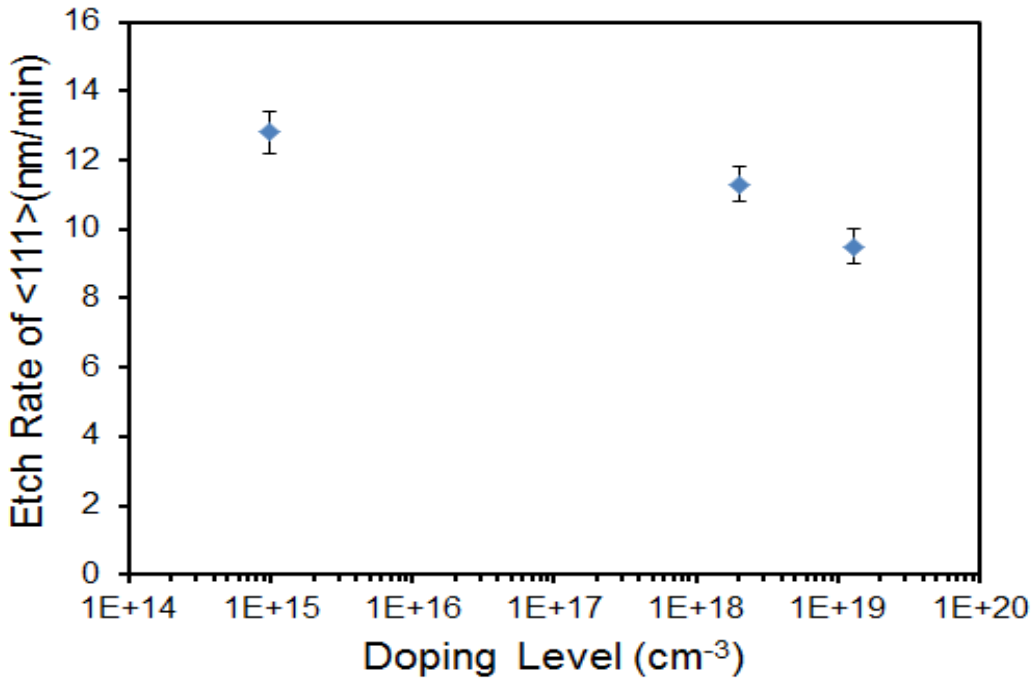

Figure 3.10: The vertical etch rate of vertical <111> as a function of doping level (each data point is the average for three experiments)

3.3.4.2 Size reduction by thermal oxidation

The fabrication process described previously can produce silicon nanowires with trapezoidal or triangular cross-section. These nanowires can be further reduced to a desired thickness by using thermal oxidation, where a controllable size reduction of nanowires can be achieved by precisely controlling the oxidation conditions. This size reduction method has been documented in more details in [19, 20]. However, the thermal oxidation step is required not only for size reduction, but also it is essential for a number of device applications. Therefore, it is worth attempting to investigate the effect of thermal oxidation on the silicon nanowires. Thus, the following steps were performed: an oxidation step by using the RTP system at 930 °C for 230 seconds to reduce the size of silicon nanowires which had a top width of 76 nm and thickness of 75 nm; then the samples were dipped in BHF for 25 seconds and scanned by using an AFM. The comparison between silicon nanowire profiles before and after oxidation are shown in Figure 3.11(a), which indicates non-uniformity in size reduction across the <111> plane thickness, where it is more apparent in the middle and at the top of the nanowire compared to the bottom corner of the nanowire. The difference in the size reduction could be due to the difference in oxidation rates between the flat surfaces and the edges. This geometry effect causes an enhancement in oxidation rate at the convex, compared to the concave edge due to the increase in the area exposed to the ambient [24, 25].

For further investigation, a Sentaurus TCAD simulation was performed to study the oxidation behaviour on the nanowires, similar to the work illustrated in [19]. The simulated structure had trapezoidal cross-sections as shown in Figure 3.11(b). Three steps of oxidation for 30, 60 and 120 min at 930 °C each were simulated. The oxide thickness and the shape of the nanowire after each step are illustrated in Figures 3.11(c), (d), (e). There are four regions to be considered during the oxidation of nanowires: region (A) the top flat <100> surface; region (B) the convex at the top edge; region (C) the flat <111> surface; region (D) the concave at the bottom edge. The ratios of oxide thickness in these regions at different duration of times are illustrated in Table 3.1. The difference in oxide thickness between these regions is visible.

The oxidation ratio between <111> and <100> surfaces at the beginning of oxidation, where the growth is in a surface reaction regime, reaches 1.65, which is typical of C/A regions, as shown in Figures 3.11(c), (d). After a formation of thick SiO_2 at the interface the oxygen needed to diffuse through the growing oxide to reach the underlying silicon, where the growth in diffusion reaction regime, which caused a decrease in the ratio, as shown in Figure 3.11(e).

There is a slow oxidation rate at the concave edge at the Si/BOX interface, which is typical of the (D) region. This can be explained by the reduction of oxidant species due to geometry effects. While this effect enhanced the oxidation rate at the convex edge, which is typical

of region (B). Moreover, region (B) is also situated between the <111> face with fastest oxidation rate and a <100> face, which could enhance the oxidation rate within this region.

Importantly, the simulated results show that a triangle nanowire is formed after 60 min oxidation which is in agreement with the results reported in [19], as shown in Figure 3.11(d).

It is also noteworthy, as can be seen in Figure 3.11(e), that the nanowire is pushed upward, which is due to the diffusion of oxidant species through the buried oxide, which oxidise the base of the nanowire resulting in the nanowire being pushed up [26].

Table 3.1: Oxide thickness ratios, regions A, B, C and D. Regions are defined in Figure 3.11(b).

Oxidation time (min)	B/A	C/A	D/A
30	1.27	1.5	0.99
60	1.41	1.64	1.17
120	1.4	1.51	1.24

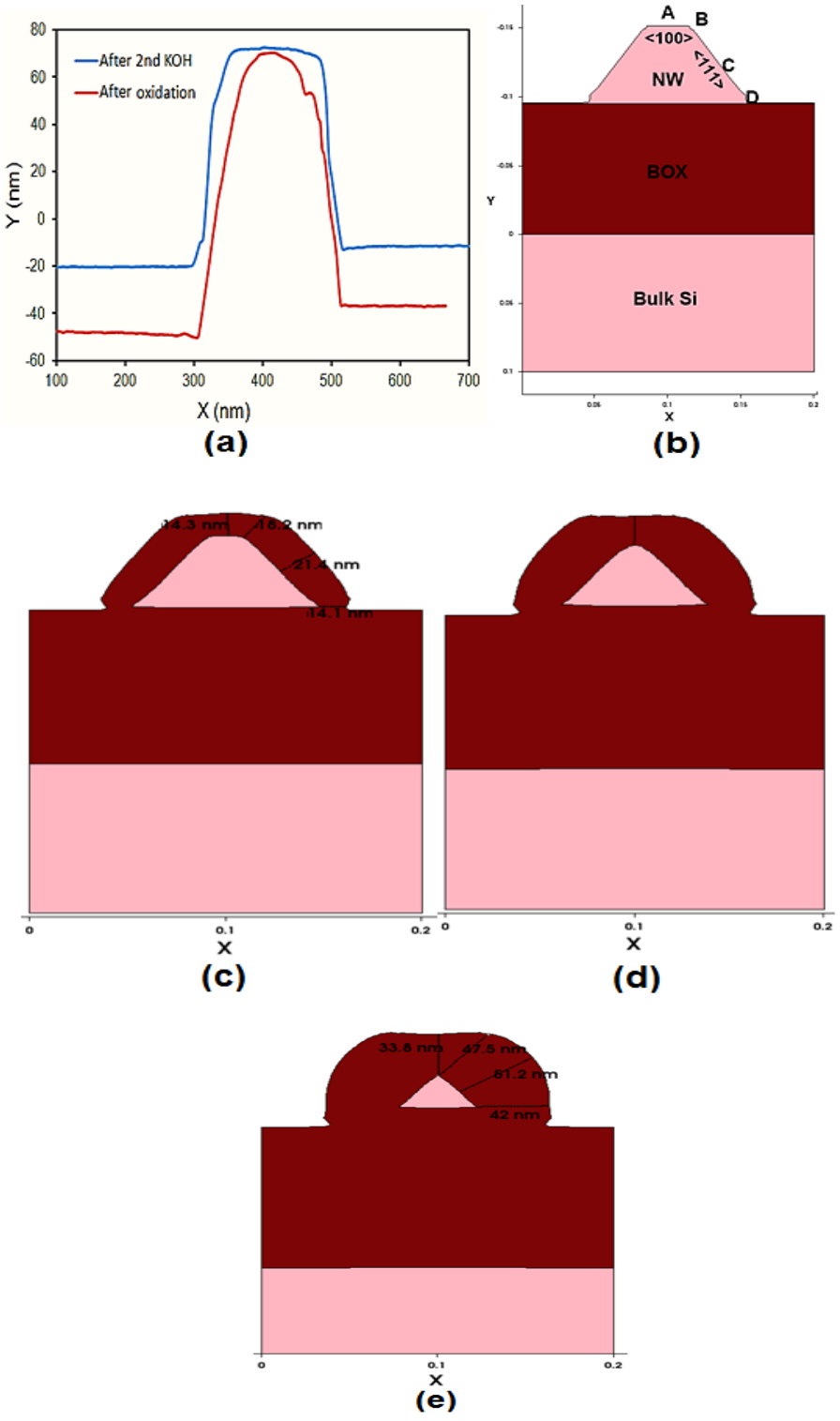

Figure 3.11: Size reduction of silicon nanowire by using thermal oxidation (a) experimental results before and after 930 °C in RTP and 20 sec in BHF; (b) simulated structure: (c) after 30 min oxidation; (d) after 60 min ; (e) after 120 min.

3.4 Fabrication considerations of silicon nanowires

In the previous sections, an optimised indirect top-down fabrication process of silicon nanowires was described, building on the method reported in [1]. The following section will focus on major fabrication steps to explore the parameters that control the yield and the reproducibility of the process. We will look further in depth into the following aspects based on experimental data:

1- The characteristics of silicon nitride films deposited, using PECVD and RF sputter methods under different conditions, as well as the impact of film property on the reproducibility and the yield of the process. Therefore, numerous experimental measurements were conducted, especially to test film behaviour following thermal oxidation, as well as to obtain a reliable etching process of thermally oxidised silicon nitride.
2- The behaviour of Si and SOI substrates during thermal oxidation performed in RTP and furnace. AFM and optical ellipsometry were used to determine the oxide thicknesses on Si and SOI. The obtained results raise the need for discussing optimising the reliability of both methods to be used during sidewall oxidation.
3- Comprehensive experimental measurements were carried out to compare the characteristics of TMAH and KOH etching to optimise the fabrication process. Thus, the etch profile; selectivity over silicon dioxide and the reliability to obtain controllable in situ size reduction were studied.

3.4.1 Characterisation of silicon nitride films

Silicon nitride has been used for a wide range of applications in the semiconductor industry. For example, it has been used as a passivation layer for integrated circuits due to its high atomic density and its resistance against diffusion of moisture or sodium ions and as an etch mask in microelectronic processing [27, 28].

Silicon nitride can be deposited by using either RF sputtering which is a type of physical vapour deposition (PVD) technique or by chemical vapour deposition (CVD).

In RF sputtering, when the negative charge is applied to a target material, in this case, silicon nitride, forming a plasma, the positive ions, (such as Ar^{+}) are accelerated by an electric field from the plasma region to the negative target and bombard it with high energy causing liberation of some surface atoms from the target. These atoms are then transported into the reacting chamber and condense on the substrate to deposit the material film (Figure 3.12(a)) [29, 30]. The RF frequency is 13.6 MHz, which is high enough to maintain the plasma on. The whole process is performed under vacuum conditions and at a low temperature.

In CVD, the thin film is deposited from a gas phase by a chemical reaction near or onto a heated substrate. The general chemical reaction is as follows:

$$\text{Gaseous reactants} \xrightarrow{T\,℃} \text{Solid material} + \text{Gaseous products}$$

The following two CVD methods can be used to deposit silicon nitride. First, low pressure chemical vapour deposition (LPCVD) which is performed at high temperature. The silicon nitride is deposited from a reaction between dichlorosilane and ammonia at a temperature between 700 °C and 800 °C as follows [11, 31]:

$$3SiCl_2H_2 + 4NH_3 \xrightarrow{\sim 750\,℃} Si_3N_4 + 6HCL + 6H_2$$

Second, plasma enhanced chemical vapour deposition (PECVD) (Figure 3.12(b)) which uses radio frequency to create plasma to transfer energy to the reactant gases, allowing deposition to occur at a lower substrate temperature than in LPCVD. The silicon nitride film in this technique is deposited by reacting silane and ammonia in argon plasma. The reaction is as follows [11, 32]:

$$3SiH_4 + 4NH_3 \xrightarrow{150-400\,℃} Si_3N_4 + 24H_2$$

The optical properties and the thickness of silicon nitride films were measured using a spectroscopic ellipsometry. It uses the change in polarisation of light after reflection from material surface to determine the optical properties of the material. When a linearly polarized beam of light is reflected from a sample surface it becomes elliptically polarized (Figure 3.12(c)). The elliptically reflected light depends on the optical properties of the material and its thickness.

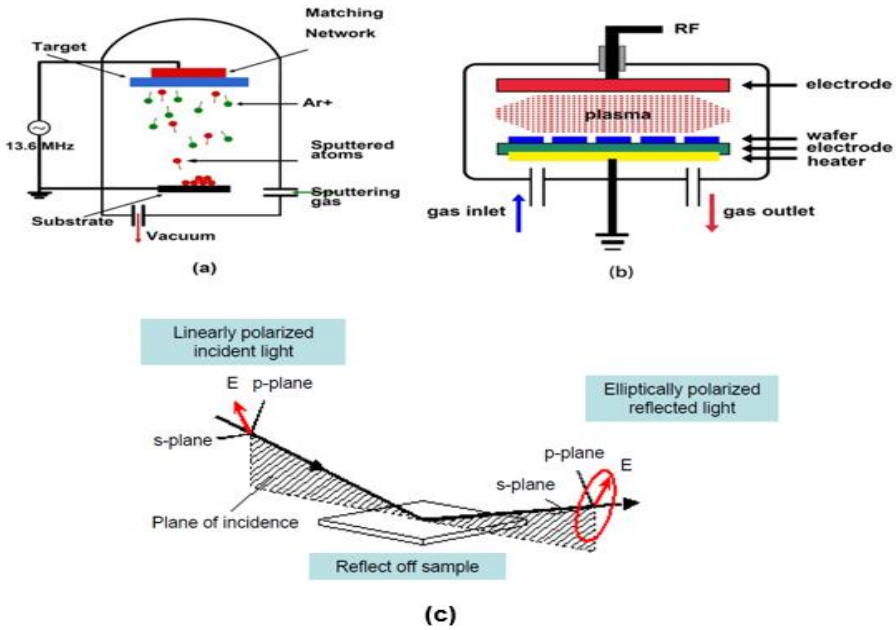

Figure 3.12: Schematic diagram of: (a) RF sputter; (b) PECVD; (c) ellipsometry experiment.

In this work, silicon nitride was used as an etch mask and as a material layer to prevent oxidation of underlying silicon during sidewall oxidation. Later, in this thesis, it was used as a passivation layer during the fabrication of a chemical sensor.

The property of the nitride film plays the most significant role in the reproducibility of the process, and thus the formation of nanowires. This is due to the behaviour of silicon nitride during thermal oxidation. When SiN_x is annealed at high temperature in oxygen ambient, the nitride film starts to convert into silicon dioxide. The amount of SiN_x converted into silicon dioxide strongly depends on the stoichiometry of the film.

A series of experiments were performed to study and optimise the properties of silicon nitride films to be used in this fabrication process.

The silicon nitride films were deposited using different techniques:

1- PECVD (externally deposited)
2- Oxford Instruments Plasmalab System 400 RF magnetron sputter with different gases pure N_2, mixed Ar/N_2, pure Ar.
3- Kurt J. Lesker PVD75 in pure N_2 and Ar.(data obtained by using this method is presented in appendix A)

3.4.1.1 Deposition rate and etch rate

Table 3.2 shows that the deposition rate of sputtered silicon nitride increases with argon flow rate, while etch rate in BHF increases with increase of nitrogen content in the films. Nitride films deposited with PECVD and RF sputter have high selectivity compared with silicon dioxide. The etch rate of RF sputtered silicon nitride in BHF decreases with increasing deposition temperature. For example, the etch rate of silicon nitride deposited in pure N_2 ambient, on hydrophobic silicon substrate, decreases four times when the deposition temperature changes from 90 °C to 250 °C. Interestingly, the etch rate of RF sputtered silicon nitride deposited on thermal silicon dioxide in BHF was observed in this research to be three to four times faster than the etch rate of silicon nitride deposited on a silicon substrate. The results in Table 3.2 are based on at least ten data points each.

3.4.1.2 Optical properties of silicon nitride

The optical properties of silicon nitride films were analysed using spectroscopic ellipsometry. The average refractive indexes of the films at wavelength 633 nm are illustrated in Table 3.3. The refractive index reduces with increasing nitrogen ratio, the deposition in pure N_2 refractive index being about 1.89, which corresponds to Si_3N_4 as it is $n = 1.35 + 0.74\frac{[Si]}{[N]}$ [33]. The refractive index of PECVD also gives a stoichiometric silicon nitride. Each data point in Table 3.3 represents the average of ten measurements, with each measurement taken at three different locations across each sample.

Table 3.2: Silicon nitride deposition conditions, deposition rates, thicknesses and etch rates in BHF and boiling phosphoric acid (H_3PO_4).

Technique	T(°C)/P(W)/P (mtorr)	Deposition rate (nm/min)	Film thickness (nm)	Etch rate BHF (nm/min)	Etch rate H_3PO_4 158-170 °C (nm/min)
PECVD SiH_4 flow: 20 sccm NH_3 flow: 30 sccm	-/30/1000	-	60	56	>20
RF sputter N_2, flow 50 sccm	90/150/10	2.6	40-60	33	>20
RF sputter Ar/N_2, flow 50/15 sccm	90/150/10	3.1	40-60	26	>20
RF sputter Ar, flow 50 sccm	90/150/10	4.2	40-60	8	<20

Table 3.3: The refractive indexes of silicon nitride films.

	PECVD	RF sputter pure N_2	RF sputter mixed N_2/Ar	RF sputter pure Ar
Average refractive index	1.94	1.9	2.04	2.37

For simplicity, SiNx deposited in pure Ar will be referred to as $\frac{[Si]}{[N]} = 1.38$, mixed Ar/N_2 as $\frac{[Si]}{[N]} = 0.94$, and pure N_2 as $\frac{[Si]}{[N]} = 0.75$ while the PECVD nitride as PECVD 0.8.

3.4.1.3 Film behaviour during thermal oxidation

As explained in section 3.3.2 (silicon nitride mask) the reproducibility of nanowire formation depends on the property of silicon nitride during thermal oxidation. A nitride film with low oxidation rate is required to be used as a mask. To investigate the film robustness to thermal oxidation, the silicon nitride films (in Tables 3.2 & 3.3) were annealed in oxygen at 930 °C for 35 min. The oxide thickness on the silicon substrate was

21 nm. The optical properties of oxidised nitride films were analysed using optical ellipsometry. The structures of oxidised films were more complex in comparison with the as-deposited silicon nitride because they contain three layers SiO_2/ SiO_xN_y/ SiN_x/ Si and there is no clear distinct phase between SiN_x and SiO_xN_y where the refractive index changes with depth. In order to study this structure and the distribution of oxynitride inside the film, two different fitting models were used in this research. The first model considered the oxidised silicon nitride, SiN_x / SiO_xN_y, as a single layer with an equivalent refractive index between 1.45-1.9 and the change of effective refractive index measured with depth after performing many etching steps. The second model considered the oxidised nitride film as a multilayer structure of SiO2 /SiO_xN_y /SiN_x, the refractive index of SiN_x layer was fixed to the value measured before annealing while fitting parameters were used to measure the effective oxide thickness and its effective refractive index.

First, the single oxynitride layer model: the oxidised film was considered as a single uniform layer. The effective refractive index of this layer n_{eff} was measured, and then the relative volume fraction of oxide f_{SiO_2} and nitride $f_{Si_xN_y}$ were approximately estimated in the film from the following equations [34]:

$$f_{SiO_2}\frac{n_{SiO_2}^2 - n_{eff}^2}{n_{SiO_2}^2 + 2n_{eff}^2} + f_{Si_xN_y}\frac{n_{Si_xN_y}^2 - n_{eff}^2}{n_{Si_xN_y}^2 + 2n_{eff}^2} = 0 \qquad (3.6.\text{a})$$

$$f_{SiO_2} + f_{Si_xN_y} = 1 \qquad (3.6.\text{b})$$

where $n_{Si_xN_y}$ and n_{SiO_2} are the measured effective refractive index of the as-deposited nitride film and the refractive index of silicon dioxide respectively.

After defining n_{eff}, f_{SiO_2} and $f_{Si_xN_y}$ of the whole film, an etching step was performed using RIE in pure Ar to etch about 2.5 nm from the oxidised film then the new n_{eff}, f_{SiO_2} and $f_{Si_xN_y}$ were estimated in the same way. This procedure was repeated a number of times until the deposited refractive index was recovered. Afterwards, the oxynitride depths were estimated for each film.

The silicon oxynitride easily reacts with the ambient air and forms a thin layer of native oxide, which may affect the ellipsometry results. Therefore, in order to minimize this effect, the ellipsometry measurements were immediately performed after each etching step.

The results are summarised in Table 3.4.

As illustrated in Table 3.4 all nitride films were affected by thermal oxidation and that can be clearly shown by the change of refractive index. The silicon-rich film with $\frac{[Si]}{[N]} = 1.38$ has the highest refractive index, after thermal oxidation, while the nitrogen-rich film with

$\frac{[Si]}{[N]} = 0.75$ has a refractive index value close to the refractive index of silicon oxide. However, all films have almost the same relative volume fraction of oxide and nitride. After each etching step, the refractive indexes of all films increased and so did the ratio of nitride in the films. However, while the refractive index of $\frac{[Si]}{[N]} = 0.75$ was recovered after the 3rd etching step the refractive index of $\frac{[Si]}{[N]} = 1.35$ started to recover after the 6th step of etching. Two results can be understood from the film profile. First, silicon-rich silicon nitride exhibits the thickest oxynitride after oxidation. Second, even though the nitrogen-rich film has the thinnest oxynitride film, most of this oxynitride volume is silicon dioxide. The change in refractive index of each film with depth and the consumed silicon nitride during thermal oxidation are shown in Table 3.4.

The change in the refractive index with depth of the film shows that the oxidized silicon nitride has a non-homogeneous structure. This could cause inaccuracies in determining the optical properties and the composition of the structure. However, accuracy improves when the silicon nitride layer starts to expose. Therefore, this model can be appropriate for estimating the thickness of the oxidised silicon nitride for different films. Conversely, it cannot predict the nature of each layer. The error in evaluating the true thickness of silicon nitride after the removal of oxynitride layer is expected to be $\pm 5\%$. This error occurs due to the excess etching of silicon nitride during the ion milling etching step, as described in section 3.4.1.4.

It is worth mentioning, that all ellipsometry data measurements of refractive indexes for films less than 35 nm were excluded as a large variation in the refractive indexes were observed. This could be in agreement with what was documented, that a very thin film has different optical properties in comparison with bulk [34, 35].

Table 3.4: Films compositions and refractive indexes of oxidised silicon nitride as a function of depth (each number represents an average of two measurements).

		Pure Ar $\frac{[Si]}{[N]} = 1.38$	Mixed Ar/N2 $\frac{[Si]}{[N]} = 0.94$	Pure N2 $\frac{[Si]}{[N]} = 0.75$	PECVD 0.8
After thermal oxidation t_{ox}=21nm	n_{eff}	1.67	1.57	1.55	1.61
	Composition	73.9%SiO_2 + 26.1%Si_xN_y	78.4%SiO_2 + 21.6%Si_xN_y	76.7%SiO_2 + 23.2%Si_xN_y	86%SiO_2 + 14%Si_xN_y
After 1st etching	n_{eff}	1.71	1.63	1.63	1.67
	Composition	65.3% SiO_2 + 34.7% Si_xN_y	68% SiO_2 + 32% Si_xN_y	58.9% SiO_2 + 41.1% Si_xN_y	53.9% SiO_2 + 46.1% Si_xN_y
After 2nd etching	n_{eff}	1.75	1.71	1.71	1.73
	Composition	65.1% SiO_2 + 34.9% Si_xN_y	54.5% SiO_2 + 45.5% Si_xN_y	41.3% SiO_2 + 58.7% Si_xN_y	41.8% SiO_2 + 58.2% Si_xN_y
After 3rd etching	n_{eff}	1.81	1.85	1.85	1.87
	Composition	58.7% SiO_2 + 41.3% Si_xN_y	31.3% SiO_2 + 68.7% Si_xN_y	10.9% SiO_2 + 89.1% Si_xN_y	14.0% SiO_2 + 86.0% Si_xN_y
After 4th etching	n_{eff}	1.85	2.0	1.92	1.94
	Composition	45.5% SiO_2 + 45.5% Si_xN_y	6.7% SiO_2 + 93.3% Si_xN_y	0% SiO_2 + 100% Si_xN_y	0% SiO_2 + 100% Si_xN_y
After 5th etching	n_{eff}	2.01	1.92	1.81	1.9
	Composition	34.6% SiO_2 + 65.4% Si_xN_y	19.8% SiO_2 + 80.2% Si_xN_y	19.6% SiO_2 + 80.4% Si_xN_y	8.0% SiO_2 + 92.0% Si_xN_y
After 6th etching	n_{eff}	2.17	1.89	1.85	1.85
	Composition	21.1% SiO_2 + 78.9% Si_xN_y	24.8% SiO_2 + 75.2% Si_xN_y	10.9% SiO_2 + 89.1% Si_xN_y	17.9% SiO_2 + 82.1% Si_xN_y

Second, SiO_2 / SiO_xN_y / SiN_x / Si model: the single model was able to estimate the oxynitride profile during thermal oxidation. The gradual increase of refractive index with depth may predict that the oxidation occurs on two basic steps, first the oxidant species diffuses into a few nanometers inside the nitride film forming an oxynitride layer then the top layer of oxynitride starts to convert into silicon oxide. Therefore, the oxidation can lead to a formation of three layers: very thin silicon dioxide on top and silicon nitride on the bottom and intermediate oxynitride layer. The SiO_2 / SiO_xN_y / SiN_x / Si model was used to determine the thickness of each layer. Then, the results were compared with oxide thickness grown on silicon substrate. The analysed data are shown in Table 3.5. The data shows that the silicon-rich film with $\frac{[Si]}{[N]} = 1.35$ has the thinnest oxide on top where the oxidation rate was about 75 times lower than the oxidation rate of silicon and approximately three times slower than the oxidation rate of the nitrogen-rich film with $\frac{[Si]}{[N]} = 0.75$. However, the oxynitride thickness on a silicon-rich nitride is higher than 100% of the thickness of oxide grown on a silicon substrate, while it was about 25% of the thickness on the $\frac{[Si]}{[N]} = 0.75$ film as it shown in Table 3.5.

It is noteworthy that the $\frac{SiO_2 \ on \ SiN_x}{SiO_2 \ on \ bulk \ Si}$ ratio is small thus the SiO_2 / SiO_xN_y / SiN_x / Si model can be reduced and represented by two layer structures model, SiOxNy / SiN_x / Si, at thinner oxide thicknesses.

In the literature, several models have been suggested to describe the oxidation mechanism of silicon nitride. One study suggests that the top layer of silicon nitride is converted into silicon dioxide. Hence, the reaction of this silicon dioxide with the silicon nitride layer will lead to the formation of an intermediate oxynitride layer [36]. Another study proposes that the oxynitride layer is formed by the transport of oxidant species across the silicon dioxide layer [37], whereas a further study suggests that the oxynitride is formed first, followed by the formation of the oxide due to the oxidation of oxynitride [38].

The oxidation kinetics of silicon nitride is generally described by a parabolic equation. The consumed thickness of silicon nitride during oxidation x as a function of time t is then given by [37]:

$$x^2 = Bt \tag{3.7}$$

where B is a parabolic constant which is given by [37]:

$$B = B_0 e^{(-E_a/RT)} \tag{3.8}$$

where E_a is the activation energy and R is the gas constant. Equation 3.7 is similar to the Deal-Grove equation that describes the oxidation of silicon. However, the parabolic constant is much higher in silicon nitride than compared to silicon. For example, the

activation energy of stoichiometric silicon nitride has been reported to be three times higher than that of silicon [37]. It has also been reported that silicon rich silicon nitride has a lower activation energy compared with nitrogen rich silicon nitride [39]. This can explain the higher oxidation rate of silicon-rich silicon nitride compared with the nitrogen-rich silicon nitride reported in this study. These results are in general agreement with other studies, which have reported that nitrogen-rich silicon nitride enhances the film resistance to thermal oxidation compared with silicon-rich silicon nitride [38, 40].

However, the oxidation rate of silicon nitride reported in this study is higher than that of many reported studies [37, 38]. Further experimental measurements using techniques such as XPS and FTIR need to be undertaken to confirm the ellipsometry results. In addition, it is important to fit the experimental data to a theoretical model.

Table 3.5: The oxynitride and oxide ratios on oxidised silicon nitride to the silicon dioxide thickness on bare silicon.

	Pure Ar $\frac{[Si]}{[N]} = 1.38$	Mixed Ar/N_2 $\frac{[Si]}{[N]} = 0.94$	Pure N_2 $\frac{[Si]}{[N]} = 0.75$	PECVD 0.8
Average $\frac{SiO_2 \text{ on } SiN_x}{SiO_2 \text{ on bulk Si}}$ %	1.3	2.3	3.6	3.2
Average $\frac{SiN_xO_y \text{ on } SiN_x}{SiO_2 \text{ on bulk Si}}$ %	104	57	23	22

3.4.1.4 Etching of thermally oxidised silicon nitride

As described in the previous section, the oxidation of silicon nitride leads to the formation of a three film structure SiO_2 / SiN_xO_y / SiN_x/Si. Etching the film with one etchant such as boiling phosphoric acid could be inadequate, especially for applications that require etching selectivity over certain materials such as silicon dioxide. Therefore, in this current research, several etchants based on wet and dry etching were used to study the etching behaviour of thermally oxidised nitride films.

Wet etching

a- Etching using BHF or diluted HF: The etch behaviour was observed to follow the material type; it started with an etch rate approximately equal to the etch rate of silicon dioxide in BHF, then the etch rate dropped when the oxynitride film was exposed and more drops in etch rate could be observed when it reached the silicon nitride film. The etch behaviour was detected as a change in the etched thicknesses in BHF as a function of time. The results of etched thickness in BHF for different oxidised nitride films and silicon dioxide with time are shown in Figure 3.13, each data point is the average measurements of three samples.

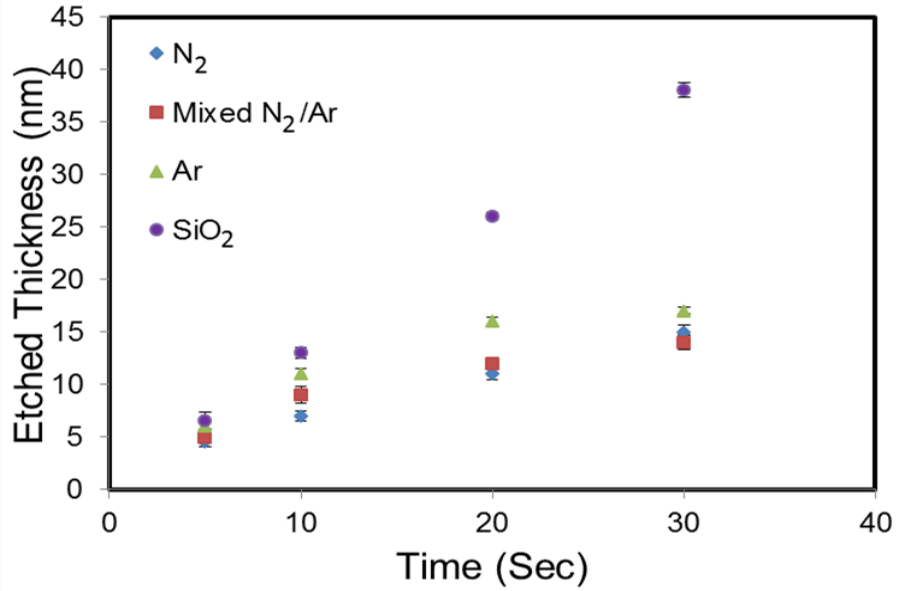

Figure 3.13: The etch behaviour of oxidised silicon nitride and silicon dioxide in BHF (N_2, mixed N_2/Ar and Ar are the process gases). (N.B. Error bars are present in each data point, although some are not visible).

b- Etching using boiling H_3PO_4: The etch behaviour began with a very low etch rate and then started to increase exponentially until it reached the silicon nitride layer when the etch rate started to be constant. The etch rate of oxidised silicon nitride films after the removal of oxynitride in H_3PO_4 is illustrated in Table 3.6. Each data point is the average measurements of three samples.

Table 3.6: Etch rates of silicon nitride films in boiling H_3PO_4 after the removal of oxynitride layers.

	Pure Ar $\frac{[Si]}{[N]} = 1.38$	Mixed Ar/N_2 $\frac{[Si]}{[N]} = 0.94$	Pure N_2 $\frac{[Si]}{[N]} = 0.75$	PECVD 0.8
Average etch rate in H_3PO_4 (nm/ min)	2.3	2.6	2.9	3.9

c- Two wet etching steps: The first BHF etching step aimed to remove the SiO_2 and SiN_xO_y layer, which was followed by H_3PO_4 to etch the silicon nitride layer. Figure 3.14 shows etch behaviour of oxidised silicon nitride and silicon dioxide after etching in boiling H_3PO_4 followed 4 sec in BHF. Each data point in Figure 3.14 has an average of five data points.

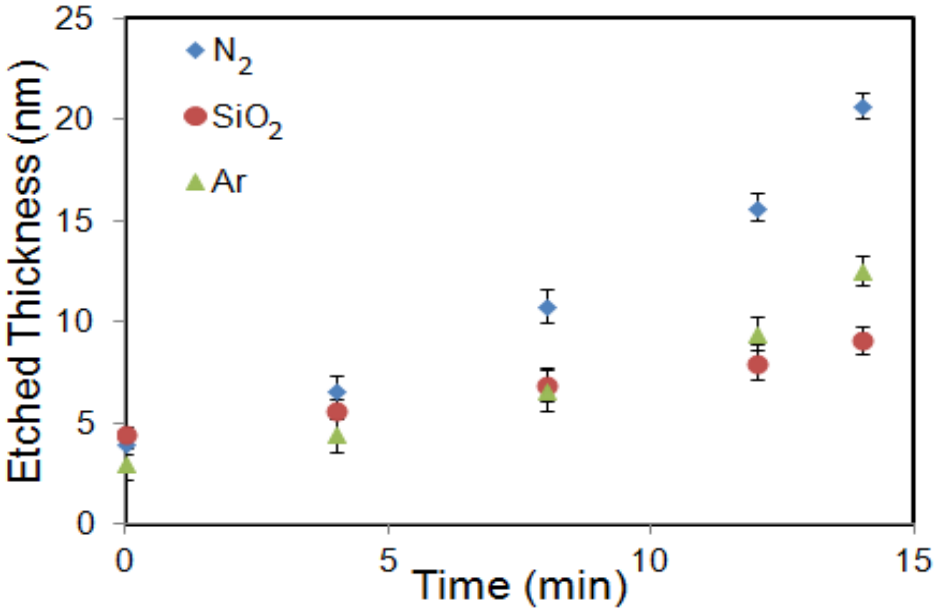

Figure 3.14: The etch behaviour of oxidised silicon nitride and silicon dioxide after etching in boiling H_3PO_4 followed 4 sec BHF (N_2 and Ar are the process gases).

Dry etching:

Dry etching by using RIE in Argon or ion milling with argon. Ion milling is a physical etching process which can etch all materials by bombarding the surface of the sample using argon ions at low pressure. The selectivity of the process is low. The etch behaviour of different oxidised nitride films in addition to silicon dioxide in ion milling with argon, at DC =530 V, P= 12 mtorr, is presented in Figure 3.15. The etch rate is approximately the same for all materials with relatively higher etch rate for silicon dioxide compared to other nitride films.

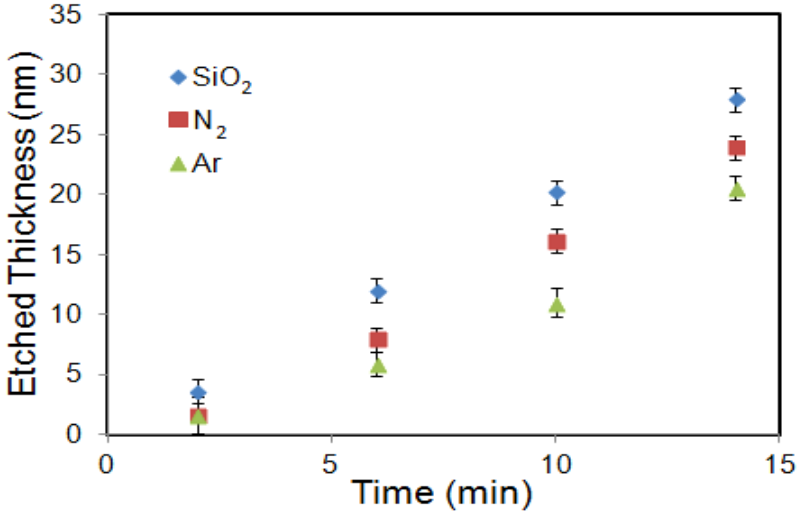

Figure 3.15: The etch behaviour of oxidised silicon nitride and silicon dioxide in ion milling with argon at DC=530 V, P=12 mtorr (each data point is an average of five points).

Dry etching followed by wet etching

The silicon dioxide and oxynitride mask were removed first using ion milling then followed by boiling phosphoric acid (H_3PO_4) etching step to remove the silicon nitride. As this etching method is a controllable method, it was selected to be used for the removal of the oxidised silicon nitride mask.

3.4.1.5 Silicon Nitride Selection for nanowire process

In the previous sections the characteristics of different types of silicon nitride films were investigated. Different film behaviours during thermal oxidation were observed and consequently different etching behaviours. Now, the following question arises: which of these films is the most suitable to be used as a mask in the fabrication process of nanowires, as described previously? Another question is what is the maximum and minimum thickness of SiNx that can be used for masking?

The oxynitride thickness and the etching selectivity of the silicon nitride over silicon dioxide are key parameters which determine the maximum thickness of the nitride mask. This is due to the fact that during the removal of the nitride mask the silicon dioxide at the sidewall is removed as well. The maximum thickness of nitride mask is given by:

$$t_{max} = S_{SiN_x/SiO_2}(t_{ox} - t_R) \tag{3.9}$$

where S_{SiN_x/SiO_2} is the etching selectivity of silicon nitride after the removal of oxynitride over silicon dioxide in the phosphoric acid (H_3PO_4) used etchant in the current experiments; t_{ox} is the maximum oxide thickness that can be removed from the sidewall without causing a failure in the process. In fact, $t_{ox} = t_{tot} - 3$, where t_{tot} is the oxide thickness grown on sidewall oxide and 3 nm represents the oxide thickness at the sidewall required to form the nanowires; t_R is the thickness of oxide consumed during the etching of oxynitride and oxide on the nitride film. The S_{SiN_x/SiO_2} of different films and the t_R are shown in Table 3.7.

It should be clarified here, that two etching steps were used to remove the whole oxidised films, first ion milling, where about 25% of the total silicon dioxide was removed during this step for all films, followed by boiling phosphoric acid. The maximum thickness of the silicon nitride mask for each type of silicon nitride material is shown in Figure 3.16. This may confirm that nitrogen-rich silicon nitride is the most suitable to be used as a mask in nanowire fabrication.

Table 3.7: Etch selectivity of oxidised silicon nitride over silicon dioxide in boiling H_3PO_4 and oxide thickness ratios consumed during the removal of oxide and oxynitride layers (each data point is an average of five points).

Silicon nitride film	Etching Selectivity over SiO_2	(t_R) the average oxide consumption during SiO_2/SiOxNy removal
Pure Ar $\frac{[Si]}{[N]} = 1.38$	3.3-3.8	$0.65t_{tot}$
Mixed Ar/N_2 $\frac{[Si]}{[N]} = 0.94$	3.5-4.2	$0.35t_{tot}$
Pure N_2 $\frac{[Si]}{[N]} = 0.75$	4.1-5.3	$0.25t_{tot}$
PECVD 0.8	5.5-7	$0.2t_{tot}$

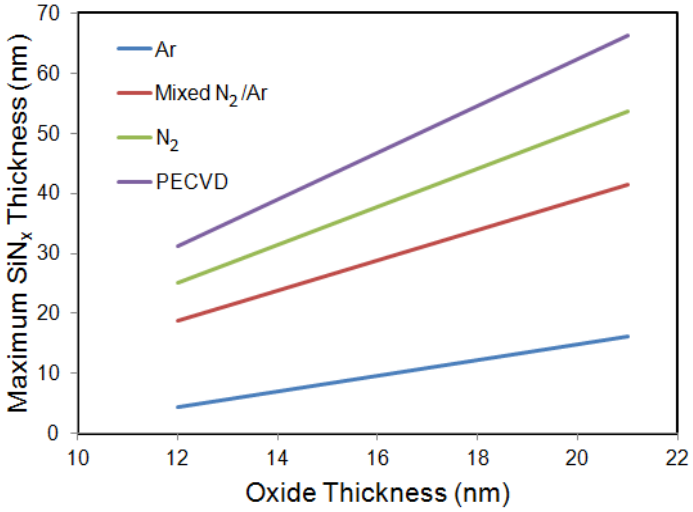

Figure 3.16: The maximum thickness of silicon nitride mask for different types of silicon nitride films as a function of sidewall oxide.

To further answer the research question, related to the minimum thickness of silicon nitride mask that can be used as an oxidation mask in this fabrication process of nanowires, depends on the oxidation rate of the nitride film. Based on the results illustrated in Tables 3.5 & 6, 4 nm of nitrogen-rich silicon nitride can protect the silicon film underneath from oxidation. However, due to the directional nature of the sputtered material, voids can be formed at the corners after the deposition of silicon nitride. For example, as shown in Figure 3.17, a discontinuity and curvature at the corner after the 1st anisotropic wet step were observed when 5 nm of sputtered nitride acted as an etching mask. Therefore, a thicker nitride film is required to form continued structure. In this work, a 25 nm thick silicon

nitride was sufficient to serve as a mask layer for the 1st ODE etching and thermal oxidation steps. However, a thinner mask thickness can be used when the deposition pressure increases due to isotropic deposition at higher pressure.

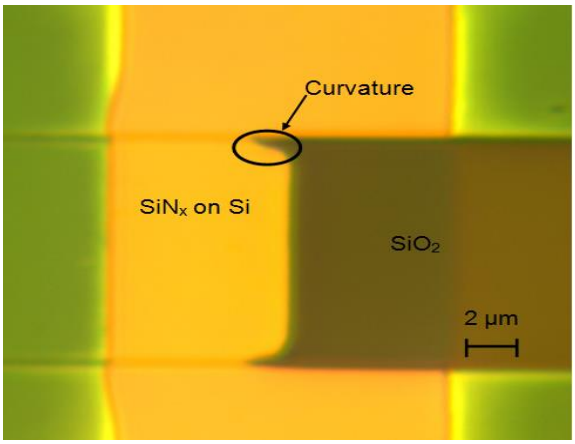

Figure 3.17: Optical microscopy image shows that an insufficient nitride mask causes a change of etch direction during ODE etching which is seen as curvature and discontinues at the corners.

3.4.2 Characteristics of thermal oxidation

3.4.2.1 RTP vs Furnace

A thermal oxidation step was used to oxidise the exposed <111> plane which worked as a mask for the 2nd anisotropic etching as shown in figure. Normally, this step is critical to realise the nanowires. Lamp based RTP radiation or a furnace with resistive heating are the methods that can be used to grow sidewall oxide. The Jet First 200 RTP system was used to perform thermal radiation processing, which is achieved with a set of 18 halogen lamps on top of the process chamber which emit infrared radiation towards a substrate wafer. The substrate temperature is measured using an optical pyrometer mounted at the bottom of the chamber which can only view the wafer. The pyrometer receives the signals from the backside of the wafer and converts the optical radiations into electrical signals and then to temperature measurements. A general view of the RTP configuration is shown in Figure 3.18(a). Meanwhile the furnace oxidation process was performed using a furnace with a resistance heater. The schematic of the thermal oxidation furnace is shown in Figure 3.18(b).

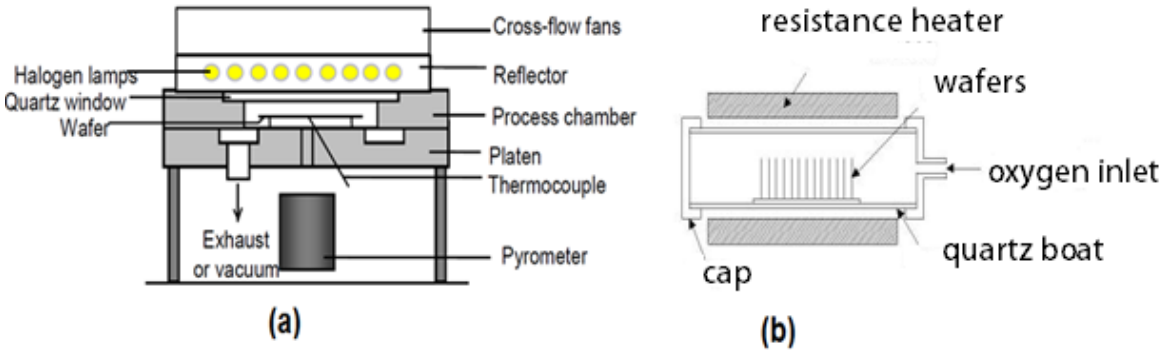

Figure 3.18: Schematics of: (a) RTP configuration; (b) thermal oxidation furnace.

The measurements indicate differences in characteristics between a multilayer structure of SOI and a single Si structure when they are oxidised using lamp based RTP radiation. If SOI and Si samples are oxidised at apparently the same temperature and for the same period of time the oxide on top of SOI sample will be thinner than the one on single Si sample.

Experiments

In order to characterise the effect of the presence of a SiO_2 layer on the thermal behaviour of SOI , 1cm x 1cm bulk-Si and SOI sets of samples were first cleaned in H_2O_2+H_2SO_4 solution, which was followed by rinsing in DI water. Then the samples were immersed in BHF for 3 sec to remove native oxide. After the cleaning step, samples were placed in Jet First 200 RTP and oxidised under different conditions. The oxidation was performed at different pyrometer setting temperatures and time periods. Two sets of samples were oxidised at pyrometer setting temperatures of 930 °C and 950 °C for 330 sec and another set for 11 min at 1000 °C. For comparison of radiative with conductive heat transfer, another set of samples were oxidised in furnace, where both SOI and bulk Si samples were placed together in resistive heating furnace for 45 min at 1000 °C in pure oxygen. The oxide thicknesses were measured using optical ellipsometry, and then the results were confirmed by using commercial non-contact AFM mode. The oxidation conditions, samples specifications and ellipsometry thicknesses measurements are summarised in Table 3.8. Importantly, the ellipsometry measurements of oxide thickness show, that all SOI samples which were oxidised in RTP had a thinner oxide thickness compared with the bulk Si. The estimated thickness of oxide on the measured SOI was between 18-21% less than in bulk. The results were confirmed using AFM which gives similar results to ellipsometry. There was a 2 % variation between both measurement techniques. The AFM profiles for the set of the samples annealed for 11 min at 100 °C in RTP is presented in Table 3.9. Moreover, it was observed that the extent of reduction in oxide thickness is higher in the samples with a thinner top silicon film compared to a thicker one.

In contrast to lamp based RTP radiation, the bulk and SOI samples annealed in a resistive heating furnace have almost the same oxide thickness. The thickness of oxide obtained on SOI after 45 min oxidation at 1000 °C is about 4% thicker than that of the bulk Si.

Table 3.8: Ellipsometry thicknesses results for SOI and Bulk Si samples. (Each number represents an average of two measurements).

Oxidation method	Pyrometer set point (°C)	Time (min: sec)	SOI specification	SOI oxide thickness (nm)	Bulk oxide thickness (nm)
RTP	930	5: 30	T_{Si}=155nm, T_{SiO2}=145nm	13.9	17.6
RTP	950	5: 30	T_{Si}=155nm, T_{SiO2}=145nm	16.8	20.9
RTP	1000	11: 00	T_{Si}=155nm, T_{SiO2}=145nm	39.3	48.7
			T_{Si} = 48nm, T_{SiO2} = 145nm	34.5	
Furnace	1000	45: 00	T_{Si} = 155nm, T_{SiO2} = 145nm	45.6	43.0

Table 3.9: AFM thicknesses results for SOI and Bulk Si samples (RTP 1000 °C, 11 min). (Each number represents an average of two measurements).

	Bulk Si	SOI 155	SOI 48
Oxide Thickness	49.1	38.2	34.7

Discussion

Several experimental studies reported different characteristics between bulk Si and SOI during thermal radiation processing [41-43]. These studies particularly aimed to investigate dopant distribution in thin SOI samples. The researchers observed a reduction in dopant diffusion in SOI compared to bulk Si. Their explanations suggest that the presence of the Si/SiO_2 interface plays the main role during dopant distribution. While one study considers that the quality of the Si/SiO_2 interface can reduce the activation of dopants in SOI [43], another study explains that the presence of Si/SiO_2 can increase the optical reflectivity of the SOI wafer and consequently reduces the temperature of the wafer [41]. Previously, Wong et al. proposed a numerical model to calculate the reflectivity and emissivity of multilayer thin film structures during thermal radiation processing [44]. They included effects such as reflection mechanisms, electromagnetic interference inside the structure and film thickness. They concluded that optical properties of the multilayer structures are determined by these microscale radiative effects [44].

The microscale radiative effect on the optical properties of the multilayer films is the most possible explanation of the observed reduction of oxide thickness on SOI wafers compared with bulk Si wafer. This can be explained briefly as follows [41, 44]:

In the case of a bulk Si wafer, when electromagnetic radiation arrives at the surface of the wafer some of the radiation is reflected at the surface and the remaining part is transmitted through the silicon as shown in the schematic, as shown in Figure 3.19(a). Since the

thickness of the wafer is ~700 µm, which can be considered to be optically thick, where all transmitted radiation is absorbed in a few tens of microns, there is no reflection from the back surface of the wafer. Therefore, the reflectivity depends only on the optical properties of silicon. For a silicon substrate in the infrared regime n=3.5-0.05i and about 30% of radiation can be reflected from the surface of the silicon substrate when radiation is normal to the surface.

In the case of a multilayer Si-SiO_2-Si structure, the radiation is partially reflected from the surface of silicon while the remaining part transmits into the silicon layer to face another reflection at the Si-SiO_2 interface and transmission into the SiO_2 layer to be partially reflected at the next SiO_2-Si interface and the remaining part absorbed into the thick substrate. So each radiation is subject to partial reflection and transmission at each interface (Figure 3.19(b)). Tracing all the reflections of each ray at all interfaces leads to the net reflectivity that is a sum of all reflected rays at the front surface of the wafer. As the thickness of the film is smaller than the wavelength, film thickness interference arises and the constructive and destructive interference between the rays can affect the net reflectivity. Therefore, the reflectivity of the multilayer film depends not only on the optical properties of the film but it also depends on wavelength and film thickness.

Thus the reflectivity of SOI and bulk Si are not the same and they reach different temperatures when they are heated by infrared radiation source.

The above experiments, which have been performed on SOI and bulk Si using radiant and resistive heating sources, conclude that the difference in thermal behaviour should be taken into account when thermal processes such as doping and oxidation are performed on SOI. Thus, in order to realise nanowire with high reproducibility, the oxide thickness on top of SOI should be estimated when RTP is used to oxidise the sidewall.

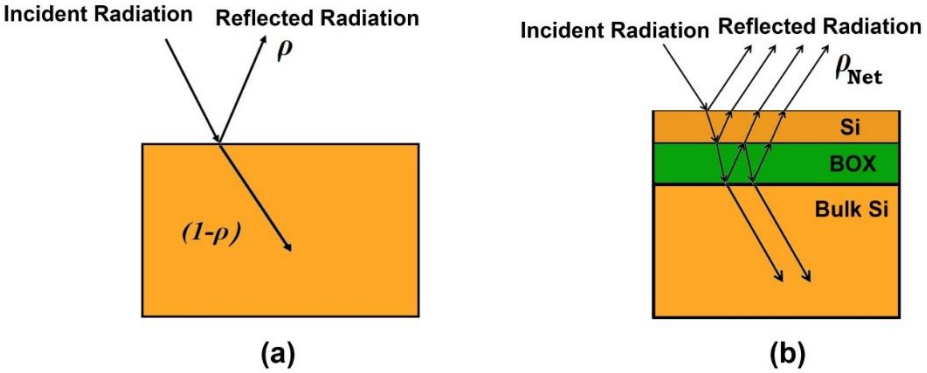

Figure 3.19: Schematic of incident and reflected radiations through (a) bulk Si wafer; (b) SOI wafer.

3.4.2.2 The robustness of sidewall oxide

Sidewall oxide was used as a sacrificial layer to protect the <111> plane during the formation of the 2nd side of the nanowire. The total oxide thickness on the sidewall must take account of the thickness consumed during the silicon nitride removal step, as mentioned earlier. Moreover, calculating the total oxide thickness should take into account the nonuniformity of oxide thickness due to the increase in compressive stress at the edges and the corners compared to the flat surfaces. As observed in previous research, the thickness at the edges could be 30% thinner compared to the flat surface, with the silicon oxidised at a temperature lower than 1000 °C [25]. This percentage can be reduced, if the temperature is higher than 1000 °C due to the relief of stress [25, 45].
During the fabrication process, this effect could be observed after the 2nd TMAH etching step (TMAH etches thermal SiO_2 very slowly) as breaks occurring along the nanowires. For example, discontinuities in nanowires, especially at the corners, were observed after the 2nd TMAH step, as shown in Figure 3.20. Since a TEM image to measure the oxide thickness at sidewall was not available, the minimum thickness, required to mask silicon efficiently before the 2nd anisotropic wet etching step, was alternatively estimated.

To further address the research questions, silicon reference samples were used to estimate the minimum mask thickness. These reference samples were put through the same process steps, section 3.3.1.1 to section 3.3.1.6, along with the actual nanowires samples. In other words, the consumed oxide thicknesses on both samples were expected to be equal after the 2nd anisotropic wet etching step. The remained thickness on the silicon reference sample, which represents the thickness of the mask, was measured by using optical ellipsometry.

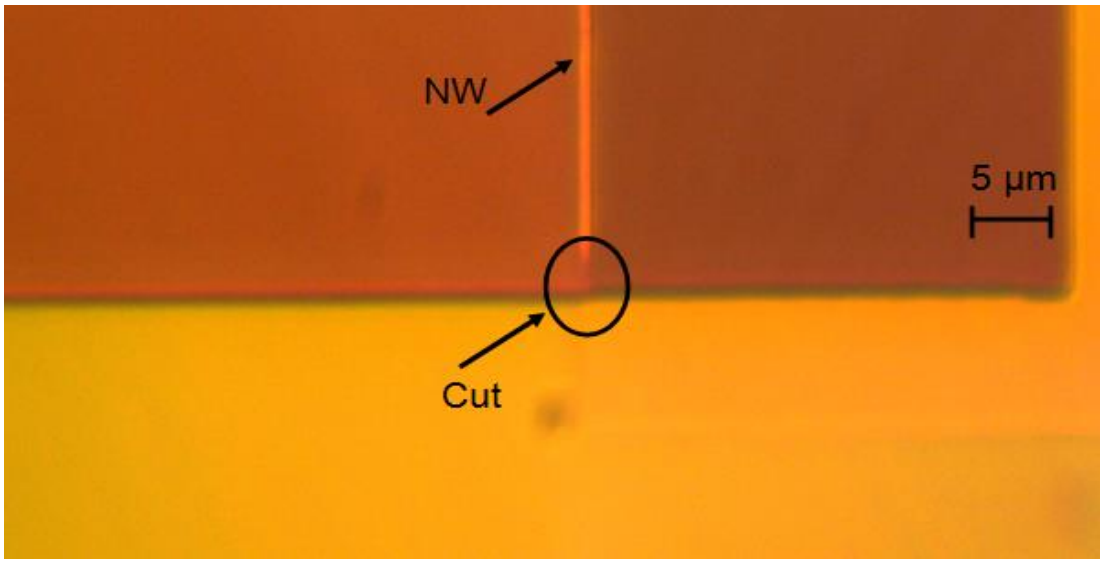

Figure 3.20: Optical microscopic image shows a cut at the corner of nanowire.

This procedure was repeated with different sets of samples while changing the time immersed in H_3PO_4. The ellipsometry results showed that the samples with oxide less than 2.9 nm had breaks along the nanowires or no nanowires were formed, while nanowires were successfully formed when the oxide was thicker than 2.9 nm.
However, this value of mask thickness was measured on <100> silicon which has a thinner oxide compared to the <111> plane where the actual mask lies. However, if the reduction of oxide thickness at the edges and corners was taken into consideration then the estimated value on the <100> edge would be accepted as the minimum oxide thickness that is required to act as a mask for the 2nd anisotropic wet etching.

3.4.3 Characteristics of TMAH and KOH for nanowire fabrication

Anisotropic wet etching of silicon using TMAH and KOH has been employed to realise many silicon nanostructures. Both etchants have similar anisotropic etching characteristics. KOH has excellent anisotropic properties and high etching selectivity over <111> and it can obtain smoother sidewall, while TMAH etchant is nontoxic and it does not contain alkaline contaminants. Moreover, it offers high etch selectivity against silicon dioxide in comparison with KOH. For both etchants the etch rate, roughness and undercut strongly depend on the temperature and concentration of the solution [46-49]. For example, the etch rate decreases with an increase in concentration and slows down again at very low concentration. The surface roughness is larger at low concentration and increases at a temperature higher than 70 °C. A relatively high temperature of TMAH (>75 °C) can produce hillocks on the etched surface [48]. The chemistry behind that is not fully understood. The etching process can be explained by a generally accepted model, as follows [48-50]: ions such as OH^-, K^+ and TMA^+, in addition to water, are absorbed on the silicon surface. Silicon is oxidised, then the reaction products are desorbed and diffused from the silicon surface. The main reacted ions on the silicon surface are OH^- and water while $Si(OH)_4$ and H_2 are the main reaction products. Thus, the overall reaction when the water and hydroxide ions participate in the etching reaction is given as follows [49]:

$$Si + 2H_2O + 2OH^- \rightarrow Si(OH)_4 + H_2$$

As shown in the reaction, the etch rate depends on the product of $[H_2O]$ and $[OH^-]$. However, the TMA^+ and K^+ can also take part in the etching process, as their absorption in large amounts at the surface can lead to a reduction in OH^- at the surface; these OH^- are necessary in the oxidation step. Moreover, at high concentration a large amount of water is consumed during the dissociation of KOH and TMAH. These processes are the possible reasons why a decrease of etching occurs at high concentration.

The surface roughness depends equally on the speed of oxidation and desorption steps. If the oxidation step is faster than the desorption step, and it happens at low concentration and

at high temperature, the reaction products (such as hydrogen) stay at the surface and act as a mask against the hydroxide ions, preventing them from reacting with silicon surface.

Adding IPA to the solution was reported to improve the quality of the etched surface. IPA particles can be absorbed on the surface and lead to a reduction in silicon oxidation rate. In other words, adding sufficient IPA to the solution provides an equilibrium in desorption rate with oxidation rate and prevents the reaction products from staying at the surface. However, IPA slows the etch rate down, because it restricts the access of silicon to hydroxide ions [47, 51].

In spite of extensive studies related to the etching of silicon in anisotropic wet etching, controlling the etch profile and reproducibility are still quite challenging tasks in nanostructure fabrication. Therefore, the selection of an etchant, concentration and temperature was dictated by this research desire to achieve a reliable process. The required process should be reproducible, compatible with IC manufacturing and the obtained nanostructure should have a controllable profile with low undercut, smooth surface and accurate alignments.

As a consequence, a series of experimental measurements were performed on TMAH and KOH to find out which of these etchants can obtain a reproducible process with high control of the etching profile. Thus, the key parameters investigated were etching rate, selectivity against silicon dioxide, undercut and etching profile. These experiments were carried out on bulk Si and SOI samples together.

High concentration solutions were chosen because they have lower surface roughness and lower etch rate; therefore, it was easier to control the etching process. The experiments were performed at relatively low temperature so that the final structure could be controlled. About 7.5 % of IPA was added to the solutions to reduce the roughness and undercut especially during the 1st anisotropic etching step. Thus, the following three types of etching solutions were used to conduct these experiments:

-40 %wt KOH with added 7.5 % IPA at 45±1 °C and 56±1 °C

-25 %wt TMAH with added 7.5 % IPA at 56±1 °C

-15.6 %wt TMAH with added 7.5 % IPA at 56±1 °C

The experiments were performed in open beakers with no stirring, with no samples placed in solution for more than 25 min. The topography of the surface was detected after 12 min by using AFM.

3.4.3.1 Etch rate and surface morphology

Table 3.10 shows the average etches rates of undoped p-type single crystal <100> silicon in TMAH and KOH solutions at different temperatures. The etch rate is higher at higher temperatures. The <100> silicon surface was observed after 12 min etching in solution using AFM. The root mean square roughness R_q of <100> is presented in Table 3.10.

Table 3.10: Average etch rates of <100> silicon, surface roughness of <100> and <111> after TMAH and KOH etching. (Each number represents an average of five measurements).

Solution	TMAH		KOH	
Conditions	15.6 wt% +7.5IPA T=56±1°C	25 wt% +7.5IPA T=56±1°C	40 wt% +7.5IPA T=44±1°C	40 wt% +7.5IPA T=56±1°C
Average etch rate of <100> (nm/min)	124	107	78	140
Average R_q of <100> (nm)	1.7	1.1	2.1	1.8
Average R_q of <111> (nm)	3.1	2.7	3.2	3.6

Since the fabricated nanowires have two <111> planes, the smoothness of this surface will play an important role in any type of device applications. Therefore, it is essential to determine the surface roughness of the <111> plane. The analysis technique which was described in [52, 53] was used to obtain the value of sidewall roughness. However, in this current research, it was not required to tilt the samples during the AFM scan due to the advantage of using anisotropic wet etching. Thus the AFM image processing required two steps of analysis, namely image levelling and root mean square roughness R_q calculations.

In the image levelling step, the scanned image was rotated around the x and y axes to obtain a horizontal image. This was done by the following matrix [53]:

$$\begin{pmatrix} X_{f_i} \\ Y_{f_i} \\ Z_{f_i} \end{pmatrix} = R_x R_y \begin{pmatrix} X_i \\ Y_i \\ Z_i \end{pmatrix} \quad 1 \le i \le n^2 \tag{3.10}$$

where (X_i, Y_i, Z_i) and $(X_{f_i}, Y_{f_i}, Z_{f_i})$ are the coordinates of point i before and after rotation, n is the number of extracted points over the image size, and R_x and R_y are the rotation matrices around the x and y axes which are given by [53]:

$$R_x = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\theta_x & -\sin\theta_x \\ 0 & \sin\theta_x & \cos\theta_x \end{pmatrix} \tag{3.11}$$

and

$$R_y = \begin{pmatrix} \cos\theta_y & 0 & \sin\theta_y \\ 0 & 1 & 0 \\ -\sin\theta_y & 0 & \cos\theta_y \end{pmatrix} \tag{3.12}$$

where θ_x and θ_y are the angles around X and Y respectively.

The levelled surface produced a 2D matrix of the heights of the surface, and in the root mean square roughness calculation step, this matrix was converted to a vector with (m) points, and then R_q was calculated as follows:

$$R_q = \sqrt{\frac{1}{m} \times \sum_{i=1}^{m} (z_i - z_{av})^2} \qquad 1 \le i \le m \tag{3.13}$$

where z_i is the height at each point and z_{av} is the mean value. The data was adjusted to obtain zero mean value, thus $z_{av} = 0$. The surface topographies of the silicon sidewalls before and after rotation in addition to 3D images are shown in Figures 3.21 & 3.22 for 40%wt KOH and 25%wt TMAH respectively. While the average calculated values of R_q are presented in Table 3.10.

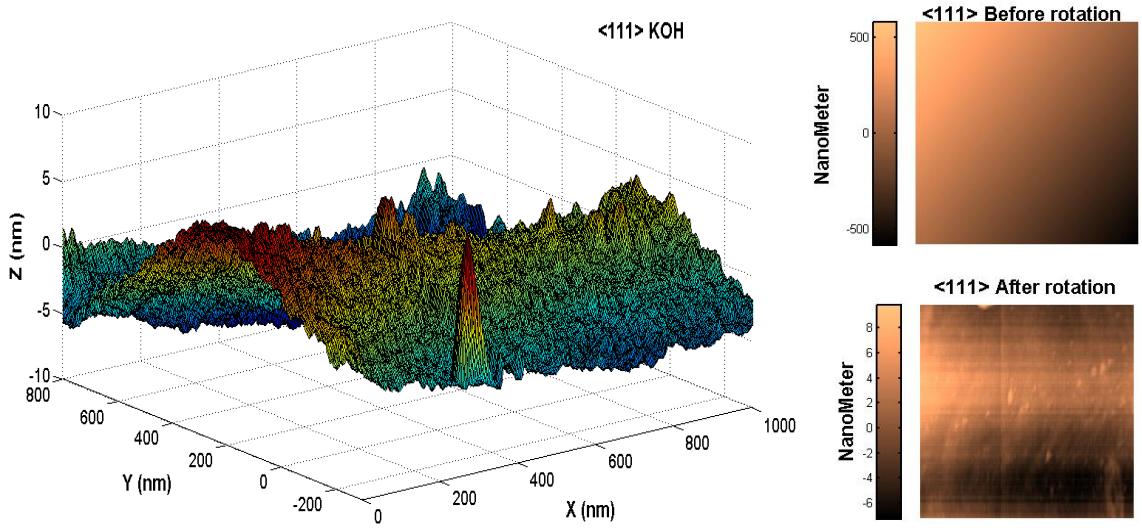

Figure 3.21: 3D image of <111> silicon surface after KOH etching (left) and 2D image of the same surface before and after rotation (R_q=3.2 nm).

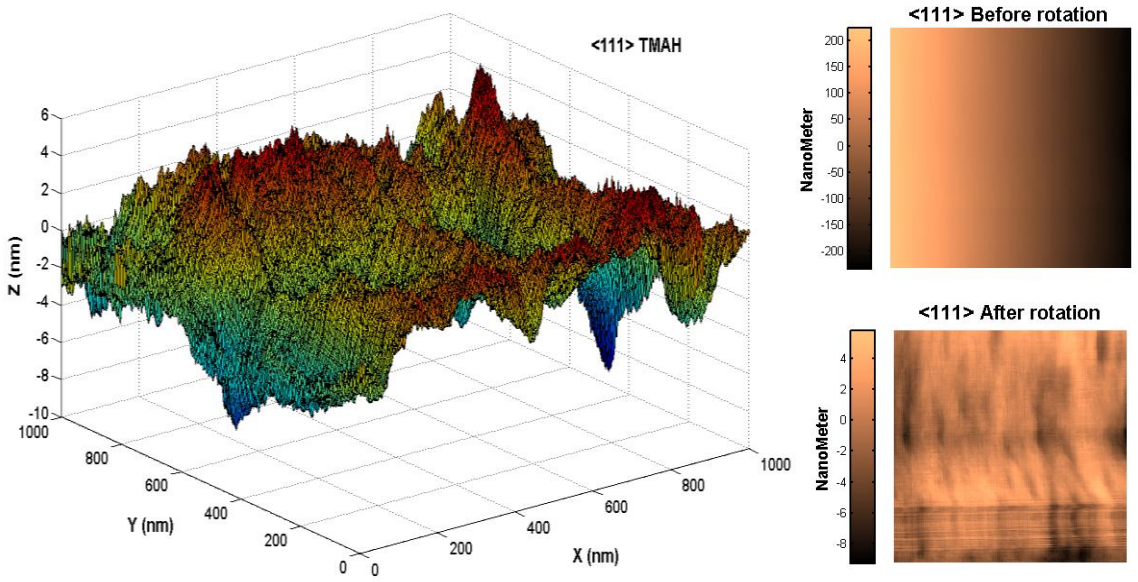

Figure 3.22: 3D image of <111> silicon surface after TMAH etching (left) and 2D image of the same surface before and after rotation (R_q= 2.4 nm).

3.4.3.2 Silicon dioxide and silicon nitride etch rates

The etch rates of thermally grown silicon dioxide and nitrogen-rich silicon nitride were determined by measuring the change of oxide and nitride film thicknesses after 20 min of etching in solution, using optical ellipsometry. The table below shows that KOH can etch thermally grown silicon dioxide more than ten times faster that of TMAH. The average etch rate in 40%wt KOH is 74 nm / hr at 65±1 °C, while it is 2.9 nm/min in 25%wt TMAH at 56±1 °C. This difference makes TMAH preferable over KOH etching. The etch rate of SiO_2 in KOH depends on the temperature and it is five times higher at 56±1 °C in comparison with 44±1 °C. Silicon nitride can be etched very slowly in both etchants and the etch rate is higher in TMAH in comparison with KOH (Table 3.11).

Table 3.11: Etch rates of thermal silicon dioxide and silicon nitride in TMAH and KOH. (Each number represents an average of five measurements).

Solution	TMAH		KOH	
Conditions	15.6 wt% +7.5IPA T=56±1 °C	25 wt% +7.5IPA T=56±1 °C	40 wt% +7.5IPA T=44±1 °C	40 wt% +7.5IPA T=56±1 °C
Etch rate of thermal SiO2 (nm/hr)	3.1	2.9	14	74
Etch rate of PVD Si3N4 (nm/hr)	2.1	2.3	<1	<1

3.4.3.3 Undercut rate

Step number (3) in the fabrication process in section 3.3.1.3 was used to measure the undercut, the schematic of which is shown in Figure 3.23, where undercut was defined as the etched silicon under the silicon nitride mask. The undercut rate is higher for TMAH in comparison with KOH. It is 19.1 nm/min in TMAH 25%wt at 56±1°C and slightly increases in TMAH 15.6%wt to reaching 22 nm/min, as shown in the Table 3.12.

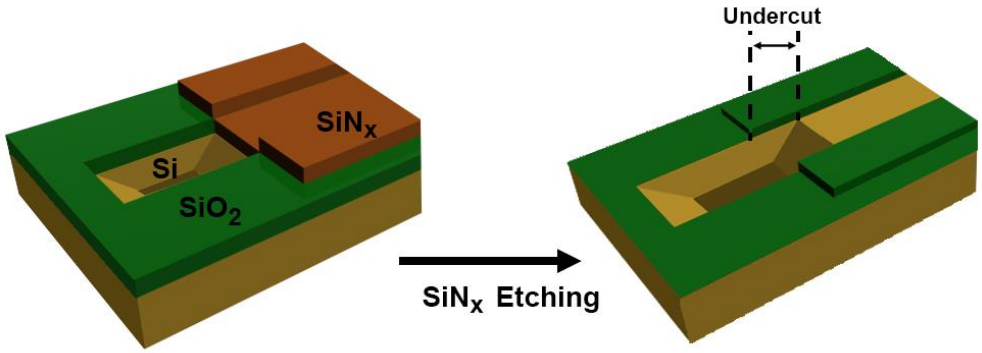

Figure 3.23: The fabrication steps that involved in the undercut measurements.

Table 3.12: Average undercut values. (Each number represents an average of five measurements).

Solution	TMAH		KOH	
Conditions	15.6 wt% +7.5IPA T=56±1°C	25 wt% +7.5IPA T=56±1°C	40 wt% +7.5IPA T=44±1°C	40 wt% +7.5IPA T=56±1°C
Average undercut (nm/min)	24.7	21.2	11.1	22.8

3.4.3.4 Anisotropic etching on fabrication of nanowires

During the fabrication of SiNWs, two steps of anisotropic wet etching were carried out to obtain triangle SiNWs with two <111> sides (section 3.3.1.3 and 3.3.1.6). In this section the impact of these two etching steps on the final nanowires structure was investigated.

3.4.3.5 First anisotropic etching step

A sequence of experiments on p-type single crystal <100> silicon was carried out to investigate the effect of etch depth on the etching profile. The AFM was used to measure the etch depth and the angle between sidewall and <100> plane. Figure 3.24 shows an exponential relationship between the angle and the depth of silicon. As indicated in the figure, at small silicon etched depth the measured angle was smaller than that of the 54.5° which is the angle between <111> and <100> planes. The appearance of the 54.4° angle between <111> and <100> is seen after the depth of silicon exceeds 150 nm. In some measurements the 54.4° did not appear even at depth exceeded a micron. The function form

in Figure 3.24 could be due to various factors. The etch rate of <111> plane is slower than that of <100> plane. Thus, for a short etching period, a few nanometers of the <100> plane would be etched before the <111> plane is completely exposed [54, 55]. The misalignment could also be a reason for this difference because all exposed planes start to be etched before reaching the <111> plane which works as an etchant stop [49].

This can be seen as a non-uniformity of etching along the sidewall. The convolution of AFM tip shape can also cause inaccuracy in the measurements, as mentioned previously (For further study, a TEM image is required to confirm the above results).

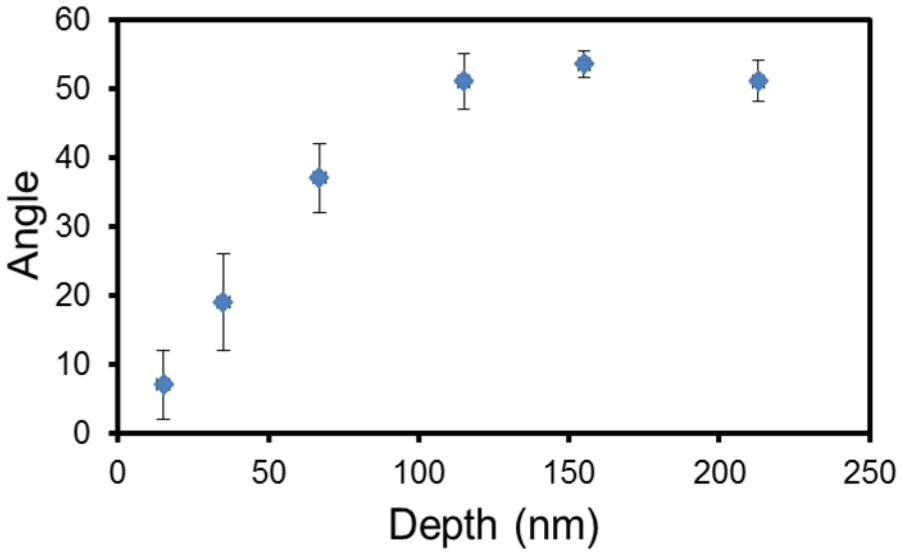

Figure 3.24: The effect of short etching time on the angle between <100> and <111> planes.

Therefore, a long etching time is required to completely expose the <111>plane and to obtain a smooth sidewall. However, prolonging etching time can increase undercut and can shift the final structure from the one originally patterned and can cause rounding at the corners.

Moreover, the etching time of the 1st anisotropic step can also have an impact on the lateral oxidation of silicon underneath silicon nitride and consequently on the final nanowire structure. Table 3.13 shows the effect of the 1st etching time on the width of the nanowires. As the etching time increases the final width of nanowire decreases. This could be explained as an increase of undercut with increasing etch time which reduces the amount of silicon exposed to thermal oxidation [56]. The schematic in Figure 3.25 shows the position of nitride and lateral oxidation for each position.

Table 3.13: Average nanowire width as a function of 1st KOH etching time (2nd KOH adjusted for 4 min at 56 °C).

	3 min 1st KOH	5 min 1st KOH	7 min 1st KOH
Average top width of NW	85	42	35

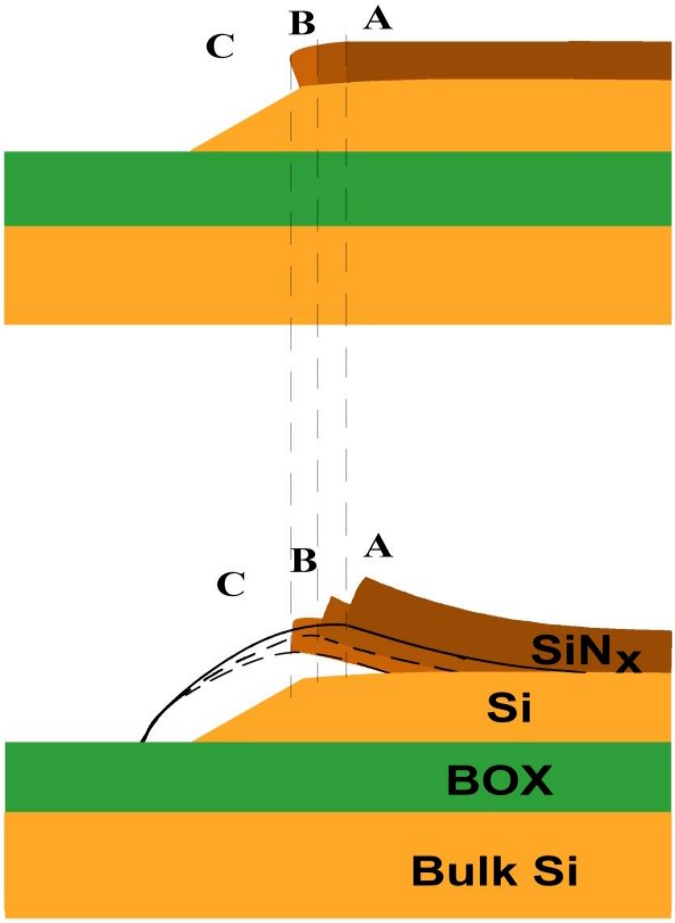

Figure 3.25: Schematic shows the impact of the position of nitride film on lateral oxidation [56].

For the reasons mentioned above, the 1st etching time should be designed carefully to obtain controllable process and should take into account all the issues discussed.

3.4.3.6 2nd anisotropic etching step

Both TMAH and KOH were used successfully in the cleanroom to fabricate nanowires on SOI. However, when the samples were immersed for a long time in KOH solution the nanowires started to break along the wire length due to the etching of the sidewall oxide. Thus, the mask thickness was not sufficient to protect the silicon. The oxide on the sidewall and the time to break depended on the sidewall oxide thickness. The AFM image in Figure 3.26 shows an example of two samples placed in KOH for five or for eight minutes. The latter revealed breaks occurring along the length of the wire. Thus, sufficient oxide thickness (Figure 3.27) must be grown on sidewall when KOH is used as an etchant.

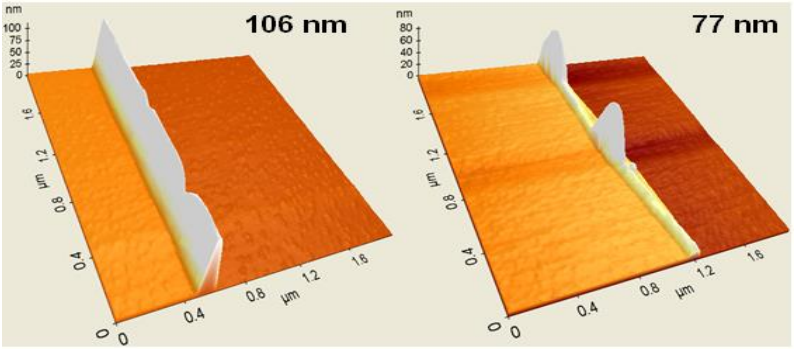

Figure 3.26: Silicon nanowires after 5 min (left) and 8 min (right) in 2nd KOH.

In situ nanowire size reduction

As was introduced previously, the process was used to successfully fabricate nanowires with different cross sections and thicknesses. Trapezoidal and triangle shapes could be obtained using anisotropic wet etching; the size could be reduced down to sub-10nm. However, this requires a controllable technique to form the desired thickness and structure. Etching in TMAH and KOH can provide *in situ* both in a fast and controllable way to shrink the dimensions of nanowires. This simply can be done by controlling the duration of the time that the samples are placed in these etchants. The reliability of this technique depends on the robustness of the sidewall mask, especially when KOH is used as an etchant.

A series of experimental measurements were carried out on SiNWs fabricated on bulk and SOI wafers using TMAH and KOH solutions under various conditions to measure the lateral and vertical reduction of nanowires sizes. The vertical size reduction was estimated by measuring the changes in nanowire thickness with time, while the lateral size reduction was estimated by calculating the change of lateral distance for different etching times. It should be noted that the values of lateral size reduction should be similar to the undercut ones, which are presented in Table 3.14.

Table 3.14: Averages etch rates of <111>. (Each number represents an average of five measurements).

Solution	TMAH		KOH	
Conditions	15.6 wt% +7.5IPA T=56±1°C	25 wt% +7.5IPA T=56±1°C	40 wt% +7.5IPA T=44±1°C	40 wt% +7.5IPA T=56±1°C
Average etch rate of <100> (nm/min)	124	107	78	147
Lateral etch rate of <111> (nm/min)	22.3	19.2	10.7	23
Vertical etch rate of <111> (nm/min)	14.2	13.1	6.7	15.6
Vertical<111>/<100> (nm/min)	0.11	0.12	0.085	0.1

There is no limit in the size reduction of nanowires during etching in TMAH. However, in the case of KOH, the etching of the sidewall oxide during the formation of the nanowires can limit the ability of the process to obtain very fine structures. Thus, the thickness of sidewall oxide and the etch rate of silicon dioxide should be considered, if KOH is applied to produce small size structures.

The maximum <111> thickness of nanowires that can be etched in KOH without any loss or cuts in the nanowires, can be given by:

$$y_{max} = (Kt_{tot} - t_c) * \frac{ER_{<111>}}{ER_{SiO_2}} \tag{3.14}$$

where t_{tot} is the oxide thickness grown on the sidewall; Kt_{tot} is the oxide thickness remaining on the sidewall after the removal of oxynitride; t_c is the sum of the oxide consumed during etching of silicon nitride, after the removal of oxynitride, and the thickness of oxide mask that is required to protect <111> plane. $ER_{<111>}$ and ER_{SiO_2} are the etch rates of <111> plane silicon and thermally grown silicon dioxide in KOH respectively. Now the minimum size of nanowires that can be obtained during the KOH etching, if the initial thickness of silicon is known, can be estimated. Figure 3.26 shows the estimated minimum thickness of nanowires as the function of the total oxide thickness at the sidewall at different initial thicknesses of silicon. The values of $ER_{<111>}$ and ER_{SiO_2} were taken from Table 3.14 and Table 3.11 respectively for 40%wt KOH at 56 °C, while nitride thickness was 27 nm. Using these etching specifications, sub-50 nm nanowires cannot be obtained with 200 nm Si starting thickness, but can be obtained if it is 150 nm, providing that the sidewall oxide is thicker than 18 nm. This makes the use of KOH with this specification incompatible with the size reduction process.

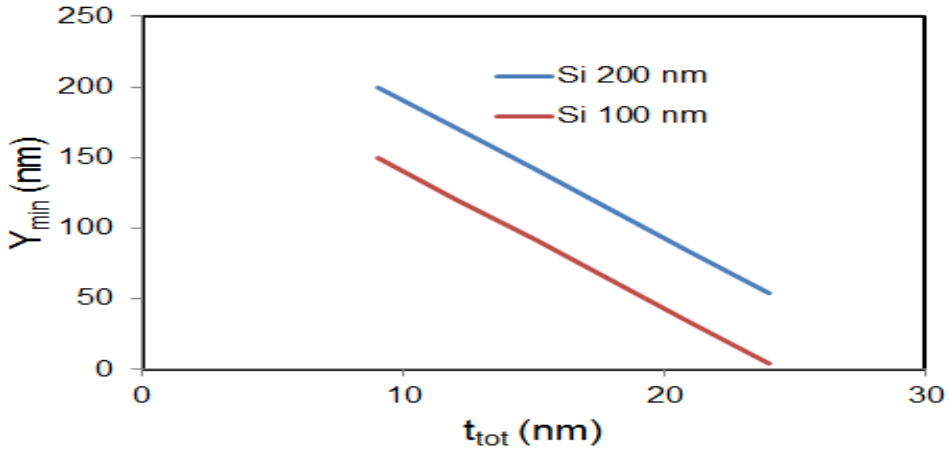

Figure 3.27: The minimum thickness of nanowires (Y_{min}) that can be obtained with KOH; $Kt_{tot} = 0.7t_{tot}$, $t_c = 5$ nm calculated for 27 nm nitride thickness.

Finally, the AFM images in Figure 3.28 show different sizes of triangle nanowires formed by using *in situ* method. It also indicates that a sub-10 nm triangle nanowire is successfully formed by reducing the size using this method. The height and the angles of the nanowires are presented in the same figure. The increase of width due to tip geometry (with AFM tip radius 5 nm) is calculated to be 8 nm using equation 3.5.

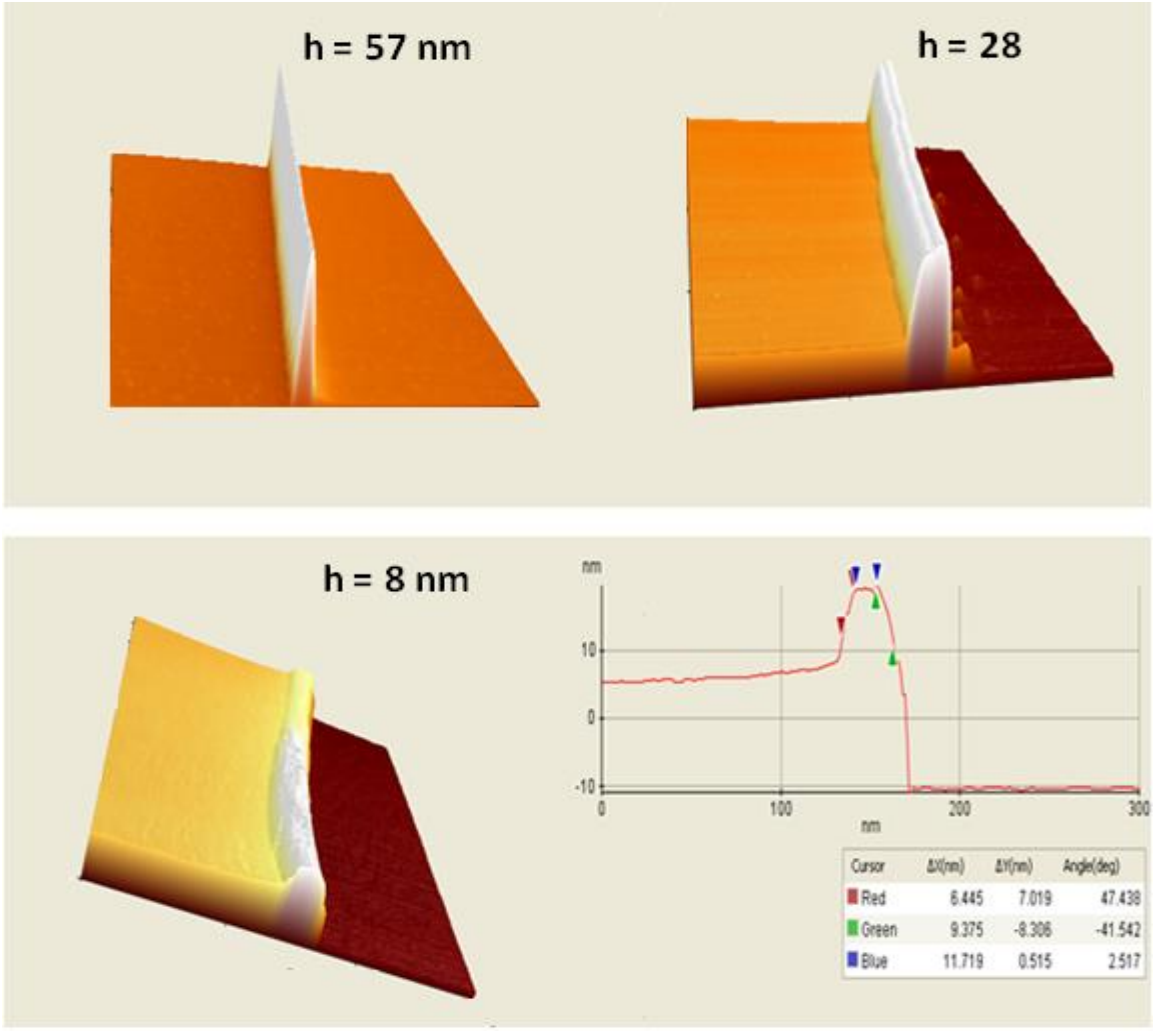

Figure 3.28: Different sizes nanowires formation by using *in situ* size reduction. (Sub 10 nm is obtained).

3.5 Null results

In section 3.3.1, after the 2nd anisotropic wet etching step, the nanowire profile is usually measured using AFM. This profile is represented by the schematic Figure 3.29 showing the nanowire with the <111> sidewall oxide remaining after the 2nd anisotropic wet etching step. It is, therefore, crucial to dip the samples for a few seconds in BHF to remove the sidewall oxide otherwise the measured thickness will be the thickness of silicon dioxide and not that of nanowire. This common mistake will result in a measured nanowire profile

different from the actual one which will eventually indicate an error in the values of the electrical measurements.

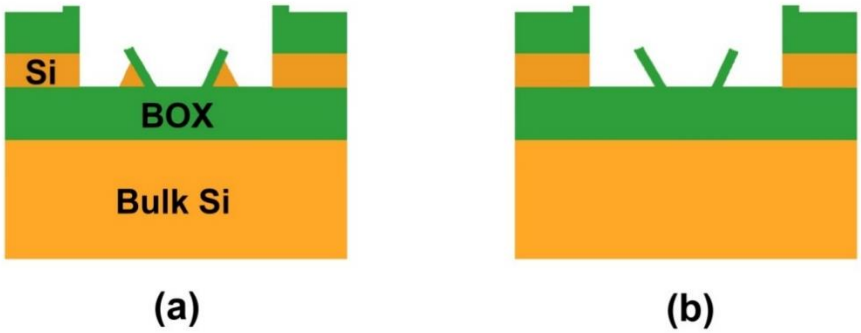

Figure 3.29: Schematic of nanowire profile after 2nd ODE etching; (a) and (b) should have the same height after AFM scan.

The reproducibility of RTP

In this research, JetFirst 200 rapid thermal processing (RTP) system was used to perform different high temperature tasks, such as introducing dopants into the silicon substrate, oxidising silicon and improving the quality of contacts. However, the annealing results using RTP were not repeatable and variations in temperature measurements at different runs were observed which largely affected the fabrication process of nanowires.

In this section two cases where variations in RTP temperature at different runs were observed:

Case 1: The sheet resistance was measured for two sets of samples apparently having the same Pyrometer temperature readings and the only difference being that the RTP was performed on one set of them after cleaning the Pyrometer window while the other was performed before Pyrometer window cleaning. Figure 3.30 shows that the variation of temperature is about 100 $^{\circ}$C which means that the reading error is about 10%.

Case 2: A run to run variation of oxide thickness on control samples was observed. Figure 3.31 shows about 30 % variation of oxide thickness over time for oxide conditions at 900 $^{\circ}$C for 160 sec in O_2.

The RTP is used by many users and with different materials and different conditions. It is expected that there will be changes in the nature of the layers on the substrate wafer with time which could change the reflectivity of the wafer and consequently give error in temperature measurement. Cleaning the pyrometer window, changing the substrate wafer and changing the whole halogen lamps at the same time if one lamp is broken and doing calibration regularly are required to achieve a repeatable RTP process.

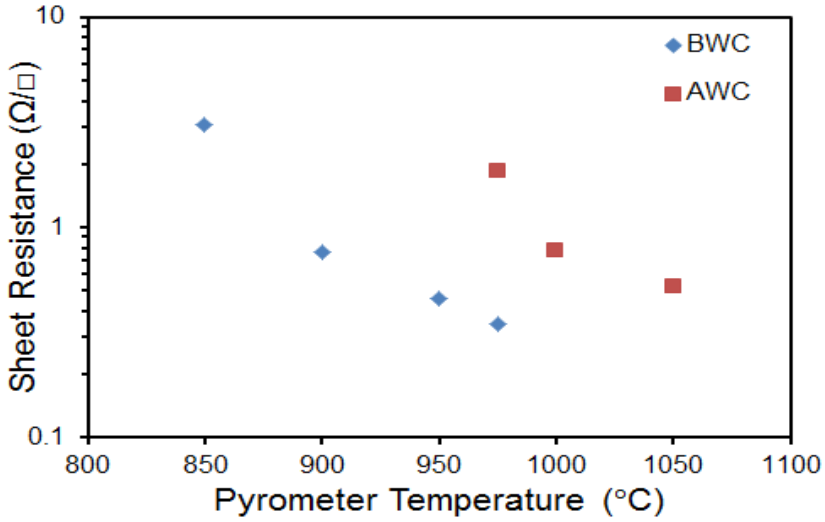

Figure 3.30: Sheet resistance measurements before (BWC) and after (AWC) pyrometer window cleaning.

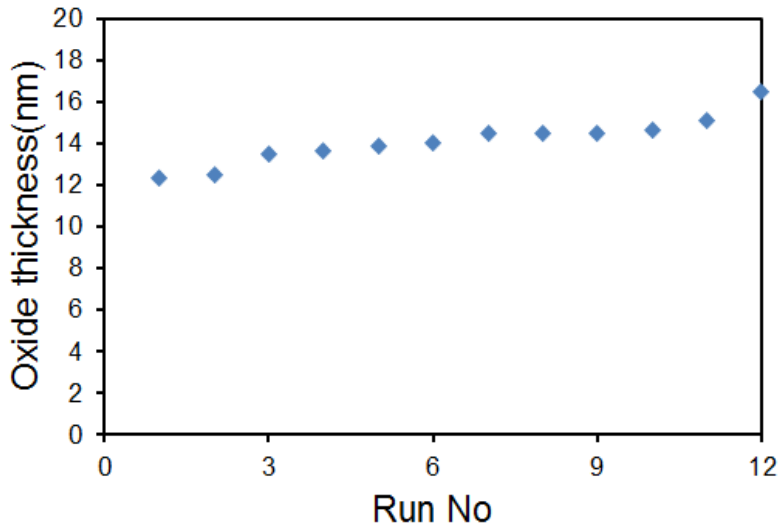

Figure 3.31: Run to run variation of oxide thickness using RTP (the trend does not represent the real order).

3.6 Summary

The optimised fabrication process of silicon nanowires using an indirect top-down method based on optical lithography, thermal oxidation and anisotropic wet etching of silicon is described in this chapter. To obtain a reliable and reproducible process, four main aspects are considered, such as the property of silicon nitride films during thermal oxidation, the behaviour of Si and SOI substrates during the oxidation using radiant and conduction heating sources, the robustness of the sidewall mask and the etching characteristics using TMAH and KOH. The nitrogen-rich silicon nitride film is preferable as an oxidation mask as it exhibits the lowest oxidation rate and the highest etch rate in boiling phosphoric acid in comparison with silicon-rich silicon nitride films. The oxidation rate of films is investigated by studying the change of refractive indexes of the oxidised films as a function of films thicknesses by using two ellipsometry models. To address the second aspect, this chapter reports differences in characteristics between a multilayer structure of SOI and a single Si structure when they are oxidised using lamp based RTP radiation. If SOI and Si samples are oxidised at apparently the same temperature and for the same period of time the oxide on top of the SOI sample will be thinner than the one on a single Si sample. Thus, in order to realise nanowires with high reproducibility, the oxide thickness on top of SOI should be estimated when the RTP is used to oxidise the sidewall. In terms of the robustness of the sidewall mask, the minimum oxide thickness required to mask the <111> silicon efficiently before the 2nd anisotropic wet etching step is found to be 2.9 nm. The etching characteristics of silicon using TMAH and KOH are also investigated. Based on the experiments in this research, the TMAH etchant offers a more reliable process with smooth surface and a controllable etching process compared with KOH. However, for both etchants the 1st and 2nd etching times should be designed carefully to obtain a controllable process, as both etching times determine the final nanowire structure. The size of silicon nanowires are reduced by using two known methods: size reduction using thermal oxidation and *in situ* size reduction. The size reduction using thermal oxidation shows nonuniformity in the reduced size. The *in situ* size reduction, on the other hand is a controllable process and it is also easier to apply. The research using this method investigates the impact of concentration, temperature, and doping and solution type on the vertical and lateral size reduction of nanowires. Silicon nanowires with vertical dimensions less than 10 nm are fabricated using this method.

Another key process described in this chapter is the diffusion of dopants into a silicon substrate by using spin-on-doping. The doping level is controlled by varying the diffusion temperature. The dopant distribution as a function of depth follows a complementary error function *erfc*.

Finally, in this chapter, a simple model is also developed to determine the apparent increase of nanowire width due to the AFM tip geometry.

Now, having obtained an optimised fabrication process with controlled dimensions, the next step is to study the electrical properties of these nanowires to demonstrate the potential of their use in devices applications, which will be introduced in the next chapter.

3.7 Future work

Section 3.2.3 SOD removal

In section 3.2.3 it has been demonstrated that a residual shallow layer between the SOD and silicon layer is formed during the SOD process and it is very difficult to remove. Cooling the samples to room temperature after SOD diffusion with certain subsequent etching steps can solve the problem with no surface damage. However, the characteristics of this shallow layer and the effect of cooling temperature are not sufficiently understood. Thus, it is important to study the characteristics of this layer using XPS or IRFT; therefore it is reasonable to suggest the following procedure:

1- Prepare two sets of SOD samples; then perform diffusion.
2- Cool one of them to room temperature and the other to 300-400 °C.
3- Measure the thickness and refractive index using ellipsometry.
4- Immerse the samples in BHF for 45 sec to 1 min depending on SOD thickness.
5- Analyse the property of the surfaces using XPS or FTRI; then make comparison between the two surfaces.
6- Once the property of the surface is analysed an ellipsometry model can be developed, so the refractive index and the layer thickness can be accurately determined.

Section 3.3 Fabrication of silicon nanowires

In section 3.2 dopants are introduced into silicon over the whole SOI sample. In other words the source (S), drain (D) and nanowire (NW) have the same doping level which is controlled simply by varying the diffusion temperature as described previously in Figure 3.2. However, in many nanodevice applications, it is essential to dope the nanowires differently from the source and drain. The fabrication process described in this chapter offers the possibility of doping the nanowire separately from source (S) and drain (D) with no extra steps. This is because after the 2nd anisotropic wet etching step only the SiNWs are exposed, while the source (S) and drain (D) are protected by oxide, as clearly shown in the schematic in Figure 3.32. This can be applied in further study focusing on the feasibility of the process.

However, this process will produce suspended nanowires which may cause collapsing of the nanowire after the removal of dopants.

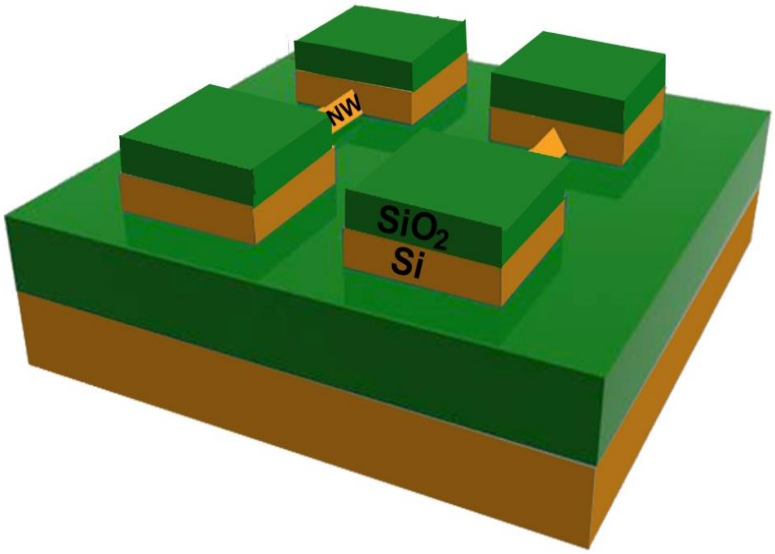

Figure 3.32: 3D schematic of the nanowires after 2nd anisotropic wet etching step; oxide remains on the bulk source and drain (useful for selective doping of nanowires).

Section 3.4.1.1

It is mentioned that the etch rate of RF sputtered silicon nitride deposited on dry SiO_2 film in BHF is three to four times faster than the etch rate of silicon nitride deposited on silicon substrate. This observation could be used in an effective way to define structures without the need for lithography patterning, as shown in Figure 3.33. It is interesting to focus further study on this Deposition-Etching technique and research how it can be optimised in many fabrication processes or how it can be minimized, in case it might seem undesirable.

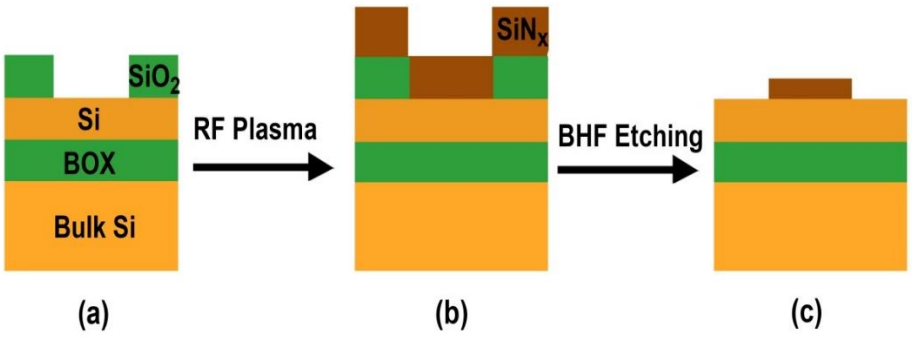

Figure 3.33: Deposition-Etching technique.

Section 3.4.1.3 Film behaviour during thermal oxidation

In section 3.4.1.3 the characteristics of thermally oxidised silicon nitride films are investigated by measuring the refractive index as a function of depth by using optical

ellipsometry. Two simple models are used to describe the characteristics of oxidised silicon nitride. However, in order to accurately determine the composition of film with depth it is recommended, for further study, to analyse the depth profile by using X-ray photoelectron spectroscopy (XPS) or Auger electron spectroscopy (AES) technique together with ellipsometry.

Section 3.4.2 Characteristics of thermal oxidation

In section 3.4.2.1 it is reported experimentally, that SOI and bulk Si samples have different characteristics when they are heated by an infrared radiation source. It is important to fit the experimental data with a theoretical model. Therefore, it is recommended to model the above structures by using similar models to the one used by [44]. It is also important to develop this model to be applied on patterned samples, such as the nanowires fabricated in this research.

In section 3.4.2.2 a TEM image is required to determine the sidewall thickness on SOI samples, and to investigate the uniformity across the sidewall. It is also required for section 3.3.3.2 to determine the oxidation behaviour of the nanowires.

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Chapter 4

Electrical Transport in Silicon Nanowire

4.1 Introduction

Silicon nanowires are attractive objects for future nanodevices, such as nanoelectronic logic, solar cells, thermoelectric devices and biological sensors. In the previous chapter, an indirect top-down method for the fabrication of silicon nanowires has been optimised which is based on optical lithography, anisotropic wet etching and thermal oxidation. Reproducible nanowires with high yield and controllability over dimension have been realised. However, the successful use of these nanoscale components in future device applications depends on the reliability and reproducibility of satisfactory performance levels.
The achievement of effective nanowire performance depends on their electrical contacts. Good ohmic and stable contacts are required to accurately determine the characteristics of nanowires.

This chapter discusses the issues related to contacts for nanowires in addition to the electrical properties of the nanowire itself. The chapter opens with an investigation of the electrical properties of different metal/silicon systems and their stability at different elevated temperatures, followed by a description of electrical transport in silicon nanowires whereby their key parameters, such as electrical resistivity, electrical resistance and impurity concentration, are investigated.

4.2 Electrical contacts

Contact between semiconductors and metals plays a crucial role in device performance. The formation of ohmic contacts requires stable and reproducible electrical characteristics as well as low contact resistance if the qualities of nanodevices are to be evaluated. These

two points should be carefully considered during the characterisation of nanowires to ensure that there is no significant impact of the contacts on the device characteristics. Thus, in this research, the choice of the metal contact system should result in an ohmic contact with low contact resistance, and it must withstand post-metallization annealing during the removal of interface traps.

In this study, three metal contact systems are realised on silicon nanowires, and their properties are investigated. However, it is useful to review the two above-mentioned issues which are required to obtain reliable contacts for nanowires along with the key properties of metal/semiconductor interfaces before starting the experimental section.

4.2.1 Energy level alignment and band bending

When a semiconductor is brought into contact with a metal under conditions of thermal equilibrium, the Fermi level in the semiconductor aligns with that of the metal. Charges flow from the semiconductor to the metal/semiconductor interface in alignment with the Fermi level, creating a space charge region in the semiconductor at the interface with the metal, causing the energy bands of the conduction and valance bands to bend at the interface. Depending on the positions of the conduction and valance bands with respect to the Fermi level, a Schottky barrier or an ohmic contact can be formed[1, 2]. If the Fermi level lies above the conduction or below the valance band, an ohmic contact is formed (Figure 4.1(b)). However, if the Fermi level lies inside the band gap of the semiconductor, a Schottky barrier $\emptyset_b$ is formed (Figure 4.1(c)). In the Schottky-Mott model, the barrier height depends on the metal's work function Φ_m and the electron affinity of semiconductor χ, and is given by: $\emptyset_b = \Phi_m - \chi$. However, if interface states are present in the semiconductor and the metal/semiconductor contacts are in the equilibrium state, interface states can penetrate the semiconductor and form a dipole on the semiconductor causing a change in the position of the Fermi level.

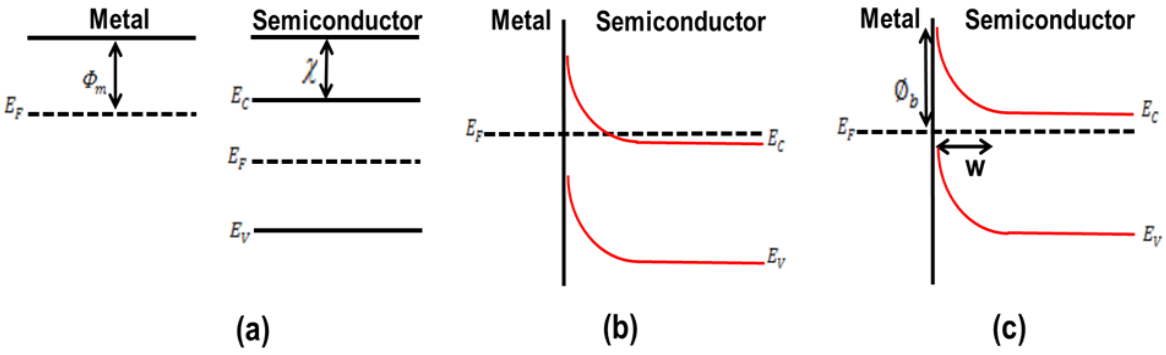

Figure 4.1: (a) Energy band diagram of a metal and semiconductor before contact; (b) energy band diagram for ohmic contact of metal/n-type semiconductor; (c) energy band diagram for Schottky contact of metal/n-type semiconductor, (w is the depletion region width).

In this case, the Schottky barrier is independent of the metal's work function and is determined by these metal-induced gap states [3, 4]. However, the scale of this effect has been reported to be lower when the depletion width is larger than the size of the nanostructures [2, 5]. The width of the depletion region is another parameter which is central to device performance, and it can be defined as the distance that the Schottky barrier may extend inside the semiconductor (Figure 4.1(c)). This parameter depends on semiconductor doping. However, at nanoscale when the depletion region is larger than the diameter of the nanowire, the effect of dimension on depletion width cannot be neglected [6].

4.2.2 Charge transport mechanism for metal/semiconductor interface

There are two main transport mechanisms across the Schottky barrier at the metal/semiconductor interface: thermionic emission and tunnelling transport [1, 7].

In thermionic emission, electrons use thermal energy to cross over the barrier (Figure 4.2(a)). This is normally dominant in low doped semiconductors at $< 1 \text{ X } 10^{17}$ cm^{-3} at room temperature. In tunnelling, electrons tunnel through the barrier, which is a quantum mechanical effect (Figure 4.2(b)). This is normally dominant in heavily doped semiconductor at $> 1x10^{19}$ cm^{-3}, where the width of the barrier is thin enough to the extent that the probability of tunnelling increases. In moderately doped semiconductors, transport can occur due to both mechanisms (Figure 4.2(c)).
Transport can also occur due to electron-hole recombination, where electrons and holes recombine in the depletion region either directly or through defects within the band gap. This occurs when the barrier height is large, making transport by tunnelling and thermionic emission insignificant.

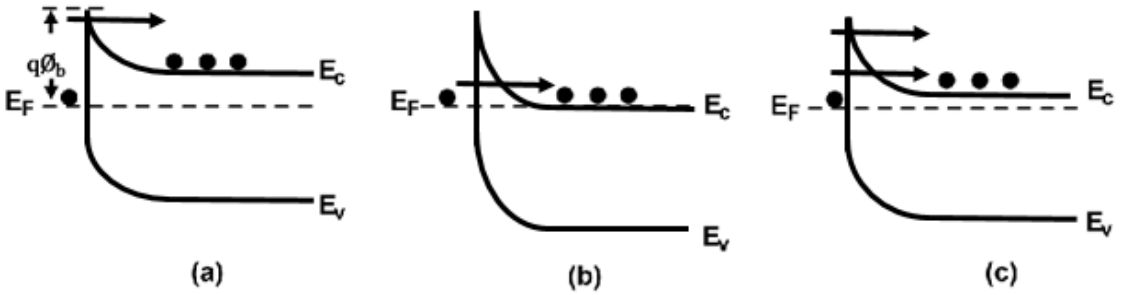

Figure 4.2: Conduction mechanism at metal-semiconductor contacts (a) thermionic emission; (b) tunnelling; (c) thermionic-tunnelling emission.

4.2.3 Ohmic contact

The specific contact resistivity ρ_c and contact resistance R_c are two important parameters in characterising metal/semiconductor contacts. The specific contact resistivity is independent of geometry and is defined as [1]:

$$\rho_c = \left(\frac{dJ}{dV}\right)^{-1}_{V=0} \qquad (\Omega.\,cm^2) \tag{4.1}$$

where J is the current density and V is the voltage drop across the metal/semiconductor interface.
In a lightly doped semiconductor where thermionic emission is the dominant transport, the specific contact resistivity is given by [1]:

$$\rho_c = \frac{K}{qA^*T}\exp\left(\frac{q\emptyset_b}{KT}\right) \tag{4.2}$$

The ohmic contact in this regime can be obtained by reducing the barrier height where K is the Boltzmann constant, and q and A^* are the elementary charge and the Richardson constant, respectively.

In a heavily doped semiconductor, where tunnelling is the dominant type of transport, specific contact resistivity is given by [1]:

$$\rho_c \sim \exp\left(\frac{4\sqrt{m^*\varepsilon_r}\emptyset_b}{\hbar\sqrt{N_D}}\right) \tag{4.3}$$

where $\hbar$ is the reduced Plank constant, ε_r is the dielectric constant of the semiconductor, and N_D and m^* are the donor concentration and electron effective mass respectively. The ohmic contact in this regime can be improved by increasing the carrier concentration.

Therefore, there are two possibilities with regards to ohmic contacts forming between the metal and the semiconductor. 1) A low Schottky barrier height, ideally lower than 0.3 eV [8], this is normally achieved by matching the work function of the metal with that of semiconductor. 2) Narrow depletion width, which can be undertaken by increasing the doping level of the semiconductor near the interface with the metal, in this case the electrons can still easily tunnel through the barrier even with a large barrier height. The first method is normally difficult to achieve. As an example, the barrier height of aluminium to p-type silicon is roughly 0.45 eV and about 0.7 eV to n-type silicon [8], which makes the specific contact resistance too high. Thus, a high doping level is required to form ohmic contact between the aluminium and the n- and p-type silicon.

The contact resistance is obtained by dividing the specific contact resistivity by the contact area.

4.2.4 Choice of material for ohmic contacts

Aluminium is widely used in silicon technology because it has low electrical resistivity, good resistance against corrosion and has an etching process which is compatible with silicon [1, 9]. However, silicon can diffuse in aluminium at a relatively low temperature, leading to the formation of holes inside the silicon. The aluminium then penetrates inside of the silicon, causing device failure [10-12]. Other metals, such as gold (Au), silver (Ag), palladium (Pd) and copper (Cu) are also used in many device applications [1, 13, 14]. However, all of these metals exhibit high diffusivity in silicon during annealing. Post-metallisation annealing is required to improve the quality of the metal/semiconductor interface and reduce interface oxide traps as well as to obtain low contact resistance [1]. Therefore, in order to prevent device failure and to obtain low contact resistance, a metal diffusive layer is normally deposited between the top metal and the silicon. This layer should have good adhesion to silicon, low contact resistance, low reactivity both to silicon and the top metal layer and, above all, it should be thermally stable. There are many metal films whose alloys are used as a diffusion barrier between silicon and the top metal, such as titanium (Ti), titanium nitride (TiN), and titanium tungsten (TiW), titanium (Ti)/ tungsten (W), Tantalum (Ta), Tantalum nitride (TaN) [12, 14, 15]. However, it is not expected that the diffusion of top metals into the silicon can be completely prevented due to the reaction of the top metal with the diffusion barrier during annealing. For example, it has been reported that the aluminium in Al/Ti/Si contact systems reacts with titanium at temperatures above 400 °C to form the titanium aluminium compound $TiAl_3$, which could lead in the end to contact failure when the diffusion layer is totally consumed [16]. Therefore, it is important to carefully select the metal system and test its electrical properties and thermal stability prior to any device characterisation.

4.2.5 Electrical characterisation of contacts

In this research, two contacts are either placed on bulk silicon connected to the silicon nanowire or directly on the silicon nanowire. In the former case, the contact area is large and an ohmic contact can be easily obtained. In the latter, the contact area is small and it is expected that high contact resistance and non-ohmic characteristics may be found. The study of both structures could give better understanding of the properties of the contact with silicon nanowires.

In this research, three contact systems are investigated, both on planar silicon microwires and triangular silicon nanowires, in order to study the formation of ohmic contact, specific contact resistivity and the stability of the contact systems at different annealing temperatures. Aluminium was selected as the top layer because it has high conductivity and a low oxidation rate at room temperature. Titanium was chosen as the diffusive layer since

it has low contact resistance, dissolves native oxide at a low annealing temperature, and forms an ohmic contact for n-type silicon.

Microwires typically have rectangular cross-sections with a thickness of about 90 nm and a width of 2 µm; while nanowires could have trapezoidal or triangular cross-sections with different thicknesses. Three contact structures were selected for these experiments:

a- Al/Ti/Si (100 nm/70 nm/Si)
b- Al/W/Ti/Si (100 nm/20 nm/70 nm/Si)
c- Al/Ti/AlO_x/Si (100 nm/70 nm/0.6 nm/Si)

All metal contacts were deposited using an electron beam evaporator (refer to Appendix B for fabrication processes and see section 3.3), while AlO_x was grown using atomic layer deposition (ALD) prior to the metallization step. Annealing was performed at various temperatures from 250 °C to 450 °C. All annealing steps below 350 °C were performed in a resistive furnace in the presence of nitrogen while the above-mentioned annealing steps were performed by using RTP in the presence of forming gas H_2/N_2 3.5 % H_2. The samples were doped with n-type phosphorous by using the spin on doping (SOD) method and the doping level on the SOI substrate ranged between 4.5 X 10^{18} – 7.5 X 10^{18} cm^{-3}.

In this research, several methods were used to measure the contact characteristics of microwires and nanowires. For microwires, the multiwire test method based on the transmission length method (TLM) was used to extract contact resistance, transfer length and specific contact resistivity [17]. For silicon nanowires, the four probe structure method and multiwire test method were both used to measure the total resistance, nanowire resistance, contact resistance and specific contact resistivity [18].

In the multiwire test method, the micro/nanowire is placed between two pairs of contacts, as shown in Figure 4.3(a). The micro/nanowire should have the same width and height and the only difference is the variation in length. The resistance of the structures is measured as a function of length, as shown in Figure 4.3(b). Parameters such as transfer length, contact resistance and sheet resistance are measured by fitting the measured resistances to the linear model. The total contact resistance is given by [19].

$$R_T = A.l + B \tag{4.4}$$

where A and B are the fitting parameters, $A = \frac{R_{sh}}{W}$, $B = 2R_C$ and $\frac{A}{B} = -2L_T$

The specific contact resistivity is then calculated by using:

$$\rho_C = R_{sh}L_T^2 \tag{4.5}$$

In the four probe structure shown in Figure 4.3(c), the electrical current is applied between the outer two probes, while the voltage drop between the inner probes is measured. Thus, the nanowire resistance R_{NW} and the effective nanowire resistivity ρ_{eff} are extracted from:

$$R_{NW} = \frac{I_{14}}{V_{23}} = \rho_{eff}\frac{l_1}{A} \tag{4.6}$$

where l_1 is the distance between the inner two probes and A is the cross section of the nanowire, and the total resistance is measured between the outer contacts and is given by:

$$R_T = \frac{V_{14}}{I_{14}} \tag{4.7}$$

The contact resistance is then measured using the following equation:

$$R_T = 2R_C + \rho_{eff}\frac{l_2}{A} \tag{4.8}$$

where l_2 is the length between the outer probes.

The contact resistance has been derived and documented in reference [18] and can be given by:

$$R_C = \frac{\rho_{eff}L_T}{A}\coth\left(L/L_T\right) \tag{4.9}$$

The above equation is used to extract the transfer length, while the specific contact resistivity in the nanowire is calculated by:

$$\rho_C = A_C R_C \tag{4.10}$$

where A_C is the contact area between the metal and nanowire. In the case of a long contact when $L > L_T$, equation 4.9 can be simplified as:

$$R_C = \frac{\rho_{eff}L_T}{A} \tag{4.11}$$

And equation 4.10 becomes:

$$\rho_C = P_l L_T R_C \tag{4.12}$$

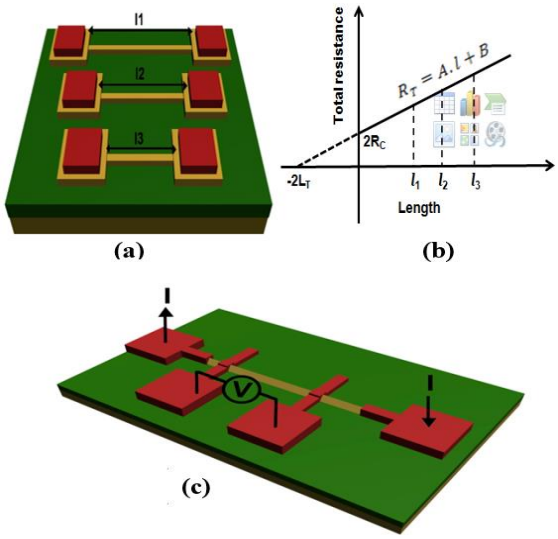

Figure 4.3: (a) Schematic of multiwire test method; (b) plot of total resistance as a function of wire length for multiwire structure; (c) schematic of four probe method.

4.2.5.1 Experimental results: microwires

Linearity of current-voltage curves

Numerous two probe measurements were performed in order to check the linearity of the current-voltage curves especially on the Al/Ti/Si system. Figure 4.4 shows the current-voltage characteristics from as-deposited microwires for different contact systems. This shows that linear and almost linear current-voltage characteristics were obtained for all contact systems. The highest current was obtained for devices with an Al/W/Ti/Si structure, while the lowest was for devices with Al/Ti/AlO_x/Si. The improvement of the current in devices with an Al/W/Ti/Si structure could be due to the improvement of conditions during the deposition of tungsten using an electron beam evaporator. It is well known that tungsten has a high melting point. Therefore, to evaporate the atoms from the tungsten target, a high current needs to be applied on the electron beam gun, which causes an increase in its temperature. As a result, the substrate temperature will also increase. The reduction of current for devices with an Al/Ti/AlO_x/Si metal structure could be due to an increase in contact resistance due to the reduction of tunnelling current.

It is also noteworthy that asymmetric current-voltage curves were observed in many devices. Generally, it is difficult to obtain identical contacts during fabrication. Thus, asymmetric curves could be attributed to difference between contacts at the two ends.
It is also important to note that some as-deposited devices exhibited nonlinear current-voltage characteristics. However, the ohmic contacts for these devices were obtained after annealing at temperatures above 300 °C, as discussed in the next section.

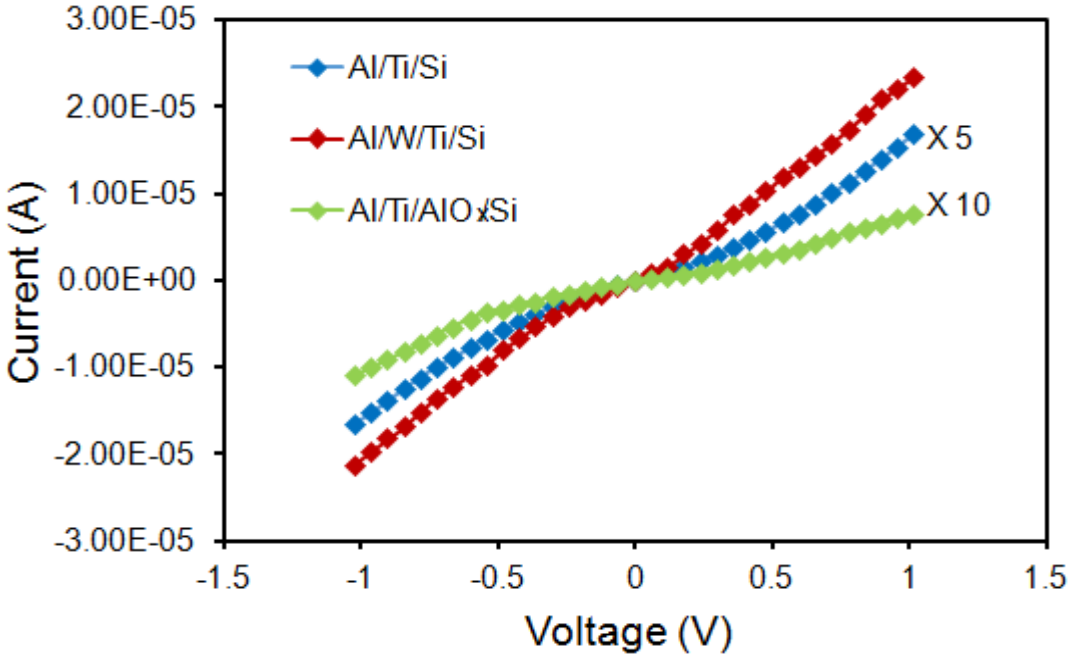

Figure 4.4: Current-voltage characteristics of as-deposited silicon microwires with contacts of different metallization structures (l=30 µm, w=2 µm, h=90 nm).

The effect of annealing on current-voltage characteristics

As mentioned previously, the devices were annealed at different temperatures in order to study the effect of annealing on contact performance and the thermal stability of the contact systems. Annealing was performed at 250 °C, 325 °C, 380 °C and 425 °C. The two probe measurements of the microwire devices with all metal systems show a three- to ten-fold increase in current after annealing at 250 °C compared to as-deposited devices. Further improvements were observed at 325 °C and 380 °C. However, a large reduction in current was observed for devices with an Al/Ti/Si contact structure after annealing at 425 °C. Similar behaviour, but with a lower reduction in current, was observed for devices with an Al/W/Ti/Si contact structure. In contrast, a slight increase in current was observed for devices with Al/Ti/AlO_x/Si after 425 °C annealing in comparison with that obtained at 380 °C. Figure 4.5 shows the effect of annealing temperature on the current-voltage characteristics for devices with different systems.

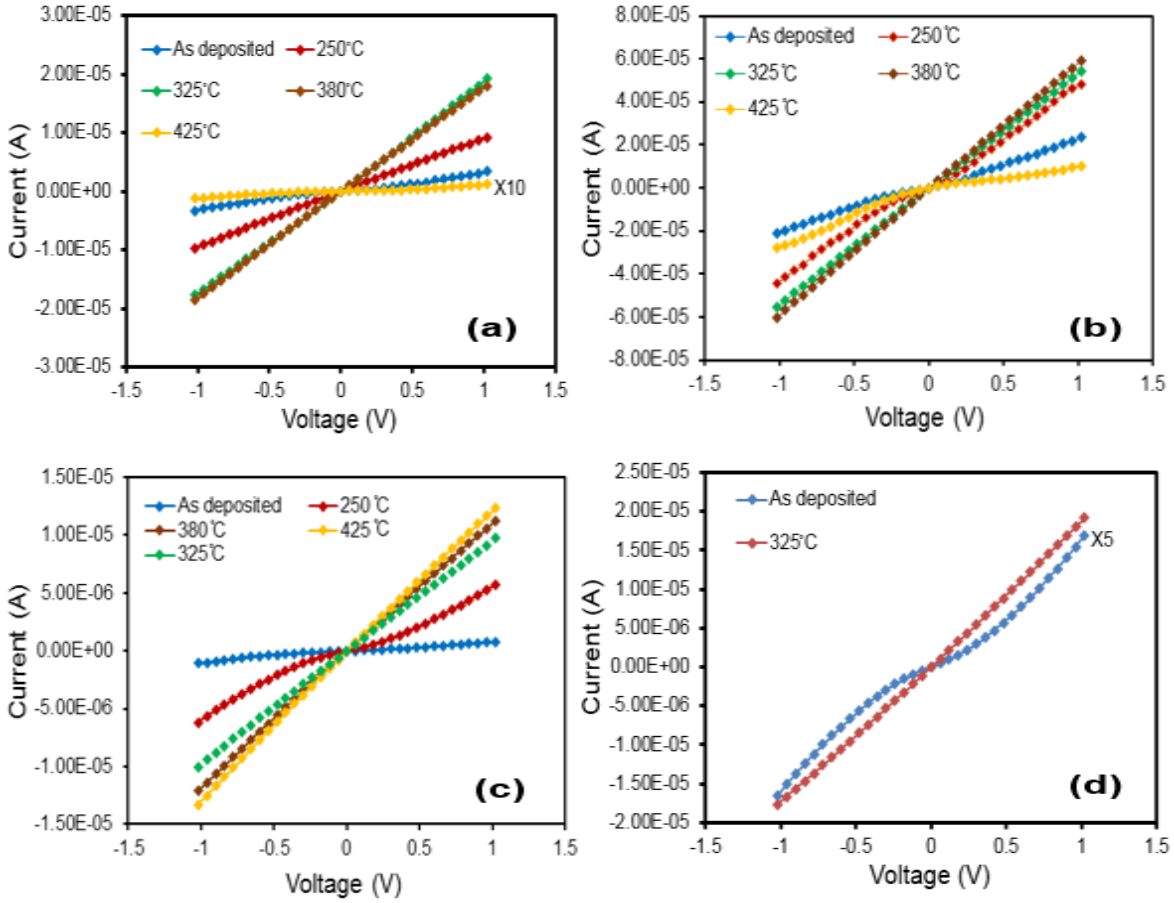

Figure 4.5: The effect of various annealing temperatures on the current-voltage characteristics of different contact systems: (a) Al/Ti/Si (Note that the current-voltage after 425℃ is after current is multiplied by 10 (orange colour)); (b) Al/W/Ti/Si; (c) Al/Ti/AlOx; (d) the effect of annealing temperature on linearity and performance of Al/Ti /Si (the as-deposited graph is after multiplying the current by 5).

The annealing treatment was also observed to improve the voltage-current linearity. Figure 4.5(d) shows an example of the effect of annealing on the linearity of current-voltage curves with respect to as-deposited devices. The linear curves were obtained after 325 ˚C annealing on devices with an Al/Ti/Si contact structure. The magnitude of current for the annealed devices at this temperature was more than five times higher compared with the as-deposited one, with the value of current value extracted at a voltage of 1 V.

The improvement of I-V characteristics after annealing at certain temperatures can be explained by the improvement of the interface between the metal system and the silicon. Organic residues at the interface could be removed after annealing at 250 °C. While a further increase in temperature reduces the metal defects and improves the chemical reaction at the metal-semiconductor interface and hence, dissolves the native oxide, which in turn leads to lower contact resistance. Upon annealing at a temperature higher than 400 C, the aluminium starts to react with the underlying titanium and form $TiAl_3$ compounds, which might diffuse into silicon and cause degradation in performance.

Results for contact resistance and specific contact resistivity

The multiwire test method (transfer length method) was applied in this research to extract the contact properties of silicon microwire devices. This method is described in the previous section. In this section, an example of the experimental measurements of contact resistance and specific contact resistivity using the multiwire test method is described first, and the contact properties of different metal structures are then summarised.

The current-voltage characteristics of microwire devices with different lengths for various devices with Al/Ti/Si are shown in Figure 4.6(a). The total contact resistance as a function of microwire length contact system was then calculated and the results are plotted in Figure 4.6(b). The data were extracted from these devices after annealing at 325 °C. The value of contact resistance is calculated at l=0 and is about $R_C = \frac{R_T}{2}\Big|_{l=0} = 3.25\ K\Omega$; while the value of the transfer length is obtained at R_T=0 and equals $L_T = \frac{6.50}{2\ X\ 1.77} = 1.83\ \mu m$. The sheet resistance is $R_{sh} = w\ \text{X}\ 1.77 = 2\ \text{X}\ 1.77 = 3.54\ K\Omega/\square$, the specific contact resistivity is $\rho_C = R_{sh}L_T^2 = 1.18\ \text{X}\ 10^{-4}\ \Omega\text{cm}^2$. The specific contact resistivity after applying different annealing temperatures and for different contact systems as defined earlier was then extracted. The results are summarised in Figure 4.7. The devices with Al/W/Ti/Si exhibit the lowest specific contact resistivity after deposition, while the devices with Al/Ti/AlOx/Si exhibit a relatively high value of specific contact resistivity due to the presence of aluminium oxide at the interface between the metal and semiconductor.

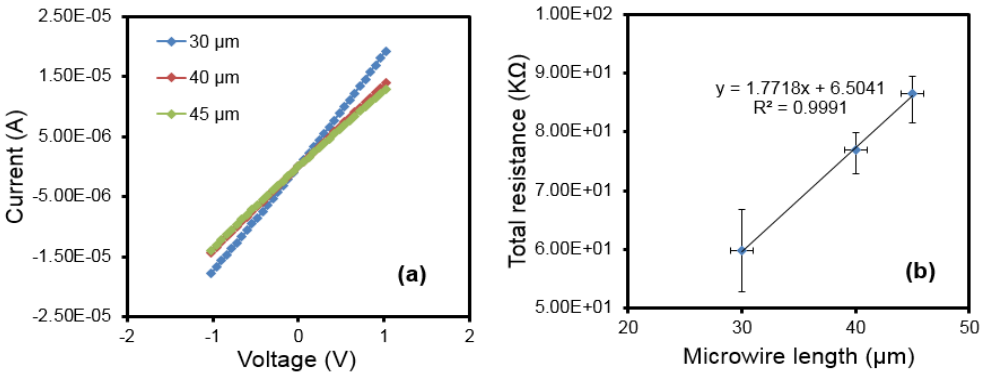

Figure 4.6: (a) Current-voltage characteristics of microwire devices with different lengths; (b) total contact resistance as a function of microwire length (Al/Ti/Si contact system, w=2 µm, doping >3.5 X 10 ^{18} cm^{-3}).

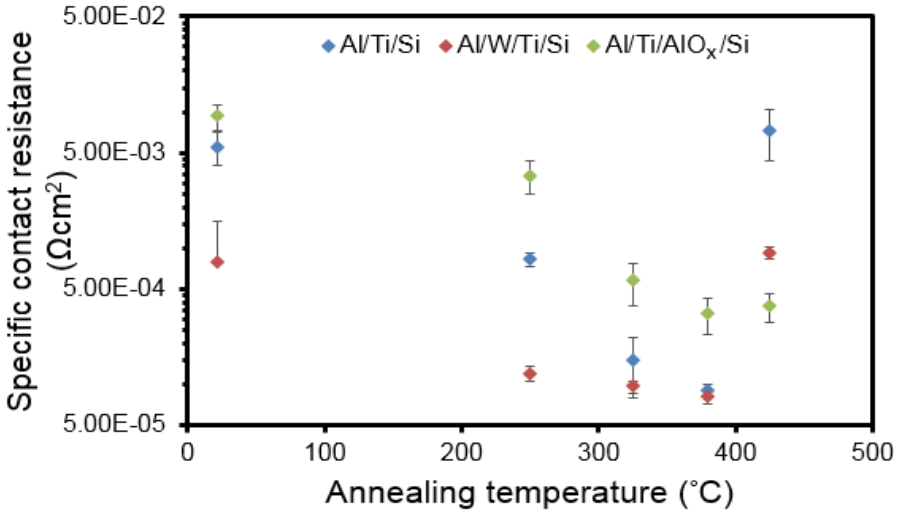

Figure 4.7: Specific contact resistivity as a function of annealing after various annealing temperatures.

In all systems, the specific contact resistivity is reduced by roughly three to five times after annealing at 250 °C with respect to as-deposited ones, which could be attributed to the removal of some organic residue at the interface which may have been formed during metal pattern. A greater reduction of specific contact resistivity was found after 325 °C and 380 °C annealing, which could be attributed to the improvement of the interface between titanium and silicon. The values of specific contact resistivity for devices with an Al/Ti/Si contact structure increases dramatically after annealing at 425 °C, which could be due to the fast diffusion of $TiAl_3$ into the silicon. The Al/W/Ti/Si contact system also exhibited a value high of specific contact resistivity after 425 °C annealing, but this value is still relatively much lower than that of Al/Ti/Si due to the presence of the tungsten barrier which reduces the diffusion rate of aluminium into titanium. However, instability in these metal contact systems occurs at temperatures lower than those reported in the literature [16], which are usually higher than 450 °C. This could be due to the error in the reading of the temperature by the pyrometer, as described in section 3.5.

In contrast, the specific contact resistivity of the Al/Ti/AlO_x/Si system continues to decrease after annealing at 425 °C, which indicates that AlO_x acts as a diffusion barrier and prevents the $TiAl_3$ from interacting with the silicon. However, this needs more investigation to determine whether or not AlO_x reacts to the aluminium titanium compound as a function of time and temperature.

Choice of contact system

A simple comparison between Al/Tl/Si, Al/W/Ti/Si and Al/Ti/AlO_x/Si shows that Al/W/Ti/Si has the lowest specific contact resistivity. However, the contact performance is degraded at an annealing temperature of 425 °C. Thus a thicker tungsten layer could slow the degradation at this level of annealing. However, it is always difficult to deposit a thick tungsten layer in an electron beam evaporator, since a high current is required to melt the

tungsten pellet and thus a high vacuum is needed to prevent failure during deposition. The Al/Ti/Si system exhibits a comparable specific contact resistivity to that of Al/W/Ti/Si. However, it has been found in this research that this system is unstable at an annealing temperature of 425 °C. The Al/Ti/AlO_x/Si system is stable at 425 °C; however, it exhibits the highest specific contact resistivity. In addition, the use of an insulating layer at the interface modifies the height of the Schottky barrier and careful selection of the insulator and its thickness is needed before it can be inserted. The choice of contact system should be based on device applications and requirements. In this research, the Al/Ti/Si system was selected as the contact system for silicon nanowires due to its low contact resistance and ease of deposition by electron beam evaporator.

4.2.5.2 Experimental results: nanowires

As mentioned previously, two methods were used to extract the properties between the contacts and a nanowire in cases where the contacts were placed directly on the nanowire: the multiwire test method (transfer length method) and the four probe method.

An experimental illustration was applied as an example, in order to compare the contact resistance values measured using these two methods. Since the nanowires could have either a trapezoidal or triangular cross-section, the value of the cross section of the nanowire was used instead of thickness. The measurements were performed on silicon nanowire with a perimeter of approximately 460 nm. The measurements were performed for devices with the Al/Ti/SiNWs contact system and after post-metallization annealing in forming gas at a temperature of 380 °C for 120 sec.

In the multiwire test method, the nanowire had lengths of 17.5, 21 and 27 µm. The total resistance as a function of length for fifteen devices is shown in Figure 4.8. The average value of contact resistance is $R_c = \frac{33.74}{2} = 16.87$ KΩ ; the average transfer length value is $L_T = \frac{33.74}{2\ x\ 10.53} = 1.6$ µm ; and the measured resistivity of the nanowire is $\rho_{2s} = 10.53\ \text{X}\ A = 10.53\ \text{X}\ 10^7\ \text{X}\ 12.5\ \text{X}\ 10^{-11} = 0.013$ Ωcm. This value of resistivity measured using this method is approximately twice as high as the 0.007 Ωcm measured using the dual configuration technique (see section 3.2.4). The specific contact resistivity was then calculated by generalizing the nanowire transmission model in circular cross section [18] to arbitrary cross-section. Therefore, the specific contact resistivity is given as follows:

$$\rho_C = \frac{L_T^2 P_i \rho_{eff}}{A} \tag{4.13}$$

where P_i is the perimeter of nanowires, A is the nanowire cross section, ρ_{eff} is the measured resistivity of nanowires, and L_T is the transfer length. The value of specific contact resistivity obtained using this method was approximately 1.17 X 10^{-4} Ωcm^2.

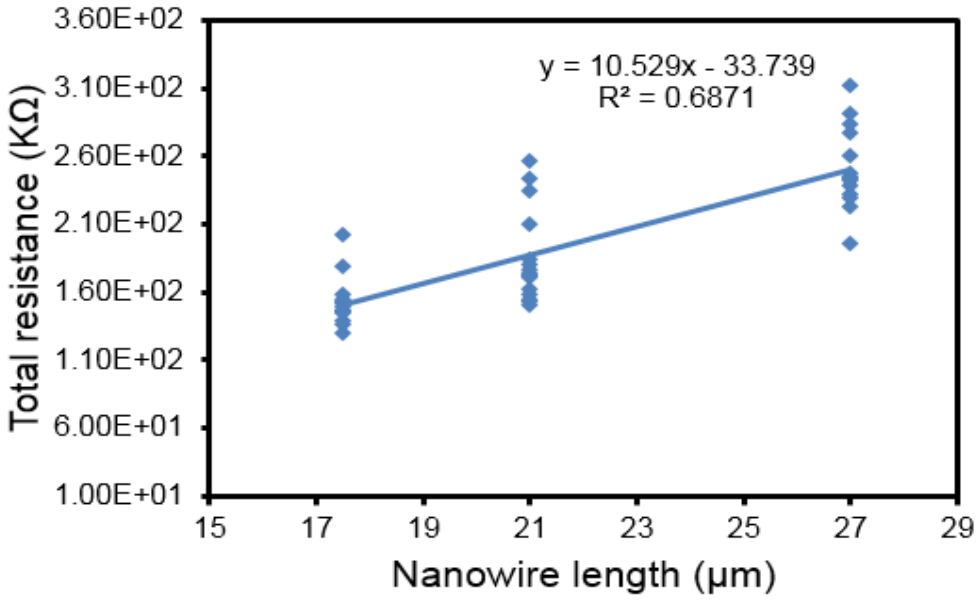

Figure 4.8: The total resistance as a function of nanowire length.

In the four probe method, the nanowire resistance was first measured between the inner two probes and was calculated using equation 4.6. The average value of nanowire resistance was about 153 KΩ. The resistivity of 0.006 Ωcm was obtained using this method, which is consistent with the value measured using the dual configuration method. The contact resistance was then measured using equation 4.8, and the average value of contact resistance was about 10.05 KΩ. The histogram in Figure 4.9(a) shows that the majority of the values of contact resistance are between 10-12 KΩ. The next step was to determine the transfer length. This was determined using $R_C = \frac{\rho_{eff} L_T}{A}$, and the approximate value of transfer length was 2.1μm. Once the transfer length was calculated, the resistivity of the nanowire was then measured. As the transfer length is larger than the contact length, thus the specific contact resistivity was determined using $R_C \times A_C$, where A_C is the effective contact area, and an average value of 9.6 X 10^{-5} Ωcm^2 was obtained. The histogram in Figure 4.9(b) shows that more than 70% of the values of specific contact resistivity are between 9 X 10^{-5} – 1 X 10^{-4} Ωcm^2. This value of specific contact resistivity is in general agreement with the values documented in the literature with n-type having the same range of carrier concentration [12, 17, 20].

A comparison between the values obtained using the transfer length method and the four probe measurements indicate that both measurements achieve the same value of specific contact resistivity. However, the four probe method provides more consistent results for resistivity with the dual configuration technique compared with the transfer length method. A possible reason of inaccuracy of measurements using the transfer length method relates to the difficulty in obtaining identical nanowires with the same thickness and width due to fabrication issues. Moreover the errors increase with very small contact areas where good ohmic contact is difficult to obtain using two contact methods.

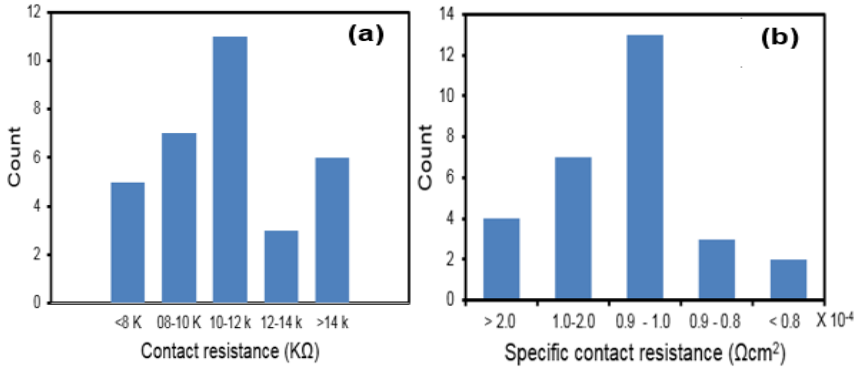

Figure 4.9: (a) Histogram of measured contact resistance of silicon nanowire using four probe method (b) histogram of measured specific contact resistivity of silicon nanowire using four probe method (Al/Ti/SiNWs, A= 12500 nm^2, doping >3.5 X 10 ^{18} cm^{-3}).

It should be noted that the above calculations assume that the entire perimeter of the nanowire was covered by metal. This assumption could be accepted, since the nanowire was expected to be suspended along the contact area due to the long etching time in BHF.

It should be noted that the contact resistance contributes to about 10 % of the total resistance when the contacts are placed directly on the nanowire, whereas it contributes less than 3 % of total resistance when the contacts are placed on a pair of bulk silicon connected to the silicon nanowire. This contact method will be used later in this thesis when the nanowires are used as sensors.

The dependence of contact resistance on the cross section of the nanowire was then studied using the four probe method. Figure 4.10 shows an increase in contact resistance with decreasing cross section area. This increase does not follow an inversely proportional trend as expected according to equation 4.13. The increase in contact resistance could be due to the decrease in carrier concentration with decreasing nanowire thickness, as described in sections 3.2 and 5.2. The increase in the surface roughness to width ratio with a decrease in the width of the nanowire could also cause the increase in contact resistance.

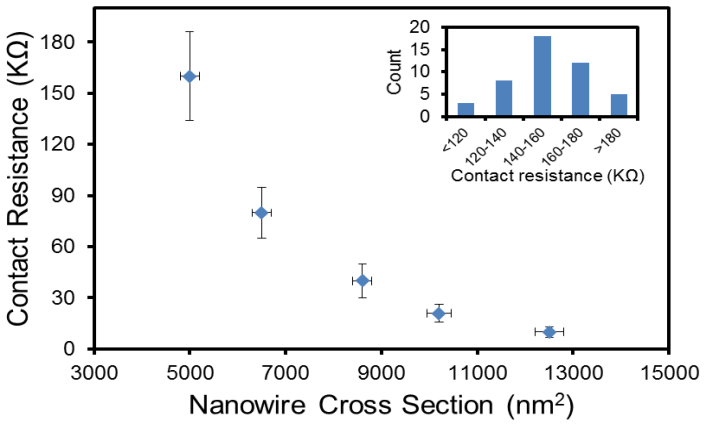

Figure 4.10: Measured contact resistance as a function of nanowire cross-section. Inset: histogram of measured contact resistance at $A = 5200$ nm^2.

4.3 Electrical characterisations of silicon nanowire

4.3.1 Effective electrical resistivity of a nanowire

Before the electrical resistivity of a silicon nanowire was measured, the resistivity of four ~100 nm thick square silicon templates on the SOI sample with 100 X 100 µm width were first measured using the van der Pauw method [21]. The area of the box was chosen to be large enough to avoid the variation in sheet resistance that may arise due to lithography misalignment. This test structure was used to ensure that an accurate value of bulk resistivity was measured. Then the electrical resistivity of the nanowire was measured using the four probe method as described earlier. The measured resistivity of the silicon template was between 0.0065-0.007 Ωcm. This value is considered as a reference value with which the nanowire's resistivity will be compared. The nanowire resistivity was then measured as a function of its diameter using the four probe measurements explained previously. The measured electrical resistivity is plotted against nanowire thickness in Figure 4.11.

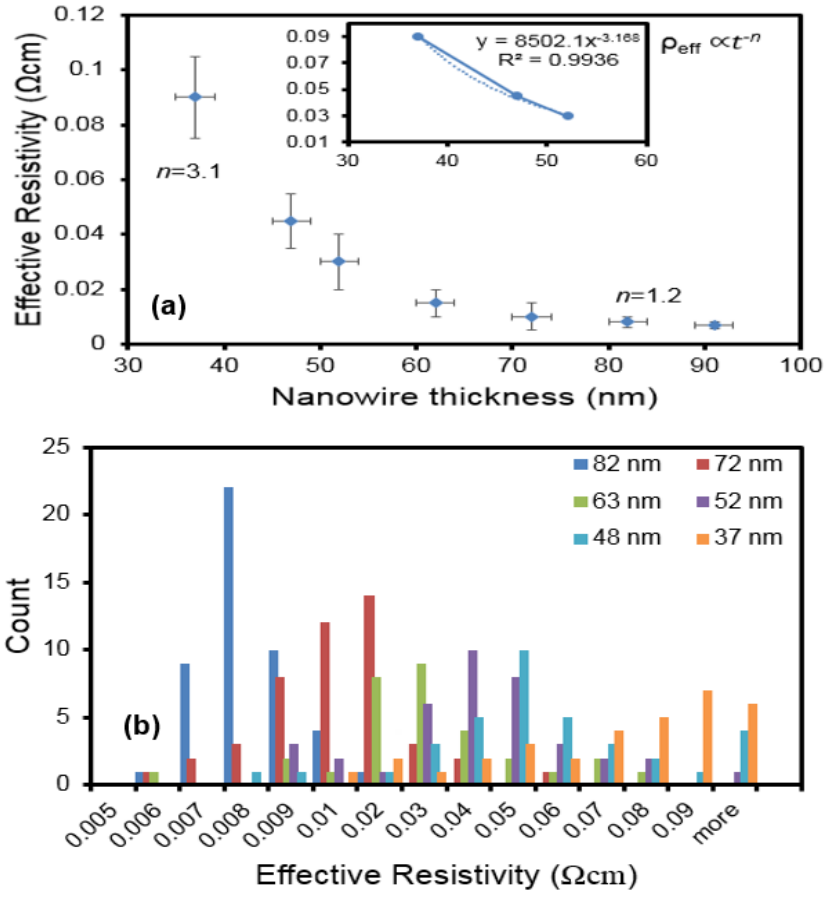

Figure 4.11: (a) The measured resistivity of silicon nanowires as a function of its thickness (the inset: the function that fits the measured resistivity when the thickness of nanowire is less than 60 nm) (b) Histogram of measured resistivity of silicon nanowire with different thicknesses.

Although the measured electrical resistivity should be independent of size, the results show that it is in fact dependent on size and follows the relationship $\rho \propto t^{-n}$. The value of the measured resistivity starts with a value close to that measured on the silicon template and n=0, and then the value of n increases to 1.2 when the thickness is between 65- 80 nm. It then increases to 3.1 when the thickness is between 40-60 nm. This increase in resistivity results could be attributed to: (i) the diameter-dependent carrier distribution [22, 23]; (ii) dielectric mismatch [24, 25]; (iii) quantum confinement[26]; (iv) size-dependent mobility [27, 28]; or (v) surface depletion due to interface traps [29]. The analytical models in the next chapter will show that the decrease in carrier distribution as a function of depth could cause the increase in measured resistivity in the regime where $n \approx 1.2$ while the surface depletion (due to the interface traps) in addition to the reduction of carrier concentration could cause the increase in the measured resistivity in the regime where $n \approx 3.1$.

The dependence of carrier concentration on the thickness of nanowire was calculated based on the measured electrical resistivity. The carrier density in silicon nanowire, as a function of thickness, is shown in Figure 4.12. This calculation data of a carrier concentration excluded the effect of mobility on the increase of resistivity. The influence of mobility on the electrical resistivity is estimated to appear at thickness less than 25 nm as will be shown in chapter five. It should be stated that several analytical models are described in chapter five so as to explain the increase in the measured resistivity of the nanowires.

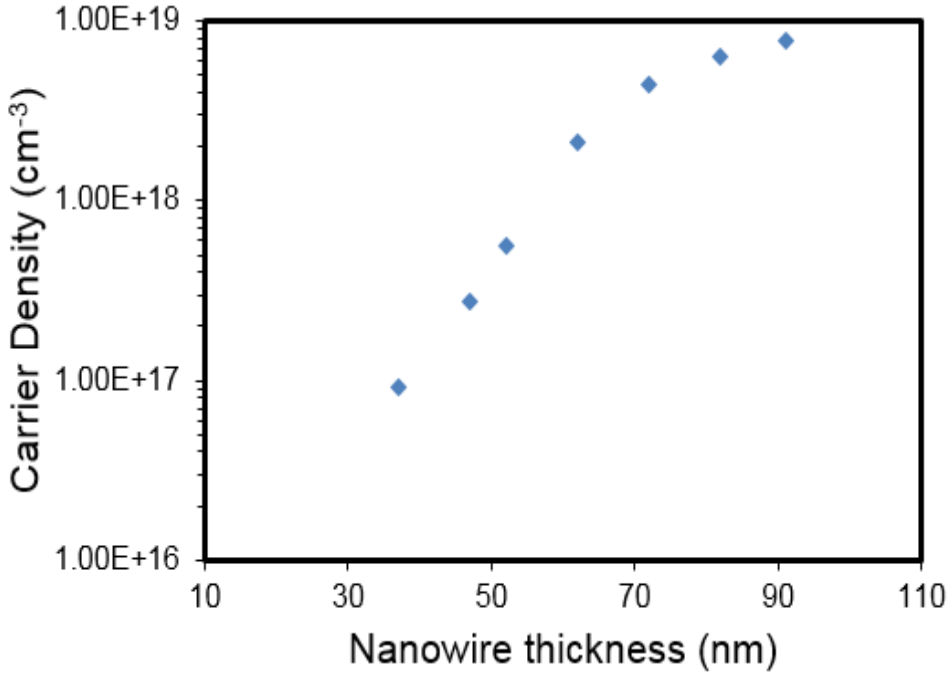

Figure 4.12: The effective carrier concentration in silicon nanowire as a function of nanowire thickness (this average calculated data is based on the measured resistivity in Figure 4.11).

4.3.2 Nonlinearity behaviour of current-voltage curves in four probe measurements

As mentioned previously, the electrical resistivity of the silicon nanowire was measured using the four probe method. The measurements were performed when a linear relationship was obtained between the dropped voltage between the inner two probes and the applied current at the outer two probes (Figure 4.13). However, in many measurements, nonlinear, non-exponential current-voltage characteristics were observed. These were largely observed in moderately doped devices with a doping level of about 5 X 10^{17} cm^{-3} with a thickness less than 45 nm. Some heavily doped nanowires with doping levels of about 5 X 10^{18} cm^{-3} with thicknesses less than 70 nm also exhibited nonlinear current-voltage characteristics. However, the nonlinearity of these devices was weaker than that of moderately doped devices.

Nonlinear current-voltage curves have been reported in many high aspect semiconductor nanostructures [30-34]. The reason for this nonlinear behaviour could be due to the presence of a Schottky barrier at the interface, surface roughness and backscattering [30], the depletion of free carriers due to surface states [35, 36], or defects in silicon nanowire and traps at the silicon/silicon dioxide interface [31, 32, 35]. In these measurements, the effect of the Schottky barrier should be negligible since the measurements were performed using the four probe method which eliminates the contribution of contact resistance between the nanowire and contacts.

In this study, certain experimental data for current-voltage characteristics are presented and an attempt is made to fit this data with adequate functions which may help to give an explanation for these observations.

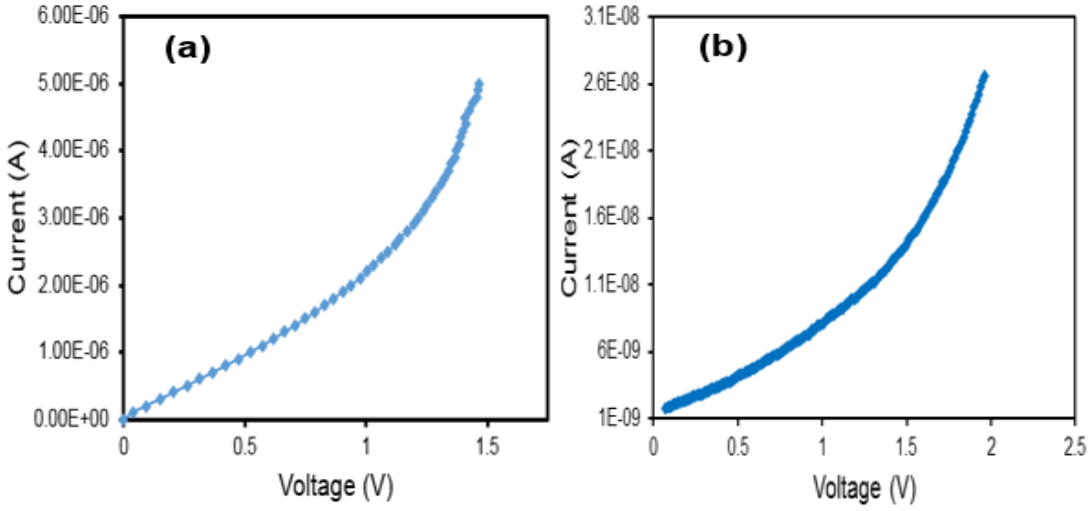

Figure 4.13: Nonlinearity examples of four probe current-voltage characteristics in four probe measurements (a) heavily doped nanowire n > 3.5 X 10 ^{18} cm^{-3}, t= 65 nm (b) moderately doped nanowire 1x $10^{17}cm^{-3}$ < n < 1X 10^{18} cm^{-3}, t= 45 nm.

The fitting functions, in addition to the analytical models described in the following chapter, may broaden understanding of the finding reported. This nonlinear behaviour in heavily doped (n > 3.5 X 10 ^{18} cm^{-3}) and moderately doped (1 X 10^{17}cm^{-3} < n < 1 X 10^{18} cm^{-3}) nanowires could originate from two different sources. Thus, it is useful to discuss both cases separately.

Heavily doped nanowires

A closer look at the current-voltage characteristics shown in Figure 4.13(a) indicates that the graph can be divided into two regimes: regime (A) at a small voltage, less than 1.2 V where the current-voltage response follows a linear relationship $I \propto V$; and regime (B) where the current-voltage response follows a nonlinear relationship $I \propto V^{\alpha}$, at a voltage higher than 1.2 V, the value of $\alpha = 2.84$ as shown in Figure 4.14. This fitting indicates that the space charge limited current (SCLC) could be a possible explanation for this behaviour [34, 36]. This space charge effect usually occurs in insulating materials or in low doped semiconductors when the injected charge exceeds the free carriers inside the material[36, 37]. It requires the formation of ohmic contact at least on one of the contacts, and the electrical current at large voltages obeys the power law of voltage, $I = V^{\alpha}$ [37]. There are several reasons for the space charge limited current effect to occur in these heavily doped nanowires. Firstly, large surface roughness may be formed during the anisotropic wet etching of silicon. Secondly, a large number of oxide traps or defects may be incorporated in the silicon nanowire during the fabrication process. Therefore, in order to investigate whether or not the observed nonlinearity of current-voltage characteristics is due to the space charge limit effect, the current-voltage measurements were performed at variable temperatures of 25 °C, 75 °C and 125 °C. The temperature measurements are useful to determine the change in the value of the exponent α with temperature, and thus the number of traps injected into the nanowire. The current-voltage curves at all temperatures exhibit linear characteristics at low bias voltage and power law characteristics at large bias voltage.

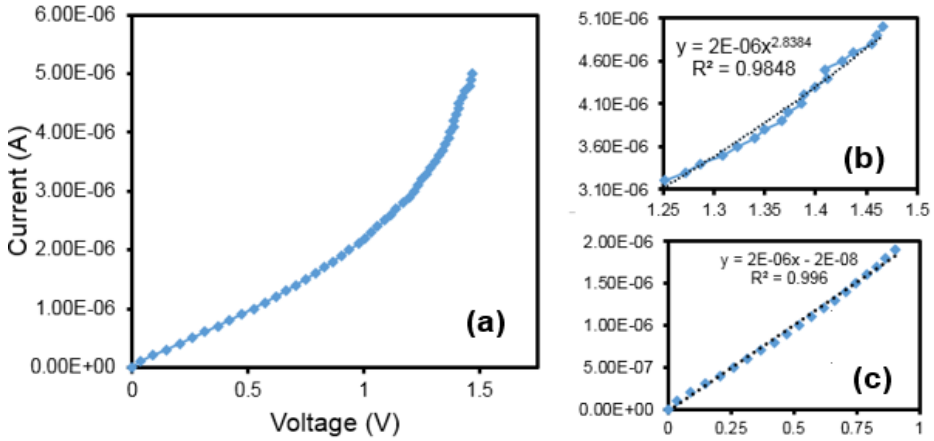

Figure 4.14: (a) Four contact current-voltage characteristics of a heavily doped silicon nanowire: (b) power fits to the nonlinear regime in (a), (c) linear fits to the ohmic regime in (a).

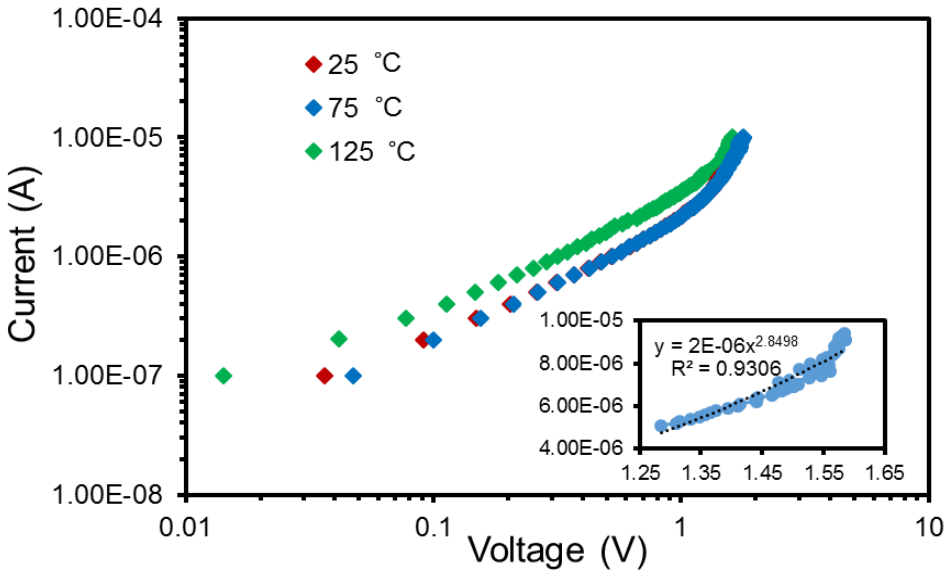

Figure 4.15: Temperature dependent four probe current-voltage characteristics of a heavily doped nanowire (the inset: power fits to the nonlinear regime at 125℃).

As for the linear regime, the linear parameter has the same value at 25 °C and 75 °C, while it increases at 125 °C. As for the power law regime, the exponent parameter α has almost the same value at all temperatures, which indicates that α is a temperature independent parameter. This suggests that the standard space charge limited current (SCLC) model is not responsible for the observed nonlinearity at large voltages [34, 35, 37].

In order to investigate this nonlinearity further, the electrical measurements were performed after annealing the samples in forming gas at 380 °C for 120 sec in a rapid thermal processing (RTP) system. The current-voltage curves before and after annealing shows a reduction of the value of parameter α after annealing with respect to the value before annealing. The value of $\alpha = 2.84$ before annealing and became $\alpha = 1.49$ after annealing (Figure 4.16). The annealing step could reduce the interface and the oxide traps. Therefore, the reduction of the value of parameter α after annealing could be attributed to the improvement in the quality of the silicon nanowire interface after annealing. In some devices the value of α was reduced to 1 after annealing, Figure 4.17 shows a good fit linear four probe current-voltage curve was obtained after device annealing, where the value of $\alpha = 1.88$ was before annealing.

Noticeably, the nanowire resistance was reduced after thermal annealing (shown in the linear part of the graphs in Figure 4.14, 4.16 and 4.17). The resistance was $R = \frac{1}{2\,X\,10^{-6}} =$ 0.5 MΩ before annealing and became $R = \frac{1}{3X\,10^{-6}} = 0.33$ MΩ after annealing; indicating that the effective area of silicon nanowire has increased due to the reduction of traps at the nanowire interface after annealing.

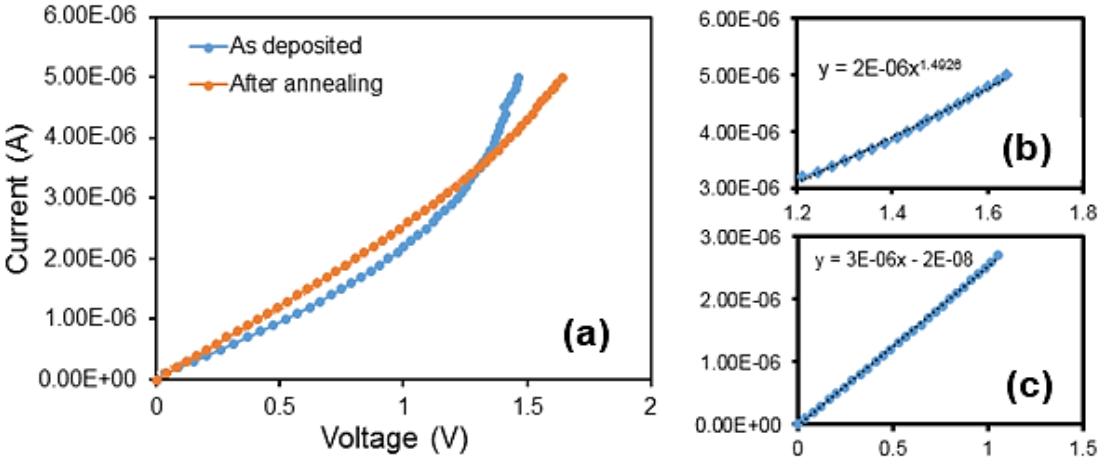

Figure 4.16: The four probe current-voltage characteristics of a heavily doped nanowire before and after annealing (b) the power fits to the nonlinear regime of the nanowire after post-metallization annealing (c) the linear fits to the linear regime of the device after post-metallization annealing.

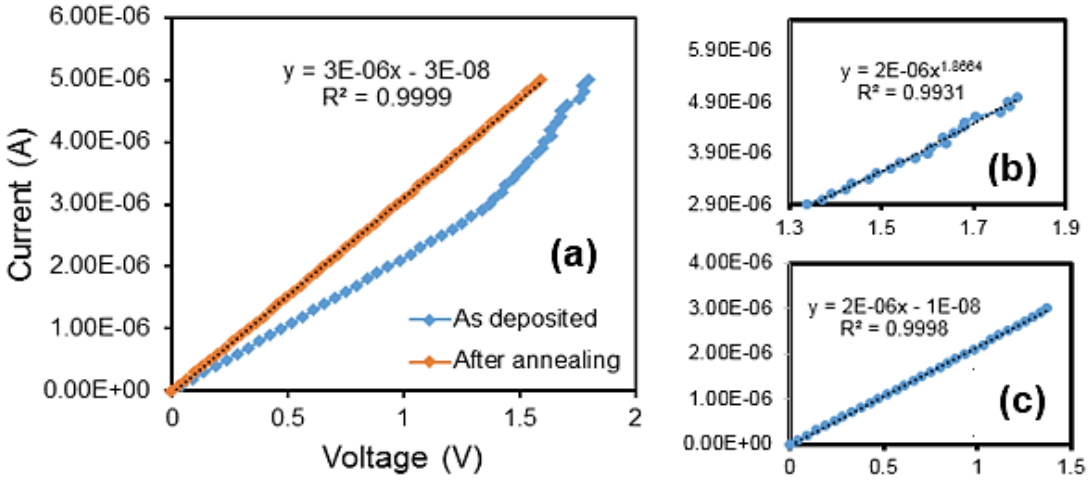

Figure 4.17: (a) A linear four probe current-voltage characteristics of silicon nanowire after annealing (b) and (c) are the nonlinear and linear regimes of the curve before annealing respectively.

Moderately doped nanowire

Figure 4.18 shows the nonlinear regime of the graph in Figure 4.13(b). The electrical current in the nonlinear regime exhibits the power law of voltage, $I = V^{\alpha}$. The value of the parameter α is approximately 2.31, although it should be noted that the current-voltage characteristics provided here were for the samples after 400 °C annealing in forming gas for 120 sec using rapid thermal processing system. In order to investigate the change in exponent α with temperature, the current-voltage measurements were performed at temperatures of 25 °C, 75 °C and 125 °C. A reduction in the value of α was observed with increases of temperature, with α approximately 1.19 at 75 °C and 1 at 125 °C. These results indicate that the space charge limit current could be dominant type of transport in the

nonlinear regime. If the space charge limit effect is present, the trap concentration can be estimated using the following formula [38]:

$$N_t = \frac{2\varepsilon V_c}{qL^2} \tag{4.14}$$

where V_c is the crossover voltage, which can be defined as the voltage where the electrical current is independent of temperature. The value of V_c can be estimated from the plot in Figure 4.19 and is approximately 10 V. The estimated trap concentration is about 4.1 X 10^{12} cm^{-3}. This value is much lower than the impurity concentration in the nanowires which could indicate that the space charge limit cannot itself explain the nonlinearity of the current-voltage characteristics [34, 36]. Further study is needed to understand this behaviour.

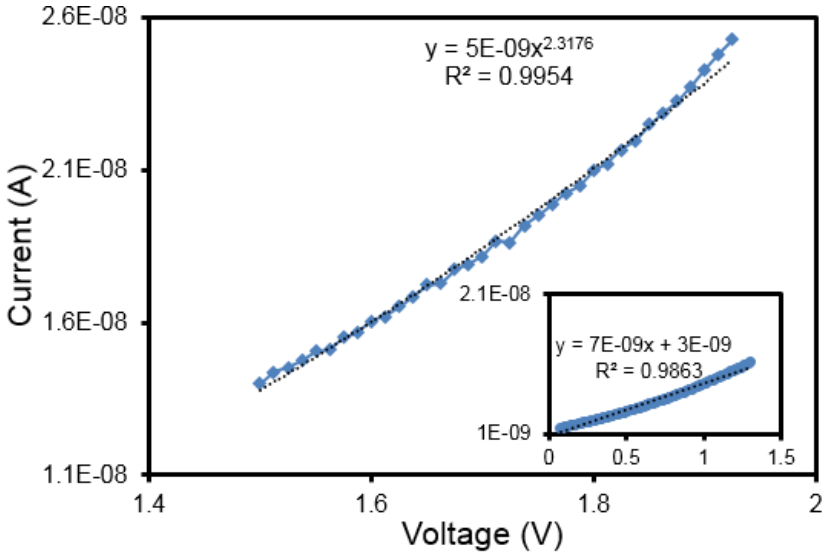

Figure 4.18: The power law fits to the nonlinear regime of the device in Figure 4.13(b) (the inset: the linear fits to the ohmic regime for the same device).

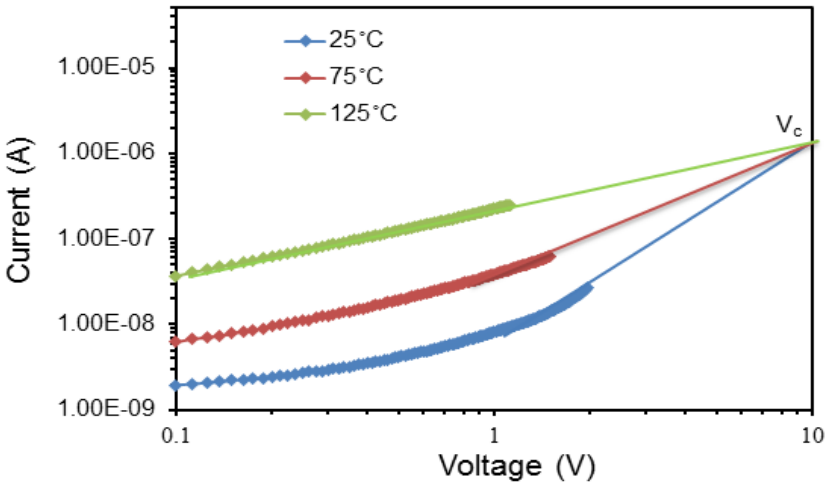

Figure 4.19: Temperature dependent four probe current-voltage characteristics of a moderately doped nanowire (V_c is the crossover voltage).

It should be noted that the silicon nanowire surface is not atomically smooth and the sidewall roughness was observed to be about 2.5 nm (see section 3.4.3.1). Moreover, the oxidation of the silicon nanowire was observed to be nonuniform along its length and across its thickness (as reported in section 3.3.3.2) which indicates that the surface roughness of silicon nanowire tends to increase after the dry oxidation step. The next chapter attempts to model the influence of interface traps, surface scattering and surface roughness on the properties of triangular silicon nanowires, which could help in obtaining a better understanding of these results.

4.4 Summary

This chapter presents details of the electrical transport of a silicon nanowire and its contact system. It mainly describes the issues related to the formation of the ohmic contact and the electrical properties of the silicon nanowire.

With regard to the ohmic contact aspect, the stability of the contact structure and the contact resistance are investigated. As for thermal stability, several contact systems namely Al/Ti (100/70), Al/W/Ti (100/20/70) and Al/Ti/AlO_x (100/70/0.6) to silicon and silicon nanowire are tested at different annealing temperatures ranging from 250 °C to 425 °C. The Al/Ti system fails rapidly at the annealing temperature of 425 °C due to the diffusion of aluminium compound into the silicon. The insertion of a 20 nm thickness of tungsten between the aluminium and titanium reduces the failure rate, but it does not completely prevent the diffusion of aluminium compounds into silicon. Whereas inserting a very thin layer of aluminium dioxide between the titanium and silicon acts as a diffusion barrier that prevents this diffusion. As for contact resistance, the transfer length model and four probe methods are used to measure the specific contact resistivity and contact resistance for the above systems to a thick silicon layer and the silicon nanowire. Al/W/Ti is found to have

the lowest contact resistance to silicon, while Al/Ti/AlO_x exhibits the highest contact resistance. The contact resistance is further reduced after annealing at a temperature of about 380 °C. Ohmic and almost ohmic current-voltage curves are obtained using the above contact systems. This chapter also compares the properties of two contact methods: in the first method the two contacts are placed on thick silicon and a nanowire is connected between them; and in the second method the contacts are placed directly on the nanowire. The contact resistance in the former method is found to contribute to less than 3% of the total resistance, while it is found to contribute to about 10 % of the total resistance in the latter. It has also been found that, when the contacts are placed directly on the nanowire, the contact resistance increases by a factor of four while the cross-section is reduced from about 12500 nm^2 to about 4800 nm^2.

For the electrical properties of a silicon nanowire, the electrical resistivity is measured by using the four probe method. The measured electrical resistivity of nanowires is found to be size dependent and follows the relationship $\rho \propto t^{-n}$. The increase in resistivity could be attributed to surface depletion due to interface traps in addition to the reduction of carrier concentration as a function of silicon depth.

In this chapter, nonlinear four probe current-voltage characteristics are observed in heavily and moderately doped silicon nanowires. The temperature measurements of heavily doped devices demonstrate that the nonlinearity is temperature independent, while in moderately doped devices the nonlinearity is temperature dependent. The improvement of nonlinearity of heavily doped devices, after annealing, indicates that the origin of the nonlinearity is possibly due to a large density of traps, which is reduced after annealing. However, further studies are required for a comprehensive understanding of the nonlinearity behaviour in the four probe measurement.

While the fabrication process of silicon nanowires is fully discussed in chapter three, the electrical properties are investigated in chapter four with various interesting behaviours observed. The successful use of these nanowires in applications such as; chemical sensing, nanoelectronics, solar cells and thermoelectric devices requires a full-understanding of the observations reported in chapter four. This is essential to enable the precise control of these nanowire properties so it can be used in the above mentioned applications. Hence, chapter five will introduce a range of models which could help in understanding the observation noted in this chapter.

4.5 Future work

The work in this chapter reveals some fundamental properties of top-down triangular silicon nanowire. Further experimental measurements and theoretical studies are essential to understand these properties.

In section 4.2.5.2 the measured contact resistance is plotted as a function of the contact area between the nanowires and metal contacts, and the results indicate that contact resistance increases exponentially with decreasing contact area. However, this increase does not represent the true trend as the effect of carrier concentration and surface charge at the semiconductor surface are not taken into account. Thus, it is important to model the impact of these two parameters on the contact resistance to reveal the effect of the contact area on contact resistance.

In section 4.3.1 the measured electrical resistance is reported to increase with the decreasing thickness of the nanowire. Understanding this phenomenon requires further experimental measurements and theoretical studies. A list of suggested future work that could help in the understanding this observation:

a- Capacitance-voltage measurements are required to extract the trap density at the interface of silicon nanowire, which may provide further understanding of the role of surface properties on the resistivity of nanowire.
b- Mobility measurements may help to understand the effect of surface scattering and geometrical effects on the electrical properties of nanowire. The capacitance-voltage technique and Hall effect in nanowire have been recently reported to measure the mobility in nanowire for further reference [39-42].
c- The impact of dielectric material on the electrical resistivity is needed.
d- Noise measurements

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Chapter 5

Analytical Modelling of Resistivity in Triangular Silicon Nanowires

5.1 Introduction

At the microscopic level, Ohm's law is described by a simple relationship between the electrical resistance and the dimensions and resistivity of the material, as follows:

$$R = \rho \frac{l}{A} \tag{5.1}$$

where R is the electrical resistance of the material, l is its length, A is its cross section and ρ is the electrical resistivity which is a size-independent property. Generally, resistivity is given by:

$$\rho = \frac{1}{\sigma} = \frac{1}{q\mu n} \tag{5.2}$$

where σ is the electrical conductivity of the material, q is the magnitude of electronic charge, n is the carrier density, and μ is the electron mobility which is given by:

$$\mu = \frac{q\tau}{m} = \frac{q\lambda}{m^* v_{th}} \tag{5.3}$$

where τ is the relaxation time, λ is the electronic mean free path, m^* is the effective mass of the charge carrier, and v_{th} is the average velocity.

However, an increase of measured resistivity in the mesoscopic regime (the intermediate regime between the nano- and micro-regimes) with a decrease in the size of the nanowire has been reported in chapter four. This increase in resistivity has been observed mainly in nanowires with thickness less than 80 nm (Figure 5.1). As a function of size, the resistivity follows the relationship $\rho \propto t^{-n}$, where the value of n is 1.2 when the thickness is larger

than 65 nm and about 3.1 when the thickness is less than 60 nm. The increase in electrical resistivity in the mesoscopic regime has often been reported experimentally in many metallic and semiconductor nanostructures [1-3]. In this regime, where the surface to volume ratio is high, the increase in resistivity with decreasing size could be attributed to the following:

i. Diameter dependent carrier distribution [4, 5]: this mostly depends on the doping method. The doping incorporated by the spin-on-doping method which has been used in this research, can produce an inhomogeneous distribution of dopant, as seen in section 5.2.
ii. Dielectric confinement effect: it has been reported that the dielectric mismatch between the silicon nanowire and its coating oxide can increase the ionisation energy in the nanowire and decrease the free carrier density with decreases in the size of the nanowire [2, 3, 6, 7]. However, this effect could be lower in a triangular cross-section compared to a circular cross-section as documented in [8].
iii. Surface depletion due to interface traps: the interface charge at the silicon-silicon dioxide interface can create a depletion region at the interface, which reduces the effective conductive area inside the nanowire [9-11]. The interface charge effect increases with decreasing size of the nanowire due to the increase in the surface to volume ratio.
iv. Surface roughness and scattering: these effects have been reported in metallic and polycrystalline structures when the dimension of the structure is comparable or less than the electronic mean free path in the material [12, 13].
v. Segregation of dopants: the dopants can leave the silicon and become segregated in the silicon dioxide layer during thermal oxidation, and this segregation normally occurs in silicon doped with boron [14, 15].

It is difficult to interpret the increase in resistivity in terms of the involvement of a single parameter, since it could be attributed to various parameters. Therefore, understanding the apparent increase in resistivity with decreasing size entails a holistic examination of all possible effects that could lead to it.

The measured electrical resistivity is the sum of all possible effects:

$$\rho_{eff} = \rho_B \left(\frac{\sum_i \rho_i}{\rho_B} - (i-1) \right) \tag{5.4}$$

$$\rho_{eff} = \rho_B \left(\frac{\rho_{dop} + \rho_{dep} + \rho_{rough} + \rho_{sc} + \rho_{seg} + \rho_{dc}}{\rho_B} - 5 \right) \tag{5.5}$$

where ρ_B is the bulk resistivity, ρ_{dop}, ρ_{dep}, ρ_{rough}, ρ_{sc} and ρ_{dc} are the resistivities due dopant distribution, depletion effect, surface roughness, surface scattering, segregation effect and dielectric confinement respectively. The contribution of dopant segregation is

neglected in this study since the samples were doped with phosphorus atoms which have a low segregation coefficient.

The contribution of dielectric confinement needs special consideration and is largely affected by the location of the dopants and the geometry of the cross section. Thus, this effect is also not considered in this study. Thus, this study examines the role of dopant distribution, size effect mobility, surface depletion due to interface traps, and surface roughness, and then the models are used to fit the experimental results. Equation 5.5 can be rewritten as:

$$\rho_{eff} = \rho_B \left(\frac{\rho_{dop} + \rho_{dep} + \rho_{rough} + \rho_{sc}}{\rho_B} - 3 \right) \tag{5.6}$$

The analytical models are used in this research instead of numerical simulation because analytical simulation can give a general description of how the model behaves under certain conditions. However, numerical simulation is used in this study to support the analytical modelling when it is required to solve a differential equation for specific values.

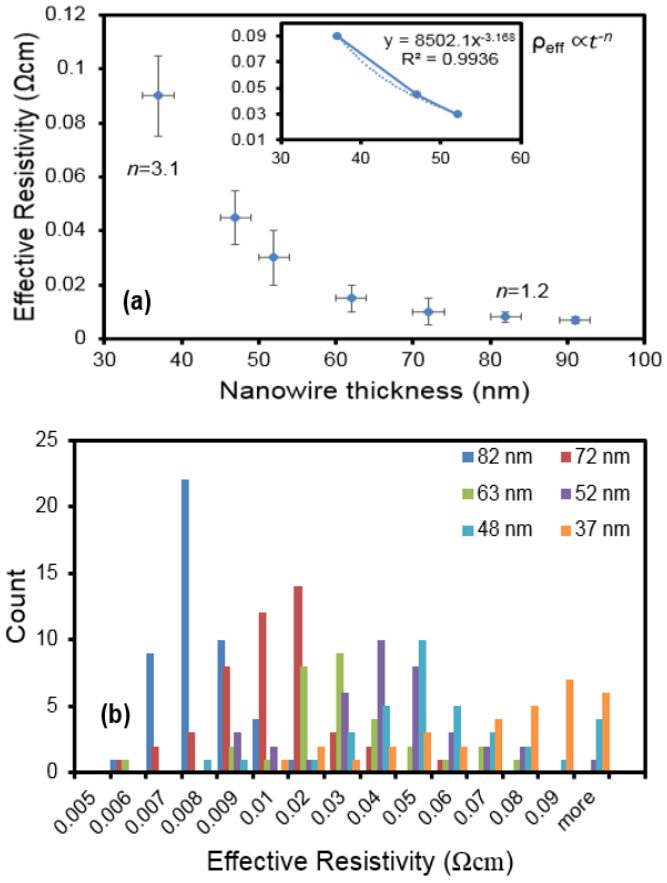

Figure 5.1: (a) The measured resistivity of silicon nanowire as a function of its thickness (inset: the function that fits the measured resistivity when the thickness of nanowire is less than 60 nm); (b) Histogram of measured resistivity of silicon nanowire with different thicknesses.

5.2 Effect of dopant distribution

The Spin-on-doping (SOD) method was used to introduce the dopant into the silicon substrate prior to the formation of silicon nanowire, as described in section 3.2. The impurity concentration profile in diffusive SOD is not constant, but instead follows a complementary error function or a Gaussian distribution depending on the way that the dopants are introduced. If the diffusion process is performed using a constant source of dopants, the dopant profile will follow a complementary error function, *erfc*. If the diffusion process is performed after the removal of the glass layer, then the dopant profile will follow a Gaussian distribution. In the fabrication process of silicon nanowire, the dopants were introduced into the silicon substrate using a constant source of dopants followed by a drive-in diffusion, to achieve homogeneity across the thickness of the silicon layer, doping after the removal of the glass layer, and the process also included subsequent annealing steps which could result in an unintentional redistribution of the dopants. Therefore, it is essential to accurately determine the dopant concentration and extract the corresponding electrical resistivity before investigating the other effects.

The thermal steps applied during the fabrication process of nanowire are as follows:

a. 975 ℃ for 300 sec in nitrogen with a constant source of dopant.
b. 1000 ℃ for 40 min in nitrogen/oxygen after the removal of the dopant source (drive-in), in addition to two other unintentional annealing steps, first at 930 ℃ for 30 min in oxygen and the second at 950 ℃ for 30 min in nitrogen/oxygen/nitrogen.

The first thermal annealing step is described in section 3.2, where a complementary error function is used to fit the experimental data (see section 3.2.4). Thus, in this section, the effects of the other thermal steps are calculated. The diffusion in these steps refers to drive-in since the annealing step was performed after the removal of the dopants. The dopant profile in each of these steps should follow a Gaussian function and can be estimated from [16]:

$$N(x,t,T) = \left(\frac{S}{\sqrt{\pi D(T)t}}\right) \exp -\left(\frac{x}{2\sqrt{D(T)t}}\right)^2 \tag{5.7}$$

where t is the diffusion time, D is the diffusion coefficient, x is the distance from the surface, T is the absolute temperature, and S is the total concentration of dopants per silicon area which results from the constant source step and is calculated from the constant source step by [16]:

$$S = 2N_s\sqrt{\frac{D(T)t}{\pi}} \tag{5.8}$$

where N_s is the concentration of dopant atoms at the surface. Since many subsequent annealing steps are applied, the $D_i(T)t_i$ product for each thermal step is calculated and added to give the total $(D(T)t)_{total}$ by:

$$(D(T)t)_{total} = \sum_i D_i(T)t_i \tag{5.9}$$

The impurity concentration at a certain depth can then be calculated using equation 5.7. The calculated impurity concentration as a function of depth is presented in Figure 5.2.

Once the impurity concentration has been determined, the impact of doping distribution on electrical resistivity can then be determined. Figure 5.3 shows the measured electrical resistivity after eliminating the effect of dopants, where the value of the exponent *n* reduces to 1.08 when the thickness of the nanowires lies between 65- 80 nm, and to 2.88 when the thickness lies between 40- 60 nm. This indicates that the doping effect alone cannot explain the increase in resistivity with the decreasing thickness of the nanowires.

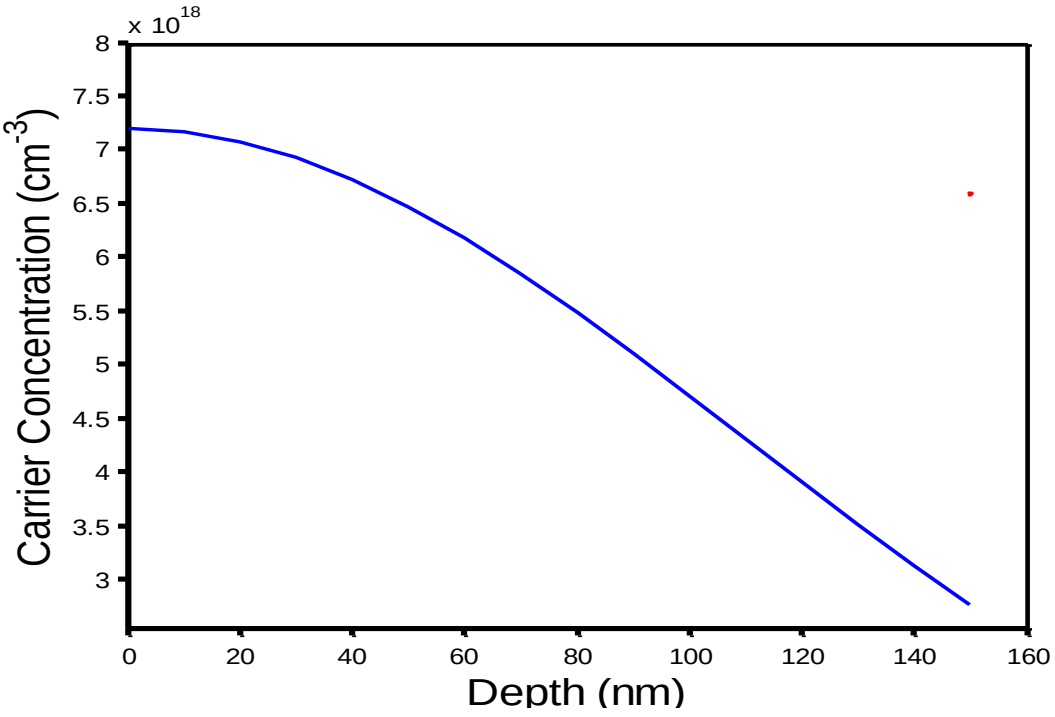

Figure 5.2: Modelling results for impurity concentration as a function of silicon depth

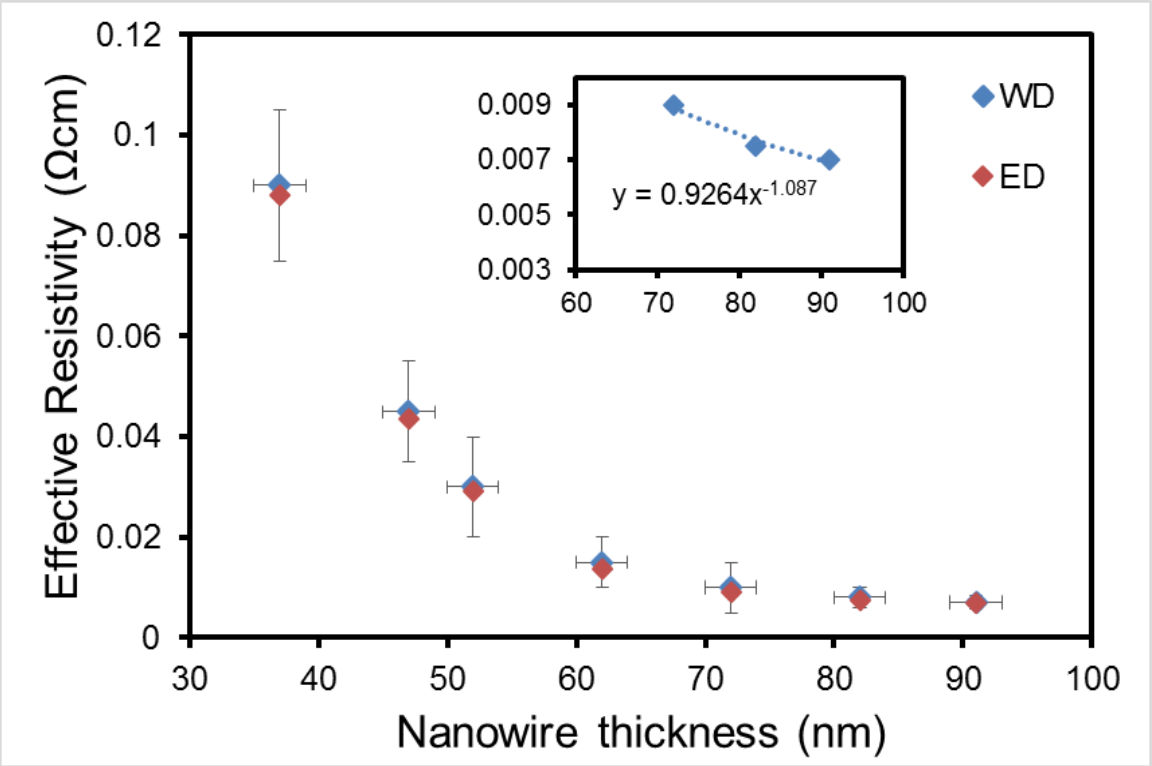

Figure 5.3: Resistivity as a function of the thickness of silicon nanowire before (WD) and after (ED) eliminating the effect of non-uniformity in impurity concentration (inset: the function that fits the measured resistivity after eliminating the doping effect for thicknesses of nanowire larger than 65 nm).

5.3 Surface-depletion due to interface traps

In nanostructures, as the surface to volume ratio increases, the surface plays a key role in determining the properties of nanodevices. In many applications, silicon dioxide is typically used to coat the surface of silicon based devices. Thus, the properties of the silicon-silicon dioxide interface will significantly influence the characteristics of devices.

There are two main types of charges associated with the silicon-silicon dioxide interface (Figure 5.4): First, charges inside the silicon dioxide, such as oxide trapped charge and mobile oxide charge; and secondly, charges at the silicon-silicon dioxide interface such as fixed oxide charge and interface trapped charge [16, 17].

Charges inside oxide:

Oxide trapped charge: this is created by broken silicon-oxygen (Si-O) bonds which may result from ionization radiation such as plasma processes, X-ray radiation or plasma bombardment. This charge could be positive or negative and can be distributed anywhere inside the oxide layer. It can be minimised by low-temperature annealing [16, 17].

Mobile oxide charge: contaminants such as potassium (K^+) or Sodium (Na^+) ions can move back and forth inside the oxide under a high electric field and during high temperature operations. This may cause instability in device performance [16, 17].

Charges at the interface:

Fixed oxide charge Q_f: This charge is positive and located within 3 nm of the silicon-silicon dioxide interface, and its density depends on orientation and oxidation conditions. Post oxidation annealing in nitrogen or argon is required to minimise the density of this charge. The "Deal triangle" is generally used to characterise the relationship between the density of fixed oxide charge and the oxidation temperature and post-oxidation annealing conditions [16-18].

Interface trapped charge Q_{it}: This trap is located at the silicon-silicon dioxide interface and is caused by the properties of the interface due to structural defects, or radiation or oxidation process defects. The density of this trap depends on orientation, and is 10^{10}-10^{12} $cm^{-2}eV^{-1}$ in the <100> orientation and it is ten times higher in the <111> orientation. This charge can be positive or negative. Annealing in hydrogen between 350-450℃ is normally used to minimise the density of this charge [16, 17, 19].

Oxide trap charge, mobile oxide charge and fixed oxide charge are better controlled using cleaning procedures and annealing conditions. Because the interface trap can act as a positive or negative charge and since it can interact directly with the silicon, it therefore has the most influence on device performance. In this study, the effect of interface charge on surface depletion in nanowires is investigated based on a previous study [9].

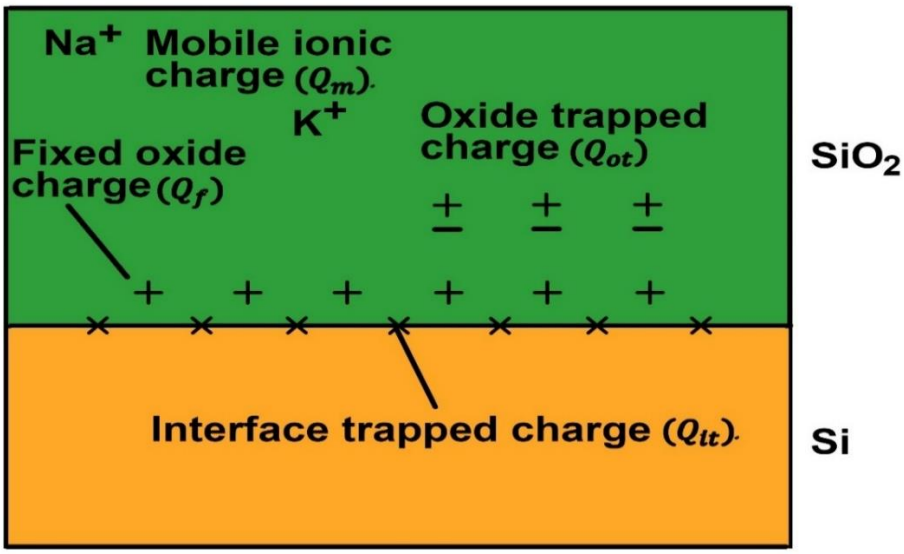

Figure 5.4: Charges associated with the silicon-silicon dioxide interface.

In this section, the aim is to study the effect of interface traps on the electrical resistivity of a silicon nanowire. Therefore, Poisson's equation should be solved to find the conductive area inside the nanowire. Poisson's equation is written [11, 20]:

$$\nabla^2\psi = -\frac{\varrho}{\varepsilon_s} \tag{5.10}$$

where ϱ is the charge density, ψ is the electrostatic potential and ε_s is the permittivity of silicon. In polar coordinates, equation 5.10 can be written in the following form:

$$\frac{1}{r}\frac{\partial}{\partial r}\left[r\frac{\partial\Psi(r,\theta)}{\partial r}\right]+\frac{\partial^2\Psi(r,\theta)}{\partial\theta^2} = -\frac{\varrho(r,\theta)}{\varepsilon_s} \tag{5.11}$$

In order to simplify the above equation, the behaviour of electrostatic potential near the corners was neglected. This assumption can be considered valid if the equipotential lines in the conductive area inside the nanowire are independent of the angle. In order to check the accuracy of this assumption, a silicon nanowire was modelled using the 3D TCAD solver to find the electrostatic potential and current density inside the cross section of the nanowire. The simulated nanowire had a triangular cross-section with a thickness of 80 nm. The applied gate voltage was fixed to -0.7 V, while the source/drain bias was 1.5 V and the oxide thickness was 7 nm. In the model, the Poisson equation and drift-diffusion models were solved self-consistently to determine the electrostatic potential and the carrier transport respectively. The electrostatic potential profile and current density of the simulated structures are shown in Figure 5.5, showing that the equipotential lines inside the conductive area of the cross section are rounded triangular or almost circular.

The circular equipotential lines indicates that the electrostatic profile inside the nanowire is independent of angle. Therefore, under this condition $\Psi(r,\theta) \approx \Psi(r)$, and Poisson's equation can be reduced to [20]:

$$\frac{1}{r}\frac{\partial}{\partial r}\left[r\frac{\partial\Psi(r)}{\partial r}\right] = -\frac{\varrho(r)}{\varepsilon_s} \tag{5.12}$$

The model further assumes a circular shape of the nanowire with an area equal to the area in triangular shape. This assumption would be valid if the value of the electrostatic potential and current density inside the conductive area in the circular shape is equal to that inside the conductive area inside the triangular shape. The TCAD simulation results in Figure 5.6 show the electrostatic potential and current density inside triangular and circular with the same cross-section area. The values of current densities and electrostatic potential are approximately the same in both structures (although about 1.15 higher in circular cross section which could be due to the corner effect).

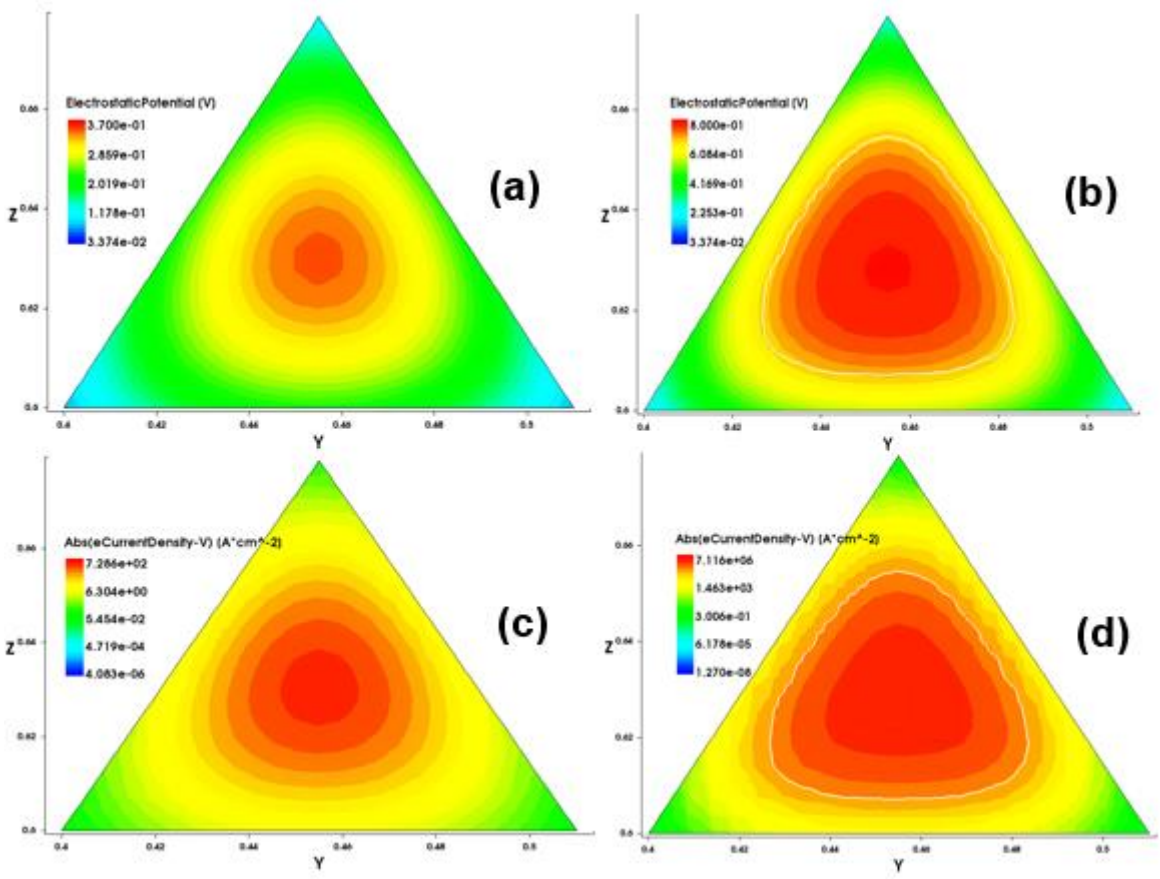

Figure 5.5: TCAD simulation of the electrostatic potential and current density distributions inside triangular silicon nanowire: (a) electrostatic potential for fully depleted nanowire with doping 1 X 10^{17} cm^{-3}; (b) electrostatic potential for partially depleted with doping 1 X 10^{18} cm^{-3}; (c) current density for fully depleted nanowire with 1 X 10^{17} cm^{-3}; (d) current density for partially depleted nanowire with 1 X 10^{18} cm^{-3}.

Under this condition, the potential distribution inside the triangle nanowire can be calculated by finding a transfer factor (T_f) which converts between the thickness of the triangle and the radius of the circle, and this factor can be derived from:

$$\pi r_q^2 = \frac{t^2}{\tan\beta} \tag{5.13}$$

where r_q is the equivalent radius in which the area of the triangle equals the area of the circle. β is the sidewall angle of the triangle shape, and in this study $\beta = 54.5°$ which is the angle between the <111> and <100> planes. Thus, the transfer factor can be obtained from:

$$t = \sqrt{\pi \tan\beta}\, r_q = T_f r_q \tag{5.14}$$

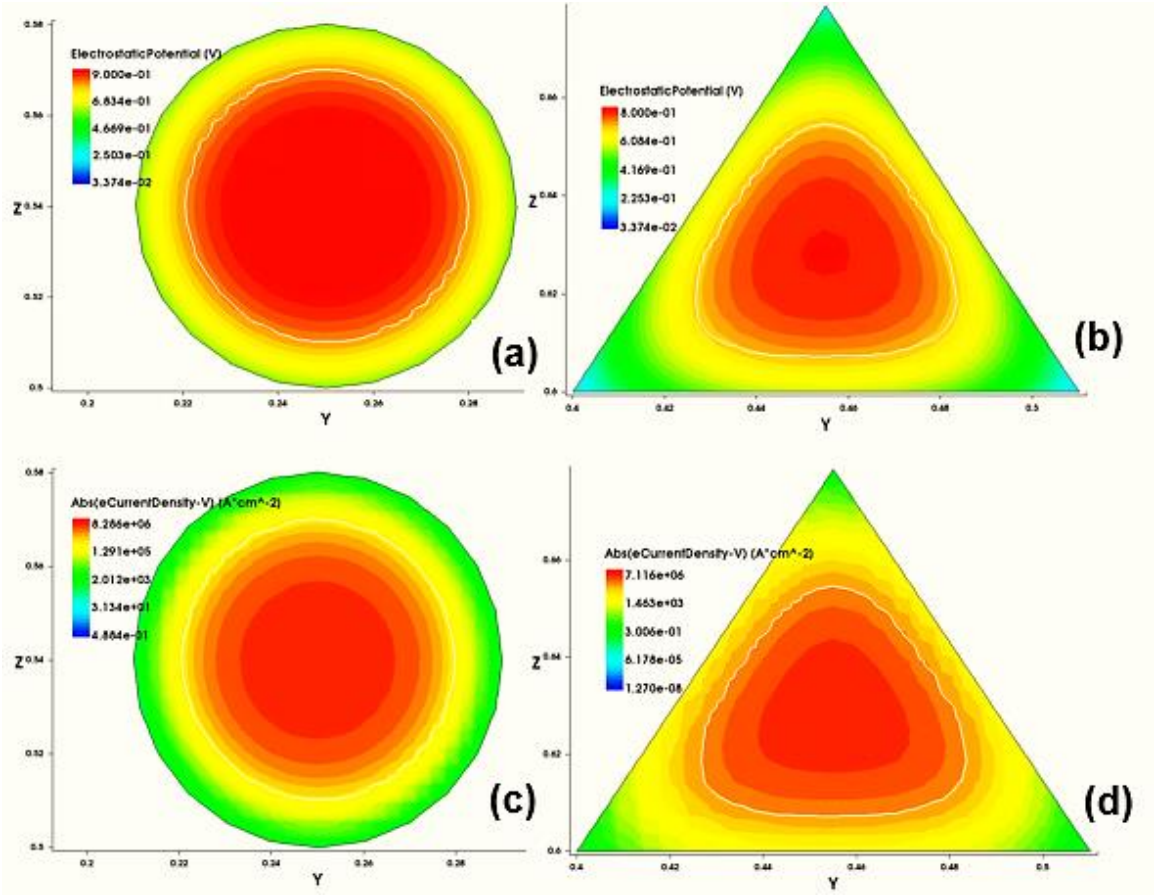

Figure 5.6: TCAD simulation of the electrostatic potential and current density distribution inside circular and triangular cross-sections: (a) electrostatic potential inside circular cross-section; (b) electrostatic potential inside triangular cross-section; (c) current density inside circular cross-section; (d) current density inside triangular cross-section (doping 1 X 10^{18} cm^{-3} for all simulated devices).

Since the model was applied to a doped nanowire, and in order to improve the accuracy of the model, the effect of doping on the position of the Fermi level and band gap is considered in this model. Therefore, band reduction was included in the calculation when the doping level was higher than 10^{+18} cm^{-3}, using [16]:

$$\Delta E_g = 22\left[\frac{N_D}{10^{18}}\right]^{1/2} \quad \text{(meV)} \tag{5.15}$$

Moreover, the Fermi-Dirac integral was used instead of the Boltzmann approximation to more accurately determine the carrier density inside the structure, as will be seen later.

It should be noted that the following model is applied for a partially depleted nanowire. However, the condition stated in section 5.7 should be taken into consideration during the modelling of partially depleted nanowires.

5.3.1 Calculation of the potential inside the neutral region ψ_0

The general solution for the second order differential equation in equation 5.12 is [11, 20, 21]:

$$\psi(r) = -\frac{\varrho(r)}{4\varepsilon_s} r^2 + K_1 \ln(r) + K_2 \tag{5.16}$$

where the values of K_1 and K_2 can be determined from boundary conditions. Since there is no electrical field in the neutral region, then the Neumann boundary condition is expressed as [22, 23]:

$$\frac{d\psi(r)}{dr} = 0 \qquad r \leq r_{qdep} \tag{5.17}$$

At the edge of the depletion region $r = r_{qdep}$, the Dirichlet boundary condition can be expressed as [20, 23]:

$$\psi(r) = \psi_0 \qquad r = r_{qdep} \tag{5.18}$$

By solving the equations 4.16, 4.17 and 4.18 at $r = r_{qdep}$, the constants K_1 and K_2 will be given by:

$$K_1 = \frac{\varrho(r) r_{qdep}^2}{2\varepsilon_s} \tag{5.19}$$

$$K_2 = \psi_0 + \frac{\varrho(r) r_{qdep}^2}{4\varepsilon_s}(-2\ln(r) + 1) \tag{5.20}$$

Then the electrostatic potential inside the nanowire will be given by:

$$\psi(r) = \frac{\varrho(r) r_{qdep}^2}{2\varepsilon_s}\left[-\frac{r^2}{2r_{qdep}^2} + \ln\left(\frac{r}{r_{qdep}}\right) + \frac{1}{2}\right] + \psi_0 \tag{5.21}$$

For $r \leq r_{qdep}$, the neutral region is obtained and the total charge density would be zero and thus the electrostatic potential in this region ψ_0 and thus $\psi(r)$ can be expressed by:

$$\psi(r) = \begin{cases} \Psi_0 & r \leq r_{qdep} \\ \dfrac{\varrho(r) r_{qdep}^2}{2\varepsilon_s}\left[-\dfrac{r^2}{2r_{qdep}^2} + \ln\left(\dfrac{r}{r_{qdep}}\right) + \dfrac{1}{2}\right] + \psi_0 & r_{qdep} < r \leq r_q \end{cases} \tag{5.22}$$

In the model documented in [9], the Boltzmann approximation was used to calculate the Fermi level position, and this model is only valid in lightly doped semiconductor when the Fermi level lies inside the band gap and more than 3KT from either band edge. However, in heavily doped semiconductor when $|E_C - E_F| < KT$, the Boltzmann approximation is

no longer accurate, and thus Fermi-Dirac statistics should be used to determine the position of the Fermi level and subsequently the electrostatic potential in the neutral region ψ_0 [24].

The Fermi-Dirac integral of order ½ ($F_{1/2}(\eta)$) can be expressed as [25, 26]:

$$F_{1/2}(\eta) = \int_0^\infty \frac{\gamma^{\frac{1}{2}}}{1+\exp(\gamma-\eta_F)} \tag{5.23}$$

or as [27]:

$$\mathcal{F}_{1/2}(\eta) = \frac{2}{\sqrt{\pi}} F_{1/2}(\eta) \tag{5.24}$$

The approximate solution of the integral can be expressed as:

$$\mathcal{F}_{1/2}(\eta) = \frac{1}{\exp(-\eta) + \frac{3\sqrt{\pi}}{4\alpha(\eta)}} \tag{5.25}$$

where [25]:

$$\alpha(\eta) = \eta^4 + 33.6\eta(1 - 0.68\exp(-0.17(1+\eta)^2)) + 50 \tag{5.26}$$

Here η is defined by [27]:

$$\eta = \frac{q\psi_{0-E_g/2}}{KT} \tag{5.27}$$

The relationship between electrostatic potential and carrier concentration can be given by [27]:

$$N_D(r) = N_C \mathcal{F}_{1/2}(\eta) \tag{5.28}$$

The distribution of carrier concentration inside the nanowire is assumed to be uniform, $N_D(r) = N_D$.

The electrostatic potential in the nanowire centre, Ψ_0, can then be determined by numerically solving equations 5.25, 5.26, 5.27 and 5.28.

The values of electrostatic potential Ψ_0 as a function of donor concentration is plotted in Figure 5.7. The values of electrostatic potential are independent of cross-section.

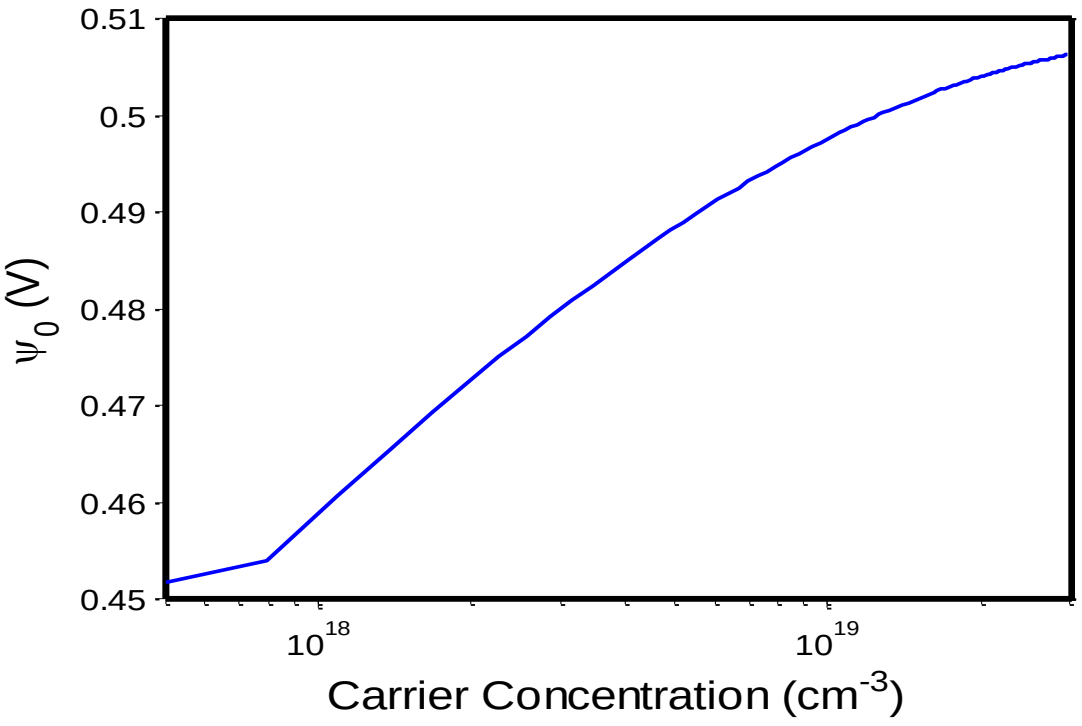

Figure 5.7: Electrostatic potential in the centre of the nanowire as a function of carrier concentration.

5.3.2 Calculation of depletion region r_{qdep}

The position of the Fermi level depends on the interface traps at the surface together with the dopants inside the nanowires. If the silicon-silicon dioxide interface contains interface trap charge D_{it} then the charge density is [9]:

$$Q_{it} = qD_{it}[E_i(0) - E_F] = -q^2 D_{it}\Psi_r \tag{5.29}$$

If charge neutrality is considered then the surface interface charge is equal to the charge in the depletion region, which can be expressed by [9]:

$$\pi\left(r_q^2 - r_{qdep}^2\right)\varrho + 2\pi r_q Q_{it} = 0 \tag{5.30}$$

$$\frac{(r_q^2 - r_{qdep}^2)\varrho}{2r_q q^2 D_{it}} = \frac{\varrho r_{qdep}^2}{2\varepsilon_s}\left[-\frac{r_q^2}{2r_{qdep}^2} + \ln\left(\frac{r_q}{r_{qdep}}\right) + \frac{1}{2}\right] + \Psi_0 \tag{5.31}$$

where $r_q = \frac{t}{T_f} = \frac{t}{\sqrt{\pi \tan\beta}}$ and $w_{dep} = r_q - r_{qdep}$ where w_{dep} is the width of the depletion region. Equation 4.31 was numerically solved to find the depletion region inside the nanowire. The effect of the thickness of the nanowire, doping level and interface trap density on the depletion region width is presented in Figures 5.8.

As shown in Figure 5.8(a), the depletion width increases with decreasing silicon nanowire thickness. When the depletion region reaches a certain value, called the "critical thickness" it starts to decrease with thickness. When the value approaches the critical thickness, this indicates that the nanowire is fully depleted and this model is no longer valid. The critical thickness can be determined by solving equation 5.31 at $r_{qdep} = 0$. The depletion region is calculated for carrier concentrations of 4 X 10^{18} cm^{-3} and 5.3 X 10^{18} cm^{-3} and for an interface trap density of 5 X 10^{12} $cm^{-2}eV^{-1}$ (Figure 5.8(a)). The depletion region width is higher of the lower concentration when the nanowire thickness is larger than the critical thickness. This effect is shown more clearly in Figure 5.8(b).

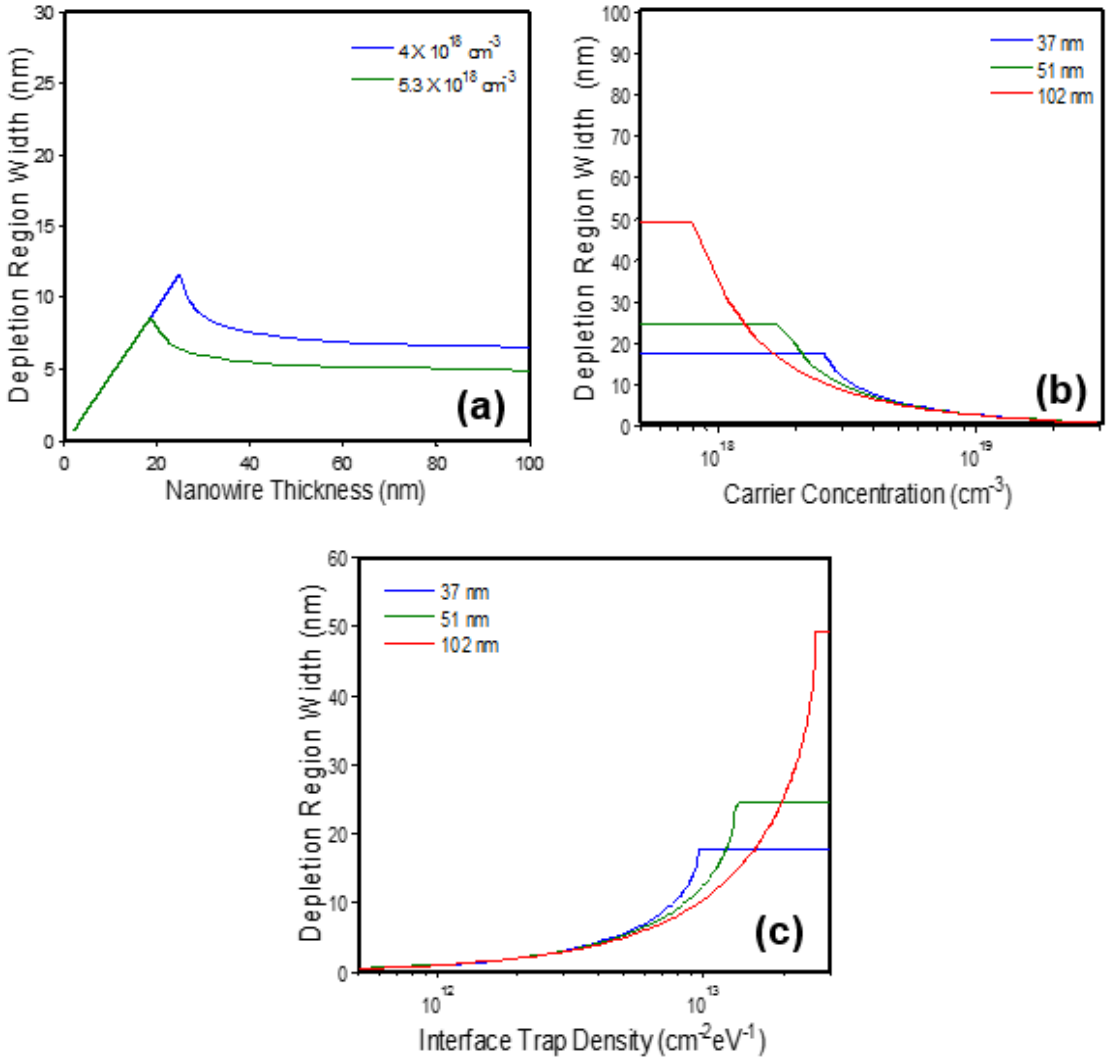

Figure 5.8: (a) Effect of nanowire thickness on depletion region width, D_{it}= 5 X 10^{12} $cm^{-2}eV^{-1}$, N_D= 4 X 10^{18} cm^{-3} and 5.3 X 10^{18} cm^{-3}; (b) effect of carrier concentration on depletion region width, D_{it}= 5 X 10^{12} $cm^{-2}eV^{-1}$, t= 37 nm, 51 nm and 102 nm; (c) effect of interface trap density on depletion region width, N_D= 5.3 X 10^{18} cm^{-3}, t= 37 nm, 51 nm and 102 nm.

The effect of interface traps on the depletion region is presented in Figure 5.8(c). The graphs are plotted for nanowires with different thicknesses and at a carrier concentration of 5.3 X 10^{18} cm^{-3}. The depletion region inside the nanowire increases rapidly with increasing trap density, with influence of interface trap density larger in nanowire of smaller thickness. The straight horizontal line in the graphs in Figures 5.8(b) and (c) indicates that the nanowire thickness is smaller than the critical thickness and the nanowire is fully depleted.

5.3.3 Calculation of the potential inside the depletion region ψ_r

The potential inside the depletion region is determined using equation 5.21. Figure 5.9 shows the effect of interface charge density and carrier concentration on the electrostatic potential inside the depletion region with various values of nanowire thickness. The surface potential in both depends on the thickness of the nanowire. At low interface trap density and large carrier concentration, the effect of traps is small at all thicknesses. At low carrier concentration and large trap density, the effect of nanowire thickness on the electrostatic potential inside the depletion region is significant. For example, the surface potential is calculated to be 0.34 V and 0.31 V for nanowire thicknesses of 37 nm and 102 nm respectively at a carrier concentration of 5.3 X 10^{18} cm^{-3} and an interface trap density of 6 X 10^{12} $cm^{-2}eV^{-1}$. The results can be explained using equations 5.29 and 5.30, since the thickness of nanowire is reduced, the surface to volume ratio increases, and this leads to an increase in the ratio of the reduction of interface trap density to the carrier concentration which consequently results in a greater reduction in electrostatic potential at the surface.

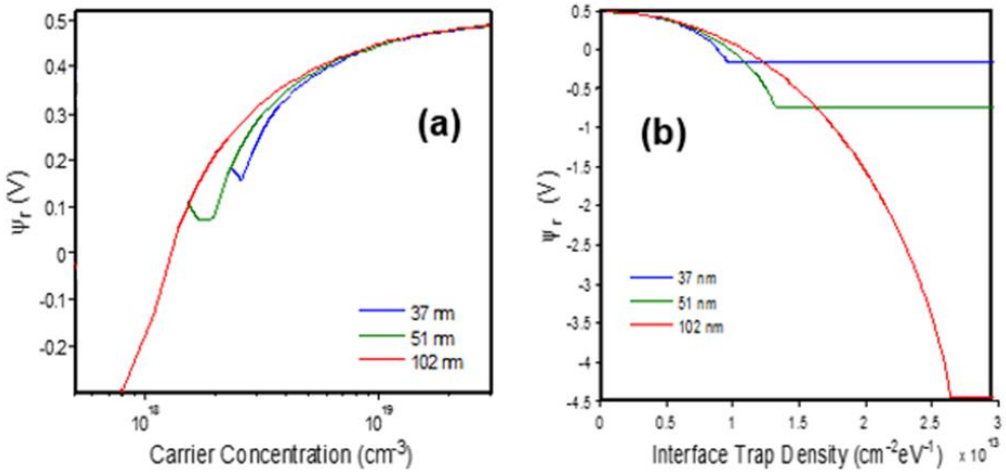

Figure 5.9: (a) The effect of carrier concentration on electrostatic potential inside depletion region, D_{it}= 5 X 10^{12} $cm^{-2}eV^{-1}$, t= 37 nm, 51 nm and 102 nm, (b) the effect of interface trap density on electrostatic potential inside depletion region, N_D= 5.3 X 10^{18} cm^{-3}, t= 37 nm, 51 nm and 102 nm.

5.3.4 Calculation of effective carrier density n_{eff} and effective resistivity

Once the depletion region due to interface traps is calculated, the effective carrier density can be determined. The effective carrier concentration can be calculated using the following equation:

$$n_{eff} = \frac{1}{\pi a^2}\int_0^a N_D\,(r) 2\pi r dr \tag{5.32}$$

For partially depleted wires, using equations 5.23 to 5.28 with equations 5.29 to equation 5.31, the effective carrier density can then be obtained using:

$$n_{eff} = \frac{2N_C}{a^2}\left\{\int_0^{r_d} \frac{1}{\exp\left(\frac{E_g/_2 - q\psi_0}{KT}\right) + \frac{3\sqrt{\pi}}{4\alpha(\eta)}} r dr + \int_{r_d}^{a} \frac{1}{\exp\left(\frac{E_g/_2 - q\psi(r)}{KT}\right) + \frac{3\sqrt{\pi}}{4\alpha(\eta)}} r dr\right\} \tag{5.33}$$

The effective carrier density is plotted as a function of carrier concentration, interface trap density and nanowire thickness and the results are presented in Figure 5.10.

As expected, at a high carrier concentration ($N_D > 10^{19}$ cm^{-3}), the effect of interface traps on carrier density is small, since as the concentration decreases the effect of interface traps is more significant. For example, the effective carrier density drops tenfold for N_D about 2.2 X 10^{18} cm^{-3} for a nanowire with a thickness of 51 nm and when interface trap density is about 5 X 10^{12} cm^{-2}eV^{-1} (Figure 5.10(a)). The effective density of carrier concentration depends on nanowire size, declining faster as nanowire thickness decreases (Figure 5.10(a), (b), (c)).

The values of effective carrier density are used to calculate the effective resistivity of the nanowire. The effective resistivity can be calculated using:

$$\rho_{eff} = \frac{1}{q\mu n_{eff}} \tag{5.34}$$

where μ is electron mobility which is assumed to be independent of size and dependent on carrier density.

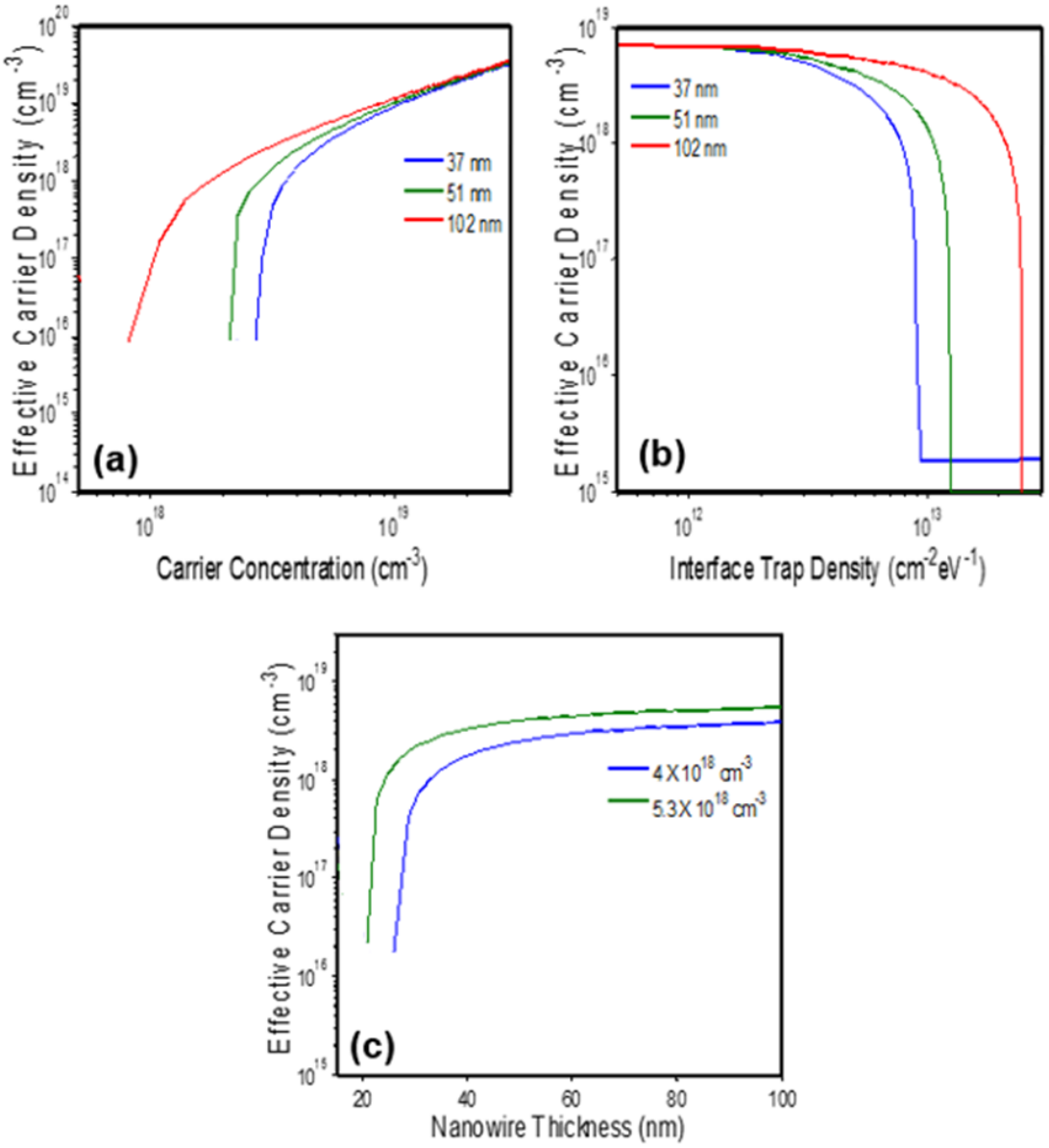

Figure 5.10: (a) Effective carrier density as a function of carrier concentration, D_{it}= 5 X 10^{12} $cm^{-2}eV^{-1}$, t= 37 nm, 51 nm and 102 nm; (b) effective carrier density as a function of interface trap density on the depletion region width, N_D= 5.3 X 10^{18} cm^{-3}, t= 37 nm, 51 nm and 102 nm; (c) effective carrier density as a function of nanowire thickness, D_{it}= 5 X 10^{12} $cm^{-2}eV^{-1}$, N_D= 4 X 10^{18} cm^{-3} and 5.3 X 10^{18} cm^{-3}.

The value of mobility, therefore, was calculated using the following expression [17]:

$$\mu = \mu_{min} + \frac{\mu_o}{1 + \left(N/N_{ref}\right)^{\propto}} \tag{5.35}$$

where $\mu_{min} = 92$ cm^2/V.s, $\mu_o = 1268$ cm^2/V, $N_{ref} = 1.3\ X\ 10^{17}$ cm^3, and $\propto = 0.92$ while N is the carrier density.

Equation 5.34 was used to plot the effective resistivity as a function of nanowire thickness. Figure 5.11 shows the effect of nanowire thickness on the effective resistivity for D_{it}= 5 X 10^{12} $cm^{-2}eV^{-1}$, N_D= 4 X 10^{18} cm^{-3} and 5.3 X 10^{18} cm^{-3}. The resistivity increases with decreases in the size of the nanowire. For a nanowire with a thickness of 40 nm (N_D= 4 X 10^{18} cm^{-3}), the effective resistivity increases about by four times compared to the 100 nm nanowire.

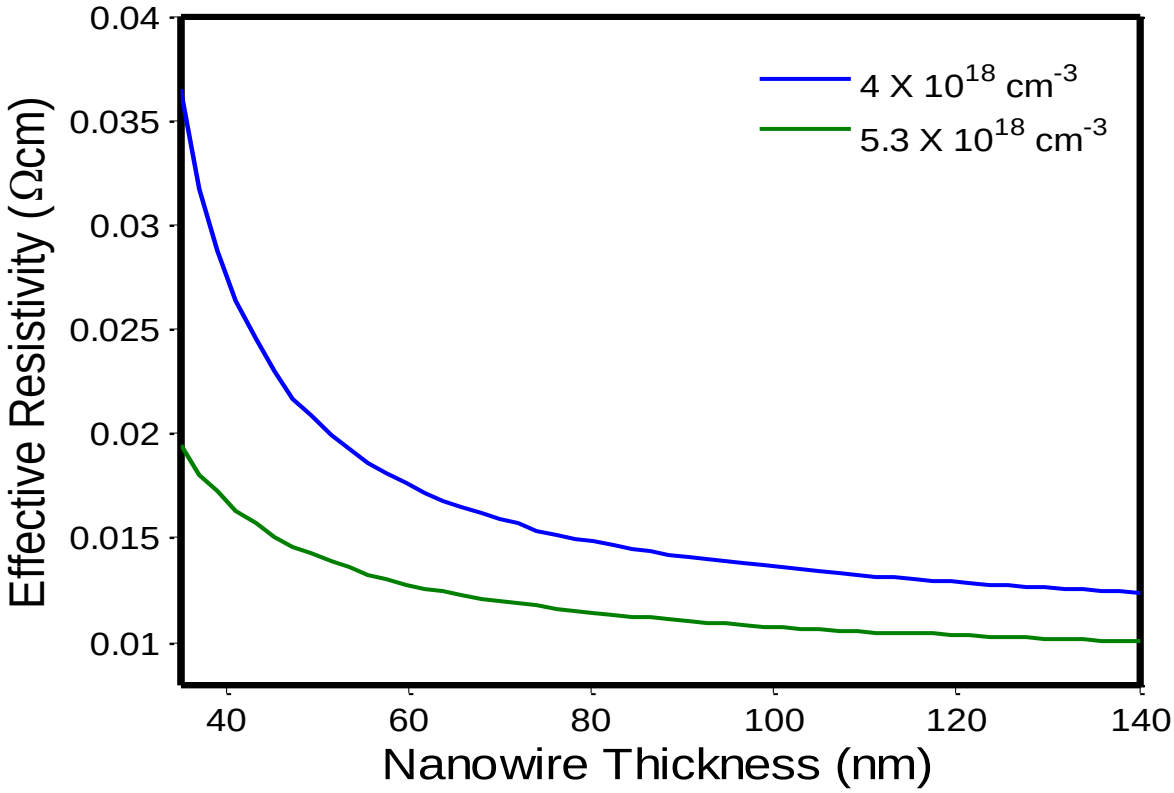

Figure 5.11: The effective resistivity as a function of nanowire thickness (D_{it}= 5 X 10^{12} $cm^{-2}eV^{-1}$, N_D= 4 X 10^{18} cm^{-3} and 5.3 X 10^{18} cm^{-3}).

5.3.5 Effective resistivity in silicon nanowire: fitting the experimental data

The goal of the previous model was to fit the effect of surface depletion to the measured electrical resistivity. Since the carrier concentration is non-uniform, its value was assumed to be $N_D = 4 \text{ X } 10^{18}\ cm^{-3}$ for nanowires with thicknesses larger than 60 nm, and $N_D = 5.3 \text{ X } 10^{18}\ cm^{-3}$ for thicknesses smaller than 60 nm. These values are the average values of carrier concentration in nanowires in that range of thicknesses (see the plot in Figure 5.2). Figure 5.12 shows the fitting model for the measured electrical resistivity, after eliminating the effect of dopant distribution. The best fit to the experimental data corresponds to the interface charge density $D_{it} = 5.9 \text{ X } 10^{12} cm^{-2} eV^{-1}$. This value of

interface trap density is high for dry oxidation, which is typically between 10^{10}-10^{12} $cm^{-2}eV^{-1}$ in <100> silicon. However, since the nanowires reported in this study have two <111> sides, it is not unusual to find a value of interface trap density in the range of 10^{12}-10^{13} $cm^{-2}eV^{-1}$ [28, 29]. Further measurements are essential to extract the density of the interface of silicon nanowire in order to provide a better understanding of the role of surface properties on the resistivity of nanowire.

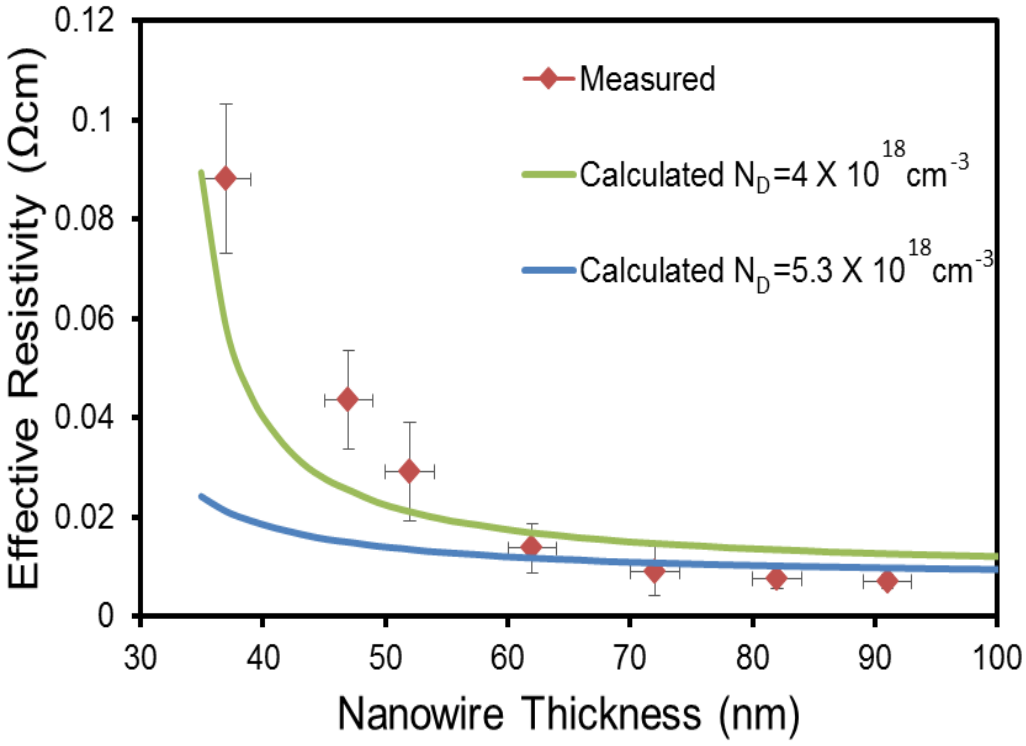

Figure 5.12: Fitting the surface depletion effect to the measured electrical resistivity of silicon nanowire for $D_{it} = 5.9 \text{ X } 10^{12} cm^{-2} eV^{-1}$.

5.4 Effect of surface scattering

The increase in electrical resistivity of thin films with decreasing size was first reported in metallic films in 1936 [1]. In the following year the effect of the surface and size on electrical resistivity in thin films was theoretically studied by Fuchs [30], who argued that the apparent electrical resistivity of metallic thin film will increase when the film thickness is comparable to or smaller than the electronic mean free path (MFP). This was attributed to the diffusive scattering at the surface. Similar results were obtained by Dingle [31] who used the Boltzmann transport equation to calculate the effect of the diffusive scattering surface on the electrical resistivity of circular wires. A simpler and more sophisticated model of the effect of the surface was suggested by Chambers in 1950 [32]. He used a kinetic theory argument to calculate the change in conductivity of thin films and wires due to the effect of the surface. The specularity parameter *p* is normally used to describe the

scattering at the surface, where the surface is called fully diffusive when the electron momentum is lost after collision with the surface, and in this case p=0. Meanwhile the surface is called fully spectral when the momentum of the electron is conserved after collision with the surface, in which case $p = 1$. The value of p is difficult to determine and is normally used as a fitting parameter.

There are many reasons to study the effect of surface scattering in single crystalline silicon nanowire. Firstly, anisotropic wet etching was utilised to fabricate the nanowire, which could lead to a formation of rough nanowire where large roughness values in the <111> plane were observed after anisotropic wet etching (see section 3.4.3.1). Moreover, oxidation of the silicon nanowires was observed to be non-uniform along its length and across its thickness (as reported in section 3.3.3.2), which indicates that the non-regularity of silicon nanowire tends to increase after dry oxidation. These two factors can lead to an increase of diffusivity at the surface due to the increase in the occurrence of backscattering. Secondly, the nanowires have a triangular cross-section, which means that there is a region in the surface with "zero width", and due to this geometric effect the diffusivity at the surface could increase. Due to its simplicity, the kinetic-theory argument will be used in this research to estimate the effect of surface scattering on the electrical resistivity of triangular silicon nanowire.

In Chambers model, the electrical resistivity depends on the thickness of the wire, and the electronic mean free path as well as the specularity parameter. The ratio of the electrical resistivity of the bulk to the electrical resistivity of a wire with an arbitrary cross-section for a fully diffusive surface is given by [32]:

$$\frac{\rho_B}{\rho_{eff}} = 1 - \frac{3}{4\pi s}\int ds \int_0^{2\pi} d\emptyset \int_0^{\pi} \sin\theta \, cos^2\theta . d\theta * \exp\left(-\frac{OP}{\lambda}\right) = 1 - \frac{3}{4\pi s} I \qquad (5.36)$$

where s is the cross section of the wire, OP is the distance that the electron passes without collision from the point O inside the cross section to the point P on the surface of the wire, λ is the electronic mean free path (MTP), θ is the angle between the z axis and the vector OP, and $\emptyset$ is the azimuthal angle around the z axis.

In order to calculate the effect of surface scattering on the electrical resistivity of a triangular nanowire, the above integral is conducted for each side length of the nanowire cross-section and then the three integrals are added together to calculate the electrical resistivity (which is similar to the work reported for the rectangular cross-section [33]). Therefore, $I = I_{AB} + I_{BC} + I_{CA}$ and due to the symmetry in the y direction $I_{AB} = I_{BC}$; thus $I = 2I_{AB} + I_{CA}$ (Figure 5.13). In order to conduct these integrals, the integral limits and the length OP should be defined for each segment first.

For side length *AB*:

To determine OP_{AB},

$OP_{AB} = \frac{OP_{xy}}{\sin\theta}$ where OP_{xy} is the projection of OP on xy. In order to find OP_{xy}, the length t_1 is determined first (schematic in Figure 5.13) as: $t_1 = \frac{w}{2} - \frac{y}{tan\beta} - x$, which is based on the law of sines:

$$OP_{xy} = \frac{t_1}{\sin(\beta + \emptyset)} \sin\beta = \frac{\frac{w}{2} - \frac{y}{tan\beta} - x}{\sin(\beta + \emptyset)} \sin\beta \tag{5.37}$$

$$OP_{AB} = \frac{OP_{xy}}{\sin\theta} = \frac{\frac{w}{2} - \frac{y}{tan\beta} - x}{\sin\theta \sin(\beta + \emptyset)} \sin\beta \tag{5.38}$$

Then, to determine $\emptyset$:

$$\emptyset_A = \arctan\left(\frac{y}{w/_2 - x}\right) \tag{5.39}$$

$$\emptyset_B = \pi - \arctan\left(\frac{h - y}{x}\right) \tag{5.40}$$

For side length *CA*:

$$OP_{CA} = \frac{OP_{xy}}{\sin\theta} = -\frac{y}{\sin\theta \sin\emptyset} \tag{5.41}$$

$$\emptyset_C = \pi - \arctan\left(\frac{y}{w/_2 + x}\right) \tag{5.42}$$

$$\emptyset_D = 2\pi - \arctan\left(\frac{y}{w/_2 - x}\right) \tag{5.43}$$

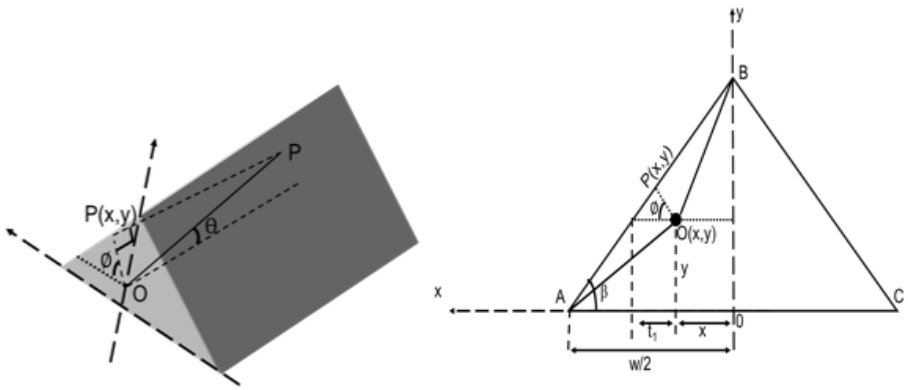

Figure 5.13: Schematic used to calculate the effect of surface scattering on the electrical resistivity in triangular nanowire.

The cross section of the nanowire is given by:

$$s = \frac{wt}{2} = \frac{w^2}{4}\tan\beta \tag{5.44}$$

where $\beta = 54.5^{\circ}$, which is the angle between the <111> and <100> planes.

Thus, the integral I_{AB} becomes:

$$I_{AB} = \int_0^{\frac{w}{2}} dx \int_0^{(\frac{w}{2}-x)\tan\beta} dy \int_{\arctan(\frac{y}{w/2-x})}^{\pi-\arctan(\frac{h-y}{x})} d\emptyset \int_0^{\pi} \sin\theta\, cos^2\theta.\, d\theta * \exp\left(-\frac{\left(\frac{w}{2}-\frac{y}{tan\beta}-x\right) sin\,\beta}{\lambda \sin\theta\, sin(\beta+\emptyset)}\right) \tag{5.45}$$

$$I_{AB} = \int_0^{\frac{w}{2}} dx \int_0^{\left(\frac{w}{2}-x\right)\tan\beta} dy \int_{2\pi-\arctan\left(\frac{y}{w/2-x}\right)}^{\pi-\arctan\left(\frac{y}{w/2+x}\right)} d\emptyset \int_0^{\pi} \sin\theta\, cos^2\theta.\, d\theta * \exp\left(\frac{y}{\lambda \sin\theta \sin\emptyset}\right) \tag{5.46}$$

Resistivity with zero specularity can be used to express the influence of non-zero specularity ($p \neq 0$) on the electrical resistivity of nanowire by using the following series:

$$\left(\frac{\rho_B}{\rho_{eff}}\right)_{\lambda,p} = (1-p)^2 \sum_{n=1}^{\infty} \left(np^{n-1}\left(\frac{\rho_B}{\rho_{eff}}\right)_{0,\frac{\lambda}{n}}\right) \tag{5.47}$$

Figure 5.14 shows the calculated nanowire resistivity as a function of nanowire thickness for different specularity values. The mean free path was assumed to be 15 nm [34]. The results indicate that the influence of surface scattering on the electrical resistivity is estimated to be important at thicknesses of nanowire less than 25 nm. Therefore, the effect of surface scattering on the measured electrical resistivity is excluded in this study.

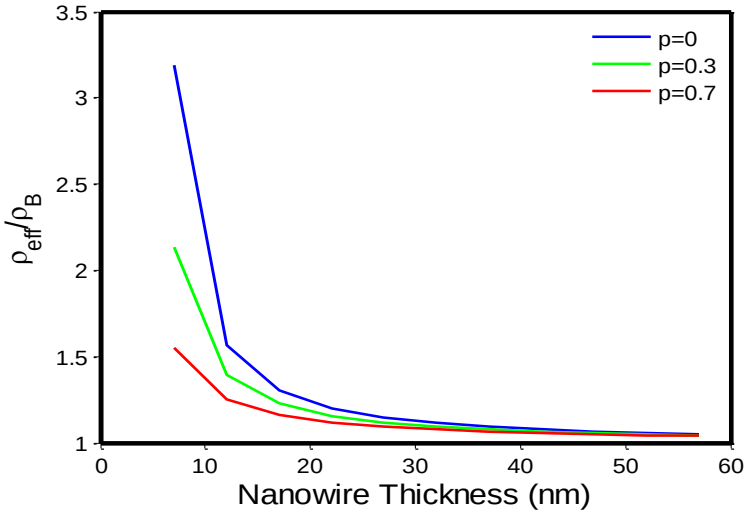

Figure 5.14: Calculated relative resistivity of nanowire to bulk resistivity as a function of nanowire thickness with different values of the specularity parameter (mean free path of 15 nm).

5.5 Effect of surface roughness

In addition to its influence on the surface scattering of the nanowire, surface roughness increases the measured resistance/resistivity due to the variation in cross section along the length of the nanowire. This variation can occur during any of the following process steps: anisotropic wet etching, lithography, or in the case of misalignment, and the thermal oxidation of silicon. This section estimates the effect of the variation in the cross section of the nanowire on its measured electrical resistance/resistivity.

The electrical resistance can be determined by the following integration:

$$R_{rough} = \int_0^L \frac{\rho dx}{A(x)} \tag{5.48}$$

For simplicity, the nanowire can be divided into two segments, the first of which is rough and has length $L1 = KL$ and cross section $A1 = \frac{(w-R_d)^2}{4}\tan\beta$, where w is the width of the nanowire, R_d is the variation in width, and β is the sidewall angle. The second segment is smooth and has length $L2 = (1-K)L$ and cross section $A2 = \frac{w^2}{4}\tan\beta$. Thus, the resistance can be rewritten as:

$$R_{rough} = \frac{\rho KL}{A1} + \frac{\rho(1-k)L}{A2} = \frac{4\rho L}{\tan\beta}\frac{KR_d^2 - 2KwR_d + w^2}{w^2(w-R_d)^2} \tag{5.49}$$

The relative resistance of the nanowire to the bulk resistance can be expressed as:

$$\frac{R_{rough}}{R_{bulk}} = \frac{KR_d^2 - 2KwR_d + w^2}{(w-R_d)^2} \tag{5.50}$$

If the value of root mean square roughness R_q is used to express the variation in nanowire width, then the value of $R_d = 2\ \mathrm{X}\ R_q$. Thus, according to the value of R_q reported in section 3.4.3.1, $R_d = 5\,nm$. Figure 5.15 shows the relative change in nanowire resistance compared to bulk resistance as a function of nanowire width assuming that $K = 0.25$. The surface roughness has a large influence on electrical resistance when the width of the nanowire is below 50 nm (or when thickness is less than 40 nm; see the inset in Figure 5.15). Since the electrical resistance is proportional to the electrical resistivity, this variation in resistance is measured as a variation in resistivity. Therefore, in order to obtain an accurate value of electrical resistivity, the influence of roughness should be considered during the measurement of the electrical resistivity of nanowires.

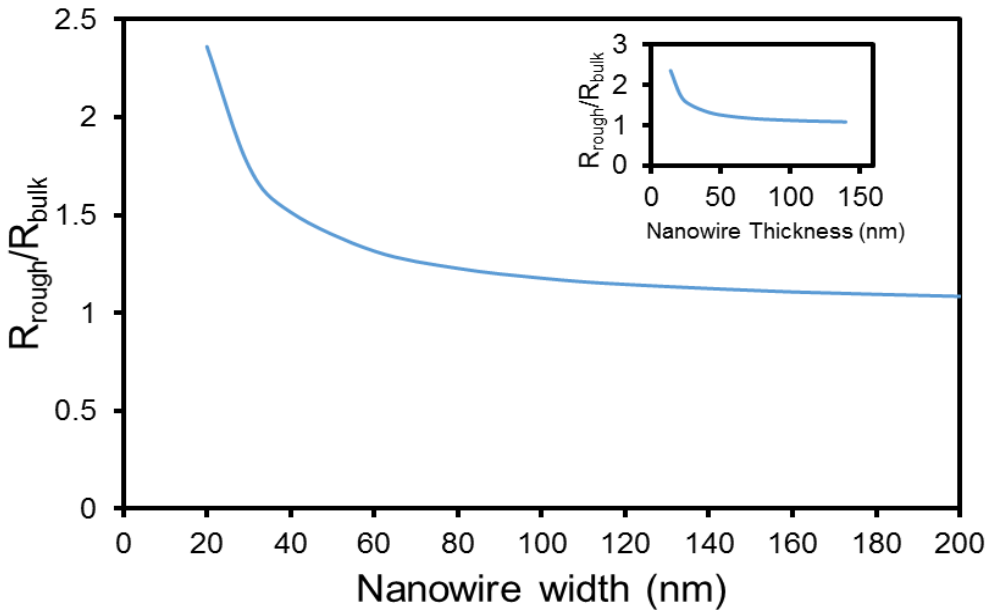

Figure 5.15: The effect of surface roughness on the electrical resistance of nanowire as a function of nanowire width (inset: relative resistance as a function of nanowire thickness).

Finally, the contribution of each model to the measured resistivity is illustrated in Figure 5.16. It is clearly shown that surface-depletion due to interface traps makes the greatest contribution to the measured resistivity in the nanowires.

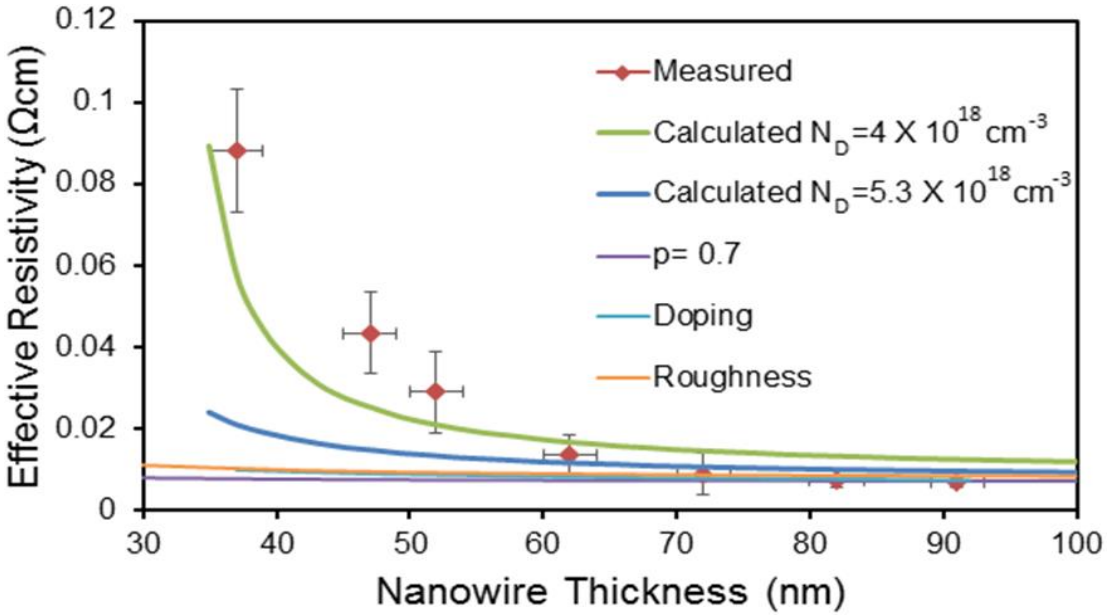

Figure 5.16: All possible models have an effect on the increase in the resistivity of the nanowire compared with the measured one (measured (red marks); the effect of doping distribution (cyan); the effect of surface depletion for $D_{it} = 5.9 \text{ X } 10^{12} cm^{-2} eV^{-1}, N_D = 4 X 10^{18} cm^{-3}$(green); the effect of surface depletion for $D_{it} = 5.9 \text{ X } 10^{12} cm^{-2} eV^{-1}, N_D = 5.3 X 10^{18} cm^{-3}$(blue); the effect of surface roughness (orange); and the effect of scattering (purple).

5.6 Summary

Several models are developed in this chapter to explain the apparent increase in the measured electrical resistivity with decreasing thickness of the silicon nanowire. The models described in this chapter show that the measured resistivity is not sensitive to only a single parameter, but can be affected by several parameters such as non-uniformity in doping distribution, surface depletion, surface scattering and surface roughness.

A Gaussian distribution function is used to calculate the carrier distribution profile as a function of nanowire thickness. The obtained profile is then used to find the change of electrical resistivity with depth, and the result is subtracted from the measured resistivity. The value of parameter *n*, which describes the relationship between the measured resistivity and thickness, is reduced from 1.19 to 1.08 after subtracting the effect of the dopant on the measured resistivity for nanowires with thicknesses larger than 60 nm.

Using self-consistent models, it is proven that solving Poisson's equation for a circular cross-section can be used to find the electrostatic potential and depletion region in triangular cross-section. Poisson's equation is used to find the relationships between interface trap density, nanowire thickness, electrostatic potential and carrier density. It is then used to study the effect of interface charge on electrical resistivity. It is found that the electrical resistivity can be largely affected by the large trap density. The analytical results suggest that the surface depletion due to interface traps could exert the dominant effect on the increase in electrical resistivity in the region with a thickness less than 60 nm.

A simple model is suggested to calculate the effect of surface roughness on measured electrical resistivity. Based on the measured value of surface roughness reported in section 3.3.1, the surface roughness has an influence on measured resistivity at nanowire thicknesses less than 40 nm.

A simple model based on the kinetic-theory argument is developed in this chapter to calculate the effect of surface scattering due to surface roughness on the electrical resistivity of a triangular nanowire. The results indicate that resistivity is largely affected by surface scattering at nanowire thicknesses less than 25 nm.

Finally, in order to accurately determine the apparent increase in resistivity, the contribution of each of the above mentioned effects should be carefully taken into consideration.

5.7 Future work

The measurement of electrical resistivity was performed on silicon nanowires coated with silicon dioxide, the low dielectric constant has been reported to increase the ionisation energy with decreasing the size of nanostructures. This effect could play an important role in the increase in resistivity with decreasing the size of silicon nanowires. However, it has been reported that the effect of dielectric confinement in nanowires can be theoretically reduced in the nanowire with triangular cross-section, leading to a decrease in the ionisation energy and an increase in free carrier density in the nanowire [8]. Therefore, it is expected that the effect of dielectric mismatch on electrical resistivity in silicon nanowires will be found to be lower with triangular cross-section compared with those previously reported [3]. Therefore, it is important to coat the nanowire with various dielectric materials and study the effect of the dielectric constant on electrical resistivity, and such a study should be supported with an appropriate theoretical model.

In section 5.3, during the solving of Poisson's equation, the doping is considered to be homogeneously distributed inside the silicon nanowire. However, as introduced in sections 3.2.4 and 5.2, the doping distribution inside the nanowire follows a Gaussian distribution. Therefore, in order to accurately determine the electrostatic potential and depletion region inside the nanowire due to the interface traps, the exponential distribution of the dopant should be included in the Poisson's equation.

The model which has been investigated in section 5.3 is intended for partially depleted nanowire, and it is not valid for fully depleted nanowire. However, in applications such as biosensing, the nanowire is always expected to be fully depleted since the nanowire is lightly doped. Therefore, it is useful to model the case when the nanowire is fully depleted.

The depletion region in this case is equals to the thickness of the nanowire. Thus $r_{qdep} = 0$ and equation 5.31 can be reduced to:

$$\frac{(r_q)\rho}{2q^2 D_{it}} = \frac{\rho r_q^2}{4\varepsilon_{Si}} + \Psi_0 \tag{5.51}$$

Section 5.3, the modelling indicates that interface traps can have a large impact on the increase in electrical resistivity of the nanowire, and the experimental results in chapter three show that the electrical resistivity of the nanowire is reduced after annealing the samples at 380˚C. Both theoretical and experimental results show the need for the special treatment of the nanowire in order to minimise the density of traps during fabrication. For example, it is expected that the oxidation furnace could be contaminated because it has been used by many users with various materials and no regular cleaning is performed. Therefore, oxidation defects are one of type of defects that are likely to be produced in this fabrication process. Thus, it is important to minimise contamination levels inside the

furnace, and also it is strongly recommended to perform furnace cleaning using oxygen and chlorine vapours prior to any oxidation process and to regularly change the quartz boat.

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Chapter 6

Silicon Nanowire Field-Effect Transistors in Aqueous Media

This chapter concerns the integration of silicon nanowires into devices for sensing applications. It includes the electrical characterisation of the devices in aqueous media, and mainly focuses on the properties of silicon nanowires as pH sensors. The chapter opens with a description of the structure and the principles of the ion-sensitive field-effect transistor (ISFET), and goes on to describe the sample design and the fabrication process of the devices. Furthermore, it presents the nanowire's response to changes in pH values. Beyond that, it discusses the factors that affect the reliability of the current process.

6.1 The ion-sensitive field-effect transistor (ISFET)

The ion-sensitive field-effect transistor (ISFET) has a similar structure to that of the conventional metal–oxide–semiconductor field-effect transistor, with the exception that the top metal gate electrode is omitted and replaced by an electrolyte solution with a reference electrode (Figure 6.1(a)) [1-3]. The reference electrode is immersed in the solution and acts as a potential regulator. Ionic exchange between the gate insulator and the solution causes a change in the surface potential. The channel conductance and the device's threshold voltage can then be altered by varying the voltage bias at the reference electrode, in addition to the surface potential at the solution-dielectric interface [1].

$$V_{th} = E_{ref} + \chi^{sol} - \psi_0 - \frac{\Phi_{Si}}{q} - \frac{Q_{ox} + Q_B + Q_{it}}{C_{ox}} + 2\Phi_B \qquad (6.1)$$

where E_{ref} is the potential at the reference electrode, ψ_0 is the potential drop in the solution at the dielectric-solution interface, $\Phi_B$is the potential difference between semiconductor surface and Fermi level, χ^{sol} is the surface dipole potential of the solvent, $\frac{\Phi_{Si}}{q}$is the work function of silicon, Q_{ox}, Q_B and Q_{it} are the fixed oxide charge, the depletion charge in silicon, and the surface state density at the silicon interface respectively.

The sensitivity of the ISFET sensor depends mainly on the interaction between the surface states at the dielectric oxide, as well as the charges in the solution [1].

In pH sensing, the oxide layer represents the active sensing layer. When it comes into direct contact with the solution, the silanol sites A-OH at the surface of the gate oxide can exchange with protons in the solution [4-7]. The nature of the surface can be determined by the value of pH, where at low values the surface charge is positive (proton acceptor) in the middle and at higher pH values the surface charges are neutral and negative (proton donor) respectively (Figure 6.1(b)). Thus, the silanol site A-OH can behave as either an acid or a base. The equilibrium chemical equations that describes protonation and deprotonation at the oxide-solution interface are [5, 7]:

$$A-OH \overset{K_a}{\Leftrightarrow} A-O^- + H_s^+; \quad K_a = \frac{[A-O^-][H^+]_s}{[A-OH]} \tag{6.2}$$

$$A-OH + H_s^+ \overset{K_b}{\Leftrightarrow} A-OH_2^+; \quad K_b = \frac{[A-OH_2^+]}{[A-OH][H^+]_s} \tag{6.3}$$

where K_a and K_b are the dissociation constants [8]; $[A-O^-]$, $[A-OH]$ and $[A-OH_2^+]$ are the concentration of the active sites per unit area, and $[H^+]_s$ is the concentration of hydrogen ions at the interface. The binding of ions with the active hydroxyl sites results in a gradient concentration of ions in the solution and a double layer at the oxide/solution being formed, according to Chapman-Stern theory [7, 8]. Thus, the hydrogen ions at the surface are related to the concentration in the bulk according to the Boltzmann equation [7, 8]:

$$[H^+]_s = [H^+]_b exp\left(-\frac{q\psi_0}{KT}\right) \tag{6.4}$$

where $\psi_0$is the surface potential drop across the double layer. The total surface charge density due to the protonated and deprotonated groups of the hydroxyl is given by:

$$\sigma_0 = q([A-OH_2^+] - [A-O^-]) = -q[B] \tag{6.5}$$

$$\sigma_0 = qN_s \frac{[H^+]_s^2 - K_aK_b}{K_aK_b + K_b[H^+]_s^2 + [H^+]_s^2} = -q[B] \tag{6.6}$$

where is N_s is the total number of surface sites which is equal to $N_s = [A-O^-] + [A-OH_2^+] + [A-OH]$, and the sensitivity of the device can be determined by the change in surface potential with changes in the pH of the solution:

$$\frac{\partial\psi_0}{\partial pH_s} = \frac{\partial\psi_0}{\partial\sigma_0}\frac{\partial\sigma_0}{\partial pH_s} \tag{6.7}$$

The general expression for the change in surface potential with changes in pH can be written as [6, 7]:

$$\frac{\partial \psi_0}{\partial pH_s} = -2.3\frac{KT}{q}\alpha \tag{6.8}$$

where α represents a sensitivity parameter that varies between 0 and 1, and this can be described by:

$$\alpha = \frac{1}{\left(\frac{2.3KTC_{dif}}{q^2\beta_{int}}\right) + 1} \tag{6.9}$$

where β_{int} is the intrinsic buffer capacity and C_{dif} is the differential double-layer capacitance. The maximum value of sensitivity which is the so-called Nernstian sensitivity, is 59.2 mV/pH and can be achieved when $\alpha = 1$.

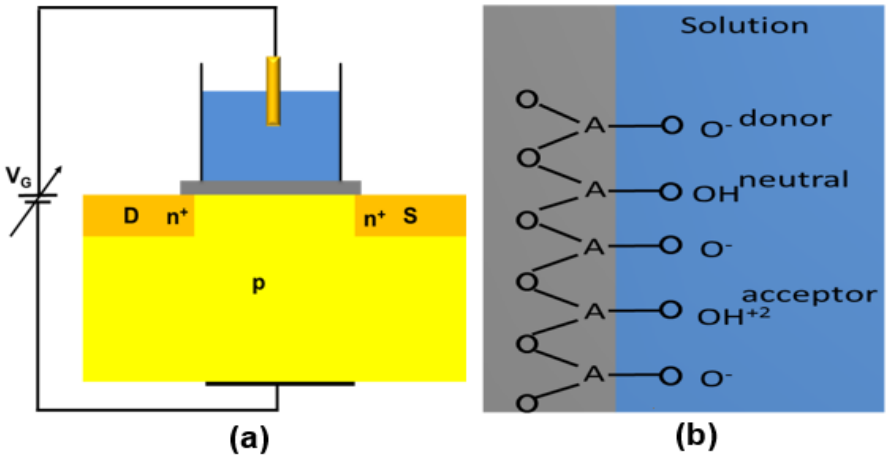

Figure 6.1: (a) Schematic diagram of basic structure of ISFET; (b) dielectric/electrolyte interface.

6.2 Sample design and fabrication

The mask layout is divided into two halves within a chip size of 1 cm X 1.6 cm. The first half of the chip includes fifty single nanowires separated from one another by 110 µm gaps to isolate the device electrically. The source/drain regions have dimensions of 40 µm X 40 µm, and each is connected to metal electrodes of 66 µm width connected to large metal pads located outside the wet area. The gap between the electrodes is 85 µm while the pads are separated by a 42 µm gap. The other half of the chip includes fifty nanowires in bundles of five each, where the shortest distance between two adjacent metal electrodes is 55 µm (Figure 6.2).

It should be noted that the mask was designed according to the customer's requirements, and this has imposed limitations on any potential change in the design.

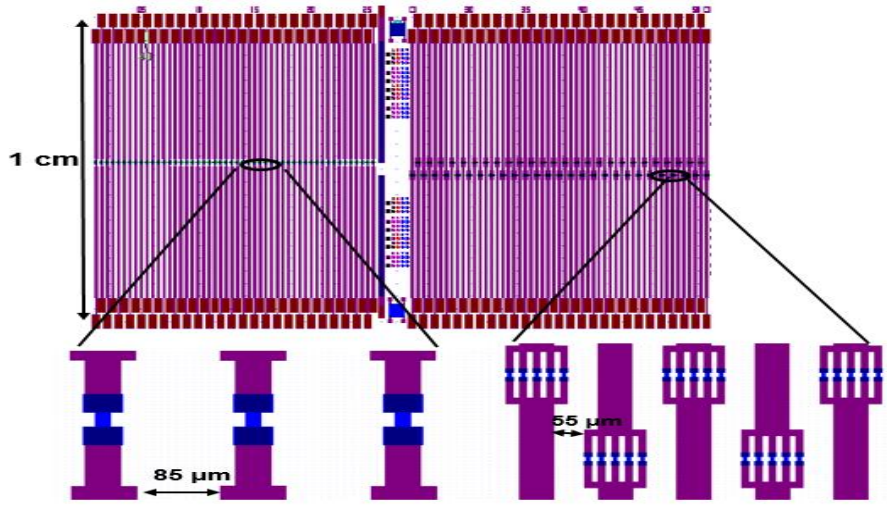

Figure 6.2: Mask layout of the nanowires where the expanded views show the distance between the electrodes in the case of a single nanowire (bottom left) and bundles of five nanowires (bottom right).

The key steps involved in the fabrication process of silicon nanowire-based devices are summarised below.

a) Printing the alignment marks: a 40-50 nm oxide was grown on a lightly p-type doped SOI substrate, and a lithography step was carried out to pattern the alignment marks. Then, the RIE etching step was performed to transfer the alignment marks to a depth of about 250 nm. (Figure 6.3(a))

b) Doping the source and drain: another lithography step was used to expose the source and drain regions, which was followed by a BHF step to define the source and drain. The spin-on-doping method was conducted to obtain n-type source/drain doped regions. The doping procedure is described in section 3.2. (Figure 6.3(b))

c) Fabrication of silicon nanowire: the nanowires were then defined by using optical lithography, anisotropic wet etching and thermal oxidation. The fabrication steps of the nanowire fabrication are described in sections 3.3.1.1 to 3.3.1.8. A typical AFM profile of the nanowire obtained is shown in Figure 6.4(a). A variation in nanowire dimensions (device-to-device variation) was observed after scanning 23 devices from different zones using AFM. The results show that the uniformity in the top width of the whole wafer is approximately more than 85 %, with more than 90 % uniformity in the thickness of the nanowires.

d) Deposition of the active sensing layer: 18 nm of aluminium oxide (Al_2O_3) was grown using atomic layer deposition (ALD). Aluminium oxide was used instead of thermal silicon dioxide because the former is more resistant to moisture and ion diffusion and has higher sensitivity. (Figure 6.3(d))

e) Contact opening: the area of contact was then patterned and defined by using lithography and BHF etching.

f) Metallisation: another lithography step was performed to pattern the contact pads. Then the electron beam evaporator was used to deposit 60/100 nm of Ti/Al, which was followed by a lift-off step in acetone in order to remove the photoresist. (Figure 6.3(e))

g) Deposition of passivation layer: to minimize the parasitic resistance between the nanowire and the metal, and to isolate the metals during the sensing experiments, a passivation layer of silicon nitride was deposited on the whole wafer leaving the sensing area above the nanowire exposed. Therefore, a photolithography step was performed first to protect the silicon nitride with photoresist, and a 70 nm silicon nitride layer was deposited using physical vapour deposition (PVD). This was followed by a lift-off step to remove the photoresist. (Figure 6.3(f))

h) Deposition of probe pads: a lithography step and etching step were used to define the probe pads. Then the electron beam evaporator was used to deposit 150 nm of Al, which was followed by a lift-off step in acetone in order to remove the photoresist.

i) The wafer was then annealed in forming gas (H_2/N_2) for three minutes in RTP to reduce the interface traps and form ohmic contacts as described in chapter four.

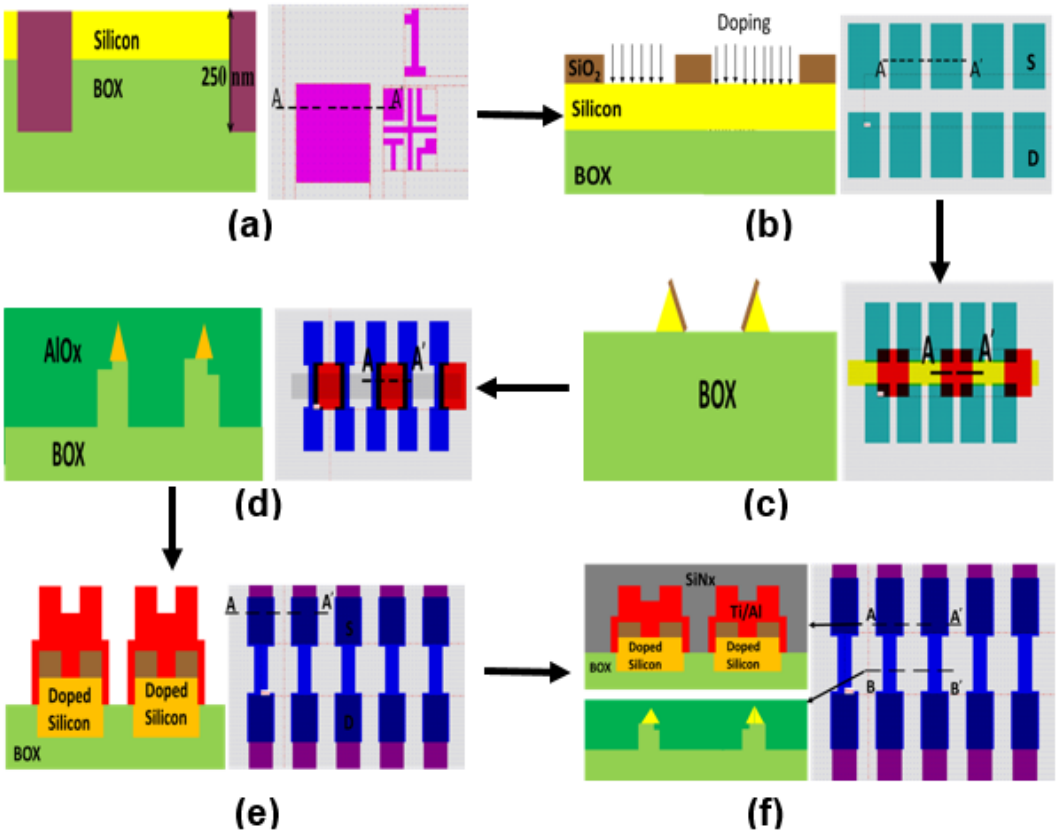

Figure 6.3: Main process steps for the fabrication of silicon nanowire field effect sensor: (a) Printing the alignment marks; (b) doping the source and drain; (c) fabrication of the silicon nanowire (see Figure 3.4 for full fabrication process of the nanowire); (d) deposition of the aluminium oxide to act as an active sensing layer; (e) deposition of the source/drain contacts; (f) deposition of the silicon nitride layer to act as a passivation layer. The cross-sections A-A' and B-B' are views of the layout.

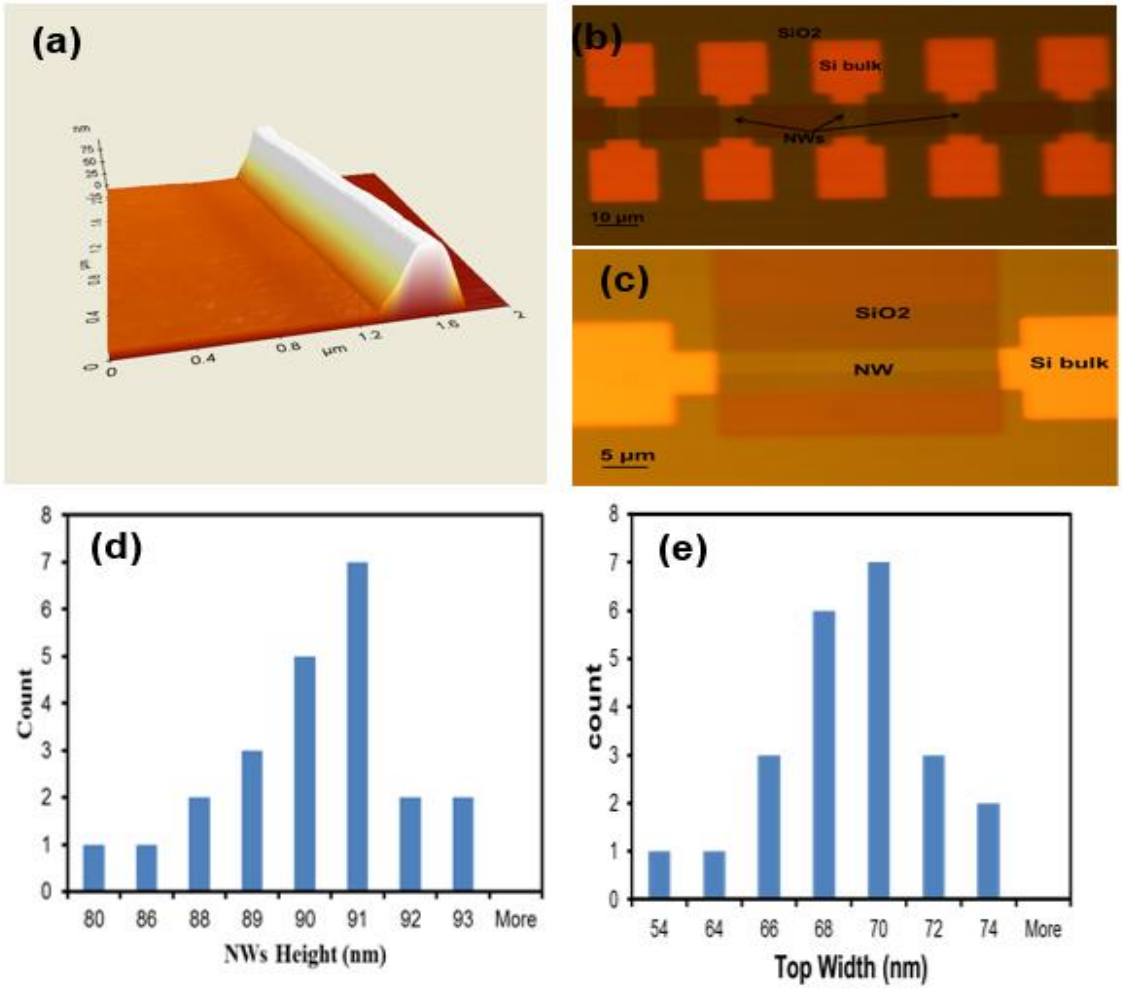

Figure 6.4: (a) An AFM image of the nanowire used as a sensor; (b) and (c) microscopic images showing the two types of structures of a bundle of five and a single nanowire; (d) and (e) histograms showing uniformity in thickness and width for 23 nanowires.

6.3 pH measurements

6.3.1 Measurement set-up

The samples were cleaned with acetone (5 mL), propanol (5 mL), deionised water (5 mL), and acetone (5 mL) and then dried with nitrogen. Samples were subsequently baked at 120 °C for 30 min under vacuum. The samples were then activated using plasma Asher at 28 W, with 5 sccm oxygen flow rate for 30 sec. Following plasma Ashing, the chip was immediately inserted into 1% 3-aminopropyl-dimethyl-ethoxysilane (APDMES) in anhydrous toluene solution at 65 °C for 18 h. The samples were subsequently rinsed with toluene and baked at 100 °C for 30 min under vacuum, to cure the silane modification. A 0.1 ionic strength buffer was prepared at a range of values of pH (pH 4-8) to determine the nanowire sensitivity and stability as a function of pH change.

A custom-made microfluidic chamber was then placed on the chip and a double tape was used to adhere the chamber to the chip. A micropipette was used to pump the buffer solution through the microfluidic chamber. Electrical measurements in the solution were performed, applying a gate voltage on an Ag/AgCl reference electrode which was used as a front gate. Prior to any gate sweeping, the samples were placed in the buffer solution for 10-15 min to ensure the stabilization of the electrolyte/solution interface. The measurements were performed using a Keithley 4200 Parameter Analyzer.

It should be noted that the results described in the following sections are preliminary results where the electrical measurements were performed only on two chips.

6.3.2 Dry test

The electrical characterisation of silicon nanowires was performed initially in dry conditions under ambient conditions. The nanowires were lightly doped with boron, while the source and drain were heavily doped with phosphorous to form ohmic contacts. In these measurements, the gate voltage was swept from -1.5 V to 1.5 V and a constant voltage of 0.4 V was applied between source and drain. The transfer characteristics are shown in Figure 6.5. The increase in gate voltage leads to a rise in the current, which indicates that the devices exhibit n–type characteristics. Nevertheless, the current at a zero gate voltage continues to flow (Figure 6.5(b)). This clearly suggests that an inversion channel is formed at the interface. This inversion channel could be formed by the presence of fixed and positive interface charges at the nanowire interface, which consequently causes the holes to be depleted near the interface. If the interface charges are large, the surface of the nanowire becomes weakly inverted, which leads to the current flow and shift in threshold voltage as described in Equation 6.1.

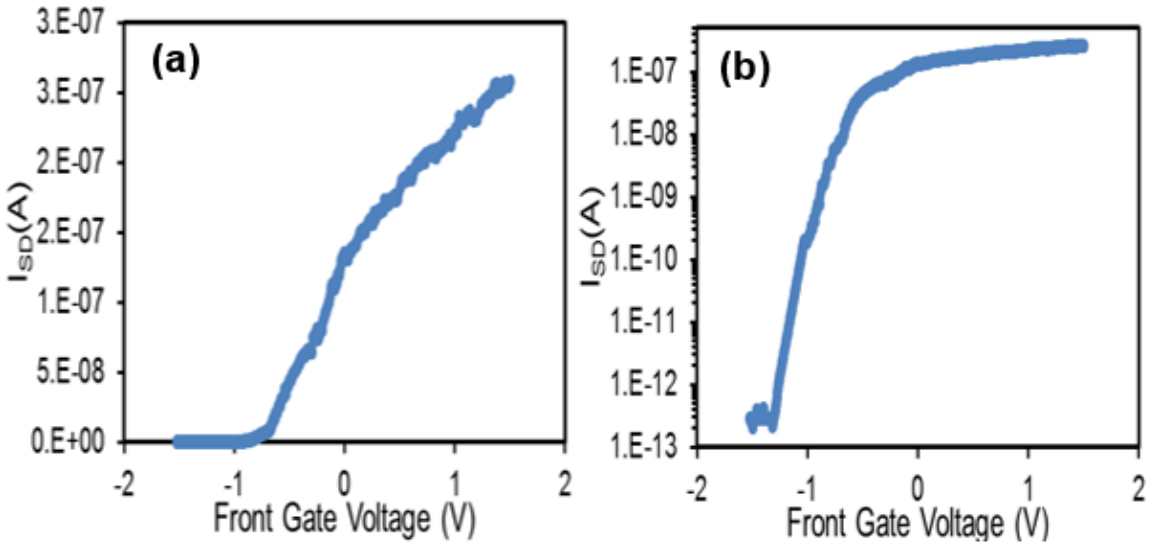

Figure 6.5: Transfer characteristics of silicon nanowire field effect transistor: (a) linear scale; (b) logarithmic scale.

6.3.3 pH response

Silicon nanowires used in this study are based on the inversion-mode of operation and have (n^+- p- n^+) configurations. A change in pH value leads to a change in the electron carrier concentration in the channel, which leads to a modulation of nanowire conductance. Figure 6.6 shows the transfer characteristics of silicon nanowires with different pH values and at fixed V_{sd}=0.4 V. The figure shows n-type characteristics with a shift towards a more positive value when the pH changes from 4 to 8. This shift is due to a reduction in surface potential which increases the negative charge at the surface of the oxide when the pH changes from low to a high value.

It should be noted that the transfer characteristics show that a large current passes through the nanowire channel even at zero gate voltage, which should not appear in the normally-off channel. The source of this large current flow could be due to a parasitic path between the buffer solution and source/drain, as discussed below in section 6.4. This large leakage current could lead to a large error in determining the threshold voltage and the sensitivity of the device.

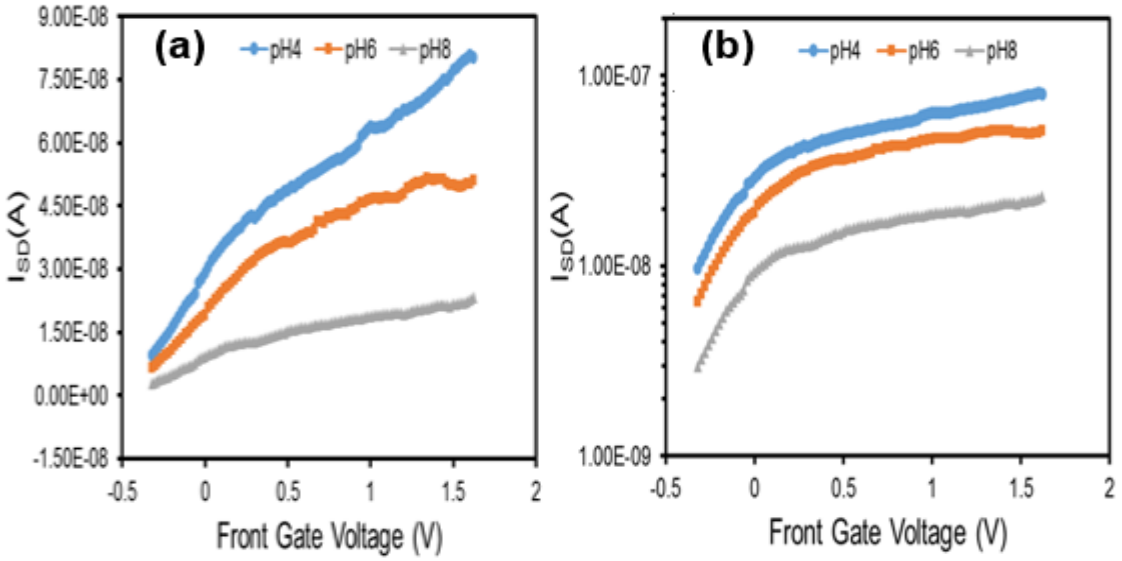

Figure 6.6: Transfer characteristics of source-drain current for different pH solution buffers, V_{sd}=0.4 V: (a) linear scale; (b) logarithmic scale.

6.3.4 pH dynamic measurements

The pH response was also measured as a function of time. This type of measurement is particularly important in biosensing applications in order to distinguish between the signal due to the proton interaction from that due to the noise signals, especially for highly sensitive detection. The nanosensor response to the change in pH as a function of time is

presented in Figure 6.7. The gate bias was set to V_{fg} = 0.3 V and V_{sd} = 0.7 V. The reduction in current with increase of pH was observed to be almost linear (Fig. 6.7(b)). This linear relationship is attributed to the existence of an amino −NH2 group at the surface of the sensing layer due to the modification of the surface with APDMES in addition to the silanol −SiOH groups, where −NH2 protonate into $-NH3^{+}$ at low pH values while −SiOH deprotonates into $-SiO^{-}$ at high pH [9, 10].

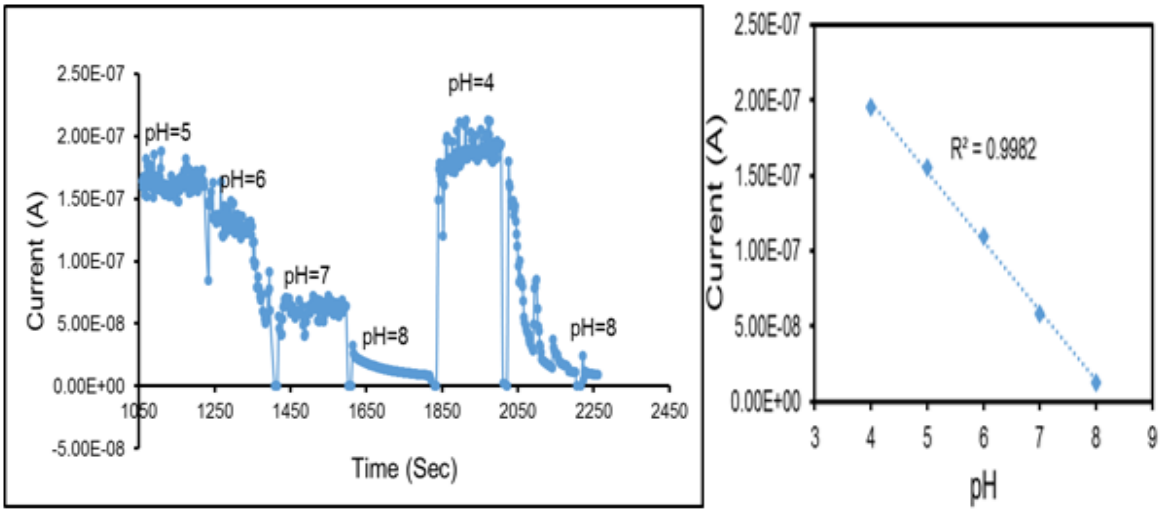

Figure 6.7: Transfer characteristics of source-drain current for different pH solution buffers, V_{sd}=0.7 V and V_{fg} = 0.3 V.

6.4 Null results

The above sections have presented the response of the nanowire to changes in the pH value of the solution. However, the sensors obtained in this study give low yield detection and there are reliability issues. Various factors could have caused the low reliability and low yield in the measurements:

6.4.1 Parasitic leakage current between the source/drain and buffer solution

A large leakage current between the source/drain and the front gate was observed as shown in Figure 6.8. This large parasitic current was observed even in the presence of a 70 nm layer of silicon nitride to isolate the source/drain from the solution. The large leakage current could be due to two factors:

a. Pinholes inside the passivation layer (silicon nitride) or defects at the metal electrodes. The silicon nitride was deposited using physical vapour deposition

(PVD), which does not result in a coating which is conformal to the shape of the structures; thus, it is expected that a discontinuity of the silicon nitride film on a polycrystalline structure such as aluminium will be observed. This could lead to a reaction between the protons in the solution and metal particles.

b. Large electrode area under the microfluidic channel: In this study, the microfluidic channel has a width of about 3 mm and the electrodes have an average width of 66 µm. This large area can allow a large leakage current through the passivation layer and this could be particularly likely to increase in the case of any defects in the passivation layer.

Leakage through the active sensing layer (aluminium dioxide) is unlikely to occur because the aluminium dioxide was deposited using ALD, which leads to a good coating and a smooth surface.

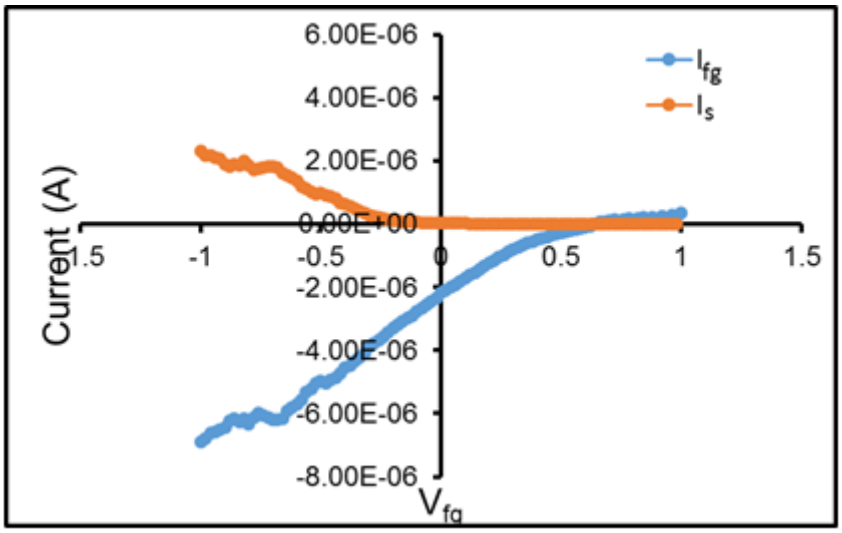

Figure 6.8: Transfer characteristics of a nanosensor in the buffer solution and the leakage current between the front gate (V_{fg}) and the source/drain.

6.4.2 Voids in the metal electrodes

Figure 6.9 shows microscopic images of an as-deposited Al/Ti metal electrode and another three months after deposition (including annealing steps). The image in Figure 6.9(b) clearly shows voids in the electrode regions after long exposure to air. The origin of these voids could be due to the diffusion of aluminium into titanium after the annealing steps (normally in this research at 380℃) [11-13] or stress-migration due to the influence of humidity and contamination in addition to the effect of the stress that could occur after the deposition of the insulating layer [13-15]. The distribution of metallic particles outside the metal electrode can increase the leakage current and if these particles are present inside the active sensing region they can interact with protons in the buffer solution and affect the reliability and performance of the device.

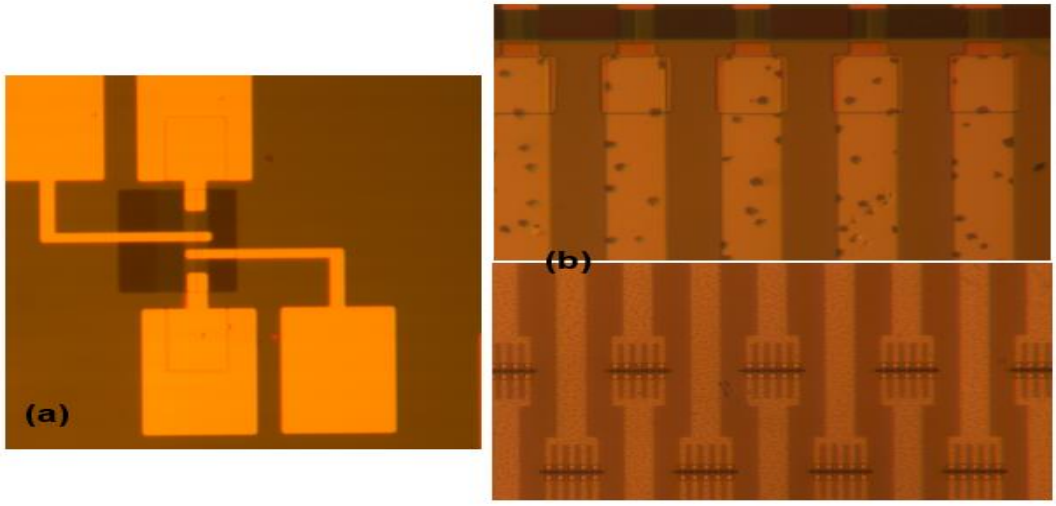

Figure 6.9: (a) Microscopic image of an as-deposited Al/Ti metal; (b) microscopic image of metal electrode after a long period of exposure to air.

6.5 Summary

This chapter describes the fabrication and characterisation of silicon nanowire sensors. The electrical characterisations were performed mainly to study the response of nanowire to changes in pH value. The pH measurements were performed by sweeping the gate voltage in the linear region. Nanowires detect the change in the pH value and a linear response between the change in pH value and the current is observed. However, the reliability and the yield are low. This chapter offers some possible explanations of the low device sensing yield, which is mainly related to the current mask design.

6.6 Future work

In this chapter the behaviour of silicon nanowires in aqueous media has been studied. However, as mentioned earlier, there are serious concerns about reliability and yield in the device performance. Therefore, some important design considerations and other technical factors should be taken into account in order to obtain reliable and high-yield device performance.

a. The parasitic leakage current between the source/drain and the buffer solution should be reduced. This can be achieved by:
   i- Reducing the contact area between the source/drain and the solution. To do so, the source/drain region should be reduced, as should the electrode area under the solution. In the current layout, the dimensions of the source/drain region are 40 μm X 40 μm and the width of the metal electrodes under the buffer solution is about 66 μm. The dimensions of these structures can be

reduced to below 5 μm without affecting the formation of ohmic contact, as described in section 4.2. The reduction of contact area under the buffer solution can also reduce the probability of finding defects in the contact region between the solution and the source/drain. In the NCL EEE cleanroom, a feature of 2 μm in width can be produced. Thus, it is recommended to use this particular width when designing the source/drain/electrode.

ii- Good coating is required to completely isolate the source/drain from the buffer solution. The passivation layer used in this study was deposited using the physical vapour deposition method, which is a directional method. Therefore, it is recommended to that Plasma-enhanced chemical vapour deposition (PECVD) silicon nitride which offers better coating, compared with physical vapour deposition (PVD) should be used. However, this method can induce a large stress on the film underneath, requiring high temperature deposition conditions. Alternatively ALD Al_2O_3, which offers good coating could be used.

b. The samples should be stored in vacuum conditions.

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Chapter 7

Thesis Review

Four main subjects have been investigated in this thesis: the optimization of the fabrication process of silicon nanowires using optical lithography, thermal oxidation and anisotropic wet etching; the characterisation of fabricated devices and the development of models and simulations to evaluate the effect of the nanowire's surface properties on their electrical properties and the integration of silicon nanowires into a functional device for chemical sensing.

7.1 Concerning the optimization of the fabrication process of silicon nanowire

The key issues that have been investigated are how to achieve a reproducible and high yield fabrication process and how to form high quality nanowires with a controllable structure.

7.1.1 Reproducibility and yield

It has been shown that the appropriate selection of silicon nitride film, the oxidation method and the characteristics of the anisotropic etchant are the key parameters that affect the reproducibility of the process.

The selection of silicon nitride film affects the reproducibility of the process because most silicon nitride films oxidize partially or completely during thermal oxidation. Moreover, oxidised silicon nitride film has lower etch selectivity over silicon dioxide in boiling phosphoric acid compared with as-deposited silicon nitride. Therefore, the silicon nitride film which has the highest resistance to thermal oxidation and the highest etch rate in boiling phosphoric acid is preferable in order to obtain a highly repeatable process. In this thesis, the refractive index of silicon nitride has been used to determine the robustness of the film during thermal oxidation, where for lower the refractive index there is higher resistance to thermal oxidation. Using two fitting models developed in chapter three it has been found that nitrogen-rich silicon nitride with a refractive index between 1.9-1.95 has the highest resistance to thermal oxidation. For example, the total oxynitride ratio of oxidised silicon nitride to the silicon dioxide thickness on bare silicon is found to be more

than 1 for silicon nitride with a refractive index of 2.37 and less than 0.3 with a refractive index of 1.9. This film also has the highest etch rate in boiling phosphoric acid. The etch selectivity of nitride-rich silicon nitride after oxynitride removal to silicon dioxide in boiling phosphoric acid has been found to be 4.1-7.0, whereas it is 3.3-3.7 for silicon-rich silicon nitride. These two properties make nitride-rich silicon nitride more suitable for a highly reproducible process. The thickness of silicon nitride is another important parameter affecting reproducibility. Equation 3.9 is used to determine the maximum thickness of silicon nitride that can be used as a mask, and this is linked to the etching selectivity of silicon nitride to silicon dioxide together with the thickness of silicon dioxide on bare silicon. The characterisations of silicon nitride films are documented in section 3.4.1.

The method for oxidation of the sidewall is another factor that should be carefully considered to obtain a reliable process in multilayer structures such as SOI. Lamp-based RTP radiation and a furnace with resistive heating are the methods that have been used to grow sidewall oxide. Oxidation using lamp-based RTP radiation is always expected to result in thinner oxide on the SOI sample compared with a bare silicon sample when both are oxidised at approximately the same temperature and for the same period of time. This is not the case during oxidation using a resistive furnace. To achieve a successful process, it is important to determine the variation in oxide thickness if lamp-based RTP radiation is used as an oxidation method for the sidewall. The characterisation of thermal oxidation is documented in section 3.4.2.

The reproducibility of the process also depends on the wet etching method chosen, using either TMAH or KOH. This is most important during the second anisotropic wet etching process which requires very high selectivity etching of silicon to silicon dioxide in order to prevent the consumption of the sidewall oxide mask. TMAH etchant can offer a more reliable process than KOH etchant because the former etches the silicon dioxide at a much slower rate than does KOH. The characterisation of TMAH and KOH for nanowire fabrication is documented in section 3.4.4.

When the above issues are taken into account, the fabrication method offers high yield over the wafer scale and the overall yield of this process can exceed 95%.

7.1.2 Controllability of the nanowire

The length of nanowire is well controlled by the lithography step. However, the shape, width and height of the nanowire are controlled by carefully designing the conditions in which the first and the second wet etching take place. A trapezoidal cross-section can be obtained by performing anisotropic etching for a short time during the first and second anisotropic etching. Meanwhile, increasing the duration of the second etch results in nanowires with a triangular cross-section. The exact time to be used depends on etchant conditions such as concentration and temperature. The thickness of the nanowire can be simply designed by controlling the length of time that the samples are placed in the etchant during the second anisotropic etching step. A high etchant concentration with relatively low etch temperature are favoured to obtain better control of nanowire thickness. TMAH and KOH have been employed to control the size of the nanowire. A well-controlled nanowire size has been obtained using TMAH for etching. Nanowires with a thickness less

than 10 nm have been fabricated using a controllable TMAH etching step. However, due to its etching of the sidewall oxide, etching using KOH requires careful consideration, especially when employed to produce very fine nanowires. The minimum size of the nanowire which can be obtained after KOH etching depends on the etch rates of <111> silicon and silicon dioxide and the total thickness of oxide on the sidewall, as described in equation 3.14 and Figure 3.26. Controlling nanowire structure during the second anisotropic wet etching step has been documented in sections 3.3.3.1 and 3.4.3.6.

The size and the shape of silicon nanowires have also been controlled using thermal oxidation. The experimental measurements and TCAD simulation data have shown non-uniformity in the nanowire profile after using thermal oxidation. These results have been documented in section 3.3.3.2.

7.2 Characterisation of devices

The profiles of the silicon nanowires have been obtained by using atomic force microscopy (AFM), and a simple model is developed to determine the apparent increase in nanowire width due to the AFM tip geometry. Modelling the tip effect on nanowire width has been documented in section 3.3.2.2.

Two issues concerning the electrical properties have been investigated: contact issues and the electrical properties of the silicon nanowire itself.

With regard to contact issues, the stability of the contact structure and the contact properties have been investigated. For thermal stability, the three contact metallisation schemes Al/Ti, Al/W/Ti and Al/Ti/AlOx to silicon and silicon nanowire are tested at different annealing temperatures ranging from 250 °C to 425 °C. It has been found that the Al/Ti/Si and Al/W/Ti/Si structures are thermally unstable at the annealing temperature of 425 °C, while the Al/Ti/AlOx/Si structure is stable at this temperature. The optimal annealing temperature for Al/Ti/Si and Al/W/Ti/Si structures has been found to be 380 °C. As for contact properties, the transfer length model (TLM) and four probe methods have been used to measure the specific contact resistivity and contact resistance for contacts to a thick silicon layer and the silicon nanowire. The properties of two contact methods have also been investigated. In the first method the contacts are made to thick silicon and a nanowire is connected between them; and in the second method the contacts are placed directly on the nanowire. The contact resistance in the former method has been found to contribute to less than 3% of the total resistance, while it is found to contribute to about 10 % of the total resistance in the latter. It has also been found that, when the contacts are placed directly on the nanowire, the contact resistance increases by a factor of four while the cross-section is reduced from about 12500 nm^2 to about 4800 nm^2. The results concerning contact properties have been documented in section 4.2.5.

The electrical resistivity (ρ) of nanowires has been measured using the four probe method. The measured electrical resistivity of nanowires is found to be size-dependent and follows the relationship: $\rho \propto t^{-n}$. The electrical resistivity measurements have been documented in 4.3.1.

Non-linear four-probe current-voltage characteristics have been observed in heavily and moderately-doped silicon nanowires. The temperature measurements of the characteristics in heavily-doped devices has been found to be temperature independent, while in moderately doped devices the nonlinearity has been found to be temperature dependent. Due to the elimination of non-linearity in heavily-doped devices after annealing, it is claimed that the origin of the non-linearity is possibly due to a large density of traps. These results have been documented in section 4.3.2.

7.3 Models of device properties

Several models have been developed to describe the electrical properties of the silicon nanowire, and in particular to understand the apparent increase in measured electrical resistivity with the decreasing thickness of the silicon nanowire.

The effect of dopant distribution has been estimated by applying both error function complement *erfc* and Gaussian distribution functions. After subtracting the effect of the dopant from the measured resistivity, an increase in resistivity has still been observed. This indicates that the doping effect alone cannot explain the increase in resistivity with decreasing thickness of nanowire. The doping profile has been documented in sections 2.2.4 and 5.2.

The kinetic-theory argument has been used to calculate the effect of surface scattering due to surface roughness on the electrical resistivity of the nanowire. The results indicate that resistivity is largely affected by surface scattering at nanowire thicknesses less than 25 nm.

The main effect on electrical resistivity has been estimated from the reduction of conductive area of the nanowire due to interface traps.

Using 3D TCAD simulation, it has been proven that the electrostatic potential and current density inside triangular and circular cross-sections with the same cross-section area are approximately the same in both structures. Based on this finding, Poisson's equation for a circular cross-section has been used to find the electrostatic potential and depletion region in triangular cross-section. Surface-depletion due to interface traps along with the TCAD results have been documented in section 5.3

7.4 Nanowire integration for chemical sensing

A first attempt has been made to integrate nanowires into functional devices for chemical sensing. Preliminary results of the pH measurements show a linear response between the change in pH value and the nanowire response. However, reliability and yield are low due to the large parasitic current between the source/drain and the buffer solution.

7.5 Recommendations for future research

Application of silicon nanowires for the sequencing of DNA: It has been shown in this study that nanowires can be fabricated with high yield and controllable dimensions with only small variations from one device to another. The ability of the nanowires to measure

changes in pH has also been demonstrated. A next step could be to use the nanowires for DNA sequencing, in partnership with companies pursuing such applications with alternative nanowire technologies. The detection of DNA can be achieved through PNA/DNA hybridization, where the PNA is immobilized on the surface of the gate oxide of the nanowire after suitable surface treatment. Then the DNA can be added to form a heteroduplex with a PNA probe which can be detected as a change in nanowire conductance. However, for reliable and high yield measurements, it is recommended to consider the issues related to the layout design as mentioned in section 6.4.

Nanowire thermoelectrics: The silicon nanowires fabricated in this study can offer the possibility to fabricate highly efficient thermoelectric devices. This exploits the ability to control the quality of the surface during the fabrication process. It has been shown that surface roughness can be tuned during anisotropic wet etching and, more importantly, surface roughness has been shown to have no impact on electrical resistivity until the thickness of the nanowire becomes smaller than 40 nm. Therefore, it should be possible to tune thermal conductivity without affecting electrical conductivity.

Appendix A

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Silicon nitride films deposited using Kurt J. Leasker PVD75

a. Deposition rate, etch rate and optical property

Table A.1: Deposition rate, etch rate and optical property.

Technique	T(°C)/P(W)/P (mtorr)	Deposition rate (nm/min)	Film thickness (nm)	Etch rate BHF (nm/s)	Average refractive index	Etch rate H_3PO_4 158-170 °C (nm/min)
Kurt J. Lesker PVD75 Pure Ar	25/100/9	0.48	40	4	1.71	>20
Kurt J. Lesker PVD75 Pure N_2	25/100/9	0.2	25	9	1.57	>20

The value of refractive indexes are smaller than 1.9 which could be due to the incorporation of oxygen in the film which could result from the nitrogen gas with oxygen contamination.

b. Etching of thermally oxidised silicon nitride

Table A.2: Etching of thermally oxidised silicon nitride.

Silicon nitride film	Etching Selectivity over SiO_2	The average oxide consumption during the removal of SiO_2/SiO_xN_y
Kurt J. Lesker PVD75 Pure Ar	3.7 - 4.6	$0.35t_{tot}$
Kurt J. Lesker PVD75 Pure N_2	3.4 - 4.4	$0.55t_{tot}$

Appendix B

a. Fabrication process flow for nanowires with Al/Ti and Al/W/Ti contact structures

SOI samples details:

Top silicon thickness Si=155 nm;

BOX = 145 nm

Doped phosphorus using SOD n-type in the range of 4.5 X 10^{18} to 7.5 X 10^{18} cm^{-3}

Table B.1: Nanowires with Al/Ti and Al/W/Ti contact structures.

Step No.	**Fabrication step**	**Fabrication details**
1	Piranha cleaning	3:1 H_2SO_4:H_2O_2 for 10 minutes
2	RCA cleaning	0.75:1 NH_4OH: H_2O_2 for 6 minutes 0.75:1:1 H_2O:H_2O_2:HCL for 10 minutes
3	Oxide growth	40 nm oxide grown in furnace
4	Spin-coating	Clean using NMP, IPA, spin at 5000 rpm
	Pre-exposure bake	At 90 ºC for 20 minutes
	Photolithography	It is carried out using contact aligner for 12 seconds.
	Development	For 41 seconds
	Post-exposure bake	Bake at 115 ºC for 15 minutes.
5	SiO_2 etching	Etch the SiO_2 using BHF
6	Remove Photoresist	NMP 2 min, IPA 2 min

7	Silicon nitride deposition	Silicon nitride deposited using Sputter RF power: 150 watts @ 13.56 MHz N2 flow: 50 sccm Pressure: 10 mTorr Temperature: 90 °C Deposited thickness=25 nm
8	Photolithography	Repeat the same process in 4
9	Si_3N_4 etching	BHF 30 sec
10	Anisotropic wet etching	TMAH 25wt% +7.5% IPA, temperature 56 ºC for 3 min
11	Oxidation	Furnace oxygen flow=500sccm T=930 ºC Time=30 min Thickness = 18 nm
12	Si_3N_4 etching	Remove silicon nitride in ion milling 2 min, boiling phosphoric acid 4 min
13	Anisotropic wet etching	TMAH 25wt%, + 7.5% IPA temperature 56 °C
14	BHF dip	BHF 10 sec
15	Photolithography	Repeat the same process in 4
16	Device isolation	RIE using SF_6/O_2, 10 min NMP 10 min Piranha
17	Piranha and RCA cleaning	Repeat steps in 1 and 2.
18	Oxidation	BHF 3 sec, Oxidation for 12 min at 930 °C
19	Photolithography	Repeat the same process in 4
20	Contact opening	BHF for 15 sec
21	Photolithography	Repeat the same process in 4
22	Metallization	BHF for 2 sec, Asher 1 min, e-beam evaporator Al/Ti (100/70) or Al/W/Ti (100/20/70)
23	Lift-off	Acetone 10 min

b. Fabrication process flow for nanowires with Al/AlOx/Ti contact structure

SOI samples details:

Top silicon thickness Si=155 nm;

BOX = 145 nm

Doped phosphorus using SOD n-type in the range of 4.5 X 10^{18} to 7.5 X 10^{18} cm^{-3}

Table B.2: Nanowires with Al/AlOx/Ti contact structure.

Step No.	Fabrication step	Fabrication details
1	Piranha cleaning	3:1 H_2SO_4:H_2O_2 for 2 minutes
2	RCA cleaning	0.75:1 NH_4OH: H_2O_2 for 6 minutes 0.75:1:1 H_2O:H_2O_2:HCL for 10 minutes
3	Oxide growth	40 nm oxide grown in furnace
4	Spin-coating	Clean using NMP, IPA, spin at 5000 rpm
	Pre-exposure bake	At 90 ºC for 20 minutes
	Photolithography	It is carried out using contact aligner for 12 sec
	Development	For 41 seconds
	Post-exposure bake	Bake at 115 ºC for 15 minutes.
5	SiO_2 etching	Etch the SiO_2 using BHF
6	Remove Photoresist	NMP 2 min, IPA 2 min
7	Silicon nitride deposition	Silicon nitride deposited using Sputter RF power: 150 watts @ 13.56 MHz N2 flow: 50 sccm Pressure: 10 mTorr Temperature: 90 °C Deposited thickness=25 nm
8	Photolithography	Repeat the same process in 4
9	Si_3N_4 etching	BHF 30 sec
10	Anisotropic wet etching	TMAH 25wt% +7.5% IPA, temperature 56 ºC for 3 min
11	Oxidation	Furnace oxygen flow=500sccm T=930 ºC Time=30 min

		Thickness = 18 nm
12	Si_3N_4 etching	Remove silicon nitride in ion milling 2 min, boiling phosphoric acid 4 min
13	Anisotropic wet etching	TMAH 25wt%, + 7.5% IPA temperature 56 °C
14	BHF dip	BHF 10 sec
15	Photolithography	Repeat the same process in 4
16	Device isolation	RIE using SF_6/O_2, 10 min NMP 10 min Piranha
17	Piranha and RCA cleaning	Repeat steps in 1 and 2.
18	Oxidation	BHF 3 sec, Oxidation for 12 min at 930 °C
19	Photolithography	Repeat the same process in 4
20	Contact opening	BHF for 15 sec
21	Deposition of ALD AlOx	TMA (adduct grade, SAFC, 35 °C) and H_2O (DI, 25 °C). 0.02 sec pulse times for both. 2 sec (TMA) and 6 second (H2O) purge times respectively, Base pressure : 2e-06 Torr Temperature : 250 °C Thickness = 0.6 nm
22	Photolithography	Repeat the same process in 4
23	Metallization	BHF for 2 sec, Asher 1 min, e-beam evaporator Al/Ti (100/70)
24	Lift-off	Acetone 10 min