Current Fed Multilevel Converters for High Current Power Applications

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Abstract

The majority of the worldwide installed power inverters today are voltage source inverters followed by current source inverters where the concluding decision lies with the performance of the applications besides the usual economic reasons. Recent active development in the current source inverter areas has seen the emerging of various generalized multilevel current source inverter topologies analogous to the existing multilevel voltage source inverter families. To date, the multilevel current source inverter families have been classified principally by the physical appearance of their basic structures and also by the number of current sources employed. The existing multilevel current source inverter topologies are unpopular for present applications due to reasons such as big sizes, high control complexity and low reliability; which circumstances are often associated to massive component counts and multiple requirements of current sources. Therefore, this research has been focused on the single-phase single-source generalized multilevel current source inverter for this apparent advantage; where this thesis proposed a novel generalized multilevel current-source inverter topology with the lowest component utilization while employing just a single current source. In addition, the proposed topology can conveniently achieved dc current balance with a simple low frequency switching strategy for the five- and nine-level current outputs. From comparison analysis, the proposed topology has significantly less number of components employed compared to the nearest topology, which implies low implementation cost. The experimental results verify the characteristics and performances of the proposed topology acquired by computer simulations.

Dedication

To my late father, my mother and my family

Acknowledgement

First and foremost, my most sincere appreciation goes to my supervisor, Prof. Volker Pickert for his guidance, encouragement, and relentlessly giving support and ideas to make this research successful. I am also very grateful to Dr. Bashar Zahawi as the co-supervisor for many valuable lessons.

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List of Abbreviations

CML	Current Multilevel Cell
CSI	Current Source Inverter
DF	Distortion Factor
DPF	Displacement Power Factor
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Transistor
GTO	Gate Turn-Off Thyristor
LCI	Load Compensated Inverter
LFM	Low Frequency Modulation
MCSI	Multilevel Current Source Inverter
MVSI	Multilevel Voltage Source Inverter
OHSW	Optimized Harmonic Stepped-Waveform
PF	Power Factor
POD-PWM	Phase Opposition Disposition - Pulse Width Modulation
PWM	Pulse Width Modulation
PWM-CSI	Pulse Width Modulation – Current Source Inverter
RMS	Root-Mean-Square
RS	Redundant Switching
RS-MPM	Redundant Switching – Multi-Pulse Modulation
SCR	Silicon-Controlled Rectifier
SHE	Selected Harmonic Elimination
SHE-PWM	Selected Harmonic Elimination – Pulse Width Modulation
SPWM	Synchronized Pulse-Width Modulation
THD	Total Harmonic Distortion
TPF	Total/True Power Factor
VSI	Voltage Source Inverter

CHAPTER 1

An Overview of Multilevel Inverters

1.1 Introduction

In the last decades, inverters have found many usages in different power segments from low to medium to high power applications whether simply as domestic DC to AC converters or as medium to high power converters in AC drives. The advancement in modern industrial machines with various AC power requirements and the growth of the renewable energy sources as alternatives to fossil fuels which naturally produce useful DC power boost the research and development activities in the field of inverter technology. Though in general inverters basically converters that convert DC power to AC power, their circuits are not uncomplicated; where, multiple research fields can be explored such as the development of power semiconductors, methods of switching and controls, inverter topologies, or industrial converter applications.

Fundamentally, as shown in Fig. 1-1, there are two types of inverters existed; the voltage source inverter (VSI) and the current source inverter (CSI). In general, an inverter that exploits the input voltage while producing controlled output voltage is classified as the VSI whereas an inverter that exploits the input current while producing controlled output current is classified as the CSI. The VSI is the more mature and proven technology where it has been successfully implemented in industry for decades [1-5]. While the 2-Level VSI has found applications in many conventional industrial machines; the multilevel VSIs are more recent and established in industry due to its advantages in particular able to generate multilevel stepped-waveform with reduced harmonic distortion, able to reach higher voltage operation, and higher modularity [3, 6]. On the other hand, the CSI load-commutated inverters (LCI) are among the earliest inverters used for variable speed drives [7, 8] before slowly being replaced by the pulse-width modulation (PWM) CSI mostly in induction motor drives.

Quite recently, similar to the VSIs, multilevel CSIs are gaining attention in new research activities [9, 10]. While both types of inverter have substantial differences topologically, they do share the same working principles. Thus, in general, common control methods and common power semiconductor switches used for VSI can also be applied to CSI with some modifications [11].

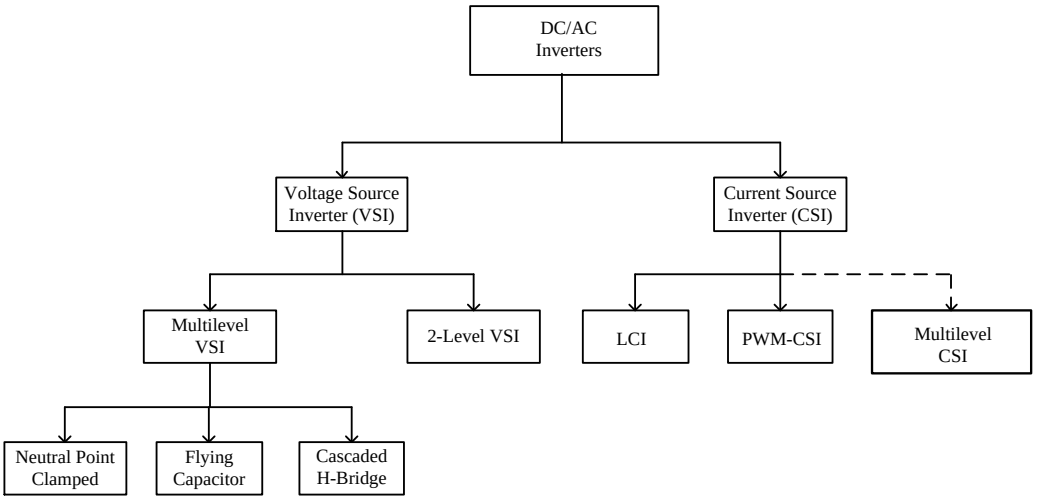


Fig.1 - 1: General Classification of Inverters

Today the majority of the worldwide installed power inverters are voltage source inverters (VSI) followed by current source inverters (CSI). Current source inverters are available as industrial drives [7, 12-15], and have also been connected to wind power and solar power generators [16] and fuel cell systems [17, 18]. Comparison between VSIs and CSIs have been reported many times [19-22] concluding that the decision lies with the performance of the application. Both inverters, however, face the same challenges; generally they have to be small, light and low cost and technically they have to operate at high efficiencies, produce low harmonics, are simple to control and must be reliable. For high voltage and high current application this has led to the introduction of multi-level topologies, first for VSIs like the diode-clamped, flying capacitor and cascaded topologies [23-25] and later to CSIs [7, 26-28]. With the

dominating VSI market research into multi-level current source inverters (MCSI) has been limited. The reason for the lag of interest is, beside the dominance of the VSI in the market, the large component count that is required to build MCSI in particular for a level higher than five i.e. an existing nine-level CSI requires three inductors and twelve power switches. This number goes up rapidly when upgrading the inverter to even higher level of currents. For example a seventeen-level CSI can have seven inductors and twenty power switches.

Recent active development of MCSI has seen the emergence of generalized multilevel CSI topologies besides the existing classical LCI and PWM-CSI topologies. However, since none specific multilevel CSI family has been universally established, their classifications are author oriented. For example, a generic multilevel CSI shown in Fig.1-2 uses a single current source where inductors acting as current sources to ensure equal current division among switches. The switches and inductors are integrated in one single structure. It was reported that the output current harmonics minimization and inductor current balance are achieved without the use of high-frequency modulation or closed-loop control [10]. A modified version of the MCSI as shown in Fig. 1-2 is represented by Fig. 1-3 [29]. It can be seen that the current returning paths of the former circuit have been simplified to only two switches. Thus the latter has achieved reduced number of components in a circuit though it should be highlighted that the returning switches must be in much higher ratings than the rest of the switches. In Fig.1-4 [30], although the generic topology also employs a single current source; however, the structure is classified based on the two isolated stages of the DC-bus current-controlling stage and the current-inverting stage. Similar to previous circuits, the inductors acting as the current sources to ensure equal current division among switches while the switch-combinations and also the switching sequences are manipulated to achieve the inductor current balance. Another classification as depicted in Fig. 1-5 [31] is based on two basic main circuits: H-bridge-based and common-emitter-based topologies. Similar to the circuit in Fig. 1-4, it is built with a single current source but multiple stages. While the first stage is to invert the source current into dual polarity, the second stage is to developed stepped-current waveform where

inductors are used to ensure equal current division among switches. The circuit operations will be discussed further in the next Chapter 2.

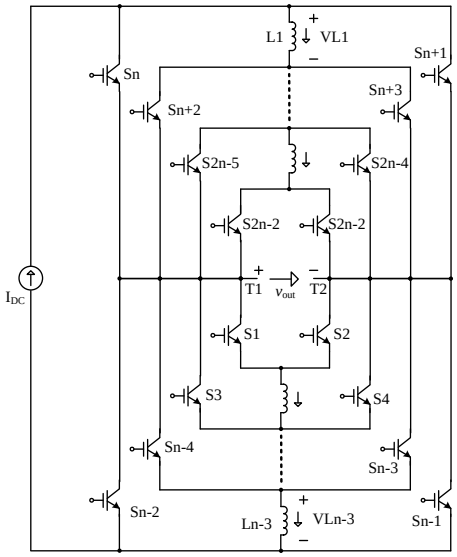


Fig.1 - 2: The generalized structure of Topology I

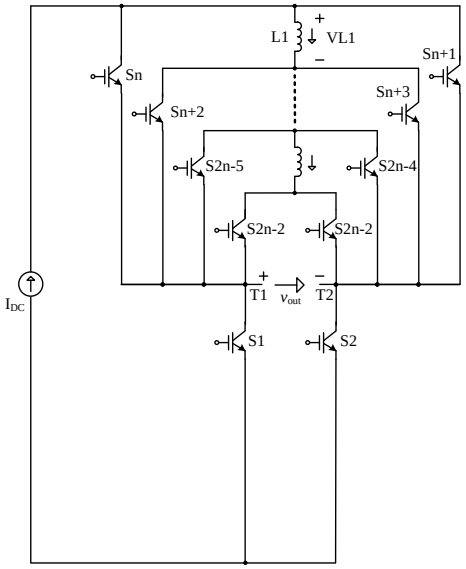


Fig.1 - 3: The generalized structure of Topology II

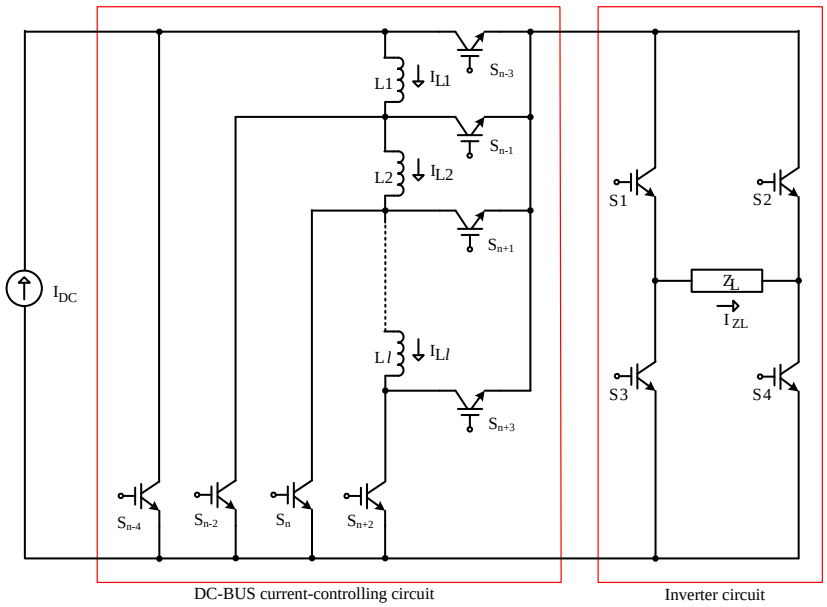


Fig.1 - 4: Generalized structure of Topology III

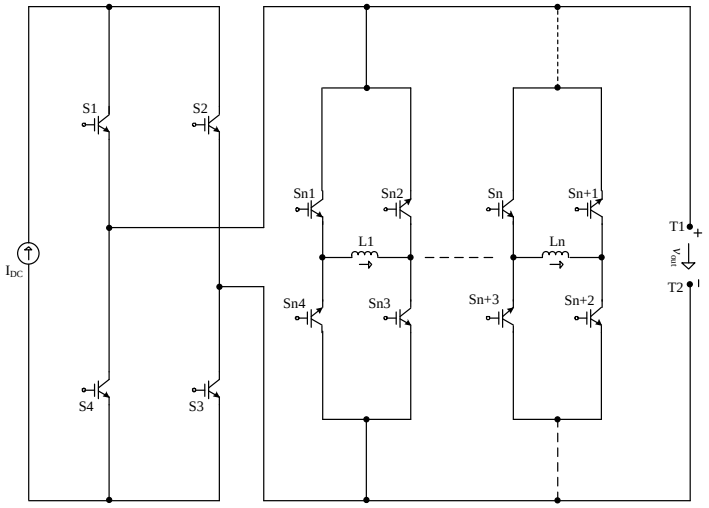


Fig.1 - 5: Generalized structure of Topology IV

Based on the discussions, the CSI cluster is revised in Fig. 1-6 where the Generalized MCSI is divided into single-stage, multi-stage and cascaded topology. The single-stage generalized MCSI is supplied with a single current-source before being split by sharing inductors and methodically forwarded to the load all in one integrated structure. On the contrary, the multiple-stage converter has two-or more isolated stages

that in combination forms a complete structure of a converter where these converters may have a single-or multiple current sources. The final category is the cascaded structure where multiple inverters are connected in parallel; therefore multiple current sources are expected. The control complexity for each category varies; relatively indicated by the converter size and the number of component in used.

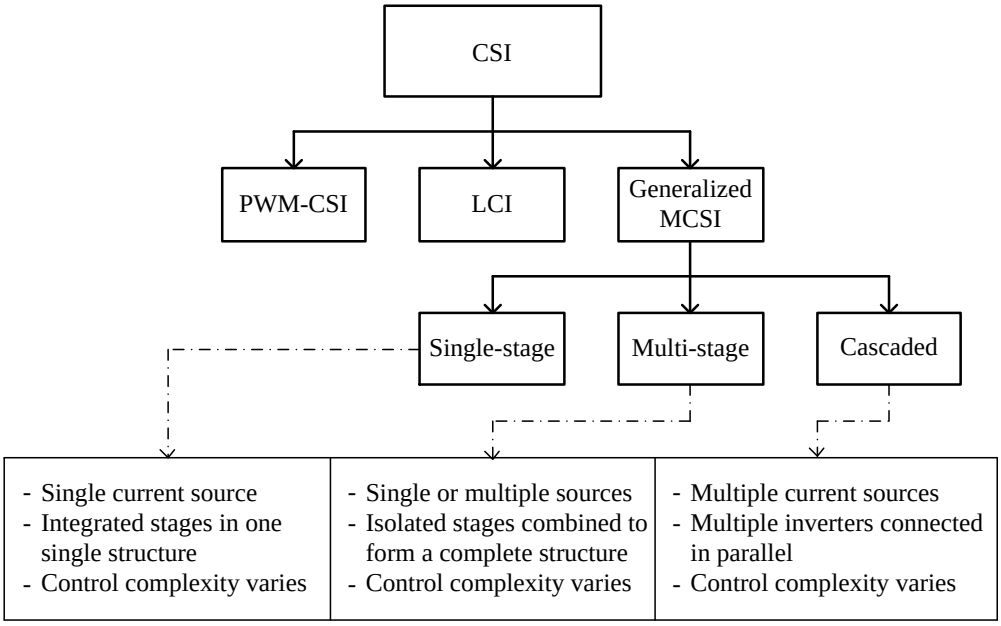


Fig.1 - 6: General Classification of CSI converters

There have been few solutions proposed to reduce the converter size by either introducing new control algorithms [29, 32] or new topologies [10, 30]. For example [29] deploys PWM closed-loop control to sense and balance the intermediate currents through inductors in order to reduce inductor losses allowing smaller inductor designs. This technique however, comes with the expense of an increased complexity. Modification work proposed in [33] on the other hand reduces the total component count but is lagging to control inductor currents at high loads. New topologies as proposed in [34, 35] however fall under the multi-stage category; where multiple current sources are required.

The duality between the flying capacitor MVSI and MCSI was shown in [26]. In theory the flying capacitor MVSI can have an infinity number of capacitors to generate an infinity number of voltage levels. Therefore the flying capacitor topology is termed as a generalized topology. A generalized topology is also referring to a group of inverter whose structure is general to its own class. The same concept applies to the MCSI topologies proposed in [10] which in the following Chapter 2 is called Topology I and is shown in Fig.2-15 where each individual current in each inductor is added to achieve the desired load current as oppose to the flying capacitor where each voltage across each capacitor is added to achieve the desired output voltage. This topology together with few others as in [29, 30, 34] are categorized as generalized MCSI topologies since their principal circuit structures are general to their own cluster which in theory, can be expanded to an infinite level of current. Unfortunately, so far hardware demonstration was always reported on the smallest level which is five [29, 30, 36-38]. There are few publications describing non-experimental work on seven or higher level inverters [33, 39]; nevertheless no detail explanation was given regarding control issues, efficiencies at load variations and current harmonics which are the main drivers in high voltage / high current applications. For example the MCSI controller must guarantee continuous current flow in the inductors to avoid voltage spikes across the switching power devices. The controller must also minimize the inductor current ripple to reduce inductor losses and finally the switches must be controlled in such a way that the average voltage across each inductor is zero in order to avoid saturation of the inductor.

In order to make MCSI more attractive for power conversion the number of components must come down dramatically in particular at high current levels. A reduction in the number of inductors will increase the efficiency and a reduction in the number of switching devices will reduce control complexity. In this research, a novel MCSI is proposed that has a minimum number of inductors and power switches for any output-current level. This causes significant reduction in volume and size of the new inverter, thus allowing the new circuit to be more competitive compared to

existing MCSIs. Furthermore, reduced switching devices simplify the control algorithm, therefore prompting that the novel inverter can become more reliable.

1.2 Objectives and possible contributions to knowledge

This research is primarily aimed to explore the basic construction of the generalized MCSI topologies and the focus is to overcome the shortcomings in the existing topologies by proposing a novel inverter topology with improved performance. Investigations on the operation characteristics of novel topologies of multilevel current-source inverter systems in typical high-current applications are carried out. The operation of these novel multilevel topologies will be analysed, modelled and experimentally verified to assess their impact on drive performance and supply distortion levels. In carrying out the experiments, lists of possible contributions to knowledge are highlighted:

- Comprehensive study of multilevel current source inverter topologies;
- Evaluate and compare the existing generalized MCSI topologies in terms of structure and performances;
- Design an improved control strategy for an MCSI under high-load as well as low-load conditions;
- Design a novel MCSI topology that overcomes current shortcomings in existing topologies;
- Evaluate the performance of the novel MCSI by computer simulation and practical experiment;
- Compare the simulation and experimental results obtained from the novel inverter for design verification.

1.3 Thesis structure

Based on the flow of the possible contributions, this thesis is divided into six chapters. **Chapter 1** provides general discussions of multilevel inverters and the generalized CSI topologies as well as the motivation and objectives behind this research.

Chapter 2 presents the general multilevel converters topologies and operations. Both classical voltage source inverter and current source inverter topologies are briefly discussed. The voltage source inverter to current source inverter duality theory is extended to the principle designs of multilevel current source inverter. Finally, carefully selected existing multilevel current source inverter topologies are discussed in reasonable details.

Chapter 3 discusses the methods of controlling the multilevel current source inverters. It was shown that the existing methods are primarily aimed at low-load operations; therefore an improved control method that is efficient for both high- and low-load operations has been developed. The proposed method is validated via simulation as well as experimentally.

Chapter 4 explains the proposed novel multilevel current source inverter topology. The structure and operational characteristics of the proposed inverter is discussed in detail. Computer simulations are performed to validate the theoretical assessment.

Chapter 5 discusses the experimental arrangement of the research, circuit and controller as well as the associated experimental parameters and experimental results. In this chapter also, the developed MCSI topology is validated experimentally.

Chapter 6 presents the conclusions and also the current and future work plans.

1.4 Publication work

[1] **B. Hassan**, V. Pickert and B. Zahawi, "Performance Comparison of single-phase current-fed inverters," in Power Electronics, Machines and Drives (PEMD 2010), Proceedings of the 2010-5th IET on, 2010.

[2] **B. Hassan**, V. Pickert and B. Zahawi, "Control of five-level single-phase current-source inverters operating at high- and low-load conditions," in Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, 2011, pp. 1-9.

CHAPTER 2

Multilevel Converter: Topologies and Operations

Multilevel converters were designed in particular to overcome the voltage and current limitations of semiconductor devices for medium- and high-power applications where switching devices are connected in series or parallel to achieve increased power ratings [26, 28, 40]. Recently, multilevel converters have also become popular in low-power applications because of their reduced EMI effects compared to two-level inverters [9]. Although multilevel converters can be constructed either as voltage-source inverter (VSI) or current-source inverter (CSI), nowadays there are more VSIs in operation than CSIs mainly because of cost. This chapter starts by reviewing the classical converter hierarchy in a typical high-power drives application leading to the main research interest, the multilevel current source inverter (MCSI). The three (3) main groups of MCSI, as discussed in chapter 1, are elaborated where four existing single-source MCSI topologies are presented in detail, compared and summarized. Some details of the Simulink models used in the simulations are presented in Appendix A.

2.1 Introduction

The invention of the multilevel converters in 1980 by Nabae et al [41] has encouraged research activities into transformer-less based investigations for high-power high-voltage electric drives because the multilevel converter topologies have the advantage of increased power rating, where they have been proven to be reliable and robust in some high power applications. They are also able to generate near sinusoidal voltages with only fundamental frequency switching or have almost no electromagnetic interference and common-mode voltage [41]. These advantages, however, are offered at the expense of extra complexities either structurally or by the switching strategies.

In numerous literatures, the term multilevel starts at the level of three, though definitions may vary either by applications or by author [6]. In this thesis, the definition of the number of levels is self-explained by the illustrations in Fig.2-1, where if *l* is simply the number of level on positive y-axis, then the number of levels, *n* for a typical staircase waveform can be mathematically determined by:

$$\text{Converter output level, } n = 2l + 1 \tag{2-1}$$

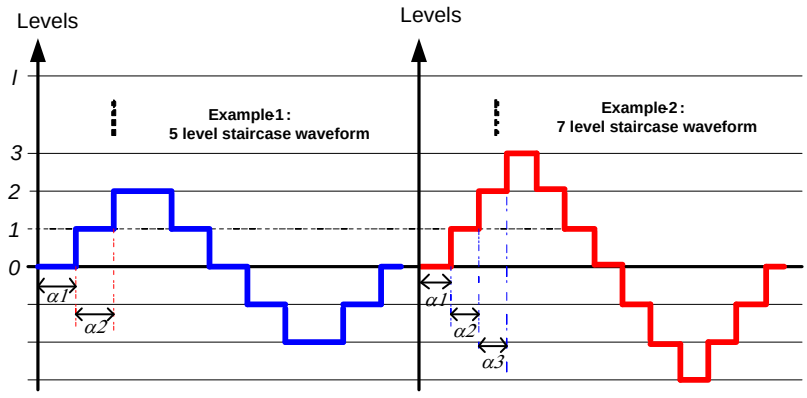


Fig.2 - 1: Converter output level determination

Generally, a higher number of level gives a better output total harmonic distortion (THD). Thus, in theory the output THD should be zero when the number of levels reaches infinity. Practically, however, the possible number of levels is bounded by various factors such as the voltage/current imbalance problems, voltage/current clamping requirements, circuit layout and packaging constraints, complexity of the controller, and also the maintenance costs [27]. These factors occurred depending on the applied topology. In multilevel topologies, the magnitude of harmonic distortion can be attuned by controlling the conducting angles; α1, α2 and α3 (Fig.2-1) to create asymmetrical staircase waveform where specific low order harmonics can be eliminated. This method of control has been commonly practised in selective harmonic eliminated (SHE) modulation technique [6].

2.2 Harmonic Minimization in MCSI

In Fig. 2-1, the parameters α_1, α_2 and α_3 are the firing angles which must be greater than zero and smaller than $\pi/2$. These angles can be chosen arbitrarily as long as they produce multilevel waveform as desired, or can be carefully selected for harmonic control in order to reduce THD. Nevertheless, by choosing the firing angles strategically, multiple harmonic orders can be completely eliminated and thus eliminating the need for filtering equipment required for that particular orders.

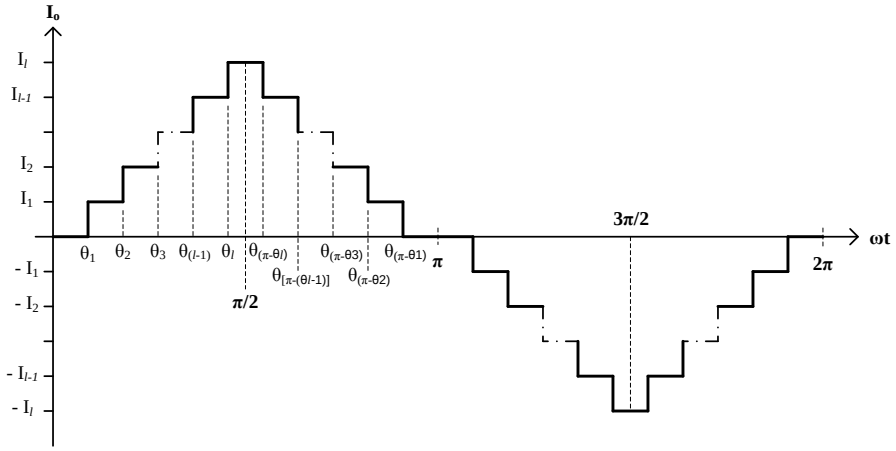


Fig.2 - 2: Output current waveform of a general single-source MCSI

Theoretically, the waveform of the load current of an MCSI, as shown in Fig. 2-2 is periodic and has the same symmetry as a sine wave. The figure illustrates a generalized output-current waveform of a single-source MCSI that consists of switching angles, θ_1, θ_2, $\theta_{3,..,}$ $\theta_{(l\text{-}1)}$ and θ_l in each quarter cycle. The maximum current level equals to I_l whereas the current of the intermediate levels are the fractions of this maximum current. The number of current fractions determines the complexity of the circuit whereby it identifies the number of current branches involved. This also reflects to the number of power switches and inductors that are required in order to divide the maximum current into current fragments. Like any other periodic function, this waveform can be expressed as a Fourier series which is a summation of sinusoids with frequencies that are integer multiples of the function's fundamental frequency. In general, the Fourier series of a periodic function $f(\omega t)$ with fundamental frequency *f* can be expressed as [42];

$$f(\omega t) = a_0 + \sum_{m=1}^{\infty}[a_n \cos(m\omega t) + b_n \sin(m\omega t)] \tag{2-2}$$

where *m* is the harmonic order; a_0 is the average value of the function; a_n and b_n are the coefficients of the series. The coefficients can be computed as follows;

$$a_o = \frac{1}{T}\int_0^T f(\omega t)\, d(\omega t) \tag{2-3a}$$

$$a_n = \frac{2}{T}\int_0^T f(\omega t) \cos(m\omega t)\, d(\omega t) \tag{2-3b}$$

$$b_n = \frac{2}{T}\int_0^T f(\omega t) \sin(m\omega t)\, d(\omega t) \tag{2-3c}$$

By referring to Fig 2-2, it can be noticed that the current waveform is both odd and half-wave symmetries. This would simplify its Fourier series equation to;

$$a_o = 0 \tag{2-4a}$$

$$a_n = 0 \tag{2-4b}$$

$$b_n = \frac{2}{\pi}\int_0^{\pi} I_o(\omega t) \sin(m\omega t)\, d(\omega t) \tag{2-4c}$$

It is also assumed that the periodic waveform has quarter-wave symmetry, therefore;

$$b_n = \frac{2}{\pi/2}\int_0^{\pi/2} I_o(\omega t)\sin(n\omega t)\,d(\omega t) \tag{2-5a}$$

$$b_n = \begin{cases} \frac{4}{\pi}\int_0^{\pi/2} I_o(\omega t)\sin(m\omega t)\,d(\omega t)\,; & m = odd \\ 0\,; & m = even \end{cases} \tag{2-5b}$$

and the resulting Fourier series of the figure in Fig 2-2 is;

$$I_o(\omega t) = \sum_{m=1}^{\infty} b_n sin\,(m\omega t) \tag{2-6a}$$

Let ωt=θ, hence

$$I_o(\theta) = \sum_{m=1}^{\infty} b_n sin\,(m\theta) \tag{2-6b}$$

From Eqn. (2-5b) and (2-6a), therefore, the Fourier series of the current waveform in Fig 2-2 can be expressed as;

$$I_o(\omega t) = \sum_{m=odd}^{\infty} \frac{4I_0}{m\pi}\left(\sum_{k=1}^{l}\cos(m\theta_k)\right) sin(m\omega t) \tag{2-7}$$

Where θ_k is the switching angles which satisfy the condition $\theta_1, \theta_2, ..., \theta_l < \frac{\pi}{2}$;

I_0 is the amplitude of dc current

l is the current-level on the positive x-axis

The amplitude of all odd harmonic components including the fundamental are given by;

$$h(m) = \frac{4I_0}{m\pi}\sum_{k=1}^{l}\cos(m\theta_k) \tag{2-8}$$

Which switching angles of the waveform can be adjusted to get the lowest THD in the output current as;

$$h(m) = \frac{4I_0}{m\pi}\left[cos\theta_1 + cos\theta_2 + cos\theta_3 + .. + cos\theta_{(l-1)} + cos\theta_l\right] \quad (2\text{-}9)$$

The fundamental component amplitude depends on the modulation index, M which is the ratio of the modulating signal amplitude to the carrier signal amplitude;

$$M = \frac{I_1}{I_{max}} \quad (2\text{-}10)$$

Where I_1 is the fundamental component of the output current

I_{max} is the maximum output current

Therefore, for the fundamental output current, the general harmonic equation can be determined by;

$$\frac{4I_0}{\pi}\left[cos\theta_1 + cos\theta_2 + cos\theta_3 + .. + cos\theta_{(l-1)} + cos\theta_l\right] = I_1 \quad (2\text{-}11a)$$

Which can be rewritten as;

$$\left[cos\theta_1 + cos\theta_2 + cos\theta_3 + .. + cos\theta_{(l-1)} + cos\theta_l\right] = M \quad (2\text{-}11b)$$

Whereas desired harmonics for elimination i.e. the 3rd, 5th and 7th harmonics (although not limited to), can be determined by;

$$\left[cos3\theta_1 + cos3\theta_2 + cos3\theta_3 + .. + cos3\theta_{(l-1)} + cos3\theta_l\right] = 0 \quad (2\text{-}12a)$$

$$\left[cos5\theta_1 + cos5\theta_2 + cos5\theta_3 + .. + cos5\theta_{(l-1)} + cos5\theta_l\right] = 0 \quad (2\text{-}12b)$$

$$\left[cos7\theta_1 + cos7\theta_2 + cos7\theta_3 + .. + cos7\theta_{(l-1)} + cos7\theta_l\right] = 0 \quad (2\text{-}12c)$$

While equation (2-11) guarantees the desired fundamental component, equation (2-12) are used to eliminate the selected harmonics i.e. the 3rd, 5th, and 7th although not limited to these specific orders. The number of certain harmonic orders that can be eliminated depends on the number of switching angles, θ_k. As an example, for the 5-level current waveform, two switching angles involved; therefore, one selected harmonics can be eliminated. Similarly, for the 9-level

current waveform, four switching angles involved; therefore, three selected harmonics can be eliminated.

Although these angles can be computed numerically, this is by no means uncomplicated due to nonlinear and transcendental characteristics of the equations. In fact, this is one of the most difficult tasks associated with the SHE technique. Several solving methods were developed for the optimized harmonic switching angles in multilevel inverters as reported in [26, 42-46] and the Table 2-1 has presented some examples of the solved angles for the 3^{rd}, 5^{th} and 7^{th} harmonics elimination by two different methods, namely the Newton-Raphson method (N-R) and the genetic algorithm based optimization method (GA) for a nine-level step-waveform [26, 42, 45]. It can be noticed that the resulted angles of the different schemes varies even though the standard step-waveform and the same modulation index are employed. Therefore, it is best to justify that these angles are only best to be used as references only since in practical hardly any two waveforms will be perfectly equivalent. Yet, it is beyond the scope of this thesis either to prove the effectiveness of any of these methods or to develop an appropriate new solving method for any particular waveform. Nevertheless, this has been recommended for future research in Chapter 6. On the other hand, it is in the interest of the thesis to demonstrate that the low order harmonics and the THD of the MCSI output current waveform can be improved with switching angle manipulation.

Table 2 - 1: Switching angles for different modulation index and solving methods

Mod. Index		Angle (Degree)	
		N-R Method	GA Method
0.8	θ_1	27.40	22.76
	θ_2	51.60	34.42
	θ_3	73.90	46.17
	θ_4	81.40	58.03
0.85	θ_1	5.25	5.79
	θ_2	28.10	17.38
	θ_3	46.40	37.61
	θ_4	84.09	55.74

2.3 Harmonics

In general, the total harmonic distortion (THD) can be determined by [47];

$$THD_{\%fundamental} = \left(\frac{I_{rms(distortion)}}{I_{fundamental}}\right) \times 100 \tag{2-13}$$

Where $I_{rms(distortion)}$ is the rms value of harmonic current without the fundamental current.
$I_{fundamental}$ is the fundamental current.

The rms current of an ac waveform can be calculated by [48];

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T {i_{ac}}^2 dt} \tag{2-14}$$

Where T is the time period.

The ac current waveform, i_{ac} in steady states is the sum of its Fourier components (assuming zero dc component) as [49];

$$i_{ac}(t) = i_{1ac}(t) + \sum_{h\neq 1} i_{hac}(t) \tag{2-15}$$

Where i_{1ac} is the fundamental component and i_{hac} is the component at the h harmonic frequency. By substituting for i_{ac} from eqn. 2-15 into eqn. 2-14;

$$I_{ac(rms)} = \sqrt{I_{1ac(rms)}^2 + \sum_{h\neq 1} I_{hac(rms)}^2} \quad (2\text{-}16)$$

The rms or the "root-mean-square" summation of current is used to determine the current whenever more than one current frequency exists. It is basically the total effective load current which contains both the fundamental and harmonics. This allows for individual calculations of the rms values of the actual waveform which can be approximated by (assuming zero dc components);

$$I_{rms} = \sqrt{I_{rms}^2(1) + I_{rms}^2(2) + .. + I_{rms}^2(n)} \quad (2\text{-}17)$$

Where $I_{rms}(1)$ is the fundamental current ($I_{fundamental}$)
$I_{rms}(2)$ *to* $I_{rms}(n)$ are the harmonic components ($I_{rms(distortion)}$)

Thus, the values of I_{rms} from eqn. 2-17 can be substituted into eqn. 2-13 to get the percentage of THD of the waveform.

2.4 Classification of converters for high-power applications

In high power applications, typically the inverters used can be classified into voltage source inverter (VSI) and current source inverter (CSI) as illustrates in Fig.2-3 [9]. VSIs are used to define the output voltages while CSIs are used to define the output currents. For multilevel topologies, the VSI has advantages such as the reduction in voltage dv/dt harmonics, electromagnetic interferences and filter size [41]. Popular MVSI topologies are the diode-clamped inverter (or neutral-point clamped), capacitor-clamped (or flying capacitor), and cascaded multi-cell with separate dc sources. These converters are commercially available and commonly found in the medium-to-high power applications of merely few megawatts to hundreds of megawatts i.e. petrochemical industry and cement industry [3]. There are other less-popular topologies such as the mixed-level hybrid inverter, the asymmetric hybrid inverter and the soft-switched inverter [6]. These are mostly available in the lower power range and subjected to on-going

research. On the contrary, even though CSI technology has been widely accepted in the industry, many of CSIs are designed for specific applications; and frequently for large ac drive [50, 51]. Previously, CSI can be divided into two classical topologies; one is called the load-commutated inverters (LCI) which utilize SCR as their switching devices, and second is the PWM-CSIs that often use either symmetrical GTOs or IGCTs devices. However, only recently new family of topology emerges; the generalized multilevel current source inverter (MCSI) which generates the output currents in multilevel forms. Although currently still at research stage, the MCSI has the potential to be used in high power applications due its ability to divide the total input current among the employed switches unlike the traditional CSI that are normally parallel-connected in order to produce multilevel waveforms with the help of inductor-links to smoothen the sharing-current outputs [26, 52].

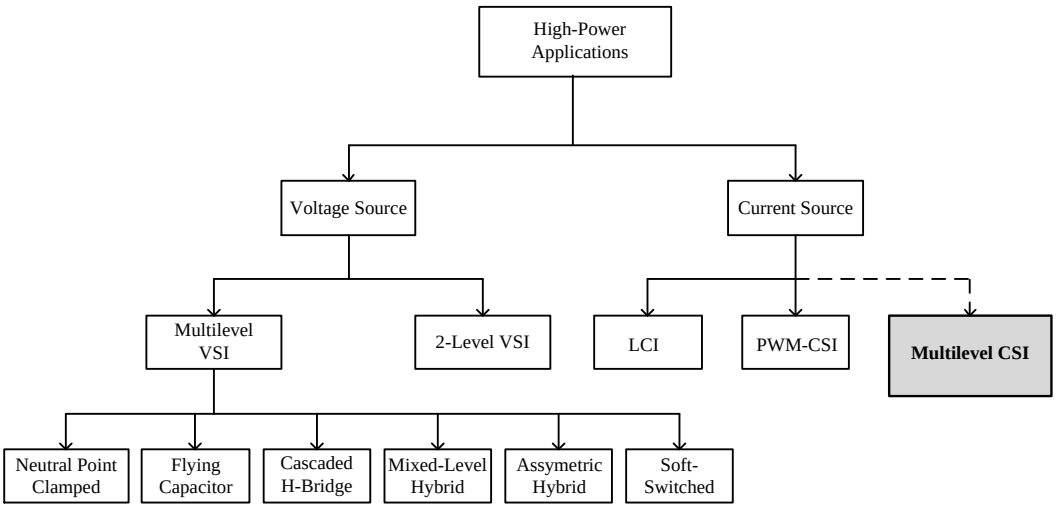


Fig.2 - 3: Classification of converters for high-power applications

2.5 Multilevel Voltage Source Inverter

The new emerging family of MCSI partly has been the result of the general viewpoint that CSI is the dual of a VSI imparts the essential step in the

construction of MCSI topologies via the duality principle [51]. By theory; two dual circuits share similar properties, thus the knowledge obtained from one topology can be applied to its dual circuit directly. Therefore, sufficient understanding of the renowned MVSI families such as the diode-clamped, flying capacitors and the cascaded H-bridge inverters are crucial.

To simplify the idea, the MVSI simply can be viewed as voltage synthesizer where the main output voltage waveform is synthesized from different levels of smaller output voltages. Fig.2-4 shows a schematic diagram of a single-phase inverter with multiple numbers of capacitors to illustrate the basis of multilevel inverter operation. The different voltage levels are represented by the capacitors whereas the ideal switch with multiple poles represents the action of power semiconductor switches. It can be seen that a number of output voltage levels can be synthesized by controlling to where the switch pole is connected to a portion of the capacitors. Similarly, for a negative output voltage, the reference node, 0 is moved to the opposite end of the capacitor string. These are the basic principles surrounding the setup of MVSI as will be discussed next.

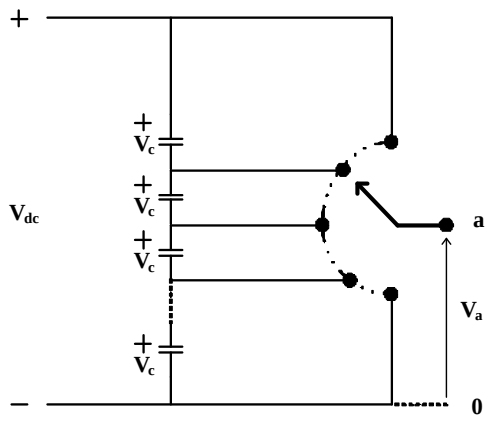


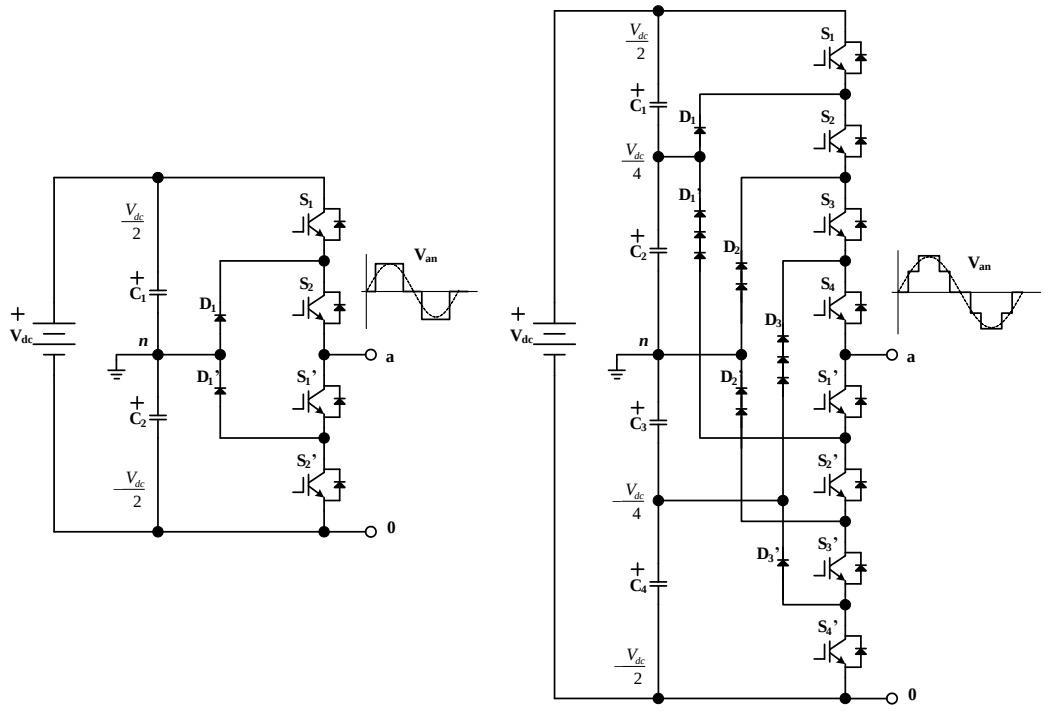
Fig.2 - 4: Multilevel inverter fundamental

2.5.1 Diode-Clamped Inverter

The diode-clamped inverter employs capacitors in series to split up the DC bus voltage into a set of voltage levels. Fig.2-5 shows the diode-clamped inverter

configurations for three-level and five-level voltage outputs. In order to produce an *n*-level phase voltage, a diode clamped converter needs (*n*-1) capacitors on the DC bus. From Fig. 2-5(a) it can be seen that for the three-level output, two capacitors are required whereby each capacitor carries ±*Vdc*/2 across them. As for the five-level output, four capacitors are required where the voltage across each capacitor is ±*Vdc*/4 . Knowing the voltage and polarity of each capacitor, the staircase output voltage can be easily synthesized by manipulating the switching combinations.

For a three-level diode-clamped inverter as shown in Fig.2-5(a), the dc-bus voltage is divided into two half values, $V_{dc}/2$ by two series-connected capacitors C_1 and C_2. The middle point, *n* between the two capacitors is defined as the neutral point. Therefore, the output voltage v_{an} has three levels; (1) $v_{an} = +V_{dc}/2$ when switches S_1 and S_2 are turned on, (2) $v_{an} = -V_{dc}/2$ when switches S_1' and S_2' are turned on, (3) $v_{an} = 0$ when switches S_2 and S_2' are turned on.



(a) (b)

Fig.2 - 5: Diode-clamped inverter (a) three-level (b) five-level

For a five-level diode-clamped inverter as shown in Fig.2-5(b), the dc-bus voltage is divided into four quarter values, $V_{dc}/4$ by four series-connected capacitors C_1, C_2, C_3, and C_4. The point, *n* between capacitor C_2 and C_3 is defined as the neutral point. Therefore, the output voltage v_{an} has five levels; (1) $v_{an} = +V_{dc}/2$ when all upper switches S_1-S_4 are turned on, (2) $v_{an} = +V_{dc}/4$ when three upper switches S_2-S_4 and one lower switch S_1' are turned on, (3) $v_{an} = 0$ when two upper switches (S_2 and S_4) and two lower switches (S_1' and S_2') are turned on, (4) $v_{an} = -V_{dc}/4$ when one upper switch S_4 and three lower switches S_1'-S_3' are turned on. (5) $v_{an} = -V_{dc}/2$ when all lower switches S_1'-S_4' are turned on.

2.5.2 Capacitor-Clamped Inverter

Fig.2-6 illustrates the capacitor-clamped inverter or the flying-capacitor inverter configurations for the three-level and five-level voltage outputs. It can be seen that, although the number of capacitors used to generate an *n*-level staircase output voltage is equal to (*n*-1) or equivalent to the requirement of the previous topology; however, this topology also requires a number of supplementary capacitors to be clamped in between switches. To better appreciate these differences, the five-level inverter circuits for both topologies are re-drawn in Fig.2-7. By looking at the capacitor-clamped inverter circuit in Fig.2-7, the figure has clearly shown that the supplementary capacitors are formed in a ladder structure such that every capacitor branch carries different value of voltages which allows mathematical exploitation of the output voltage. Knowing the different voltage value between branches and using the point *n* as the common reference, the staircase output voltage waveform can be obtained by manipulating the switching combinations.

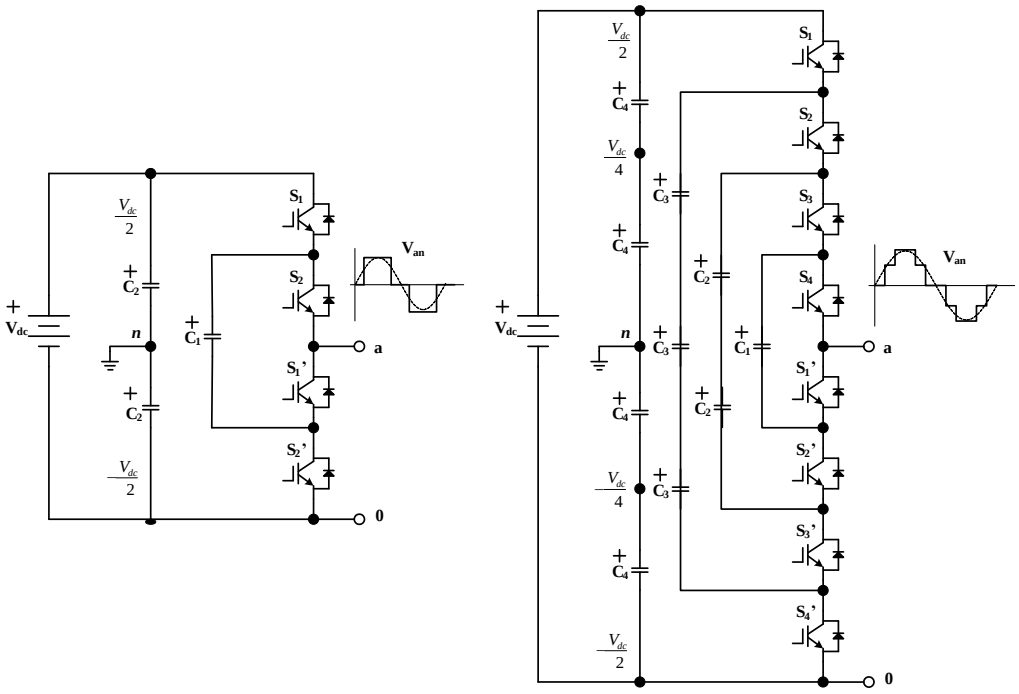


Fig.2 - 6: Capacitor-clamped inverter (a) three-level (b) five-level

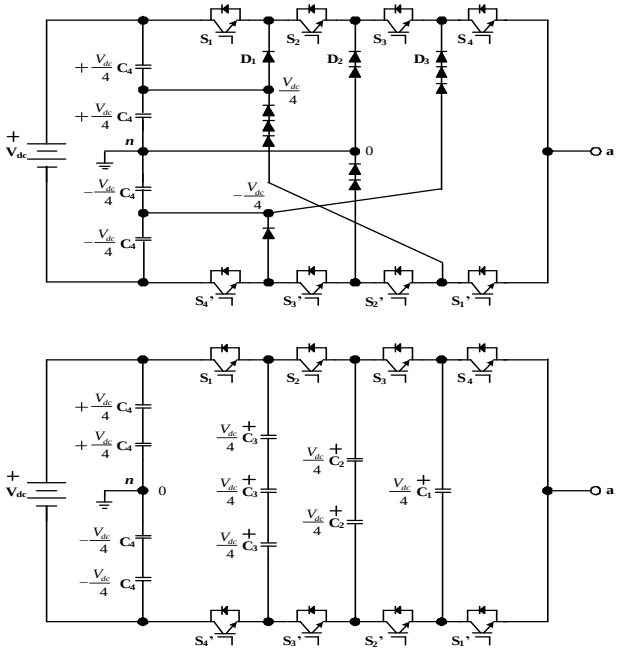


Fig.2 - 7: Re-drawn figures of the (top) five-level diode-clamped inverter and (bottom) capacitor-clamped inverter

As the example, for a three-level capacitor-clamped inverter as shown in Fig.2-6(a), similar to the diode-clamped topology, the dc-bus voltage is divided into two half values, $V_{dc}/2$ by two series-connected equivalent capacitors C_2. The middle point, *n* between the C_2 is defined as the neutral point. Therefore, the output voltage v_{an} has three levels; (1) $v_{an} = +V_{dc}/2$ when switches S_1 and S_2 are turned on, (2) $v_{an} = -V_{dc}/2$ when switches S_1' and S_2' are turned on, (3) $v_{an} = 0$ when either switches (S_1 and S_1') or (S_2 and S_2') are turned on. The clamping capacitor C_1 is charged when (S_1 and S_1') are turned on, and is discharged when (S_2 and S_2') are turned on.

The five-level capacitor-clamped inverter shown in Fig.2-6(b) has more flexibility than a diode-clamped inverter. The dc-bus voltage is divided into four quarter values, $V_{dc}/4$ by four series-connected equivalent capacitors C_4. The middle point, *n* between capacitor C_4 is defined as the neutral point. Therefore, by manipulating switch combinations similar to the diode-clamped topology, the output voltage v_{an} also has five levels but with more possible combinations;

(1) $v_{an} = +V_{dc}/2$ when all upper switches S_1-S_4 are turned on,

(2) $v_{an} = -V_{dc}/2$ when all lower switches S_1'-S_4' are turned on.

(3) $v_{an} = +V_{dc}/4$ has three possible combinations:

(a) S_1,S_2,S_3,S_4' are on, where ($v_{an} = +V_{dc}/2 - V_{dc}/4 = +V_{dc}/4$)

(a) S_2,S_3,S_4,S_4' are on, where ($v_{an} = +3V_{dc}/4 - V_{dc}/2 = +V_{dc}/4$)

(a) S_1,S_3,S_4,S_3' are on, where ($v_{an} = +V_{dc}/2 - 3V_{dc}/4 + V_{dc}/2 = +V_{dc}/4$)

(4) $v_{an} = -V_{dc}/4$ has three possible combinations:

(a) S_1,S_1',S_2',S_3' are on, where ($v_{an} = +V_{dc}/2 - 3V_{dc}/4 = -V_{dc}/4$)

(a) S_4,S_2',S_3',S_4' are on, where ($v_{an} = +V_{dc}/4 - V_{dc}/2 = -V_{dc}/4$)

(a) S_3,S_1',S_3',S_4' are on, where ($v_{an} = +V_{dc}/2 - V_{dc}/4 - V_{dc}/2 = -V_{dc}/4$)

(5) $v_{an} = 0$ has six possible combinations:

(a) S_1,S_2, S_1',S_2' (b) S_3,S_4, S_3',S_4' (c) S_1,S_3, S_1',S_3'

(d) S_1,S_4, S_2',S_3' (e) S_2,S_4, S_2',S_4' (f) S_2,S_3, S_1',S_4'

2.5.3 Cascaded Multi-Cell Inverter

The cascaded multi-cell inverter practically consists of many identical single-phase H-bridge converters connected in a string where each of the bridge is separately supplied with a DC voltage sources. Fig.2-8 illustrates the nine-level cascading multi-cell inverter with its corresponding waveform. For each H-bridge converter, three different voltage outputs, *+Vdc*, *-Vdc* and zero can be generated through different combinations of the four switches. By connecting the bridges in series, the AC voltage output generated is such that the synthesized voltage waveform is the sum of the individual converter outputs (Fig.2-8). The staircase output voltage waveform again can be generated by manipulating the appropriate switch combinations. For this topology, the output voltage levels can be determined by (*n = 2N+1)*, where *N* is the number of DC voltage sources.

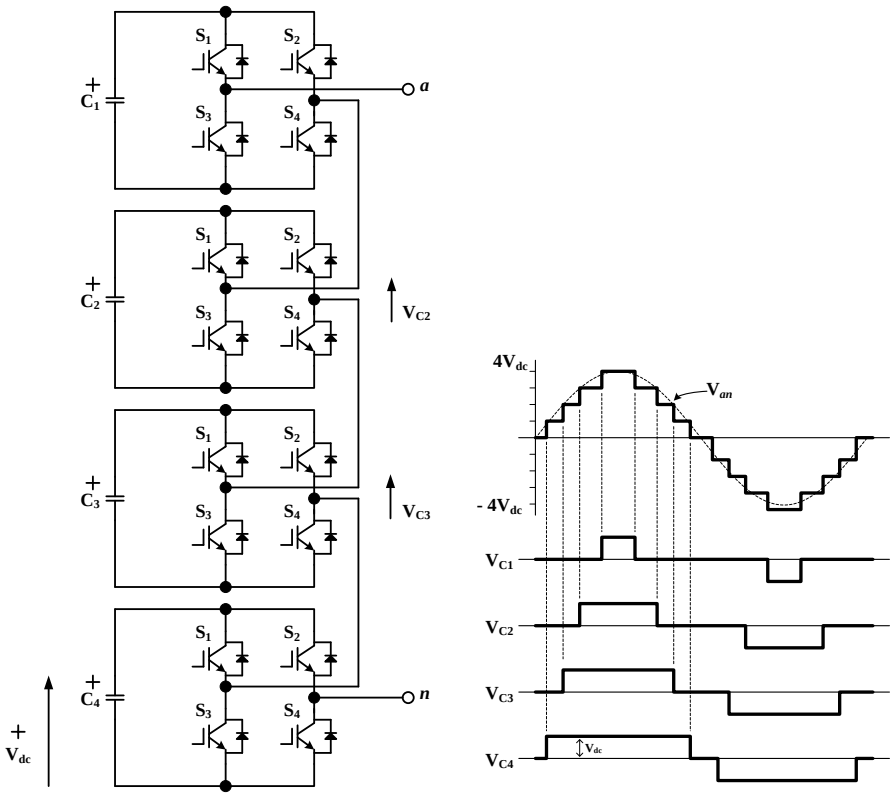


Fig.2 - 8: Cascaded inverter with corresponding output waveform

2.6 Classical Current Source Inverter

It has been reported that amongst the advantages of CSI topologies include: (1) short-circuit protection, where the output current is limited by the dc-bus current; (2) low output voltage *dv/dt*, which resulted from the output capacitor filtering effect; (3) high converter reliability, due to the unidirectional nature of the switches and the inherent short-circuit protection; and (4) instantaneous and continuous regenerative capabilities [53-56]. These features, in addition to the availability of large reverse blocking devices such as GTOs or IGCTs make the CSI-based drive attractive in medium to high power applications. Despite the above advantages, research development in CSI is far behind that of VSI. This can be justified simply by comparing the number of available literatures from both topologies. Over the last decade approximately six thousand (6000) papers and journals have been published on VSIs in IEEE Library whereas only three thousand and five hundred (3500) papers and journals have been published on CSIs.

2.6.1 Load-commutated inverter (LCI)

The SCR-based LCI is one of the earliest inverters developed for variable-speed drives. A three-phase LCI has three parallel poles; representing by two series-connected SCRs per-pole which in total requires six SCRs. As shown in Fig.2-9, the SCR or thyristor switches are numbered according to their firing sequence whereas the commutating elements, capacitors between the phase legs and series diodes are intentionally excluded for simplification. A nearly constant current, Idc is sourced by connecting a large inductor between the input dc voltage source, Vdc and the inverter components; thus creating a current-source inverter circuit. When a thyristor is fired, it immediately commutes the conducting thyristor of the same group (upper and lower groups) i.e. when S1 and S2 are conducting, the input current Idc will flow through (S1- phase A load– phase C load- S2) and back to the input source. The idealized waveforms of the input and output currents are shown in Fig.2-10 [57]. It can be seen that each thyristor conducts for

a 120 degree interval. Since a thyristor is a load commutated device, these inverters have to be made to operate at leading power factor.

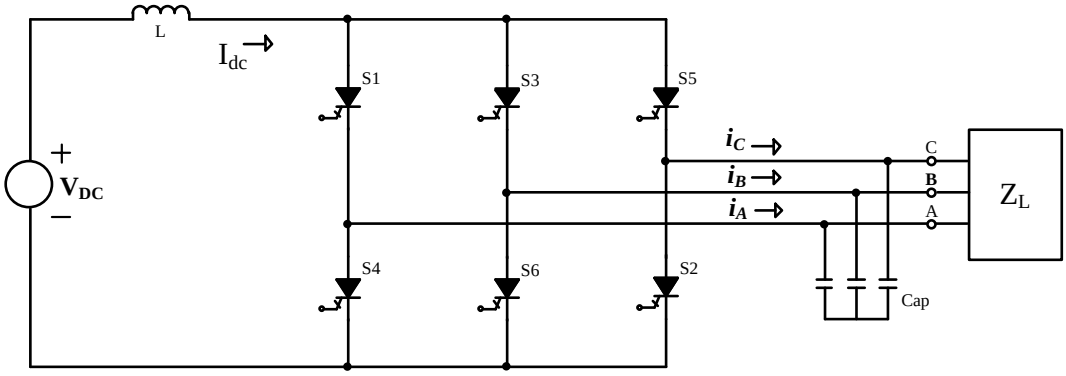


Fig.2 - 9: Schematic of a classical SCR-based CSI

While popular, SCR-based CSI is most commonly used for the low cost solution since higher power rated thyristors are easily available [58]. A major disadvantage of this topology is the limited control strategies applicable since a thyristor cannot be switched off from the gate drive circuit. Therefore, the most common control technique applied is the six-step switched control [59] although this controller is known for generating large amount of harmonics in the load voltage and load current. These harmonics can be reduced by connecting the output filter capacitors as illustrated in the Fig.2-9. Another approach to minimise the current and voltage harmonics in CSI is the application of PWM control which can be achieved easily by replacing the thyristor switches with gate turn-off devices such as the GTO or IGCT switches. This would allow turn-off capability and result in the extension of operation to loads with wider power factor and even pulse width modulation (PWM) capability [60].

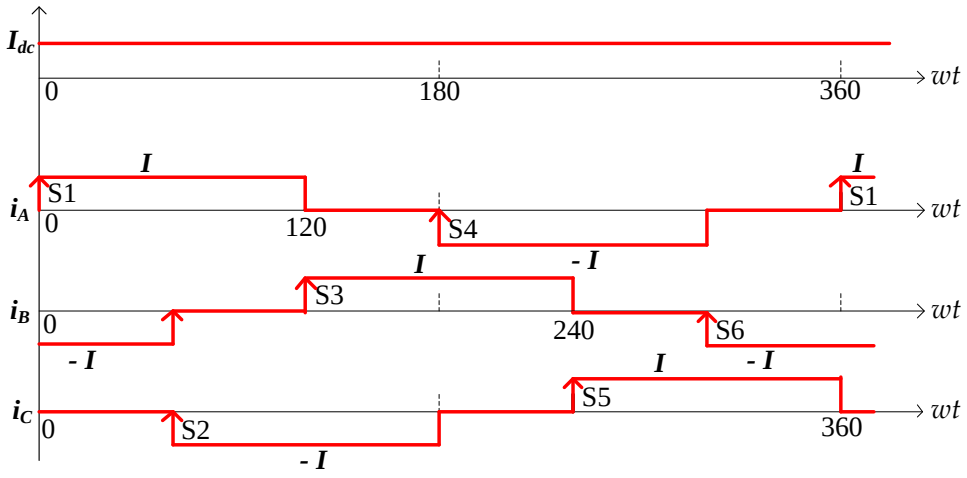


Fig.2 - 10: Three-phase SCR-based CSI typical current waveforms

2.6.2 PWM-CSI inverter

The CSI using IGBT switches is shown in Fig.2-11. In the figure, the series diodes are excluded for simplicity. The waveforms of currents i_A, i_B and i_C are the same as those shown in Fig.2-10 except that the switches S1-S6 can be turned on and off by the gate voltages or gate currents of the devices. Various modulation techniques therefore can be applied in order to improve the output current harmonics including trapezoidal pulse width modulation (TPWM), selective harmonics elimination (SHE), and space vector modulation (SVM) [61, 62]. Whilst, the capacitor bank purposes are to assist the commutation process during switchover of current between devices by providing temporary load current, to filter out current harmonics then generate a sinusoidal load current, and to reduce voltage spikes.

Essentially in CSI, all switching devices must be able to withstand equally both forward and reverse blocking voltage, thus symmetrical switching devices are often preferred. In cases where unsymmetrical devices are used, series diodes are necessary to protect the switches from reverse voltage. This practice has however, not just increased the cost, but also the complexity and conduction losses [59]. Another disadvantage of PWM control is that it degrades the converter efficiency due to high switching losses.

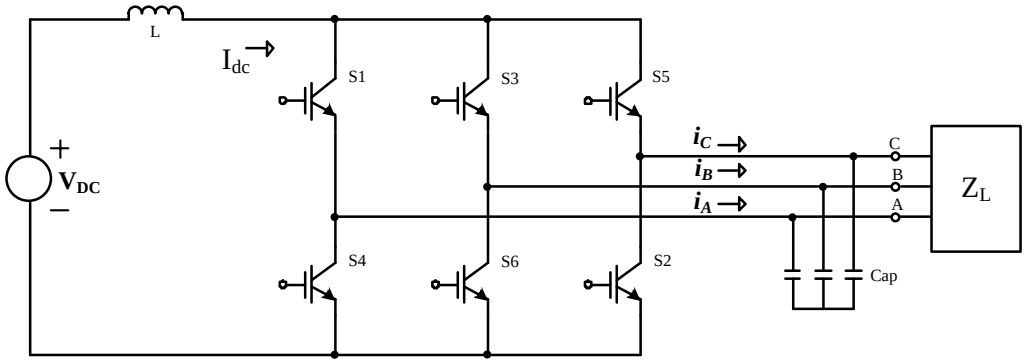


Fig.2 - 11: Schematic of a CSI using IGBT switches

Despite the drawbacks, PWM-CSI inverters are continuously explored by many researchers for new or improved control algorithms [63-65] and topologies [66-68]. Apparently its ruggedness and reliability in general outweigh its disadvantages. Recent development in multilevel current source inverters (MCSI) which present several advantages regarding total harmonic distortion and stress on inductors and switches are progressively published. Several MCSI topologies have been developed and presented in the literature [29, 32, 34, 36, 39, 69, 70]. The next chapter will explain the different types of MCSI topologies in existent.

2.7 Introduction to MCSI

The CSI has certain performance advantages especially in the medium-voltage drive applications such as simple converter structures, low switch count, low switching $\delta v/\delta t$, and reliable over-current/short-circuit protection; however, its major disadvantages are the poor dynamic performance due to the use of dc chokes which limits the rate of dc current changes [61] and higher power losses in comparison to its dual, the voltage source inverters (VSI). In the past, the VSI designs have been proven to be more efficient, have higher reliability with faster dynamic response in the industrial markets [71]; therefore more investigations are carried out in this area. Amongst significant accomplishment is the introduction of multi-level voltage source inverters (MVSI) which have been installed in a range

of medium-to-high power applications such as in the retrofitted medium power drives [3] and high voltage dc transmission (HVDC) systems [72].

Just recently, since the availability of modern gate turn-off switching devices at increasing power levels, significant interest in the MCSI topologies have emerged. A number of new MCSI topologies have been developed. However, unlike the classical CSI topologies as previously discussed, these new topologies have different structure as well as characteristics to both classical CSIs that they fall into a new sub-category to the existing CSI family as illustrated in Fig.2-12. Comprehensive description of the figure has been previously discussed in chapter 1 (Fig.1-6). Many of these new topologies are developed as the equivalent to the MVSI topologies based on duality principles[11, 73-75].

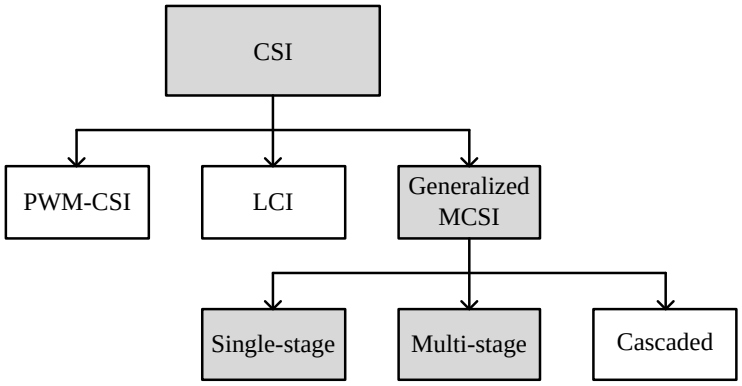


Fig.2 - 12: Generalized MCSI under CSI classification

2.7.1 MCSI Topology: Principles of Design

Generally, the classical CSI-based multilevel topologies are designed based on parallel-connection of multiple CSI circuits or cascaded MCSI. These can be either LCI-parallel with-LCI [76], PWM_CSI-parallel with-PWM_CSI [77], or LCI-parallel with-PWM_CSI (or hybrid topology) [78, 79]. The new emerging generalized MCSI topologies can be either of single-stage structure [10, 29], multi-stage structure [30, 34, 80] or cascaded structure [39].

2.7.2 Duality Transformation

The general viewpoint that CSI is the dual of a VSI imparts the essential step in the construction of MCSI topologies via the duality principle. The principle has been widely used in the development and understanding of power electronic converter topologies in both planar and non-planar [59] circuits. By theory; two dual circuits share similar properties, thus the knowledge obtained from one topology can be applied to its dual circuit directly. Eventually, sufficient understanding has been gained from well-known MVSI families such as the diode-clamped, flying capacitors and the cascaded H-bridge inverters where for these topologies, their MCSI duals have been progressively developed.

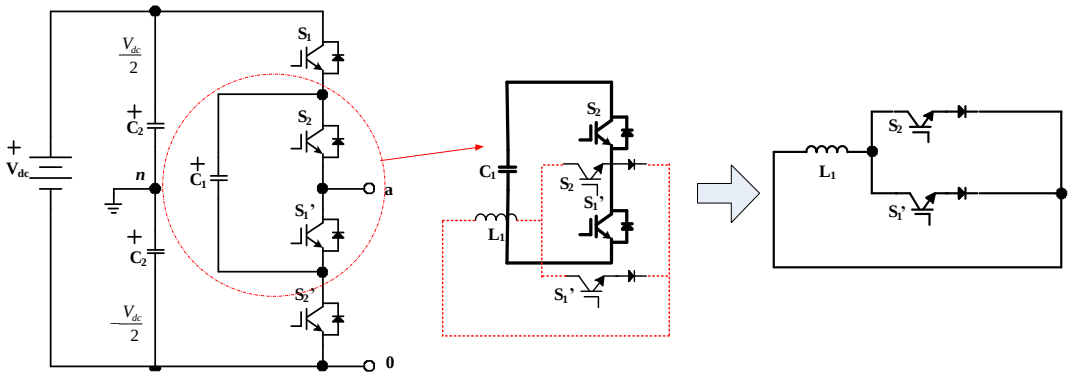


Fig.2 - 13: Duality principle transformation

Dual circuits can be developed by constructing the duals for like-to-like elements. For example in Fig.2-13, the capacitor in capacitor-clamped VSI is replaced with an inductor for CSI. The orientation of passive elements is not important for the duals; however the switches and diodes must be oriented precisely. Fig.2-13 also illustrates this conversion where parallel diodes are replaced by series and inverted diodes whilst power switches in series are replaced by switches in parallel with inverted switching functions. Recently, the subject matter of duality principle and related issues of constructing MCSI topologies from their MVSI equivalent has been extensively discussed [26, 37, 38, 52, 74, 81]; nevertheless, a common agreement has been realized that all direct duals are dysfunctional

circuits where intuitive modifications are necessary before the dual converters become viable. There are numbers of new MCSI families, of both single-phase [82] and three-phase [36-38] topologies that have been originally derived by this theory and successfully experimented. Certainly these circuits are indebted to the duality principle for the insight.

2.7.3 Current-Multilevel (CML) Cells

Prior to CML cell discovery, the concept of multilevel has been exclusively used in MVSIs where the total input voltage among a number of employed PWM cells are divided to provide a number of smaller voltage sources. However, the introduction of the generic CML cell (Fig.2-14) which allows current sharing via small balance inductors has instigated the feasibility of MCSI implementation [27]. The concept of CML has been originated from the proposed parallel association of PWM cells as an alternative to the series association of cells in generic multilevel voltage cell in order to increase the power capability of the anticipated converters [50, 69, 83]. The configuration, as shown in Fig.2-14a consists of multi cells arrangement of two complementary PWM switches per-cell (S1/S1' and S2/S2'), a voltage source between point T1 and T2 and also a current source at point C connected by means of balance inductors. The inductor is assumed to be in continuous conduction mode with negligible ripple and has a specific and fixed current level i.e. (I/*n*) current, where *n* equals the total number of complementary switches (Fig.2-14b). It is shown that it is possible for PWM cells to share the total current of a converter using inductors as pathways as long as the current is continuously conducting with negligible ripple about a fixed current value.

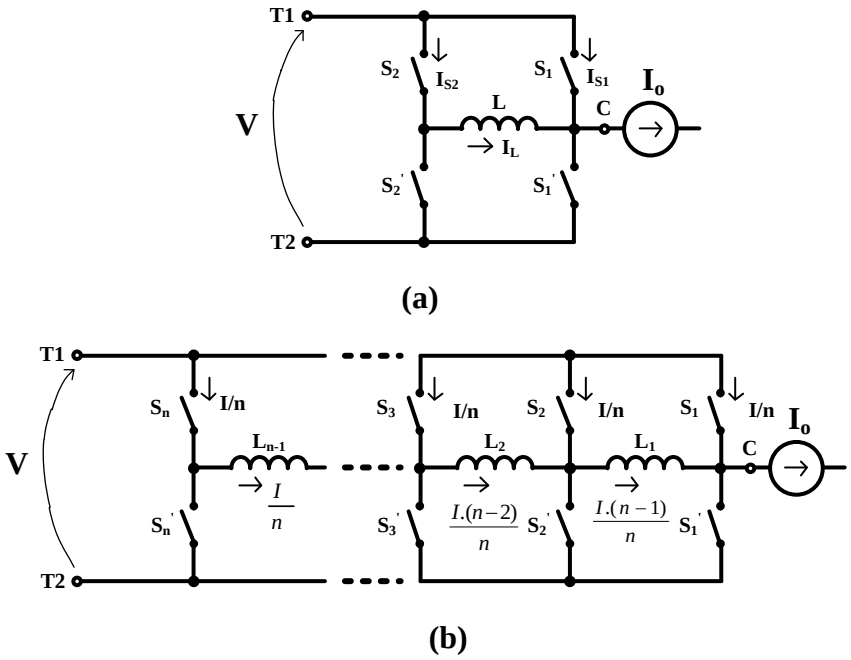


Fig.2 - 14: The original generic cell; (a) single-cell (b) multiple-cells

By adapting the PWM switches to a current source input, acting as a voltage bi-directional/current unidirectional switch, this configuration can be re-shaped as a current inverter cell as shown in Fig.2-15. The re-oriented cell seems incomplete as it prohibits a complete current flow throughout the circuit. This however can be simply solved by applying mirror circuit at node A and P; by taking special care to the directions of current flow, which yields the final MCSI circuit as in Fig.2-16. In the figure, the mirror images of components are denoted by '*' signs at the beginning of their labels. This particular circuit configuration has been actively adopted in many latest publications regarding generalized MCSI topology [10, 29, 73, 80].

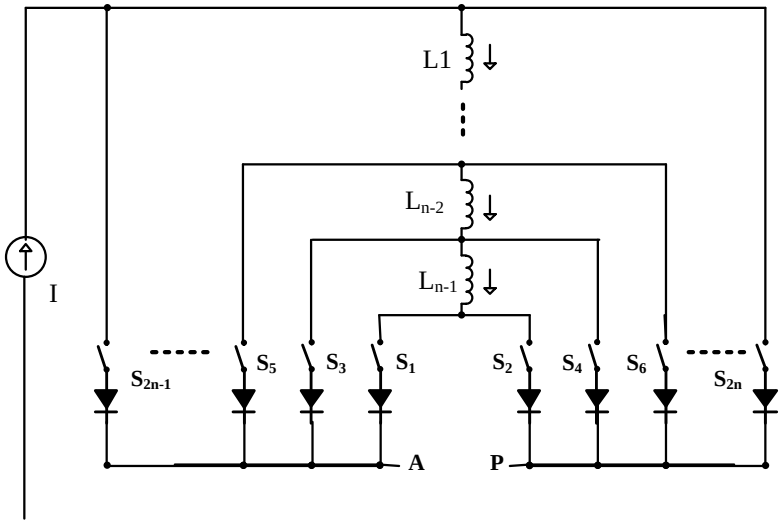


Fig.2 - 15: The generic cell re-oriented

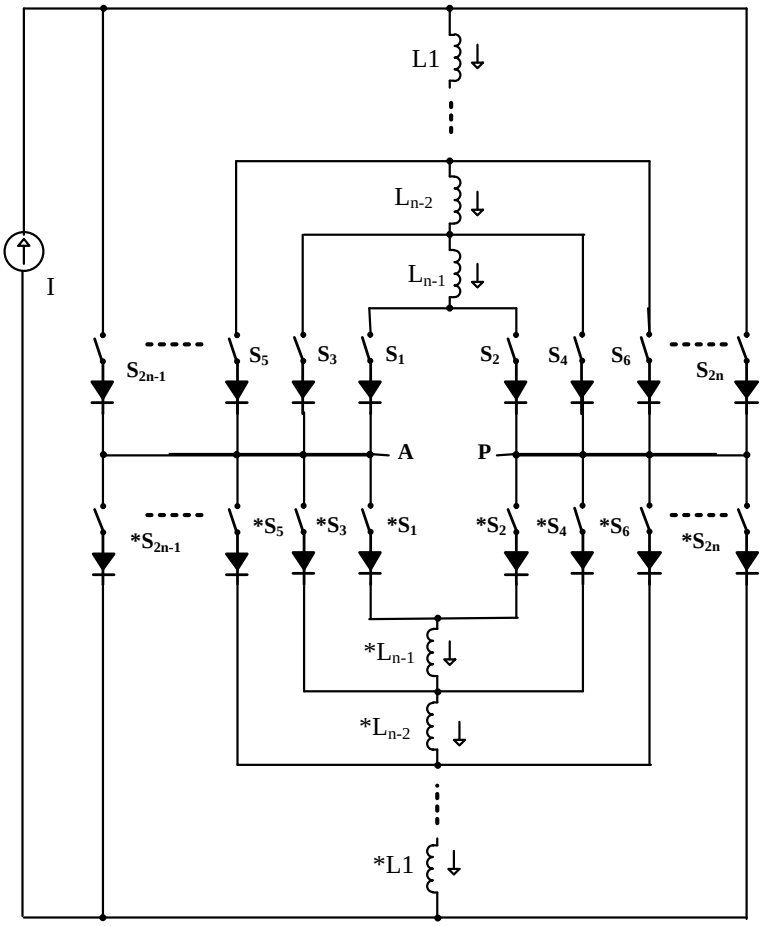


Fig.2 - 16: Final MCSI circuit

2.8 Generalized MCSI Structures

Theoretically, a generalized MCSI topology can be expanded to an infinite number of current-level thanks to its flexible generic structure. More number of levels means higher currents can be spanned by parallel switches; where theoretically a zero harmonic distortion of the output current waveform can be obtained by an infinite number of levels. In practice however, the number of achievable current levels is rather limited due to factors such as current unbalance problem, inductor current limit, packaging constraints, and the specified rating. At present, any MCSI circuit operating above five-level current output is reported to have some complexities in its control strategy. This is however, reasonable due to the fact that the generalization of MCSI topologies is relatively new compared to MVSI, which has been established for a while.

The biggest challenge in shaping the step-current waveform is to balance the dc inductor current between levels. Fortunately, albeit scarce, there are published literatures regarding this issue of MCSI available. Later in this thesis, four existing topologies (named here as Topology- I, II, III, and IV); all with one single current source, are discussed. A single-source MCSI topology is particularly attractive since it anticipates a more cost-effective structure besides a more practicable single supply of current.

2.8.1 Topology I (Antunes et al, 1999)

This particular topology (Topology I) was published in [10]. In its generic form as illustrated in Fig.2-17, this topology is identical to Fig.2-16. The structure has two parts, top and bottom parts that are symmetrically balanced; where the components (switches and inductors) from both parts are equal in numbers. With its symmetrical structure, finding the total number of switches, k employed for an n level of current can be done by;

$$k = 2(n\text{-}1) \tag{2-18}$$

Subsequently, the number of inductor, *L* can be calculated by;

$$L = (k\text{-}1) \tag{2-19}$$

Based on this generalized structure, its corresponding five-, seven- and nine-level structures are illustrated in Fig.2-18 as the examples.

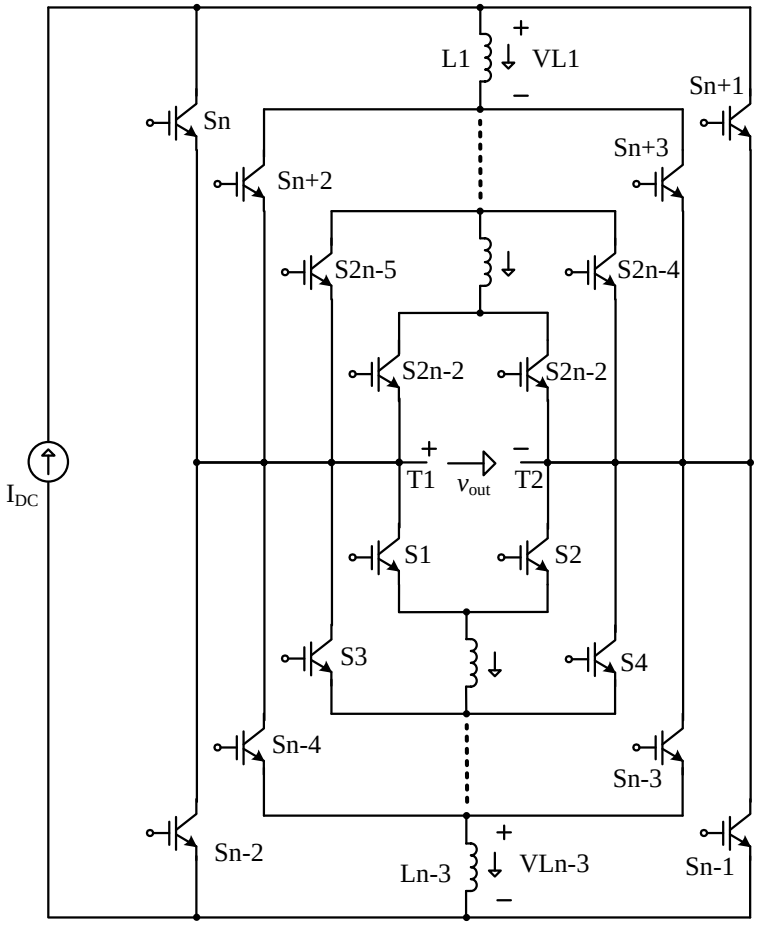


Fig.2 - 17: The generalized structure of Topology I

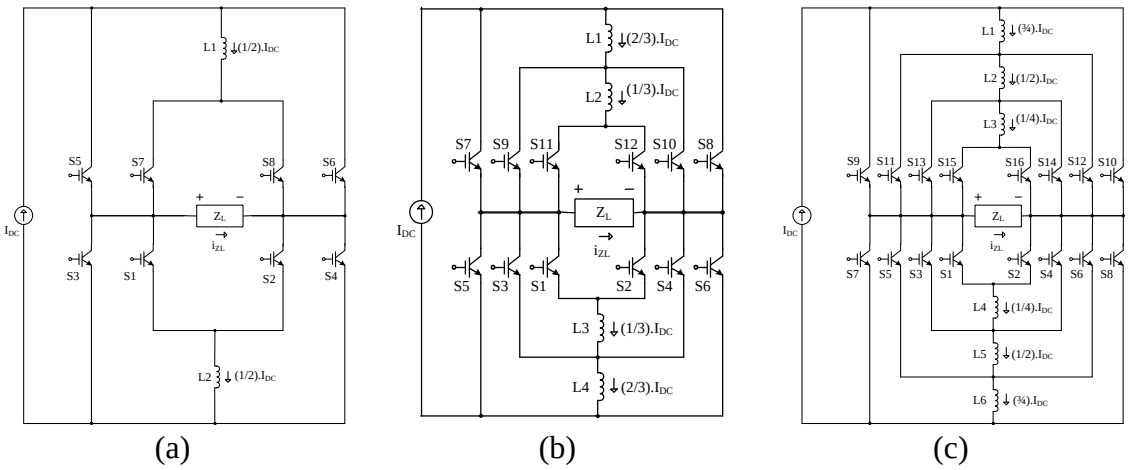


Fig.2 - 18: Topology I (a) 5-level (b) 7-level (c) 9-level

As depicted in Fig.2-18, each switch connects at one end to a sharing inductor and the other end to the load, Z_L. In order to function properly, each switch that connects to the same inductor must be complementary to each other. By designation, only one of these two switches can be turned on at one time. In Fig.2-18(a) for example, the five-level inverter structure is made up of eight PWM switches in total but only four of them are complementary switch pairs (S1-S2, S3-S4, S5-S6, and S7-S8). Similarly, for the seven-level CSI in Fig.2-18(b), the twelve switches made up six complementary switch pairs (S1-S2, S3-S4, S5-S6, S7-S8, S9-S10, and S11-S12) whereas for the nine-level CSI in Fig.2-18(c), the sixteen switches made up eight complementary switch pairs (S1-S2, S3-S4, S5-S6, S7-S8, S9-S10, S11-S12, S13-S14, and S15-S16).

Referring to Fig.2-18(a), it can be seen that in order to get through the load, the supplied dc current must enter three branches (of S5, S6, and L1) and later returns to the source also via three branches (of S3, S4, and L2). As illustrated in Fig.2-19, there are eight different states required to obtain a five-level current waveform; therefore, it is crucially important to determine the appropriate switch combinations and sequences for each state in order for the inverter to operate effectively. These switch combinations are summarized in Table 2-2.

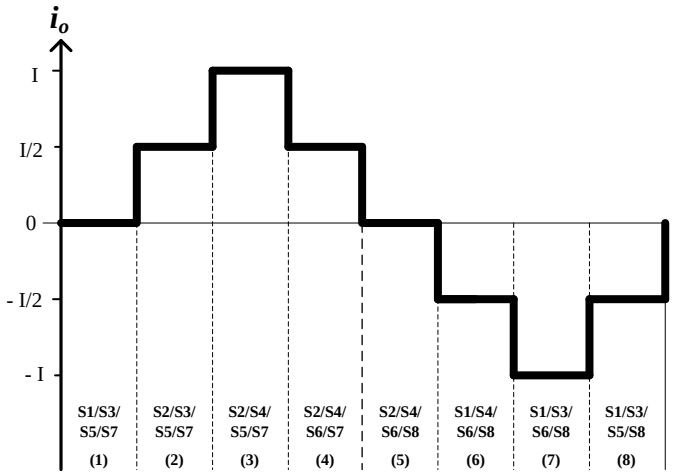


Fig.2 - 19: Five-level CSI switching sequence

Table 2 - 2: Five-level switch combinations for Topology I

Output current	Switch combination
0	S1-S3-S5-S7; S2-S4-S6-S8
+ (1/2) I	S2-S3-S5-S7; S2-S4-S6-S7
+ I	S2-S4-S5-S7
- (1/2)I	S1-S4-S6-S8; S1-S3-S5-S8
- I	S1-S3-S6-S8

Essentially, the simplest approach to appreciate the basic operation of this inverter and how the stepped-waveform can be obtained is to assume that both inductors, L1 and L2 as lossless inductors and at any time carrying half-current (I/2). It is equally important to understand that each state will not succeed individually and they must be implemented consecutively in correct sequence, in order to achieve the expected results.

From Table 2-2, for the zero output current as shown in state-I (Fig.2-19), two possible combinations existed. Suppose in the positive half-cycle, the half-current through inductor L1 commutes via switch S7 and the other half-current commutes via S5, by diverting these half-currents through switches S1 and S3, zero current will be flowing through the load. Because of the complementary operation of the

switches, the switches S6, S8, S4, and S2 are off in this state. In state-II, the half-current through inductor L1 still commutes via switch S7 and the other half-current commutes via S5; by turning off S1 and turning on S2, half of the current will have to flow by the load impedance. Similarly in state-III, the half-current through inductor L1 still commutes via switch S7 and the other half-current commutes via S5. When switch S3 is turned off and its complementary switch S4 is turned on instead, both half-currents are forced to flow by the load impedance, providing the full-current for the current state. Finally in state-IV, when the switch S5 is turned off and replaced with its complementary switch S6, half of the current is forced to return to the source and now the load impedance only sees half-current through it. Similar switching procedures are practised for the negative half-cycle of the output current. The full switch sequences and load current paths of the five-level inverter demonstrating how individual sequences are combined to yield the desired output are depicted in Fig.2-20.

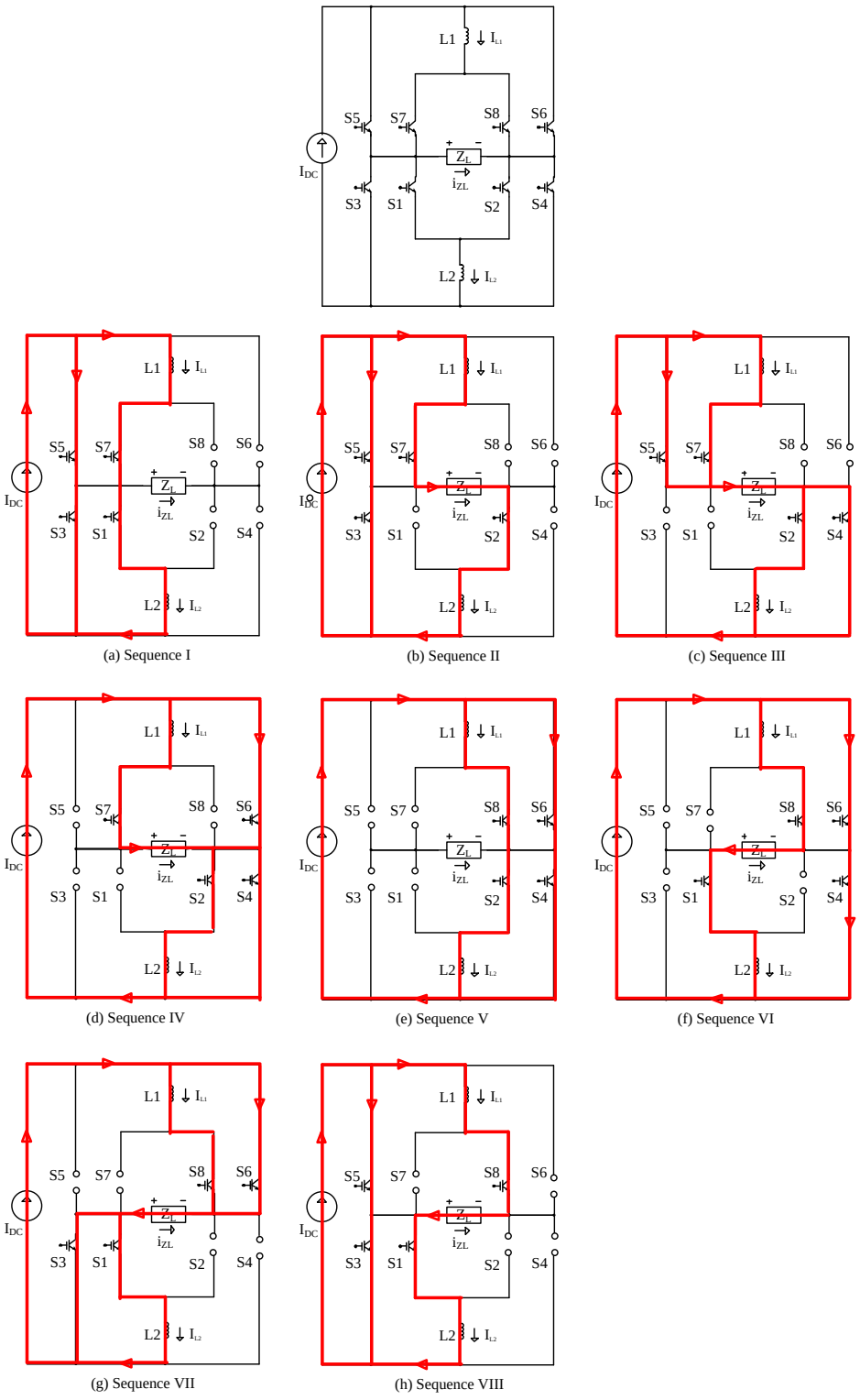


Fig.2 - 20: Single-phase five-level inverter circuit and its corresponding switching sequences (a)-(h)

In reality however, these inductors contain losses and their currents can be out of balance by the effect of the load impedance. This can be explained in Fig.2-20(b) (Sequence-II) in steady state, where it is expected that the current through S5 will be larger than through S7 since the branch of S7 sees both inductor and load impedances; therefore some sort of current compensation method is required in this state to overcome this setback. It is also shown that during intermediate levels (Fig.2-20(b), (d), (f), and (h)), the load impedance is always present in series with one sharing inductor, hence reducing the respective inductor current in steady state. To avoid current imbalance in this particular inductor, this can be compensated by choosing the next intermediate switch sequence that in series with the other inductor; thus raising the previously decreasing inductor-current while at the same time reducing the other branch-current. This multilevel CSI also has demonstrated an effective inductor balancing technique via an open-loop control by manipulating the occurring redundant switch combinations. With balanced inductor current, step current waveform can be effortlessly achieved; consequently minimizing the current harmonics.

For a multilevel CSI, a switching sequence is called a "symmetric strategy" (Fig.2-21) if all the switches conduct precisely with a pulse-width of 50 % and an "asymmetric strategy" (Fig.2-22) if otherwise [10, 84, 85]. A well-chosen switching strategy influences distinct achievement i.e. the symmetric strategy is convenient but it contributes to a higher current ripple in inductors while the asymmetric strategy can further reduce the current harmonics with appropriately selected angles of α and β. With symmetric strategy also as illustrated in Fig.2-21, the inductor current balance is achieved in two periods whereas with asymmetric strategy shown in Fig.2-22, the inductor current balance is achieved in one period. Nevertheless, at higher than five-level CSI, this topology provides excessive numbers of redundant switch combinations that identifying the accurate switching sequence to balance the inductor current is particularly demanding to be realized; therefore restricting its potential for a higher levels of CSI.

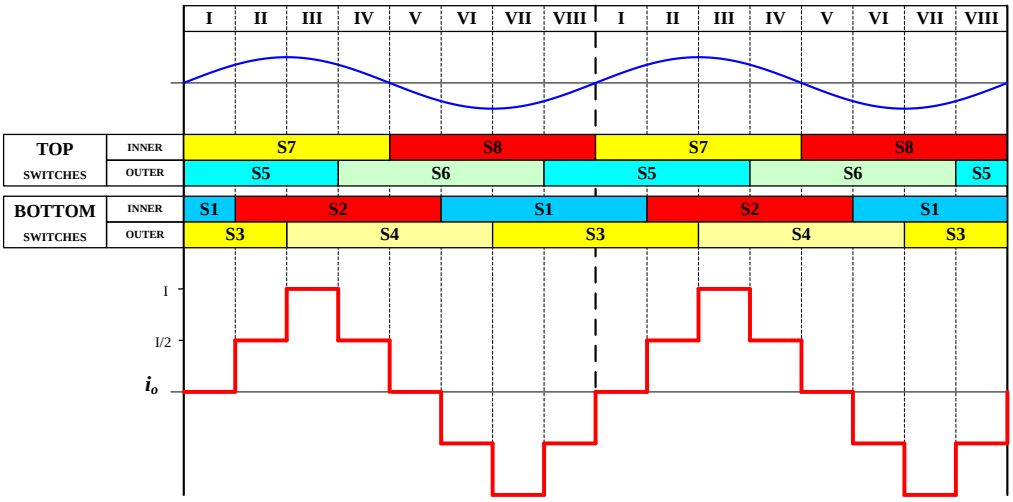


Fig.2 - 21: Five-level symmetric switching sequence

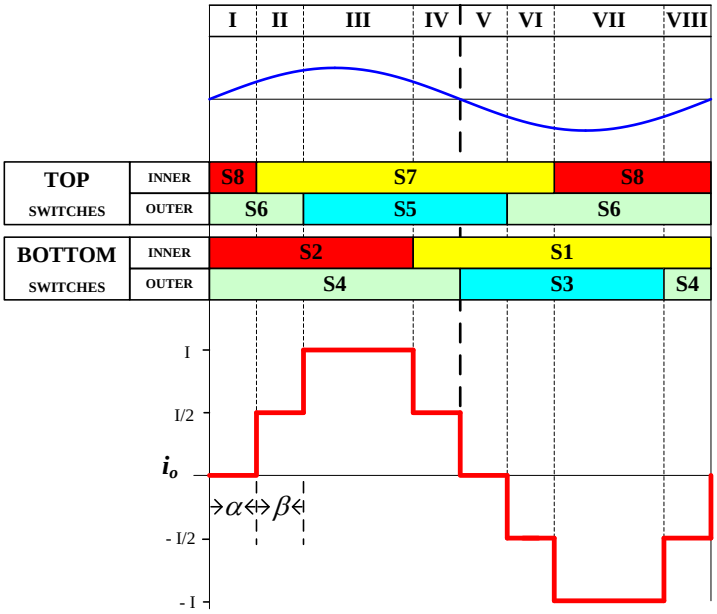


Fig.2 - 22: Five-level asymmetric switching sequence

2.8.2 Topology II (Bao et al, 2006)

Fig.2-23 shows the generic structure of the Topology II whereas its corresponding five-, seven- and nine-level CSI are as illustrated in Fig.2-24. Topology II was proposed in [29] as an alternative to Topology I where the latter was simplified by

eliminating the mirror circuit and replaced with two switches. The load is connected between the two return switches S1 and S2.

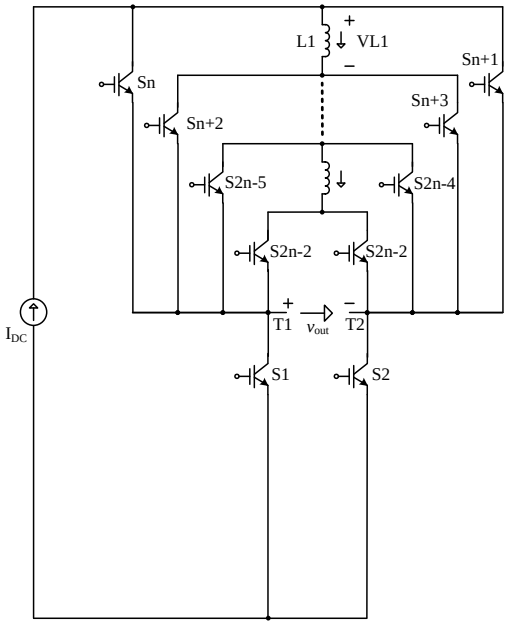
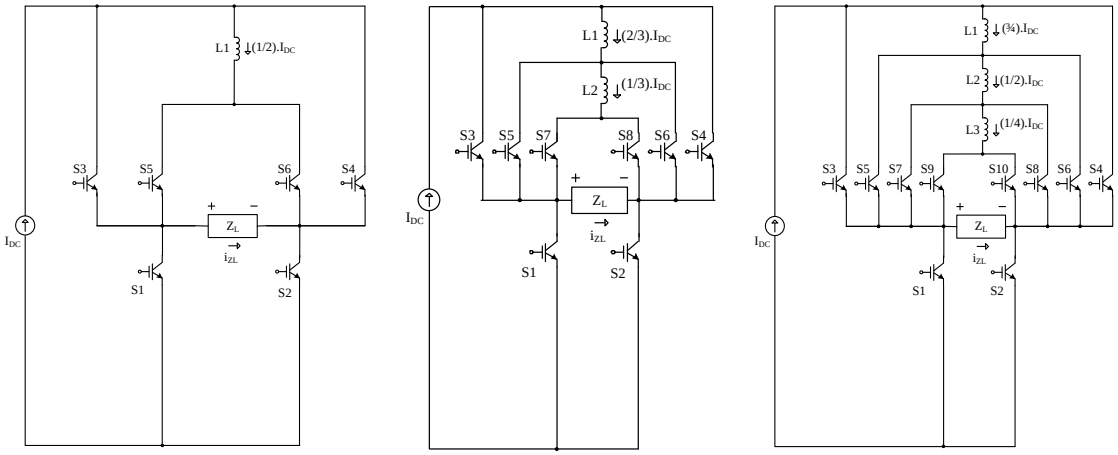


Fig.2 - 23: The generalized structure of Topology II



(a) (b) (c)

Fig.2 - 24: Topology II

(a) 5-level inverter circuit (b) 7-level inverter circuit (c) 9-level inverter circuit

Except for the switch combinations and sequences, the fundamental operation of topology II does not differ from previously discussed strategy. Fig.2-25 depicts the new switching combinations and sequences necessary in order to acquire the five-level CSI current waveform of Topology II. It can also be seen that in Topology II, with symmetric strategy the current balance can be achieved in just one period compared to two periods previously in Topology I. The full switch sequences and load current paths of the five-level inverter are shown in Fig.2-26.

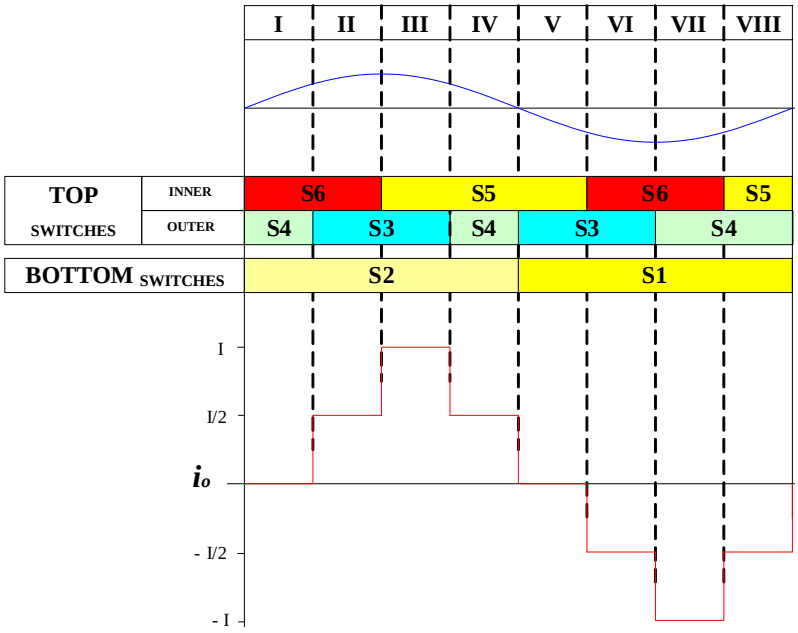


Fig.2 - 25: Topology II five-level switching sequence

The modified topology has not only successfully reduced the number of components compared to its origin, but it has also simplified the control strategy where the dc inductor current balance in symmetrical switching sequence can be achieved in a single period as opposed to two consecutive periods in Topology I. The setback is that the two return switches must have bigger ratings than all other switches since there is only a single load current pathway for returning currents compared to multiple splitted pathways in the previous topology. Other than that, similar to Topology I, the control complexity for higher level CSI is remained.

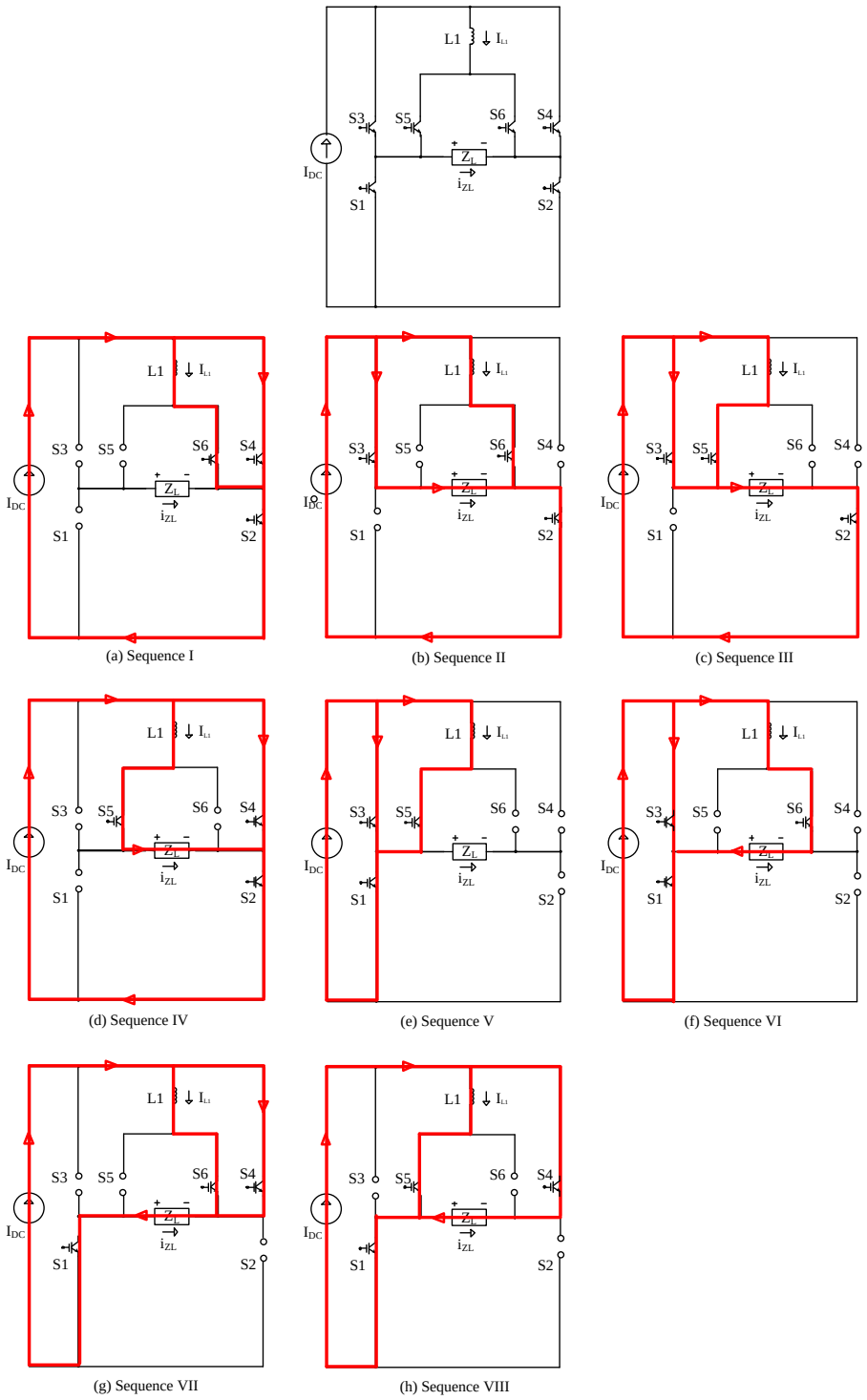


Fig.2 - 26: Single-phase five-level inverter circuit and its corresponding switching sequences (a)-(h)

2.8.3 Topology III (Xiong et al, 2004)

Unlike the previously discussed topologies, the third topology (Fig.2-27) that was proposed in [30] is classified as the multi-stage group from Fig.2-12. Obviously, its key dissimilarity to previous topologies is the two parts structure; (1) the DC bus current controlling circuit and (2) the inverter circuit. In the first circuit, the main current supply is divided into branches that controls the magnitude of current flow through the load; which magnitude depends on the level of CSI employed i.e. for five-level CSI each branches will carry half-current ($I_{DC}/2$). Since these currents are unidirectional, an H-bridge is utilised in the second circuit to allow bidirectional current flow. Thus, the term multi-stage is used. The circuit is re-drawn to illustrate Topology III structures in five-, seven- and nine-levels (Fig.2-28).

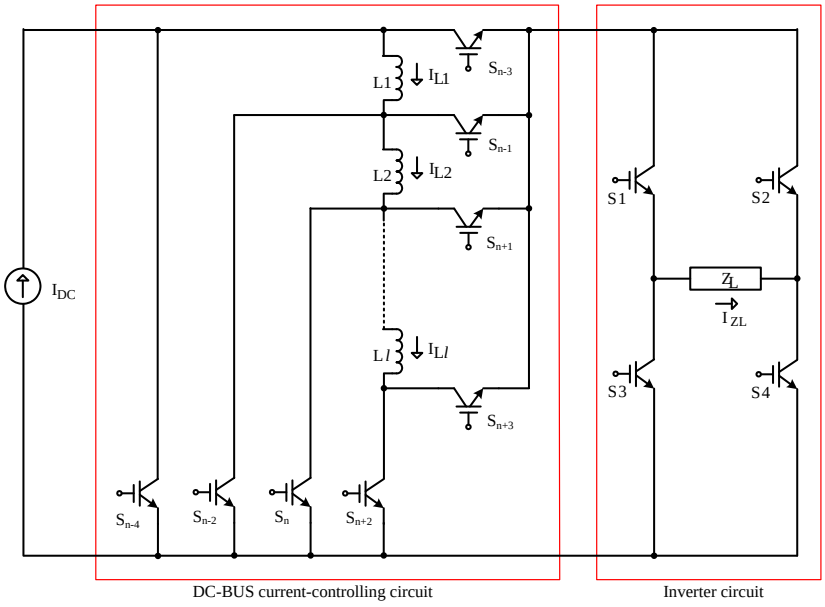


Fig.2 - 27: Generalized structure of Topology III

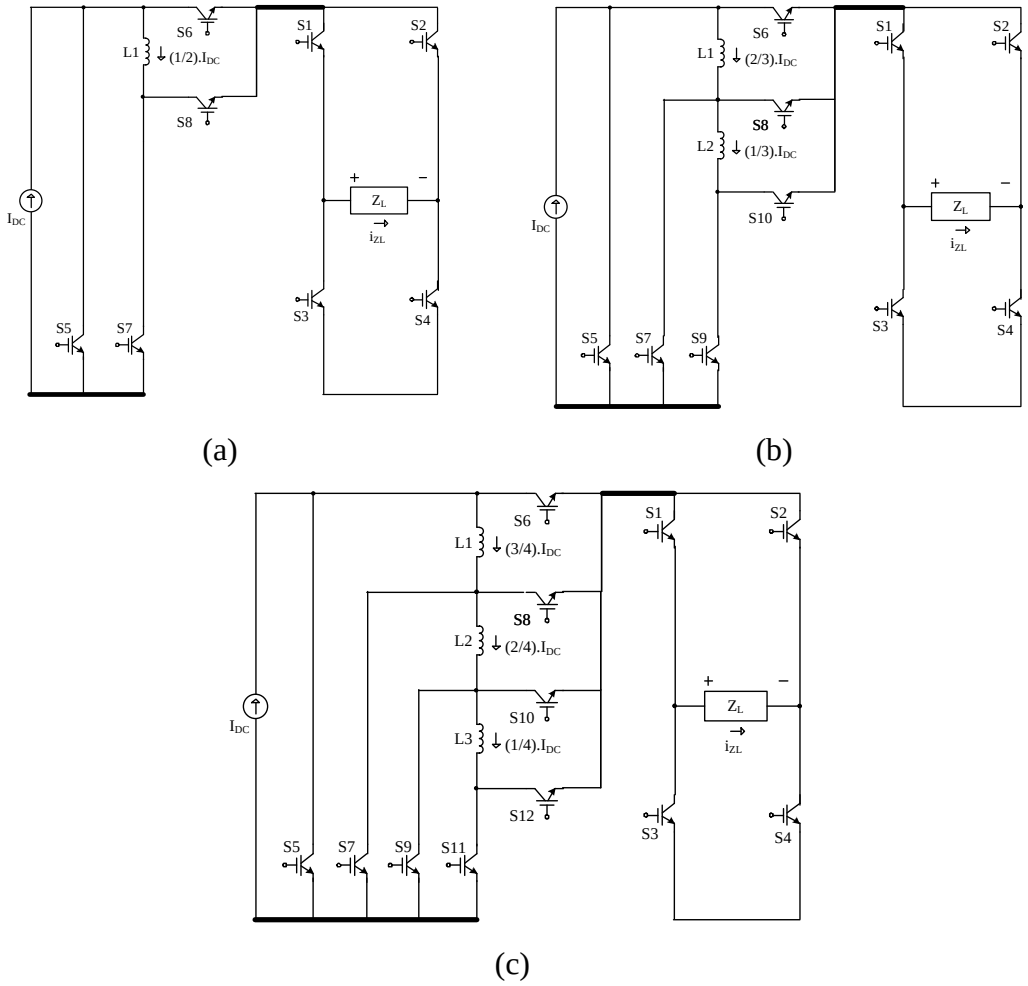


Fig.2 - 28: Topology III

(a) 5-level inverter circuit (b) 7-level inverter circuit(c) 9-level inverter circuit

By referring to the switching sequence and the switch combinations for the five-level CSI in Fig.2-29, it can be seen that in terms of standard operating procedures, this topology works in similar way to both previously discussed topologies where the expected staircase-shaped current can be achieved via pre-determined switching sequence in one period. It is also demonstrated that the five-level current can be realized by simple open-loop control although just like previous topologies, it is less appealing at higher than five-levels due to increased control complexity. In addition, the H-bridge adds extra power switches to the

circuit, which indicates that this topology requires more component than Topology II but fewer components than Topology I. The full switch sequences and load current paths of the five-level inverter are shown in Fig.2-30.

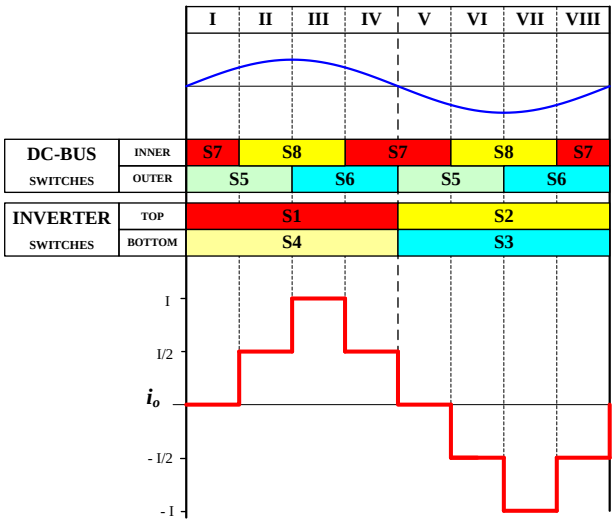


Fig.2 - 29: Topology III Five-level switching sequence

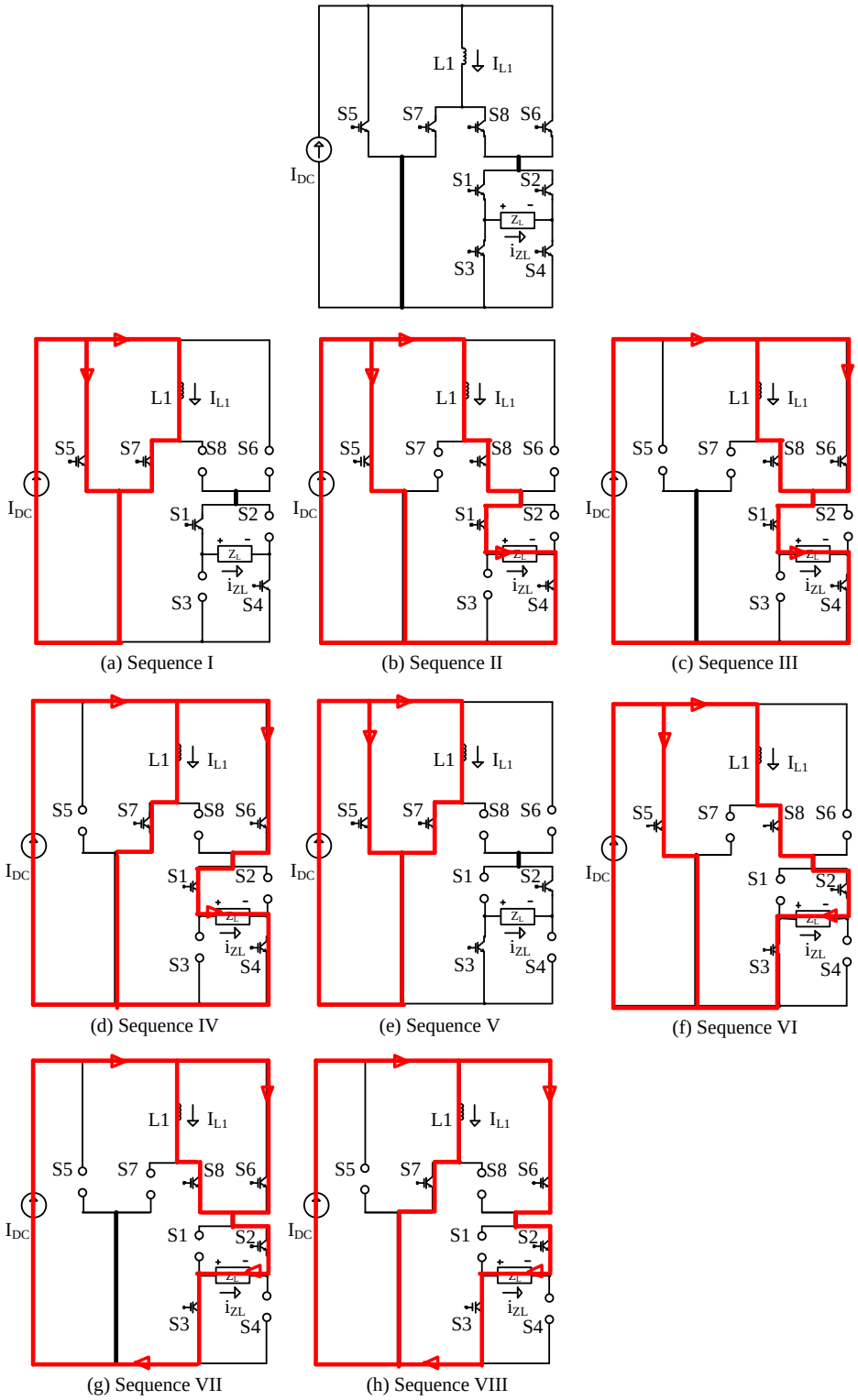


Fig.2 - 30: Single-phase five-level inverter circuit and its corresponding switching sequences (a)-(h)

2.8.4 Topology IV (Suroso et al, 2010)

Topology IV was proposed in [34] and is shown in Fig.2-31 . In this topology, an H-bridge is intentionally employed at the front-end to allow bidirectional current flow. The other H-bridges are connected in parallel with inductor cells. These inductor-cells generate intermediate currents for multilevel current waveforms; where each H-bridge in the main inverter circuit generates five-level current output including zero level, thus two H-bridges generate a nine-level inverter. A seven-level inverter can not be achieved. The circuit for five- and nine-levels are shown in Fig.2-32.

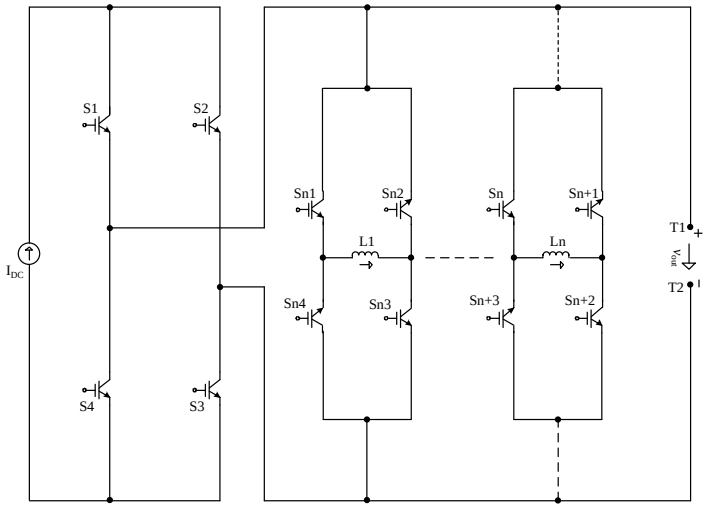


Fig.2 - 31: The generalized structure of the Topology IV

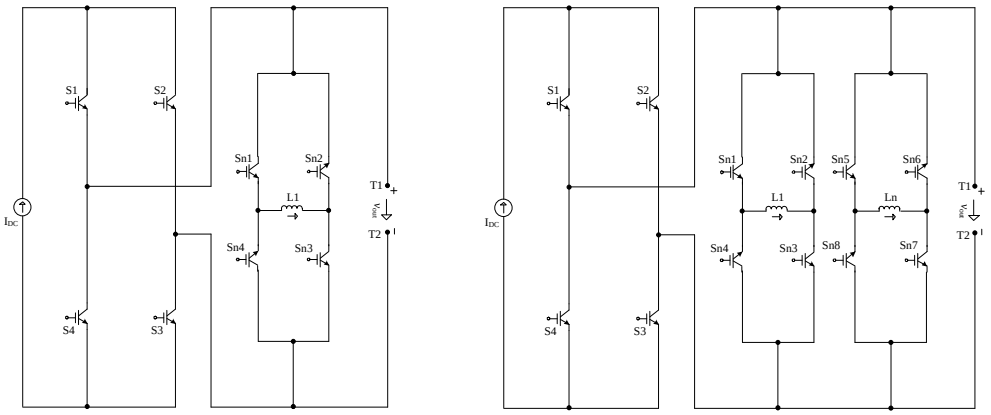


Fig.2 - 32: Topology IV

(a) 5-level inverter circuit (b) 9-level inverter circuit

Similar to previous topologies, switch combinations and switching sequences are the two main elements that determine successful operation of inverter. By careful selection of pre-determined switch combinations and switch sequences, the output current waveform can be predicted to be as shown in Fig.2-33. It is expected that for five-level CSI, five-level current can be realized by simple open-loop control just as other topologies. However, increased control complexity is foreseen for higher levels. Similar to Topology III, the H-bridge adds extra power switches to the circuit therefore comparable operational characteristics of both inverters can be expected. The full switch sequences and load current paths of the five-level inverter are shown in Fig.2-34.

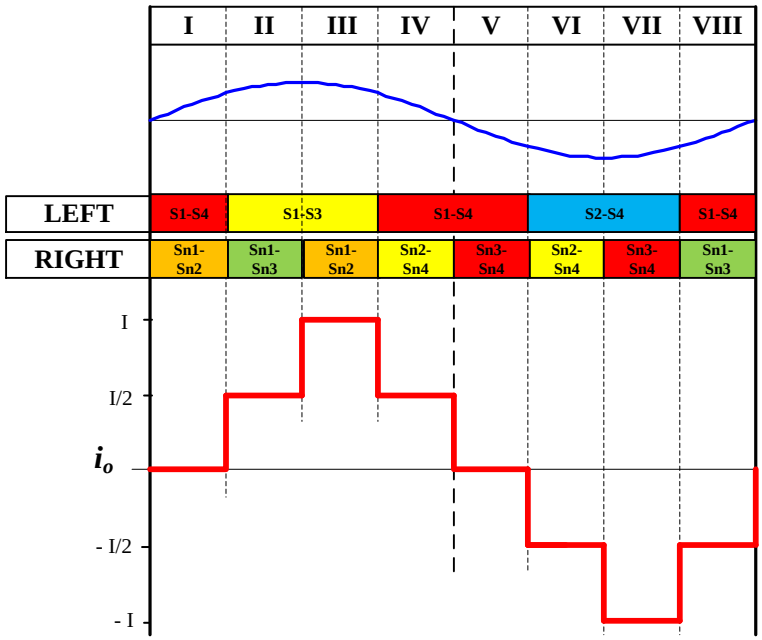
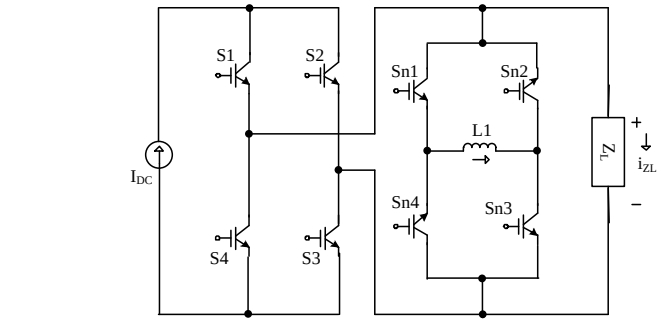
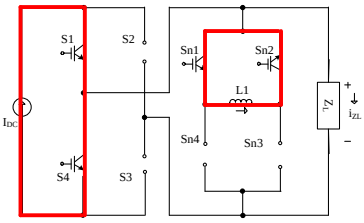
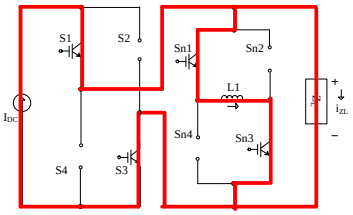


Fig.2 - 33: Topology IV five-level switching sequence

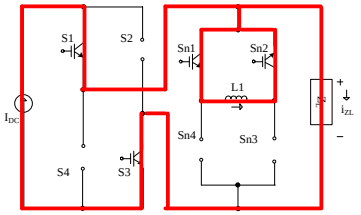




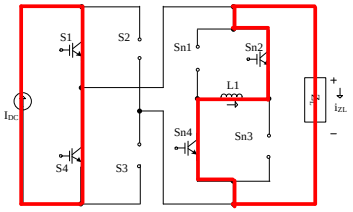
(a) Sequence I



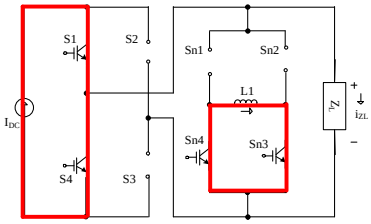
(b) Sequence II



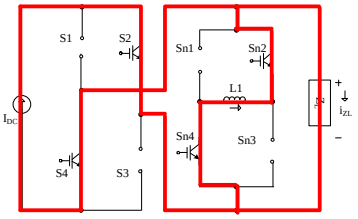
(c) Sequence III



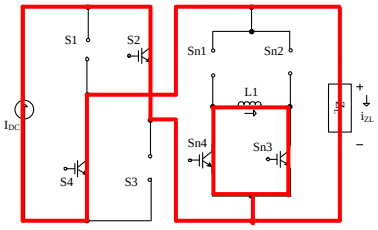
(d) Sequence IV



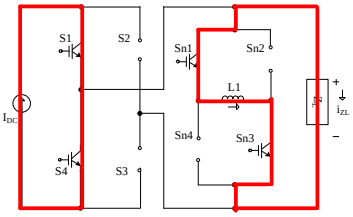
(e) Sequence V



(e) Sequence VI



(f) Sequence VII



(g) Sequence VIII

Fig.2 - 34: Single-phase five-level inverter circuit and its corresponding switching sequences (a)-(h)

2.9 Topology Comparisons

In order to compare topology performances, a number of evaluations including computer simulations are performed. From the economic point of view, it is convenient to compare the number of components employed in each topology to relate to cost. Table 2-3 shows that circuit Topology I employs the highest number of components for the five-level CSI and requires twice as many components per-increment compares to other topologies for higher-than-five level CSI whereas Topology II employs the lowest number of components with six power switches. By correlating the number of components employed to cost, it can be observed that the cost estimation for Topology II is the lowest of all four topologies. This estimation intensifies significantly at increased CSI level i.e. for a nine-level CSI, Topology I employs the most components of 22, followed by Topology III of 15, Topology IV of 14 and Topology II of 13. In terms of percentages, the estimated cost of Topology II will be at 59.1 %, 68.2 % and 63.6 % of the costs associated to Topology I, III and IV respectively.

Table 2 - 3: Structural comparison for five-level CSI

	Multilevel Topology	**I**	**II**	**III**	**IV**
(a)	No of power switches	8	6	8	8
(b)	No of sharing inductors	2	1	1	1
(c)	Total = (a)+(b)	10	7	9	9
(d)	cost per-unit (a)+(b) / (c)	1	0.7	0.9	0.9
(e)	Additional no of switches required per 2-level increment	+4	+2	+2	+2
(f)	Additional no of inductors required per 2-level increment	+2	+1	+1	+0.5*
(g)	No of switches required for 9-level CSI (4 level increment) = (e) x 2	+8	+4	+4	+4
(h)	No of inductors required for 9-level CSI (4 level increment) = (f) x 2	+4	+2	+2	+1
(i)	Total components for 9-level CSI Total = (c)+(g)+(h)	22	13	15	14
(j)	Estimated cost comparison (%) (i)/22 x 100%	100%	59.1%	68.2%	63.6%

* Topology IV level increment jumps from level 5 to level 9 thus +0.5 inductor increment per 2-level

The better approach to compare the operational cost of these inverters is via their volt-ampere (VA) ratings; where, VA are the product of the peak voltage and average current of the circuit [86];

$$VA = V_{avg} \text{ x } I_{pk} \tag{2-20}$$

The VA unit is used for the apparent power in an ac electrical circuits which provides information on how much energy these inverters will consume thus directly reflecting on its operating cost. The system overall efficiency is another characteristics that is directly related to inverter cost although indirectly related to system reliability since an inverter efficiency also depends on its load profile [87]. Conventionally, to analyse an inverter efficiency, η can be calculated as;

$$\eta = \frac{P_{out}}{P_{in}} x \ 100 \ \% \tag{2-21}$$

Where η is the efficiency in percentage (%);

P_{out} is the output power (in Watts);

P_{in} is the input power (in Watts).

While an electric current flowing through a conductor generates heat (power dissipation), the dissipated power can be calculated as;

$$P_{diss} = I^2R \tag{2-22}$$

where P_{diss} is the dissipated power (Watts);

R is the resistance of the conductor (Ω);

I is the current (A).

Although there are various types of losses in power electronic circuits i.e. DC losses, switching losses, semiconductor losses and high frequency transformers losses; however, regularly equation (2-22) is a good approximation of the overall losses in the circuit [87, 88]. The power dissipation P_{diss} of the circuit can then be

calculated by defining R as the overall resistance between input and output of the circuit and I as the output current. Better approximation can be obtained if the no-load power consumption or the power dissipated by the circuit without any load connected is considered. For that case, the total power loss can be calculated as;

$$P_{loss} = P_o + I^2_{out} R \quad (2\text{-}23)$$

Where P_{loss} is the total power dissipation (Watts);

P_o is the no-load power dissipation (Watts);

R is the "resistance" between the input and the output (Ω);

I_{out} the output current (A).

Taking equation (2-23) into account, the simplified equation for the inverter efficiency can be calculated as;

$$\eta = \frac{P_{out}}{P_{out}+P_{loss}} x\ 100\ \% \quad (2\text{-}24)$$

Where η is the efficiency measured in percentages (%).

In this chapter, the topology performance comparisons are performed via computer simulations using SimPowerSystems toolbox in Matlab/Simulink applying parameters as summarized in Table 2-4. In every simulation, the value of load resistance, R_{Load} are adjusted so that the input current, I_{in} will always equals to 10A. This practice is especially crucial when comparing the VA ratings of the IGBT switches of different topologies since it involves the measurement of the peak voltage and the average current across switches. Other than the VA ratings, these inverters are also compared in terms of their efficiencies, η, the total harmonic distortions (THD) and also distortion factors (DF). All switching simulations are using low-frequency modulation techniques as applicable methods in most previously published CSI papers.

Table 2 - 4: Simulation parameters

Parameter	Label	Value	Unit
Rated power	-	0.5	kW
Rated input current	I_{in}	10	A
Output frequency	-	50	Hz
Load	R_{Load}	adj*	Ω
Inductor	L	45	mH
Internal resistance	r'_L	0.3	Ω
Filter capacitor	C	150	µF
$V_{CE\ (IGBT)}$	-	2	V
$R_{OFF(IGBT)}$	-	1	MΩ

As illustrated in Fig.2-35, it can be seen that Topology II which has the lowest components employed also exhibits the lowest VA units. This indicates that Topology II has the lowest operating cost of the four. The recorded VA units do varies considerably among topologies; however, the Topology I which utilized the most number of components plus an extra inductor has VA rating more significant than others. It should be expected that structures with less inductors such as topology II, III and IV would produce less losses and would hence enjoy better efficiencies. However, as shown in Fig.2-36, the topologies with least number of inductors such as Topology II, III and IV have better efficiencies only at lower load currents, however, the Topology I proves to be more efficient at higher load currents.

By comparing the inverters current THD before and after filtration, as can be seen in Fig.2-37, it is demonstrated that the current THD without any filtering are equally high for all topologies i.e. at approximately above 25 %; whereas for the filtered current the THD is much lower at below 15 %. Clearly, it can be suggested that all topologies exhibit comparable performances for the five-level CSI.

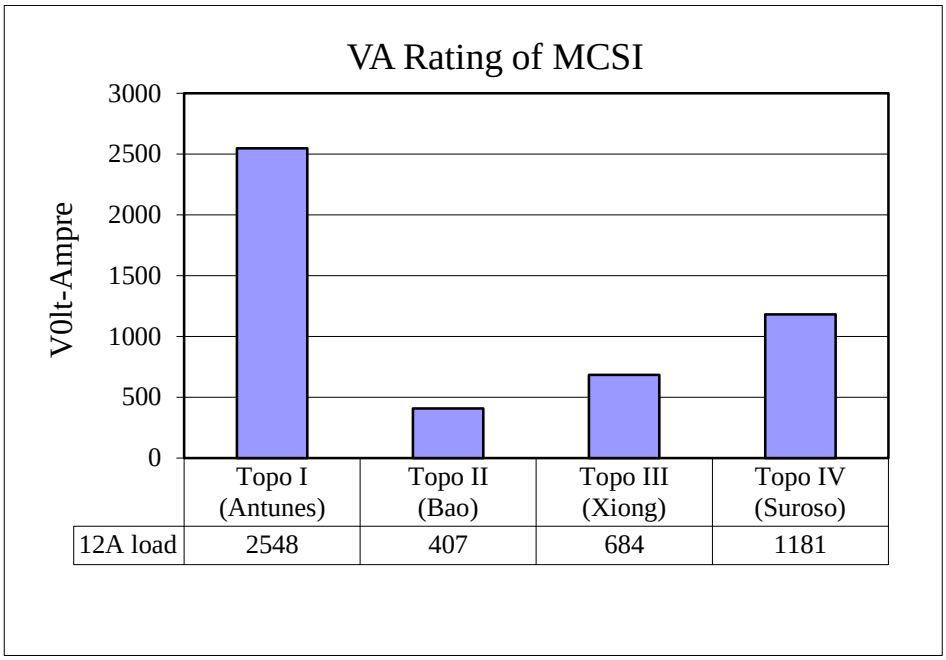


Fig.2 - 35: Volt-Ampere (VA) comparison

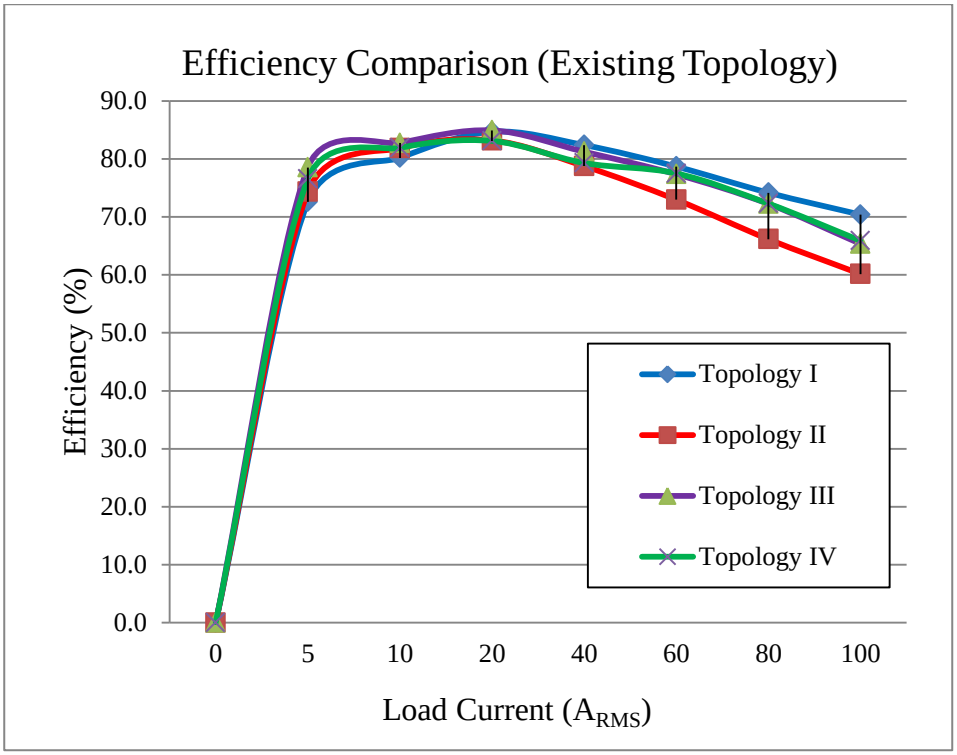


Fig.2 - 36: Efficiency vs. Load Current

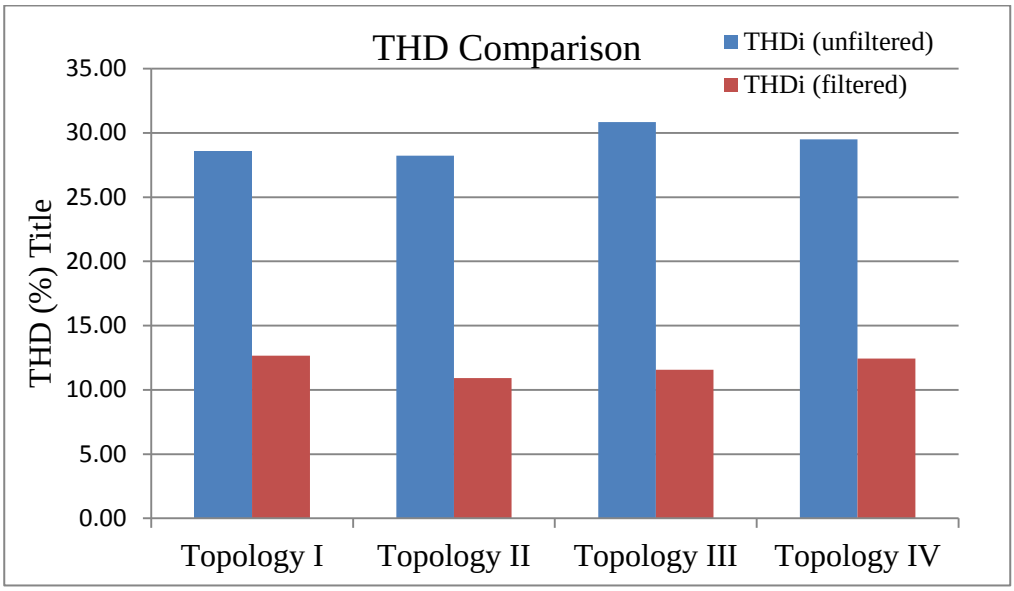


Fig.2 - 37: THD comparison

Finally, it can be summarized that although the structures with less per-unit inductance (topologies II, III and IV) produce lower losses, they also produce higher current ripples. This could imply that more complex control technique would be required for satisfactory operation while this extra complexity can be easily translated into additional cost. Therefore, it can be concluded that none of these topologies is superior to others. Moreover, at seven output levels or higher, the control needed for each topology are equally complex, and the best course of action would often be to select the topology with the least number of components and lowest cost.

3.0 Summary

Recent development in electronic devices incites many new researches into MCSI area. Emerging generalized MCSI inverters have been developed mainly by the duality theory concept.

Single-source generalized topologies have distinctive characteristics; for instance, their main current supplies are split to a number of smaller current sources by DC inductors before being feeded into the loads. At any instance, the load must be

located in an H-bridge. The H-bridge; with four complementary fully controllable switches such as IGBTs, allows the total current to change direction cyclically through the load, thus shaping an alternating step-current waveform through it.

The biggest challenge in shaping the step-current waveform is to balance the dc inductor current between levels. More number of levels means higher currents can be spanned by parallel switches; where theoretically a zero harmonic distortion of the output current waveform can be obtained by an infinite number of levels. Unfortunately, the number of achievable current levels in practice is rather limited due to factors such as current unbalance problem, inductor current limit, packaging constraints, and also the circuit layout restrictions. Finally, by simulation it was found that existing topologies have comparable performances and the preferred topology would finally come down to the economic factor.

CHAPTER 3

Current-Source Inverter Control for High- and Low-Load Conditions

Previously in Chapter 2, it was clear that the staircase-shaped waveforms generated by multilevel inverters reduce the harmonic contents of the signals. While it is fairly easy to produce these waveforms regardless of topology with currently available control methods; it is quite challenging to achieve high quality output waveforms. For example, for the redundant-switching (RS) control technique, an open-loop control strategy based on different switch combinations with identical outputs were introduced in [10, 69]; while the system operation is simple and economical, this technique however suffers when operating under high-load conditions. In [32, 37], the closed-loop control based on phase-opposition disposition PWM (POD-PWM) is used to control switch combinations in accordance with the output voltage and current polarity at each switching period to maintain the dc inductor current. Although this technique is effective for different types of loads (resistive, inductive and capacitive), its operation under high-load condition has not been experimentally investigated. Finally in [30], no explicit description of the switching control was provided for high-load conditions. This chapter proposes a control strategy to improve the harmonic content of the inverter output current when operating under both high- and low-load conditions, named here as redundant switching-multi pulse modulation (RS-MPM) [33]. The remainder of the chapter focuses on this simple and inexpensive controlling strategy of the half-level inductor current and also its resulting simulation and experimental performances.

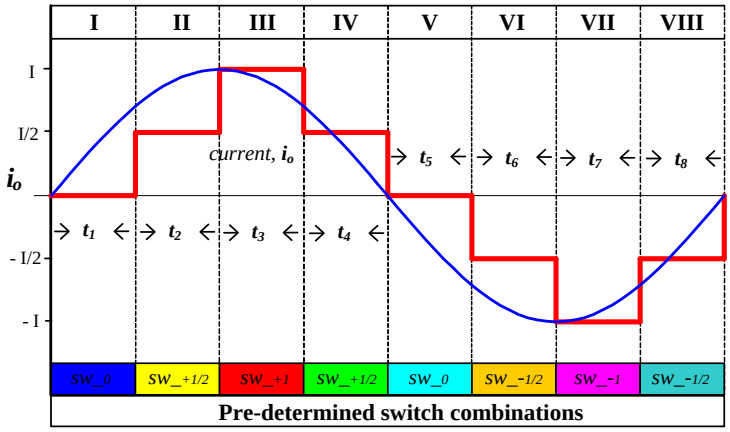
3.1 MCSI Control Strategy

Generally the performance of an MCSI, with any switching strategies, can be related to the harmonic contents of its output current regardless of topologies. Their control strategy is simplified by duality principle whereby any methods that works for MVSI topology can also be adapted to work for MCSI. At present, in multilevel technology there are several well-established modulation strategies such as the Sinusoidal Pulse Width Modulation (SPWM), Selective Harmonic Eliminated Pulse Width Modulation (SHE-PWM), and Optimized Harmonic Stepped-Waveform Technique (OHSW) [32]. However as multilevel CSIs are sparely used, only a few control methods have been published [1, 48, 89]. This is reasonable since any methods that were adapted from MVSI require diverse complexity of modifications which resulted in many researchers prefer to adhere to the well known approaches among the MVSI family. Regardless of any specific MCSI topology that is used, the common issue for these multilevel inverters is how to control effectively the magnitude of the intermediate dc-link current level where, without current balancing control of some sort, the current cannot be maintained at a constant level. Previously, this current balance has been achieved using either fundamental frequency switching [90], or active PWM control [91] using switching state redundancies.

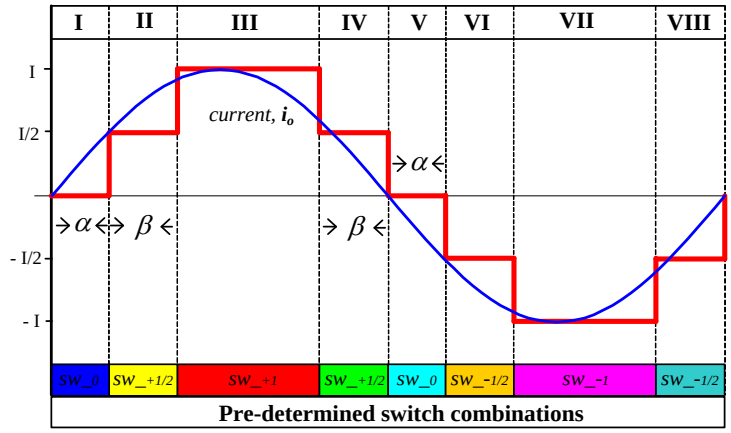
3.1.1 Fundamental frequency Switching Strategy

The fundamental frequency switching strategy also known as the low frequency modulation (LFM) is often employing a redundant switching (RS) technique that can be classified as design-level control for MSCI where it takes advantage of many occurrences of switching combinations with the same current output to generate the desired staircase-shaped current in an open-loop setting. This technique, as illustrated in Fig.3-1 can be divided into two categories; (a) symmetrical- and (b) asymmetrical control strategies. For a five-level MCSI in symmetrical control strategy, its period is divided into eight different states that

have equal switching times for t1~t8. In every states however, the switching combinations vary according to the anticipated level of current-output either zero, intermediate or full current. This strategy is effortless yet working. Alternatively, an asymmetrical control strategy can be implemented whereby the state's switching times, α and β are controlled; thus at the same time controlling the output current shape. With this strategy, superior THD can be accomplished when using the correct value of α and β [91].



(a) Symmetrical Switching Strategy



(b) Asymmetrical Switching Strategy

Fig.3 - 1: Low frequency switching

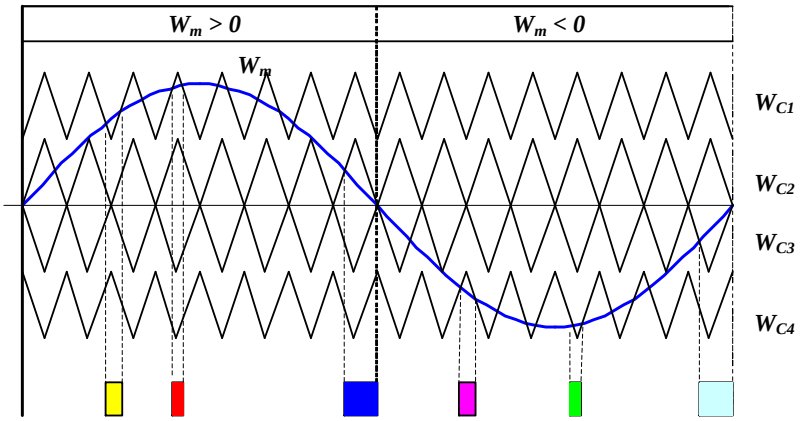
Antunes et. al. [10] introduced redundant-switching (RS), a control strategy based on different switch combinations with identical outputs in LFM. The system

operates without any closed-loop control and is simple and economical. However, this technique suffers when operating under high-load conditions. Similarly, Xiong et. al. [30] claimed success in controlling the inverter current using this technique but no explicit description of the switching control was provided for high-load conditions. Although low frequency switching implementation has been proven to be easy and simple for five-level MCSI, it is however, too complex or even impractical at much higher MCSI level. An immediate solution to this problem is to employ PWM switching with closed-loop control.

3.1.2 PWM Control Strategy

PWM controls with feedback are generally employed in MCSI not just as an alternative but most frequently as an upgrade to LFM control since PWM controls are more precise and complex; hence more costly. While LFM method operates with fixed switching pattern, the PWM method allows alternate switching patterns to be implemented according to the feedback signal; thus this method demonstrates better flexibility and practicality than the previous method particularly when the converter has large number of switching states redundancies.

Fig.3-2 illustrates one example of the POD-PWM control strategy by Bao et. al. [29] which could control this CSI appropriately. In this approach, the modulation signal, Wm is continuously compared to four triangular carrier signals, WC1, WC2, WC3, and WC4 in order to determine which switching combinations will produce the desired output current. The outputs of these comparisons are used to determine the required switching combinations. Whilst in the event of more than one possible switching combination existed; which normally occurs during intermediate current level, the inductor-current balancing is achieved via phase detection scheme where the inductor-current and voltage polarity is fed back to the controller to determine the required switching combination. The overall control procedures are summarized in a simplified diagram as illustrated in Fig.3-3.



W_m	Comparator states	Switching combinations
$W_m > 0$	$W_m > W_{C1}$	
	$W_{C2} < W_m < W_{C1}$	
	$W_m < W_{C2}$	
$W_m < 0$	$\|W_m\| > \|W_{C4}\|$	
	$\|W_{C3}\| < \|W_m\| < \|W_{C4}\|$	
	$\|W_m\| < \|W_{C3}\|$	

Fig.3 - 2: POD-PWM control

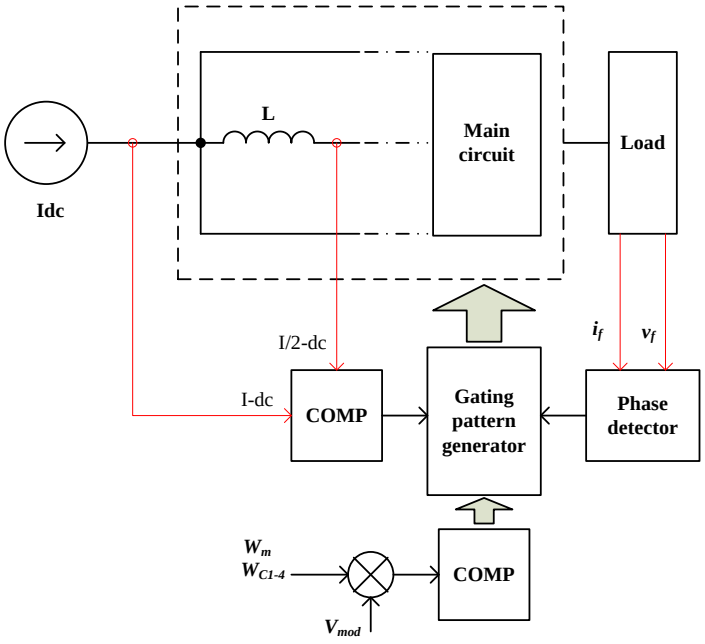


Fig.3 - 3: Simplified overall control diagram

The utilization of the PWM control strategy has been very effective to control the intermediate inductor current for different types of loads (resistive, inductive and capacitive); however, similar to the LFM control strategy its operation under light-load condition requires additional control complexity in order to be as effective. Therefore, a new control strategy has been proposed to improve the harmonic contents of inverter output current when operating under both high-load and low-load conditions while focusing on a control strategy with low level of complexity and also cost.

3.2 Proposed MCSI Control Strategy

Although both techniques as discussed above provides satisfying methods to control the half-level inductor currents in MCSI circuits, both also exhibit severe deficiency when operated under high-load conditions. Thus, a new control strategy to improve the harmonic content of the inverter output current when operating under high-load conditions is proposed where the focus is on controlling the half-level inductor current to a constant dc value without using any complex or costly control technique. This is achieved by combining the advantages of previously published methods; LF modulation and PWM modulation, into one simple and low-cost solution, named here as redundant switching-multi pulse modulation (RS-MPM).

For ease of understanding, all discussions will be based on one topology, shown in Fig.3-4 [29] although RS-MPM is applicable to other multilevel CSIs. This topology (Topology II) was selected because it has the lowest component count and therefore offers the lowest redundant switch combinations to be considered for the proposed method. To generate the five-level output current, the possible switching combinations that can be utilized are shown in Table 3-1. There are two possible combinations for each zero- and half-current level, a feature that will be utilised in the proposed control method to improve the quality of the circuit output current waveforms.

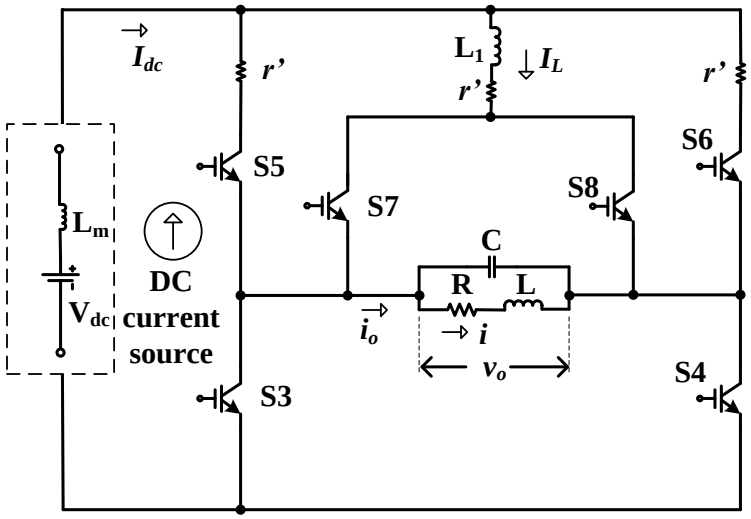


Fig.3 - 4: Single-phase five-level CSI

Table 3 - 1: Switching combinations of the single-phase five-level CSI

Output current	Possible switching combinations	
0	S4/S6/S8	S3/S5/S7
$+\frac{1}{2}I_{dc}$	S4/S5/S8	S4/S6/S7
$+I_{dc}$	S4/S5/S7	-
$-\frac{1}{2}I_{dc}$	S3/S6/S7	S3/S5/S8
$-I_{dc}$	S3/S6/S8	-

By previously discussed POD-PWM strategy, CSI switching combinations resulted from continuous comparators comparisons in Fig.3-2 is presented in Table 3-2. The positive modulation signal defines switching combinations that produce positive output currents whereas the negative modulation signal defines switching combinations for the negative currents. The defined switch combinations are processed from the comparator outputs using simple logic coding to create the switch gate signals.

Table 3 - 2: Switching combinations of POD-PWM

Wm	Comparator State	Switching Combinations	Output Current
$W_m > 0$	$W_m > W_{C1}$	$S_4S_5S_7$	$+ I_{dc}$
	$W_{C2} < W_m < W_{C1}$	$S_4S_5S_8$	$+1/2\ I_{dc}$
		$S_4S_6S_7$	
	$W_m < W_{C2}$	$S_4S_6S_8$	0
$W_m < 0$	$\|W_m\| < \|W_{C3}\|$	$S_3S_5S_7$	0
	$\|W_{C3}\| < \|W_m\| < \|W_{C4}\|$	$S_3S_6S_7$	$-1/2\ I_{dc}$
		$S_3S_5S_8$	
	$\|W_m\| > \|W_{C4}\|$	$S_3S_6S_8$	$- I_{dc}$

Generally, for any ideal symmetrical control of a CSI at the supply frequency of 50Hz, the steady-state output current waveform can be depicted as in Fig. 3-5 and the total harmonics distortion [42] is given by:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^{\ 2}}}{H_1} \qquad (3\text{-}1)$$

where H_1 is the amplitude of the fundamental component at frequency ω_0 and $H_{(n)}$ is the amplitudes of the nth harmonics at frequency $n\omega_0$.

By assuming that the amplitude of the fundamental and harmonic components of the waveform is quarter-wave symmetric, the output current THD of the waveform can be represented mathematically by[42]:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty}\left[\frac{1}{h}\sum_{k=1}^{n}\cos(h\alpha_k)^2\right]^2}}{\sum_{k=1}^{n}\cos(\alpha_k)} \qquad (3\text{-}2)$$

where α_k are the switching angles which must satisfy [$\alpha_1,\alpha_2,\ldots,\alpha_n < \pi/2$], *n* is the number of level defined by (2*n*+1) and *h* is the odd harmonic order.

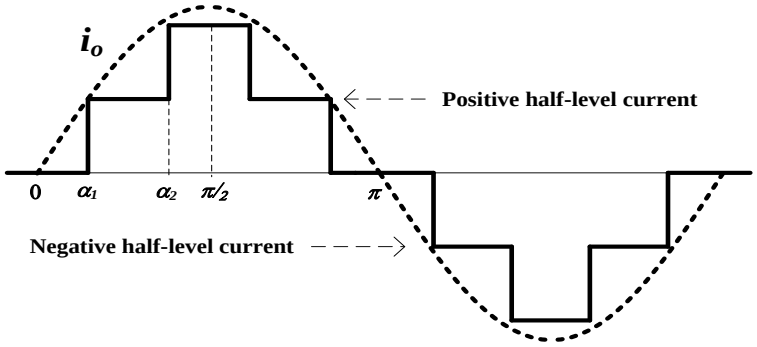


Fig.3 - 5: Quarter wave symmetrical five-level output current

Unfortunately, a ripple-free waveform as such is not possible in practice since the inductor current contains both dc and ac components as depicted in Fig. 3-6. The inductor current alternates about the half-current level; ramping up or down depending on the switching combinations at any moment. At high-load, the inductor (L_1) current ripple will cause the current to decay faster, as highlighted in Fig. 3-6. This causes the current THD to increase and degrade the inverter performance. Thus, half-level current control is critical.

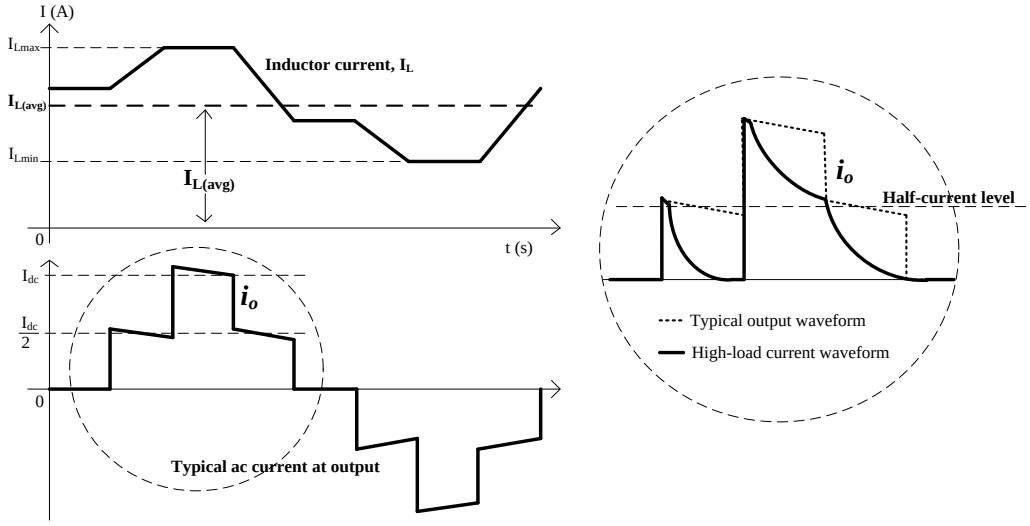
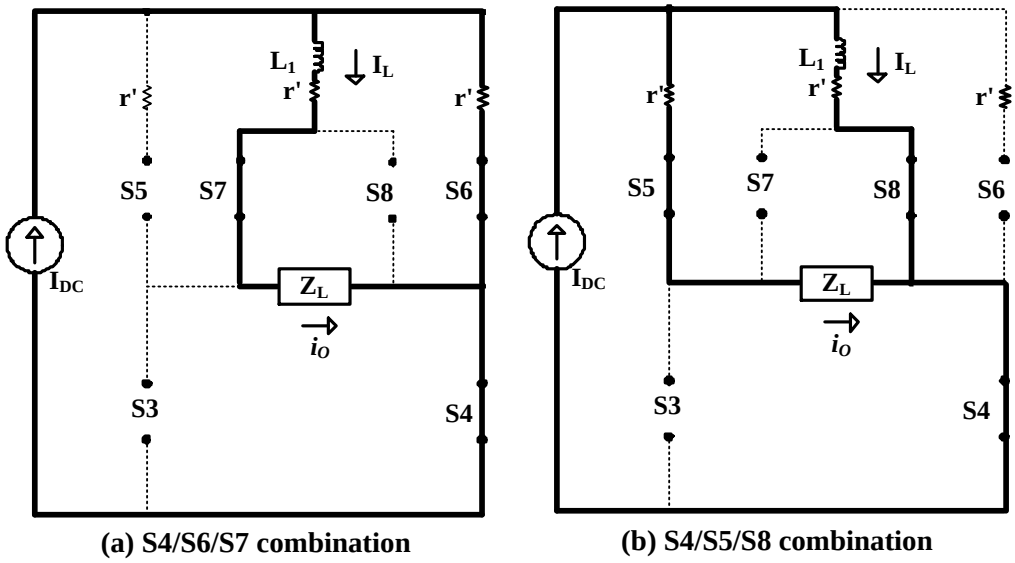


Fig.3 - 6: Typical average inductor current (top, left); the respective five-level output current waveform (bottom, left) and its comparison to the high-load current condition (as highlighted on the right).

The proposed RS-MPM control strategy is aimed at improving the intermediate-current level so that the output current waveform will regain its typical staircase shape. This can be achieved by first identifying the different switch combinations that will produce identical outputs (or redundant switch combination). Table 3-1 shows that if the current across the inductor in Fig. 3-4 is at half-level dc then the circuit has two switch combinations that will produce identical output currents through the load at steady–state. These combinations, shown in Fig. 3-7 operate as follows: In Fig. 3-7(a), when switches S4/S6/S7 are closed, the current through inductor L_1 will quickly fall since it is directly connected to the load Z_L. This will produce a ramp-down current from the half-value. On the other hand, the current through L_1 rises when switches S4/S5/S8 are closed as shown in Fig. 3-7(b). Thus, by alternately switching between these two combinations at higher frequency, the half-current level can be kept constant as shown in Fig. 3-8.



(a) S4/S6/S7 combination **(b) S4/S5/S8 combination**

Fig.3 - 7: Half-current redundant switching states

Fig.3-8 provides an explanation of the RS-MPM control technique described earlier. In this method, high-frequency (HF) switching is utilized only during certain states (half-level) while low-frequency control is retained during both full-current and zero-current states. This simplifies the control design thus reducing

the implementation cost. HF control is achieved by alternately switching the pre-determined switch combinations in Fig.3-7 at a much higher fixed frequency.

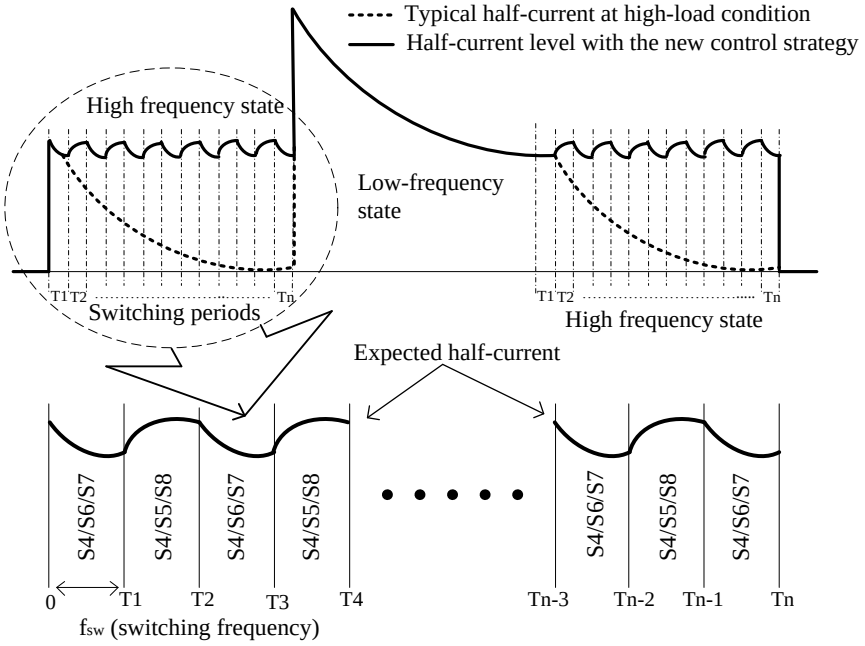


Fig.3 - 8: Proposed RS-MPM control strategy

3.3 Simulation Results

The proposed RS-MPM control method is simulated using Matlab/Simulink (SimPowerSystems) to verify the feasibility of the technique. Circuit parameters used in the simulations are as follows:

For a purely resistive load (R-load):

(Low-load): V_{dc}=25Vdc, L_m=112mH, L_1=20mH, r'=0.33Ω, and R = 5Ω.

(High-load): V_{dc}=25Vdc, L_m=112mH, L_1=20mH, r'=0.33Ω, and R = 100Ω.

For an impedance load (RLC-load):

(Low-load): V_{dc}=25Vdc, L_m=112mH, L_1=20mH, r'=0.33Ω, R = 5Ω, L=10mH, and C=150μF.

(High-load): V_{dc}=25Vdc, L_m=112mH, L_1=20mH, r'=0.33Ω, R = 100Ω, L=10mH, and C=50μF.

Fig.3-9 shows the simulated performance of the RS, PWM and RS-MPM control strategies during low-load condition together with an ideal staircase-shaped CSI output current waveform. It can be clearly seen that the proposed RS-MPM method has successfully improved the half-level current control to a nearly constant dc value. Fig.3-10 shows circuit current waveforms with an RLC load, where waveforms $\mathbf{i_o}$ shows the unfiltered switched current feeding into the load, while waveforms **i** shows the load current after filtration (refer to Fig.3-4). It can be seen that with the RS-MPM method, the filtered output current is sinusoidal as anticipated, with minimal distortion.

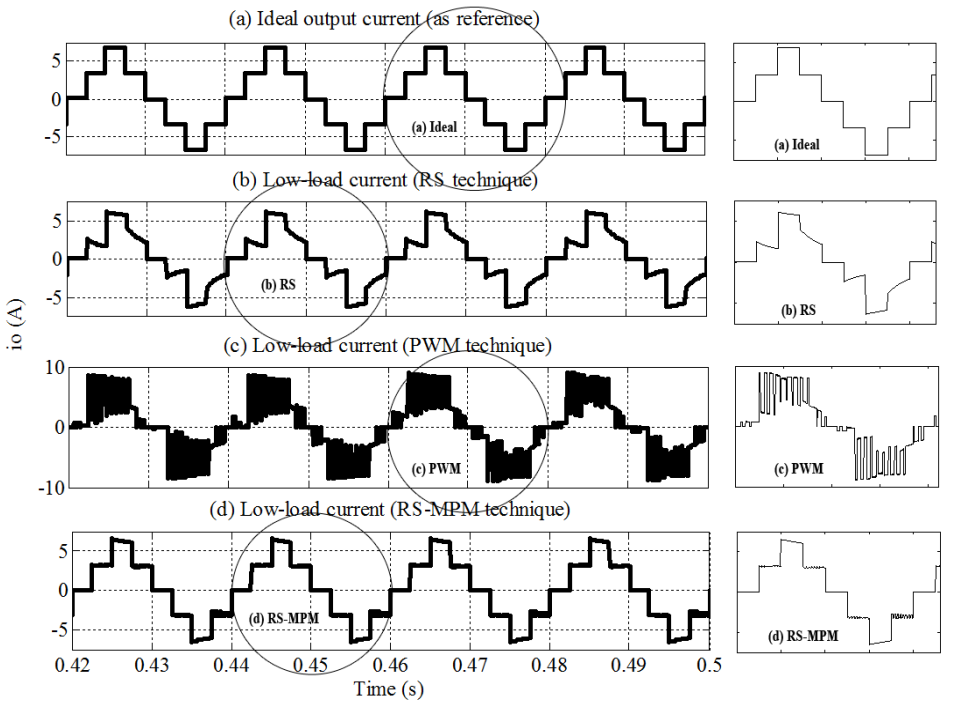


Fig.3 - 9: Simulated output current waveforms; low resistive load (from the top: ideal, RS, PWM and RS-MPM)

Since RS-MPM control is aimed to improve the intermediate-current level of a multilevel CSI, it is essential to investigate the circuit operation at high-load conditions when this level is at its worst profile. From Fig.3-11, it can be seen that while both RS and PWM control techniques are unable to maintain the staircase-

shaped of the load current at high-load condition, the RS-MPM technique shows better control of the half-current level whilst preserving the multilevel shape. Fig.3-12 shows the current waveforms, $\mathbf{i_o}$ and **i** at high RLC load; where the filtered output current is closer to sinusoidal with RS-MPM control but not so with RS or PWM control. Simulation results show that the RS-MPM control performance is superior to any of the other control techniques investigated; where the intermediate current level before filtering is nearly constant around an average dc value and minimal distortion is achieved after the waveform is filtered. The proposed control strategy improves the output load-current waveform and the associated current THD at both low- and high-load conditions as summarized in Table 3-3.

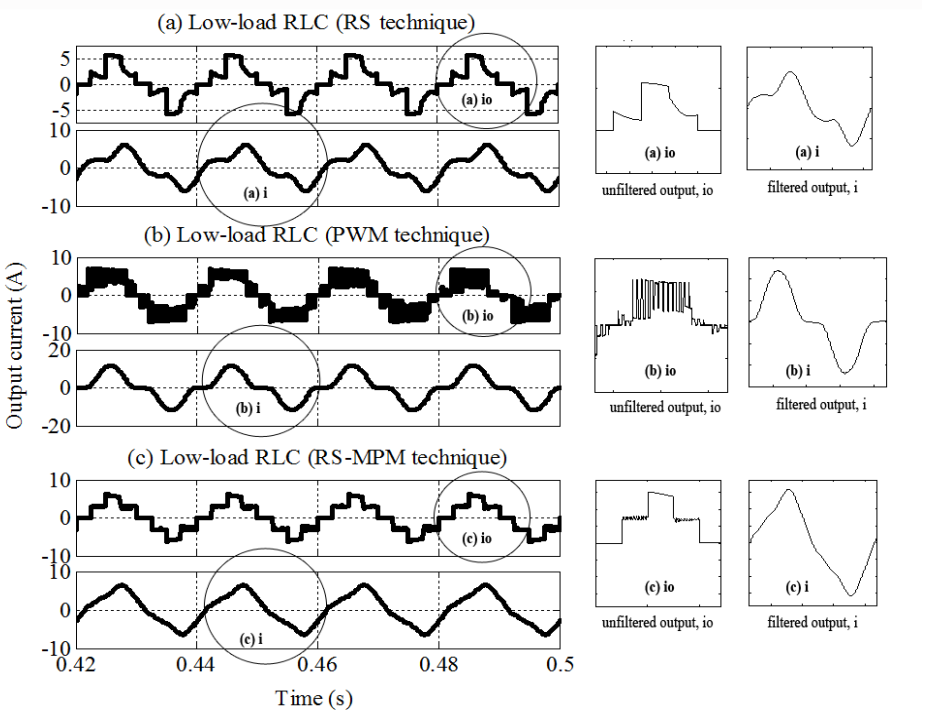


*Fig.3 - 10: Simulated output current waveforms (**i_o** & **i**); low RLC load*

(a)) i_o & i - load current using RS technique

(b) i_o & i - load current using PWM technique

(c) i_o & i - load current using RS-MPM technique

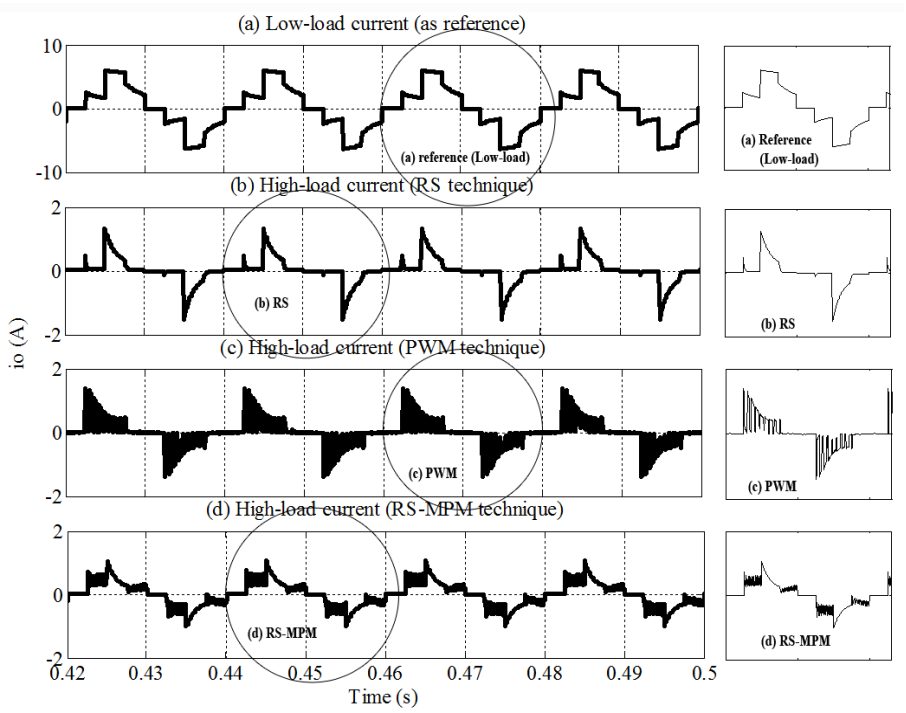


Fig.3 - 11: Simulated output current waveforms; high resistive load (from the top: low-load current for reference, RS, PWM and RS-MPM)

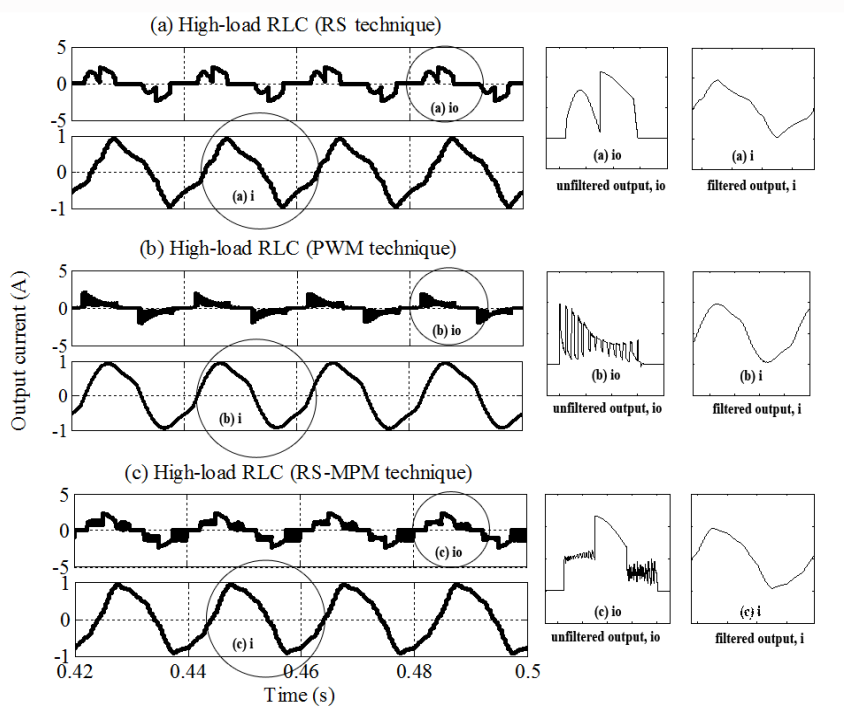


Fig.3 - 12: Simulated output current waveforms ($\boldsymbol{i_o}$ & $\boldsymbol{i}$); high RLC load

(a) i_o & i - load current using RS technique

(b) i_o & i - load current using PWM technique

(c) i_o & i - load current using RS-PWM technique

Table 3 - 3: Current THD comparison by methods of control

Control Method	Parameter / Condition	THD (%)		
		Resistive	Inductive	
		i_o (unfiltered)	i_o (unfiltered)	I (filtered)
Calculated/RS	Ideal condition	28.97	29.24	7.51
	Low-load condition	(R=15 Ω)	(R=15 Ω; L=10 mH; C=150 uF)	
RS		36.37	44.88	19.23
PWM		44.75	33.74	27.05
RS-MPM		29.28	29.89	8.44
	High-load condition	(R=250 Ω)	(R=250 Ω; L=10 mH; C=50 uF)	
RS		95.54	57.92	18.00
PWM		98.31	66.58	11.75
RS-MPM		45.68	43.80	11.15

Initially, by using equation (3-2) the THD of the ideal current waveforms in Fig.3-5 are calculated. Since infinite harmonics is not possible, by common practice, replacing (∞ = 63) is reasonably sufficient [42]. By substituting the angles (α_1 = 22.5 degree) and (α_2 = 67.5 degree), the calculated output current THD of five-level waveform is 28.97 %. The waveforms in Fig.3-5 are also simulated in Matlab/Simulink using redundant switching (RS) technique for verification. These values are used in Table 3-3 as the main references for the THD in ideal condition. It can be seen that although RS-MPM is designed especially to deal with high-load condition, its recorded THDs excel for both high- and low-load conditions; either unfiltered or filtered. Furthermore, the filtered THD for low-load condition for example, is much closer to the ideal value.

3.4 Laboratoty investigation

To demonstrate the validity of RS-MPM control, a 25 V, 10 A laboratory prototype for a five-level single-phase CSI system (as shown in Fig.3-4) has been constructed. The insulated gate bipolar transistors (IGBT) IRGB30B60K are used for the active switches; controlled by the FPGA based digital control system Xilinx Spartan-3A DSP 1800A. The experimental set-up test parameters were as follows:

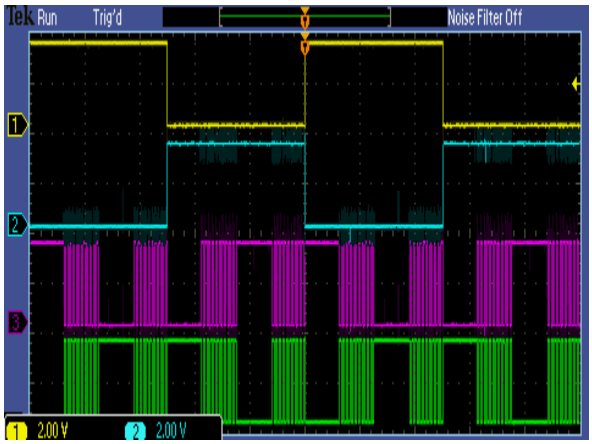
For a typical (low-load condition) resistive:

- V_{dc}=25Vdc, L_m=112mH, L_1=20mH, r'=0.33Ω, and R = 5Ω.

For high-load conditions (resistive load):

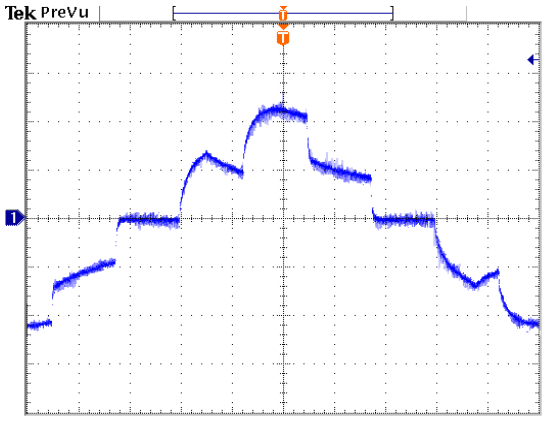
- V_{dc}=25Vdc, L_m=112mH, L_1=20mH, r'=0.33Ω, R = 100Ω.

The waveforms obtained from the laboratory prototype are captured in Fig.3-14, Fig.3-15 and Fig.3-16; whereas part of the gate signals used to drive IGBTs are as illustrated in Fig.3-13. These gate signals are generated using FPGA controller that produces predetermined gate sequences combination of low and high switching frequencies. Fig.3-14 is the typical five-level low-load output current waveform obtained by RS control method similar to the simulation waveform in Fig.3-9(b). Fig.3-15 on the other hand is typical five-level high-load output current waveforms also by RS control method similar to the simulation waveform in Fig.3-11(b) where distorted output current waveform can be seen. The smaller the inductor current, the faster it depreciates to zero. This condition is detrimental in MCSI since the inductor current balance is not achieved and this could spark inverter failure. The distorted waveform however is successfully improved by employing the proposed RS-MPM control as illustrated in Fig.3-16. It can be seen that the intermediate current level is maintained at about the half-level which is vital in order to ensure the continuous flow of the inductor current. The close agreement of the simulation and the experimental results confirm the validity of the proposed control strategy.



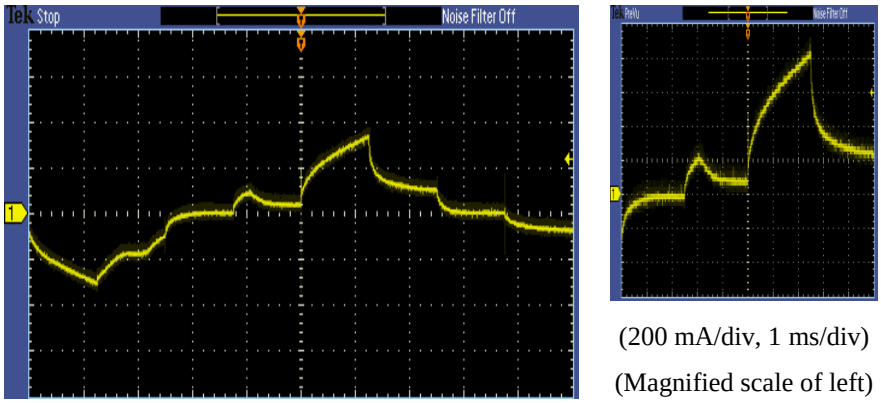
(2 V/div; 4 ms/div)

Fig.3 - 13: FPGA gate signals of (top to bottom: S3, S4, S5, and S6)



(2 A/div; 2 ms/div)

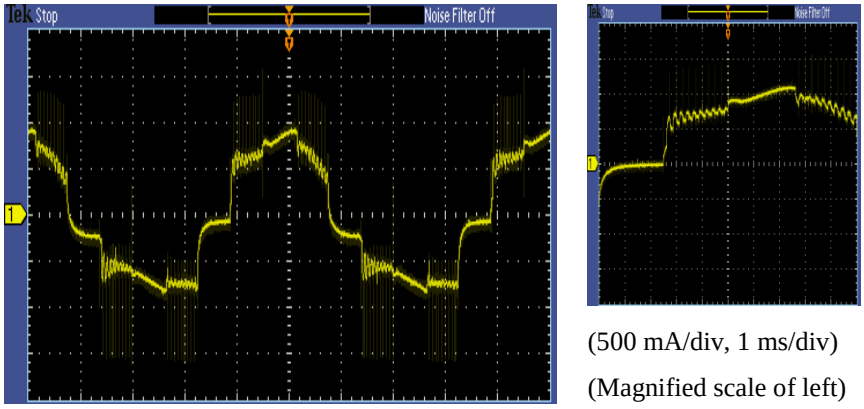
Fig.3 - 14: Typical experimental five-level output current at low-load (with RS technique)



(500 mA/div; 2 ms/div)

(200 mA/div, 1 ms/div)
(Magnified scale of left)

Fig.3 - 15: Five-level output current at high-load condition (with RS technique)



(500 mA/div; 4 ms/div)

(500 mA/div, 1 ms/div)
(Magnified scale of left)

Fig.3 - 16: Improved output current at high-load condition (with RS-MPM)

In conclusion, the proposed modified control technique, referred to as RS-MPM has successfully improved the output current waveform of multilevel current source inverters operating at various load conditions. This was achieved by combining simple RS control with PWM control strategies to reduce the current THD levels. The proposed method has been shown to have the potential to be a low-cost yet efficient control technique. Although analysed for one single

multilevel CSI topology, the RS-MPM control can also be implemented in other CSI topologies with redundant switch combinations.

3.5 Summary

The design of MCSI is greatly dependent on the control strategy employed within the converter. Currently these converters are either controlled by LFM or PWM control strategies; however neither of these methods have been practically experimented for high-load condition nor explicitly discussed. This chapter describes an enhanced control technique to improve the output current quality of a multilevel current-source inverter operating especially at high-load condition. The new technique, named here as RS-MPM, combines the simple control of redundant-switching methods with more flexible PWM methods and has been shown in this study to be superior to both. The results have been validated by laboratory experiments using a 250 VA test circuit.

CHAPTER 4

Novel Multilevel Current Source Inverter Topology

In Chapter 3, it was shown that the MCSI design is greatly dependent on the control strategy employed within the converter in order to achieve not only stable converter operation but also reduced current harmonics at the output. In the existing MCSI topologies however, though theoretically doable; if the expected current level is above five-level, the control system required will be nearly too complex to achieve. This is due to (1) the increasing number of power switches indicates increased switching sequence redundancies which resulted in nearly impossible means to discover the workable switching sequence arrangement without involving any intelligent tools or control technique and (2) the increasing number of the DC inductors, where the currents through them must be managed individually to the approximately constant currents at the specific level or amplitudes. In this chapter, a novel generalized multilevel CSI topology has been proposed which significantly reduces the number of crucial elements such as the power switches and inductors and demonstrates a modest control system. The new converter topology, its principle of operation, as well as simulation results are presented and discussed in this chapter.

4.1 Novel Generalized MCSI Topology

The key component that distinguish the new topology from the existing topologies is the employment of bidirectional switches, which has helped to reduce the number of total components employed within the structure. As illustrated in Fig.4-1, the bidirectional switch can be set up in two different arrangements; (a) either as a single power switch that connects to four diodes or (b) two power switches that are connected in parallel. The advantage of (a) is that a single power switch is used, thus saving on control complexity hence cost. However, with additional four power rectifier utilized within the circuit as pictured in Fig.4-1(a), the number of overall components employed increases which may be misleadingly reflected on the total cost increment. On the contrary, in (b) , two power switches are connected in parallel as pictured in Fig.4-1(b). Therefore, lesser overall components are used; however, the control complexity increases with the additional of a gate signal.

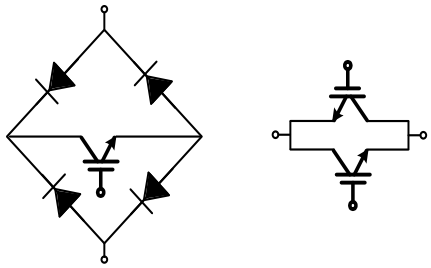


Fig.4 - 1: (a) 1-IGBT with 4-diodes (b) 2-IGBTs in parallel

The novel topology proposed is illustrated in its generalized form in Fig.4-2. It can be seen that the proposed topology is from the single-stage group of multilevel inverter since it employs a single current-source and built in a single integrated structure. Besides the bidirectional switches, another key component of the topology is the employment of the inductor L0 in parallel to the outer power switches. This inductor can be perceived as a all-time constant half-current source which supplied the needed currents for the succeding inductors at a fraction of the supplied amplitude. Since in typical MCSI, all inductors are constant current source with specific amplitude similar to capacitors role in MVSI,

therefore accumulating for particular current stages can simply be explained mathematically i.e. adding more inductor currents to increase the stage current or taking away inductor currents to decrease the stage current. The events of adding and taking away currents are benefited from the employement of the bidirectional switch. Also, the bidirectional switch is there to ensure that all currents through the inductors are continuously flowing.

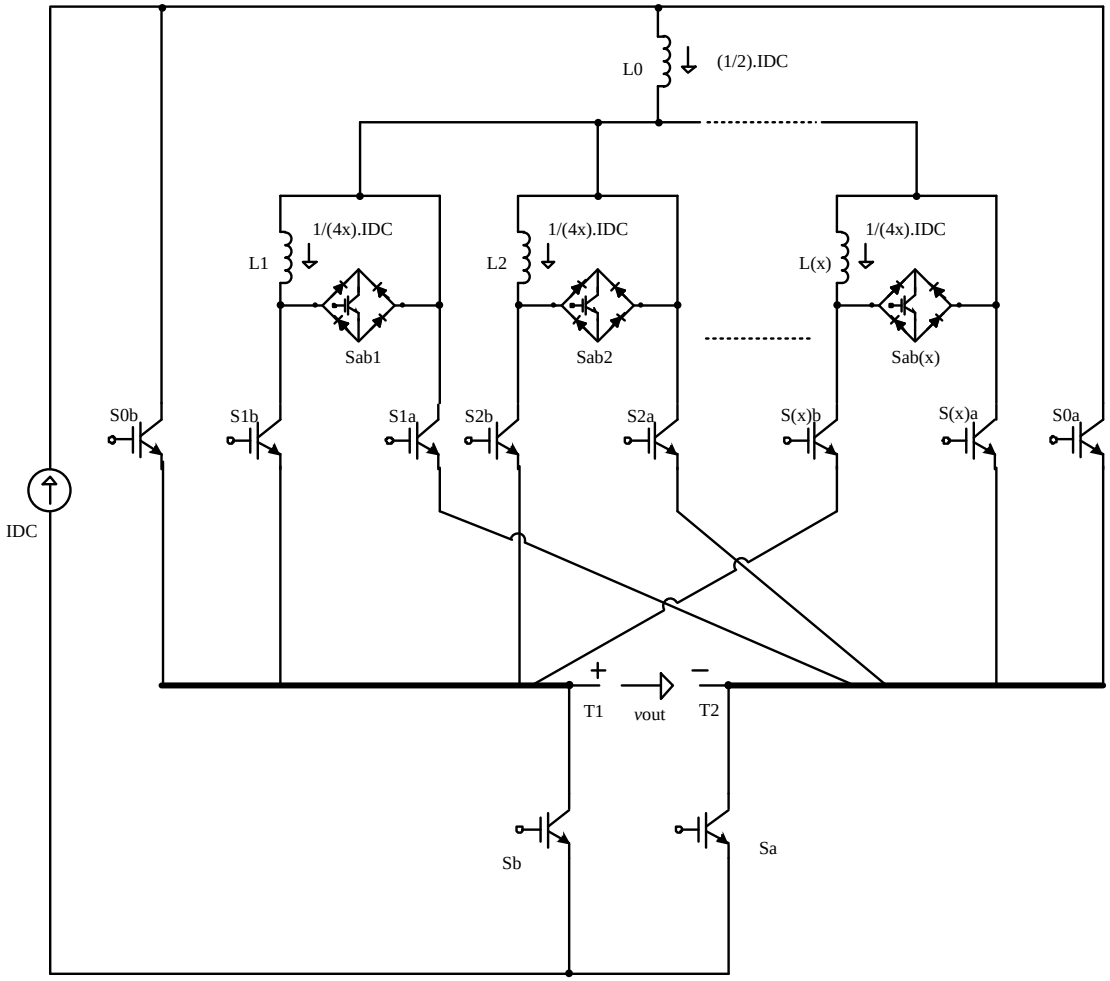


Fig.4 - 2: The proposed novel generalized topology

Fig.4-3(a) and (b) illustrate the new proposed five-level and nine-level CSI respectively based on the novel generalized MCSI in Fig.4-2. It can be seen in Fig.4-3 (a), that there are only five power switches, one inductor and four diodes employed, which has

effectively made the new proposed five-level CSI the most simplest topology by far. By adding two additional switches to the outer ring of the five-level CSI as shown in Fig.4-3(b), the present circuit is now able to produce up to nine levels of the output currents. This topology (Fig.4-3(b)) has reduced a significant amount of components compared to existing topologies. Table 4-1 summarizes the total number of components employed in four existing topologies compared to the novel topology for up to seventeen levels. It can be seen that for the five-, nine- and seventeen-level CSI, the novel topology employed the least number of fundamental components (inductor and power switches) in both arrangements and the higher the level, the advantages are more significant. It can also be noted that, except for Topology IV, all other topologies increase their level by (***n***+2); whereas for Topology IV the level increment is (***n***+4). However, for the proposed topology the increment is (2***n***-1) where ***n*** is the current inverter level. These differences are shown in Table 4-1.

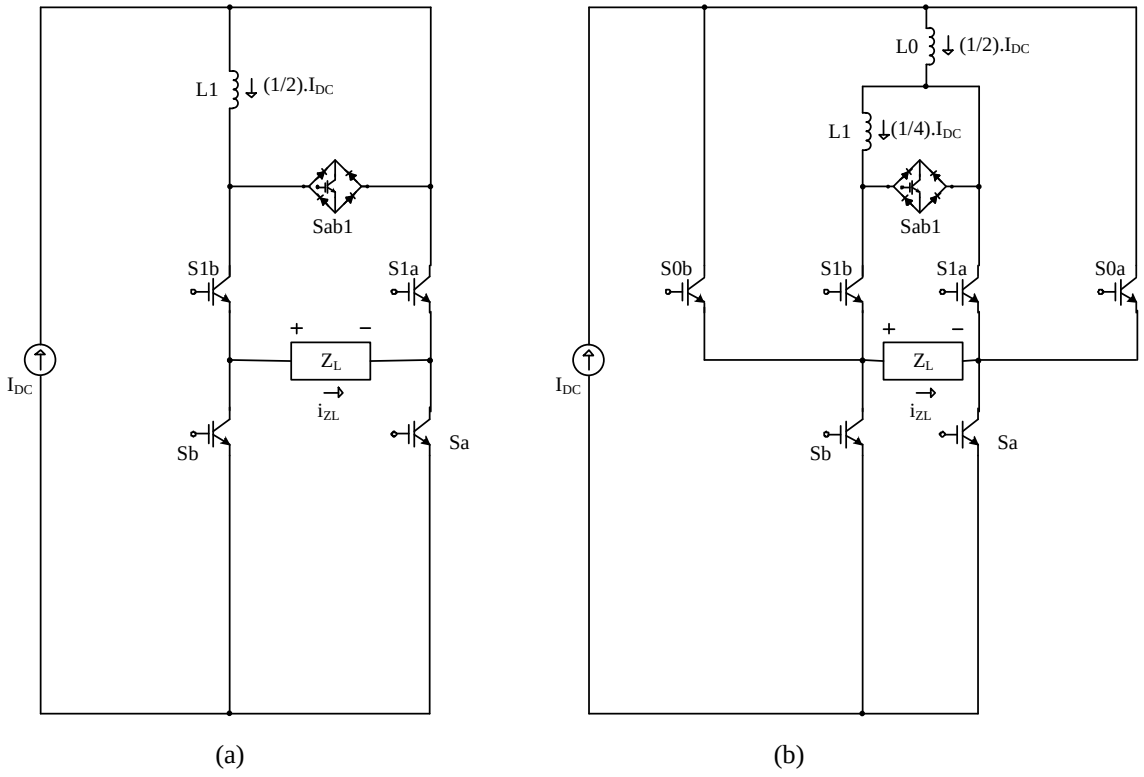


Fig.4 - 3: (a) The novel 5-level CSI (b) The novel 9-level CSI

Table 4 - 1: Comparison of number of components

Current level	Topology / Component	Topo I	Topo II	Topo III	Topo IV	NOVEL Topo	
						1-sw with diode	2-sw in parallel
5-level	Inductor	2	1	1	1	1	1
	Switch	8	6	8	8	5	6
	Diode	0	0	0	0	4	0
Total no. of component:		10	7	9	9	10/(6)*	7
7-level	Inductor	4	2	2			
	Switch	12	8	10			
	Diode	0	0	0			
Total no. of component:		16	10	12			
9-level	Inductor	6	3	3	2	2	2
	Switch	16	10	12	12	7	8
	Diode	0	0	0	0	4	0
Total no. of component:		22	13	15	14	13/(9)*	10
11-level	Inductor	8	4	4			
	Switch	20	12	14			
	Diode	0	0	0			
Total no. of component:		28	16	18			
13-level	Inductor	10	5	5	3		
	Switch	24	14	16	16		
	Diode	0	0	0	0		
Total no. of component:		34	19	21	19		
15-level	Inductor	12	6	6			
	Switch	28	16	18			
	Diode	0	0	0			
Total no. of component:		40	22	24			
17-level	Inductor	14	7	7	4	3	3
	Switch	32	18	20	20	10	12
	Diode	0	0	0	0	8	0
Total no. of component:		46	25	27	24	21/(13)*	15

*The numbers in brackets are to exclude diodes

4.2 Operation of MCSI

To achieve a successful operation of the multilevel inverter, it is mandatory to determine the accurate switch combinations and sequences, besides fulfilling other requirements

such as zero average voltage accumulated across inductors and minimized inductor current ripple. This set of requirements will ensure continuous and balance inductor current for every circuit branches, thus, constant current sources provided. In the next sections, the operational analysis of the proposed topology will be discussed in details for the five- and nine-level inverters.

4.2.1 Five-Level MCSI

The five-level inverter in Fig.4-3(a), similar to topologies discussed in Chapter 2, consists of eight variable states that are made of zero-current, half-current, and full-current states of both polarities. The pre-determine switch combinations and the correct switching sequence in order to obtain the output current, i_o are as illustrated in Fig.4-4. In order to demonstrate the typical operation of the proposed inverter, the load current (i_{ZL}) paths for every states are exaggerated as illustrated in Fig. 4-5 where the combined sequences of these paths make up for the output current, i_o. In state (1), four switches S1a/S1b/Sa/Sb are closed therefore no current is flowing through the load (Fig.4-5(a)). In states (2), while switches S1a/S1b/Sa are still closed, switch Sb is opened forcing the half-current (I/2) to flow through the load (Fig.4-5(b)). The positive full current in state (3) is achieved whenever switch S1a is opened and at the same time the bidirectional switch Sab1 is closed therefore providing path for half-current (I/2) to add-up with another half-current (I/2) before flowing through the load with the full-current amplitude (Fig.4-5(c)). It can be observed that the bidirectional switch, Sab1 provides the path for the second-half of the current in order to build up the full-current at the load point. Similarly, the reverse current polarity can be obtained simply by toggling the returned current path to Sb as illustrated in Fig.4-5(d) and Fig.4-5(e). It can also be seen that, with the bidirectional switch in place, the current through the inductor, L_1 is uninterrupted; thus fulfilling the requirement for continuous current flow through inductors and avoiding peak voltages across switches during turn-off period. However, for a successful operation, it is important to understand that the action of switch combinations and sequence must be continuous and repetitive in order to achieve steady state current output.

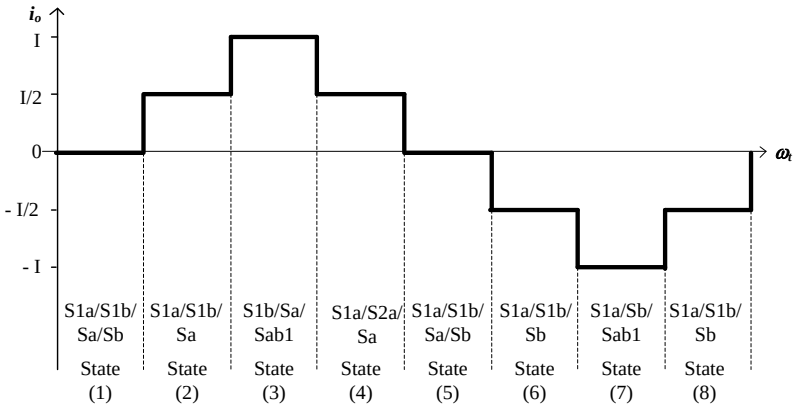


Fig.4 - 4: Five-level CSI switching sequence

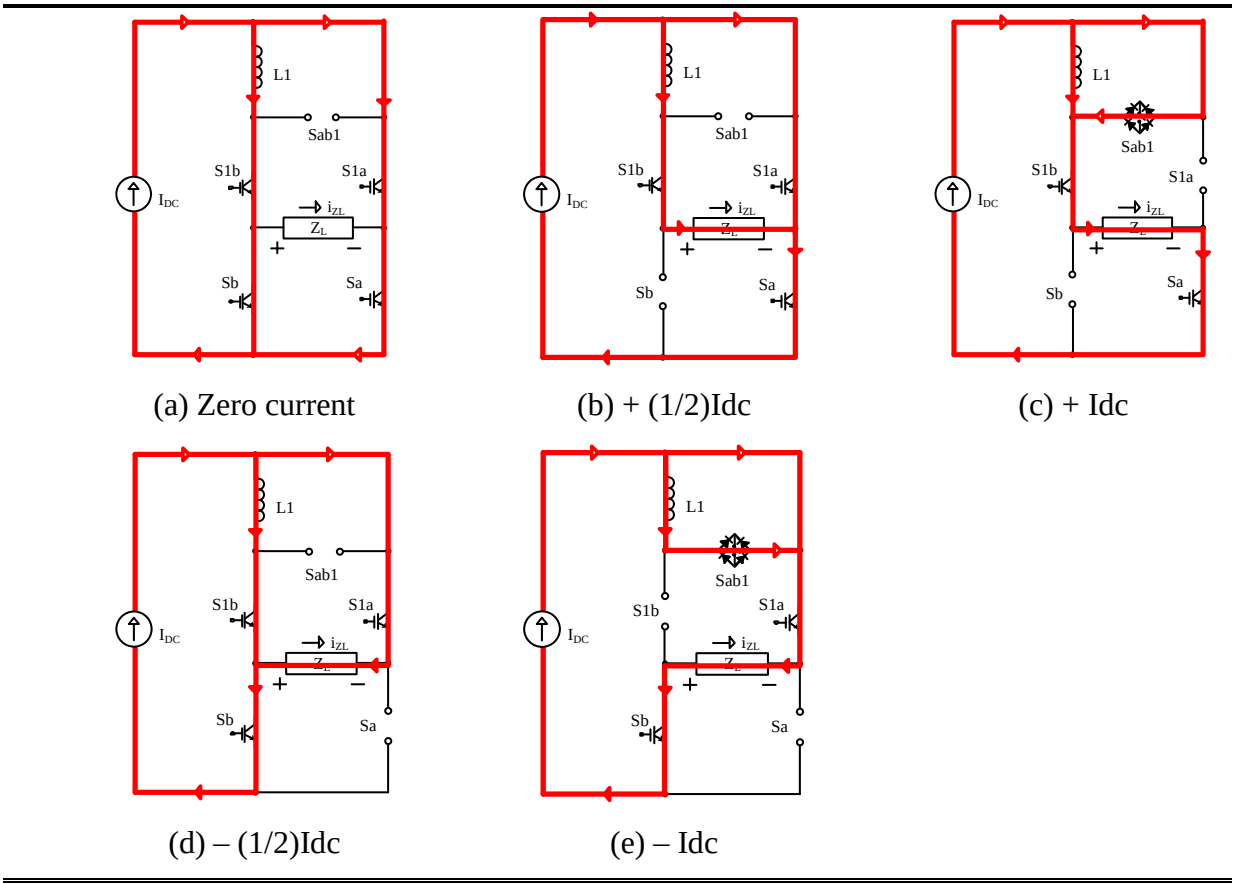


Fig.4 - 5: Load current path of the five-level CSI

4.2.2 Nine-Level MCSI

Essentially, for the nine-level inverter in Fig.4-3(b), sixteen variable states are required to construct a nine-level stepped current waveform as illustrated in Fig.4-6. The pre-determined switch combinations and appropriate switch sequence for the proposed topology is also given in Fig.4-6. When comparing this inverter to other existing topologies, finding the correct switch combinations and sequence is very straightforward due to lacking of switch redundancies i.e. the total switch combinations is 16 compares to Topology I with 256 combinations [10]. Unlike other nine-level inverters, which typically have few possible switch combinations for the half-current (I/2) and quarter-current (I/4) outputs to be selected precisely; thus switch redundancy, this novel inverter makes use of only a single switch combination for the half-current (I/2) and quarter-current (I/4) outputs in its operation. The two inductors, firstly L0 can be perceived as a constant half-current (I/2) source whereas the second inductor, L1 is the constant quarter-current (I/4) source. These two current sources can be mathematically added up to generate higher output current levels i.e. the three-quarter current (3I/4) and full-current (4I/4 or I) in such a way identical to the technique used to sum the voltage in flying-capacitor inverter circuit [6, 32, 92]. To better appreciate the basic operation of the novel nine-level inverter, its pre-determined switch combinations and the associated path currents are artistically exaggerated in Fig.4-7.

In state (1), four switches (Sa/S0a/S1a/Sab1) are closed therefore all current bypassing the load therefore generating zero current across the load (Fig.4-7(a)). In state (2), while switches (Sa/S0a/S1a) are still closed, the bidirectional switch , Sab1 is opened allowing the quarter-current (I/4) to flow through the load via the switch S1b (Fig.4-7(b)). In order to generate the positive half-current (I/2) in state (3), as depicted by Fig.4-7(c), the bidirectional switch , Sab1 again is closed together with switches (Sa/S0a/S1b) allowing the quarter-current to add-up before flowing through the load. Then in state (4), for the three-quarter (3I/4) current, the bidirectional switch, Sab1 is again opened while at the same time switches (Sa/S1a/S1b/S0b) are closed; allowing the half-current and quarter-current to add-up generating the positive three-quarter (3I/4) current amplitude (Fig.4-

7(d)). Finally, the positive full current in state (5) is achieved whenever the combination of switches (Sa/S1b/S0b) together with the bidirectional switch, Sab1 is used therefore providing path for the quarter-currents and half-current to add-up before flowing through the load with the full-current (I) amplitude as illustrated in Fig.4-7(e). It can be observed that the bidirectional switch, Sab1 is the key component which provides the path for currents in smaller amplitudes to add-up generating a higher-current amplitude as discussed earlier. Therefore allowing step-current waveform to be created at the load point. Similarly, the reverse current polarity can be obtained simply by toggling the returned current path to Sb as depicted in Fig.4-7(f-i). It can also be seen that, with the bidirectional switch in place, the current through the inductors, L_0 and L_1 are uninterrupted; thus fulfilling the requirement for continuous current flow through inductors and avoiding peak voltages across switches during turn-off period. Again, it is important to reiterate that the action of switch combinations and sequence as discussed above must be continuous and repetitive in order to achieve steady state current output.

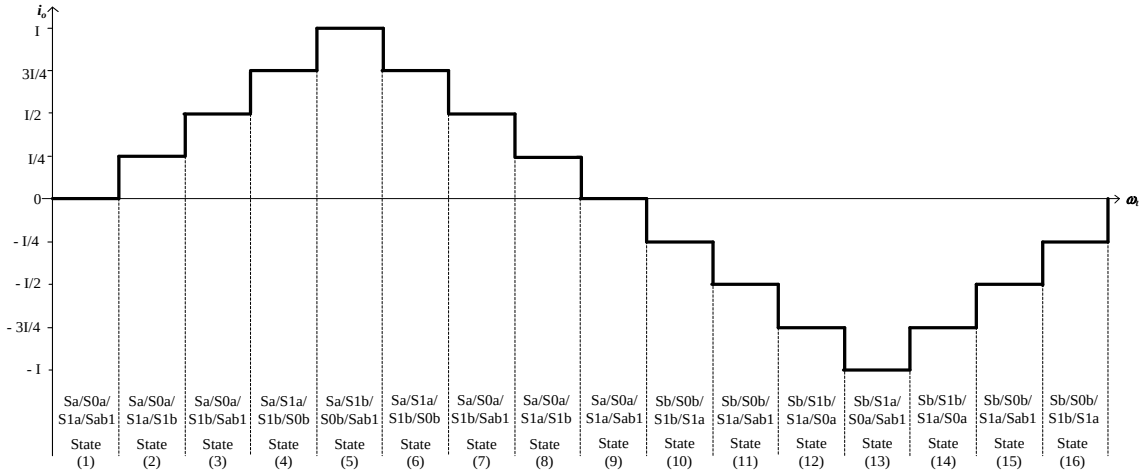


Fig.4 - 6: Nine-level CSI switching sequence

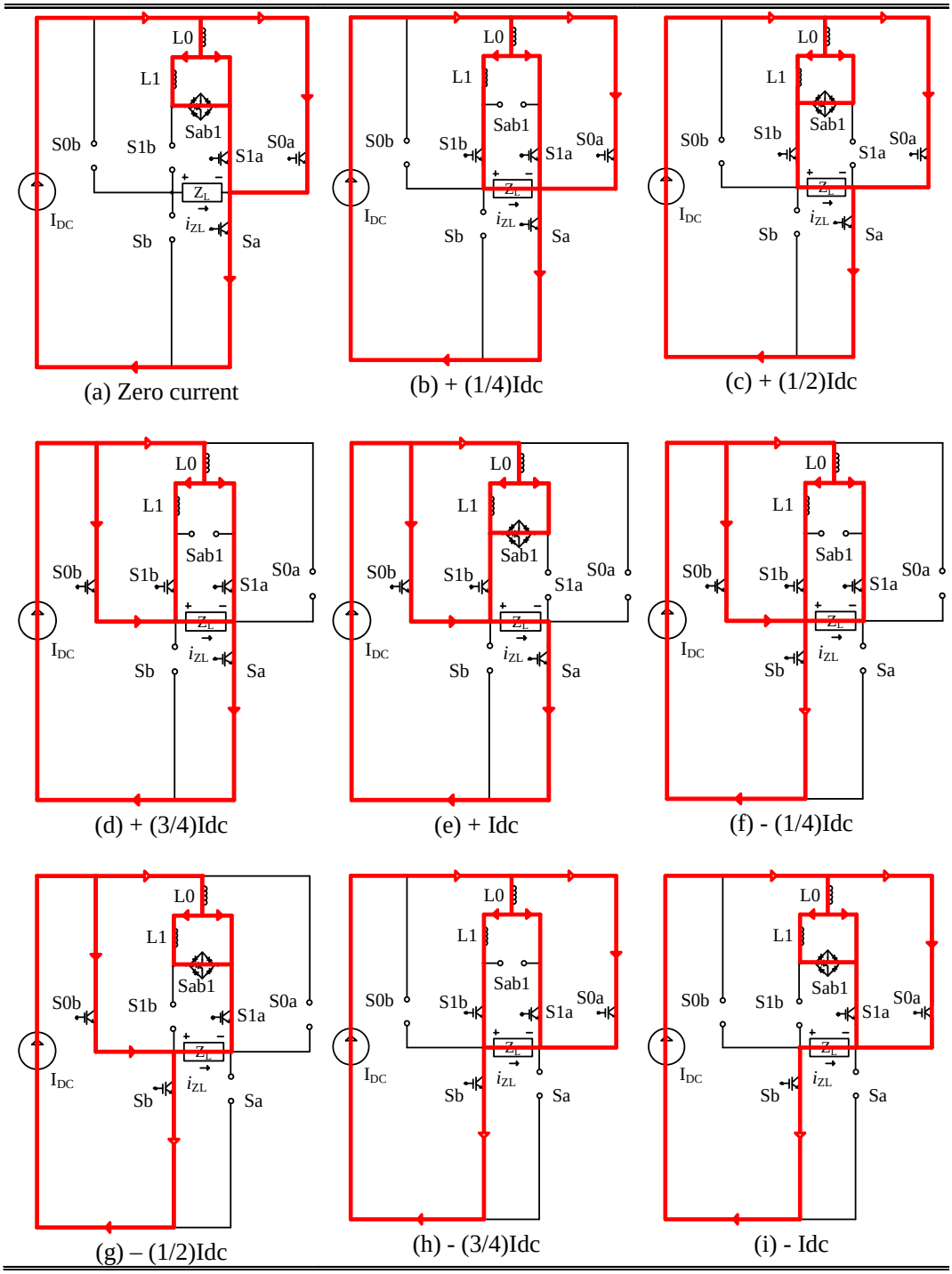


Fig.4 - 7: Load current path of the nine-level CSI

4.3 Computer Simulations

Theoretically, the proposed topology has the advantages of low utilization of power switches; thus, decrease control complexity. In this section, the inverter is modelled in Matlab/Simulink using SimPowerSystems blockset for initial verification. The models, as shown in Fig.4-8 and Fig.4-9 are for the five-level and the nine-level inverter respectively, comprises of IGBT as the main switches, inductors, resistors and also capacitors. The constant dc current source is a build-up of a dc voltage source (Vdc) and a large inductor (Lm) with internal resistance (r'_{Lm}). In order to have current equally distributed among the branches and to avoid current short circuit in the branches without inductor, internal resistances (r'_1 and $r'_{2)}$ are added whose values are equal to the inductor's internal resistance. This practise has been an acceptable solution in order to balance the inductors in MCSI and has also occurred in previously discussed topologies. Although the application of this internal resistances will cause a small decrease of the converter efficiency; however, the effect is minimal compares to when an equivalent inductor is used to balance these branches. The internal resistance values, as given in Table 4-2 and Table 4-3 must be higher than the IGBT's 'on' resistance for proper operation of the inverters. Based on the datasheet of the employed IGBT switches as in the next chapter, the 'on' resistance stated is 0.12 Ω, which is smaller than the internal resistance of a 20 mH inductor at 0.36 Ω and 40 mH inductor at 0.72 Ω.

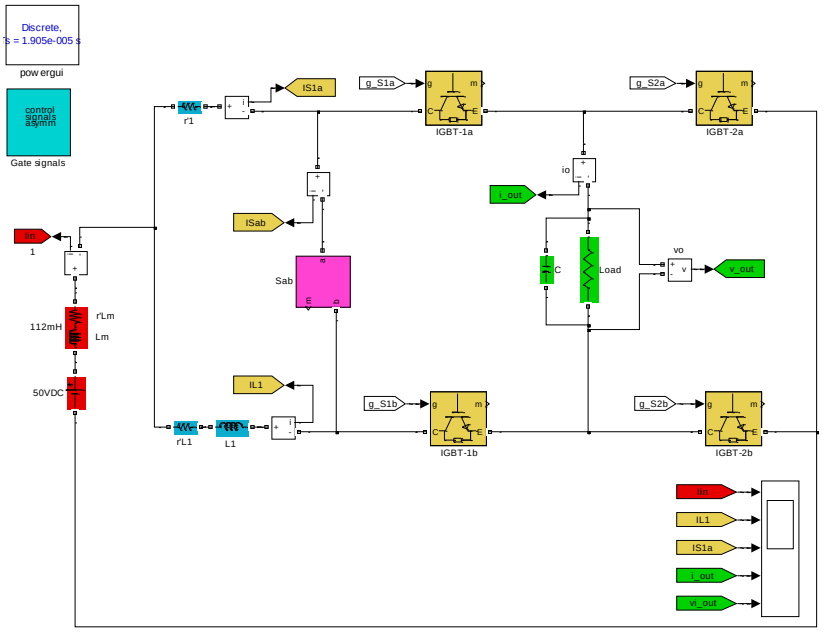


Fig.4 - 8: Matlab/Simulink model of the novel five-level CSI

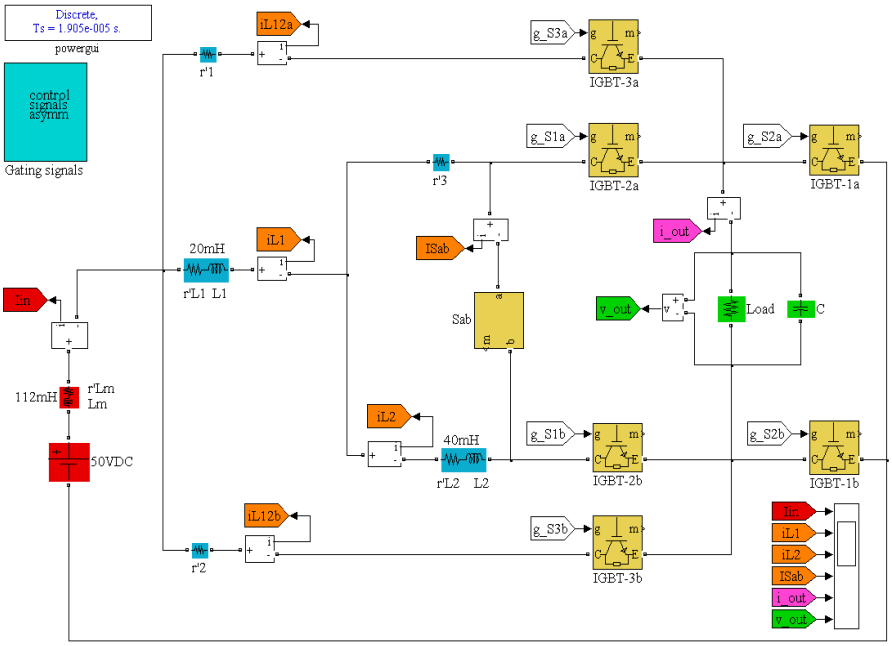


Fig.4 - 9: Matlab/Simulink model of the novel nine-level CSI

Controlling IGBT switches in a CSI unlike typical VSI requires special adaptation. In CSI, switch dead-time [93, 94] cannot be tolerated since the current

must always be continuous to avoid voltage peak damaging the switches. This circumstance is critical where two complementary switches must be turned on simultaneously forming a period called switch over-lapping. Fig.4-10 highlighted an example of the overlapping situation where the power switches conduction periods are over-lapped as much as 3-us to ensure continuous current flow. The figure illustrates an example of the gating signal-block for a five-level inverter that was developed with reference to a 50 Hz sine wave generator; comprising of eight states per period, the signal-block outputs pre-determined gating signals required to drive the power switches of the inverter. The logic signals generation method via Simulink is explained in reasonable details in Appendix A.

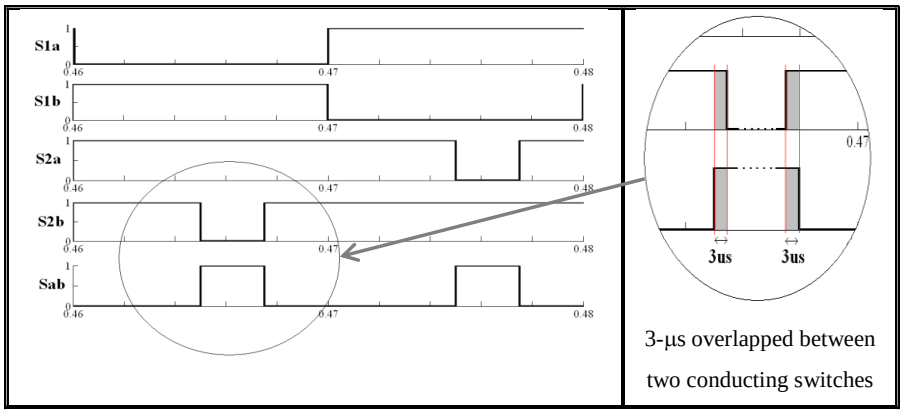


Fig.4 - 10: Five-level CSI gate signals with overlapping periods highlighted

4.3.1 Harmonic Minimization

Regardless of the switching strategy, the fundamental issue for a MCSI is to control the output current either the magnitude or harmonic. For this purpose, the appropriate values of the switching angles are to be determined so that the inverter produces the required fundamental current and does not generate specific low order harmonics. These angles can be computed numerically by solving simultaneous nonlinear and transcendental equations such as equations (2-11) and (2-12) which correspond to the fundamental and odd harmonic components for the specific harmonic order elimination. As previously stated in Chapter 2.2,

although it is beyond the scope of this thesis to prove successful harmonic elimination method e.g. SHE method; nevertheless, it is in the interest of the thesis to demonstrate that the low order harmonics and the THD of the MCSI output current waveform can be improved with switching angles manipulation. Using the angles in Table 2-1 as the references, numerous simulations using Matlab/Simulink were run by trial-and-error in order to determine the appropriate switching angles that would provide improved THD reading. These angles then applied in both simulations and experiments for the variable angles (asymmetrical) current waveforms. In this thesis, two MCSI waveforms of interest are the 5-level and the 9-level current outputs. While the 5-level waveform are triggered by two firing angles (θ_1; θ_2), the 9-level waveform are triggered by four firing angles (θ_1; θ_2; θ_3; θ_4).

4.3.2 Novel five-level CSI

For the five-level novel inverter, the simulation parameters are summarized in Table 4-2. In this investigation, Matlab/Simulink simulations are run in two setups;

1) with equal angles; (θ_1=θ_2=45°) where all states have equal lengths in one period;
2) with variable angles; (θ_1=15.5°; θ_2=38.5°) where all states have variable lengths in one period.

Table 4 - 2: Simulation set of parameters 1

Parameter	Label	Value	Unit
Rated power	-	1	kW
Inductor	L1	40	mH
Internal resistor	r'_1	0.68	Ω
Capacitor	C	100	uF
Output Freq	-	50	Hz
Load	R_{load}	6	Ω

The simulated performance of the five-level inverter, driven by ($\theta_1=\theta_2=45°$) is shown in Fig.4-11. The figure shows the waveforms for the input current, inductor current (intermediate current), unfiltered output current and also the filtered output. It can be seen in Fig.4-11(b) that the inductor current is averaged around half (I/2) of the input current with some ripples which verifies the feasibility of the topology. The total harmonic distortion before filtering is recorded high at 35.12 %, nevertheless, after filtering the index is much smaller at 16.31 %. The figures also highlighted some details of the recorded waveforms.

In the second set-up, with variable angles of ($\theta_1=15.5°$; $\theta_2=38.5°$), the inverter exhibits much improved performance in many ways. Firstly, as can be seen in Fig.4-12, smaller current ripple can be seen for the intermediate current (inductor current) compares to the previous set-up. This also reflects better current balance occurs in the power switches. Secondly, the output current harmonic as recorded is much smaller in both before and after filtering at 21.37 % and 8.43 % respectively. This verifies that the THD of a current waveform can be improved with certain selected angles. The waveform details are highlighted in the figure.

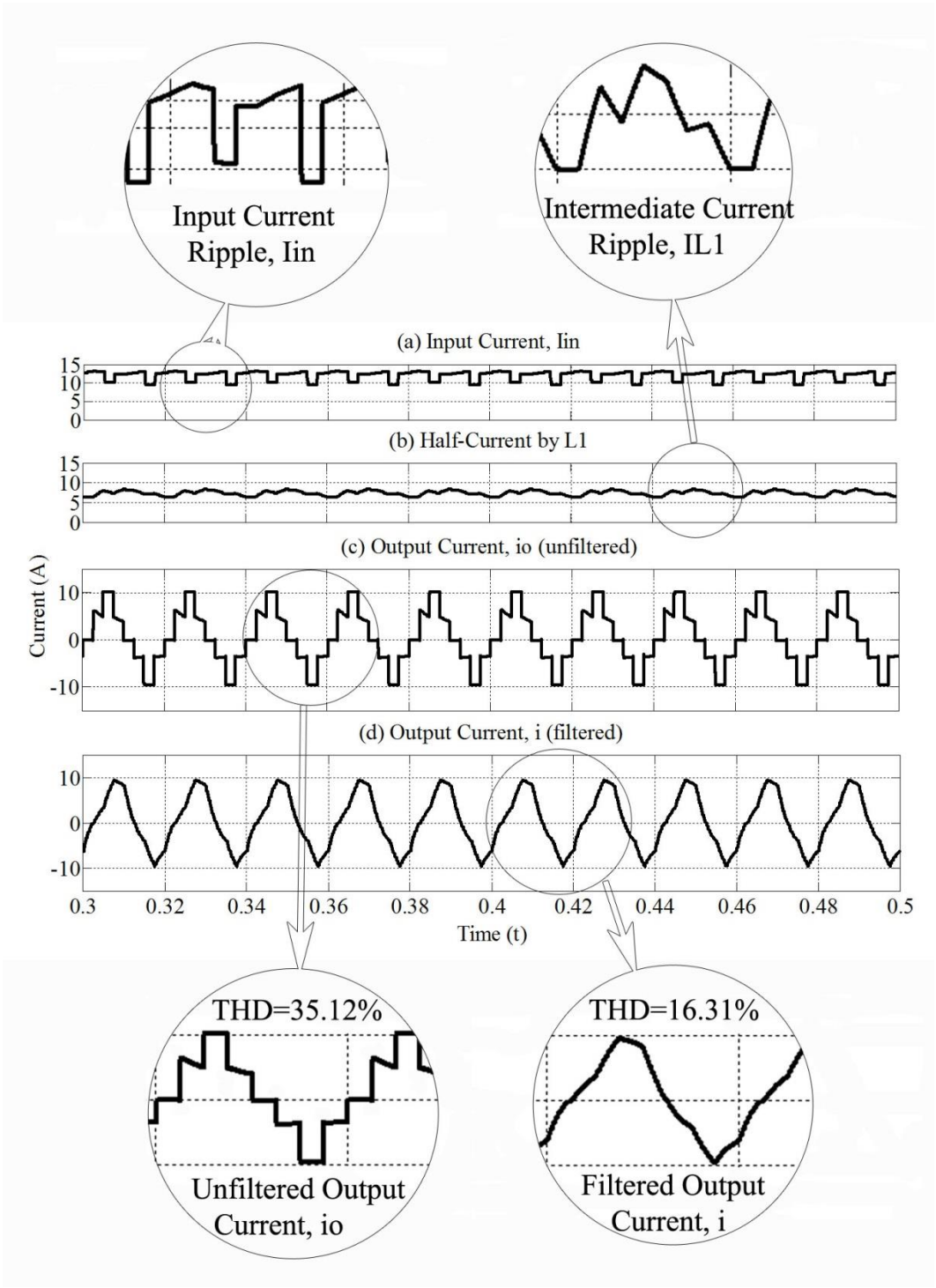


Fig.4 - 11: Five-Level CSI with equal switching angles

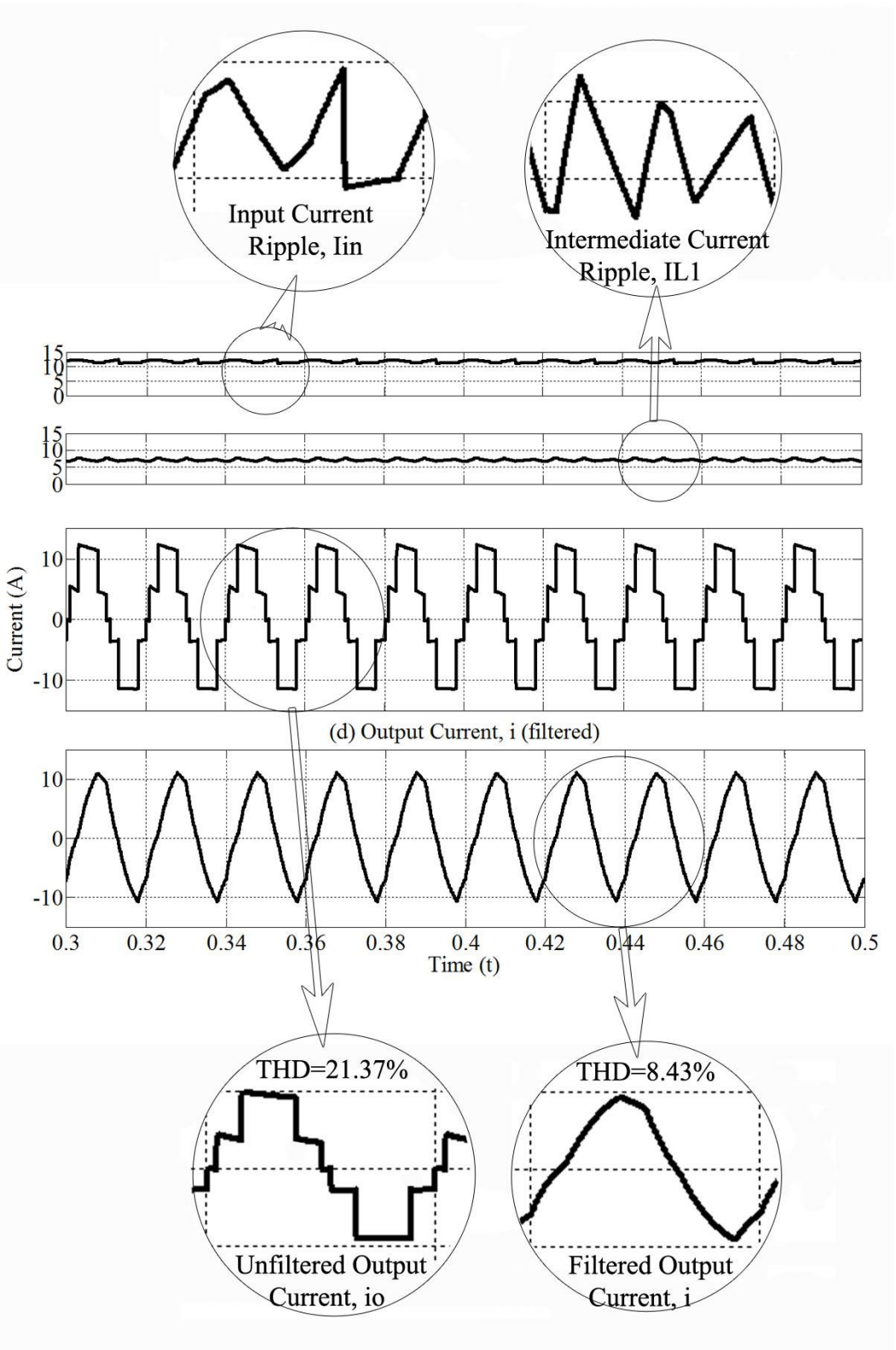


Fig.4 - 12: Five-level CSI with selected switching angles

4.3.3 Novel nine-level CSI

Similarly, for the nine-level novel inverter, the simulation parameters are summarized in Table 4-3. In this investigation, Matlab/Simulink simulations are run in two setups;

1) with equal angles; ($\theta_1=\theta_2=\theta_3=\theta_4=22.5°$) where all states have equal lengths in one period;
2) with variable angles; ($\theta_1=12.5°$; $\theta_2=15.5°$; $\theta_3=15.5°$; $\theta_4=22.5°$) where all states have variable lengths in one period.

Table 4 - 3: Simulation set of parameters 2

Parameter	**Label**	**Value**	**Unit**
Rated power	-	1	kW
Inductor	L1	20	mH
	L2	40	mH
Internal resistor	$r'_1 = r'_2$	0.33	Ω
	r'_3	0.68	Ω
Capacitor	C	150	uF
Output Freq	-	50	Hz
Load	R_{load}	6	Ω

The simulated performance of the nine-level inverter, driven by ($\theta_1=\theta_2=\theta_3=\theta_4=22.5°$) is shown in Fig.4-13. The figure shows five waveforms of the input current, inductor current L1 (half-current), inductor current L2 (quarter-current), unfiltered output current and the filtered output. It can be seen in Fig.4-13(b) that the inductor current through L1 is averaged around half (I/2) of the input current with some ripples whereas the inductor current flowing through L2 (Fig.4-13(c)) is averaged about a quarter (I/4) of the input current, I_{in}. Essentially, this verifies the stability thus feasibility of the topology. The total harmonic distortion before filtering is recorded much lower at 25.76 % compared to the one of five-level CSI, nevertheless, after filtering the index drops to 12.58 %. Additional details can be observed from the given figures.

For the second set-up, the variable angles choosen are (θ_1=12.5°; θ_2=15.5°; θ_3=15.5°, θ_4=22.5°). Similar to the five-level CSI, the inverter operated with variable angles exhibits much improved performance i.e. less ripple current particularly for the intermediate currents (inductor currents) and lower THD of the output current. In this set-up, the output current harmonics recorded before and after filtering are at 13.47 % and 7.77 % respectively. This reflects current balance in the power switches at steady-state and also verifies that the current THD of waveform can be improved with carefully selected angles. The details of the discussions are highlighted in Fig.4-14.

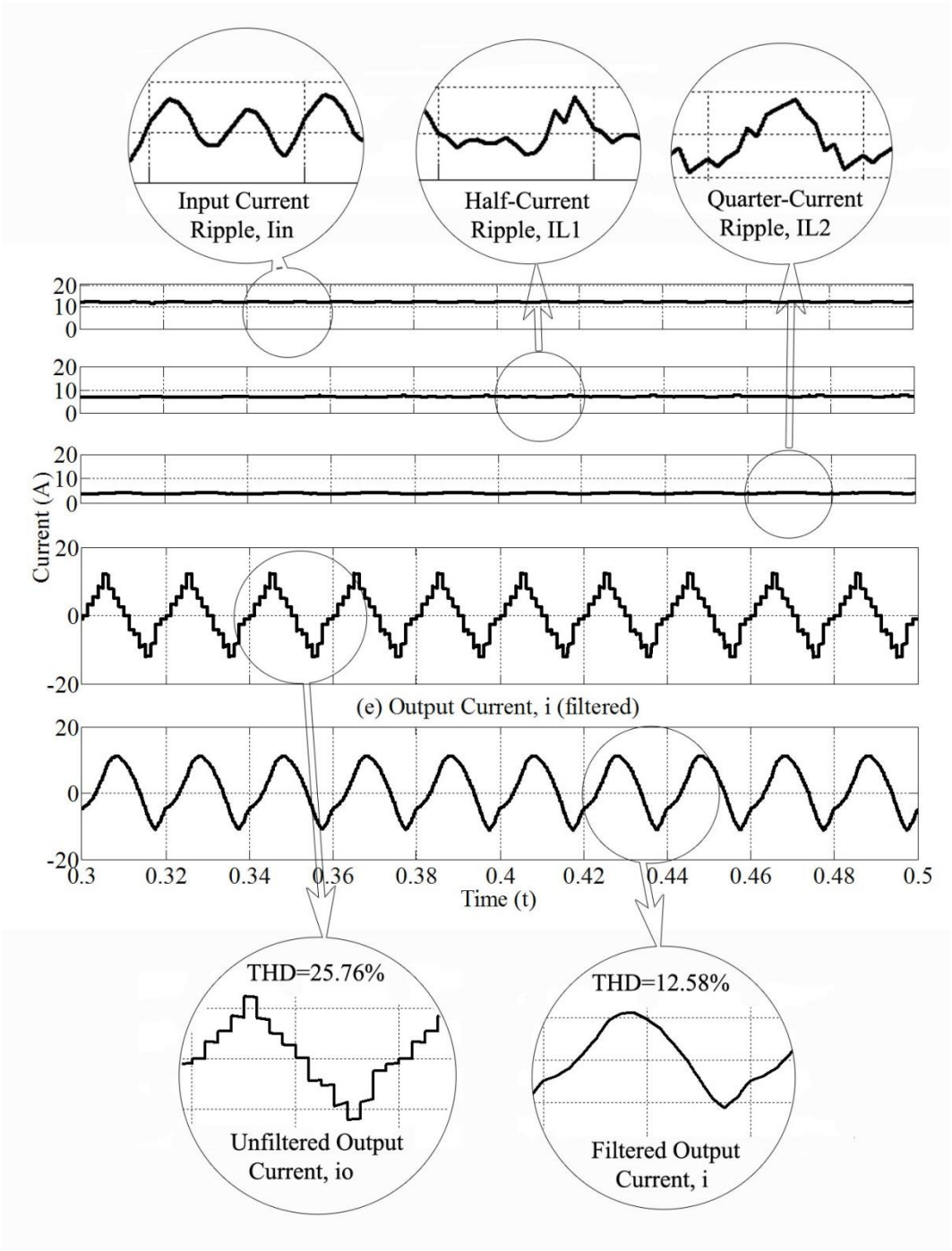


Fig.4 - 13: Nine-level CSI with equal switching angles

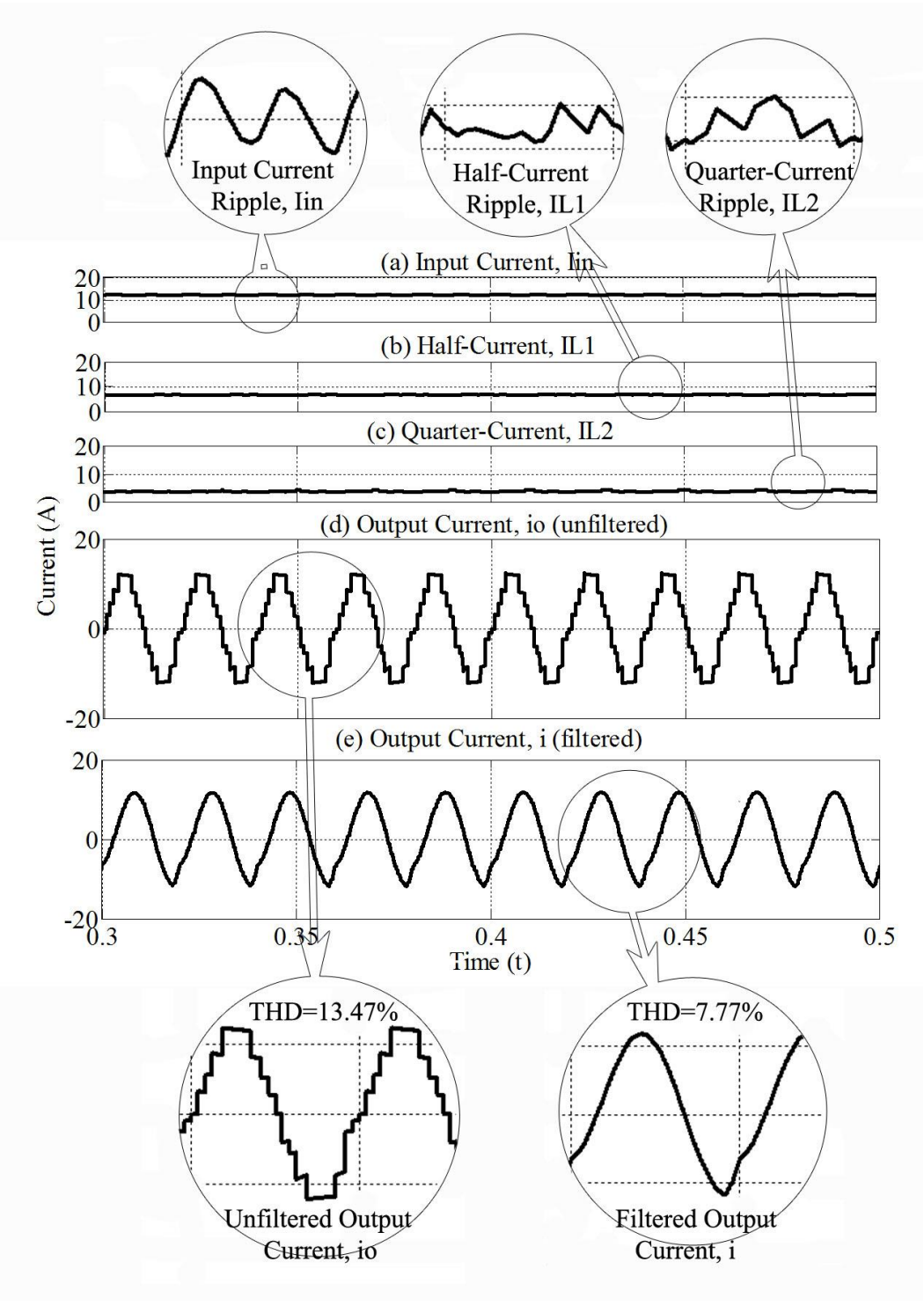
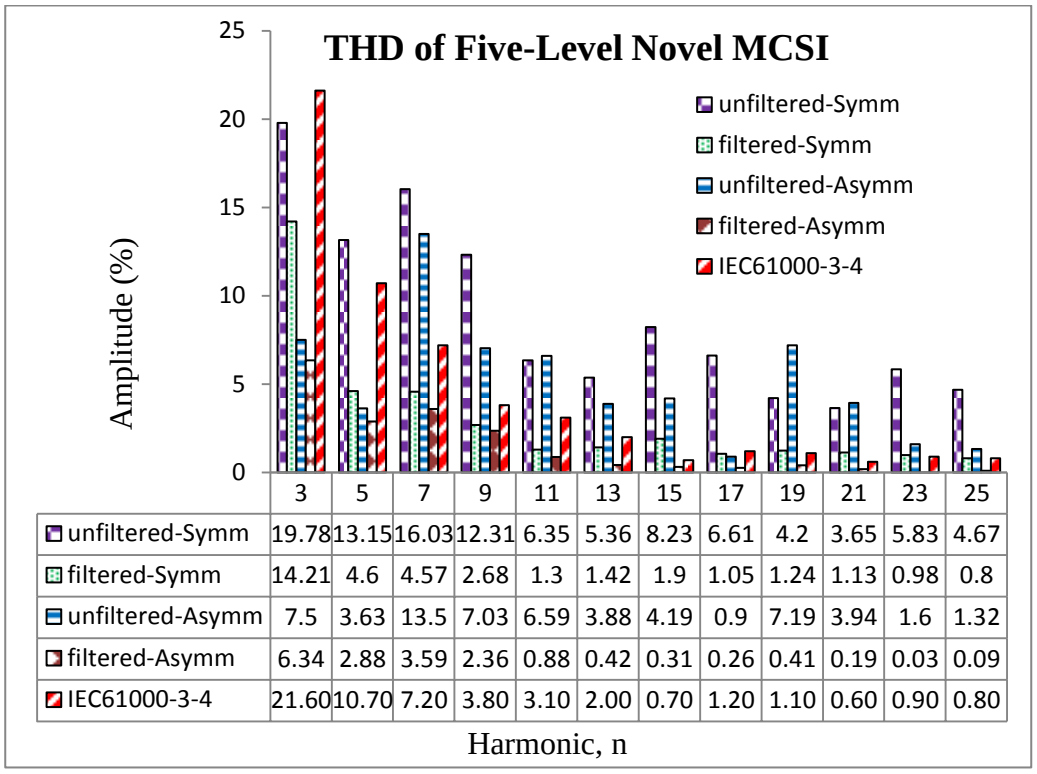


Fig.4 - 14: Nine-level CSI with variable switching angles

4.3.4 Total harmonic distortion

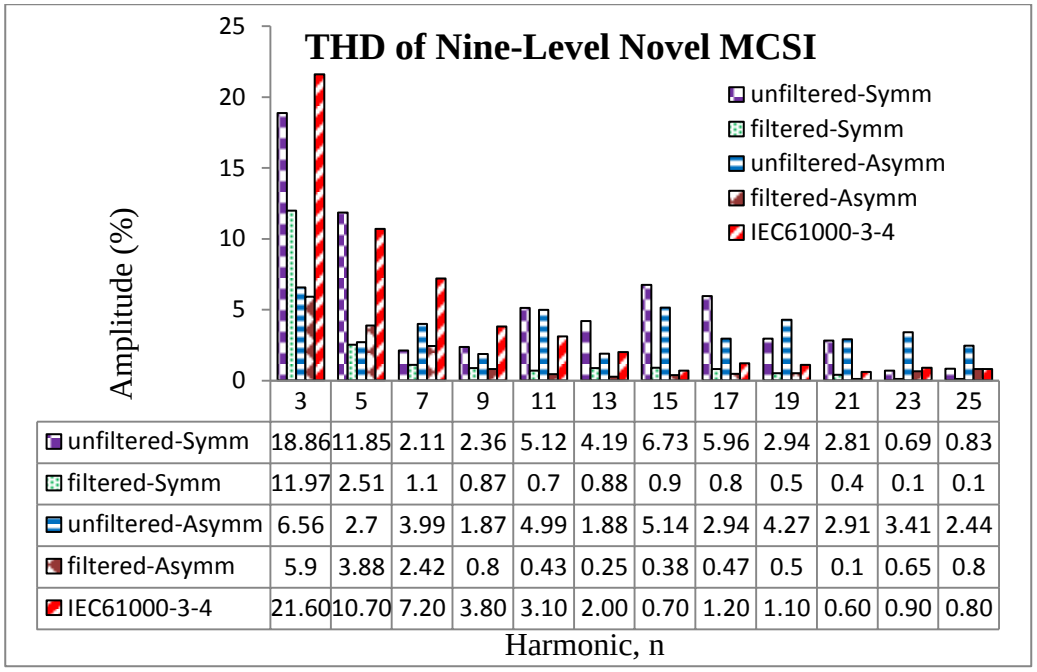
The current THD for all setups as per discussed previously are summarized in the bar graphs of Fig.4-15 for the novel five-level MCSI and Fig.4-16 for the novel nine-level MCSI. An international standard, IEC61000-3-4 [95] is included for reference. The IEC 61000-3-4 is an international standard for limitation of emission of harmonic currents in low-voltage power supply systems for equipment with rated current greater than 16 A of type 2; when the subject is still under technical development.

It can be observed in Fig.4-15 that for the novel five-level topology, the odd harmonics in general exceeds the minimum requirement set by the IEC61000-3-4 standard. However, for the asymmetrical angle switching, the THD reading are lower than the standard which indicates that the novel five-level MCSI can achieve low THD with proper switching angles acquisition and filtering. For the novel nine-level MCSI in Fig.4-16, it can be seen that in general the odd harmonics are lower than the set standard. The results are improved with the acquisition of appropriate switching angles and filtering.



	3	5	7	9	11	13	15	17	19	21	23	25
unfiltered-Symm	19.78	13.15	16.03	12.31	6.35	5.36	8.23	6.61	4.2	3.65	5.83	4.67
filtered-Symm	14.21	4.6	4.57	2.68	1.3	1.42	1.9	1.05	1.24	1.13	0.98	0.8
unfiltered-Asymm	7.5	3.63	13.5	7.03	6.59	3.88	4.19	0.9	7.19	3.94	1.6	1.32
filtered-Asymm	6.34	2.88	3.59	2.36	0.88	0.42	0.31	0.26	0.41	0.19	0.03	0.09
IEC61000-3-4	21.60	10.70	7.20	3.80	3.10	2.00	0.70	1.20	1.10	0.60	0.90	0.80

Fig.4 - 15: Current harmonic contents of the novel five-level topology



	3	5	7	9	11	13	15	17	19	21	23	25
unfiltered-Symm	18.86	11.85	2.11	2.36	5.12	4.19	6.73	5.96	2.94	2.81	0.69	0.83
filtered-Symm	11.97	2.51	1.1	0.87	0.7	0.88	0.9	0.8	0.5	0.4	0.1	0.1
unfiltered-Asymm	6.56	2.7	3.99	1.87	4.99	1.88	5.14	2.94	4.27	2.91	3.41	2.44
filtered-Asymm	5.9	3.88	2.42	0.8	0.43	0.25	0.38	0.47	0.5	0.1	0.65	0.8
IEC61000-3-4	21.60	10.70	7.20	3.80	3.10	2.00	0.70	1.20	1.10	0.60	0.90	0.80

Fig.4 - 16: Current harmonic contents of the novel nine-level topology

4.4 Performance comparison

Though the proposed topology has been the simplest topology, it may be useful to compare its other performances with more established existing topologies. In order to compare their VA ratings and efficiencies, the simulation parameters as in Table 2-4 are applied to the circuit. Fig.4-17 shows the voltage-ampere reading of the novel five-level CSI compared to the previous four topologies that were discussed in Chapter 2. It can be seen that not only the novel topology is the simplest, its VA rating is one of the lowest. Fig.4-18 compares the novel five-level inverter efficiency. It can be seen that the novel inverter has the highest efficiency at lower load currents. However, the efficiency at midrange is rather constant before plummeting at high load currents. It is convincing that the proposed topology has comparable performances to the existing topologies if not better in certain areas.

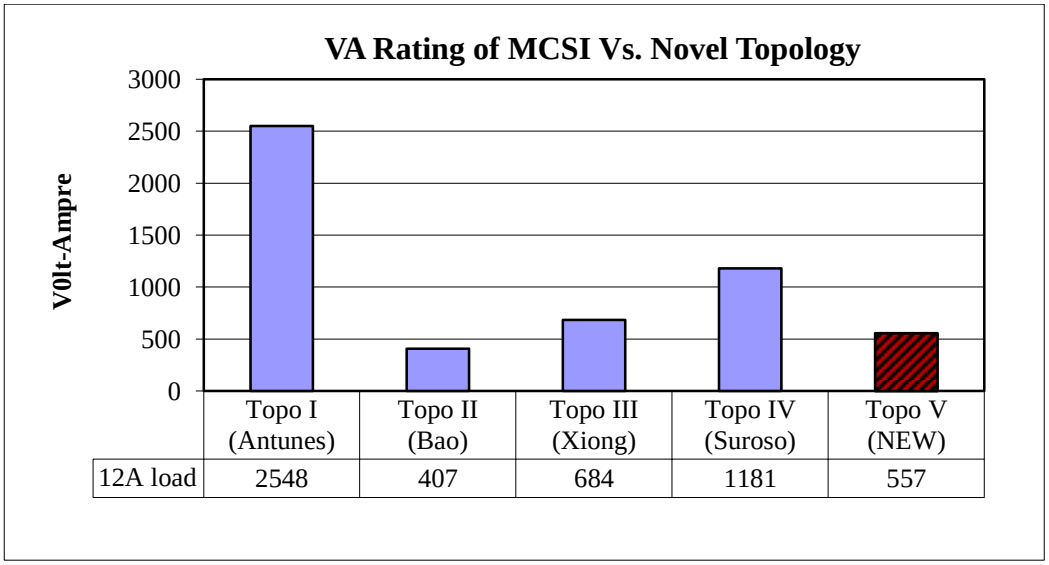


Fig.4 - 17: VA rating of novel topology

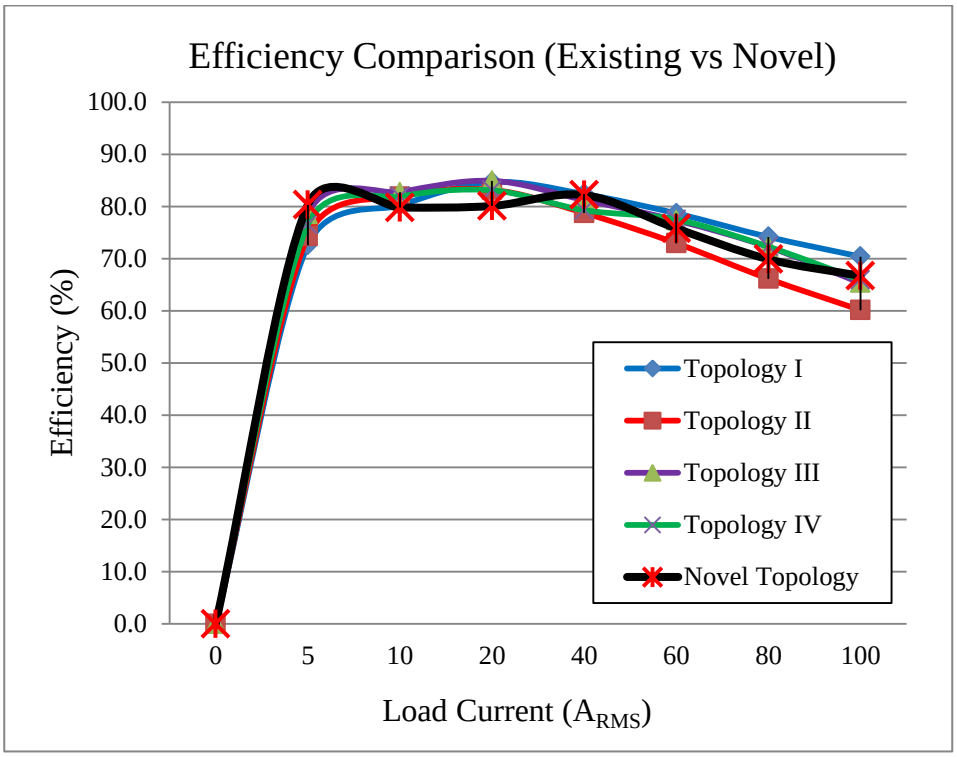


Fig.4 - 18: Efficiency vs. Load current of novel topology

4.5 Summary

A new topology to overcome common problems faced by the existing multilevel current-source inverters such as large component count, high control complexity to balance the inductor current and thus uneconomic is proposed. It is based on a generic multilevel structure with one single current source that theoretically can be expanded to infinite level to gain zero THD. Its main attraction is the simplest structure, with fewer numbers of power devices and sharing inductors which essentially reduces the design complexity as well as control complexity. The novel inverter starts with five-level current output, and can be extended to nine-level current with only two additional power switches and one inductor added to the circuit. The employment of a bidirectional switch is the key factor of the simple design.

For initial design verification, the novel inverter is simulated via Matlab/Simulink to investigate the feasibility of the topology. By computer simulation it was found

that the inverter has successfully achieved inductor current balance at steady-state for both five- and nine-level current outputs with a simple low frequency modulation control technique. The current harmonic contents recorded are also of acceptable values after some filtering. Finally, upon comparing the proposed topology to existing topologies, it is proven that their performances are comparable.

CHAPTER 5

Experimental Arrangements, Results and Discussions

This chapter discusses the practical construction of the novel multilevel current source inverter topology. Its primary aim is to verify the theoretical analysis as well as the simulated characteristics of the proposed five- and nine-level current source inverters. A 1 kW experimental prototype was built and tested. The experimental results are discussed and compared with the simulation results at different operating conditions. Tests for various switching angles were carried out in order to demonstrate the feasibility of the new circuit. Comparisons of the harmonic contents of the proposed inverter to the simulated results are provided to verify the proposed inverter feasibility.

5.1 General experimental set-up of the inverter test circuit

As illustrated in Fig. 5-1, the experimental test set-up consists of four main units: a dc current source as the main input that supplies the required power to the main dc/ac inverter circuit under experiment, the multilevel inverter power circuit employing IGBTs, the Xilinx FPGA controller board, and the resistive load of 6 Ω that connected to the main circuit allows a maximum output power of 1 kW. Fig. 5-2 showing the actual experimental test rig as was explained before. By referring to the component groupings, the leftmost components are the three inductors of 2 x 40mH and 1 x 32mH that are connected in series with total accumulation of 112 mH. These inductors are connected to the main dc voltage supply unit (Fig. 5-1) to emulate a dc current supply source. The second group shows the sharing inductors which formed the L1 and L2. In the actual experiment, the rig is current-level adjustable i.e. the rig can be run either in the five-level mode or nine-level mode. For example in the nine-level mode, both L1 and L2 are employed whereby they are 20mH and 60mH respectively. However, in the five-level mode, only one inductor is required. When referring to circuit of Fig. 5-1, the inductor L1 will be bypassed while the inductor L2 is adjusted to 40mH. These changes must be done manually before each experiment. For safety reasons, each inductor group is equipped with protection diode. The third group consists of a number of resistors representing r'1, r'2 and r'3 (Fig 5-1). The r'1 and r'2 are the internal resistance value of L1 while the r'3 is the internal value of L2. These resistors are utilized to stabilize the current branches without any sharing inductors. Finally the last group consists of the IGBT driver board and also the CSI power circuit in cascading arrangement which will be discussed next.

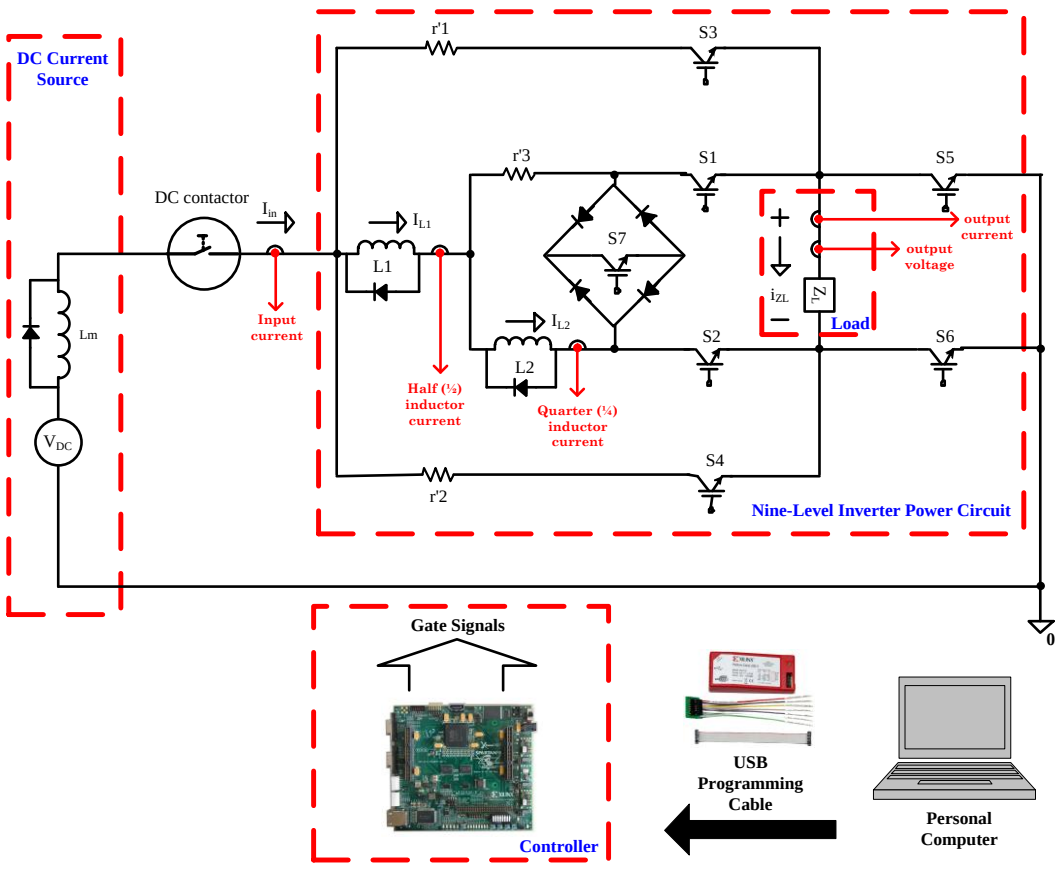


Fig.5 - 1: General experimental layout

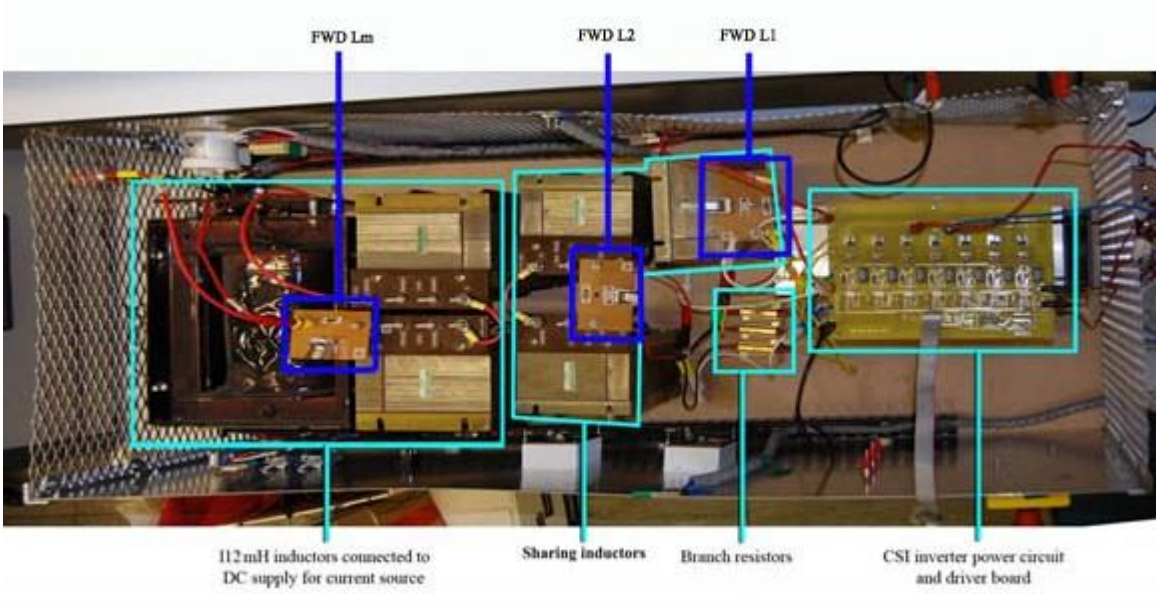


Fig.5 - 2*:* Actual experimental test rig

5.2 IGBT driver circuits

Fig. 5-3 shows the IGBT driver board with seven separate circuits to drive seven IGBTs that made up the CSI power circuit. These drivers and power circuits are properly designed so that these circuit boards can be used to run the five- and nine-level CSI with minimal adjustment in the circuit. Fig. 5-4 shows a cut-out of one driver circuit. An ideal driver circuit is important because it provides isolation and protection between the FPGA controller and the power devices. In this project, the driver circuit is designed using the HCPL-316J by Avago Technologies. The HCPL-316J is a 2.5A isolated gate drive optocoupler with integrated (VCE) desaturation detection and fault status feedback. Its intelligent fault detection mechanism makes this driver a good choice for this application where it can drive a high power IGBT and isolate the FPGA controller from high voltages. This driver also has extra features like fast IGBT switching and short propagation delay times for fast switching [96] that makes it more interesting.

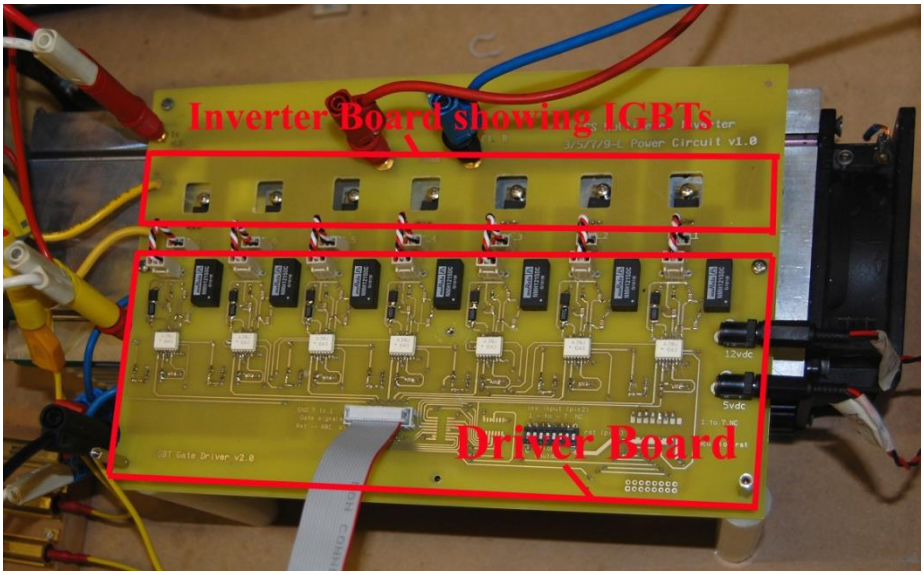


Fig.5 - 3: IGBT driver circuit and the power circuit

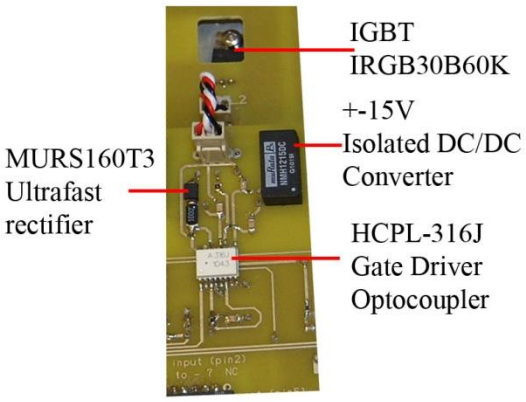


Fig.5 - 4: Single 316J driver circuit and IGBT

5.3 CSI power circuit

The experimental CSI power circuit (Fig. 5-5) consists of seven IGBTs including one bidirectional IGBT employing four ultrafast diodes in the centre. The experimental CSI power board is designed such a way with connecting points on one side so that the board can be multi-tasking; whereby the board can run three-, five- or nine-level inverter experiments with minor adjustments. For example, to run the basic three-level inverter experiments, two IGBTs on each sides of the bidirectional IGBT located at the centre are utilized. Whenever the level is increased to five-level current, this bidirectional IGBT will be utilized together with the two previously stated IGBTs and lastly for the nine-level output, all IGBTs will be operated. Table 5-1 summarises the specifications of the IGBT switches and the diodes of the experimental CSI power board.

Table 5 - 1: IGBT switches and diodes of the CSI power board

Components	Manufacturer	Part No.	Max Voltage	Max Current
IGBT	International Rectifier	IRGB30B60K	600V V_{GE} =15V	50A
Power diodes	Vishay Semiconductors	HFA30TA60CS	600V V_f =1.7V	15A

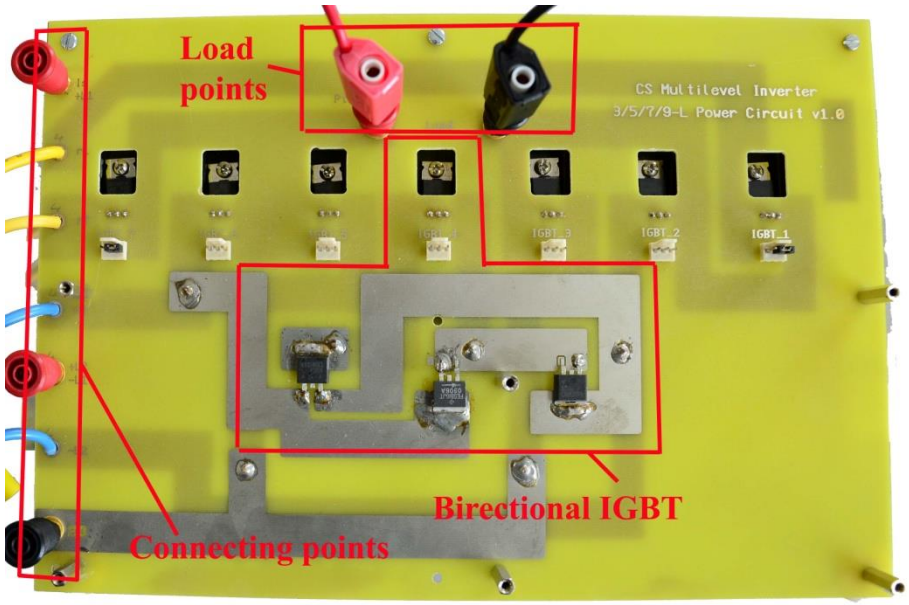


Fig.5 - 5: CSI power board

5.4 Controller circuit

The seven IGBT switches experimented above are all independently controlled by seven independent PWM generators; hence, the Field Programmable Gate Array (FPGA) is the best solution for the application since it can provide a good number of simultaneously running independent PWM generators. The Xilinx Spartan-3A DSP 1800A (Fig. 5-6) FPGA board is the low-cost solution for the design nevertheless performs satisfactorily in the proposed application. While all control applications can be easily developed using the Spartan-3A development board, the Xilinx FPGA is programmed using Xilinx ISE 10.1 software. The Xilinx ISE (Integrated Software Environment) is a software tool for synthesis, analysis and compiling (or synthesizing) the Verilog and VHDL languages. Appendix B also presents the VHDL programming for the five-level MCSI with switch overlapped period of 3us for the experiment. Finally, while the key features of the Spartan-3A controller above are summarized in Table 5-2, more information can be found in [97].

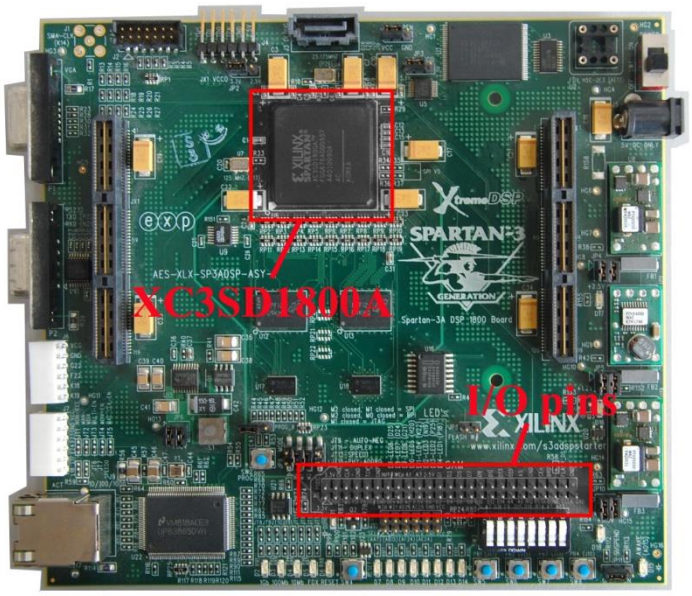


Fig.5 - 6: Spartan 3-A DSP 1800A development board

Table 5 - 2: Summary of the key features of the Spartan-3A

Parameter Name	Value
Xilinx Devices	• XC3SD1800A-4FGG676C Spartan-3A DSP FPGA
Clocks	• 125 MHz LVTTL SMT oscillator • LVTTL oscillator socket • 25.175 MHz LVTTL SMT oscillator (video clock) • 25 MHz Ethernet clock (accessible to FPGA)
Memory	• 128 MB (32M x 32) DDR2 SDRAM • 16Mx8 parallel / BPI configuration flash • 64 Mb SPI configuration
Interfaces	• 10/100/1000 PHY • JTAG programming/configuration port • RS232 Port • Low-cost VGA • 4 SPI select lines
User I/O and Expansion	• Digilent 6-pin header (2) • EXP expansion connector (2) • 30-pin GPIO connector

5.5 Design and construction of the proposed inverter circuit

Fig. 5-7 shows the complete MCSI experimental set-up for this research. For safety reasons, the power circuits, controller, and all electronic components were housed in the main rig that was built by a metal cage except for the load because of its extra-large size. The programmable dc power supply used was made by Regatron (UK); where its positive output terminal was connected to the 112 mH inductor to emulate a constant dc current source. The current source was connected to the power circuit via a dc contactor to avoid voltage and current sparking whenever the inductors were energized. Although the proposed inverter were designed to drive a load of up to 1 kW; however, in this experiment the load resistance used was represented by a variable resistor of 10Ω (12A rated current). Therefore the maximum current by the programmable dc source was limited to 12 A to avoid damages and safety concerns. Further details of the experimental set-up and also most key components employed in this experiment are described in Appendix C.

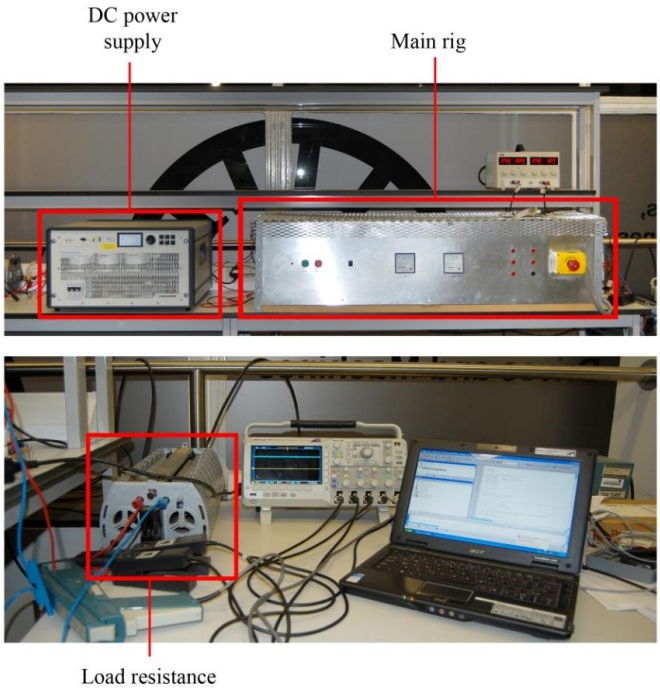


Fig.5 - 7: Complete MCSI experimental arrangement set-up

5.6 Experimental analysis and results

Fig. 5-8 shows the experimental results for the current at the input, I_{in} and the current through the inductor, I_{L1}. It can be seen that both currents are essentially an average constant current at steady state although there are observable ripples in both currents. The inductor current is obviously averaged at around half of the input current which is expected in a balanced system; therefore allowing the five-level output current to be generated at steady-state as shown in Fig.5-9. With some filtering, a near sinusoidal load current waveform is obtained as shown in Fig.5-10. Although filtered, this waveform however, still contains a quite high distortion level. This is evident from Fig.5-11 where both waveforms exhibits THD levels at 28.25 % before filtration and 17.31 % after filtration.

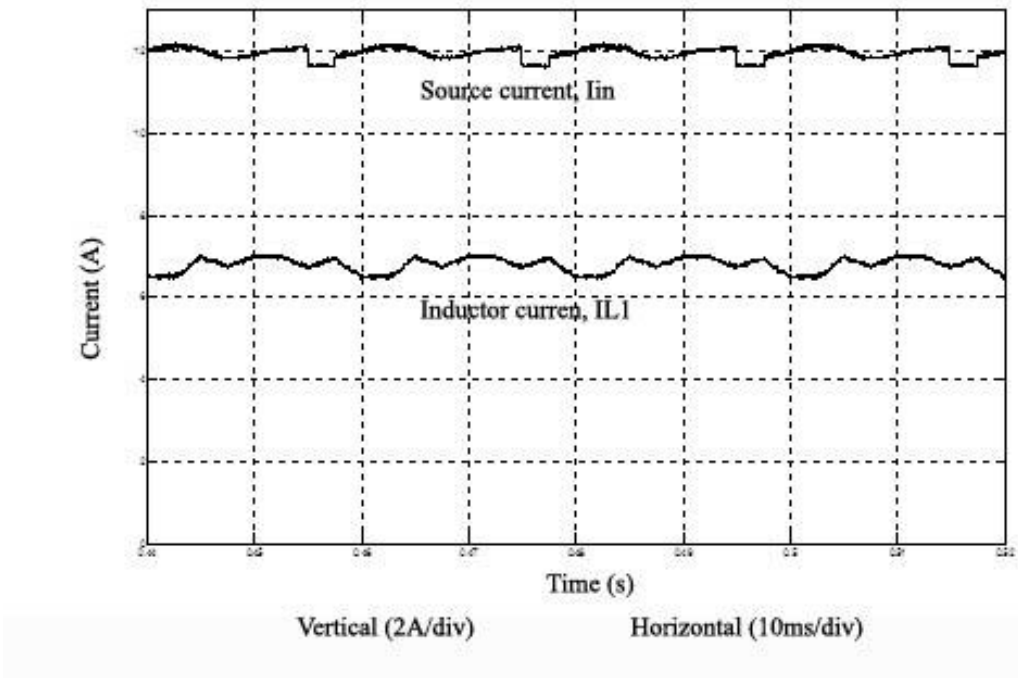


Fig.5 - 8: The source current and inductor current waveforms

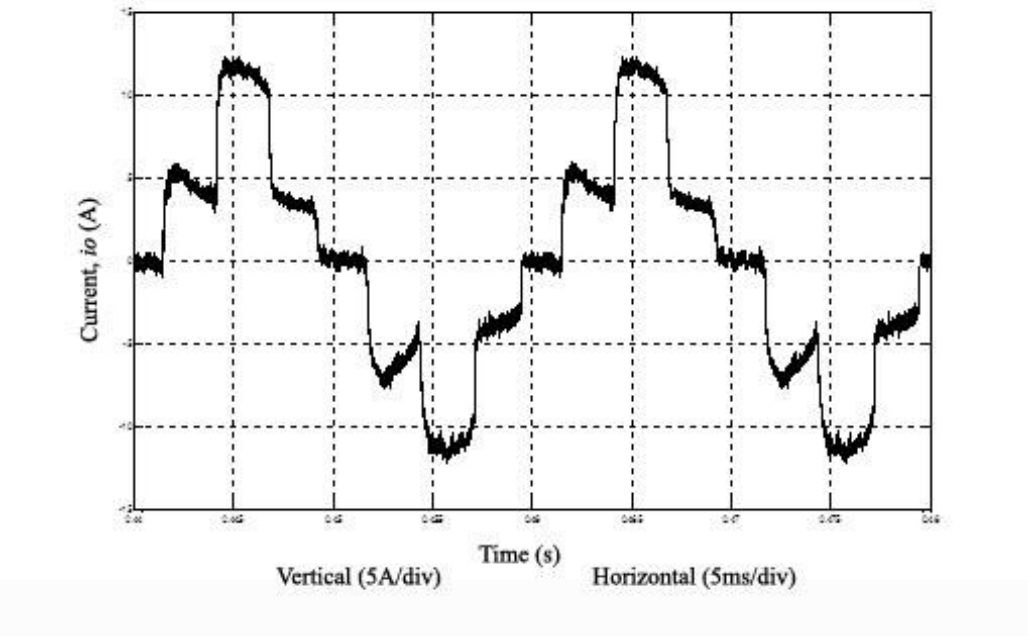


Fig.5 - 9: The five-level output current waveform

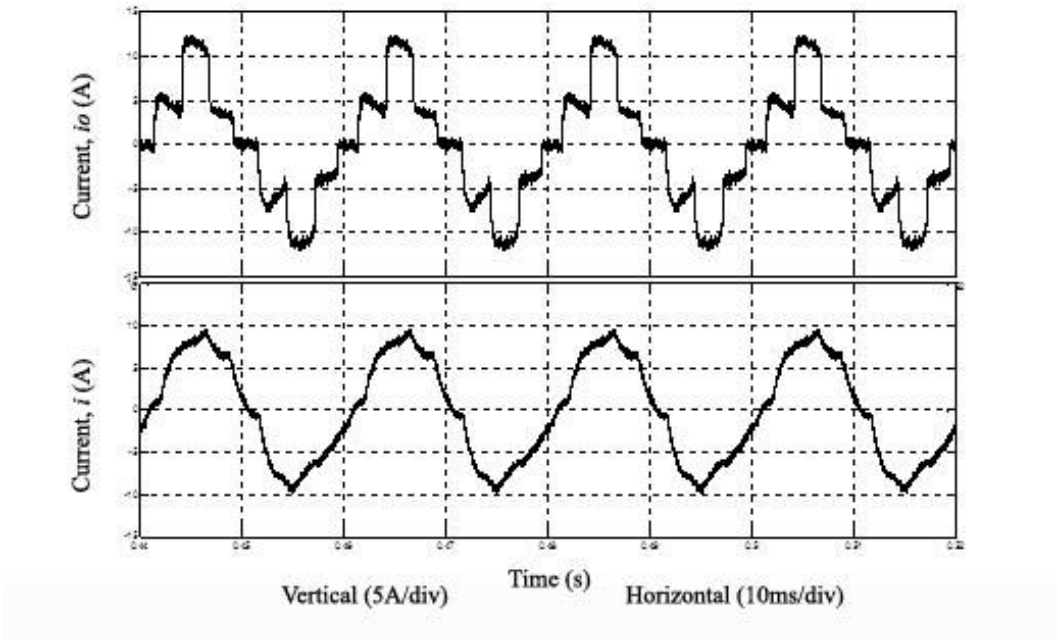


Fig.5 - 10: The output current before and after filtering

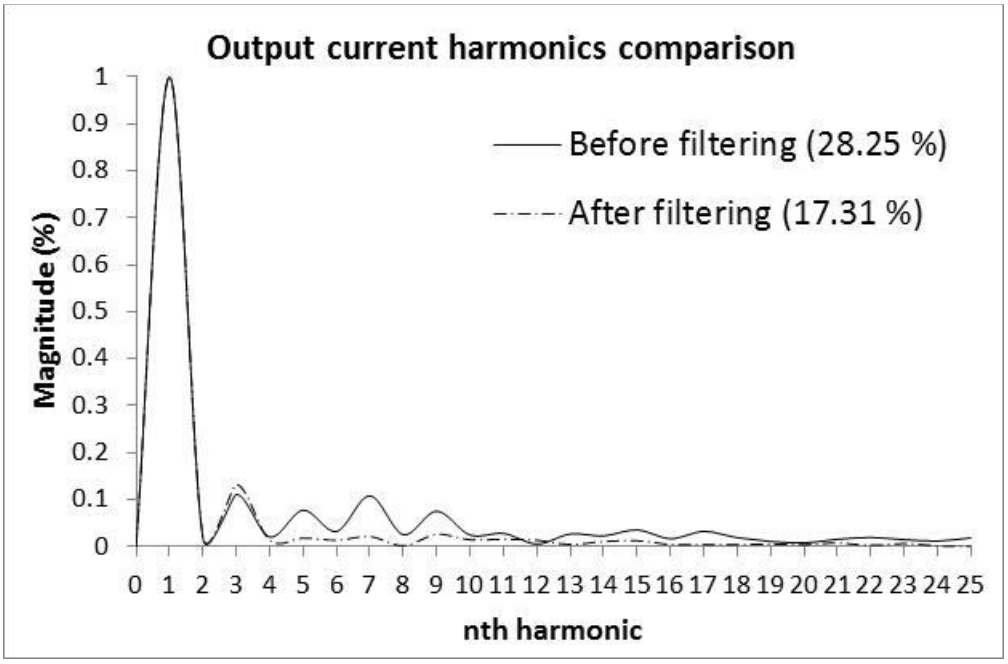


Fig.5 - 11: Harmonics comparison before and after filtering

In Fig.5-12 and Fig.5-13, the experimental output current waveforms are compared to the simulation results obtained earlier in chapter 4. By comparing both results, it can be seen that both waveforms are identicals in terms of shapes and amplitudes although some variations in amplitudes are expected since typical hardware specifications; particularly inductors, varies considerably eventhough bought from the same manufacturer. The harmonics contents of the four waveforms from Fig.5-12 and Fig.5-13 are compared and presented in Fig.5-14. It is evident that both simulation and experimental waveforms exhibits equivalent amount of harmonics which verifies the feasibility of the proposed novel MCSI topology.

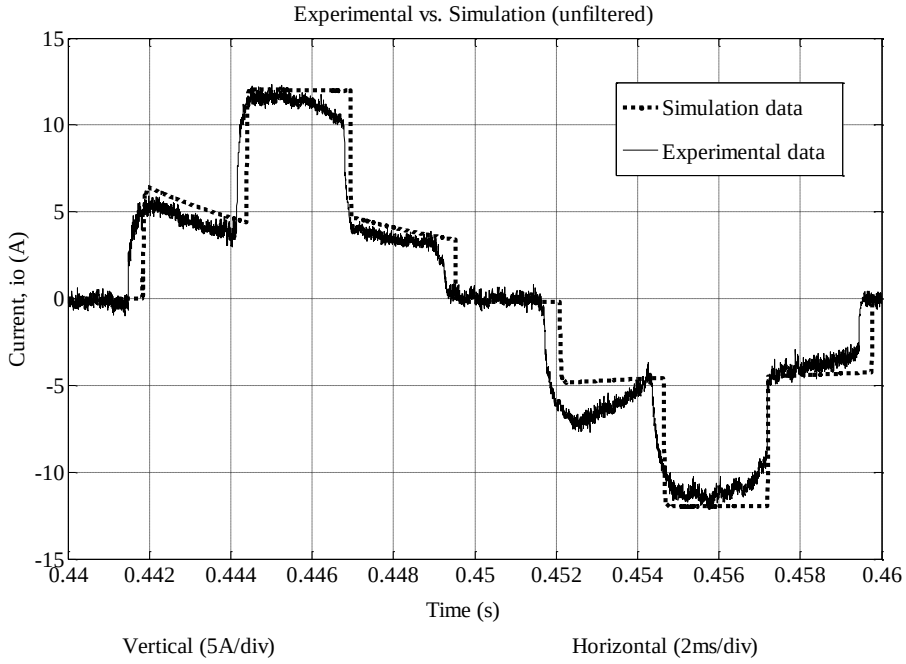


Fig.5 - 12: Experimental vs. simulation (unfiltered waveforms)

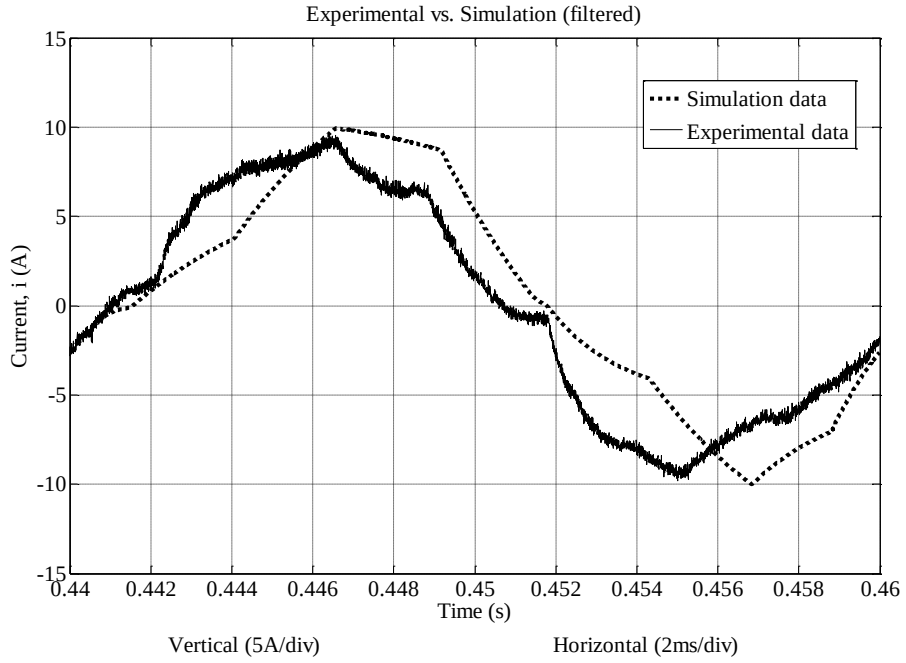


Fig.5 - 13: Experimental vs. simulation (filtered waveforms)

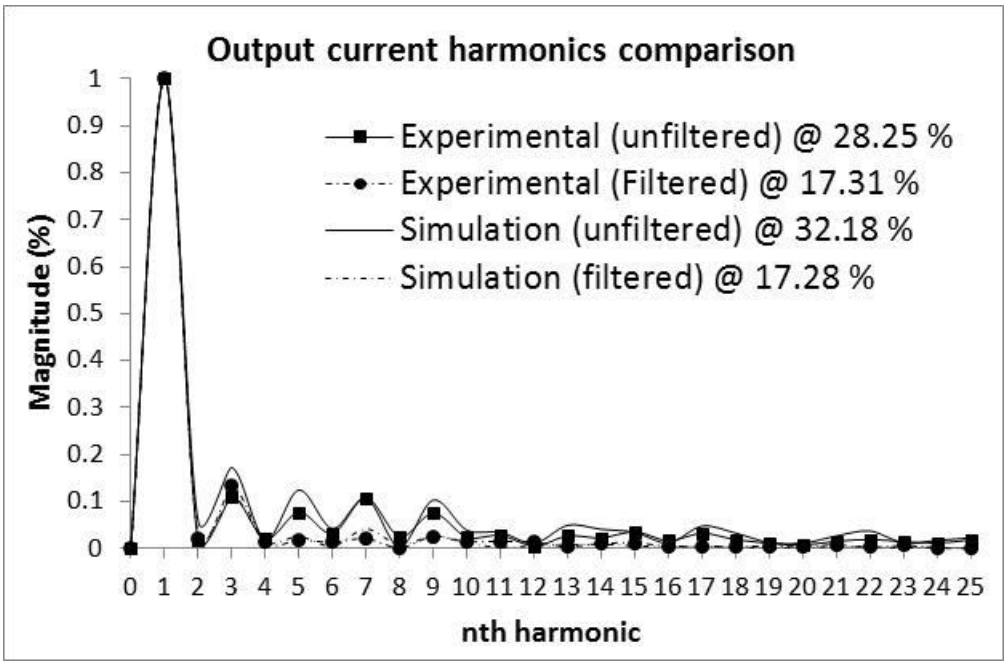


Fig.5 - 14: Harmonics comparison between experimental and simulation

Previously, it was also demonstrated by software simulation that the harmonic contents of the five-level inverter can be reduced by applying different switching angles, θ to the power switches. By using the same switching angles previously applied in the simulation of (θ_1=15.5°; θ_2=38.5°), the waveform of Fig.5-15 is obtained. The five-level output inverter current shown here is an unfiltered waveform. By comparing the harmonic contents of the waveform to the harmonic contents of the unfiltered waveform from Fig.5-9, it is proven that the harmonic contents improved with specific switching angles. This is due to the massive reduction of some of the low order harmonics i.e. the 5^{th} and 9^{th} harmonics are nearly eliminated in Fig.5-16.

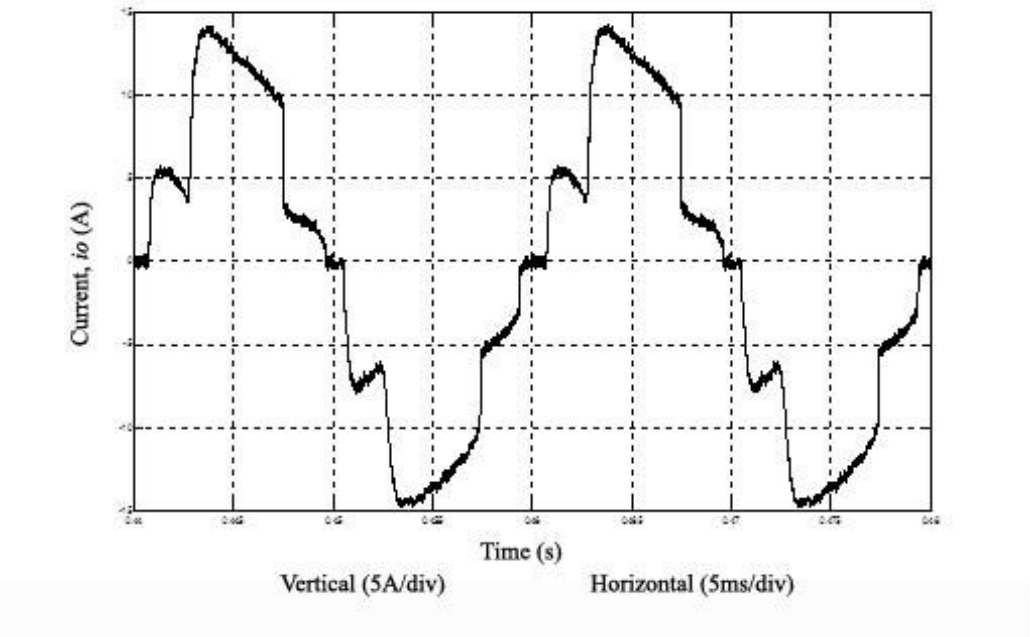


Fig.5 - 15: The five-level output current with different switching angles

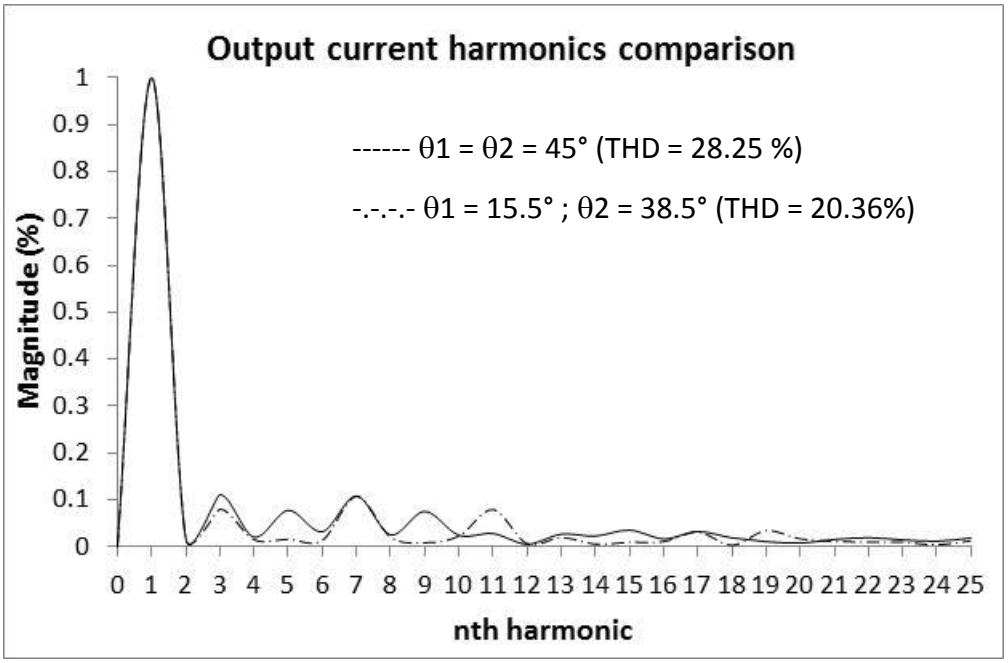


Fig.5 - 16: Harmonic contents improved at specific switching angles, θ

5.7 Summary

This chapter has presented the detail descriptions of the novel MCSI and its experimental rig construction. The constructed experimental rig has been successfully tested to run the novel five-level inverter. The experimental results of the five-level inverter has been presented and verified by the simulation results. By the close proximity of both results, it can be concluded that this investigations have proven the feasibility of the proposed novel multilevel current source inverter.

CHAPTER 6

Conclusions and Suggestions for Further Works

This thesis presents an investigation of a novel multilevel current source inverter (MCSI) topology in particular of a generic inverter family with a single dc current source. The term "generalized" as discussed in chapter 2, is basically referring to the multilevel inverter's basic circuit arrangement that allows that particular multilevel topology to be elevated to a higher level by adding more switches to the circuit in such a way common to the specific multilevel topology without modifying its basic circuit. This is an interesting feature for MCSI topologies since it will provide future expansion of the hardware with ease besides being a single current source inverter. Amongst limited literatures, there were four topologies adhere to the research ideas. These existing topologies were generally experimentally tested up to five-level current outputs whereas for the higher current level, it is simply executed by computer simulations mainly due to control complexity. Therefore, the aim of this project was to study the feasibility of the generalized single-source MCSI topologies. The results of the first study allowed the critical assessments and comparisons between these topologies, in terms of power rating, component count, design complexity and efficiency. From the assessments, a novel topology was proposed where the new topology improved the feasibility of MCSI for practical implementation at higher current-level. An experimental rig has been constructed and the experimental results have been presented and compared with the simulation results.

6.1 Conclusion

This research has investigated the operation characteristics of novel topologies of multilevel current-source inverter systems to produce the required high levels of dc current with near sinusoidal ac current waveforms in some high-current applications such as in a large ac variable speed drive. The operation of these novel multilevel current-source inverter topologies has been analysed, modelled and experimentally verified to assess their performances. Initially, the research has been focused on the analysis side of works which were targeted to come out with a new converter topology that will improved the existing topology performances and diminishes any limitations. In carrying out the research and experiments, lists of contributions are discussed below.

6.2 Contributions to knowledge

The research work has reviewed the present state-of-the art in MCSI technology by discussing the classical and the more recent MCSI topologies to the newly emerging generalized MCSI topologies, its modulation and example applications. It can be concluded that although its complement topology of MVSI has been widely accepted in modern industrial applications and has reached a certain level of maturity, MCSI on the other hand is far behind at laboratory research stage. Nevertheless, the recent increased in the amount of publications on this particular subject indicates that there are rooms for further development. With continuous development of new topologies and modulation strategies recently, it is a fact that the generalized MCSI topologies are getting more attentions and will be the future of multilevel converter technology.

The thesis also describes in details the concept of multi-levelling of current in typical generalized MCSI topologies. The differences in terms of the structures and control requirements amongst the existing generalized MCSI topologies are investigated. It was established that in the existing generalized MCSI topologies, though theoretically doable; if the expected current level is above five-level, the

control system required will be nearly too complex to achieve. This is due to (1) the increasing number of power switches which results in nearly impossible means to discover the workable switching sequence arrangement without involving any complex tools or control technique and (2) the increasing number of the DC inductors, where the currents through them must be managed individually to the approximately constant currents at the specific level or amplitudes.

In this thesis, a novel generalized multilevel CSI topology has been proposed which; significantly reduces the number of crucial elements such as the power switches and inductors and has a modest control system compared to its peers. This has been proven experimentally by the successful implementation of a five-level inverter derived from the proposed topology. Although only experimented at the low power level, it is expected that this topology will be also practically viable at higher power levels and even possibly cost-efficient.

6.2.1 Other contributions:

Performance investigations were carried out on four existing generalized MCSI topologies. The inverters were compared in terms of total installed power rating, total component count, design complexity, control complexity and efficiency in order to find out the most cost effective topology. It was found out that there is no superior circuit amongst them.

As MCSIs are sparely used, only a few control methods have been published to control the half-level inductor currents in order to achieve high quality output waveforms. However, the published technique suffers from the high-load conditions. This thesis proposes an enhanced control technique to improve the output current quality of a multilevel current-source inverter operating at both high- and low-load conditions. The new technique, named as redundant

switching-pulse width modulation (RS-PWM), combines the simple control of redundant-switching methods with more flexible PWM methods and has been shown in this study to be superior to both. The results have been validated by laboratory experiments using a 250 VA test circuit.

6.3 Further works

As discussed, the proposed five-level MCSI has shown comparable performances to the existing topologies. The statement is supported by the experimental analysis discussed in Chapter 5. However, previously the finding focuses only on the resistive load. Perhaps it is worthwhile to investigate the capability of the proposed inverter topology to operate with a common load e.g. ac motor. Since an ac motor is inductive by nature, it should be interesting to see the current output behaviour resulted while employing a practical load in comparison to purely resistive load. It is clear that higher inductance value in MCSI helps reducing the output current ripple. Whereby, general MCSI topologies exhibits inductive characteristics which of much higher values than an ac motor. Therefore, it is presumable that an inductive load such as motor would perform equivalently to a resistive load.

In the Chapter 4, it was established that the newly proposed topology gives the best advantage with its nine-level inverter topology although only the five-level inverter was experimented. The nine-level output current is easier to filter thus making it more advantageous for practical application in conjunction to its smallest component count. The control strategy of the nine-level inverter however, is a bit complex than before. Nevertheless, it becomes an interesting challenge for future research to develop a new or improved switching scheme to make use of the nine-level MCSI advantages. Pairing the new control scheme with a practical load should enhanced the idea.

Appendix A

Simulink Model

Appendix A describes the Simulink models used for the simulations. The logic signals generation method is also explained in reasonable details. Although most figures are acquired from one topology; however, the method explained is common to all other topologies.

A.1 IGBT Block

The IGBT Block implements a macro model of the real IGBT device which is employed from the SimPower Systems blocks of power electronics library (Fig. A.1). The IGBT block implements a semiconductor device controllable by the gate signal which is simulated as a series combination of a resistor R_{on}, inductor L_{on}, and a DC voltage source V_f in series with a switch controlled by a logical signal ($g>0$ or $g = 0$) [81].

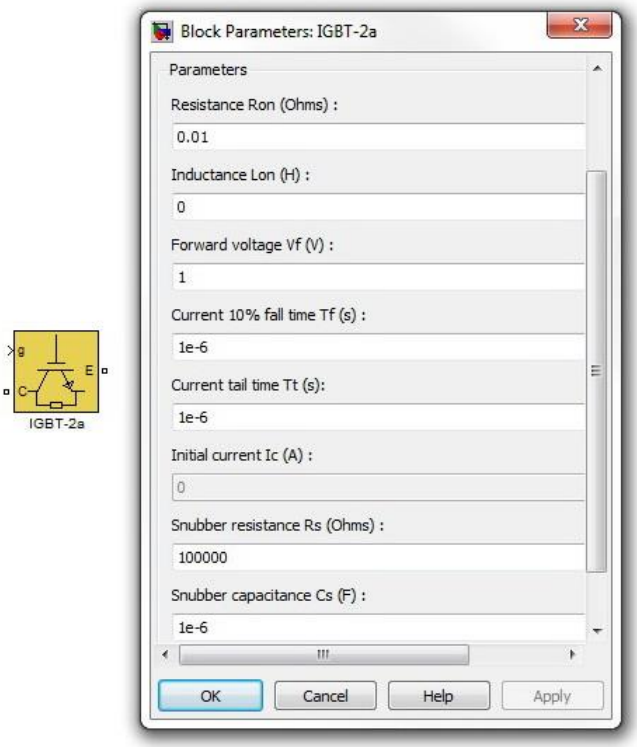


Fig.A.1: The IGBT block showing the dialog box and parameters

Depending on the value of the inductance L_{on}, the IGBT is modelled either as a current source ($L_{on} > 0$) or as a variable topology circuit ($L_{on} = 0$). The IGBT block cannot be connected in series with an inductor, a current source, or an open circuit, unless its snubber circuit is in use. The parameters in the dialog box are:

a. Resistance R_{on} - The internal resistance R_{on}, in ohms (Ω).
b. Inductance L_{on} - The internal inductance Lon, in henries (H).
c. Forward voltage V_f - The forward voltage of the IGBT device, in volts (V).
d. Current 10 % fall time - The current fall time T_f, in seconds (s).
e. Current tail time - The current tail time T_t, in seconds (s).
f. Initial current I_c – The initial current flowing in the IGBT (usually set to 0)
g. Snubber resistance R_s - The snubber resistance, in ohms (Ω). (R_s = inf to eliminate the snubber from the model).
h. Snubber capacitance C_s - The snubber capacitance in farads (F). (C_s = 0 to eliminate the snubber or C_s = inf to get a resistive snubber).

Fig.A.2 shows the model used for the bidirectional switch which consists of an IGBT block and four (4) diodes model from the same library as the IGBT. The diode block implements a macro model of a diode device in Simulink.

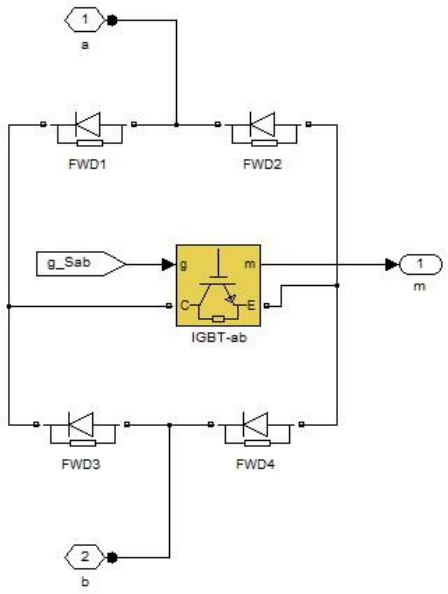


Fig. A.2: The bidirectional IGBT switch

A.2 Gate Signal Block

By referring to the Matlab/Simulink model in Fig.4-8, the expanded gate signals block for the five-level MCSI is shown in Fig.A.3. From the block on right, it can be seen that there are five (5) signals are yielded and assigned to the five (5) IGBT switches. Several blocks on left are to specify the different switching angles (θ_1 ; θ_2) used for asymmetrical simulations in Chapter 4. By expanding the signal block of Fig.A.3, more controlling blocks are revealed as in Fig.A.4. Each switches on left are assigned with the pre-defined gate control signals as previously illustrated in Fig.4-4 of Chapter 4. The development of these signals will be discussed next.

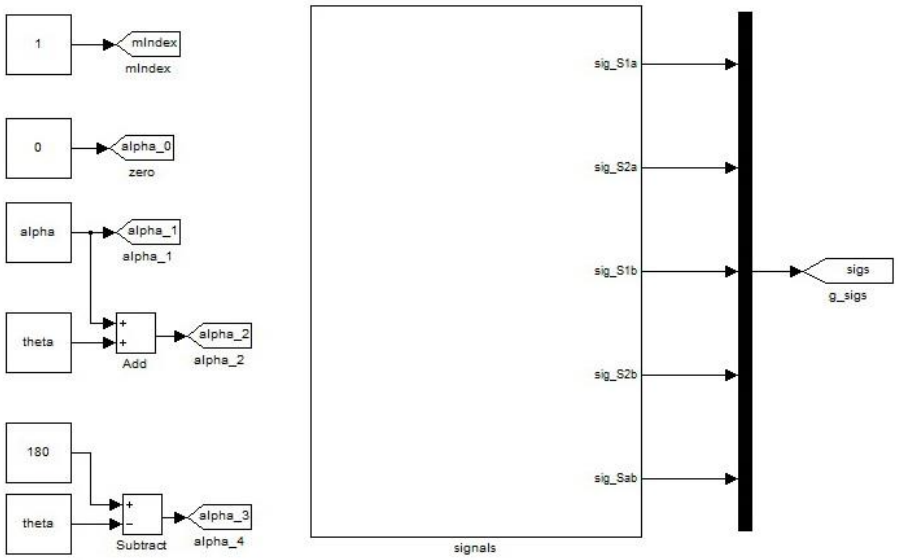


Fig. A.3: The gate signal blocks

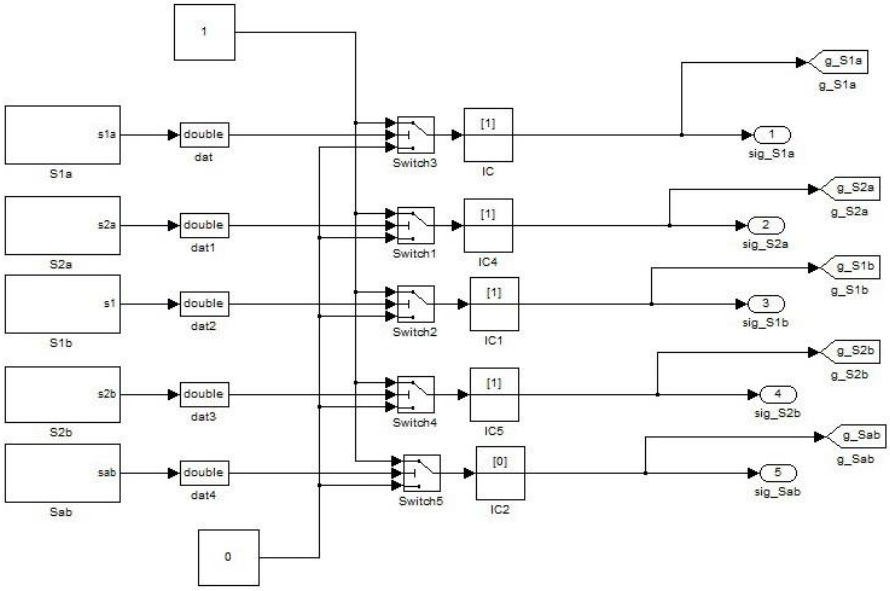


Fig. A.4: The controlling blocks

A.2.1 Control Signals Development

Fig.A.5 shows five gate signals that were developed via Simulink for the simulation purposes. A 50 Hz sine wave is used for the reference. Since the gate signals are repeated every one period (360°); therefore, it is convenient to generate these signals based on the polarity of the reference waveform i.e. the positive cycle (0° to 180°) and negative cycle (180° to 360°). For a five-level inverter, each cycle must be divided into four states whereby each of the state runs for maximum 45°. The positive cycle and the negative cycle blocks are shown in Fig.A.6 and Fig.A.7 respectively. It can be seen in Fig.A.6 that the blocks outputs four different scales from zero to pi (180°) whereas in Fig.A.7 the blocks outputs four scales from pi (180°) to 2 times pi (360°).

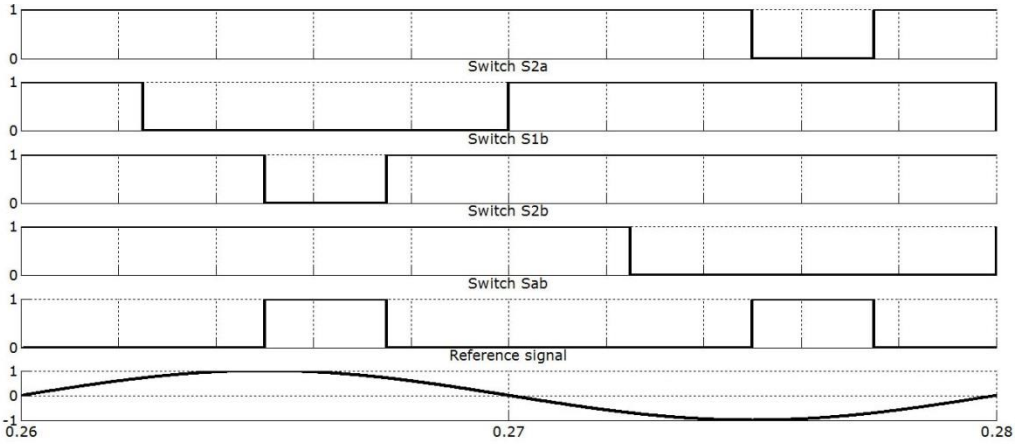


Fig. A.5: The control signals

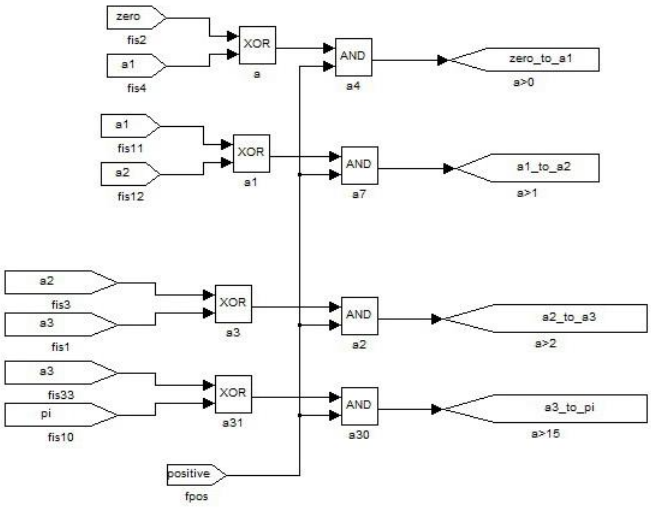


Fig. A.6: The positive cycle block

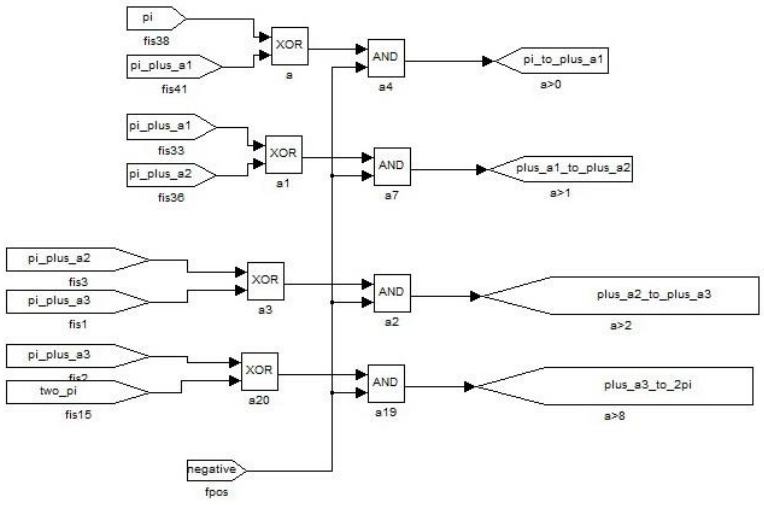


Fig. A.7: The negative cycle block

A.2.2 Variable Switching Angles (Positive Cycle)

The control signals are also developed for the variable switching angles capability (Fig. A.8) which enables the user to specify the value of the α and β (Fig.2-1). This is useful for harmonic elimination of the current waveform similar to the

approach exercised in SHE method. By expanding both blocks on right (Fig. A.8), yields Fig.A.9 and Fig.A.10 which blocks show details of how Simulink is programmed.

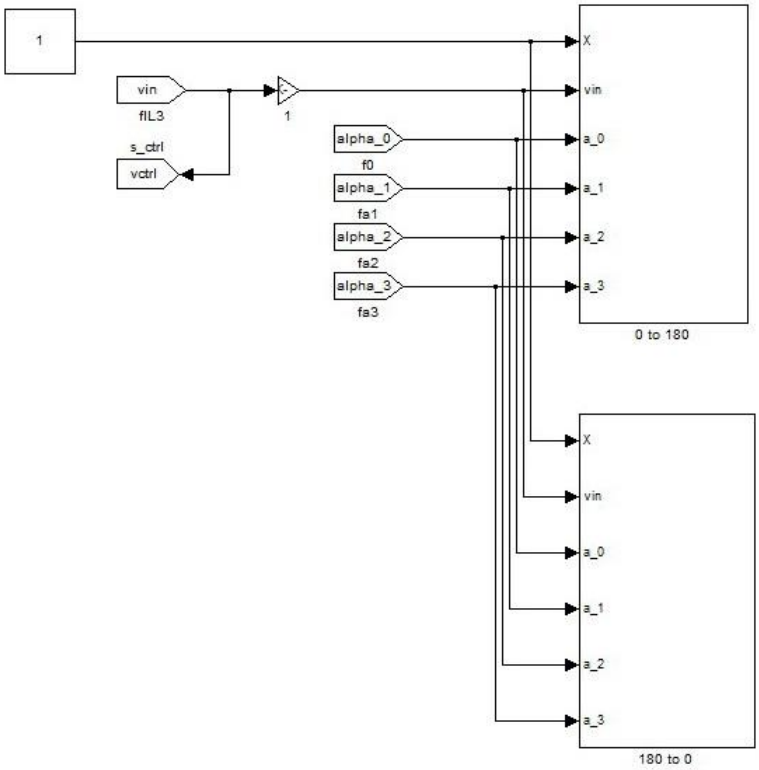


Fig. A.8: The positive cycle (variable switching angles)

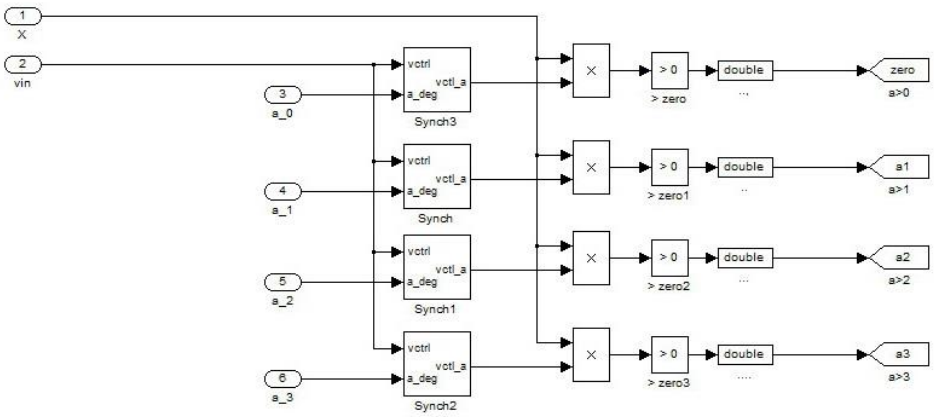


Fig. A.9: The positive cycle (zero to 180)

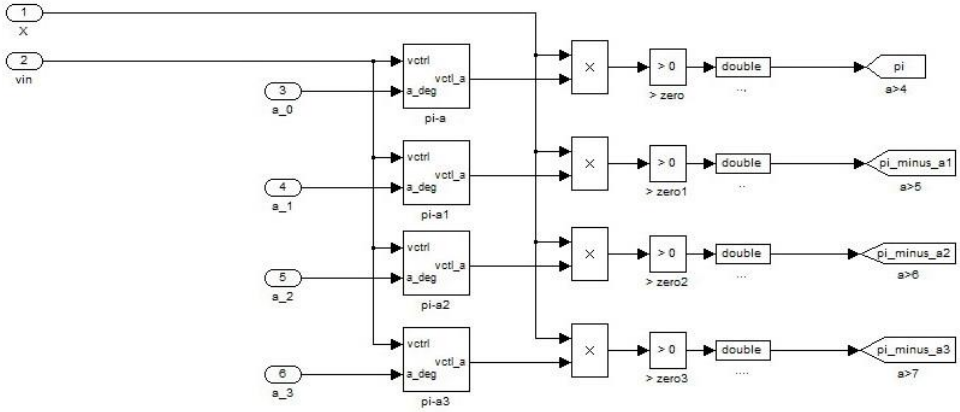


Fig. A.10: The positive cycle (180 to zero)

A.2.3 Variable Switching Angles (Negative Cycle)

Similarly, the variable switching angles control block for the negative cycle is shown in Fig.A.11. The figure when expanded is shown in Fig.A.12 and Fig.A.13.

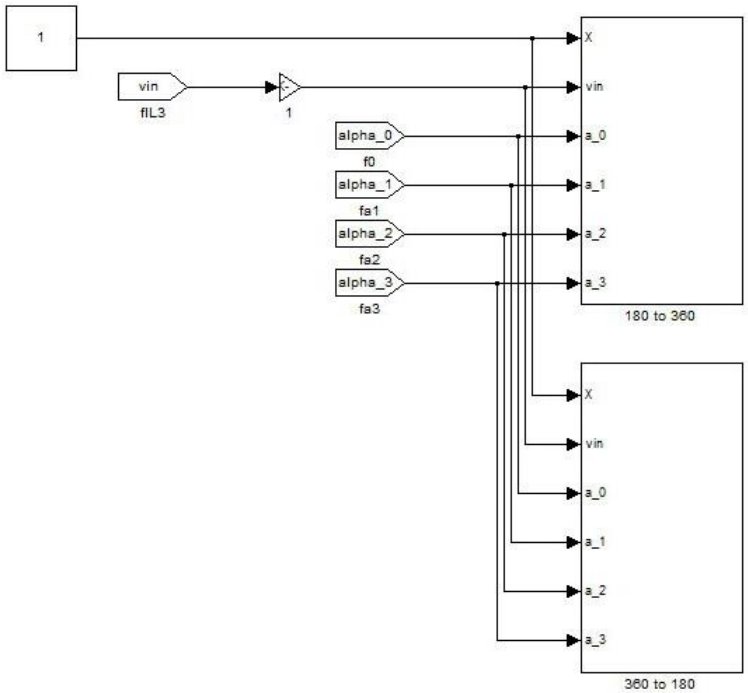


Fig. A.11: The negative cycle (variable switching angles)

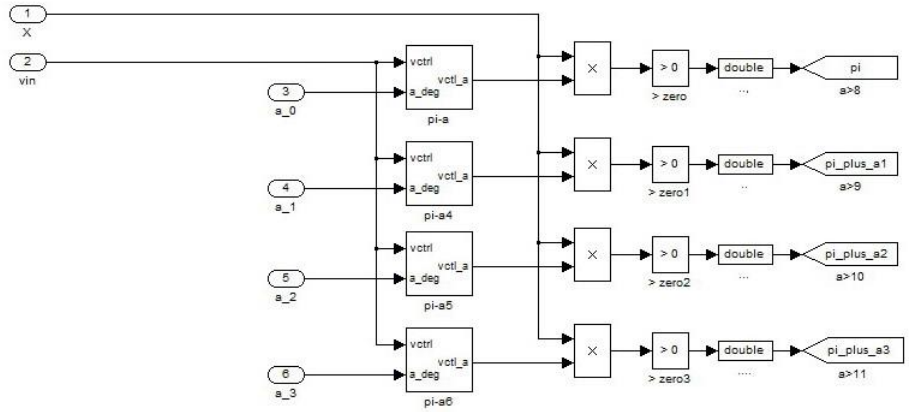


Fig. A.12: The negative cycle (180 to 360)

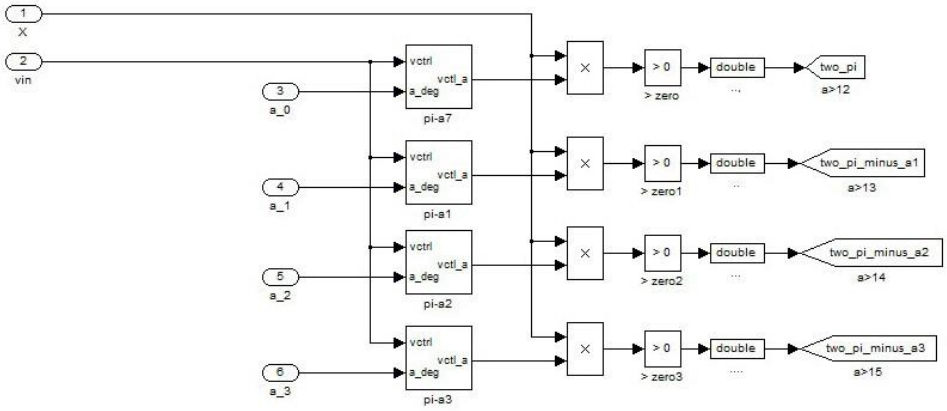


Fig. A.13: The negative cycle (360 to 180)

A.3 Logic signals

The final logic signals generated for the MCSI inverter are shown in Fig.A.14, Fig.A.15, Fig.A.16, Fig.A.17, and Fig.A.18 for switch S1a, S2a, S1b, S2b, and Sab respectively. The signals shown are for an open-loop control of the inverter.

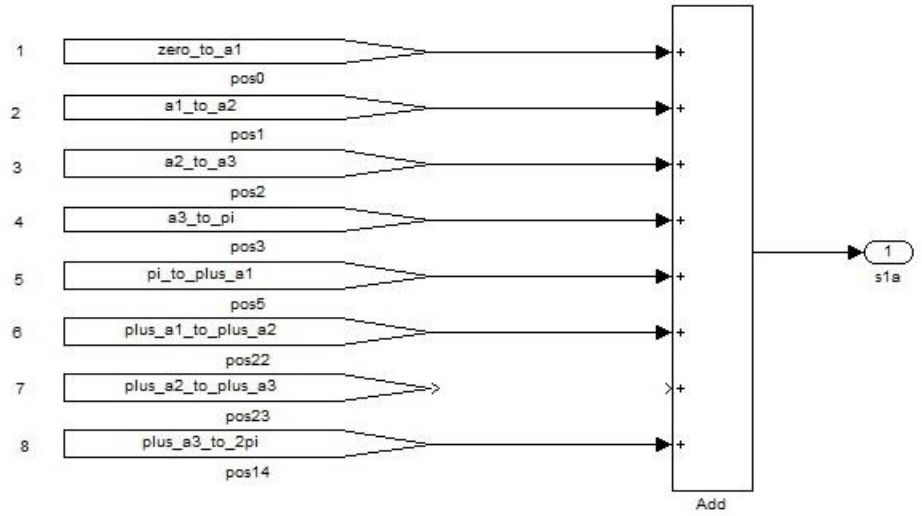


Fig. A.14: The logic signals of the switch S1a

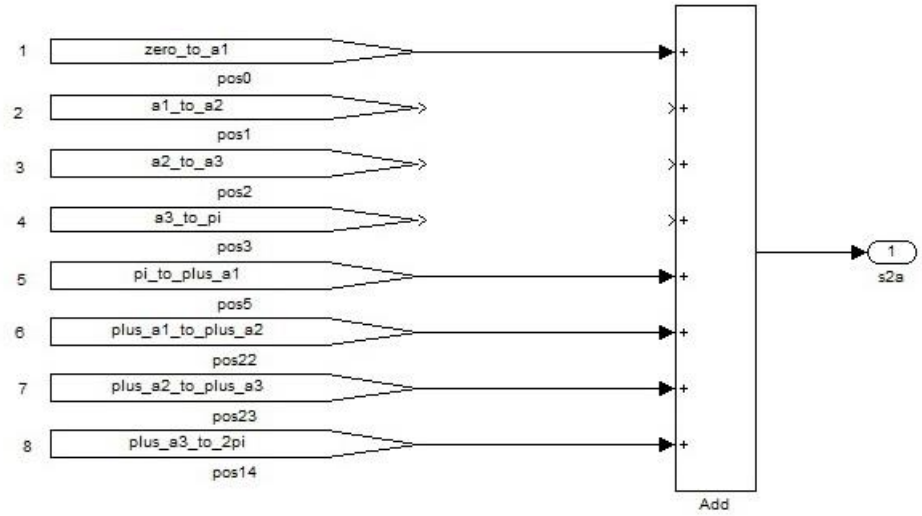


Fig. A.15: The logic signals of the switch S2a

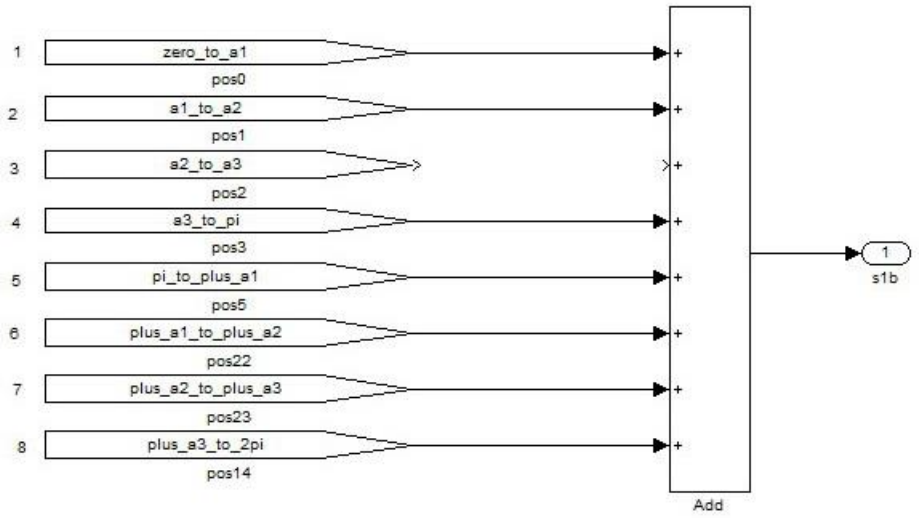


Fig. A.16: The logic signals of the switch S1b

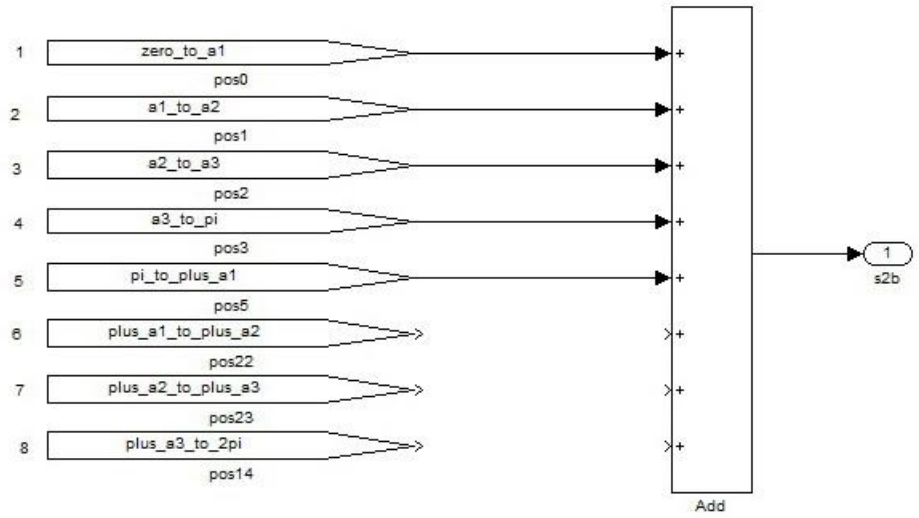


Fig. A.17: The logic signals of the switch S2b

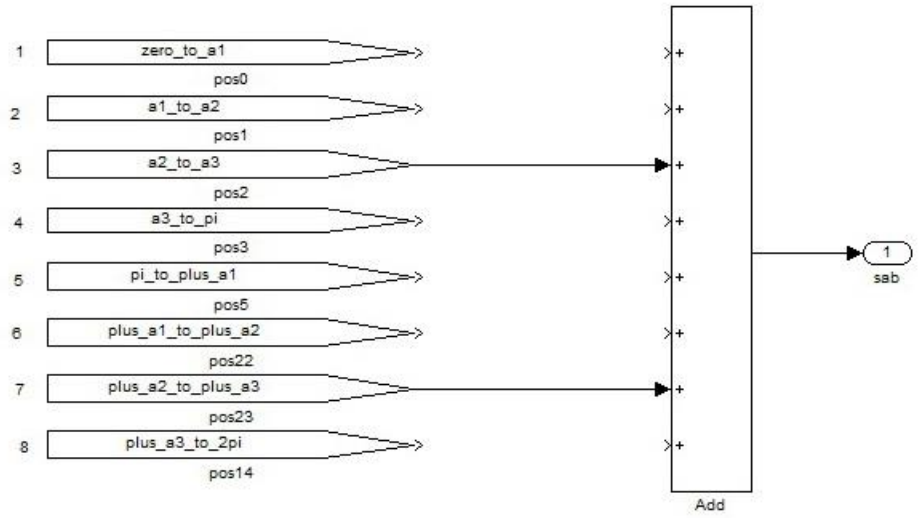


Fig. A.18: The logic signals of the switch Sab

Appendix B

FPGA Programming

Appendix B presents the VHDL programming of the FPGA board. The program shown is for the five-level MCSI with switch overlapped period of 3us. The resulted gate signals are captured and explained briefly.

B.1 VHDL Programming

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    15:13:31 08/26/2010
-- Design Name:
-- Module Name:    PWM5L_3u - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
-- library UNISIM;
```

```
-- use UNISIM.VComponents.all;

entity PWM5L_3u is
port
        (       CLK     : in std_logic;  -- 125MHz clock
                LED     : out std_logic;  -- led for display
                START : in std_logic;-- PWM on switch
                SwT1 : out std_logic; -- Top Switch 1
                SwB1 : out std_logic; -- Bottom Switch 1
                SwT2 : out std_logic; -- Top Switch 2
                SwB2 : out std_logic; -- Bottom Switch 2
                SwD1 : out std_logic);          -- Bidirectional Switch 1

end PWM5L_3u;
architecture Behavioral of PWM5e1_3u is

        signal count : std_logic_vector(18 downto 0); -- integer range 1 to 19
        signal slow_clk: std_logic;   -- slow clock
        signal clk_div : std_logic_vector (2 downto 0) := "000";
        signal ST1, SB1, ST2, SB2, SD1, LED1 : std_logic;

begin
----------------------- clock that makes slow clock go high only when MSB of
-----------------------clk_div goes up----------------
clk_division : process (CLK, clk_div)

begin
        if (CLK = '1' and CLK'event) then
        clk_div <= clk_div +1;
        end if;
        slow_clk <= clk_div(2);

end process;
-----------------------counter-----------------------
counting : process (slow_clk, count)

begin

if slow_clk'EVENT and slow_clk = '1' then
        if count < 312504 then
           count <= count + 1;
        else
           count <= "00000000000000000001";
        end if;
        end if;
```

```
end process;

------------------------ end counter-------------------------
----- add xtra 3us (46x64ns=2.944us) after turnoff
------------------------ Gate Signals --------------------

ST1_signal : process (count)

        begin

        if  count = 1 or count < 46 then     -- xtra 46 = 46x64 ns
                ST1 <='1';

        elsif count >= 46 and count < 39063 then
        ST1 <='0';

        elsif count >= 39063 and count < 234424 then
        ST1 <='1';

        elsif count >= 234424 and count < 273441 then
        ST1 <='0';

        elsif count >= 273441 and count < 312504 then
                ST1 <='1';

        end if;

end process;
-----------------
SB1_signal : process (count)

        begin

        if  count = 1 or count < 78172 then      -- xtra 46 = 46x64 ns
                SB1 <='1';

        elsif count >= 78172 and count < 117189 then
        SB1 <='0';

        elsif count >= 117189 and count < 156298 then
        SB1 <='1';

        elsif count >= 156298 and count < 195315 then
                SB1 <='0';

        elsif count >= 195315 and count < 312504 then
```

```
        SB1 <='1';

        end if;

end process;
-----------------
ST2_signal : process (count)

        begin

        if  count = 1 or count < 46 then        -- xtra 46 = 46x64 ns
                ST2 <='1';

        elsif count >= 46 and count < 156252 then
        ST2 <='0';

        elsif count >= 156252 and count < 312504 then
        ST2 <='1';

                end if;

end process;
-----------------
SB2_signal : process (count)

        begin

        if  count = 1 or count < 156298 then       -- xtra 46 = 46x64 ns
                SB2 <='1';

        elsif count >= 156298 and count < 312504 then
        SB2 <='0';

                end if;

end process;
-----------------
SD1_signal : process (count)

        begin

        if  count = 1 or count < 39109 then      -- xtra 46 = 46x64 ns
                SD1 <='1';

        elsif count >= 39109 and count < 78126 then
        SD1 <='0';
```

```
        elsif count >= 78126 and count < 117235 then    -- xtra 15 = 15x64 ns
        SD1 <='1';

        elsif count >= 117235 and count < 156252 then
                SD1 <='0';

        elsif count >= 156252 and count < 195361 then    -- xtra 15 = 15x64 ns
        SD1 <='1';

        elsif count >= 195361 and count < 234378 then
                SD1 <='0';

        elsif count >= 234378 and count < 273487 then    -- xtra 15 = 15x64 ns
        SD1 <='1';

        elsif count >= 273487 and count < 312504 then
                SD1 <='0';

        end if;

end process;
-----------------
LED1_signal : process (count)

        begin

        if  count = 1 or count < 150000 then        -- led 'on'
                LED1 <='1';

        elsif count >= 150000 and count < 312504 then    -- led 'off'
        LED1 <='0';

                end if;

end process;
-----------------
process(START, CLK, ST1, SB1, ST2, SB2, SD1, LED1)
begin

  if START = '1' then
    SwT1 <= ST1;
    SwB1 <= SB1;
    SwT2 <= ST2;
    SwB2 <= SB2;
    SwD1 <= SD1;
```

```
    LED  <= LED1;

  elsif START = '0' then

    SwT1 <='0';
    SwB1 <='0';
    SwT2 <='0';
    SwB2 <='0';
    SwD1 <='0';
  LED  <='0';

   end if;

end process;

end Behavioral;
```

B.2 Captured Signals

The logic signals shown in Fig.B.1 are captured in 5 periods (50 Hz line frequency modulation or 5 x 20ms). The exploded view of the signals (2.5ms/div) are shown in Fig.B.2 to expose the 3us overlapped period that is required to ensure smooth current flowing during switch turn-on and turn-off.

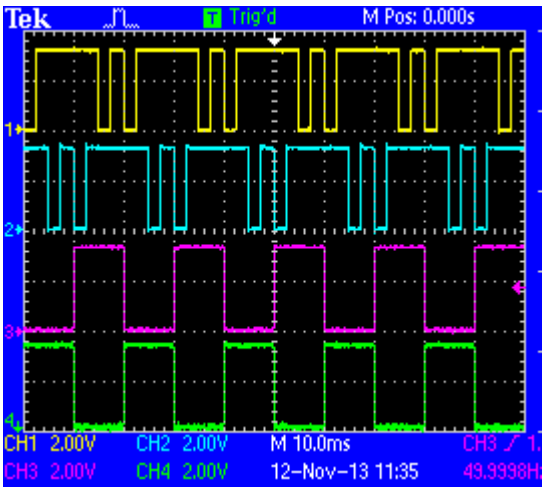


Fig. B.1: Logic signals of;
(Signal 1: Switch S1a); (Signal 2: Switch S2a)
(Signal 3: Switch S1b); (Signal 4: Switch S2b)

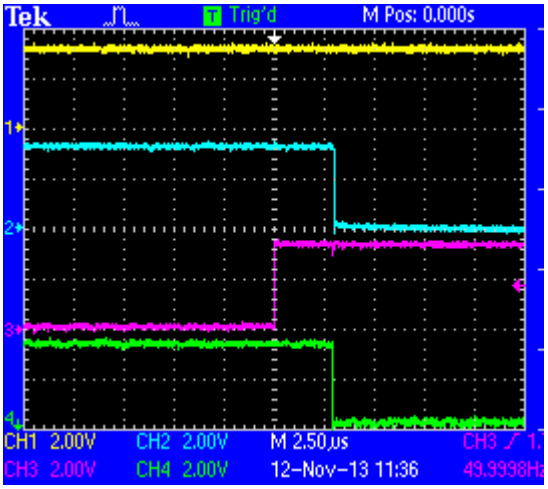


Fig. B.2: Overlapped period of 3us of;
(Signal 1: Switch S1a); (Signal 2: Switch S2a)
(Signal 3: Switch S1b); (Signal 4: Switch S2b)

Fig.B.3 shows the same signals from Fig.B.1 except for the fourth signal which belongs to the bidirectinal switch Sab. The same signals from Fig.B.3 are again shown in Fig.B.4 for much larger period (25ms/div) to demonstrate the consistency of the gate signals employed.

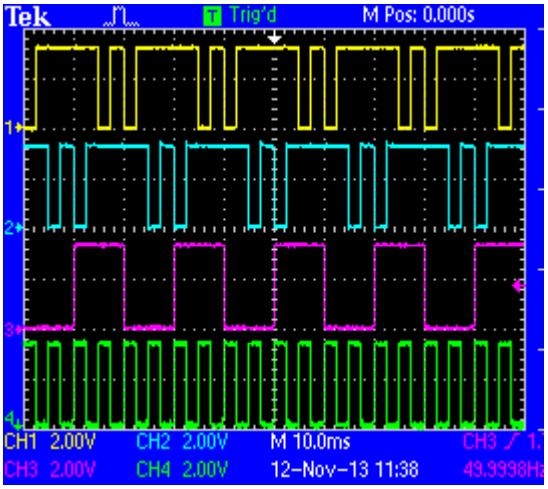


Fig. B.3: Logic signals of;
(Signal 1: Switch S1a); (Signal 2: Switch S2a)
(Signal 3: Switch S1b); (Signal 4: Switch Sab)

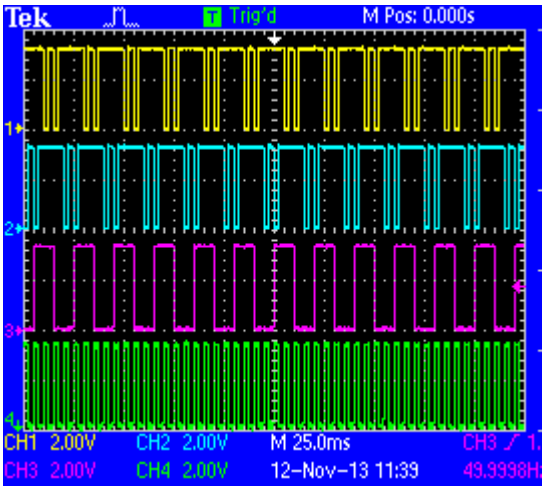


Fig. B.4: Logic signals in 25ms of;
(Signal 1: Switch S1a); (Signal 2: Switch S2a)
(Signal 3: Switch S1b); (Signal 4: Switch S2b)

Appendix C

Experimental Components

Appendix C describes most of the key components employed in the experiment. The schematics and relevant pictures are included where appropriate.

C.1 Inverter Test Circuit

The experimental circuit (Fig.C.1) has been designed to be able to work either as a five-level inverter or a nine-level inverter with minimum adjustments. The square box in the figure below shows how the 5-level experimental test was set-up. The main components as marked are an inductor (L1), four IGBT switches (Q2, Q3, Q5 and Q6), a bidirectional IGBT switch (Q4, D1, D2, D3, D4), a current supply and resistive load. Three pins connectors are used to connect the main circuit to the gate driver outputs.

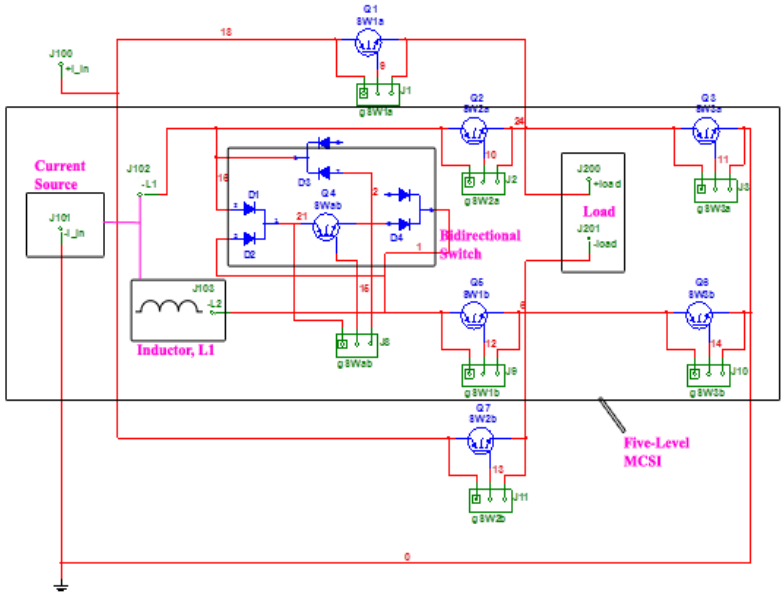


Fig.C.1: Schematic test circuit of the new 5/9-level MCSI

C.2 Gate Driver Circuit

The HCPL-316J (Fig.C.2) is an IGBT gate drive IC with isolated input and output circuit. At the input side, the TTL input logic levels allow direct interface with a microcontroller whereas a high speed internal optical link provides isolation to the power output circuit that can drives IGBTs with power ratings of up to 150 A and 1200 V (Fig.C.3). The input buffer IC, the output detector IC and the two optical channels are housed in the same SO-16 package that also features fault protection and isolated feedback system for circuit protection. Under normal operation, the input gate control signal directly controls the IGBT gate while LED2 remains off and a fault latch disabled. When a fault is detected, the output IC immediately begins a "soft" shutdown sequence; reducing the IGBT current to zero while transmitting fault status to the input buffer IC via LED2 where the fault latch disables the gate control input. Other features that provide constant IGBT protection are the Under Voltage Lockout (UVLO) and DESAT (VCE). The UVLO prevents the application of insufficient gate voltage during power-up by forcing the IC's output low. Once the output is in the high state, the DESAT detection provides IGBT protection.

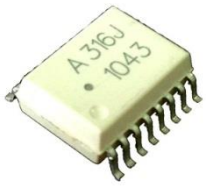


Fig.C.2: HCPL-316J

The schematic for a single gate driver circuit is shown in Fig.C.4. It can be seen that besides the two three-pin terminals; one that is connected to the controller output (JCtrl) and the other that is connected to the IGBT (JSw), there are also two two-pin terminals that are connected to an isolated dc/dc converter. The isolated dc/dc converter used is the muRata [98] NMH1215DC (Fig.C.5) whose provides two outputs of ±15V from a single input of 12V with the total load

cannot exceed 2 Watts. The rated efficiency is up to 86 %. The schematic for the final gate driver board is shown in the Fig.C.6.

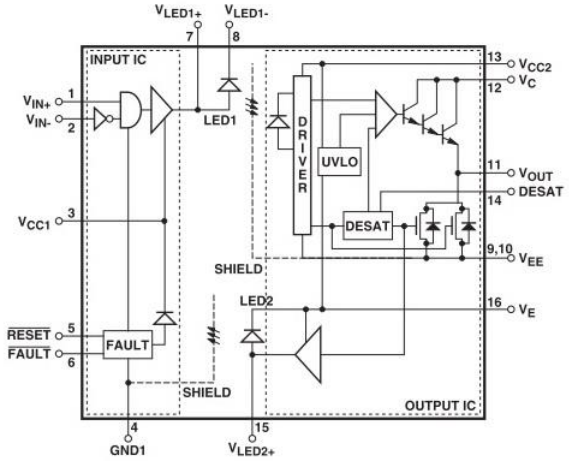


Fig.C.3: HCPL-316J IC inside components [99]

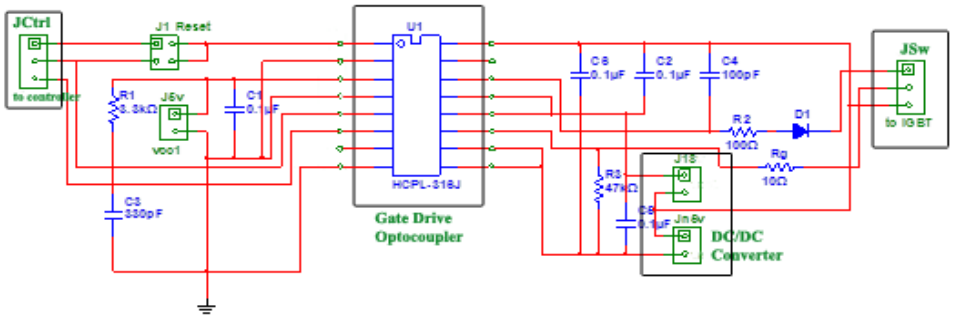


Fig.C.4: Schematic for the gate driver circuit

Fig.C.5: NMH1215DC

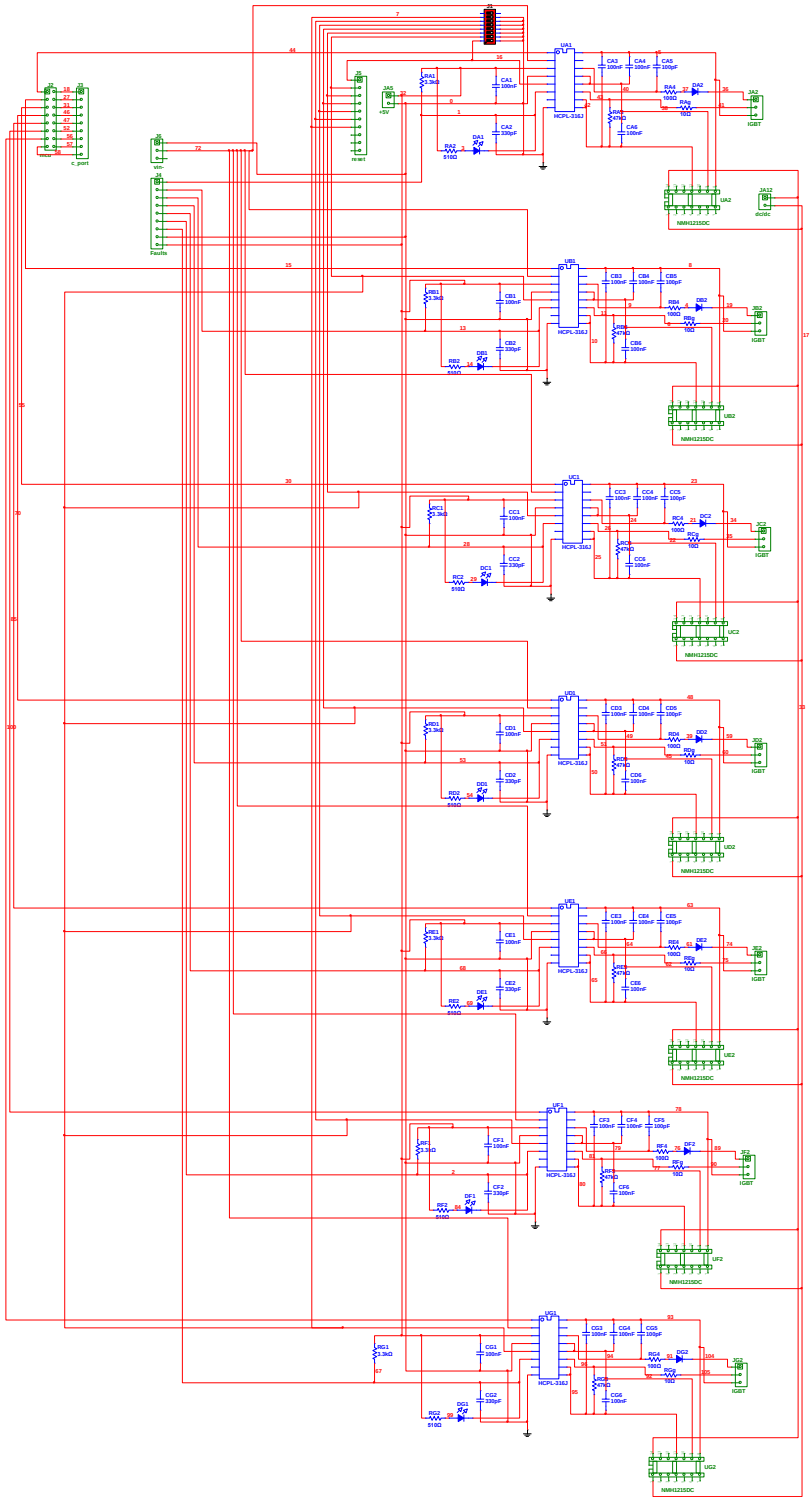


Fig.C.6: Schematic circuit for experimental MCSI Gate Driver

C.3 IGBT Switches

The IRGB30B60K (Fig.C.7) is an insulated gate bipolar transistor that benefits many uses such as the multilevel converter and motor control applications due to its rugged transient performance, low EMI and excellent current sharing in parallel operation. It features among others are;

- Low VCE (on) non punch through IGBT technology
- 10μs short circuit capability
- Square RBSOA (Reverse bias safe operating area)
- Positive VCE (on) temperature coefficient.
- Maximum junction temperature rated at 175°C.

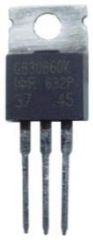


Fig.C.7: IRGB30B60K

C.4 Ultrafast Rectifier

The FESB16JT (Fig.C.8) are the ultrafast rectifiers that are used with the IGBT switch IRGB30B60K for a bidirectional switch formation. The rectifier specifications are;

Parameter	Symbol	Unit
Max repetitive peak reverse voltage	VRRM	600 V
Max RMS voltage	VRMS	420 V
Max DC blocking voltage	VDC	600 V
Max average forward rectified current (100 °C)	IF(AV)	16 A
Peak forward surge current at TC=100 °C	IFSM	250 A
Max reverse recovery time at IF = 0.5A, IR = 1.0A, Irr = 0.25A	trr	50 ns
Operating storage and temperature range	TJ, TSTG	-65 to + 150 °C

Fig.C.8: FESB16JT

C.5 Inductors

The employed inductors are custom built by Magtor Ltd. of Manchester, UK. Each of the inductors have four terminals which give three pre-determined inductances of 20 mH, 30 mH and 40 mH respectively (Fig.C.9). These inductors are rated at $600V_{RMS}$ and $15A_{RMS}$.

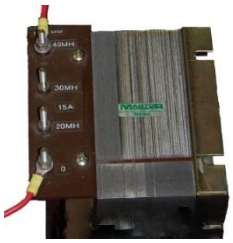


Fig.C.9: Inductor

C.6 DC Contactor

The Tyco Electronics' Kilovac EV200HAANA DC contactor (Fig.C.10) is used to connect the high current input source to the inverter circuit to avoid damaging effect of current arcing from the turning ON and OFF of the supply. The contactor's auxiliary contacts can be energized by a 9-36 VDC source with maximum inrush current of 3.8 A. The normal holding current is averaged at 0.13 A at 12 VDC or 0.07 A at 24 VDC. The rated operating voltage and the typical continuous current that this contactor can handle is 12-900 VDC and 500+ A respectively.

Fig.C.10: EV200HAANA

C.7 Main Power Supply

The Regatron's TopCon Quadro programmable DC power supply (Fig.C.11) offers full output control of voltage, current and power. This DC supply covers the voltage range of up to 100 VDC and the current range of up to 200 A. Its rated power is 16 kW.

Fig.C.11: Regatron Programmable DC power supply

C.8 DC Power Supply

The TTi EL302D (Fig.C.12) compact bench dual-output power supply is used to energized the DC contactor as well as to power up the isolated DC/DC converter for the gate driver board. The EL302D provides 2 x 30 V maximum output voltages rated at 2 A with 120 Watts maximum power.

Fig.C.12: EL302D Dual-Output DC power supply

C.9 Digital Oscilloscope

The Tektronix DPO2014 is a 100 MHz Digital Phosphor Oscilloscope with four analogue channels. Each channel can rate samples up to one Giga-Sample/sec with one Mega-Sample record length. Its waveform capture rate is 5000 waveform/sec.

Fig.C.13: Tektronix DPO2014

C.10 Current Probe

The Tektronix A622 clamp-on current probe uses a Hall Effect current sensor to provide a voltage output to oscilloscopes. The output voltage provided is either 10 mV or 100 mV for each ampere measured where the A622 can measure AC/DC currents from 50 mA to 100 A peak over a frequency range of DC to 100 kHz.

Fig.C.14: Tektronix A622

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