ASSESSMENT OF SINGLE PHASE SRM CONVERTERS FOR LOW POWER APPLICATIONS

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ABSTRACT

The switched reluctance machine (SRM) is the least expensive machine to produce yet it is very reliable. The drive system for an SRM has to be designed so that there is integration between the machine and the converter-controller configuration. This thesis represents a study relating to power electronic converters for single-phase switched reluctance machine drives with emphasis on cost implication of the converters. The study of the converters results in the proposal of a new converter concept based on minimizing the cost contribution of the dc link capacitor. By reducing the size of the capacitor, smaller and lighter SP-SRM drive is achieved. A detailed analysis and simulation of the proposed converter has been conducted and enabled a design guideline for the proposed converter to be laid out. A model of the SRM with hysteresis controller is developed. Consequently, components have to be chosen carefully to minimise voltage dip, component stress, and energy loss from the freewheeling resistor. To verify the operation of the new converter, tests were conducted on an experimental rig. The proposed converter has the ability to supply double the peak supply voltage to the machine winding. In addition, the arrangement of the capacitors and diodes in the voltage multiplier means that positive and negative voltage rails can be supplied to the machine, which is very useful in an SP-SRM drive. The high voltage allows fast magnetisation of the windings and enables the machine to achieve potentially high speed. Through the arrangements of the capacitors and diodes, the converter is able to handle recovered energy from the windings.

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I praise the enormous help and support given by my fellow UG lab mates, during the challenging practical work; among them John, Matthew, Jackie and others too many to mention here. Also to the electronics and mechanical workshop technicians for their perseverance and patience in tackling my requests for help.

This thesis is dedicated to my parents, who have always given me the strength and encouragement to follow my dreams, and never left me in doubt of their love for me. Finally, to my husband and children, I owe my deepest gratitude, respect and affection. Their love, dedication and prayers were always sources of my inspiration. I am glad that they can finally see what I have been doing all these years.

Terima kasih, Wahai Tuhanku yang Maha Pengasih Lagi Maha Penyayang di atas kejayaan ini...

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Abbreviations

Synonyms when talking in general terms

AC	Alternating Current
ADC	Analog to Digital Converter
ANN	Artificial Neural Network
BNC	Bayonet Neill-Concelman (connector)
DC	Direct Current
DIL	Dual-In-Line
DSC	Digital Signal Controller
DSP	Digital Signal Processor
DZ	Zener Diode
ECR	Electronically Commutated Machine
EMF	Electromotive Force
HV	High Voltage
HVIC	High-Voltage Integrated Circuit
IC	Integrated Circuit
I^2C	Inter-Integrated Circuit
I/O	Input/ Output
ICSP	In-Circuit Serial Programming
LC	Inductor-capacitor
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LRC	Inductor-Resistor-Capacitor
LVIC	Low-Voltage Integrated Circuit
MIPs	Millions Instructions Per second
p.u.	Per unit value
PCB	Printed Circuit Board
PIC	Programmable Integrated Circuit*
RC	Resistor-Capacitor
RLC	Resistor-Inductor-Capacitor

RCD	Resistor-Capacitor-Diode
RMS	Root Mean Square
SPICE	Simulation Program for Integrated Circuits Emphasis
SPMTM	Smart Power Module
SP-SRM	Single Phase Switched Reluctance Machine
SR	Switched Reluctance
SRD	Switched Reluctance Drive
SRM	Switched Reluctance Machine
TTL	Transistor-Transistor Logic

Synonyms when talking about power semiconductors

IGBT	Insulated Gate Bipolar Transistor
Mini-DIP	Mini- Dual In-line Package
MOSFET	Metal Oxide Surface Field-Effect transistor
SCR	Silicon Controlled Rectifiers

Synonyms when talking about control techniques

CGSM	Current Gradient Sensorless Method
DCR	Delta Current Regulator
HCR	Hysteresis Current Regulator
PWM	Pulse Width Modulation

Symbols

A	Aligned rotor and stator position
C	Capacitor
C_{snub}	Snubber capacitor
D_{Di}	Diode conduction time
D_{rect}	Rectifier diode
E	Energy
f_{source}	Supply frequency
$i(t)$	Instantaneous phase current as a function of time, t
$i(\theta)$	Instantaneous phase current as a function of rotor position θ

iM(θ)	Motoring current as a function of rotor position θ
iG(θ)	Generating current as a function of rotor position θ
i_m	Current in the main SP-SRM windings
i_r	Current in the SP-SRM auxiliary rotor coils
I_{DZ}	Maximum Zener current
I_p	Average load current
I_{upper}	Upper threshold of hysteresis current band
I_{lower}	Lower threshold of hysteresis current band
I_{max}	Maximum current
k_d	Duty cycle
L(θ)	Phase inductance
L_L	Leakage inductance of a bifilar winding
L_m	Inductance in the main SP-SRM windings
L_{min}	Minimum inductance value
L_{max}	Maximum inductance value
L_r	Inductance in the SP-SRM auxiliary rotor coils
m	Coil mutual coupling
m_p	Number of phase
n	Number of stages in a multiplier circuit
N_{steps}	Number of steps per electrical rotation
N_r	Number of rotor poles
P_d	Output power
q	Number of motor phases
r_{int}	Internal resistance
$r_{freewheeling}$	Freewheeling resistor
R	Effective resistance of the SRM converter circuit
R_m	Resistance in the main SP-SRM windings
R_r	Resistance in the SP-SRM auxiliary rotor coils
R_{dump}	Dumping resistor
R_{source}	Resistance of the power supply
S	Number of sensor used
S_r	Voltage ripple factor (of a voltage multiplier output)

t	Time
t_{delay}	Time delay
T	Switch
T_{inst}	Instantaneous torque
T_{max}	Peak torque
T_{off}	Turn-off angle
$t_{turn\text{-}off}$	Switching turn-off time
$t_{turn\text{-}on}$	Switching turn-on time
U	Unaligned rotor and stator position
V_c	Capacitor voltage
V_D	Voltage across the freewheeling diode
V_{DZ}	Zener diode voltage
V_N	Nominal DC supply voltage
V_s	Supply voltage
V_p	Average open circuit output dc voltage (of voltage multiplier)
V_{pk}	Peak value of the supply voltage
V_{max}	Maximum open circuit output dc voltage (of voltage multiplier)
V_{min}	Minimum open circuit output dc voltage (of voltage multiplier)
$V_{primary}$	Voltage across the primary windings
$V_{secondary}$	Voltage across the secondary windings
Q	Switching signal from J-K flip-flop
α_p	Rotor pole pitch
δV	Voltage ripple
θ	SRM rotor position/ angle
θ_O	SRM turn-on angle
θ_C	SRM commutation angle
θ_D	SRM dwell angle
θ_{step}	Rotor electrical travel per step
θ_{slot_min}	Minimum slot angle
θ_{res}	Resolution angle
θ_{p_shifts}	Phase shift angle

ψ	SRM flux linkage
τ	Time constant
ρ	Mean resistive volt drop due to resistance during θ_D
η	Efficiency of the machine
ω	Angular speed

CHAPTER 1
INTRODUCTION

1.1. Introduction

Switched reluctance motors (SRMs) are motors with a simple mechanical construction. The rotor is a device with no windings or magnets, whilst the stator is mostly made out of steel laminations forming poles on which series of coils are wound. A rotating magnetic field is produced when current is 'switched' between the phase coil windings in a sequential pattern. The magnetic circuit is subject to saturation and therefore the machine is highly non-linear.

In order for the machine to rotate smoothly the current switching must be precisely timed with the rotor position. Therefore, for proper control, some form of rotor position feedback is required. As long as the commutation is accurately controlled with respect to the rotor position angles, the machine is capable of reaching high speed with high efficiency. Also, the simple construction means that the machine offers low cost. However, the cost of the power electronics driving the SRM is high.

There was never a real breakthrough involving SRM technology in the mainstream market. Apart from the inherently non-linear machine parameters, other major hindrance to the advancement of the machine is high torque ripple and acoustical noise.

1.2. Advances in switched reluctance machine technologies

In the last decade there has been an increase in research to tackle the obstacles described above. Areas that have seen significant progress are in consumer products, automotive, aerospace and domestic appliances [2]. The reason is due to the need for

machines with high-grade performance, robustness to harsh conditions, rugged operation and economical prices [3, 4].

One of the growing markets for SRM technology is the automotive industry [1, 5, 6]. According to [1] the SRM is very prominent because it has a modular and rugged structure, wide speed range and insensitivity to high temperatures. The normally associated noise due to stator vibrations can be reduced by methods like high stiffness stator design [7] and active noise cancellation technique [8].

In the aerospace industry, the SRM is a main contender because it has the capability to achieve high rotational speed combined with high power density [9], reliability [10] and lower cost. There is an increasing interest in the concept of 'more-electric aircraft' due to commercial and environmental pressures. Once again, the simple SRM rotor design allows higher operating speeds and operation within harsh environment especially in high temperatures [11]. As far as power converters are concerned, weight, volume, efficiency and reliability are key considerations, and thus having the usual electrolytic capacitors becomes unsuitable [11].

There is also a rapid increase in SRM-based domestic products. Some popular ones are 'Maytag Neptune' washing machine by Emerson Electric Co. and 'DC05' vacuum cleaner by Dyson. Significant cost savings can be achieved at higher operating speeds.

An SRM cannot produce motion when it is directly connected to a voltage supply line, but instead relies on intelligent control for electronic commutation. The performance of an SRM is very much dependent on the applied control. For any specific application, the machine design and power converter must be designed as a whole [12]. The integration of SRM and the control devices is termed Switched Reluctance Drive (SRD) [13]. In a typical SRD, control of the machine torque is achieved by setting control variables according to calculated or measured functions [14].

Well known methods to control SRM current are hysteresis control (HCR), delta modulation (DCR) and voltage PWM control [15]. Many variations exist on

these basic schemes. In all cases, the most important variable is the turn-on and turn-off angles. During this period, the flux builds up from zero to its peak value.

In current hysteresis control, the switches are turned on and off based on specified set-point values, and a hysteresis band. A generally flat current waveform is maintained with ripple determined by the size of the hysteresis band and the bandwidth of the current regulator. At high speeds, the back-EMF may prevent the machine from reaching the maximum hysteresis current level, and therefore, as the rotor rotates, the current is defined by the changing inductance and the back-EMF (and this mode is called single-pulse mode). The problem with this method of control is that it suffers from variable switching frequency. Especially at low speeds, the uncontrollable high switching frequency may damage the switching devices used [16].

DCR is quite similar to HCR, in that the switching frequency is not fixed. However, there is maximum current reference value which causes the switches to turn-off if exceeded. DCR methods will limit the maximum switching frequency but at the expense of increased current ripple.

In voltage PWM control, the switching frequency is fixed. There is no closed-loop control of the instantaneous current. Therefore, there is current limiting function provided for safety and protection. Although there is constant switching frequency and small ripple, the system is sensitive to parameter variation and this could compromise the system response.

For targeted domestic appliances, hysteresis control is the simplest and most cost-effective method to be implemented. In all of these SRM control methods, the rotor position sensor becomes the most important variable. As long as the commutation can be accurately controlled with respect to the rotor position, the SRM can become most efficient.

As far as the switching devices are concerned, the choice of which to use depends on the requirement of the application. Generally, for applications requiring higher switching frequencies, MOSFETs are used, whilst IGBT's are used for higher

voltage applications. However, quite recent progress power electronics devices means there are MOSFETs that can operate at very high voltage ratings.

The process of developing a new domestic appliance product is quite elaborate, from designing the machine parameters, to the power converter as well as the control strategies. Although the SRM can be the most economical machine to be built mechanically, one thing that has kept this machine type from widespread use is that there is no standard converter bridge available.

In February 2005, Fairchild Semiconductor has introduced the first Smart Power Module (SPMTM) [17] which is designed for driving low power inverter driven SP-SRM application like a vacuum cleaner [18]. Fairchild describes the module as, "The power module which integrates a high-voltage IC (HVIC) and low-voltage IC (LVIC), IGBTs, fast recovery diodes and a thermistor in an ultra-compact Mini-DIP package...". It is claimed that the module is capable of reducing the power circuit by up to 40%. This compact solution is one of the most recent developments in solving the cost competitiveness of this topology.

Similar advances in SRM technology are very much welcomed in order to maintain the competitiveness of SRMs in consumer oriented products, specifically domestic appliances. Home appliances buyers do look at product prices and desirable features when making choices. Therefore, any new designs in SRD for domestic consumers should consider these compromises as long as they meet the consumer needs. SRM has been concluded to have superior performance compared to a comparable induction machine [19] and that is a motivation.

1.3. Cost considerations for SRM drives

In the selection of an SRM motor and drive for any application, the main concerns are performance and costs. Many novel approaches to SRM drives have focused on reducing the cost through topological and control modifications [20]. Topological modifications involve the reduction in the number of components, namely the switches in the converter circuit. New control algorithms are then proposed which take into account the reduced number of components, to produce the desired speed-torque output.

Some of the common features of low cost motor drives that would be desirable by industry would be minimal number of controllable switches, thus minimal cost of the attendant circuits such as gate drives and logic power supplies, and cooling mechanisms [21]. Low cost motor drives would also be required to have the smallest volume, weight and cost of the power electronics and controller.

To address this issue, single-switch-per-phase converters have been proposed [22-26] and are most suitable for low cost applications due to the relatively low component count and drive simplicity [27]. While being the most cost effective circuit, single-switch-per-phase converters face challenges such as unability to provide four quadrant operation as well as wide variable speed control. To achieve this, two-switch-per-phase converters have also been proposed [28].

In a typical SRM converter, the components generally involved are capacitors (usually to function as a dc link storage device), diodes and switches. To illustrate the cost implication to the converter, the average prices of these components (from three major electronic distributors) are compared in Table 1-1.

	Price		**% change in price**
	100V	**600V**	
Capacitor (aluminium)	66.22	75.05	+13
MOSFET	0.22	0.26	+17
IGBT	0.71	0.52	-26
Diode	0.20	0.16	-18

Table 1-1 – Cost (average price in British Pounds) comparison between aluminium electrolytic capacitor, MOSFET, IGBT and diode (components are chosen for equal power ratings in case of devices and equal energy storage for capacitors)

From the table above, it can be generalised that the cost of components will increase with the voltage. The increase in price for capacitors and MOSFETs if used as the switching device is large. Table 1.1 shows also that the dc-link capacitor is by far the most expensive component in an SRM drive. Therefore, in order to reduce any converter cost, it would be wise to take into account the cost contribution from a capacitor as well as the MOSFET. Also, for high voltage applications, there is still the choice of replacing the MOSFETs with suitable IGBTs at a reduced cost. In

addition, cheaper capacitors tend to be smaller, and lighter, which are desirable features in low cost motor drives.

An established method commonly applied in high voltage applications is used as a basis for rearranging the capacitors to propose a new converter design. The usage of a voltage multiplier circuit is further investigated to provide justification that the topology is applicable for SP-SRM drives.

1.4. Voltage multiplier in machine applications

Generally, an SRM application needs a rectifier of some sort to convert the ac supply to suitable dc for use by the machine. Normally, this will involve an electrolytic capacitor connected to the output of a diode bridge rectifier circuit. The capacitor will be charged to the peak rectified voltage and energy is then provided to the load, while the capacitor is always being charged.

If the components are rearranged like in Figure 1-1 a voltage multiplier circuit is created. This circuit configuration is one of the most effective and a popular way to generate high voltages at relatively low currents. The basic circuit was first introduced by Cockroft and Walton in 1932 [29], and because of this, the circuit is also called Cockroft-Walton voltage multiplier circuit.

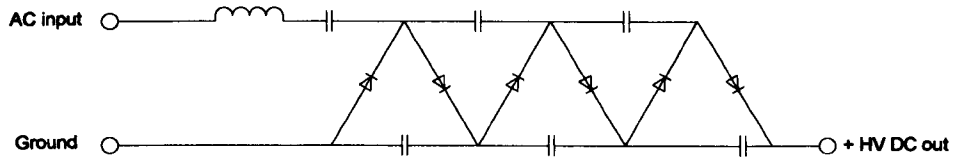


Figure 1-1- Typical arrangement of the Cockroft-Walton multiplier circuit

Voltage multiplier circuits have been popular for applications in laser systems, power supplies, particle accelerators, x-ray systems and many other applications that utilise high voltage DC. However, in machine applications, particularly for the SRMs, the circuit has not been used previously.

1.5. Objectives and contribution to knowledge

The objectives of this work were:

1. Overview of state of the art converter topologies for SP-SRM drives up to 1kW.
2. In depth evaluation and comparison of all SP-SRM converter operation by simulation.
3. Propose a novel SP-SRM converter topology demonstrating/showing reduced cost.
4. Critical assessment of the proposed SP-SRM converter topology using simulation.
5. Experimental verification of the proposed SP-SRM converter and comparison with standard SP-SRM converters.

All the objectives of the work has been completed and shown in the chapters of this thesis. The following are believed to be new areas of work, previously unpublished by other authors:

1. State of the art family tree of SP-SRM converter topologies.
2. Application of voltage multiplier topologies to SP-SRM drive.
3. Introduction of positive and negative voltage rails to SP-SRM operation.
4. Reduction of SP-SRM cost by focusing on capacitors as the main cost driver.

1.6. Overview of thesis

The chapters of this thesis describe the theory and simulation results of the state of the art SP-SRM converter topologies, as well as the experimental results of the proposed novel SP-SRM converter. Detailed information regarding the hardware and software of the electrical and electronics circuits is also provided.

This chapter provides an introduction to general SP-SRM drives, with brief description of the SRM, its application, and control methods. **Chapter 2** provides a more detailed insight into the SP-SRM including torque production, starting methods and operation modes. **Chapter 3** introduces the family tree of SP-SRM converter

topologies. A detailed comparison of all available topologies was made, with description of each operation mode. Each topology is then critically assessed in **Chapter 4**, based on the same simulation criteria, to compare the performance. The benefits, drawbacks and limitations of each converter are investigated. The investigation will also address the differences in SRM performance when considering static and variable machine reluctance.

Chapter 5 is dedicated to the proposed novel SP-SRM converter. It includes a theoretical analysis of the converter as well as its critical assessment based on simulation. **Chapter 6** is the experimental implementation of the proposed converter in order to verify its operation. All related waveforms and other practical results are included in this chapter. A detailed description of the experimental set-up is provided in Appendix A with related pictorial description in Appendix C. Appendix B shows the flow of the controller software. **Chapter 7** concludes the work and provides an overall assessment of the different SP-SRM converter topologies.

CHAPTER 2
SWITCHED RELUCTANCE DRIVES

This chapter gives an introduction to SRM drives. In Section 2.1, there will be a discussion on the background of SRMs, which includes the machine history, some description of the machine, as well as the advantages and disadvantages compared to other machine types. The general equation for an SRM is discussed and the relationship between the applied voltage and the machine speed is provided. The production of torque is also discussed. Section 2.2 continues with the rational for choosing single-phase machines as opposed to three phase machines. The next section, 2.3, will discuss the problem of single-phase SRM starting. A few self-starting methods are highlighted. Then, Section 2.4 will discuss the rotor position estimation techniques. Section 2.5 discusses briefly the operation of the 'classical' SRM converter topology. This will include some discussion on the demands for the converter and touches briefly on the control techniques that are normally applied. Section 2.6 concludes the chapter.

2.1. Switched reluctance drives technologies

The interest in the field of conversion of mechanical energy to electrical energy by electromagnetic means was first demonstrated by the British scientist, Michael Faraday in 1821 [30]. Since then, a large variety of motor designs have emerged, and one of the results of this is the SRM.

2.1.1. History and the future

The SRM is the term used to describe a machine that operates by switching of the phase currents through a variable reluctance magnetic circuit. SRM is also known as the Electronically Commutated Machine (ECR) [31]. The term 'switched

reluctance' was first used by Nasar in 1969 [32] to describe the machine. However, the most common terminology is SRM.

The SRM is basically a stepper motor with a different control method, and has different performances and applications. The modern SRM concept, which involves the electronic commutation of the machine based on the rotor position feedback, was described in [33, 34]. The SRM control was achieved by using thyristors which were the only power semiconductor available at that time that could cater for the relatively high current and high voltage type of control needed for the SRMs.

During the period of the 1970's, along with the development of fast switching devices, concepts of the SRM were further developed [35]. Since then, there have been massive developments of the SRM involving both the machine design as well as the machine control. Nowadays, power semiconductor technologies such as power transistors, IGBTs and power MOSFETs are available to fulfil SRM power requirements. The progress in research involving SRMs can be demonstrated by the graphs in Figure 2-1 and Figure 2-2 showing the trends in the publications and patents involving the SRMs from the 1980's until now [36].

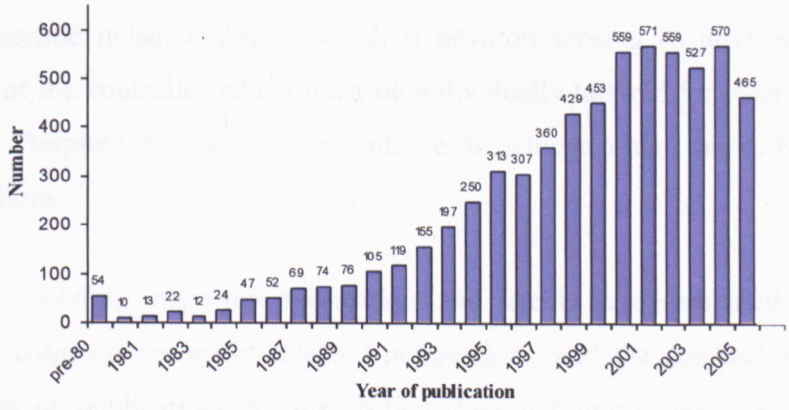


Figure 2-1- Publications on SRMs (up to 9th February 2006)

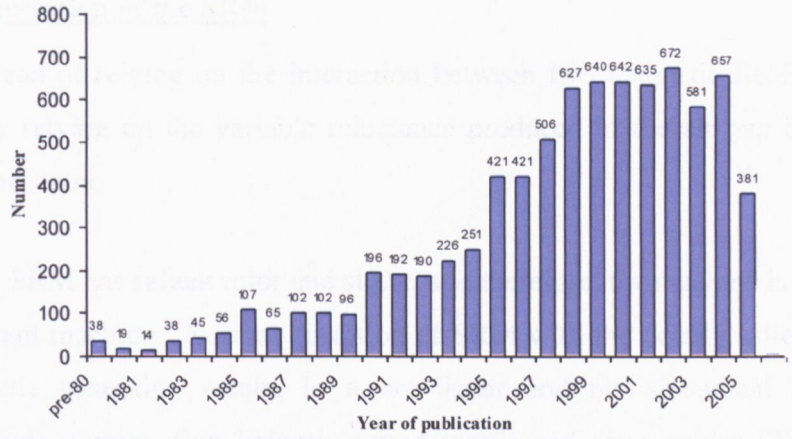


Figure 2-2- SRM patents recorded (up to 9th February 2006)

The graphs show that the research interest in SRMs have increased dramatically since the 1980s. By 2005 the number of publications has increased by about 57 from a total of 10 publications in the 1981. A similar trend is demonstrated in Figure 2-2 showing the number of SRM patents granted.

Many companies have built prototype SRM drives for test and evaluation purposes, but very few of these made it to the market. A few existing examples of SRM based commercial product is the Maytag Neptune® washing machine produced by Emerson Electric Company and vacuum cleaners produced by Ametek, LG or Dyson [37]. Miller [15] suggests that the reasons for this unpopularity are the high levels of acoustic noise, tooling cost, shaft position sensing requirement, and the complexity of the controller which must be individually tailored for each design and application. Despite that, the machine continues to achieve a high rate of filed patents and publications.

In this section, only a few publications and patents have been cited. This is by no means a complete record of relevant publications, and the non-inclusion of any other patents or publications in this section does not imply that it is considered unimportant. The ones cited here are considered sufficient to describe the progress of the SRM until the present time.

2.1.2. Description of the SRM

Instead of relying on the interaction between two magnetic fields, the SRM operates by relying on the variable reluctance produced in the air gap between the rotor and the stator.

An SRM has salient rotor and stator, and therefore, the machine is said to be a doubly-salient machine. Normal operation of SRM with the doubly salient structure and magnetic saturation results in a non-linear and non-sinusoidal relationship between phase current, flux linkage, output torque and rotor angles [38]. For the purpose of this work, the objective of which is mainly focused on SRM converter technologies, the machine is assumed linear. Therefore, all relationships between phase current, flux linkage, output torque and rotor angles are assumed to be sinusoidal. This assumes that the flux is present only when the rotor is producing positive torque, and is zero when rotor is producing negative torque. By making this assumption, the simulation is assuming no saturation in the machine and the machine works like a resistive load.

The simplest form of a single-phase SRM having two stator poles and two rotor poles (called a 2/2 motor) is illustrated in Figure 2-3. Other combinations such as 4/4 and 6/6 are equally possible. The stator has two projecting poles (otherwise called salient poles), that terminate at a central bore. In Figure 2-3 the poles shown are 180° apart. The stator and rotor are both formed by laminations of ferromagnetic materials. Energising coils are wound around each of the stator poles. When these coils are energised by applying a voltage to them, temporary magnetisation of the stator poles will occur. These attract the rotor thereby imparting a torque on the rotor.

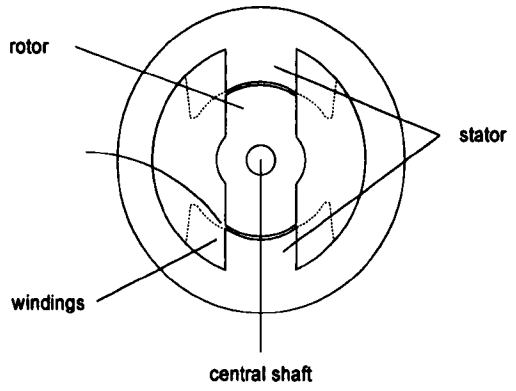


Figure 2-3- A 2/2 SP-SRM

The movement of the rotor is described in Figure 2-4. Here it is assumed that the rotation is clockwise. In (a) the stator coils are energised until the poles are in the fully aligned position (b). At the instant when the rotor is at or past this position, the windings are de-energised, causing the rotor to freely rotate due to inertia. If the coils are not de-energised at this moment, a negative torque would be applied to the rotor and the direction of rotation will be reversed. At (c), the windings have been de-energised and the rotor will move freely until it reaches the unaligned or the minimum inductance position shown in (d). The rotor inertia will rotate the rotor until it reaches the position shown in (a) where the rotor is energised again, and the cycle continues.

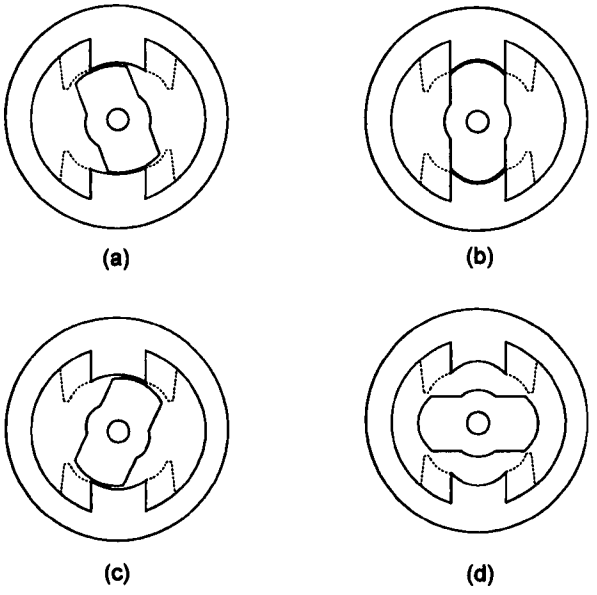


Figure 2-4- Movements of an SP-SRM

Figure 2-5 shows the starting torque against angular rotor displacement for one complete revolution. In the figure, the SP-SRM rotor position has been included to

enable visualisation of the rotor movements in relation to the starting torque curve. It can be seen that the machine only develops torque in the positive direction between points 2 and 4. Therefore, for the machine to rotate in the positive direction, the exciting current would need to be supplied between these positions. If the machine is excited when the rotor is between the positions 5 and 6, the torque produced would be in the opposite direction. Preferable, the machine should not be excited in positions between 1 and 2 and 4 and 5. This is because, at these positions, virtually no torque will be produced. Between position 1 and 2, the inductance is minimum, and the rotor is in the unaligned position. Between position 3 and 4, the inductance is maximum and the rotor is in the aligned position. From the curve, if the machine rotates with constant current in the windings, the positive and negative torque cancels, and the average torque becomes zero over the complete cycle. Therefore, it is essential that the machine operates in the region of positive torque if only positive torque is desired. The current must be switched off when the poles are separating to avoid negative torque impulses.

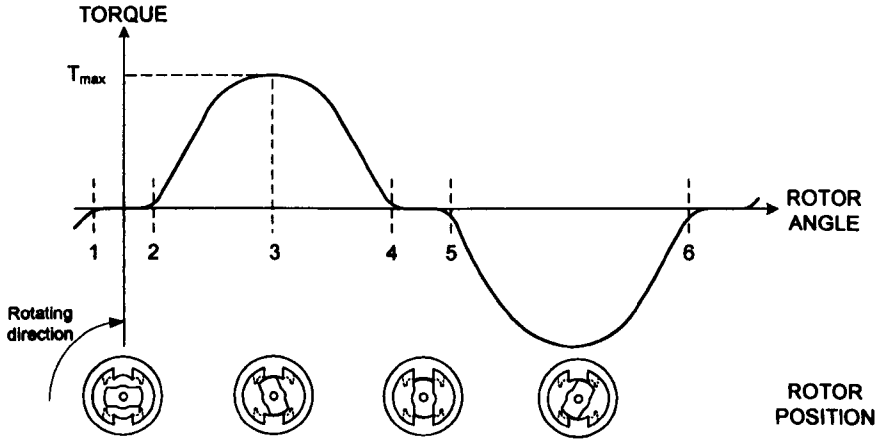


Figure 2-5- Starting torque vs. angular rotor displacement

Due to the tendency for the rotor to stop at the positions where no starting torque can be developed, methods for self-starting for SP-SRM have been researched and this is described in Section 2.3.

From the description of the machine above, a prime feature of the SRM is its physical construction. The motor is simple and eliminates the need for permanent magnets, brushes and commutators. Therefore, it can be maintenance-free. The machine is the only motor with salient poles in both rotor and the stator. For an SP-

SRM, this makes it potentially small size and result in efficient use of materials, while achieving low manufacturing costs [39]. This small size results in high energy density per unit volume. Windings only on the stator reduce the heat generation and makes cooling relatively easy. The SRM construction is considered rugged and it would be suitable for use in a harsh environment such as high vibration and temperature.

As the current is unipolar, the controller can be made simple regardless of torque direction. This means solutions with minimised switch number can be realised.

One major disadvantage of the SRM is that the machine requires information on rotor position for commutation. This will usually include sensors at a cost or include position sensorless methods. As the inductance varies with the rotor position, the torque is not constant causing a high torque ripple content. Due to the vibrations during operation, some acoustic noise control has to be considered. Also, the SP-SRM will almost certainly need an inverter for it to operate. Depending on the applications, the SRM can sometimes require complex electronics for control and power conversion.

Although the SRM has many outstanding characteristics, many of these can be equally achieved by using more conventional motors. With the advent of power electronic technologies and computing methods, all the other motor technologies have also made some progress, which made it more challenging for SRMs to compete. Only in certain applications where the special characteristics unique to the SRM could be well suited to the application, it stands a chance of success. For example, in a domestic fan blower, the noise usually associated with the SRM is negligible compared to the fan normally noisy application, and therefore SRM could be the more economical choice.

2.1.3. General equations of an SRM

In general, the equation of a voltage-controlled SRM is given by,

$$v = ir_{\text{int}} + L(\theta)\frac{di}{dt} + i\frac{dL(\theta)}{d\theta}\omega \qquad (2\text{-}1)$$

where v is the machine applied voltage, ir_{int} represents the voltage across the internal resistance (r_{int}) of the machine, $L(\theta)\frac{di}{dt}$ represents the voltage across the winding of the machine where the inductance is variable depending on the rotor position, and the third term, $i\left(\frac{dL(\theta)}{d\theta}\right)\omega$ represents the machine back-EMF (produced by the current and the rate of change of inductance as a function of rotor position at an angular speed).

During the period of conduction, the current is switched on and off (chopping) based on the position of the rotor. However, for the purpose of this work, it is assumed that an average value of current is applied, and the current pulses are shown to have a flat top. From equation 2.1, if the current is assumed constant, the term $L(\theta)\frac{di}{dt}$ is equal to zero. As the term ir_{int} is also assumed negligible, the back-EMF of the machine will be equal to the applied voltage, v. Therefore, for a voltage-controlled machine, the applied voltage will define the speed. If the voltage is increased, the speed will react to match the supplied voltage.

2.1.4. Torque production

The instantaneous torque, T_{inst} of an SRM at any given rotor position, θ is given approximately by,

$$T_{inst}(\theta) = \frac{1}{2}i(\theta)^2\frac{dL(\theta)}{d\theta} \qquad (2\text{-}2)$$

where $i(\theta)$ is the instantaneous phase current, $L(\theta)$ is the phase inductance and θ is the rotor position. The term $i(\theta)^2$ is always positive, and this shows that the torque is independent of the phase current direction. Therefore this means the current through the machine windings can be unipolar. This is the unique difference of an SRM compared to most other machines.

Positive (motoring) or negative (regenerating) torque can be achieved by switching the winding currents on and off at appropriate instances during the inductance cycle. Figure 2-6 shows the positions of current pulses for torque generation in the SRM.

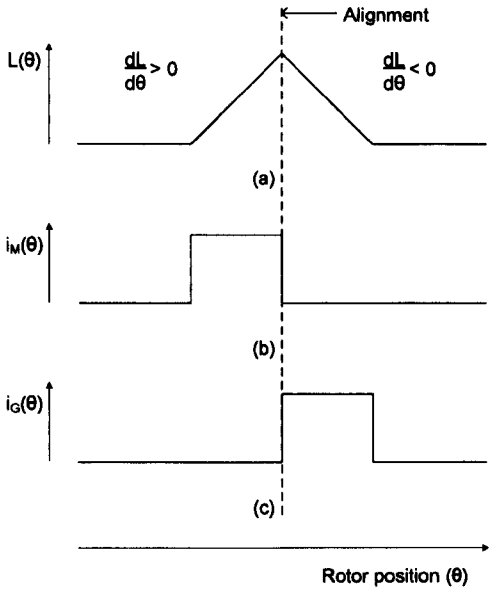


Figure 2-6-.Current pulses for torque generation (a) idealised phase inductance L(θ); (b) motoring current ($i_M(\Theta)$); (c) generating current ($i_G(\Theta)$)

Figure 2-6(a) shows the idealised phase inductance as a function of rotor position. For motoring operation, the current, $i_M(\Theta)$ is turned on while the rotor is approaching the aligned position, as shown in Figure 2-6(b). In this region, the phase inductance is increasing ($\frac{dL}{d\theta}>0$), and the torque acts in the direction of rotor motion. For generating, the current, $i_G(\Theta)$ must be on while rotor poles are being pulled away from the aligned position, as shown in Figure 2-6(c). In this region, the phase inductance is decreasing ($\frac{dL}{d\theta}<0$), and the torque opposes the rotor motion.

In a simple 2/2 machine as described before, the coil inductance, L varies with the rotor position, θ. As the rotor approaches the aligned position, the inductance is increasing, and positive motoring torque is produced. In Figure 2-7 this is between positions 1 and 2. The torque curve has been simplified to a positive and negative polarity square wave. At position 2, the rotor and stator are fully aligned. This

defines the start of overlap (overlap is the position where the rotor coincide partly or wholly with the stator). At position 3, the overlap ends. As mentioned in Section 2.1.2, the cycle of torque within one current pulse is called a *stroke*.

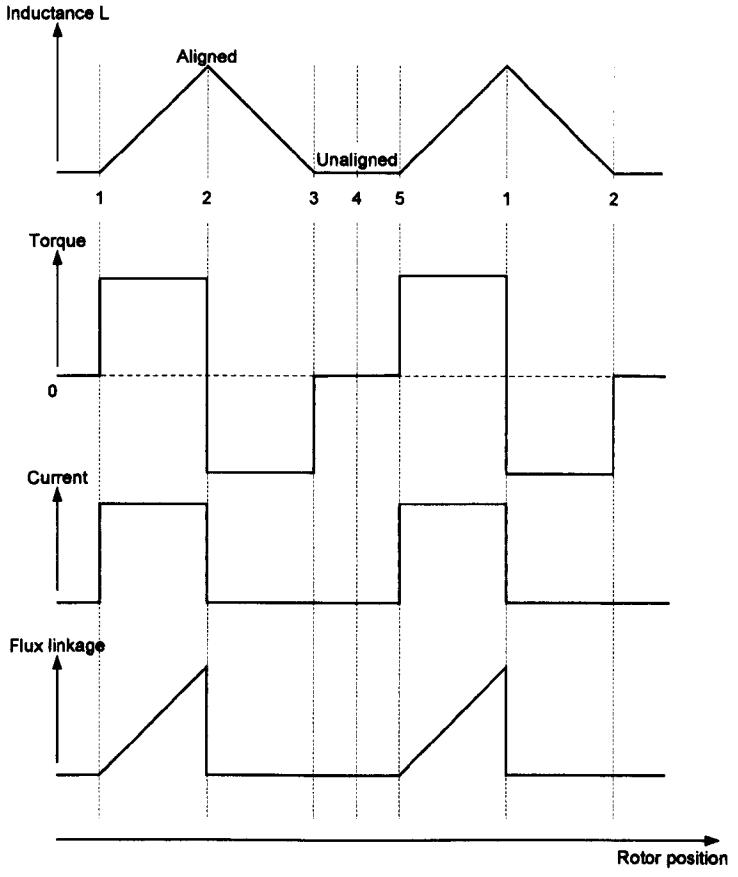


Figure 2-7- Variations of inductance, torque, current and flux linkage with rotor position with ideal pulsed unidirectional current (2=aligned position, 4=unaligned position, 1=start of overlap, 3=end of overlap)

At the aligned position, the torque changes direction. Negative torque is produced causing a braking force. Therefore, the magnetising current must be switched off while the poles are separating, i.e. from position 2 to 3. This will reduce the flux linkage to zero. The ideal current waveform shows the current is only flowing during the period of increasing inductance. As can be seen from Figure 2-7, the flux linkage curve is represented by a sawtooth waveform since flux linkage, ψ, is a function of the inductance, L and current, i.

$$\psi = Li \qquad (2\text{-}3)$$

However, in reality, the flux linkage cannot suddenly drop to zero. This is practically impossible since it would need infinite negative voltage. At the start of each stroke, the inductance is not zero, and therefore, the current waveform cannot have a step function but instead is more like a ramp which builds up from zero at the start of the motoring stroke and ramps down at the aligned position.

The process of current build-up is controlled by switching the supply voltage on at the turn-on angle, θ_O and switching the supply off at the commutation angle, θ_C. The difference between both angles is called the dwell angle, θ_D, where,

$$\theta_D = \theta_C - \theta_O \qquad (2\text{-}4)$$

In practice, the current is chopped at low speeds and the resulting average voltage will be much lower than the supply voltage. This is shown in Figure 2-8.

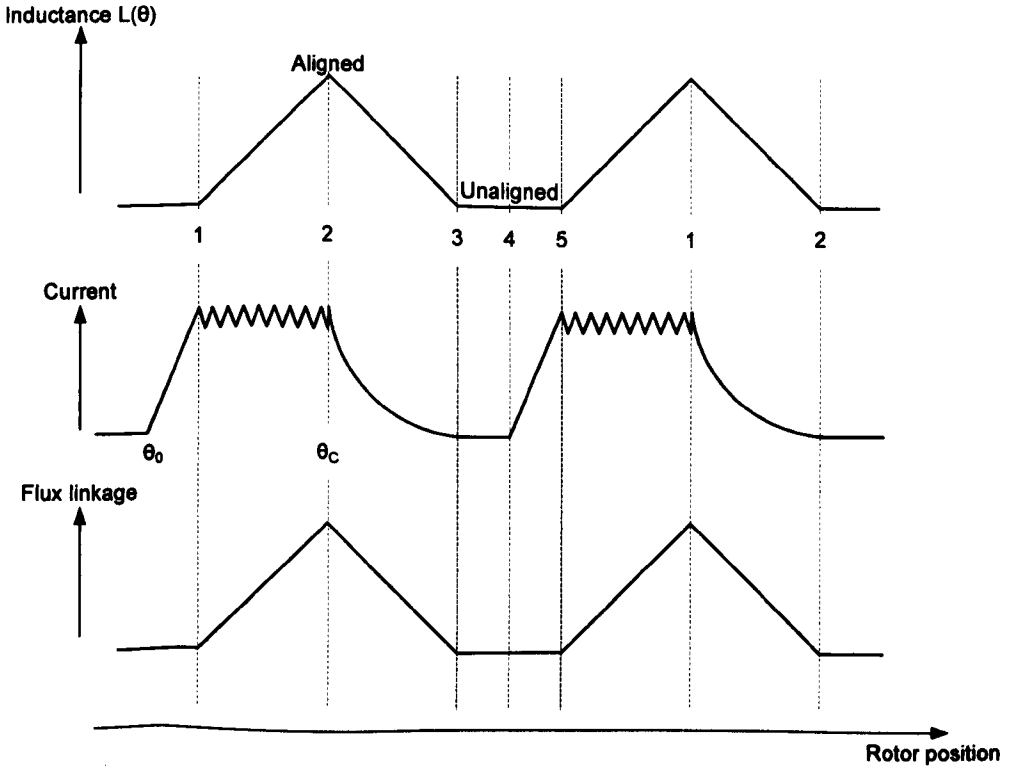


Figure 2-8- More realistic representation of the variations of inductance, torque, flux linkage and current with rotor position showing chopped current

At high speeds, the current waveform will approximate to a single pulse. Figure 2-9 shows the more realistic curves of the inductance, current and flux linkage.

Current chopping is no longer achievable because at sufficiently high speed, the dwell angle is small, and the current must be switched off before the rotor reaches the aligned position and the back-EMF reverses.

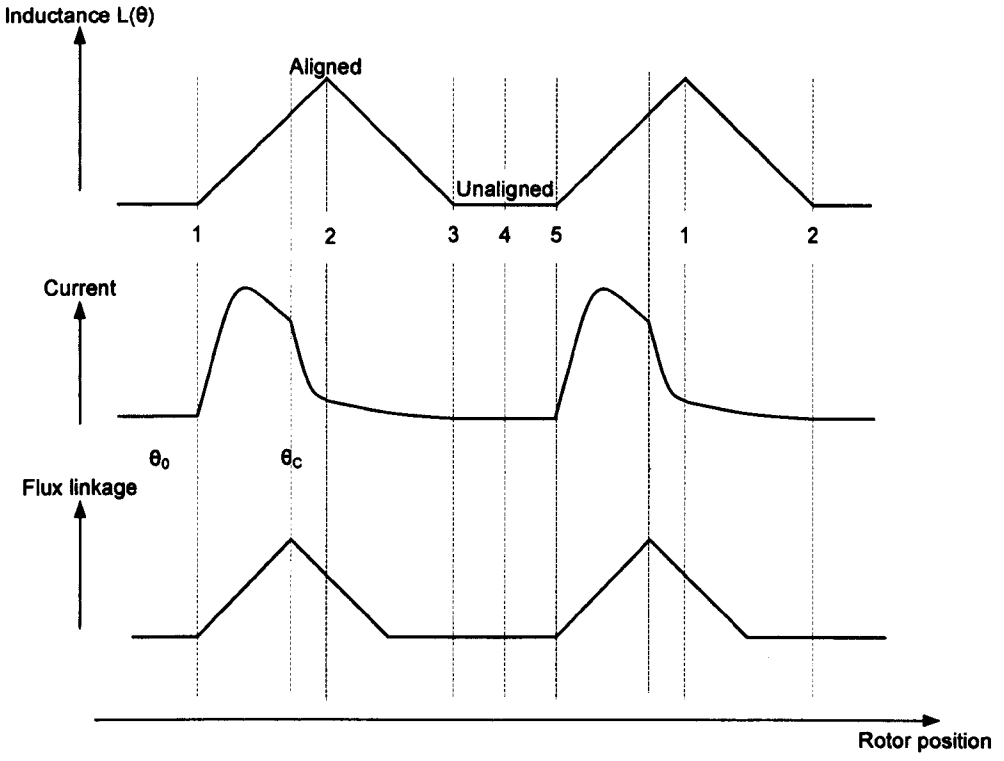


Figure 2-9- More realistic representation of the variations of inductance, torque, flux linkage and current with rotor position showing single pulse current approximation

At the aligned position, the back-EMF reverses and the rate of fall of current decreases. There is a possibility that the back-EMF may exceed the supply voltage and cause the current to increase again. Therefore, at high speeds, it is necessary to advance the turn-off angle so that this is prevented. The turn-off angle is set at several degrees before the aligned position.

These requirements for producing effective torque at variable speeds became the motivation behind the many SP-SRM converter topologies discussed in Chapters 3 and 4.

2.1.5. High speed operation of an SRM based on its dynamic behavior

To enable a close investigation of the dynamic behaviour of an SRM, the inductance-current-position characteristics of the machine has to be represented

accurately. The instantaneous voltage equation across the phase of an SP-SRM by Faraday's Law can be written as [40, 41]

$$v = iR + \frac{d\psi}{dt} \tag{2-5}$$

and since $\psi = Li$,

$$\begin{aligned} \frac{d\psi}{dt} &= \frac{dL}{dt} i + Li \frac{di}{dt} \\ \frac{d\psi}{dt} &= i \frac{dL}{d\theta} \frac{d\theta}{dt} + i \frac{dL}{di} \frac{di}{dt} + L \frac{di}{dt} \\ \frac{d\psi}{dt} &= i\omega \frac{dL}{d\theta} + (i \frac{dL}{di} + L) \frac{di}{dt} \end{aligned} \tag{2-6}$$

Therefore, we can express the equation of an SRM as,

$$v = iR + i\omega \frac{dL}{d\theta} + (i \frac{dL}{di} + L) \frac{di}{dt} \tag{2-7}$$

In equation 2-7, the first term is the voltage drop due to the internal resistance of the machine, the second term is the back-emf and the third, is the instantaneous inductance. From the equation, it is found that the voltage of an SRM is significantly affected by the inductance and the back-emf. At higher speeds, the back-emf term dominates the behaviour of the drive.

At low speeds, the back-emf can be ignored [42], compared with the DC supply voltage, and the machine is assumed to be current-fed. At this speed, the phase current waveforms should be programmed to be flat-topped to minimise torque pulsations. For medium speed operation, the back-emf increases and rapid current build up is limited. Therefore, the excitation for the ongoing phase is advanced. As the machine runs faster, the back-emf becomes comparable and maybe larger than the supply voltage. The phase excitation needs to be conducted at a larger advance angle. However, at this point, the inductance is small to build up sufficient torque. At these speeds, the machine is voltage-fed. The converter and controller must be able to program the current pulses as required by the machine.

To enable the SRM to achieve high speeds, where advance angle firing of the switches is necessary, the build up of current in the ongoing phase and turning off of current in the offgoing phase needs to be as fast as possible. A number of methods have been developed for faster transfer of energy during the magnetisation and demagnetisation period which includes modifications to the machine design, new control schemes as well as new power converter configuration for the SRM.

An alternative single-switch-per-phase converter topology has been proposed which includes a capacitor to dump the energy before the aligned position is reached [43]. When one phase is switched off, the stored energy is transferred into a capacitor. At the start of the next phase, the high DC-link voltage enables faster current rise. This topology enables fast demagnetisation of the commutating phase. The capacitor voltage needs to be maintained at 2Vs by hysteresis control so that –Vs is applied across the phase for fast demagnetisation. The capacitor must be controlled so that it is never overcharged, and therefore the control of the circuit becomes rather complex. An improvement made in [42] incorporates the same advantages but manages to reduce the voltage stress of the dump switch.

In [44], the energy from the off-going phase is dumped directly into a capacitor rather than through the DC voltage source as in the previous work. Therefore, the capacitor energy requirement is reduced. The converter achieved lower voltage stresses across the devices, a much simpler control algorithm and improved performance.

King-Jet [45] proposes a hybrid C-dump and buck-fronted converter topology that enables variable DC-link voltage to supply the desired voltage to the converter. Compared to the previous C-dump converters, the dump capacitor needs no additional control, as the voltage is regulated automatically by a chopper. The dump capacitor would stop being charged if the chopper fails. This circuit also achieves higher phase demagnetisation voltage as well as reduction of acoustic noise. However, the topology does not work well if the energising voltage is more than 80% of the DC source voltage due to the limitation of the power ratings of the switches and diodes.

Another proposed converter [46, 47] achieved faster excitation and demagnetisation, as well as smaller voltage rating of the dump capacitor. The effective excitation and demagnetisation of a phase are achieved via the boosted voltage from a capacitor that is placed in series with the DC link. The controllability and capability of the boost capacitor are also improved.

In [48] modifications have been made to the classical asymmetric half bridge converter to provide the boost voltage. An extra capacitor, controlled via a bi-directional switch, is added to the circuit after the DC link capacitor. The switch allows control of the boost voltage so that any desired boost voltage can be achieved. However, control is more complex and losses are greater.

All the above topologies work on the basis that a higher voltage will enable faster current build up during magnetisation and faster decay during demagnetisation. The boost circuit enables extra voltage during the commutations, thereby resulting in a square current waveform. This enables a larger advance angle to be achieved to enable operation at high speeds.

2.2. Single phase vs. three phase machine

To date, a lot of work has been carried out on multi-phase switched reluctance drives, but single phase has also received some attention. Single phase SRMs are much more suitable for low power, low performance applications such as hand tools, and domestic appliances, because the machine is simple, robust, compact, low cost and highly efficient. The SRM can be made more attractive for low cost applications if the number of switching devices is reduced, which has been the focus of many publications [38, 39, 49, 50].

In terms of the converters, the converter topology for poly-phase SRMs can be simplified to be used in single phase machines, because, in the single phase SRMs, all poles in the machine can be simultaneously excited by a single pole [51]. This will enable the controller to be simplified. Work by Lim *et al* [52] proves this, by testing the same converter for a single phase and a three phase SRMs. The experimental work on the converter demonstrates that the same performance is achieved when single phase and three phase SRMs with the same number of poles are used. The only

difference is as all coils of the SP-SRM were energised at the same time, the SP-SRM has higher DC link current and higher voltage ripples. However, this can be solved using a small series inductor at the front of the DC link.

One major disadvantage of a single phase SRM is the lack of self-starting capability, where the motor has the tendency to lock in a position that does not allow further rotation. The motor would be incapable of producing torque if the rotor is locked at the minimum inductance position at the end of the previous motoring stroke. There have been many developments on SP-SRM starting which is discussed in the next section. In this work, the emphasis is on the converter topologies, and so, it is assumed that the machine is operating at steady state.

2.3. SRM starting

SP-SRM starting is crucial for reliable operation. There can be two consequences for wrong starting. Firstly, the machine could start in an incorrect direction if the rotor is in an inappropriate quadrant or in the unaligned position. Secondly, if the rotor is at the aligned position, the machine may not rotate at all. This has been described in Section 2.2. Numerous methods either mechanically or electronically have been established in order to achieve reliable SP-SRM self-starting. All these starting methods must be simple, robust and economical for the SP-SRM to still be more attractive compared to having additional phase windings. There should also be no detrimental effects to the operation of the SP-SRM.

One of the earliest works on SP-SRM self-starting is that by Giardini *et al.* in 1976 [53] where they used magnetic materials positioned in the vacant inter-polar spaces to park the rotor at the position where it could produce adequate starting torque. Another work [54] uses parking magnets with a vane attached to the SP-SRM shaft together with Hall-effect sensor to form a rotor position transducer (Figure 2-10). A curved shaped slot wedges with cut-out portions could also be attached to the poles [55]. The use of the 'parking' magnet technique is effective but it must be considered during the machine design phase. The torque developed by the magnetic field of the magnets must be sufficient to overcome the friction due to the bearings or the rotor could stop in the undesirable area. However, work has been presented which shows that the machine can be self-started even under this condition [56]. The

disadvantage of using parking magnets is that it will increase the manufacturing complexity and the cost of the machine significantly. The torque developed by the magnets is limited and this could be a problem when the load is larger than the torque developed by the magnets.

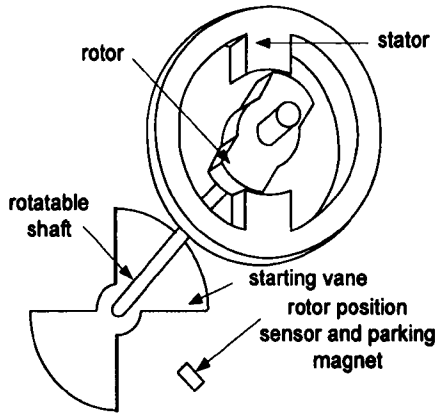


Figure 2-10- SP-SRM with the starting vane and sensor

Another method to self-start the SP-SRM is by using a mechanical mechanism that engages the rotor by having teeth on the rotor shaft and on a starting shaft [57] shown in Figure 2-11. There are two variations of this method. Firstly, the rotor is positioned in a preferred starting position before the stator coils are energised by using a rotor positioning mechanism. Secondly, the rotor is set into motion before the stator coils are energised so that the rotor is never static at any position by using a motor starting mechanism. Both these variations involve a switch to be pressed which is connected to a shaft with teeth that could latch on to a disk with similar teeth at the rotor shaft. This latch is connected to a microprocessor which then provides the signal for current to energise the coils.

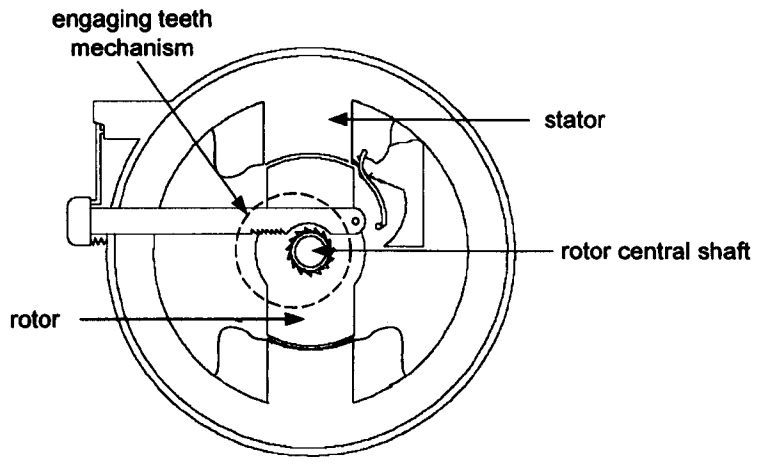


Figure 2-11- SP-SRM with the mechanical mechanism for starting

There are also starting methods which involve the design of the machine itself. One idea is to shift the pole-pairs [58]. This method has successfully been implemented in a blower [59]. The poles have shoulders that are placed diametrically opposite each other. These shoulders result in different air gaps leading to continuous variation of reluctance and hence torque generation at all positions. The shifted stator pole has a parking magnet attached to ensure the rotor is parked at the desired position. The shift is to eliminate the rotor stopping in the completely aligned position. This is shown in Figure 2-12.

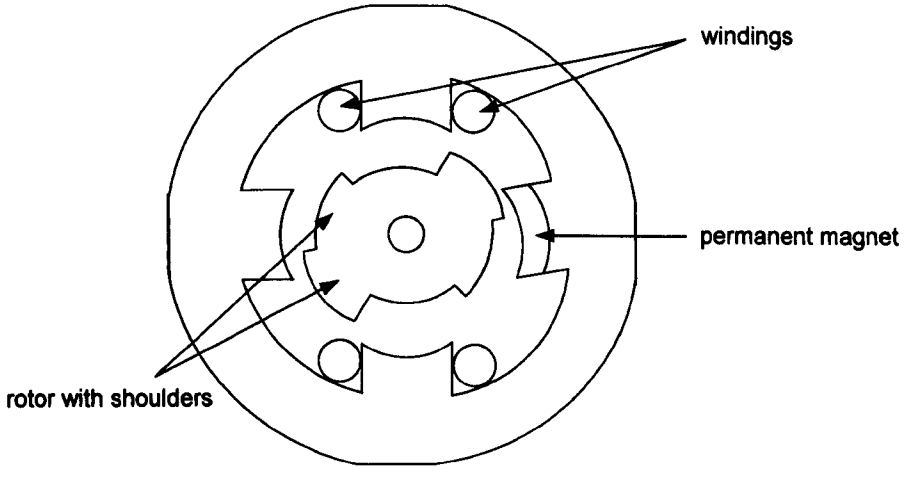


Figure 2-12- SP-SRM with the shifted pole-pairs

A quite recent publication [60] suggests using a 4/4/4 motor design (Figure 2-13). The machine has four auxiliary stator poles referred to as interpoles. The interpole windings are pulsed with small currents that will pull the nearest rotor poles to complete alignment with the interpoles. At any one time, only one set of interpoles

is used for starting in any one direction. The design involving the interpoles contributes to a higher manufacturing cost.

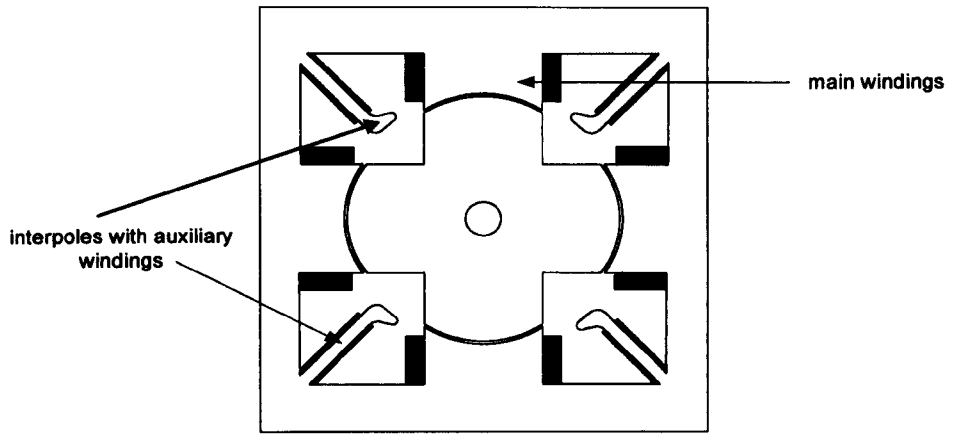


Figure 2-13- SP-SRM with the interpoles

In [61] the motor uses magnetic saturation effects for starting. Finite element analysis is used to determine the best iron saturation to use on the rotor teeth. The motor can then produce sufficient starting torque from every rotor position.

All the SP-SRM self-starting methods described above, work by preventing the rotor from being in the fully aligned position in the first place. However, in [62] the opposite is required at the start. The way that this is useful is by using shorting rings mounted on each pole of the rotor. The shorting rings are electrically insulated from the rotor conducting material. The starting procedure involves energising the phase windings so that the rotor poles are fully aligned with the stator. Then, the rotor coils are pulsed (with predetermined current magnitude and duration) to shift the rotor away from the aligned position. The way the shorting rings are mounted will cause the opposing flux to force the rotor away. As the rotor rotates away from this position, the phase currents can be commutated in the usual manner. Figure 2-14 shows the position of the shorting rings with respect to the rotor and stator of the SRM.

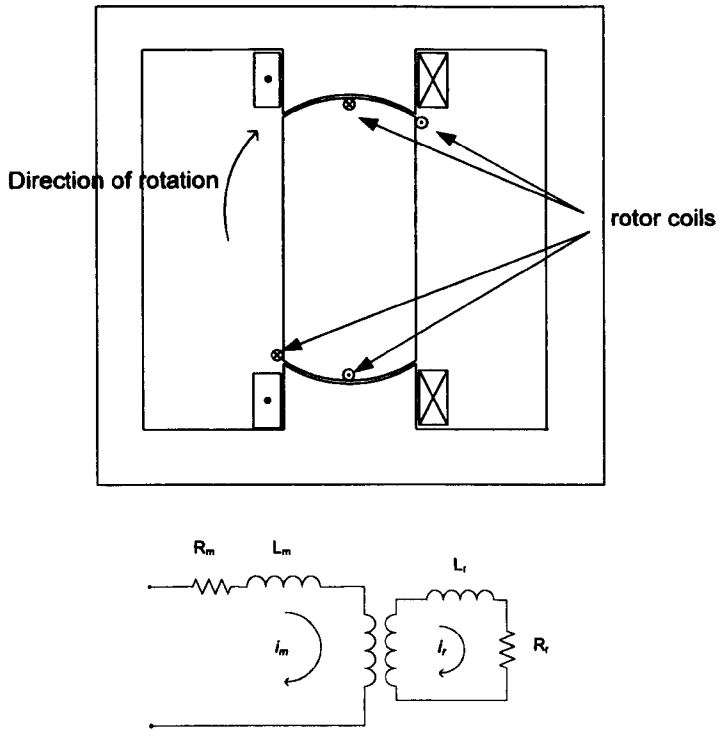


Figure 2-14- SP-SRM with the shorting rings at the aligned position – the current polarities in the phase and the shorting rings are shown as the current increases (R_m, L_m and i_m : resistance, inductance and current in the main windings, R_r, L_r and i_r : resistance, inductance and current in the rotor coils)

In addition to all the methods described above, it has become increasingly popular to use sensorless method in order to self start the machine. With all these sensorless achievements, the benefits are twofold. The sensorless method is used to obtain data to control the machine and also for starting of the machine. The focus is to use sensorless methods to estimate the rotor position. Once the rotor position has been determined, the SP-SRM controller will then use the information to start the machine. Some of the ways to determine the rotor position is by estimating the inductance profile at machine standstill [63, 64], measuring mutually induced voltage of an inactive phase of the SP-SRM [65] and using a fuzzy algorithm to estimate the shaft position [66, 67]. This will be detailed in Section 2.4.

2.4. Rotor position estimation

For small low power SR drives, voltage control operation is most appropriate [68]. The required parameters would be the voltage, the turn-on, θ_O and turn-off (commutation) angles, θ_C. Control of the voltage is achieved by using a variable DC supply, or by using switching devices to chop the bus voltage. The angles are selected

so that the requirements of the whole system, such as maximum efficiency, can be achieved.

As explained before, the commutation of SRMs require rotor position information to derive the converter commutation signals. This could be done by using position sensors, position encoder or estimation of the position using sensorless techniques.

One of the cost effective solution for obtaining commutation signals for an SRM is by using low-resolution position sensors [68] such as Hall effect sensors or opto-interrupter with a slotted disk. Opto-interrupter devices are mounted onto the motor frame, and a slotted disk is then mounted onto the rotor shaft. Two consecutive edges of the disk slot will be detected by the opto-interrupters and position feedback is derived. The intervals between the two edges will be the resolution of the rotor position and using this information, the operating modes can be determined.

The design of the commutation scheme is dependent on the motor type and drive requirements. Once that is established, the number of sensors, sensor placements and slot patterns on the disk can be specified. Figure 2-15 shows a slotted disk and the position of an opto-interrupter.

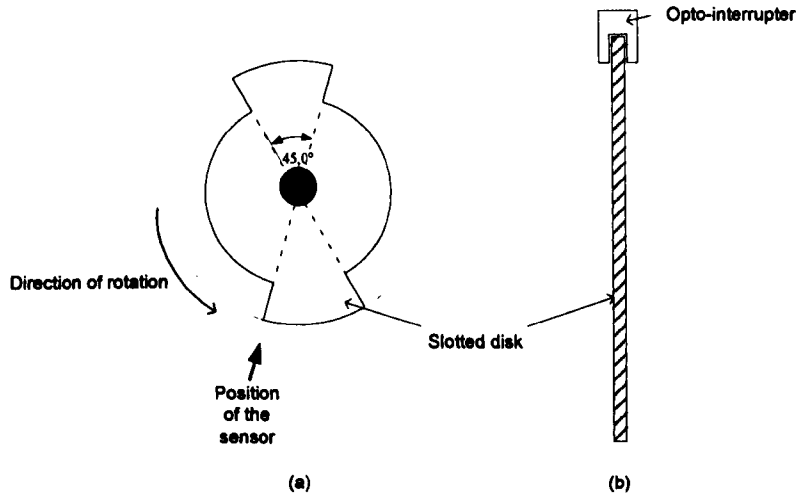


Figure 2-15- Position sensors (a) slotted disk; (b) side view showing the position of the opto-interrupter

Other methods for obtaining position feedback, use more complex schemes involving high-resolution position sensors or extensive circuitry. This is more

suitable in applications where the use of position sensors might be inconvenient such as in sealed compressors [68], and also for low cost drives where the cost of the sensors could be significant.

In active probing, a relatively low amplitude test pulse is injected to a phase when it is not in use for torque generation. This method is suitable for lower speed machines. This is because at higher speeds, the excitation waveforms become significant in each phase period, and there would be little time to inject any additional signals. Also, the low amplitude test signals can be seriously degraded by the mutual coupling of the adjacent phases. This method was first proposed by Accarnley [69]. This method would only be suitable to a multi-phase machine.

The rotor position information can also be obtained using passive waveform monitoring. One of the methods proposed by Gallegos-Lopez [70] relies on the detection of the change in sign of the phase current derivative, and is called the current gradient sensorless method (CGSM). Husain [65] also proposes to use the inter-phase coupling effect. Voltage induced by mutual coupling is induced into any phase which is adjacent to an active phase due to inter-phase coupling effects. These voltages vary as a function of rotor position, and it would be possible to use these voltages for position estimation. The benefit of using passive waveform monitoring to detect rotor position is that there would be no additional switching or signal injection circuitry required. Also, the problem of mutual effects can be reduced. This method is however more generally suited to higher speed operation.

Another class of position detection is by using mathematical modeling, achieved via either a state observer or artificial intelligence techniques. If using a state observer [71], a state space model of the complete system, including the motor and the load, is developed. The model then uses real physical inputs to estimate motor speed, rotor position, phase currents and flux linkages. One advantage of using this technique is that no additional signal injection circuitry is required, and there would be no inherent speed limitation. However, significant computational power is needed. The success of this method will depend on the accuracy of the state space model. More recent techniques focus on using artificial intelligence for position detection. Fuzzy logic is used to generate data for the positions based on flux current

curves during aligned and unaligned positions [66, 72]. Artificial neural network (ANN) could also be used for position estimation as used in [73, 74]. These mathematical modeling techniques can be used for low or high speed operation. These techniques do not require any additional switching or signal injection circuitry as mentioned in previous techniques. However, a fast digital signal processor (DSP) will be necessary to implement any of these methods due to the significant processing involved.

2.5. Operation of SP-SRM drives

Despite all the advances in the SRM design and power electronics, there is still a lack of readily available standardised power electronic converters [75]. This is totally opposite to other machine types, especially induction motors, where the converters, drives and protection circuits are all available readily packaged for use.

The dynamic operation of the SP-SRM is best described based on the asymmetric half bridge topology, with single-pulse operation assumed. The SP-SRM conduction mode is shown in Figure 2-16.

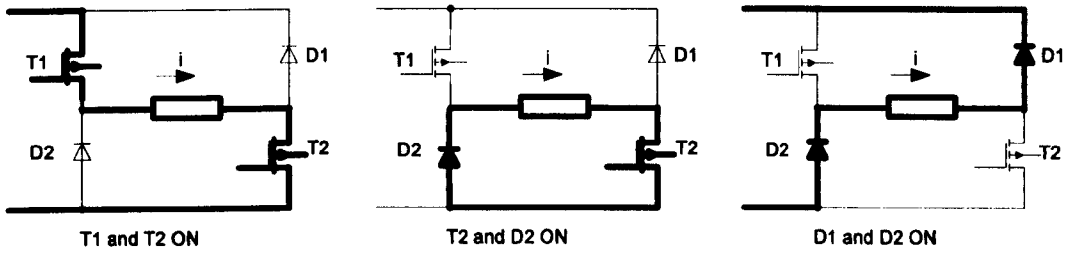


Figure 2-16- SP-SRM conduction mode

The three operation modes can be described as follows.

Mode 1: Magnetisation by the source –T1 and T2 ON

Both switches T1 and T2 are turned on, and the current, *i* in the phase winding rises rapidly.

Mode 2: Freewheeling – T2 and D2 ON

During this mode of operation, the energy freewheels through switch, T2 and diode, D2. There is no flow of energy back into the supply. The demagnetisation proceeds very slowly through the winding resistance.

Mode 3: Demagnetisation via freewheeling diodes – D1 and D2 ON

When both the switches are turned-off, the energy is returned back to the supply via the freewheeling diodes.

Figure 2-17 shows the waveforms of motor inductance, voltage, flux linkage and phase current at a sufficiently high speed. It is assumed that the SP-SRM has an ideal inductance profile. Aligned, *A*, and unaligned positions, *U*, are shown. Both the switches are switched on at θ_O and both are switched off at θ_C.

To accomplish zero flux linkage at the end of each motoring stroke, the terminal voltage is reversed at θ_C and this is seen in the voltage waveform in Figure 2-17. This is achieved via the freewheeling diodes when both the switches are turned off as described in Mode 3.

Using this method of operation, during commutation, there are always two switching devices in series, and this will cause high conduction losses. However, in terms of the machine efficiency, it is still very high since the energy is recovered at the supply at the end of each commutation.

Using this converter configuration the converter achieves full control and flexibility. Other topologies for the SP-SRM exist and will be further discussed in the next chapter.

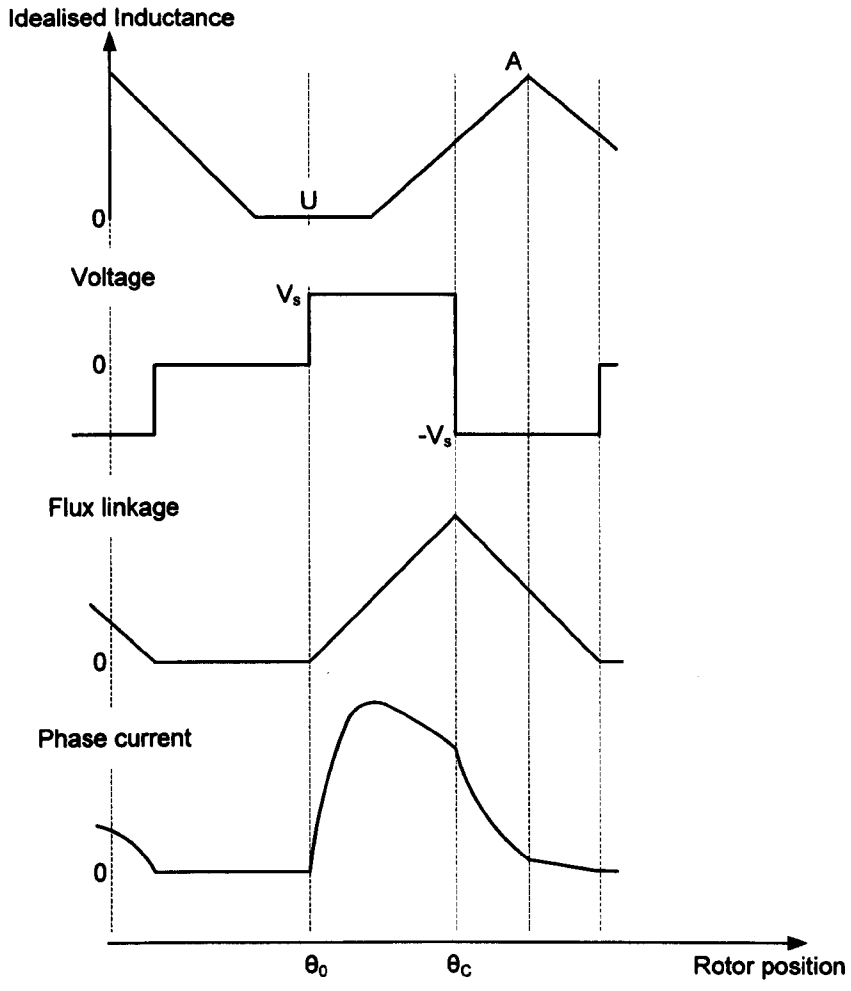


Figure 2-17- SP-SRM single pulse waveforms

2.5.1. Control techniques for SP-SRM converters

Many control algorithms for the SP-SRM have been proposed. The torque in an SRM is independent of the values of the current and flux-linkage directions, but depends only on the rate of change of the inductance with rotor position. Therefore, the current and flux-linkage could be unipolar and still the machine would be able to produce torque. One advantage of this mode is it will reduce iron losses and require simpler controller [68].

The controller must be able to supply unipolar current in pulses based on the rotor position. To achieve the desired torque and speed, the controller must be able to regulate the magnitude and the shape of the current. It must also be able to provide pulses of reverse voltages for de-fluxing.

Because of these requirements, the controller must be tailored to each specific motor as different motor will have different characteristics. For SP-SRMs, the most convenient power source is the AC mains. As the current ripple is large, harmonics will be introduced to the mains supply. Therefore, filters might need to be added.

The method implemented throughout this thesis is current hysteresis control. The power switches are switched on or off according to whether the current is greater or less than a preset upper and lower current limits. In practise, the instantaneous phase current is obtained by a current transducer and the value compared against the hysteresis thresholds.

Recently, as described in [63-67] sensorless control methods have been implemented. It is claimed that the sensorless method will make the motor more cost effective and more reliable since the sensors are eliminated. However, the control algorithm would not necessarily be simple to implement.

The best SP-SRM controller must be able to vary the firing angle as the speed and torque vary. Also, the shaft position signal must be accurately and immediately available for commutation.

2.6. Summary

This chapter has discussed the technology behind the SRM, including its history and its future. A description of the machine and how torque is produced is given in detail. The choice between single-phase and multi-phase machines is justified. The self-starting of the single phase machine has also been discussed. The chapter also touched on the converter design including a discussion on the controller requirements.

Chapters 3 and 4 that follow will be about the converter topologies for SP-SRMs. Detailed explanation and simulation results for each converter topology are provided.

CHAPTER 3
OVERVIEW OF SINGLE PHASE SRM CONVERTER TOPOLOGIES

Regrettably, most of the work on SRM related technologies has been predominantly directed toward a single topology, elaborating on certain attributes such as their mode of operation and advantages, thus, giving a general impression of numbers of unconnected techniques. An overview of the single phase SRM converter topologies is given in this chapter, with the aim of providing a greater understanding of the wide ranging subject area. [76]

Previously in Chapter 2, the SRM is discussed in general, and the conventional SRM converter is explained in detail. In this chapter, the single phase SRM converters are classified according to the mode of operation, and a family tree encompassing all single phase converters is derived. Selected converters from each class are analysed by discussing the advantages and disadvantages. Some mathematical equations are also provided based on the modes of operation. The converters considered are intended for use in variable speed applications with peak power rating of up to 1kW.

3.1. Classification of converter topologies

There are quite a number of publications [22, 27, 38, 77-79] which have attempted to give a review of the SRM converters. However, none have been really comprehensive and as a result, converters for SP-SRM seem to have no similarities at all. What is different in this work is that it reviews all the available SRM converters, and classification was made based on the distinguishing factor, how the stored energy in the phase windings is managed. The relationship between these converters can be summarised in Figure 3-1.

Based on this criterion, single phase SRM converters generally fall into either one of two categories: (a) converters with energy dumping or (b) converters with energy recovery.

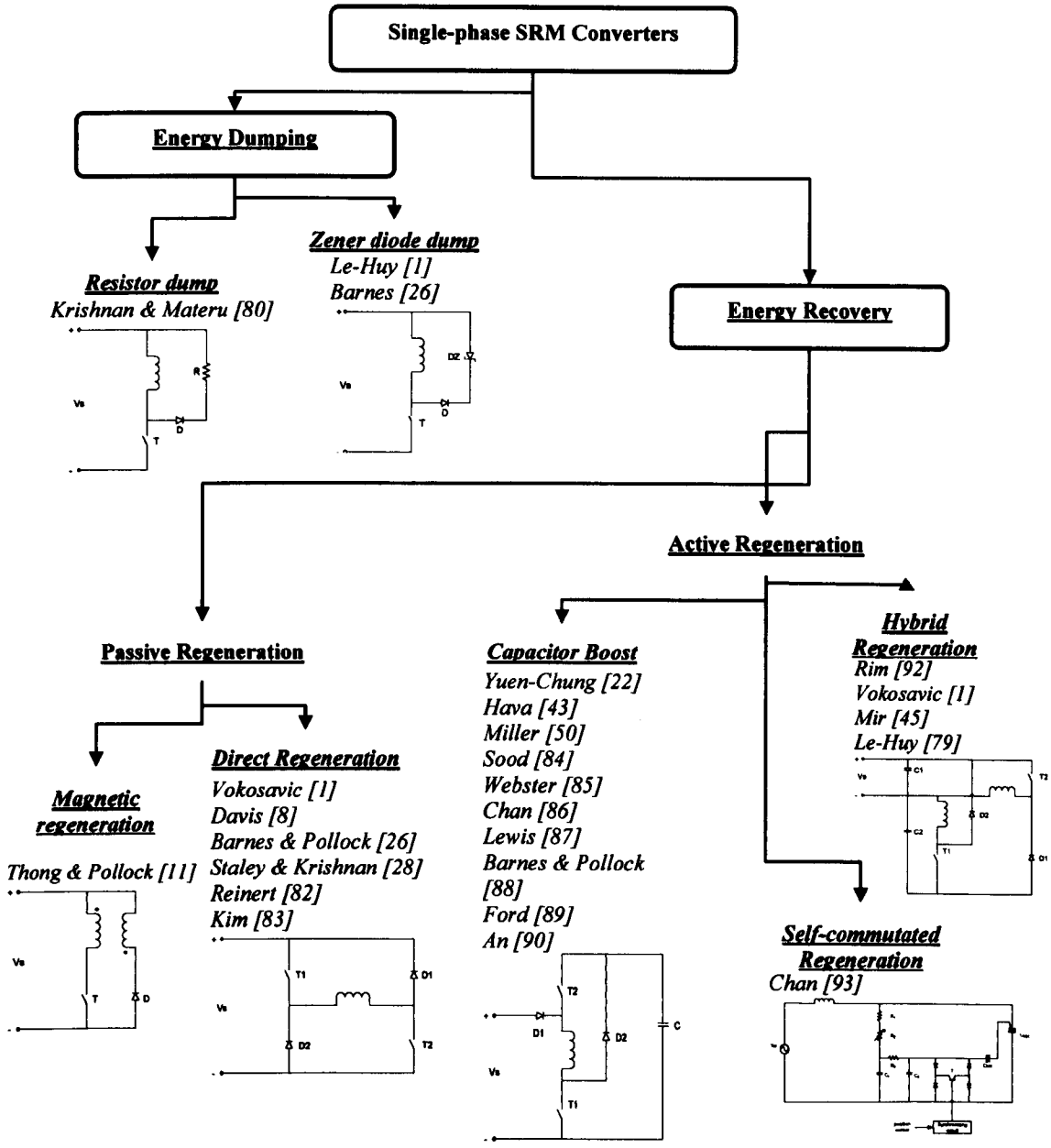


Figure 3-1- Single phase SRM converter classification

The detail description of the converters in each of the sub-class will include mathematical analysis of the equivalent circuit. For the equivalent circuit, it is assumed that all components are ideal except where specifically noted. From this point on, the equation used to model the SRM would be the general equation assuming the machine is linear.

As mentioned in the previous chapter, the motor is represented by an inductance that is variable depending on rotor position, $L(\theta)$, machine back-EMF (produced by the current and the rate of change of inductance as a function of rotor position at an angular speed), $i\left(\frac{dL(\theta)}{d\theta}\right)\omega$, and an internal resistance, r_{int}. The equivalent circuit is shown in Figure 3-2. All circuits use a constant voltage source, V_S at the input side to represent the DC link voltage. This is equivalent to the peak voltage of the single phase mains supply.

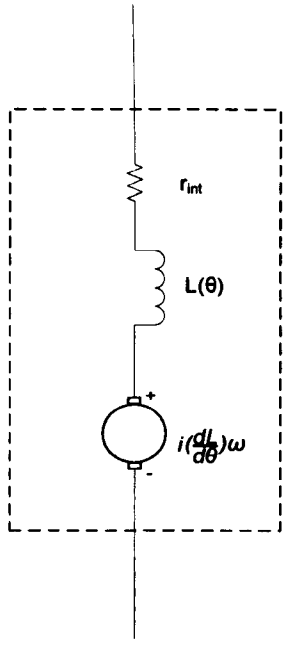


Figure 3-2- The SP-SRM equivalent circuit

The converters need to be controlled so that switching occurs only when the rotor is at the position of increasing inductance. Therefore, a position sensor will need to be used. This signal, combined with some defined hysteresis band will enable the SRM to pull the required current during operation. All converters are analysed based on using the same hysteresis current control that will be explained in detail in Chapter 4.

3.2. Energy Dumping

In Energy Dumping converters, as the name suggests, part of the energy in the phase windings are either dissipated (or dumped) in a resistor or a Zener diode. Individual descriptions of the converters are detailed separately below.

3.2.1. Resistor Dump

The equivalent circuit of a single phase resistor dump converter is shown in Figure 3-3. Part of the stored energy is dissipated in a resistor (R_{dump}) instead of being regenerated into the DC link. A diode is also needed for freewheeling.

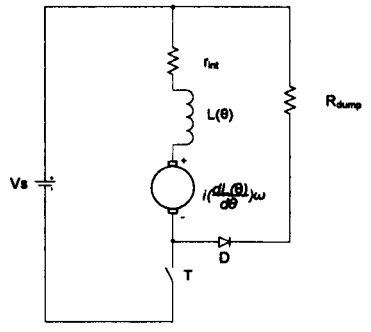


Figure 3-3- Resistor Dump converter

The significant cost reduction in this topology is because a resistor is used in place of the extra semiconductors for the regeneration path. Although this circuit has been available for some time, it was first analysed by Krishnan in [77].

The main advantage of this converter topology is the simple configuration since there is only one switch per phase. The switch driving requirement is minimal as the switch shares a common source (emitter) connection.

The major drawback of this circuit is that the energy is simply dumped during each commutation process resulting in a low efficiency converter. This inefficiency is, however, more than compensated by their simplicity, low cost and low component count. Also, as the dissipative component is a resistor, the defluxing voltage will tend to drop as the current decreases. The resistor will also need to have a high power rating, which will create the necessity for adequate cooling of the resistor.

The converter with such drawbacks makes it undesirable. However, it is considered suitable for low cost variable speed applications that require intermittent use such as hand tools [77].

The operation of this circuit can be described in two basic modes of operation:

Mode 1: Magnetisation from the source

When the switch is turned on, the source voltage is applied to the winding. The equivalent circuit during turn-on is shown in Figure 3-4. Energy is transferred from the DC link to the SRM. Part of this energy is converted to mechanical energy by the machine, whilst some are being stored in the magnetic field.

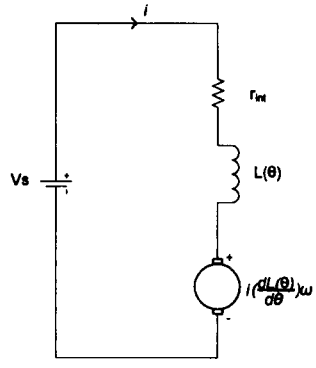


Figure 3-4- Resistor Dump converter – Mode 1

Since the inductance is increasing during this turn-on time, the current builds up exponentially with the time constant of τ_1 from zero at the start of the conduction period. As soon as the switch is turned-on, the current in the equivalent circuit should increase to a maximum current value, I_{max} (defined by the L and R of the circuit) However, the current only rises up to the maximum value defined by the upper threshold of the hysteresis band, I_{upper} (on the same current curve shown in Figure 3-5). In the figure, I_{lower} refers to the minimum value defined by the lower threshold of the hysteresis band.

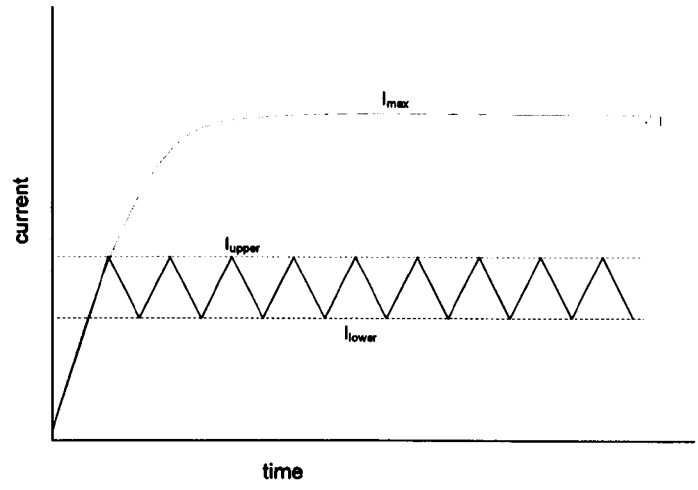


Figure 3-5– Current waveform of the circuit showing the relationship between I_{max}, I_{upper} and I_{lower}.

The current during this period is given by:

$$i(t) = I_{\max}\left(1 - e^{\frac{-t}{\tau_1}}\right) \qquad (3\text{-}1)$$

where

$$I_{\max} = \frac{V_S}{R} \qquad (3\text{-}2)$$

$$R = r_{\text{int}} + \frac{dL(\theta)}{d\theta}\omega \qquad (3\text{-}3)$$

$$\tau_1 = \frac{L(\theta)}{R} \qquad (3\text{-}4)$$

R is the effective resistance of the circuit, and is the sum of the machine internal resistance and the rate of change of inductance as a function of the rotor position at an angular speed. The time constant τ_1 of the circuit is based on motor inductance as a function of rotor position.

The value of i at the start of the conduction period is zero, and for subsequent switching during the same conduction period, the current will rise from the value of I_{lower} defined by the minimum threshold of the hysteresis band.

Mode 2: Demagnetisation via the dump resistor

At turn-off, the energy freewheels through the windings, the diode and the dump resistor. The equivalent circuit during this period is shown in Figure 3-6. At the instant of turn-off ($t_{turn\text{-}off}$), the energy through the windings de-energises through the resistor from current value of I_{upper}, until it reaches the minimum threshold value set by the hysteresis band, I_{lower}.

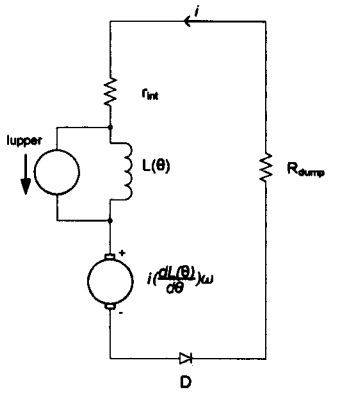


Figure 3-6- Resistor Dump converter – Mode 2

The decaying current during this period is given by the equation below. The final current, *i(t)*, at the end of Mode 2 is equals to I_{lower} for each subsequent switching during the same conduction period. At the end of the conduction period, the current will decay down to zero and therefore, *i(t)* = 0 at the end of Mode 2.

$$i(t) = I_{upper} e^{\frac{t}{\tau 2}} \qquad (3\text{-}5)$$

where

$$\tau_2 = \frac{L(\theta)}{r_{\text{int}} + \frac{dL(\theta)}{d\theta}\omega + R_{dump}} \qquad (3\text{-}6)$$

Since the inductance is decreasing, the current decays exponentially over the turn-off period with the time constant of τ_2. The new time constant is now dependent on the internal resistance of the SP-SRM, the rate of change of inductance as a function of rotor position at an angular speed and the dump resistance. Since there is the additional component in the calculation of τ_2 it is expected that during current decay, the time constant is much faster. This results in a faster current decay as the

dump resistor value gets bigger. A more detailed analysis of this resistor effect on current decay is available in Chapter 4.

Although this converter has a single switch topology which means the cost could be reduced, the efficiency of the overall system is compromised since all the winding energy is lost completely in the resistor.

3.2.2. Zener Diode Dump

The Zener Diode Dump is similar to the Resistor Dump circuit, but differs as the resistor is replaced by a Zener diode (*DZ*). The equivalent circuit of this converter is shown in Figure 3-7. A diode is also needed for freewheeling.

Although this topology has been mentioned in literatures [78] and [24], no further detail is available especially in terms of the circuit design and analysis. The work in this section and the simulation results in Chapter 4 will attempt to design an equivalent circuit to look in detail into how the circuit works.

This circuit shares the same advantages with the resistor dump. In the case where the dissipative component is a resistor, the defluxing voltage will tend to drop as the current decreases. Substituting the resistor with a Zener diode improves this, because the Zener diode stabilizes the defluxing voltage. This results in a quicker decline of the inductor current.

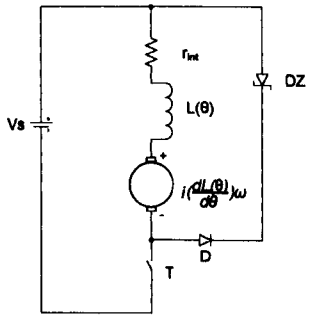


Figure 3-7- Zener Diode Dump converter

The operation of this circuit can also be described in two basic modes of operation:

Mode 1: Magnetisation by the source

When the switch is turned on, the source voltage is applied to the winding. The equivalent circuit is shown in Figure 3-8.

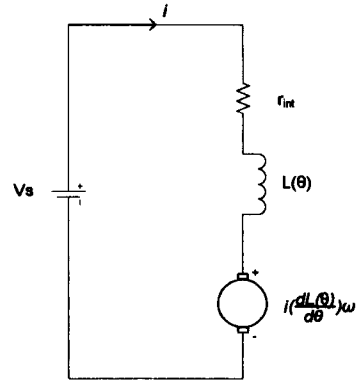


Figure 3-8- Zener Diode Dump converter – Mode 1

This circuit is identical to Figure 3-4. The current during this period is given by the same equation as in a resistor dump:

$$i(t) = I_{\max}\left(1 - e^{\frac{-t}{\tau_1}}\right) \qquad (3\text{-}7)$$

where

$$I_{\max} = \frac{V_S}{R} \qquad (3\text{-}8)$$

$$R = r_{\text{int}} + \frac{dL(\theta)}{d\theta}\omega \qquad (3\text{-}9)$$

$$\tau_1 = \frac{L(\theta)}{R} \qquad (3\text{-}10)$$

Mode 2: Demagnetisation via the Zener diode

At turn-off, the energy freewheels through the windings, the diode and the Zener diode. The equivalent circuit during this period is shown in Figure 3-9.

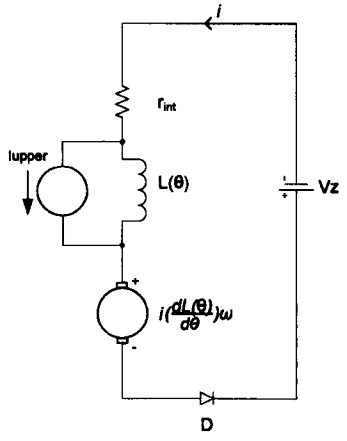


Figure 3-9- Zener Diode Dump converter – Mode 2

The decaying current during turn-off is given by the equation below.

$$i(t) = I_{upper} e^{\frac{t}{\tau 2}} - I_{DZ}\left(1 - e^{\frac{t}{\tau 2}}\right) \qquad (3\text{-}11)$$

where I_{DZ} is the maximum Zener current $\frac{V_{DZ}}{R}$, and,

$$R = r_{\text{int}} + \frac{dL(\theta)}{d\theta}\omega \qquad (3\text{-}12)$$

$$\tau_2 = \frac{L(\theta)}{R} \qquad (3\text{-}13)$$

The current decays exponentially over the turn-off period with the same time constant of τ_2.

Again, similar to the Resistor Dump topology, this circuit has low efficiency since the energy is lost.

3.3. Energy recovery

Figure 3-10 is an extract from Figure 3-1, and shows the branch of the family tree which describes the Energy Recovery type of converters.

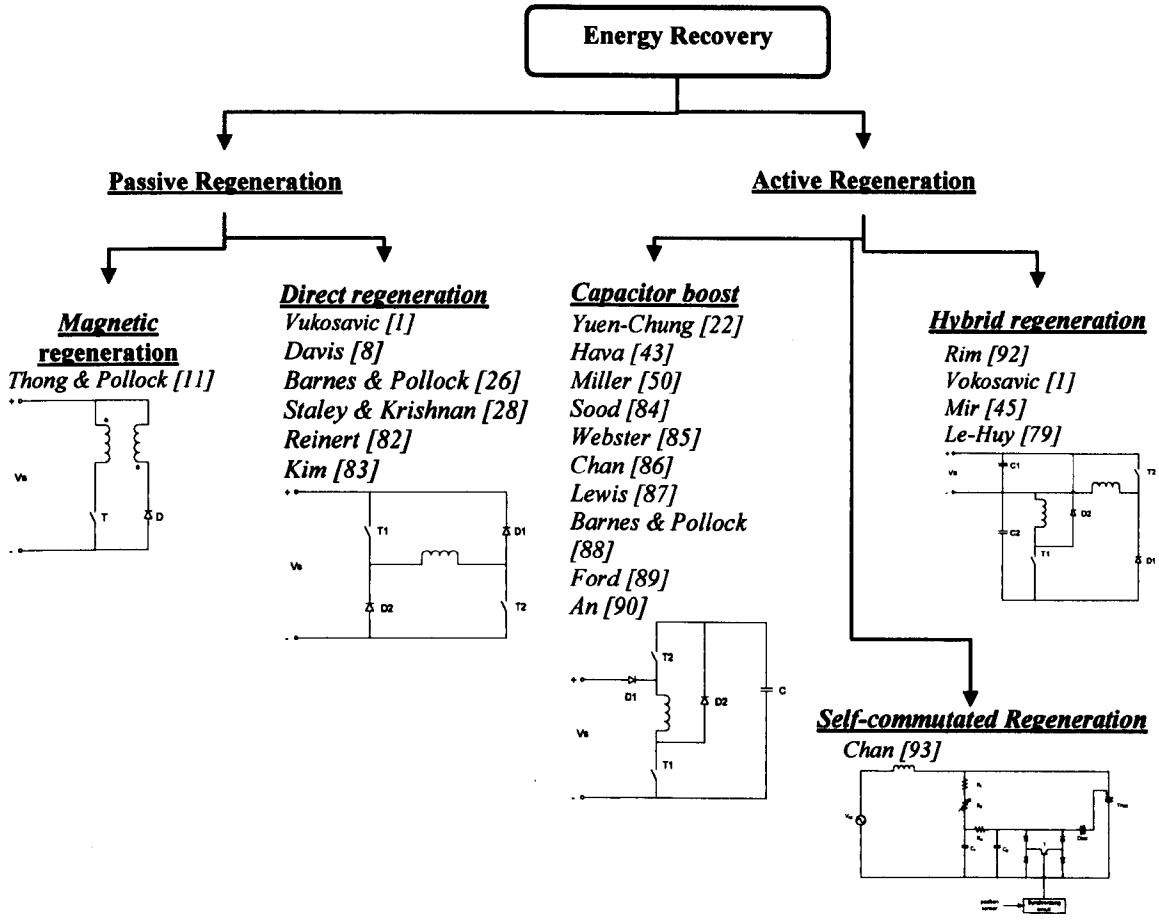


Figure 3-10- Energy Recovery branch of the converter family tree

This type of converters is so called because the energy in the windings is recovered at the end of each commutation period. The method by which the energy is recovered is used to further classify the converters. If the energy is returned directly to the supply, the converters are classed into the Passive Regeneration group. If an intermediate stage is used to store the energy temporarily before returning it to the source, the converters are classed as Active Regeneration.

3.3.1. Passive Regeneration

The term *passive* is used because it indicates that the process of returning the energy back to the source is natural, without additional intermediate components. This group of converters can be further split into two categories since there are two distinct methods of returning the energy back to the supply.

3.3.1.1 Magnetic Regeneration

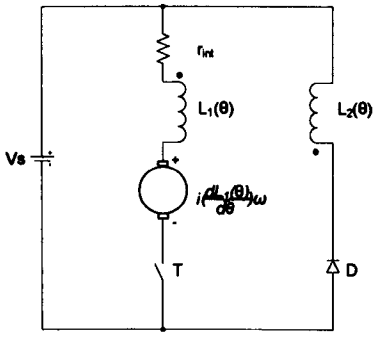


Figure 3-11- Magnetic Regeneration converter

Figure 3-11 shows the magnetic regeneration converter. The energy stored in the magnetic field of the phase winding is transferred to a closely coupled auxiliary winding. The number of turns for the primary and secondary are identical, in order to be able to generate the same input and output voltage. This can be achieved if there is perfect coupling of magnetic flux between the windings and the coupling factor will be unity. Therefore, the two coils act as a 1:1 transformer. However, in practice, this is impossible to achieve, and this has an effect on the converter which will be described later. The sense of the connection of the primary and secondary windings is chosen so that $V_{primary} = - V_{secondary}$. The voltage across coil 1 is equals to the source only when the switch, T is on. By transformer action the voltage of $-V_S$ appears across coil 2. The relationship between the induction and the coupling factor for coils 1 and 2 is:

$$\frac{L_1}{L_2} = \frac{m_1}{m_2} = k \qquad (3\text{-}14)$$

where L_1 and m_1 are the inductance and mutual coupling of coil 1, and L_2 and m_2 are the inductance and mutual coupling of coil 2. The coupling factor is a constant which relates the inductance and the mutual inductance of both the coils.

The main advantage of this converter is that it requires only one switch per phase, and therefore the switching losses can be minimised. Another advantage is that the power switch used is referenced to ground resulting in cheaper low side gate driver [25]. Since the energy is recovered in a magnetic system, the rate of change of current in the circuit is high. This is beneficial especially for high speed applications.

In [80] the converter is claimed to be the simplest and lowest cost. However, the author suggested an RCD snubber network to reduce the switch stress during conduction.

The disadvantage of such system, however, is that the construction of the bifilar winding is complex. The leakage inductance due to any imperfect coupling will have to be controlled during switching transitions in order to prevent overvoltages across the power switch [81]. This will result in the need for additional snubber circuits [80, 81] and overrated components. This is discussed further in Chapter 4.

The operation of the converter can be described in two modes of operation.

Mode 1: Magnetisation by the source

When the switch is turned on, the source voltage is applied to the winding. The equivalent circuit is shown in Figure 3-12.

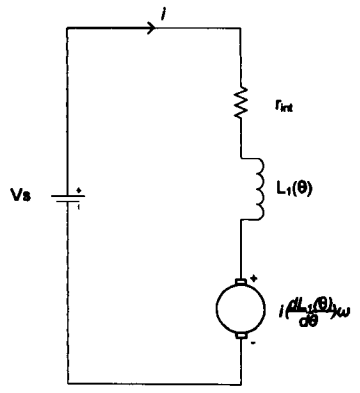


Figure 3-12- Magnetic Regeneration converter – Mode 1

Once the switch is turned on, the current builds up in the main winding. The diode in series with the auxiliary winding is reverse biased. The current equation during turn-on is as equation (3-1) of section 3.2.1.

The current increases exponentially over the period with the time constant of τ_1.

Mode 2: Demagnetisation by the auxiliary winding

At commutation, current flow transfers from the primary to the auxiliary winding. The EMF of the primary coil is represented by V_S. The equivalent circuit is shown in Figure 3-13. The time constant during this cycle is τ_2. The decaying current during turn-off is given by the equation below. I_{upper} is defined by the maximum threshold of the hysteresis band.

$$i(t) = I_{upper} e^{\frac{-t}{\tau_2}} - I_{\max}\left(1 - e^{\frac{-t}{\tau_2}}\right) \qquad (3\text{-}15)$$

where

$$I_{\max} = \frac{V_S}{R} \qquad (3\text{-}16)$$

$$R = r_{int} + \frac{dL_2(\theta)}{d\theta}\omega \qquad (3\text{-}17)$$

$$\tau_2 = \frac{L_2(\theta)}{R} \qquad (3\text{-}18)$$

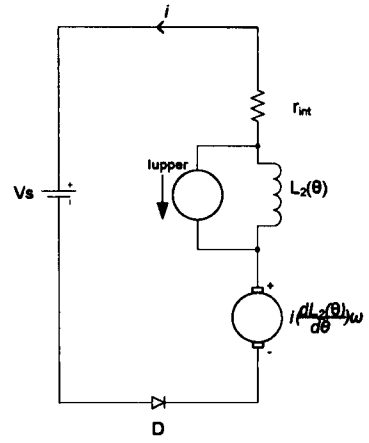


Figure 3-13- Magnetic Regeneration converter – Mode 2

From the detailed description of the mode of operation, the converter has the potential to achieve very high machine efficiency if perfect coupling can be provided. This is because, in this case, all the energy from the primary winding is fully transferred to the secondary to be returned to the supply.

3.3.1.2 Direct Regeneration

The direct regeneration converter has been the subject of most research interest in SRM converters due to the flexibility and reliability of the operation [26, 79]. The Direct Regeneration converter is the most commonly used converter topology for SRMs. Some of the literatures which utilised this converter are described in references [24, 27, 82, 83].

In this configuration, the phase winding is connected to the DC link, and allows positive, negative and zero voltages to be applied to the phase windings. The component stress is rated at supply voltage (minus switch conduction drops). The converter is shown is Figure 3-14.

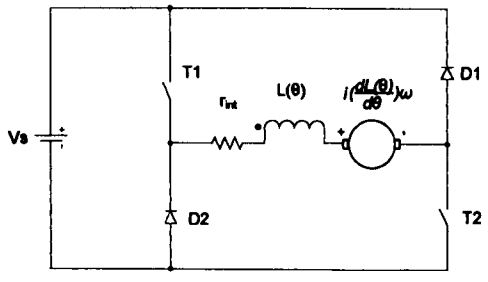


Figure 3-14- Direct Regeneration converter

There are a few variations of this converter. One such variation is the addition of a capacitor to boost the DC link voltage, and for the purpose of the classification, the converter has been included in the Capacitor Boost type of converters. Other variations of this class of converter are only applicable for multi phase machines [24], two of which are briefly mentioned in the next chapter.

The disadvantage of this circuit is that the component count per phase is high since there are always a minimum of two diodes and two switches. These components can be quite costly in a low power system [26]. Since two devices are always in series with the winding, conduction losses is nearly twice compared to a single switch solution. Another disadvantage is the floating gate drive that would be required by the top switching device.

The direct regeneration converter has three modes of operation.

Mode 1: Magnetisation by the source

The operation during this mode is represented in Figure 3-15 below. Both switches are turned on, and the current in the phase winding rises rapidly.

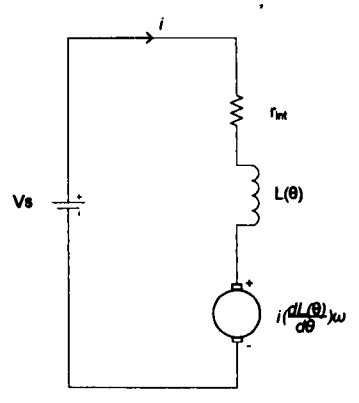


Figure 3-15- Direct Regeneration converter – Mode 1

The current equation during turn-on is as follows:

$$i(t) = I_{max}\left(1 - e^{\frac{-t}{\tau_1}}\right) \qquad (3\text{-}19)$$

where

$$I_{max} = \frac{V_S}{R} \tag{3-20}$$

$$R = r_{int} + \frac{dL(\theta)}{d\theta}\omega \tag{3-21}$$

$$\tau_1 = \frac{L(\theta)}{R} \tag{3-22}$$

Mode 2: Freewheeling

During this mode of operation, the top switch turns off and the energy freewheels through one switch and one diode (the equivalent circuit is shown in Figure 3-16). There is no flow of energy back into the supply. The demagnetisation proceeds very slowly through the winding resistance.

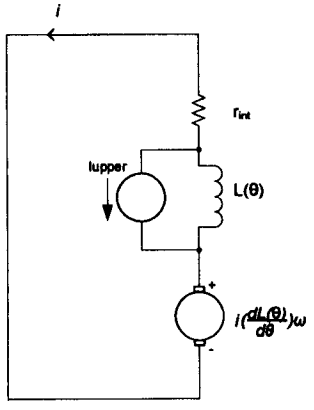


Figure 3-16- Direct Regeneration converter – Mode 2

Current flow is given by equation 3-21.

$$i(t) = I_{upper} e^{\frac{t}{\tau 2}} \tag{3-23}$$

where

$$\tau_2 = \frac{L(\theta)}{R} \tag{3-24}$$

$$R = r_{int} + \frac{dL(\theta)}{d\theta}\omega \tag{3-25}$$

Mode 3: Demagnetisation via freewheeling diodes

When both the switches are turned-off, the energy is returned back to the supply via the freewheeling diodes. The equivalent circuit is shown in Figure 3-17.

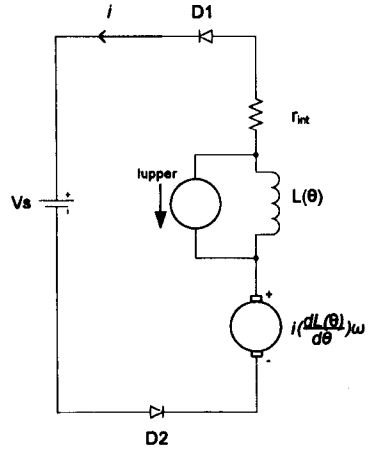


Figure 3-17- Direct Regeneration converter – Mode 3

The decaying current during turn-off is given by:

$$i(t) = I_{upper} e^{\frac{-t}{\tau_3}} - I_{\max}\left(1 - e^{\frac{-t}{\tau_3}}\right) \qquad (3\text{-}26)$$

where

$$I_{\max} = \frac{V_S}{R} \qquad (3\text{-}27)$$

$$R = r_{\text{int}} + \frac{dL(\theta)}{d\theta}\omega \qquad (3\text{-}28)$$

$$\tau_3 = \frac{L(\theta)}{R} \qquad (3\text{-}29)$$

During commutation, there are always two switching devices in series, and this will cause high conduction losses. However, in terms of the machine efficiency, it is still very high since the energy is recovered at the supply at the end of each commutation.

3.3.2. Active regeneration

Active regeneration implies that an intermediate stage is used to store the energy temporarily before returning it to the source. The intermediate could be just an additional component or a complete set of system such as a buck converter. This group of converters can be further split into two categories based on the different intermediate stages.

3.3.2.1 Capacitor Boost

In this topology, the energy from the offgoing phase is stored in a capacitor via a switch. This energy is then transferred directly to the motor windings.

The Capacitor Boost converter has received quite a lot of attention in the past. As the name suggests, a converter is classed as a Capacitor Boost circuit if there is an auxiliary capacitor in the circuit, whose primary function is to boost the DC link voltage. In an SRM it is desirable to have a converter which could demagnetise the commutating phase as quickly as possible [31]. This is somehow limited in the Direct Regeneration converter since the voltage available at the start of commutation is limited by the DC link. Also, with the Capacitor Boost, a single switch per phase solution is achieved compared to the high component count of the Direct Regeneration converter.

Early designs of the Capacitor Boost converters began with the C-dump converter for a poly-phase SRM described in literature [49]. Here, an inductor or a resistor is used to feed directly to the source. Another variation of this converter is described in [27, 84] which eliminates the DC link. Therefore the winding will receive the full rectified DC voltage. The boost capacitor will act as a dump capacitor, and will discharge to overcome the voltage shortfall over part of the rectified AC mains cycle. In [85] the dump capacitor is controlled by an SCR, and again this is another converter without the DC link. The converter is suitable for use with single and poly-phase machines.

A modification of the existing Direct Regeneration converter involves an auxiliary capacitor in parallel to the DC link voltage [86]. The additional voltage provided by the auxiliary capacitor will boost the DC link voltage especially during

turn-on and turn-off part of the machine. If the auxiliary capacitor is in series with the DC link [87], the auxiliary capacitor can be rated at a smaller voltage because the boost voltage is smaller. In [88], a similar topology with one less diode was proposed. The advantage of the circuit is cost reduction and a limited voltage stress across one of the switches, as this switch sees only the voltage difference between the boost voltage and the DC link voltage.

In [89] a split dc link topology is introduced where the DC link is replaced by two capacitors in series. The challenge with this circuit is to ensure the voltage is balanced over the common point, or some phase switching might be lost. The voltage ripple in this configuration is high. All these circuits are shown in Appendix A.

It is also possible to have the boost capacitor switched on and off by means of an additional switch and a diode [42, 84]. The converter is shown in Figure 3-18. The problems of this circuit are the reduction of switching frequency and losses in the dump switch, T2, and as the voltage stress across the devices gets higher, the control of the dump capacitor voltage gets more complicated. As a result, the dump capacitor needs to be rated at a higher voltage. However the operation of the converter is favoured because zero-voltage loop is possible, which means hysteresis losses and current ripple are reduced. An *et.al* [90] did a modification of the converter by addition of one more switch. This extra switch is used to control the current flow due to changes in the mutual inductance of the windings.

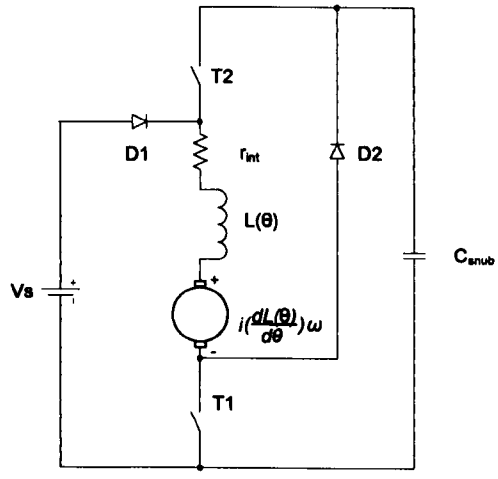


Figure 3-18- Capacitor Boost converter

The Capacitor Boost circuit in Figure 3-18 is chosen for the analysis because of its simplicity which has also made it a favourable topology for use in a automobile applications [91]. In this circuit, the energy freewheels into a capacitor, C at turn-off, effectively creating an additional voltage rail. The capacitor is then discharged at a later energisation process. The voltage on the capacitor is allowed to rise very quickly, thus increasing the turn-off voltage. At turn-on, the stored energy will boost the voltage applied to the phase winding. This process will decrease the switching advance angles. The reduction in the switching advance angle will improve the drive efficiency since less current is required to flow during the interval when the phase is not producing any torque. Alternatively, with the same advance angle, larger output power may be achieved. Therefore, for any given DC supply voltage, the boost capacitor will allow for the enhanced output performances of the SP-SRM [48].

At a glance, although this topology can be said to be costly since there are two switches per phase, at a closer inspection this is not entirely true. This is because the second switch has a lower rating since it is only effectively turned on to pass voltage to the capacitor at a relatively low voltage and its switching frequency is relatively low.

The disadvantage of this topology is that the control is complex (due to the capacitor voltage regulation and advance angle calculation) and the voltage rating of the components, particularly the additional capacitor, is high.

The operation of the converter can be described in four modes of operation.

Mode 1: Direct magnetisation

When the switch T1 is turned on, the source voltage is directly applied to the windings via D1. The equivalent circuit is shown in Figure 3-19.

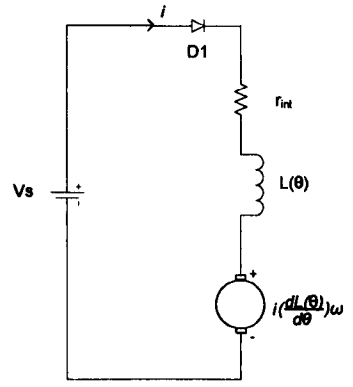


Figure 3-19- Capacitor Boost converter – Mode 1

The current equation during turn-on is as follows:

$$i(t) = I_{max1}\left(1 - e^{\frac{t}{\tau_1}}\right) \qquad (3\text{-}30)$$

where

$$I_{max1} = \frac{V_S}{R} \qquad (3\text{-}31)$$

$$R = r_{int} + \frac{dL(\theta)}{d\theta}\omega \qquad (3\text{-}32)$$

$$\tau_1 = \frac{L(\theta)}{R} \qquad (3\text{-}33)$$

Mode 2: Magnetisation from the capacitor

In this mode, both the switches T1 and T2 are turned on. The capacitor voltage which is larger than the source voltage causes the current to flow to the windings until the capacitor voltage becomes smaller than the rectifier voltage. Then, T2 is reverse biased and the operation of the circuit reverts back to Mode 1. The equivalent circuit is shown in Figure 3-20 .

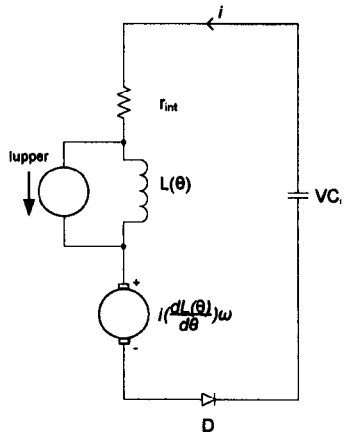


Figure 3-20- Capacitor Boost converter– Mode 2

The current equation during turn-on is as follows:

$$i(t) = I_{\max 2}\left(1 - e^{-\frac{t}{\tau_2}}\right) \tag{3-34}$$

where

$$I_{\max 2} = \frac{V_C}{R} \tag{3-35}$$

$$R = r_{\text{int}} + \frac{dL(\theta)}{d\theta}\omega \tag{3-36}$$

$$\tau_2 = \frac{L(\theta)}{R} \tag{3-37}$$

Mode 3: Freewheeling

The winding is shorted as the switch T2 turns on and D2 conducts. This energy freewheels slowly through the loop. Figure 3-21 illustrates the operation.

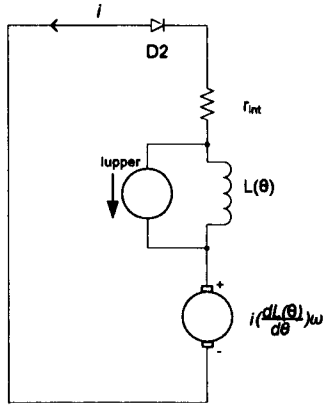


Figure 3-21- Capacitor Boost converter – Mode 3

Current flow:

$$i(t) = I_{upper} e^{\frac{-t}{\tau_3}} \qquad (3\text{-}38)$$

where

$$\tau_3 = \frac{L(\theta)}{R} \qquad (3\text{-}39)$$

$$R = r_{\text{int}} + \frac{dL(\theta)}{d\theta}\omega \qquad (3\text{-}40)$$

Mode 4: Demagnetisation by capacitor charging

Both the switches are turned off. The winding is demagnetised through D1, the capacitor, D2 and the source. Figure 3-22 shows the equivalent circuit.

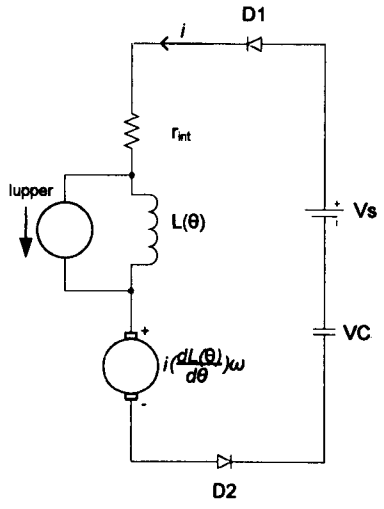


Figure 3-22 - Capacitor Boost converter – Mode 4

The demagnetisation current is given by:

$$i = I_{upper} e^{-\frac{t}{\tau}} - I_{max1}\left(1 - e^{-\frac{t}{\tau}}\right) - I_{max2}\left(1 - e^{-\frac{t}{\tau}}\right) \qquad (3\text{-}41)$$

where

$$I_{max1} = \frac{V_S}{R} \qquad (3\text{-}42)$$

$$I_{max2} = \frac{V_S}{R} \qquad (3\text{-}43)$$

$$R = r_{int} + \frac{dL(\theta)}{d\theta}\omega \qquad (3\text{-}44)$$

$$\tau = \frac{L(\theta)}{R} \qquad (3\text{-}45)$$

With the additional capacitors, the energy from the windings is never lost, but it is being used to boost the subsequent commutation. The small auxiliary capacitor means faster turn off times can be achieved. At turn on, advance angles can be reduced because the boost voltage can be applied to the windings to raise the current rapidly. Therefore, this topology is very useful to achieve higher output power, and since the energy is never lost, machine efficiency is also very high.

3.3.2.2 Hybrid Regeneration

Converters in this group are similar to the Capacitor Boost converter in the sense that it requires additional components on top of the energy storage element. The energy is then transferred back to the source via additional circuitry. As mentioned in Section 3.3.2.1, the Capacitor Boost converter functions by boosting the voltage during turn-on and turn off. However, this converter, with the help of the additional components, will enable voltage boosting in during either one of the two.

With the boosted voltage, all components need to have boosted ratings even when the boosted voltage is available only during turn-on or turn-off. The increase of component count is the major drawback of this converter type. The additional circuitry, which mostly includes an inductor, a capacitor and a switch, means that converter costs would increase. Figure 3-23 shows one configuration of the converter class.

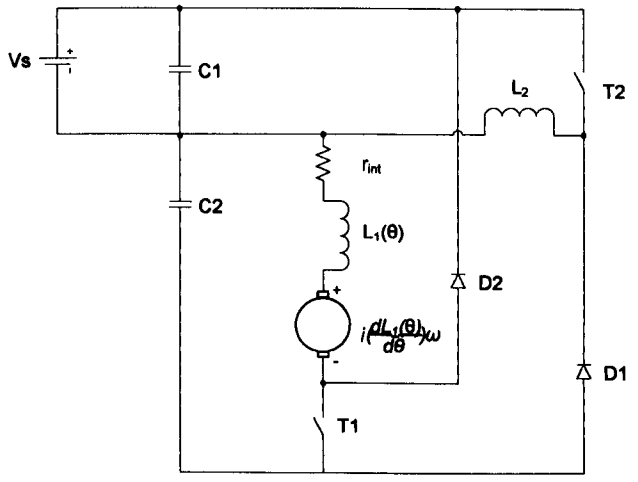


Figure 3-23- Hybrid Regeneration converter

This topology can also be classed as a dual rail converter [27]. L_2, T2 and D1 supply the second DC link capacitor C2. One advantage of having such configuration

is the extra controllability obtained by separating the magnetising (V_{C1}) and the demagnetising (V_{C2}) voltages. It is also possible to use the converter if the 0V-end of C1 is connected to the negative terminal of C2 [92].

It would also be possible to position the auxiliary capacitor in series or in parallel to the DC link capacitor [27, 78]. If it is connected in series, the auxiliary capacitor will only be used during de-energisation of the phase windings, and thus, can be rated at a lower voltage. If an extra diode is added to the circuit conduction path [44], it is claimed that the VA rating of the circuit could be reduced. Also, the auxiliary inductor L_2 could be eliminated. However, the additional diode voltage drop during conduction would mean this topology would be unsuitable in some low-voltage applications.

The operation of the circuit can be described in four modes of operation. The extra inductor is shown as L_2. L_2, T2 and D1 form the buck-boost chopper.

Mode 1: Magnetisation of the main winding

T1 is on, and therefore the voltage from C2 flows to magnetise the winding. Figure 3-24 illustrates the equivalent circuit. The equation of the winding current is:

$$i(t) = I_{max1}\left(1 - e^{\frac{t}{\tau_1}}\right) \qquad (3\text{-}46)$$

where

$$I_{max1} = \frac{V_S}{R} \qquad (3\text{-}47)$$

$$R = r_{int} + \frac{dL_1(\theta)}{d\theta}\omega \qquad (3\text{-}48)$$

$$\tau_1 = \frac{L_1(\theta)}{R} \qquad (3\text{-}49)$$

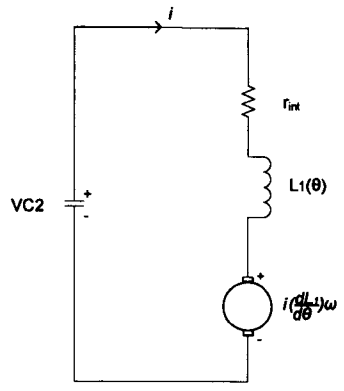


Figure 3-24- Hybrid Regeneration converter – Mode 1

Mode 2: Forced demagnetisation

During this period, T1 is turned off. D2 then conducts and the demagnetisation of the windings occurs and the magnetic energy flows to charge C1. This is shown in Figure 3-25 below. Voltage across T1 is $V_{C1} + V_{C2}$.

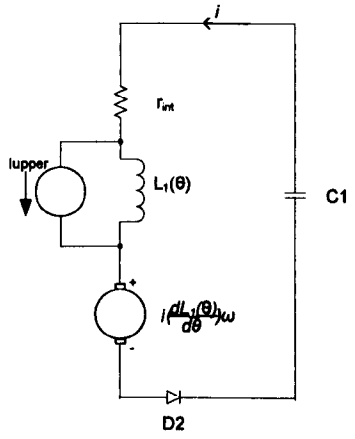


Figure 3-25- Hybrid Regeneration converter – Mode 2

The demagnetisation current is:

$$i = I_{upper} e^{\frac{t}{\tau 1}} - I_{\max 2}\left(1 - e^{\frac{t}{\tau 1}}\right) \qquad (3\text{-}50)$$

where

$$I_{\max 2} = \frac{V_{C1}}{R} \qquad (3\text{-}51)$$

$$R = r_{int} + \frac{dL_1(\theta)}{d\theta}\omega \qquad (3\text{-}52)$$

$$\tau_1 = \frac{L_1(\theta)}{R} \qquad (3\text{-}53)$$

Mode 3: Discharging of C1

T2 is turned-on, and the current builds up in L_2. Capacitor C1 discharges and the current flows through T2. The equivalent circuit is shown in Figure 3-26.

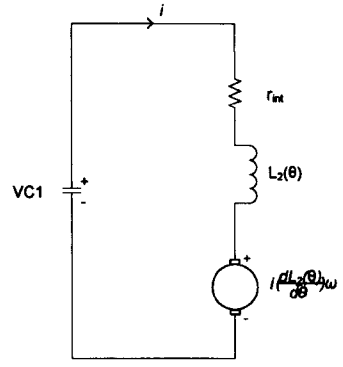


Figure 3-26- Hybrid Regeneration converter – Mode 3

The equation for the current increase in L_2 is:

$$i = I_{max2}\left(I - e^{\frac{-t}{\tau_2}}\right) \qquad (3\text{-}54)$$

where

$$I_{max2} = \frac{V_{C1}}{R} \qquad (3\text{-}55)$$

$$R = r_{int} + \frac{dL_2(\theta)}{d\theta}\omega \qquad (3\text{-}56)$$

$$\tau_2 = \frac{L_2(\theta)}{R} \qquad (3\text{-}57)$$

Mode 4: Charging of C2

T2 is turned-off, and D1 conducts. This causes the winding L_2 to become demagnetised. The stored magnetic energy flows to charge capacitor C2. The equivalent circuit is shown in Figure 3-27. Voltage across T2 is $V_{C1} + V_{C2}$.

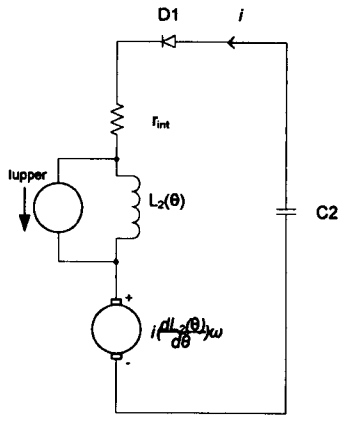


Figure 3-27- Hybrid Regeneration converter – Mode 4

The equation of current decay in L_2 is:

$$i = I_{upper} e^{\frac{-t}{\tau 2}} - I_{\max 2}\left(1 - e^{\frac{-t}{\tau 2}}\right) \qquad (3\text{-}58)$$

where

$$I_{\max 2} = \frac{V_{C2}}{R} \qquad (3\text{-}59)$$

$$R = r_{\text{int}} + \frac{dL_2(\theta)}{d\theta}\omega \qquad (3\text{-}60)$$

$$\tau_2 = \frac{L_2(\theta)}{R} \qquad (3\text{-}61)$$

At a glance, this circuit can be very complicated to implement. However, the inclusion of the additional stage means that the energy is always recycled, resulting in a high efficient SRD.

For the purpose of this work, this class of converter has not been considered since the additional components will increase the overall converter cost and decrease reliability.

3.3.2.3 Self-commutated Regeneration

The converter in this class (shown in Figure 3-28) uses resonant techniques in order to ensure commutation. Therefore, it is claimed that the losses and component stresses are reduced [24]. Here, self commutating switches may be used.

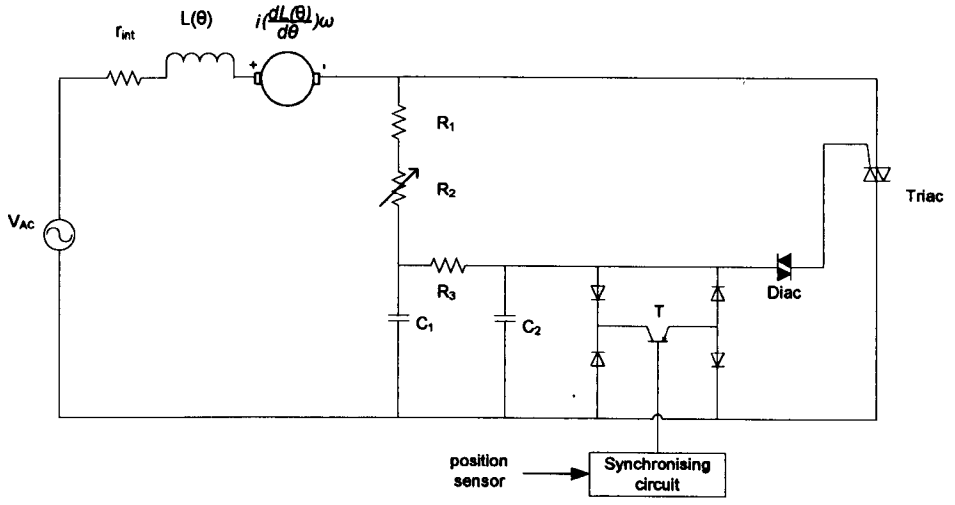


Figure 3-28 - The self-commutated regeneration converter

The advantage of this circuit is that the converter configuration is very simple, and relatively cheap components can be used [93].

However, the circuit has a disadvantage that the component count is high, and due to the complicated technique to regenerate the energy, some performance degradation is expected. This is proven by the limited speed control range of the machine, and some non-linearities in the control as mentioned in [93].

The circuit includes a triac and the commutation is controlled by the AC voltage. Therefore the drive speed is limited by the AC input frequency. This becomes another disadvantage of the circuit.

The converter mode of operation is dependent on the self-commutation of the triac. This differentiates this converter with the other converters in this review. The mode of operation of this converter is based on the method to turn-on and off the triac.

Mode 1: Turning-on of the triac

The firing of the triac is controlled by an RC circuit and a diac. Referring to Figure 3-28, the capacitor C2 is charged to the breakdown voltage of the diac; the charging time is dependent on the size of R_2. As this happens, the triac will be turned on based on the conduction period defined by the diac.

Mode 2: Turning-off of the triac

This happens just before the rotor poles align with the next stator poles. The triac is turned-off. This is implemented by short-circuiting C2 with the bridge circuit and a transistor, T. The transistor is controlled by a position sensor signal via a synchronising circuit. Once T is off, Mode 1 repeats.

For the purpose of this work, this class of converter has been excluded because of limited controllability.

3.4. Conclusion

In this chapter, converters for single-phase switched reluctance motor have been reviewed and the detailed operation has been explained by equivalent circuits and mathematical equations. The overview shows that all published SP-SRMs make use of the classical drive topology: diode bridge rectifier - dc-link capacitor - inverter. Only variations of the inverter have been proposed so far and the variations in each class have been described in this Chapter. It is apparent that all the topologies published must make use of a relatively large dc link capacitor in order to connect the rectifier circuit with the inverter.

In the next chapter, a more extensive analysis of each class of converter will be presented. Each of the converters will be simulated using PSpice, and their performance then compared.

CHAPTER 4
ASSESSMENT OF SINGLE PHASE SRM CONVERTER TOPOLOGIES

In Chapter Three, a family tree has been developed to classify the single phase SRM (SP-SRM) converters. This chapter presents simulation results of the introduced converters. The results of the simulations are used in order to assess converters for SP-SRMs in terms of efficiencies, voltage and current stresses, control complexity and cost. The Hybrid Regeneration and the Self-commutated Regeneration converters have been excluded because of their disadvantages in speed control and cost as already discussed in Chapter Three.

This chapter starts with Section 4.1 that describes the simulation program and the simulation set-up. In Section 4.2 a detailed analysis of each converter is presented. A first analysis is carried out using a static inductance giving a first indicator of the converter performance. In a second step, a variable inductance model of the SRM has been used. The chapter ends with Section 4.3 that concludes the converter assessment with discussion on the device ratings, control complexity, number of additional components and cost. The differences between the simulation results for static and variable inductance model are also discussed.

4.1. Simulation set-up

In this chapter, only selected waveforms are presented since the amount of waveforms that can be obtained would overwhelm the chapter. All presented topologies were simulated in Orcad/PSpice. This is a version of the analog circuit simulator developed at Berkeley, called SPICE (Simulation Program for Integrated Circuits Emphasis).

PSpice is a powerful software that is used to verify circuit designs and predict circuit behaviour in graphical form. It enables the design and simulation of analog and/or digital circuits based on physical models of electronic components. PSpice can be used for various analyses such as calculation of DC bias, DC/AC transient analysis or temperature sweep.

The normally applied analysis is the time domain transients where waveforms over time are observed. For this type of analysis, the transient output variables of the circuit such as currents, voltages and switching frequency are observed over a user specified time interval. The initial conditions are automatically determined by a DC analysis. To obtain the transient analysis, PSpice will conduct an iterative process until two conditions are satisfied:

1. the non-linear branch currents converge to within a tolerance of 0.1% or 1 picoamp ($1x10^{-12}$) whichever is larger
2. the node voltages converge to within a tolerance of 0.1% or 1 microvolt ($1x10^{-6}$) whichever is larger.

If one of the above conditions is not met, PSpice terminates the job and changes in the circuit schematics are required.

All test circuits use a voltage source at the input side to represent the DC link. Usually, this would be equivalent to an ideal voltage supply, a full wave diode bridge rectifier and DC link capacitor. However, as the performance of the prior art converters will be compared to the proposed converter in Chapter 5, the DC link voltage is set to be 600V. This is equivalent to the $2Vpk$ value used in the proposed converter in the latter chapter.

The main focus of this work is to obtain a detailed analysis of the different converter topologies. Throughout the simulation, the 1kW motor is modelled by a static inductor value (therefore no change in position) and a small winding resistance.

The simulation is performed with the minimum inductance value of a 1kW SP-SRM. The low inductance value was chosen to simulate the worst case scenario,

where smaller inductance will generate larger current and voltage stresses across the components. The value of the inductor initially used for the purpose of the simulation is 17mH. This was selected based on the practical values used in the references [22, 86]. The equivalent model for the SP-SRM for simulation purposes is shown in Figure 4-1. The 1Ω resistor is used as the voltage drop across it represents the current that is flowing through the load.

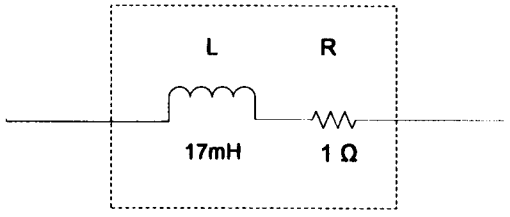


Figure 4-1 - SP-SRM model used in the simulation

In a real machine, switching only occurs during the dwell angle, θ_D of the rotor. The dwell angle is defined as the angle between the turn-on angle and the commutation angle (or turn-off angle). In the simulation, where the rotor signal is not present, this can be implemented by a clock signal. To determine the frequency of the clock signal, the following assumptions have been made on the machine:

SP-SRM type: 2/2 motor (two stator and two rotor poles)

SP-SRM speed: 1500 rpm

The entire conduction must be completed during one rotor pole pitch, α_P, and for this machine, the value is:

$$\alpha_P = \frac{2\pi}{N_r} = \pi = 180^\circ \qquad (4\text{-}1)$$

where N_r = number of rotor poles = 2

In this pole pitch, the permissible θ_D can be calculated as follows:

$$\theta_D = \alpha_P \cdot \frac{(1+\rho)}{2} = 90^\circ \qquad (4\text{-}2)$$

where ρ is the mean resistive volt drops due to resistance during θ_D, assumed to be zero.

Therefore, the time, t, needed to provide 90° of dwell angle for a 1500 rpm machine is:

$$t = \frac{60}{1500} \times \frac{90^\circ}{360^\circ} = 10ms \qquad (4\text{-}3)$$

Based on this calculation, the clock signal needs to have a frequency of 50Hz (period of 20ms) with 50% duty cycle. This is taken as the worst case.

All converters are simulated using a hysteresis current controller. An upper band and a lower band are set as reference values. The current through the SP-SRM is measured and compared with the reference. The current value is obtained by reading the voltage drop across the 1Ω resistor shown in Figure 4-1. Based on Ohm's Law, any voltage across a unit value of resistor will be equal to the current. The power switches are turned off when the upper band is reached, and turned on when the lower band is reached.

The calculation of the hysteresis window size is based on the pulsed current rating of the SP-SRM [94]. This is at least equal to the value of the maximum peak current of the drive. During chopping, the current can be approximated by periodically rectangular blocks of current. For a 1kW SP-SRM, the peak current per phase, I_p is calculated by:

$$I_p = \frac{P_d}{m\eta k_d V_N} = 5.88A \qquad (4\text{-}4)$$

where,

P_d = power output = 1kW

m = number of phase = 1

η = efficiency of the machine = assumed at 100%

k_d = duty cycle = 50%

V_N = assumed average voltage applied for 57% of the time, via chopping

Therefore, for the simulation, I_p is used as the average value of the hysteresis window.

As for the hysteresis current band, according to [95] only a few publications focused on the optimisation of hysteresis band level control. Therefore, for the simulation, the value of 6% ripple has been chosen for the hysteresis band as a compromise to limit torque ripple, switching losses, conduction losses and core losses [95].

4.2. Performance of converters

For the purpose of simulation of each circuit, it is assumed that all components are ideal except where specifically noted.

All topologies simulated are compared with the Direct Regeneration converter type. This is because the asymmetric half-bridge converter is accepted as the benchmark, as it is by far the most commonly used configuration for an SP-SRM converter

The simulation is done in two parts. Firstly, a static inductance is used as described in the section above. Then, the same simulation setup is applied but using a variable inductance model that has been described in Chapter 2.

4.2.1. Simulation with static inductance

The approach taken when doing the simulation with static inductance is initially to keep almost the same value of switching frequency in all the topologies. For further analysis of the topologies, the switching frequency was increased to find the limitations for each topology.

4.2.1.1 Resistor Dump

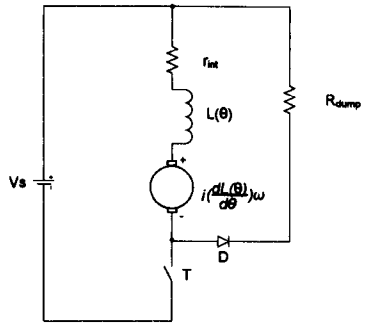


Figure 4-2- Resistor dump converter

Figure 4-2 shows the resistor dump converter. The size of the resistor in the converter determines the demagnetisation current fall time, the current through the freewheeling diode, switch stresses, and the power dissipation across the resistor. The power rating of the resistor is calculated at the worst case where all the energy from the winding is dissipated in the dump resistor.

As the value of the resistor increases, the current decays faster and vice versa. Therefore, as the switching frequency increases, the resistor value has to be increased to match the switching frequency increase.

The simulation result is shown in Figure 4-3. Here, two values of resistance have been provided for comparison. The figure shows the associated phase current waveforms for the two resistor values. Smaller resistances will cause longer switching current fall time. As discussed in the previous chapter, during the demagnetisation mode, the current decays with a time constant of τ, where:

$$\tau = \frac{L(\theta)}{R_W + \frac{dL(\theta)\omega}{d\theta} + R_D} \qquad (4\text{-}5)$$

$L(\theta)$ is the inductance, ω is the angular speed and R_D is the dump resistance. From this, we can see that small values of R_D will result in longer decay times.

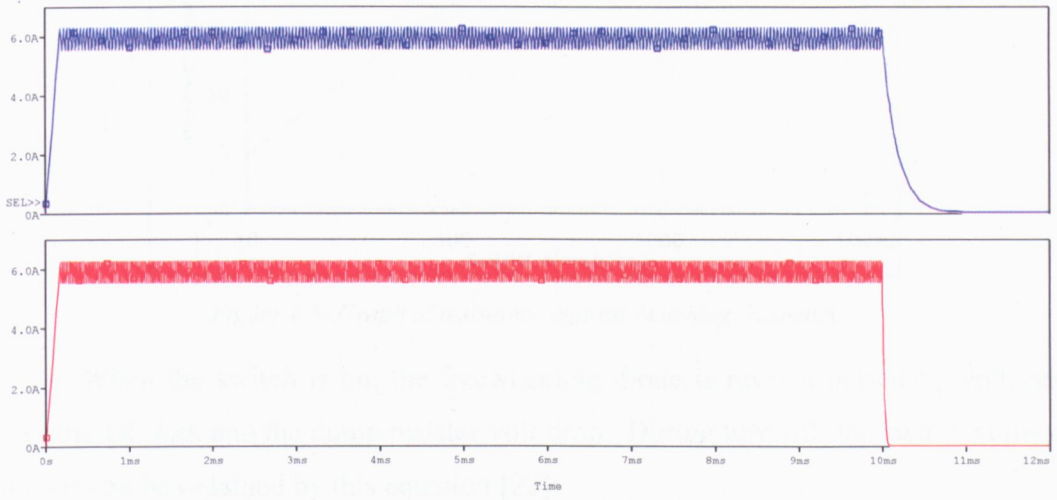


Figure 4-3- Phase current waveform using two values of resistors; (top) 100Ω (bottom) 1kΩ

It can be seen from the figure that the smaller resistor results in a lower switching frequency of 24.73 kHz compared to a frequency of 44.84 kHz using a ten times larger resistor. Also, the 100Ω resistor has a longer current turn-off time.

Figure 4-4 shows the relationship between resistor size and length of phase turn-off tail current. This clearly demonstrates that higher resistor value results in shorter current turn-off times. The next graph in Figure 4-5 shows the relationship between resistor sizes to the switching frequency. As the resistor size increases, the switching frequency will increase as well.

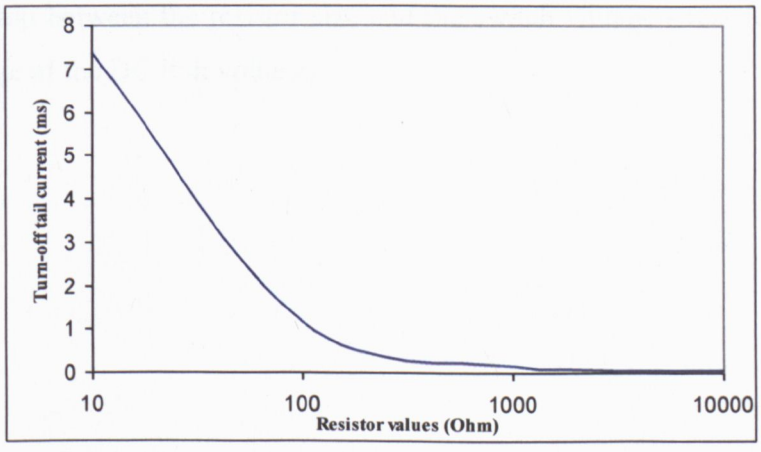


Figure 4-4- Graph of resistance against length of turn-off tail current

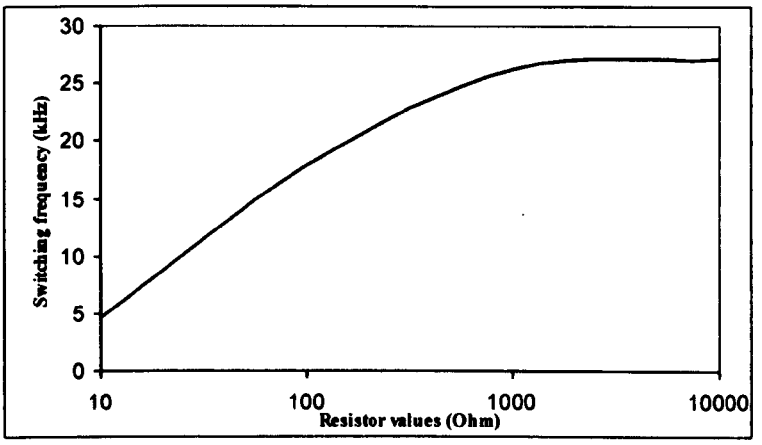


Figure 4-5- Graph of resistance against switching frequency

When the switch is on, the freewheeling diode is reverse biased by voltages from the DC link and the dump resistor volt drop. During turn-off, the switch voltage stresses can be obtained by this equation [22]:

$$V_{stress} = V_S + V_D + I_P R_D \qquad (4\text{-}6)$$

where V_S is the DC link voltage, V_D is the forward drop of the freewheeling diode, and $I_P R_D$ is the volt drop across the dump resistor.

Figure 4-6 shows the voltage across the switches when two different resistors are used. When a 100Ω resistor is used, the voltage is approximately twice the DC link voltage, but when a 1kΩ resistor is used, the voltage is nearly 7kV. From the waveforms it is clear that the voltage across the switch is larger if a larger resistor is used. It can be concluded that the use of a larger resistor results in higher voltage stresses across the switch and the freewheeling diode. The graph in Figure 4-7 shows the relationship between the resistor size and the switch voltage stress (calculated as the percentage of the DC link voltage).

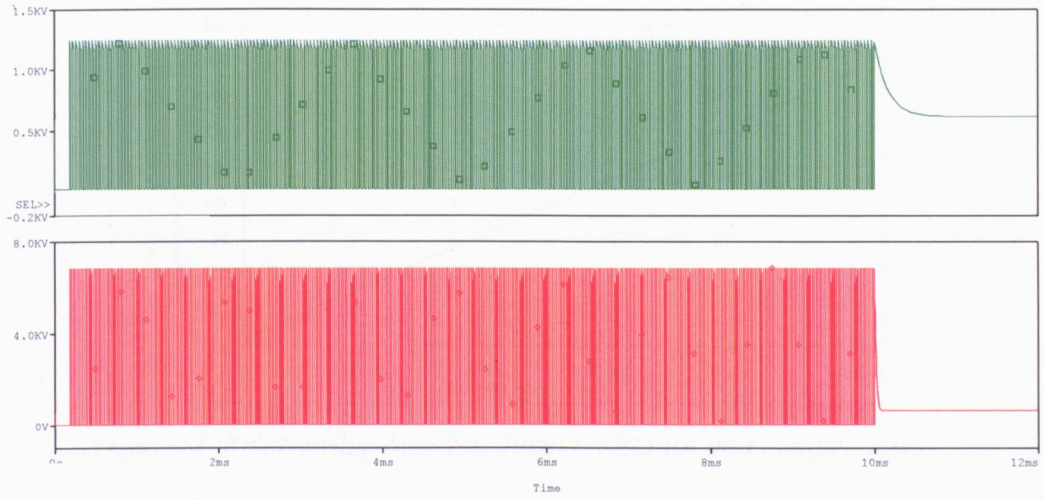


Figure 4-6- Voltage across the switches; (top) 100Ω (bottom) 1kΩ

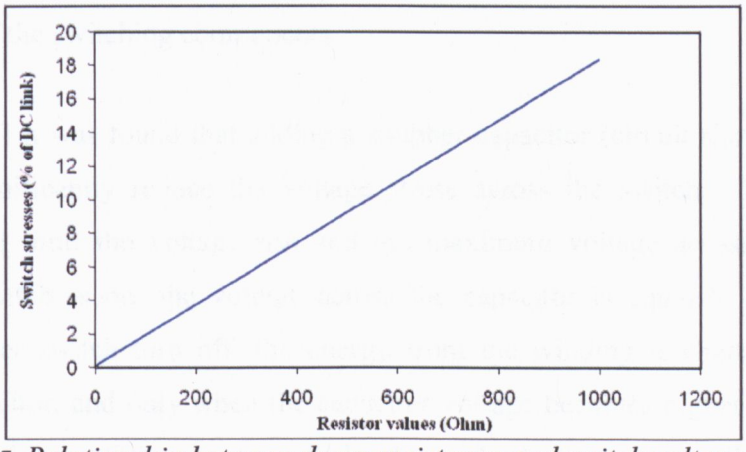


Figure 4-7- Relationship between dump resistance and switch voltage stresses

The average power rating, P_D of the resistor is calculated when the stored energy is dissipated in the dump resistor during every switch turn-off. It can be calculated as:

$$P_D = I^2 R_D \qquad (4\text{-}7)$$

where I is the average demagnetising current and R_D is the dump resistance.

The graph in Figure 4-8 shows the relationship between resistor sizes and the dumped power based on the simulated values. The bigger the resistor, the larger power can be dumped.

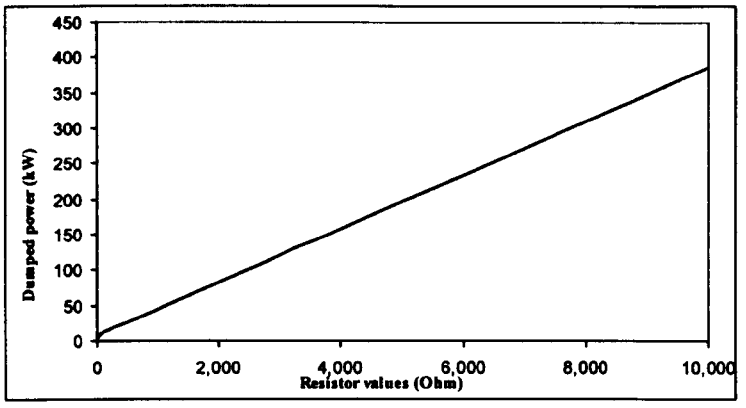


Figure 4-8- Relationship between dump resistance and dumped power

Figure 4-5 to 4-8 shows that careful consideration of the size of the resistor is very critical to the efficiency and torque production, the voltage ratings and the power dissipation of the switching components.

In [77] it was found that adding a snubber capacitor (circuit shown in Figure 4-9) will significantly reduce the voltage stress across the switch. This snubber capacitor will limit the voltage rise and the maximum voltage across the switch. When the switch is on, the voltage across the capacitor is equal to the DC link voltage. After switch turn off, the energy from the winding is channelled to the snubber capacitor, and only when the capacitor voltage becomes higher than the DC link voltage, the remaining energy will be dumped into the resistor. Therefore, the circuit limits the switch stress because the voltage across the switch is now the voltage across the snubber capacitor plus the forward volt drop of the diode.

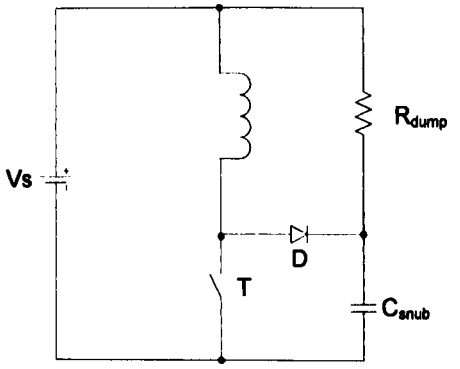


Figure 4-9- Resistor dump circuit with snubber capacitor

One drawback is that immediately after turn-off the circuit is effectively an RLC circuit and the rate of de-energising the inductor will depend on the RLC time constant.

4.2.1.2 Zener Diode Dump

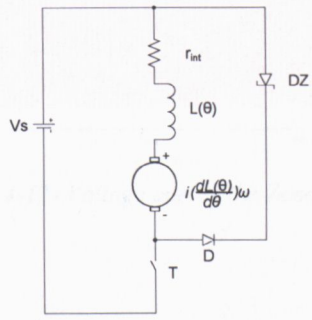


Figure 4-10- Zener diode dump converter

A Zener diode dump converter is shown in Figure 4-10. In this configuration, a Zener diode, *DZ*, is used to replace the dissipative resistor used in the resistor dump converter. The Zener diode behaves like a voltage source and this energy together with the demagnetising energy from the windings, will force the current decay times during turn-off to be reduced (as demonstrated in the mathematical analysis in Chapter Three). Figure 4-11 shows the load current waveform of a typical Zener diode dump converter.

The voltage across the Zener diode is shown in Figure 4-12. The Zener diode used this analysis is assumed to have a breakdown voltage (V_Z) of 35V. This is assuming two Zener diodes in series, each having a V_Z of 17.5V. In the simulation, the Zener is represented by a voltage source of 17.5V. The simulation waveform shows the voltage across the Zener is (V_Z + (Vs - V_Z)).

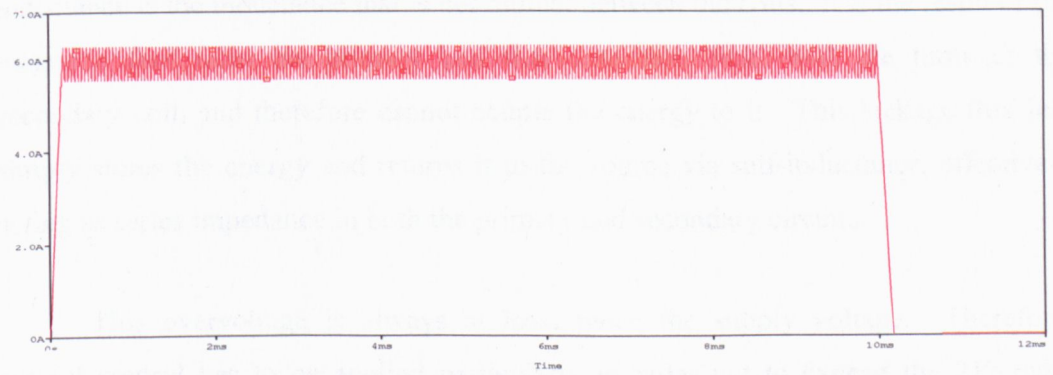


Figure 4-11 - Load current waveform of a typical Zener diode dump converter

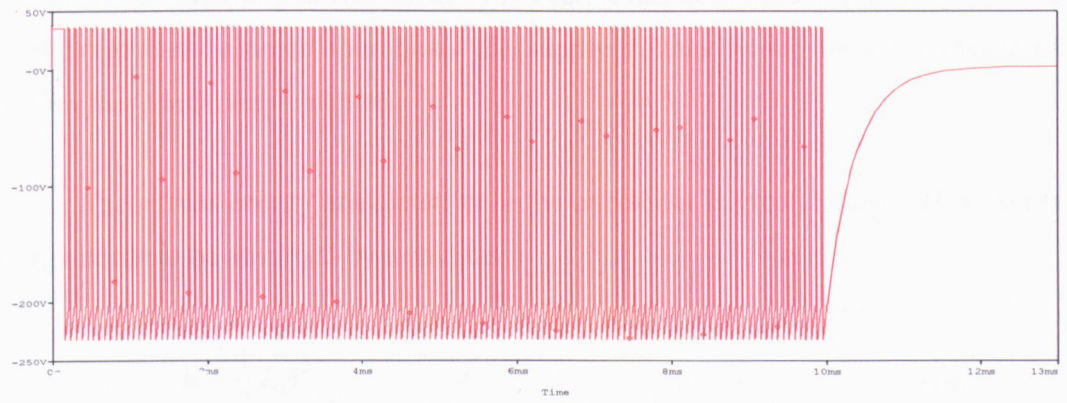


Figure 4-12- Voltage across the Zener diode

4.2.1.3 Magnetic (Bifilar) Regeneration

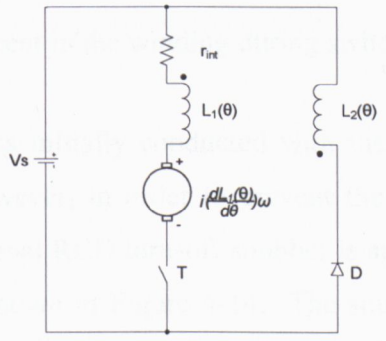


Figure 4-13- Magnetic (bifilar) regeneration converter

Figure 4-13 shows the magnetic (bifilar) regeneration converter topology. Employing a bifilar phase winding would be one of the simplest converter topology if perfect coupling is assumed. As previously mentioned in Chapter 3, unless the motor windings are closely coupled, the associated leakage inductance will cause overvoltages across the power switch especially during turn off. Leakage or *stray* inductance is the inductance that is not mutual between the coils. It is the result of the magnetic flux from the primary coil that does not 'link' with the turns of the secondary coil, and therefore cannot couple the energy to it. This leakage flux just simply stores the energy and returns it to the source via self-inductance, effectively acting as series impedance in both the primary and secondary circuits.

This overvoltage is always at least twice the supply voltage. Therefore, careful control has to be applied particularly in order not to exceed the $2V_S$ rated

voltage of the switching device used. However, it has been observed in [25] that this overvoltage can be up to four times the supply voltage which limit the choice of devices that can be implemented.

The excess energy associated with the overshoot is given below. This excess energy needs to be absorbed by a snubber.

$$E = \frac{1}{2} L_L i^2 \qquad (4\text{-}8)$$

where

L_L = leakage inductance of the bifilar winding

i = current in the winding during switch off

Simulation work was initially conducted with the bifilar windings having a unity coupling factor. However, in order to prevent the large voltage spike at the power switches, a conventional RCD turn-off snubber is applied [80, 96]. The circuit with the RCD snubber is shown in Figure 4-14. The snubber consists of a snubber capacitor, C_{snub}, a resistor and two diodes, D_a and D_b. The overvoltage is absorbed in the snubber capacitor, C, as given by:

$$\frac{1}{2} C\left(V_{max}^2 - V_{min}^2\right) = \frac{1}{2} L_L i^2 \qquad (4\text{-}9)$$

where V_{max} is the maximum voltage across the snubber capacitor and V_{min} is the minimum voltage across the snubber capacitor.

During switch turn-on, current is flowing in L1 and the snubber capacitor discharges through the resistor, R. When the switch, T, turns off, the energy is diverted from T into the snubber capacitor. Subsequently, current in coil L1 commutates into coil B, and allows the recovery of energy into the source.

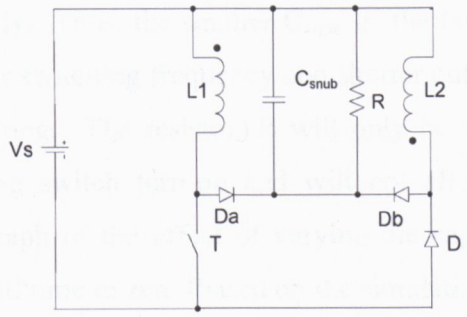


Figure 4-14- Magnetic (bifilar) regeneration converter with RCD snubber

Figure 4-16 shows the phase current using a 200uF capacitor and 300Ω resistor. Figure 4-16 shows the voltage across the switch, T, where there is no voltage overshoot during switching.

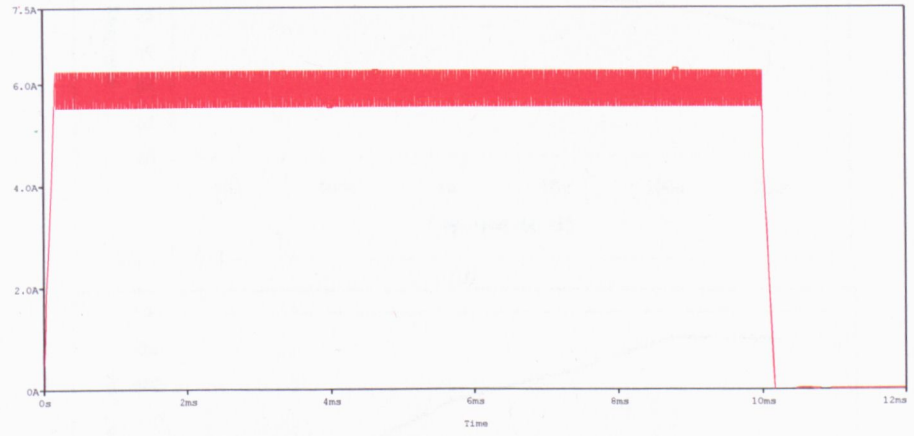


Figure 4-15- Phase current waveforms

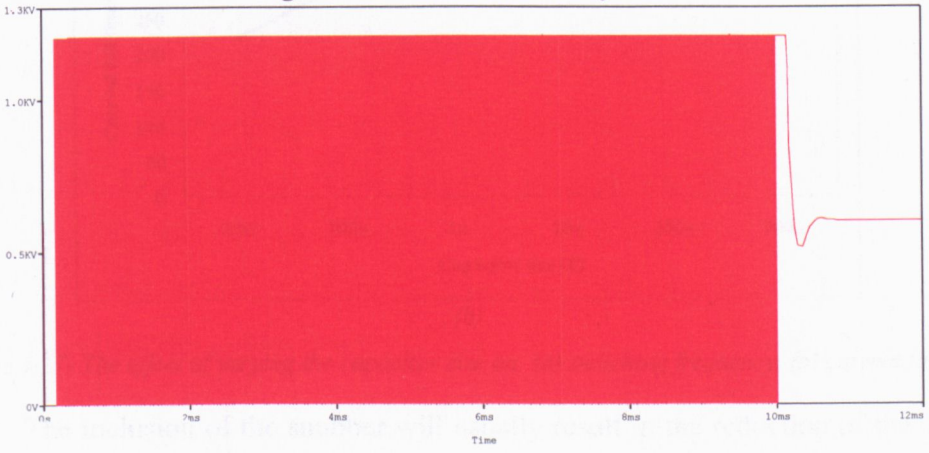


Figure 4-16- Voltage across the switch

The critical component in the snubber design is the capacitor. The snubber capacitor voltage is designed so that V_{min} is at least the DC link voltage. During switch turn-off, the energy from L1 will discharge into the snubber capacitor. Only when the voltage across L1 is equal to the DC link voltage, current will flow in L2 returning the

energy back to the supply. Thus, the smaller C_{snub} is, the faster is the current decay. This will result in higher switching frequency and shorter current decay to zero at the end of the phase switching. The resistor, R will only be used for discharging the snubber capacitor during switch turn-on and will not affect the winding current. Figure 4-17 shows a graph of the effect of varying the capacitor size to switching frequency and current fall time to zero (based on the simulations).

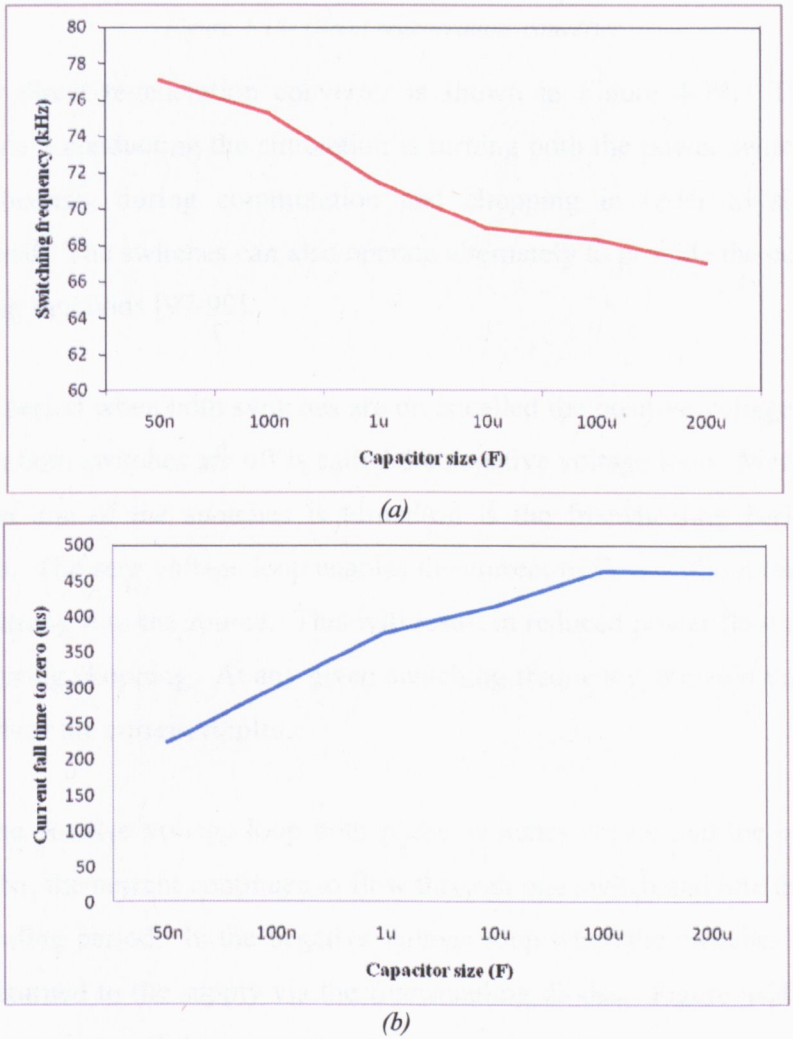


Figure 4-17- The effect of varying the capacitor size on; (a) switching frequency, (b) current fall time

The inclusion of the snubber will usually result in the reduction of the overall power output of the motor by about 5 – 10% [25, 80] and some cost increase.

4.2.1.4 Direct Regeneration

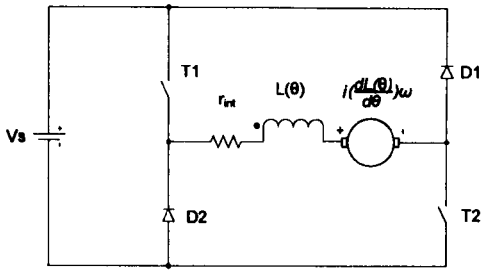


Figure 4-18- Direct regeneration converter

The direct regeneration converter is shown in Figure 4-18. The strategy employed when conducting the simulation is turning both the power switches on and off simultaneously during commutation and chopping in order to simplify the controller used. The switches can also operate alternately to provide the commutating and chopping functions [97-99].

The period when both switches are on is called the positive voltage loop. The period when both switches are off is called the negative voltage loop. Meanwhile, the period when one of the switches is turned-on is the freewheeling period or zero voltage loop. The zero voltage loop enables the current to flow without taking energy from or returning it to the source. This will result in reduced power flow to and from the motor during chopping. At any given switching frequency, the zero voltage loops will also reduce the current ripples.

In the positive voltage loop both phase switches are on and the current rises rapidly. Next, the current continues to flow through one switch and one diode during the freewheeling period. In the negative voltage loop when the switches are off, the current is returned to the supply via the freewheeling diodes. Figure 4-20 shows the simulation waveforms of the converter.

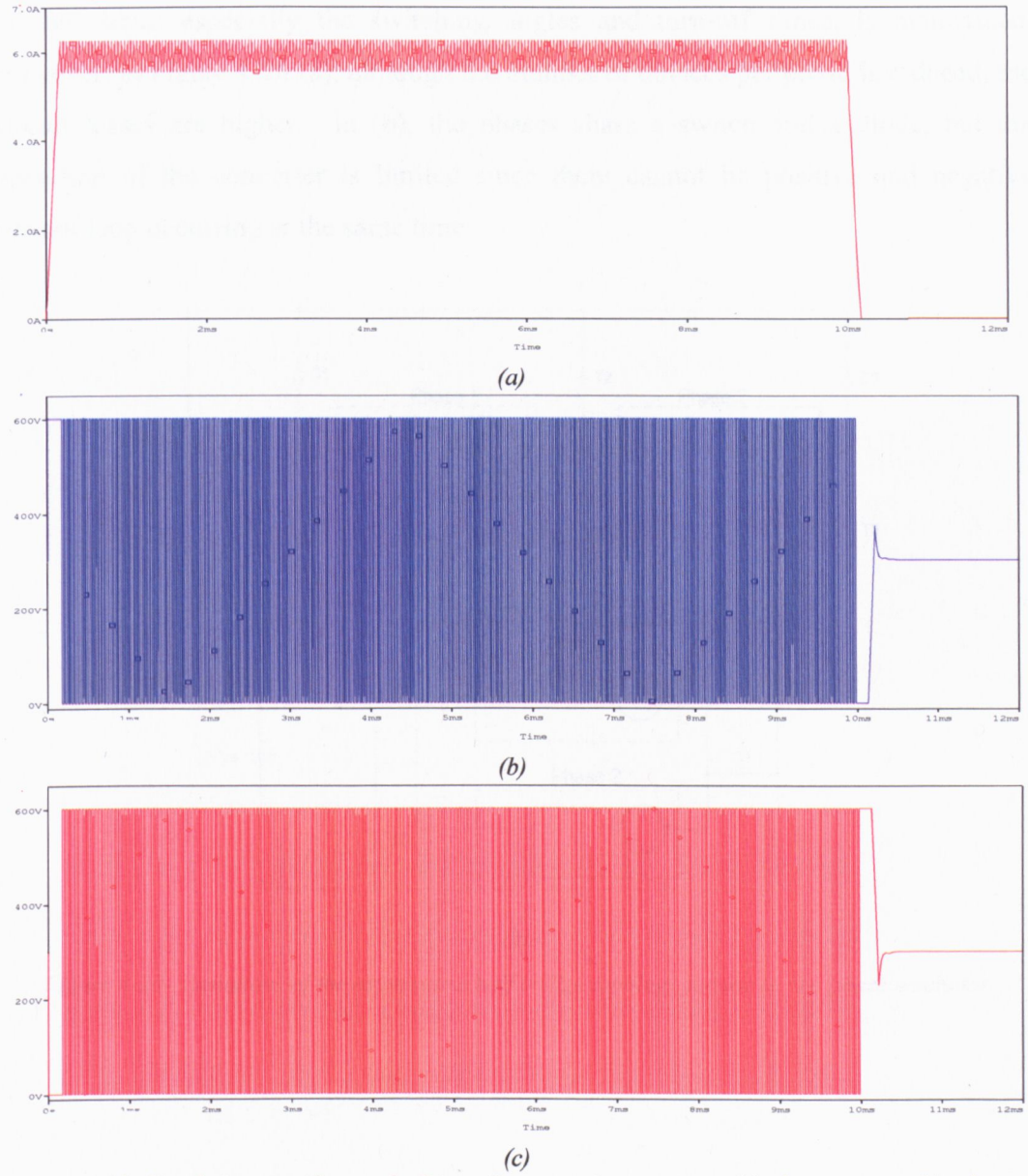


Figure 4-19- Simulation waveforms of a Direct Regeneration converter (a) phase current (b) voltage across diode D1 (c) voltage across switch S1

It can be seen from the results that the diodes D1 and D2 and the switches T1 and T2 can be rated at the supply voltage. However, the switches have high conduction losses because there are always two switches in series during each switching.

Modifications on this circuit will enable it to be used for machines with higher number of phases which is not the scope of this work, but is mentioned here to highlight that the developments in this topology is not geared towards modifying the circuit but instead making it more useful in multiple phases application. Figure 4-20 shows the variation of this topology for use with two-phase machines. The flexibility

of the circuit especially the switching angles and turn-off times, is maintained. However, in Figure 4-20 (a), although the number of devices per phase is reduced, the circuit losses are higher. In (b), the phases share a switch and a diode, but the operation of the converter is limited since there cannot be positive and negative current loop occurring at the same time.

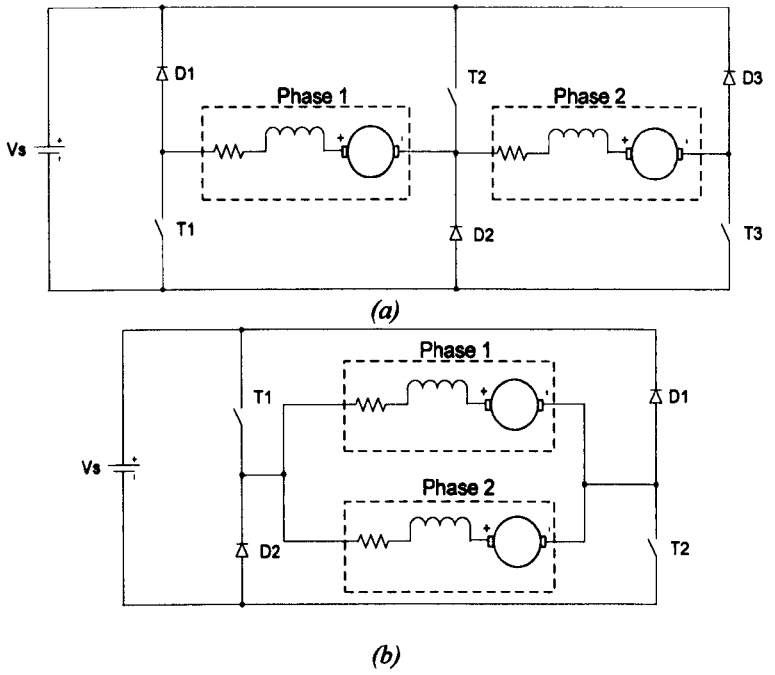


Figure 4-20- Variations of the asymmetric half bridge topology for use in two phase machines

4.2.1.5 Capacitor Boost

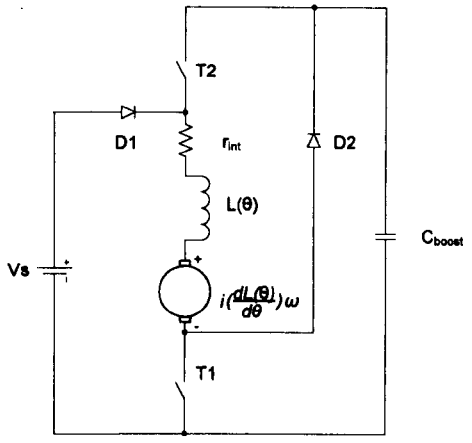


Figure 4-21- Type B.2.1 converter

The converter is shown in Figure 4-21. The main challenge in this topology is the control of the capacitor voltage as demonstrated in [42, 100]. It is established that the controller needs to ensure rapid evacuation of the stored magnetic energy during the off going phase. Only then, would this topology be advantageous compared to the asymmetric half bridge.

During the period where both switches are off, there is no control over the capacitor voltage except by the defined capacitance. Voltage across the capacitor is monitored so that if it is lower than the value of *Vs*, the switch T2 will be closed. Once the voltage exceeds *Vs*, T2 will turn-off, and the winding will be energised by the supply. As seen in the simulation results shown in Figure 4-22, the capacitor voltage keeps on increasing after each phase switching. However, in order to control the capacitor voltage, the LC time constant of the circuit during turn-on of T2 has to be taken into account. Having such elaborate control will therefore result in a higher cost converter.

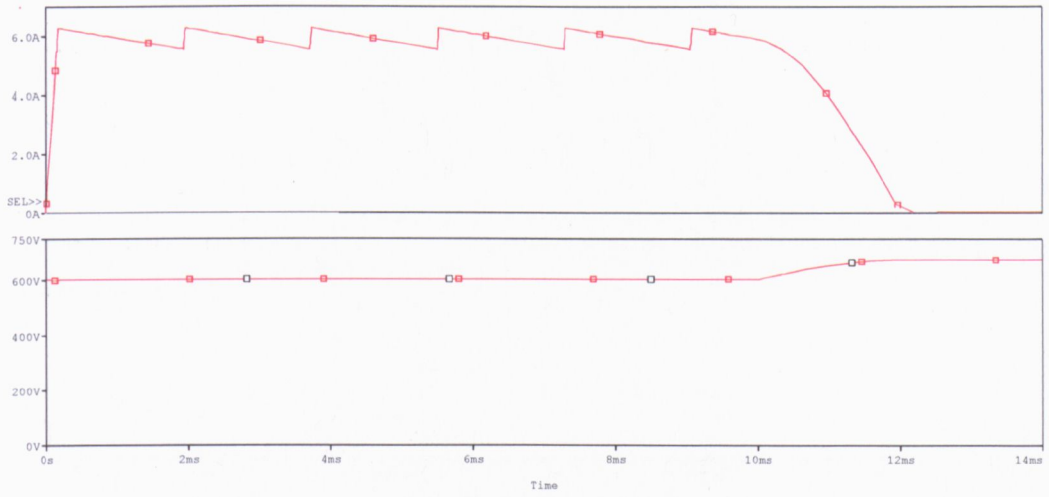


Figure 4-22- Simulation results showing the phase current (top) and the voltage across the capacitor (bottom)

It is found that the switching frequency is only approximately 3% the switching frequency of those investigated in the other topologies. Even if the capacitance value is changed, the frequency remains the same. Therefore, this is the limit of the simple controller that has been used in the simulation. If the complexity of the controller is to be increased, it could be possible to match the switching frequency to some extent, but this would mean the converter cost would have to increase as well.

Figure 4-23 shows the results over three switching periods. The capacitor is never really fully discharged. So, it will keep on increasing. This is the limit of the simple controller used in the simulation. A solution to this might be to add a resistor in parallel to allow for dumping of the excessive energy.

Another observation with this topology is, with higher voltage across the capacitor, less time is needed to build up the current in the ongoing phase where advance firing angle of the switching is necessary. Therefore, the converter becomes highly efficient.

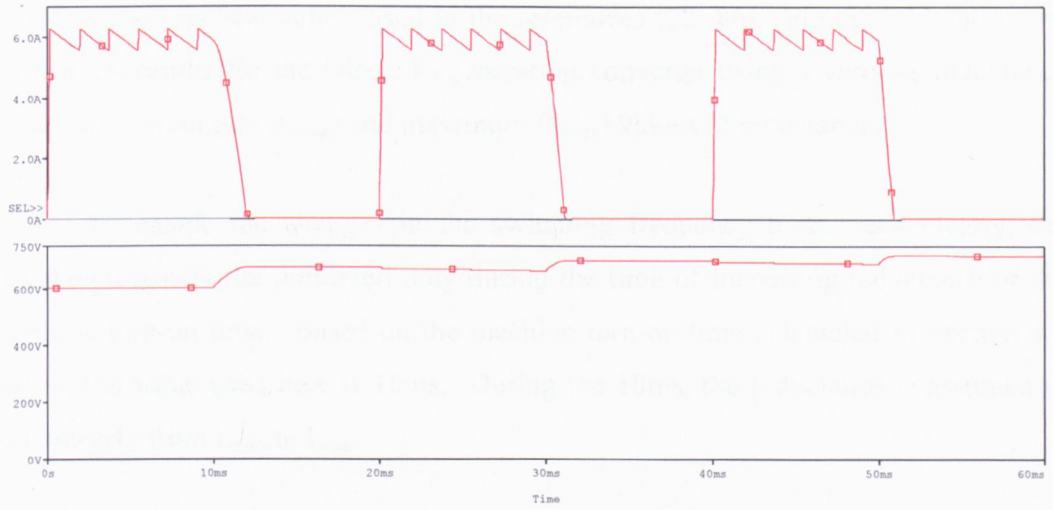
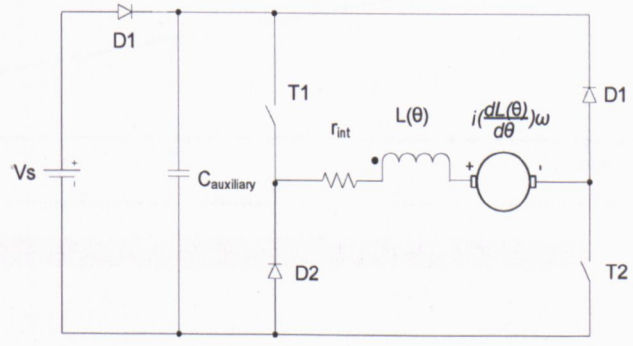


Figure 4-23- Simulation results showing the phase current (top) and the voltage across the capacitor (bottom) within three phase switchings

This is especially true with another variation of the capacitor boost circuit [86] (Figure 4-24) that has an auxiliary capacitor in parallel to the DC link. When switches are off, the windings de-energise into C_b and VC_b is at its maximum value. When the switches are on, the motor windings are energised rapidly by the high voltage at C_b. Current will then flow from the DC link into the windings, after VC_b is fully discharged. Therefore, the rapid charging and discharging of the windings using the higher voltage of VC_b ensures that the turn-on and turn-off times are faster, and enables the machine to be used at higher speeds. This circuit also represents the classical Direct Regeneration converter discussed in section 4.2.1.4.



1.

Figure 4-24- Another variation of capacitor boost circuit [86] with an parallel DC link auxiliary capacitor

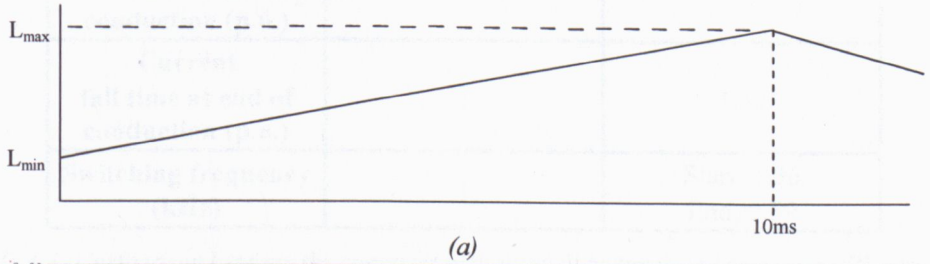
4.2.2. Simulation with variable inductance

The same simulation settings have been applied to all circuits but this time, a variable inductance model as described in Chapter 2 is used. The value of minimum inductance is 11.7mH, and the maximum inductance is 30mH. This has been selected

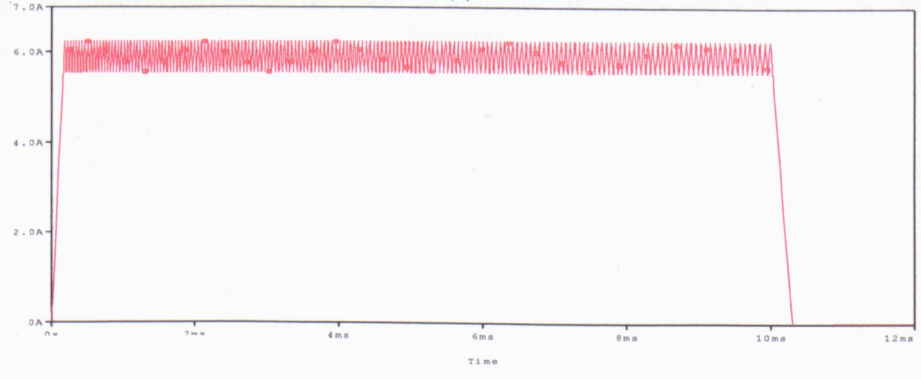
based on the practical values used in the references [22, 86]. Figure 4-25 shows the simulation results for the Direct Regeneration converter using a variable inductance model with minimum (L_{min}) and maximum (L_{max}) values of inductance.

To enable the changes in the switching frequency to be seen clearly, the simulation results are presented only during the time of increasing inductance or the machine turn-on time. Based on the machine turn-on time calculated in Section 4.1 above, the value used here is 10ms. During the 10ms, the inductance is assumed to rise linearly from L_{min} to L_{max}.

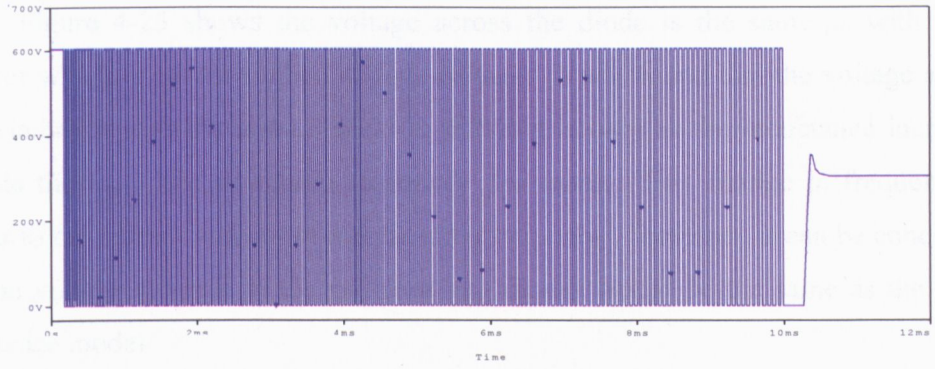
The discussion on the performance of the converter in this section is based on the differences with the converter using a static load. It can be observed in the converter with a variable inductor that the current rise time (107.78μs) is faster than the current fall time (225.4μs) due to the different values of inductance at the start and the end of the phase conduction. Moreover, it can be seen from the curve of voltage across D2, the positive voltage has been applied to the phase at turn on for shorter time than the negative voltage at turn off. This is due to the energy that is taken out of the phase at turn off is greater than the energy required to energise the phase at turn on.



(a)



(b)



(c)

Figure 4-25- Simulation of Direct Regeneration converters using variable inductance model (a) variable inductance profile; (b) the current through the load inductor (c) voltage across diode D2

Table 4-1 compares the two converters. In comparison with the converter with static inductor, at the start of the conduction, as expected, the current rise time of the converter with variable inductor is much faster since the inductance is lower at the start of conduction. The current fall time for the converter with the variable inductor is also longer since at the end of the conduction, the inductance value is bigger. However, the switching frequency is 136% larger at the start of phase conduction, and 59% less at the end of phase conduction, when compared to the static inductor.

	Static Inductor	**Variable Inductor**
Current rise time at start of conduction (p.u.)	1	0.6
Current fall time at end of conduction (p.u.)	1	1.32
Switching frequency (kHz)	1	Start: 1.36 End: 0.59

Table 4-1- Comparison between the converter with static inductance and converter with variable inductance

Figure 4-25 shows the voltage across the diode is the same as with static inductor which is equals to the DC link voltage. It was found that the voltage across the switches is also the same. What is different is only as the inductance increases towards the L_{max}, the switching frequency decreases. This change in frequency is similar to the current waveform mentioned previously. Therefore, it can be concluded that the voltage stresses of the switches and diodes would be the same as the static inductance model.

Similar observations were achieved with the other topologies. Although the impedance will change with the inductance value, the amplitude of the voltage and current will remain the same for all topologies because of the defined upper and lower current hysteresis thresholds.

4.3. Conclusion

Sections 4.1 and 4.2 gave an analysis of all converter topologies. To enable a direct comparison of the topologies, Table 4-2 is presented which gives a summary of the prominent advantages and disadvantages of each converter class.

From this table, it can be concluded that although each class of converters has many advantages, there are also significant disadvantages which may hinder their application in mainstream products.

<table>
<tr><th>Converter Class</th><th colspan="2">Advantages</th><th>Disadvantages</th></tr>
<tr><td>Resistor Dump</td><td colspan="2" rowspan="2">• simple configuration
• one switch</td><td rowspan="2">• energy wasted
• low efficiency
• additional snubber may be required</td></tr>
<tr><td>Zener Diode Dump</td></tr>
<tr><td>Magnetic (bifilar) Regeneration</td><td rowspan="4">• energy is recovered</td><td>• one switch
• good high speed operation</td><td>• complex construction
• additional snubber may be required</td></tr>
<tr><td>Direct Regeneration</td><td>• component rated at supply voltage</td><td>• high conduction loss
• floating gate drives required</td></tr>
<tr><td>Capacitor Boost</td><td>• good high speed operation</td><td>• complex control
• high component voltage rating</td></tr>
<tr><td>Hybrid Regeneration</td><td>• good voltage regulation at low speeds</td><td>• very complex control
• very high component count</td></tr>
</table>

Table 4-2- Summary of converter class advantages and drawbacks

Based on the theoretical work, simulation results and previous publications, the following comparison was made.

Previous publications seem to point at having the lowest component count as the main strategy to achieving a low cost converter. From the family tree, it can be seen that magnetic (bifilar) regeneration converter matches the direct regeneration converter for having 1 p.u. component count. The capacitor boost converter has 1.25 p.u. component counts because of the extra inductor, capacitor and switch. The rest of the converters have less component count.

In terms of the control drives (apart from the Hybrid Regeneration Converter), control for all the other converters are easily achieved. This could mean controller using analog devices or basic microprocessors e.g. PICs may be implemented.

The component involved during phase turn on and turn off will influence the current rise time and current fall time to zero. The shortest current rise time is achieved by the capacitor boost converter. In this topology, using an auxiliary

capacitor will produce boosted voltage to allow current to commutate quickly. However, the current fall time to zero is the worst among the topologies. This is because the demagnetisation occurs by natural commutation and not by external factors such as a boosted negative voltage which could quickly forces the flux to reduce to zero.

It was seen in the simulation results that for the resistor dump converter, Zener diode dump converter and the magnetic (bifilar) regeneration converter, additional snubbers are required. This leads to an increase in complexity of the controller as more parameters need to be considered. Also, the addition of the passive components of the snubber makes the circuit less reliable and costly.

Table 4-3 provides a comparison of the topologies according to a variety of performance metrics. Table 4-4 shows the voltage ratings of the components in the converters.

	Component count (p.u.)	Control Drive	Current rise time (p.u.)	Winding voltage during energisation (p.u.)	Current fall time (p.u.)	Winding voltage during deenergisation (p.u.)	Switching frequency (p.u.)
Direct Regeneration	1	Easy	1	1	1	1	1
Resistor Dump	0.75	Easy	1	1	3.43	1	1
Zener Diode Dump	0.75	Easy	1	1	3.44	1	1
Magnetic (bifilar) regeneration	1	Easy	1	1	1	1	1
Capacitor Boost	1.25	Moderate	0.72	1.5	3.69	1	0.07

Table 4-3- Comparison of SP-SRM converters based on simulation

The switching frequency of all converters has been made the same throughout the comparison in order to achieve a comparable result. However, as shown from simulation results in Table 4-3, the best match for the switching frequency for the capacitor boost converter is only 7%. As explained before, the equivalent circuit used

in the simulation is considered sufficient for the purpose of obtaining a direct comparison with the other topologies.

	S1 (p.u.)	S2 (p.u.)	D1 (p.u.)	D2 (p.u.)	Da (p.u.)	R1 (p.u.)	Cb (p.u.)
Direct Regeneration	1	1	1	1	-	-	-
Resistor Dump	2	-	1	-	-	1	-
Zener Diode Dump	2	-	0.81	-	-	-	-
Magnetic (bifilar) regeneration	1	-	1	-	-	-	-
Capacitor Boost	1.96	0.96	1.85	-	0.85	-	1.96

Table 4-4- Voltage rating comparison between SP-SRM converters

Simulation with the variable inductor simulates the machine more accurately. As what would be expected, the switching frequency would be higher if a smaller inductance is used and vice versa. The equivalent circuit of the machine during switching could be reduced to just a voltage source, and inductor and a resistor. Therefore, the rate of current increase and decrease is dependent on the τ, given by $\frac{L}{R}$. With a smaller τ, the rate would be smaller, and this in turn reflects on a shorter current rise time and fall time.

For the purpose of just looking into detail on the behaviour of the converter, it is sufficient to look at the results of the simulation using a static inductor to model the SP-SRM. This has enabled a direct comparison to be made.

Each topology can be seen to be unique in its own sense. If cost is to be the priority, the most economical choice must be made but still within limits of the application.

From the machine background in Chapter 2, and further analytical results in Chapters 3 and 4, it is shown that SP-SRM can be manufactured at low-cost but with limitations in performance. Cost reduction was so far driven on reducing the number

of switches in the inverter. The inverter, however, is only one sub-system of the SP-SRM. Reduction in cost of the rectifier and the dc-link capacitor has not been considered in SP-SRM. In Chapter 1 it was identified that the dc-link capacitor is the most expensive component. Therefore, this research work focused on a new circuit that allows a reduction in cost of the capacitor by developing a new SP-SRM topology.

In the next chapter, the new SP-SRM converter topology is presented. The theory behind the circuit is discussed, and further analysis is done via simulation to verify its operation for use with an SP-SRM.

CHAPTER 5
NOVEL CONVERTER TOPOLOGY

5.1. Overview

The converter classification described in Chapter 2 is an overview of the types of converters available for SP-SRMs. In the consecutive two chapters, detailed analysis of each converter has confirmed that all converters are capable of supplying pulsed current for the SP-SRM requirements.

From the analysis of the existing converter topologies, it can be concluded that any new converter concepts must fulfil the following criteria:

1. The new concept must be able to provide unipolar current in pulses based on rotor position. The converter must also be able to provide pulses of reverse current for defluxing.
2. The converter must be able to provide fast demagnetisation of the windings in order to reduce the flux linkage to zero before subsequent commutation.
3. For high speed operation, the converter must be able to handle advance angles.
4. The converter needs to be highly efficient under most load conditions.
5. The converter needs to be cost effective either by having a minimum number of components or by rearrangements of components

This chapter introduces a novel converter design which has satisfied all the criteria above while achieving lower cost and better performance at high speeds. The chapter is sub-divided into sections to facilitate the explanation. Section 5.2 is a description of the approaches taken to achieve the criteria above. This is followed by Section 5.3 which describes the design of the input and output stages of the converter. Section 5.4 gives the justification on how the proposed converter achieves all the

criteria described in Section 5.2. This is followed by Section 5.5 with a detailed analysis of the operation modes for the proposed converter. Next is Section 5.6 which presents the simulation results using a static and a variable inductance model. Section 5.7 follows giving the performance and limitations of the circuit before Section 5.8 compares the circuit to previous literature. Section 5.9 concludes the chapter.

5.2. Approaches to achieve a new converter concept

Approaches that need to be taken to achieve the five criteria listed in section 5.1 can be described in five corresponding processes:

1. All state-of-the-art converter topologies for SP-SRM have been able to produce unipolar current in pulses based on the feedback from rotor position sensors. It is only appropriate to extend any available technologies to the new converter concept so that unipolar current can be provided to the machine.
2. The converter needs to run at higher DC link voltage since a higher voltage will achieve high $\frac{di}{dt}$. High $\frac{di}{dt}$ means a faster demagnetisation of the phase windings.
3. In high speed operations, commutation must preceed the aligned position by several degrees. As the speed increases the angle must be advanced. Therefore, higher machine efficiency is achieved if the advance angle can be controlled.
4. To achieve high efficiency, the dwell angles of the machine need to be carefully calculated. Most importantly, T_{off} need to be carefully selected so that it does not happen beyond the full alignment rotor position and negative torque is then produced. If this happens, the machine efficiency is compromised.
5. Most work on SP-SRM converter focus on the standard diode bridge rectifier, where diodes need to withstand at least 1.5 the peak supply voltage. Adjusting the VA ratio of the diodes would also lead to cost reduction. Another strategy would be to focus on the dc link capacitor as the main cost contributor in a standard diode bridge rectifier.

Work on a new converter concept has taken into account all five approaches above. A new converter concept is proposed and described in the next section.

5.3. Design of the proposed converter

Figure 5-1 shows the proposed converter. In order to describe the novel converter, the description is divided into two sections; input side and output side. The input side of the converter involves the AC mains feeding two capacitors as temporary storage elements. The output side describes the inverter stage.

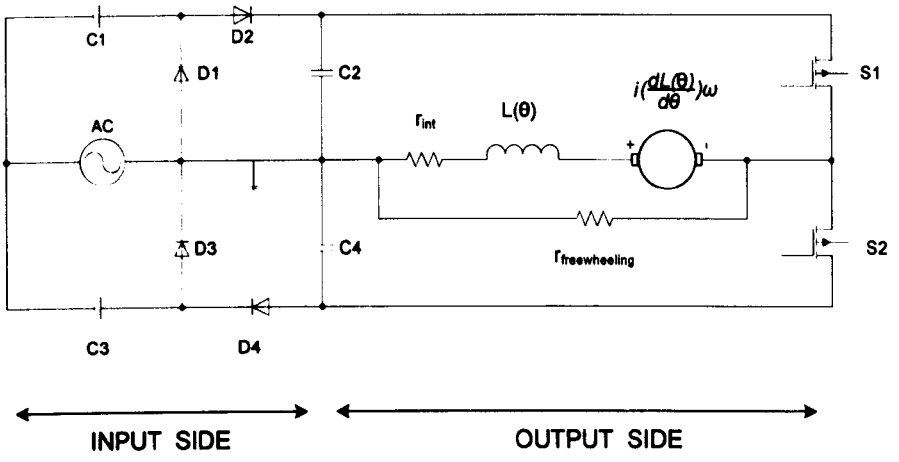


Figure 5-1- Novel converter showing the input and output sides

5.3.1. Input side

The input side of the converter is based on one of the most cost effective and popular ways to generate high voltages at relatively low currents. The circuit configuration is called the diode/capacitor voltage multiplier circuit. The basic circuit was first introduced by Cockroft and Walton in 1932 [29], and because of this, the circuit is also called Cockroft-Walton voltage multiplier circuit. Figure 5-2 shows a typical arrangement of the multiplier circuit showing the AC input and the high voltage DC output.

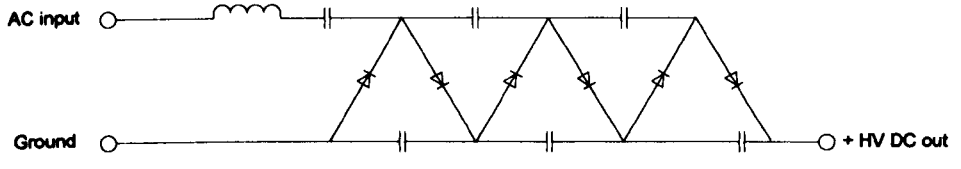


Figure 5-2- Typical arrangement of the Cockroft-Walton multiplier circuit

In high voltage, this circuit arrangement eliminates the need for the heavy core and bulky insulation required if transformers were used. The voltage multiplier circuit is capable to step up relatively low voltages to extremely high values, while at

the same time being much lighter and cheaper than conventional methods [101]. One of the biggest advantages of this circuit is that the voltage across each stage of the cascade is equal to twice the peak input voltage. If for example, a design requires voltage of four times the peak input voltage, a two stage voltage multiplier cascade needs to be applied. Therefore, the circuit design process can be completed in a shorter period of time.

Voltage multiplier circuits have been popular for applications in laser systems, power supplies, particle accelerators, x-ray systems and many other applications that utilise high voltage DC [102-104].

The circuit consists primarily of diodes and capacitors. To best describe the circuit, Figure 5-3 is used showing two typical voltage multiplier circuits to obtain voltage doubling. It is assumed that there are no losses in the circuit. The operating principles of all multiplier circuits are essentially the same. In the circuit, capacitors are connected in series, and are charged and discharged on alternate half-cycles of the supply voltage. The diodes and additional capacitors are arranged to effectively obtain equal voltage increments across the series capacitors.

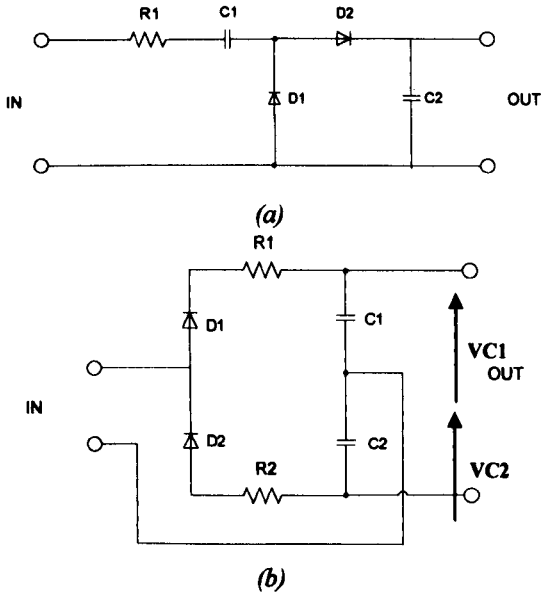


Figure 5-3- Two basic multiplier circuits (a) half wave voltage doubler; (b) full wave voltage doubler

As a specific example, consider the single stage circuit in Figure 5-3 (a). At $t=0$, all capacitors are uncharged. During the negative half cycle of V_S, the voltage across capacitor C_1 becomes,

$$V_{C1} = V_S \qquad (5\text{-}1)$$

where V_S is the peak voltage of the supply voltage.

C1 is now treated as a voltage source. Therefore, during the positive half cycle, V_{C2} becomes,

$$V_{C2} = V_S + V_{C1} \qquad (5\text{-}2)$$

Using equation 5-1, the output voltage is,

$$V_{C2} = 2V_S \qquad (5\text{-}3)$$

and for subsequent stages of the circuit,

$$V_{Cn} = 2nV_S \qquad (5\text{-}4)$$

where n is the number of stages. The output of the multiplier circuit is taken as the sum of the voltages in the series capacitors. There is a short delay of a few cycles of the supply before the capacitors are fully charged. As mentioned in [105], this delay between the input and the output is the main disadvantage of this circuit.

In Figure 5-3 (b) each capacitor is charged to the peak voltage separately during the different half cycle. The output voltage is the sum of both capacitors. This circuit is called full wave voltage doubler because both half-cycles of the incoming ac wave are used.

The principle of a voltage doubler circuit is used for the input side of the proposed SP-SRM converter topology, shown in Figure 5-4. In this circuit, there are two single stage voltage doubler circuits connected back to back. Again, assuming no losses, the voltage output would be $+2V_S$ and $-2V_S$ at both the output stages respectively.

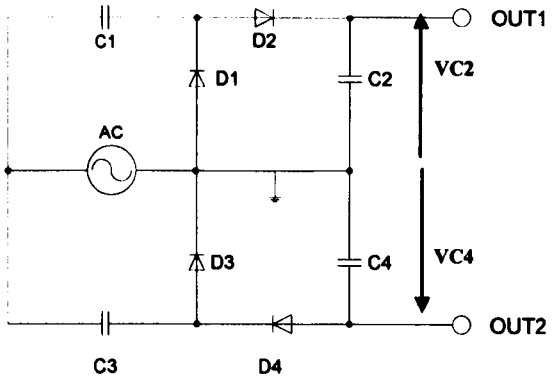


Figure 5-4- Input side of the novel converter topology

For the top voltage doubler, C1 is charged via D1 during the negative half cycle of the supply voltage. During the next half cycle, the C2 will be charged by the peak supply voltage and V_{C1} via D2. The same happens in the bottom voltage doubler. However, in this case, C3 is charged during the positive half cycle of the supply, and C4 is charged at the negative half cycle. At the end of each cycle of the supply, there would be twice the supply voltage across capacitors C2 and C4 respectively.

The Cockroft and Walton circuit inherently has a long charging time. The same applies to the circuit shown in Figure 5-4. The four capacitors must be allowed to charge fully before the inverter starts operating. This is done by monitoring the capacitor voltage. Once both V_{C2} and V_{C4} reached the desired value, a feedback will be sent to a controller to commence switching.

Applying the rectifier shown in Figure 5-4 to SP-SRM has not been reported and is seen as the first novelty of the proposed SP-SRM. A voltage multiplier circuit similar to the one shown in Figure 5-3(b) has just been applied to a two phase SRM [28]. The concept proposed in [103] is different to the one proposed here. The main difference is that the converter in [103] is only suitable for use in a double phase machines. Also, the voltage available to each phase of the machine is only V_S, and the regeneration of energy back to the supply is done via diodes similar to the ones in the conventional Direct Regeneration converter described in Chapter 3.

5.3.2. Output side

The concept of the inverter stage (shown in Figure 5-5) is based on the 'half-bridge Voltage Source Inverter' configuration [106]. The output side of the converter is made up of series connected output capacitors, a freewheeling resistor and the power switches connected to the load machine.

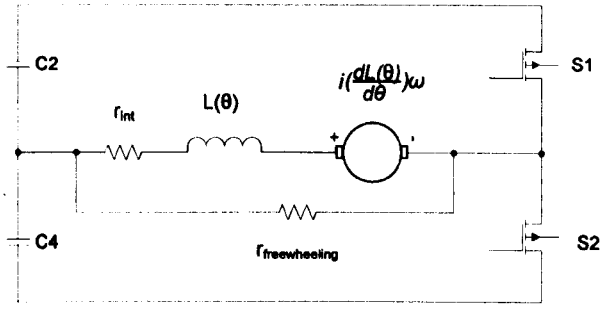


Figure 5-5- Output side of the novel converter topology

The power switches are turned on and off to achieve magnetisation and demagnetisation of the windings based on the rotor position information. The freewheeling resistor is used to provide the zero current loop.

In the classical 'half-bridge Voltage Source Inverter' circuits, the DC-link voltage is halved at a neutral point or mid-point, so that each capacitor maintains an equal constant voltage. This concept has been applied in the Capacitor Boost circuit described in Chapter 3. With the proposed converter concept, the voltage across the capacitors has two different polarities, which is seen as a second novelty for SP-SRM drives.

The operation of the circuit will be described in the next sections.

5.4. Justification for achievement of converter improvements

The new converter concept fulfils all five criteria and approaches as listed in Section 5.1 and 5.2.

The converter is able to provide pulses of unipolar current to the machine based on the rotor position signal. The rotor position signal comes from a position

sensor that is mounted on the shaft of the SP-SRM. The current in pulses is drawn from the storage capacitors alternatingly, based on which switching device is on.

As a voltage doubler concept is used in the input stage, double the peak supply voltage is available to be injected across the windings. During turn-off, this high voltage is used to force the defluxing at a faster rate. Therefore the current goes to zero very quickly before the next commutation.

As for the capability to achieve high speed operation, the faster turn-on and turn-off will allow for better advance angles to be applied to the machine. Faster turn-on and turn-off is achieved as the defluxing current goes to zero at a faster rate. Therefore, the machine has the capability to be working at higher speeds.

To increase the efficiency of the machine, the initial selection of the firing angles need to be carefully adjusted so that the input power (that is the input current to the storage capacitors) during steady state is minimised. To achieve this, the power flow is calculated based on the voltage and current of the storage capacitors. Then the turn-on and turn-off angles are adjusted so that the desired speed is achieved. The process of power flow calculation and dwell angle adjustments are repeated until the minimum dwell angle for the desired speed is achieved. Minimum dwell angle is necessary to produce maximum torque [107], and therefore maximum efficiency of the machine. In the proposed converter, this high efficiency machine is obtained by online monitoring and control of the turn-on and turn-off angles, as well as the power flow.

The proposed converter has two switching devices and two diodes per phase, resembling the conventional Direct Regeneration converter. However, the standard diode bridge rectifier has been replaced by an arrangement of capacitors and diodes. In previous SP-SRM converter technologies, the diodes in the bridge rectifier are rated at 1.5 times the peak supply voltage. However, in the proposed converter, the VA ratio of the diodes is reduced since the diodes are used only to provide charging and discharging of the storage capacitors.

From the simulation work that has been done, it can be seen that charging and discharging of the capacitors does not happen from zero as the capacitors have been charged up before the operation of the converter (refer to the proposed converter modes of operation). When switching commences, some of the capacitor voltage is used for providing energy to the windings. During the period of deenergising, this energy is returned to the source. At the same time this happens, the capacitor is also being constantly charged up via the supply. Looking at the proposed converter configuration, it can be seen that the diodes are in forward biased only during the period when the storage capacitors are being supplied by the voltage source. Therefore, the VA requirements of the capacitors and diodes are reduced. Hence, through topological rearrangements of the inverter-rectifier, cost reduction can be achieved.

Figure 5-6 shows both the novel converter and the Direct Regeneration converter including the input sides and enables direct comparison to be made.

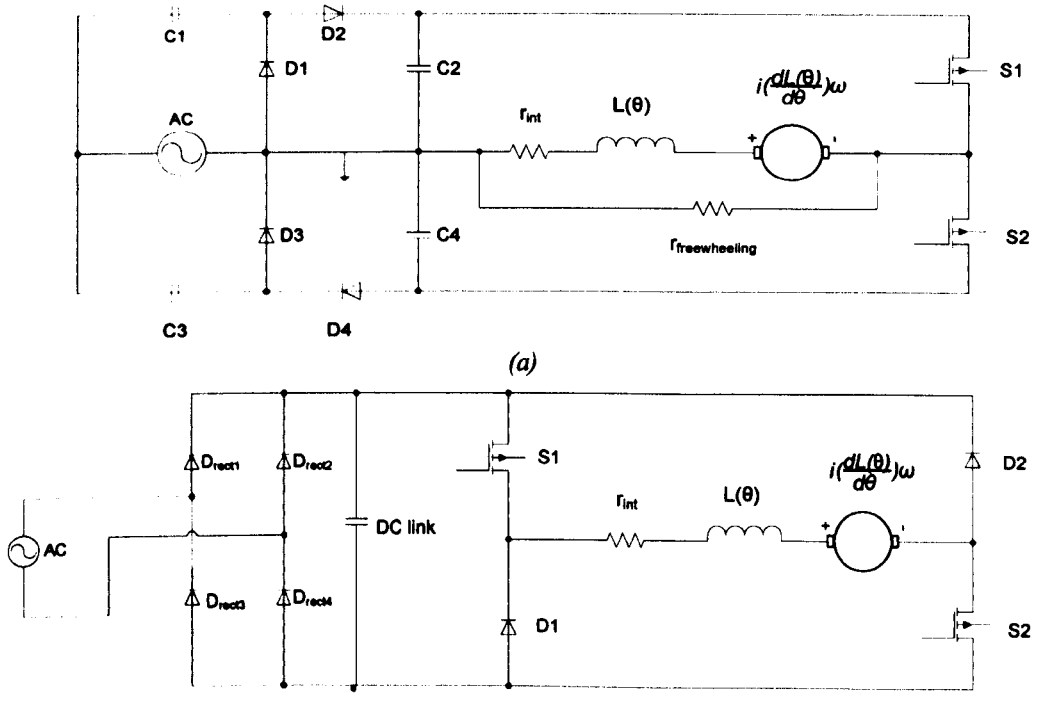


Figure 5-6- Comparison of both converters; (a) proposed novel converter (b) classic Direct Regeneration converter

5.5. Operation modes

The operation of the converter can be described in three operation modes. However, a pre-requisite for these modes would be the charging of the capacitors. All components are assumed to be ideal.

Pre-requisite: Charging of the capacitors

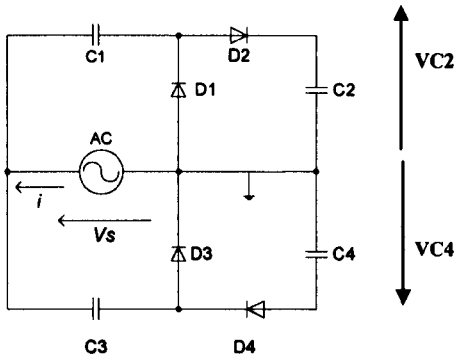


Figure 5-7- Mode 1 of the converter

The charging of the capacitors occurs at zero load current. The equivalent circuit for charging of the capacitors is shown in Figure 5-7. The two capacitors C2 and C4 are charged up to their maximum value. (The capacitors C2 and C4 are called 'storage capacitors' from this point forward to ease the circuit explanation.) It may take a few cycles of the supply before both capacitors are fully charged. Based on equation 5-4, the voltage across each capacitor is,

$$V_{C2} = 2V_S \qquad (5\text{-}5)$$

$$V_{C4} = -2V_S \qquad (5\text{-}6)$$

The charging time of the capacitors in this circuit is not as straightforward as in a classic resistor-capacitor (RC) circuit. The charging time of a capacitor for such circuit is defined as the time required for the charging current of a capacitor to fall to $\frac{1}{e}$ of its initial value. This time is called the time constant of the circuit, denoted by τ.

For example, in a classic capacitor circuit as shown in Figure 5-8, the one time constant τ for the circuit (after the switch S is closed) can be expressed as,

$$\tau = RC \qquad (5\text{-}7)$$

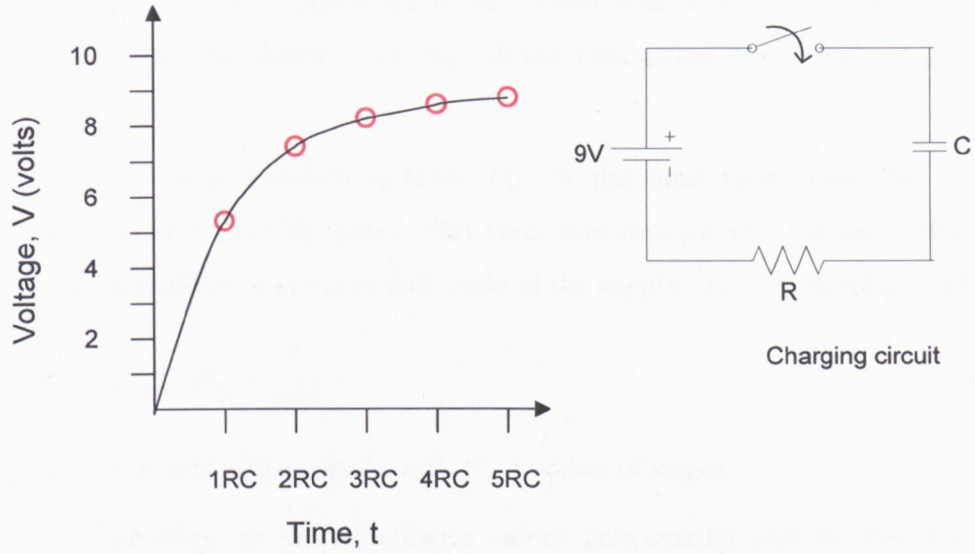


Figure 5-8 Simple capacitor charging circuit

The diagram in Figure 5-8 shows that it takes 5 RC's to charge the capacitor above 95% of its maximum voltage value.

For a Cockroft-Walton voltage doubler, the charging time of the capacitors is also influenced by R and C. R (R_{source}) is the resistance of the supply and is mainly made up of the resistance of the wire connection, and the internal resistance of the capacitors and diodes. R is therefore small. C is the effective capacitance of the multiplier circuit (C).

In addition to R and C, the time constant is also a factor of the supply frequency (f_{source}) and therefore, the mathematical expression in equation 5-7 is not applicable. The effect of the number of stages in the voltage doubler circuit to the capacitor charging time is negligible since in the proposed converter the number of stages is always constant.

For ease of explanation, the time constant, $\tau_{multiplier}$ for this circuit can be expressed as:

$$\tau_{multiplier} = \sum \frac{R_{source} C}{f(D_{di}, f_{source})} \qquad (5\text{-}8)$$

where R_{source} = input impedance of the power source, C = capacitance value, and $f(D_{di}f_{source})$ is the function of D_{di} (diode conduction time) and f_{source} (supply frequency)

The diode conduction time, D_{di}, is the total time when the diodes are conducting over one full cycle. This takes into account whether the diodes conduct during the positive or negative half cycle of the supply. D_{di} can be simplified as,

$$D_{di} = \frac{T}{2N} \qquad (5\text{-}9)$$

where T = period of the supply, and N = number of stages.

Therefore, as the capacitance values gets smaller and the frequency of the supply gets bigger, the charging times of the capacitors becomes smaller.

This pre-requisite step runs independently from the next described modes.

Mode 1: Phase magnetisation

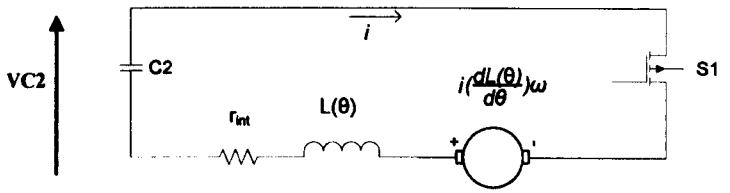


Figure 5-9- Mode 1 phase magnetisation

Figure 5-9 shows the equivalent circuit for Mode 1. When V_{C2} is fully charged, S1 will turn-on causing C2 to discharge, and at the same time magnetising the phase windings. S2 is kept off during this time. The current through the load windings increases from zero to the maximum value, I_{max}. However, the maximum load current is limited by the maximum threshold of the hysteresis band, I_{upper}.

The current through the load windings can be derived as,

$$i(t) = I_{max}\left(1 - e^{\frac{-t}{\tau_1}}\right) \qquad (5\text{-}10)$$

where

$$I_{max} = \frac{V_{C2}}{R} \qquad (5\text{-}11)$$

$$R = r_{int} + \frac{dL(\theta)}{d\theta}\omega \qquad \text{with } r_{freewheel} >> r_{int} \qquad (5\text{-}12)$$

$$\tau_1 = \frac{L(\theta)}{R} \qquad (5\text{-}13)$$

Mode 2: Freewheeling

The freewheeling period is the shortest period of all modes. During this mode of operation, (the equivalent circuit is shown in Figure 5-10) the energy freewheels through the freewheeling resistor. There is no flow of energy back into the supply. The rate of decay, τ_2 depends mainly on the freewheeling resistor value, $r_{freewheeling}$.

This mode is applied only during the time when both switches S1 and S2 are turned off. The mode is applied in order to turn off S1 fully before turning on S2 and vice versa. The current at the start of the Freewheeling mode is equal to the current defined by the maximum hysteresis threshold, I_{upper}.

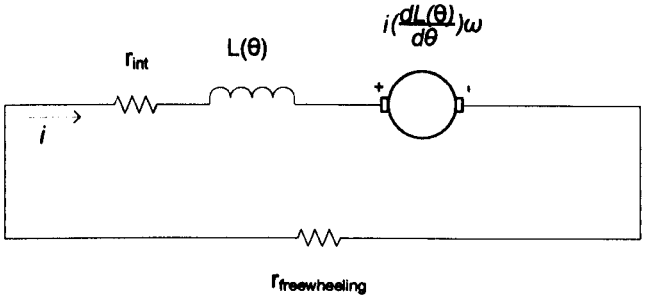


Figure 5-10- Mode 2 Freewheeling

Current flow:

$$i(t) = I_{upper} e^{\frac{-t}{\tau 2}} \qquad (5\text{-}14)$$

where

$$\tau_2 = \frac{L(\theta)}{r_{freewheeling} + r_{int} + \frac{dL(\theta)}{d\theta}\omega} \qquad (5\text{-}15)$$

It is desirable for the freewheeling resistor to have a large value so that the freewheeling time can occur longer than the dead time of the switches. However, there has to be some compromises in choosing the resistance of the freewheeling resistor in order to limit losses.

Mode 3: Demagnetisation of the windings

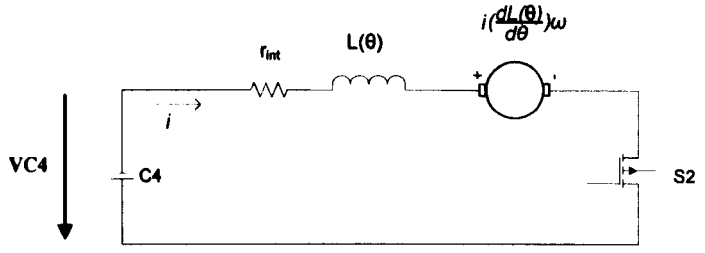


Figure 5-11- Mode 3 Demagnetisation of the windings

Figure 5-11 is similar to Figure 5-9. The windings are demagnetised when S2 is on and S1 is off. The energy is returned to C4. The demagnetisation current flows in the same direction and is given by:

$$i(t) = I_{upper} e^{-\frac{t}{\tau_3}} \qquad (5\text{-}16)$$

where

$$\tau_3 = \frac{L(\theta)}{r_{int} + \frac{dL(\theta)}{d\theta}\omega} \qquad (5\text{-}17)$$

The demagnetisation current decays down to the current value defined by the minimum hysteresis threshold, I_{lower}. After Mode 3, all three modes repeat.

5.6. Simulation work

The simulation work of the novel converter follows the same simulation setup as described in Chapter 4. The software PSpice is used to verify the circuit design. For the purpose of simulation, it is assumed that all components are ideal except where specified.

Similar to the simulation settings in Chapter 4, the rotor position signal is implemented by a clock signal of a frequency of 500Hz (period of 2ms) with 50% duty cycle. This is taken as the worst case for the switching and operating at this duty cycle will mean high component stress.

A hysteresis controller is used for controlling the converter. When the controller receives information that the two capacitors have been fully charged, the inverter starts its operation. The current is allowed to increase and decrease based on the hysteresis upper and lower bands.

The analysis of the converter is divided into simulation with static inductance and simulation with variable inductance.

5.6.1. Simulation with static inductance

For the simulation with static inductance, the same model of the SP-SRM as presented in Chapter 3 is used (Figure 5-12). The simulation is performed with the minimum inductance value of the SRM in order to simulate the worst case scenario, where smaller inductance will generate larger current and voltage stresses across the components.

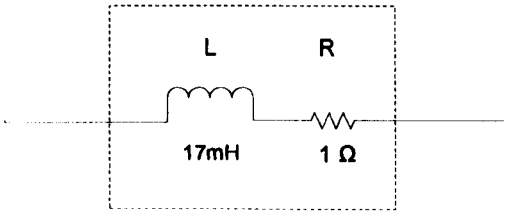


Figure 5-12- SP-SRM model used in the simulation

The capacitor size is calculated based on the design guidelines [108] where the capacitor size should be directly proportional to the frequency of the input signal. Typically, for a 230V rms, 50Hz supply, the capacitors used are in the range of 1.0μF to 200μF. For the simulation purposes, initially, all capacitors are taken as 200μF. This value is actually much bigger than would be sensible for a production drive. However, it is chosen just for demonstration purposes only.

Figure 5-13 shows the voltages across the capacitors C1 and C3 while Figure 5-14 shows the voltages across capacitors C2 and C4.

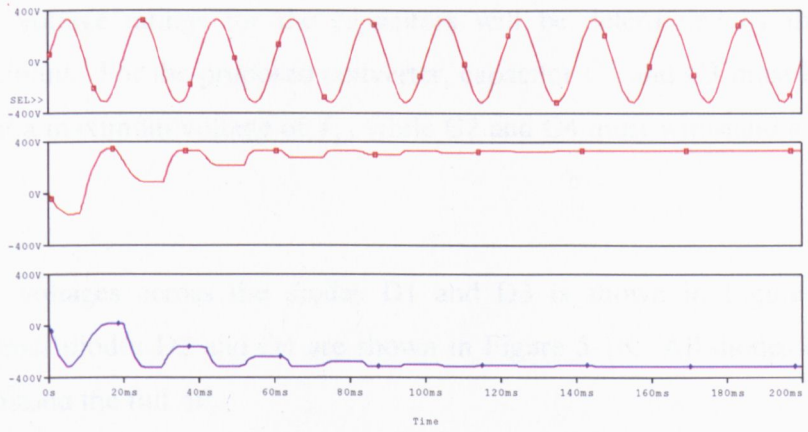


Figure 5-13- Voltages of the mains supply (top), across capacitor C1 (middle) and C3 (bottom)

As seen in Figure 5-13, capacitor C1 is charged during the negative cycle and C3 is charged during the positive cycle of the supply. The voltages in C1 and C3 reach the maximum values of $\hat{V}_S$ after approximately seven cycles of the mains at around 130ms.

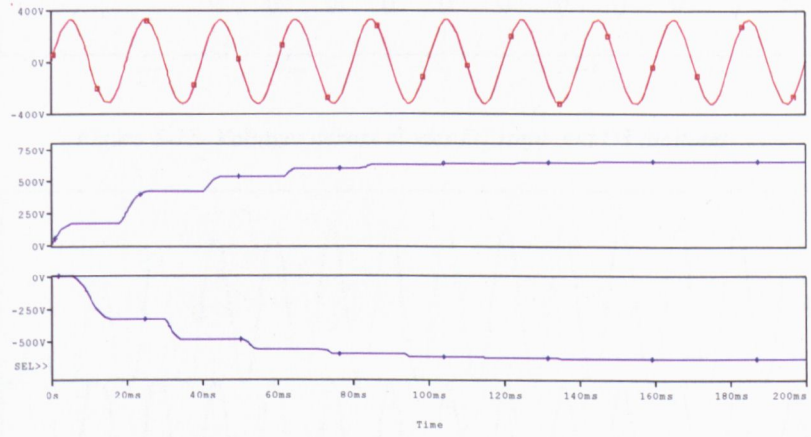


Figure 5-14- Voltages across capacitors C2 (middle) and C4 (bottom) compared to the mains ac voltage (top)

Figure 5-14 shows that the capacitors are fully charged at $2\hat{V}_S$ after seven cycles of the main at around 130ms. The maximum voltage of approximately 700V in each capacitor is calculated as,

$$V_{C2} = V_{C4} = 2\hat{V}_S \qquad (5\text{-}18)$$

where

$$\hat{V}_S = \sqrt{2}V_{rms} = 325V \qquad (5\text{-}19)$$

The voltage ratings for the capacitors will be determined by the type of multiplier circuit. For the proposed converter, capacitor C1 and C3 must be capable to withstand a maximum voltage of $\hat{V}_S$, while C2 and C4 must withstand a voltage of $2\hat{V}_S$.

The voltages across the diodes D1 and D3 is shown in Figure 5-15 and voltages across diodes D2 and D4 are shown in Figure 5-16. All diodes need to be able to withstand the full $2\hat{V}_S$.

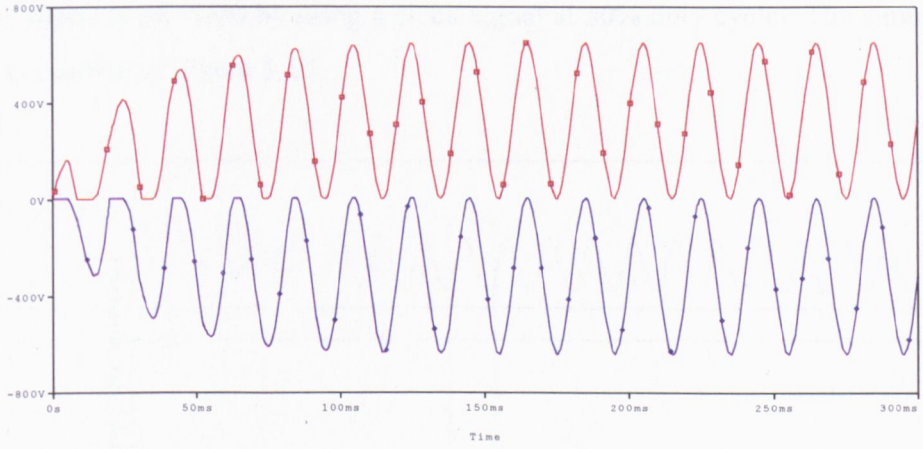


Figure 5-15- Voltages across diodes D1 (top) and D3 (bottom)

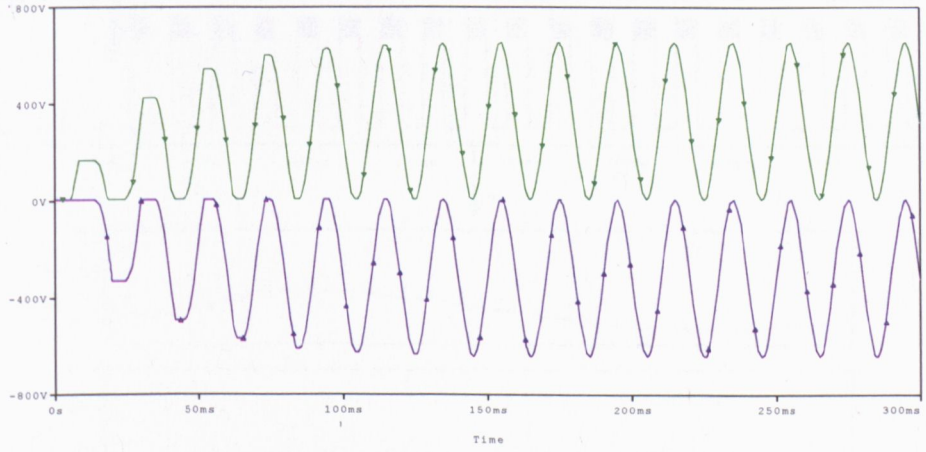


Figure 5-16- Voltages across diodes D2 (top) and D4 (bottom)

It is established from the simulation above that the input stage is capable of producing the multiplied supply voltage. The input stage is then connected to the output stage as described in Section 5.3. Initially, these parameters are used for the simulation:

$V_{supply} = 230Vac$ $R_{freewheel} = 110\Omega$

$C_1 = C_2 = C_3 = C_4 = 200\mu F$ $t_{delay} = 1\mu s$

Clock period = 20ms (for 1500 rpm SP-SRM speed)

At the start the switches are both off. Switching will commence when the capacitors are fully charged (for the purpose of the simulation, the capacitor fully charged value is defined as 600V). Based on the calculation in Chapter 4, the rotor position signal is provided by using a clock signal at 50% duty cycle. The simulation results are shown in Figure 5-17.

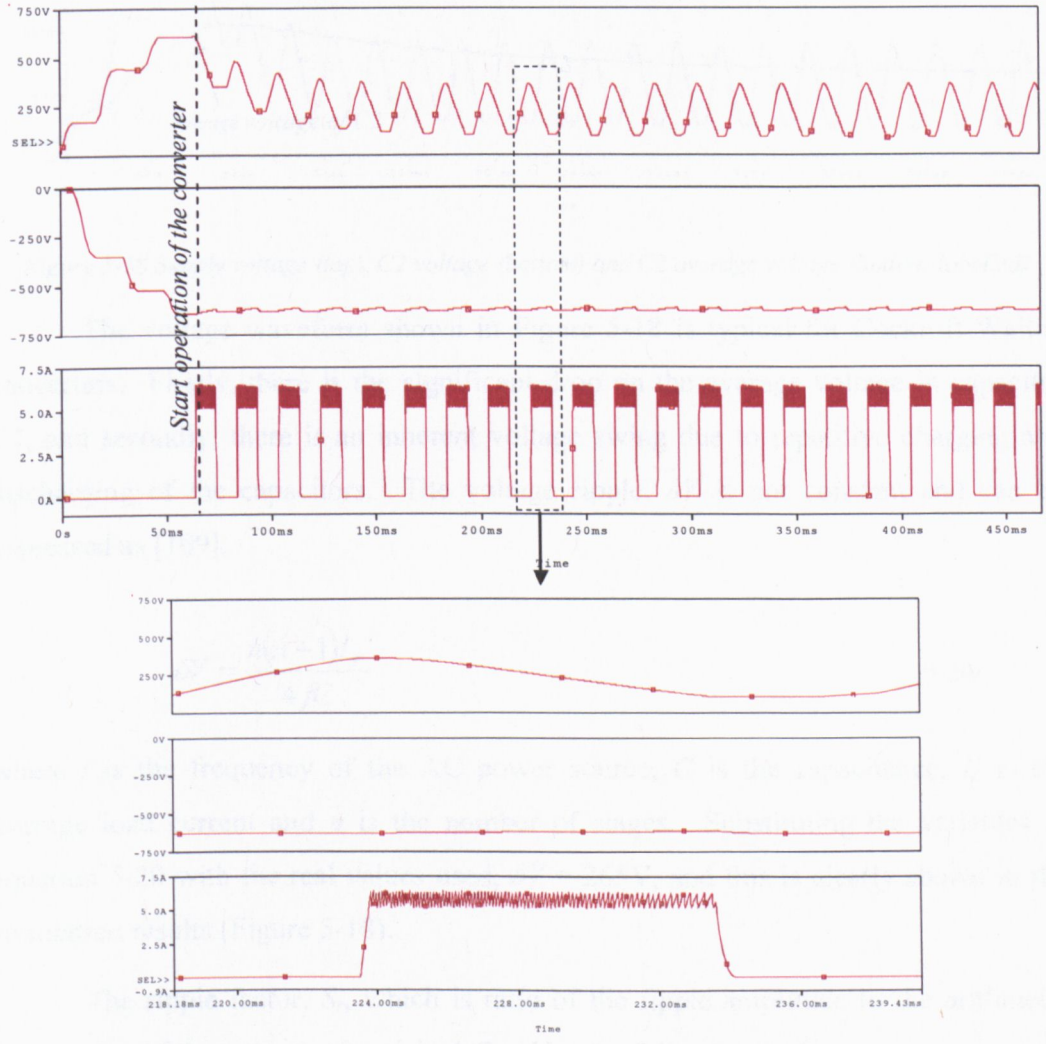


Figure 5-17- Voltage of capacitors C2 (top) and C4 (middle), and load current (bottom) – both capacitors are 200μF

From the simulation, it is seen that switching commences at after 60ms, when the capacitor voltages have reached $2\hat{V}_S$ value. When the switching commences, the voltage in C2 dips to an average steady state value of 263V (40% of $2\hat{V}_S$) after 160ms.

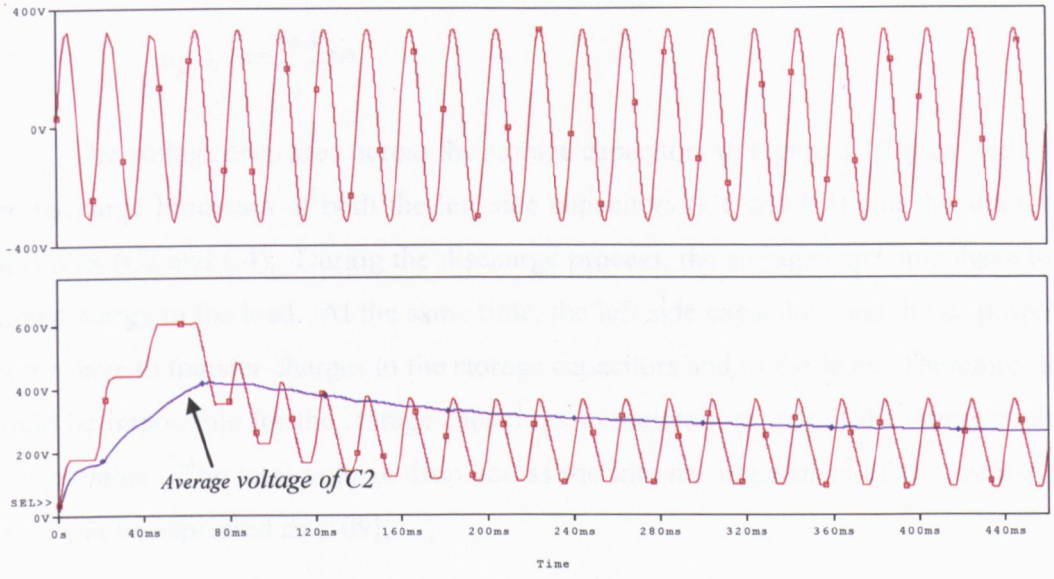


Figure 5-18 Supply voltage (top), C2 voltage (bottom) and C2 average voltage (bottom-labelled)

The voltage waveform shown in Figure 5-18 is typical for Cockroft-Walton converters. Firstly, there is the significant drop on the average voltage in capacitor C2, and secondly, there is an inherent voltage swing due to repetitive charging and discharging of the capacitors. The voltage ripple, δV is not constant and can be expressed as [109],

$$\delta V = \frac{n(n+1)I_P}{4fC} \qquad (5\text{-}20)$$

where f is the frequency of the AC power source, C is the capacitance, I_p is the average load current and n is the number of stages. Substituting the variables in equation 5-20 with the real values used, δV = 265V, and this is clearly shown in the simulation results (Figure 5-18).

The ripple factor, S_r, which is ratio of the ripple amplitude to the arithmetic mean value of the output voltage, is defined by the following equation,

$$S_r = \frac{\delta V}{V_p} = \frac{n(n+1)I_P}{4fCV_P} \qquad (5\text{-}21)$$

where V_p is the average open circuit output dc voltage (V_{max} is the maximum open circuit output dc voltage and V_{min} is the minimum open circuit output dc voltage) and V_p can be expressed as,

$$V_P = \frac{V_{max} + V_{min}}{2} \qquad (5\text{-}22)$$

The voltage drop seen across the storage capacitors in Figure 5-17 is caused by the discharge processes of both the left side capacitors (C1 and C3) and the storage capacitors (C2 and C4). During the discharge process, the storage capacitors have to supply energy to the load. At the same time, the left side capacitors and the ac power source have to transfer charges to the storage capacitors and to the load. Therefore, it would be impossible for the storage capacitors to maintain supply at the open circuit voltage value. The total voltage drop across the internal impedance of the rectifier, ΔV_{min} can be expressed as [109],

$$\Delta V_{min} = \frac{I_P}{12fC}\left(8n^3 + 3n^2 + n\right) \qquad (5\text{-}23)$$

The sum of the ripple voltage (equation 5-20) and the voltage drop across the internal impedance (equation 5-23) equals to the average voltage drop of the capacitor outputs, ΔV_P. It can be expressed as,

$$\Delta V_P = \frac{I_P}{6fC}\left(4n^3 + 3n^2 + 2n\right) \qquad (5\text{-}24)$$

Therefore, an expression for the average output voltage of the rectifier, V_P, is the difference between the open circuit output voltage (equation 5-4) and the total average voltage drop (equation 5-24),

$$V_P = 2nV_S - \frac{I_P}{6fC}\left(4n^3 + 3n^2 + 2n\right) \qquad (5\text{-}25)$$

Substituting equation 5-25 with the real values used, the average output voltage of the rectifier is 260V. Therefore, this validates the simulation output.

The voltage curve of capacitor C2 in Figure 5-17 shows a regular pattern in the voltage ripple. Figure 5-19 shows the capacitor current of C2, the load current, the supply voltage and voltages across capacitors C1 and C2.

A section of the curves in Figure 5-19 is zoomed and displayed in Figure 5-20. Figure 5-20 shows that both capacitors C1 and C2 are charged during the different half cycle of the supply. During commutation, voltage in C2 is used to supply current to the load, and this depletion in voltage can only be replaced in the next positive half cycle.

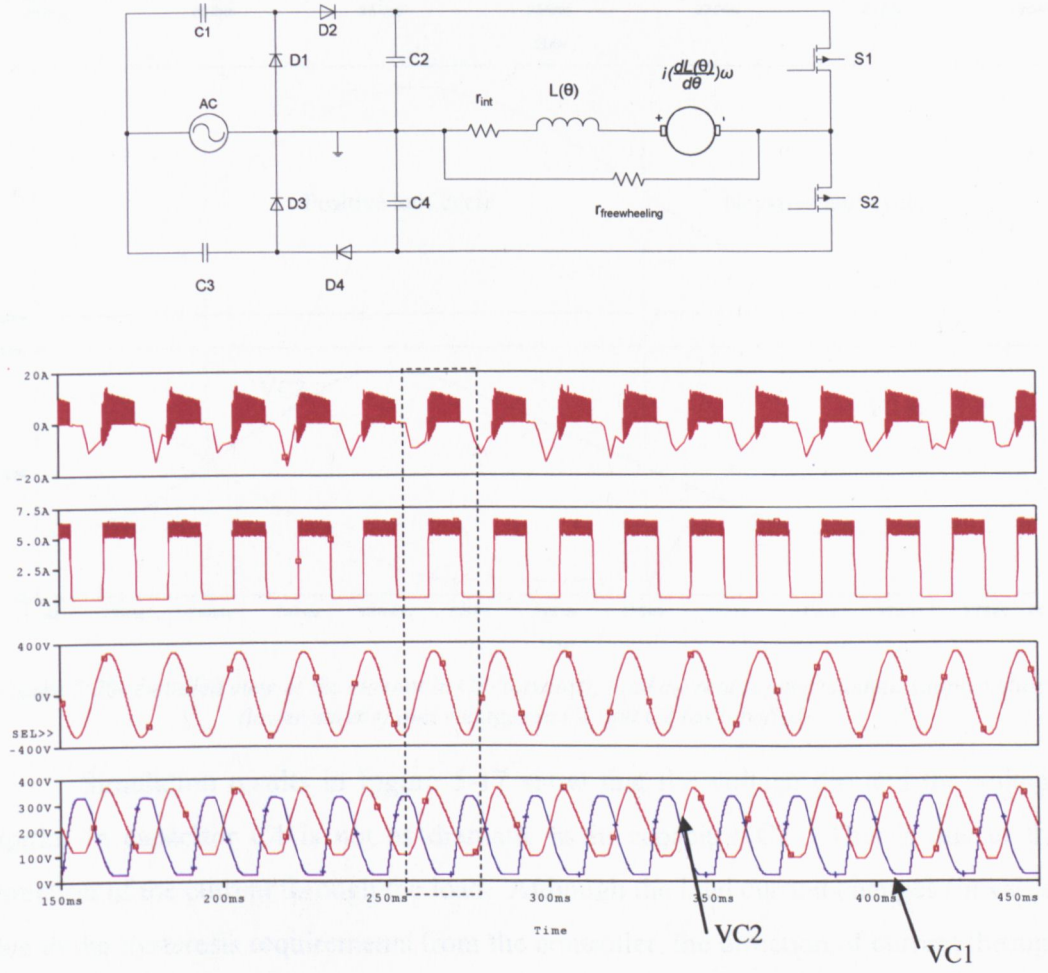


Figure 5-19- Simulation results showing capacitor C2 current (topmost), load current (upper middle), source voltage (lower middle) and voltages across the capacitor C1 and C2 (bottom labelled)

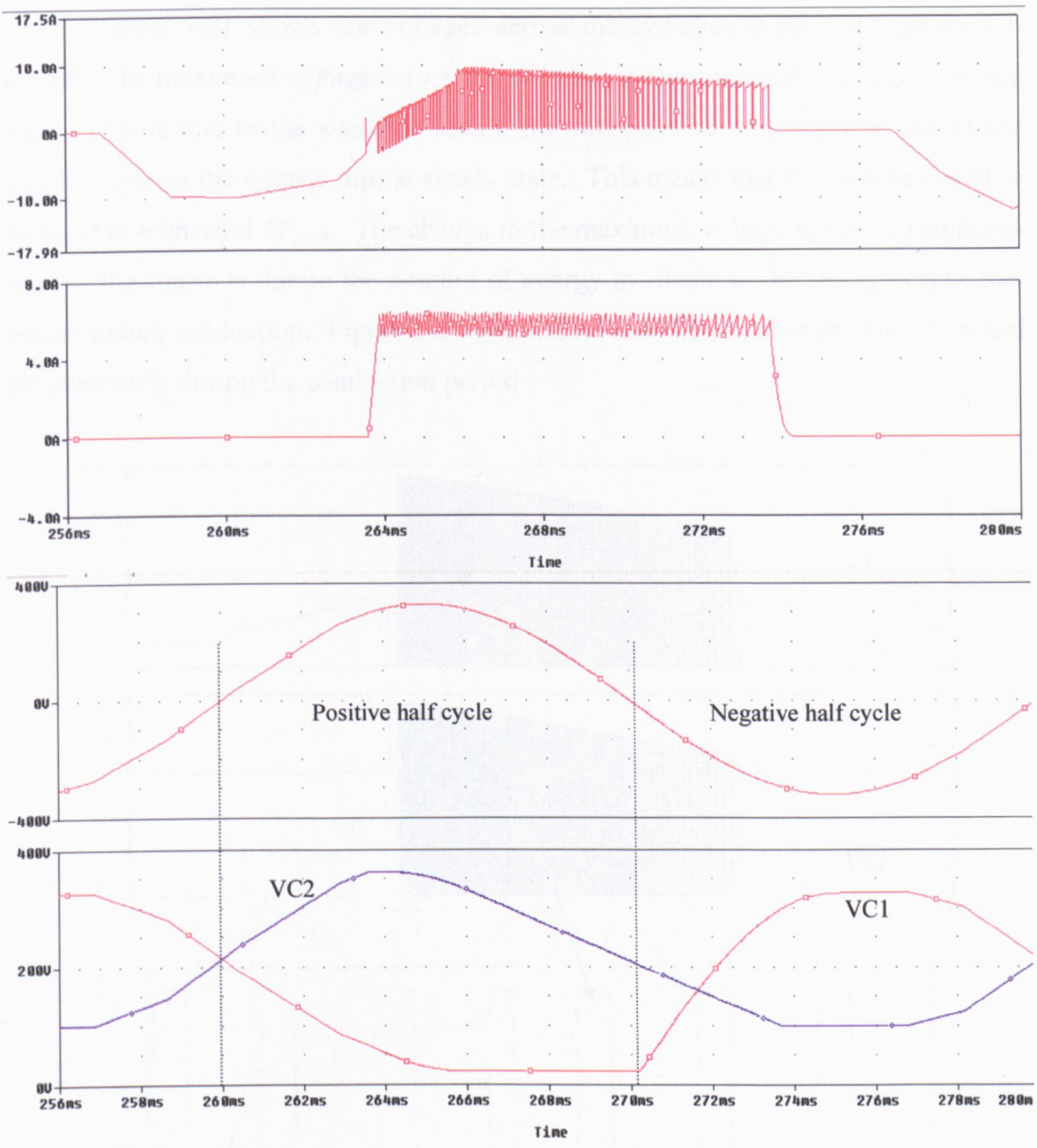


Figure 5-20- Detailed view of the current in C2 (topmost), load current (upper middle), supply voltage (lower middle) and voltages in C1 and C2 (as labelled)

Simulation results in Figure 5-17 show that the voltage dip and the voltage ripples in capacitor C4 is not as dramatic as in capacitor C2. This is due to the direction of the current through the load. Although the load current changes (in value) due to the hysteresis requirements from the controller, the direction of current through the load is maintained. Commutation of the switches begins with T1 when the inductive load is de-energised. During the time when T1 turns-off, and T2 turns-on, the load is already energised. Capacitor C4 does not have to supply as much energy as C2 to the load and all charges are maintained. This is seen in Figure 5-17 as a relatively stable output voltage of capacitor C4.

Figure 5-21 shows the voltages across the switches during one conduction period. The maximum voltage across the switches is approximately ($2V_{peak}$ – *voltage dip*). This is due to the switches seeing the full positive and negative rail of the supplies (minus the voltage dip) at steady state. This means that the switches need to be rated to withstand $2V_{peak}$. The change in the maximum voltage across the switches seen in the figure is due to the amount of energy available in the storage capacitors before switch conduction. Figure 5-21 also shows that the switches are turned on and off alternately during the conduction period.

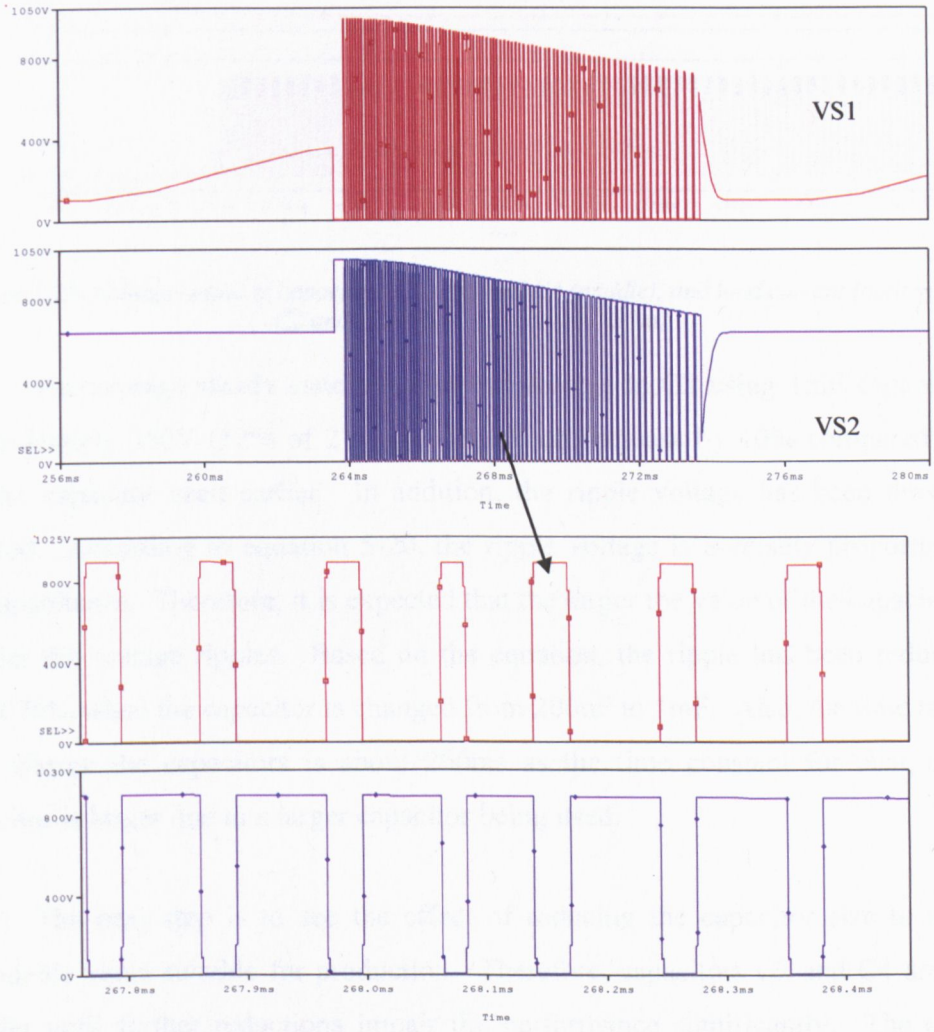


Figure 5-21- Voltages across switches S1 and S2 during one conduction period. A zoomed in version included to see the alternate switching

To see the effect of changing the capacitor values, capacitors C2 and C4 is made bigger so that the rate of voltage discharge is slower and the voltage dip is reduced. When a 1mF capacitor is used, the change in the results is shown in Figure

5-22. Capacitors C1 and C3 remains the same since changing them will only affect the charging and discharging times of the first set of the capacitor-diode configuration.

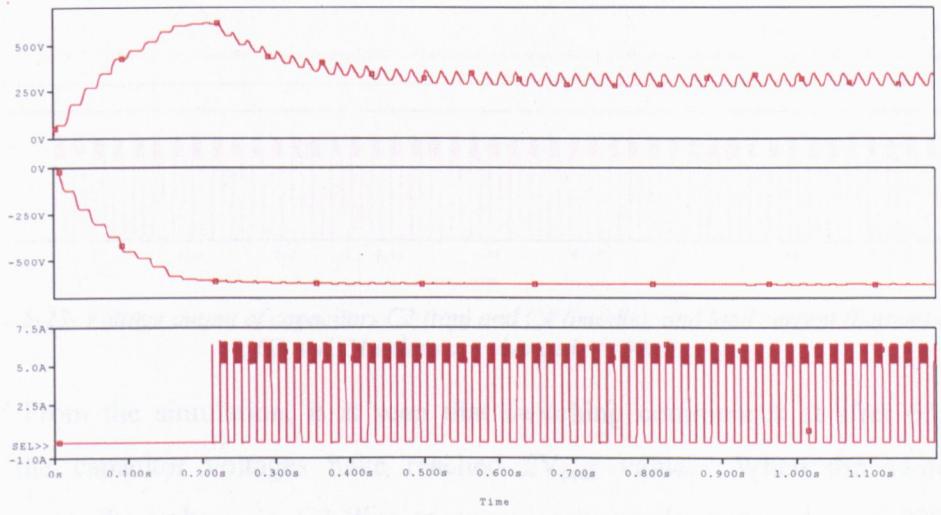


Figure 5-22- Voltage output of capacitors C2 (top) and C4 (middle), and load current (bottom) after C2 and C4 values are changed to 1mF

The average steady state value of the voltage in C2 using 1mF capacitors is approximately 350V (52% of $2V_{peak}$). This is an increase by 10% compared to the smaller capacitor used earlier. In addition, the ripple voltage has been drastically reduced. According to equation 5-20, the ripple voltage is inversely proportional to the capacitance. Therefore, it is expected that the larger the value of the capacitor, the smaller the voltage ripples. Based on the equation, the ripple has been reduced by about 70% when the capacitor is changed from 200uF to 1mF. Also, the time taken to fully charge the capacitors is about 200ms as the time constant for charging the capacitor is larger due to a larger capacitor being used.

The next step is to see the effect of reducing the capacitor size to a more reasonable value suitable for production. Therefore, capacitors C2 and C4 are made smaller until further reductions impair the performance significantly. The optimal capacitor size is 100uF. The change in result is shown in Figure 5-23.

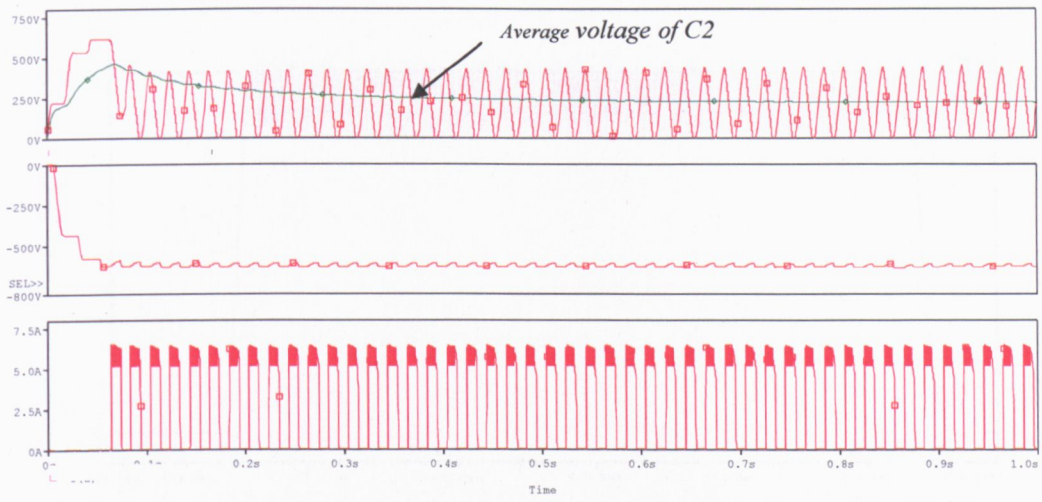


Figure 5-23- Voltage output of capacitors C2 (top) and C4 (middle), and load current (bottom) after C2 and C4 values are changed to 100uF

From the simulation, it is seen that switching commences at after 63.4ms, when the capacitor voltages have reached $2V_{peak}$ value. When the switching commences, the voltage in C2 dips to an average steady state value of 229.2 V (approximately 35% of $2V_{peak}$) after 440ms. The ripple voltage at this capacitance is large. However, the performance of the converter is still acceptable. Also, the time taken to fully charge the capacitors is 63.4ms.

A close inspection of the load current at steady state found that the current does not follow the hysteresis threshold band closely. This is shown in Figure 5-24. The explanation for this can be explained when looking into the converter modes of operation as explained in Section 5.5. In Figure 5-24, the average switching frequency is 13.2 kHz.

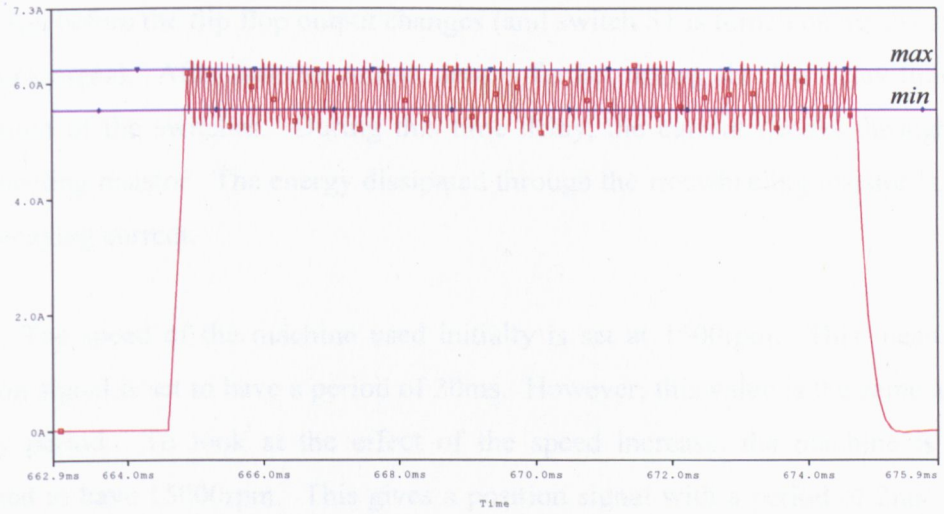


Figure 5-24- The load current taken after 662ms showing the variations against the hysteresis band (shown in dashed lines labelled max and min)

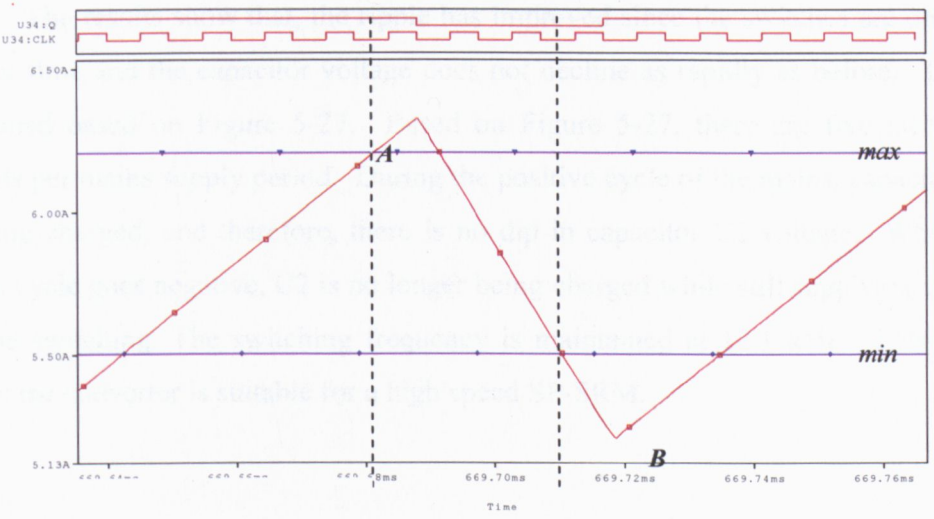


Figure 5-25- A section of the load current showing the overshoot from the upper and lower hysteresis thresholds (dashed lines show the switching thresholds)

Figure 5-25 shows a section of the load current which shows the overshoot of the current from the upper and lower thresholds (labelled max and min respectively). In the controller a JK flip flop is used to produce the switching signal, Q on every negative edge of the clock cycle. The signal Q is then subjected to a delay of 1µs to realise the dead time of the switches. At the time when the maximum threshold is reached (section A), the current still ramps up for about 3µs before the switch S1 turns off and the current goes down. This is because the flip flop is still waiting for a negative edge on the clock signal before the output can change. The switch S1 can turn off only when the output flip flop has changed. Looking at section B, it takes

about 8μs before the flip flop output changes (and switch S1 is turned on again) due to the clock signal. After 8μs the current decays further during the 1μs delay time for dead time of the switches. During this time delay, the current decays through the freewheeling resistor. The energy dissipated through the freewheeling resistor is seen as a decaying current.

The speed of the machine used initially is set at 1500rpm. This means the position signal is set to have a period of 20ms. However, this value is the same as the supply period. To look at the effect of the speed increase, the machine is now assumed to have 15000rpm. This gives a position signal with a period of 2ms. The simulation result is shown in Figure 5-26.

The results show that, the ripple has improved since the switches are on for a shorter time and the capacitor voltage does not decline as rapidly as before. This is explained based on Figure 5-27. Based on Figure 5-27, there are five switching periods per mains supply period. During the positive cycle of the mains, capacitor C2 is being charged, and therefore, there is no dip in capacitor C2 voltage. When the mains cycle goes negative, C2 is no longer being charged while still supplying energy for the switching. The switching frequency is maintained at 12.1 kHz. This result shows the converter is suitable for a high speed SP-SRM.

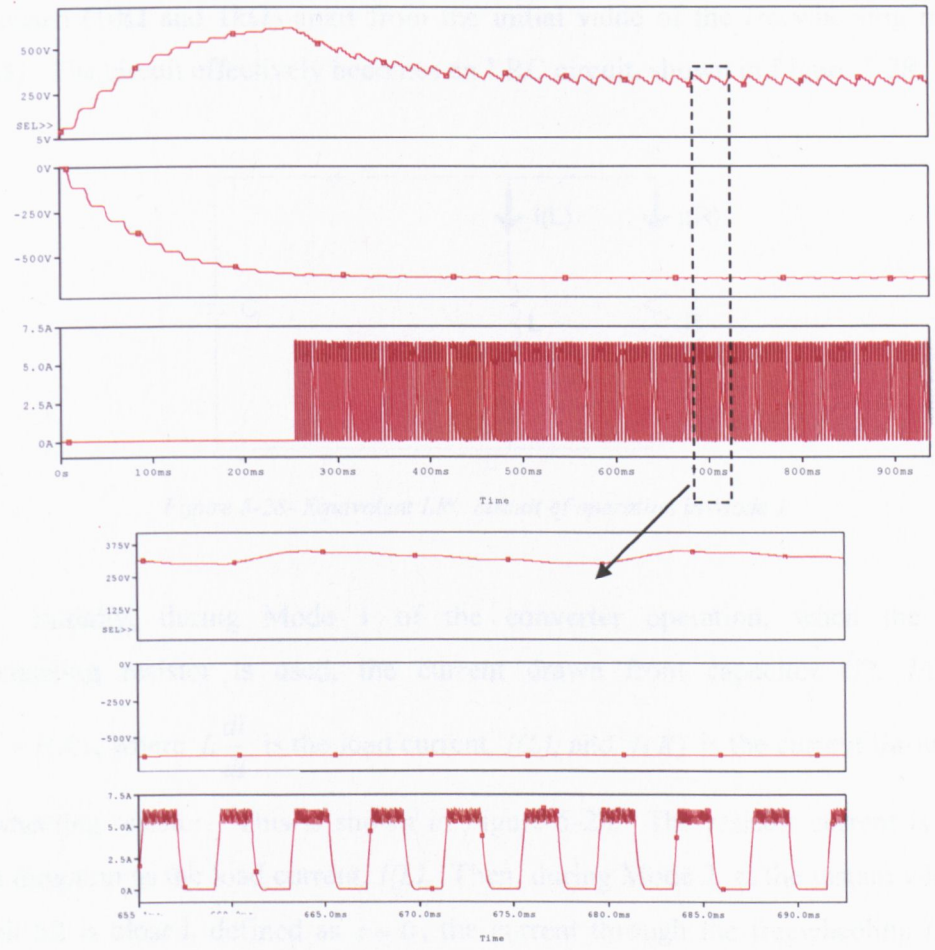


Figure 5-26- Voltage output of capacitors C2 (top) and C4 (middle), and load current (bottom) at increased speed of 15000rpm – zoomed out section marked with the dashed lines

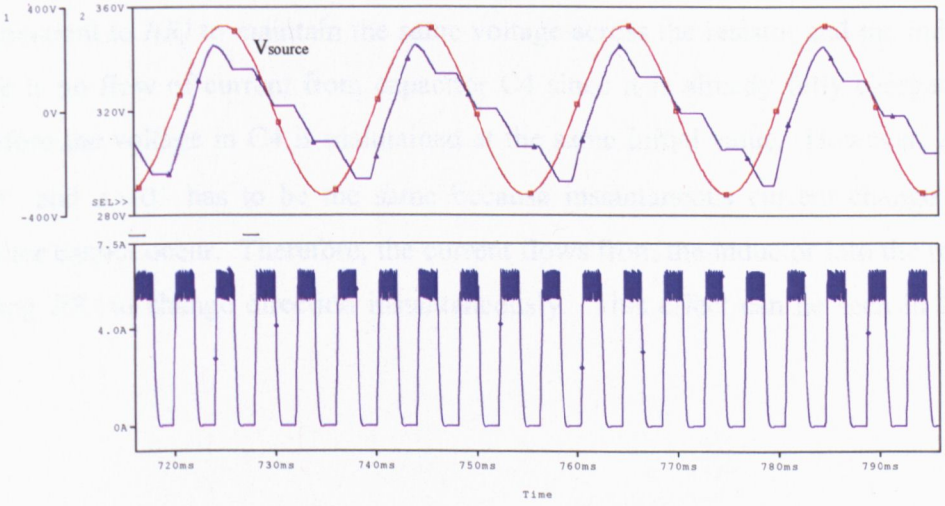


Figure 5-27- Voltage output of capacitors C2 (top) compared with the mains supply voltage, and load current (bottom) at increased speed of 15000rpm

Further analysis of the converter looks at the criteria for selection of the freewheeling resistor size. To demonstrate this, two values of freewheeling resistors

are chosen (10Ω and 1kΩ) apart from the initial value of the freewheeling resistor (110Ω). The circuit effectively becomes an LRC circuit, shown in Figure 5-28.

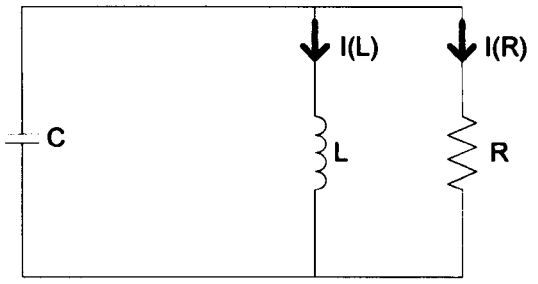


Figure 5-28- Equivalent LRC circuit of operation in Mode 1

Initially, during Mode 1 of the converter operation, when the 110Ω freewheeling resistor is used, the current drawn from capacitor C2, *I(C2)* is $L\frac{di}{dt} + I(R)$, where $L\frac{di}{dt}$ is the load current, *I(L)*, and $I(R)$ is the current through the freewheeling resistor. This is shown in Figure 5-28. The resistor current is in the same direction as the load current, *I(L)*. Then, during Mode 2, at the instant when the switch S2 is closed, defined as $t = 0$, the current through the freewheeling resistor instantaneously changed to the opposite direction. The reason for this is as follows: At $t = 0^-$, *I(L)* is equal to the maximum hysteresis threshold value, but *I(L)* at $t = 0^+$ is equivalent to *I(R)* to maintain the same voltage across the resistor and the inductor. There is no flow of current from capacitor C4 since it is already fully charged, and therefore the voltage in C4 is maintained at the same initial value. However, *I(L)* at $t = 0^-$ and $t = 0^+$ has to be the same because instantaneous current change in an inductor cannot occur. Therefore, the current flows from the inductor into the resistor causing *I(R)* to change direction instantaneously. This effect can be seen in Figure 5-29.

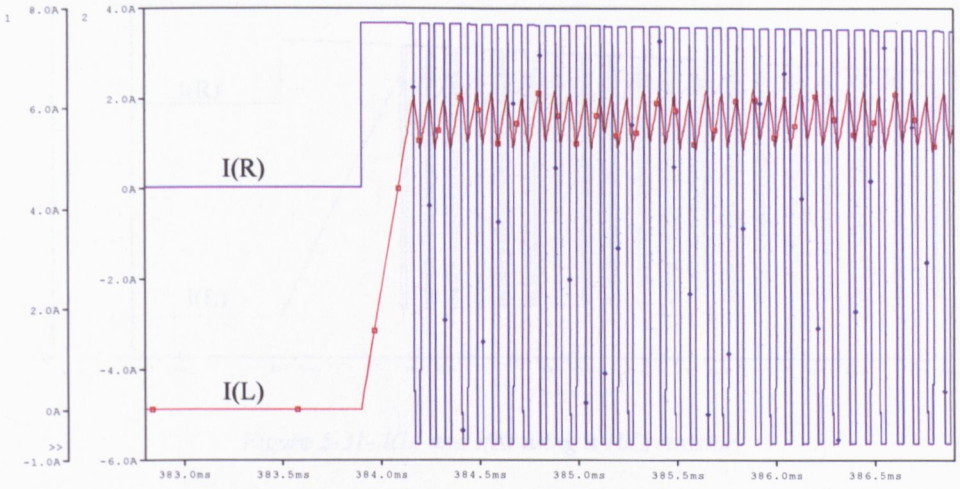


Figure 5-29- Load current, I(L) and current through the freewheeling resistor, I(R)

A smaller value of R will result in a smaller RC time constant (C is always the same). In Mode 1, during the time when *I(L)* increases from zero to reach the maximum defined hysteresis threshold, *I(R)* instantaneously reaches the maximum value defined by $\frac{V_{C2}}{R}$. As the value of R is small, *I(R)* is therefore very large. Therefore, a significant amount of energy is drawn from capacitor C2 to provide this large current. This is seen as a significant voltage drop in VC2 shown in Figure 5-30. Figure 5-31 shows *I(L)* and *I(R)* using the 10Ω resistor. In Mode 2, at the instant when the switch S2 is closed, $t = 0$, the current through the freewheeling resistor instantaneously changed to the opposite direction. Since current cannot change instantatenously through the inductor between $t = 0^-$ and $t = 0^+$, a significant amount of energy is drawn from the capacitor C4 to provide same voltage across the inductor and the resistor.

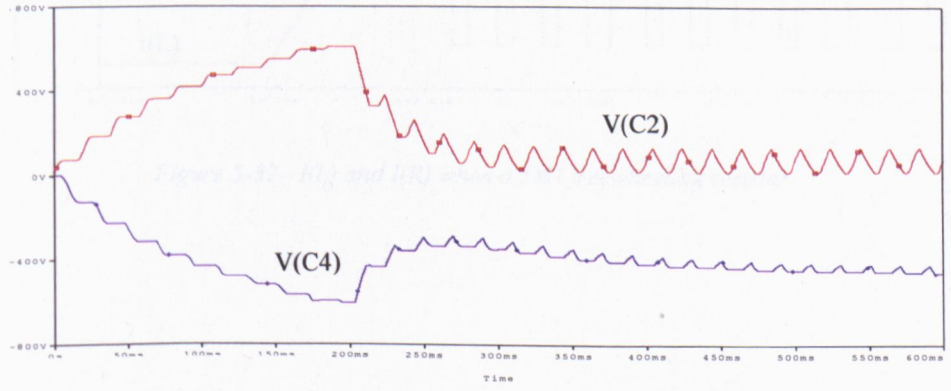


Figure 5-30– Significant voltage drop in VC2 and also in VC4.

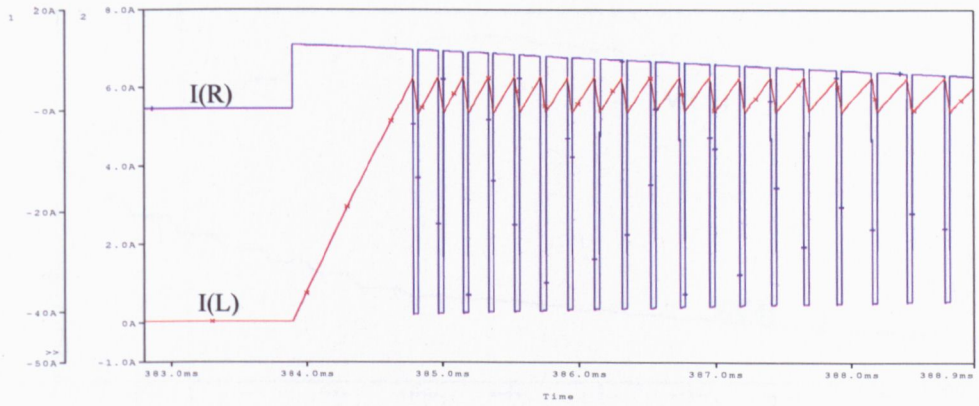


Figure 5-31- I(L) and I(R) using a 10Ω resistor.

Using the largest value of the freewheeling resistor, the RC time constant becomes the slowest. Therefore, during the time when *I(L)* increases from zero to reach the maximum defined hysteresis threshold, *I(R)* instantaneously reaches a small value since the circuit is more resistive. Only a small amount of energy is drawn from capacitor C2 to provide this small current, $L\frac{di}{dt} + I(R)$. Figure 5-32 shows a portion of *I(L)* and *I(R)* using the 1kΩ resistor. In Mode 2, again using the argument that *I(L)* cannot change instantaneously between $t = 0^-$ and $t = 0^+$, the current flows into the resistor, and since the resistor is large, some of the current flows into capacitor C4 providing an energy increase to the capacitor. This is shown in Figure 5-33.

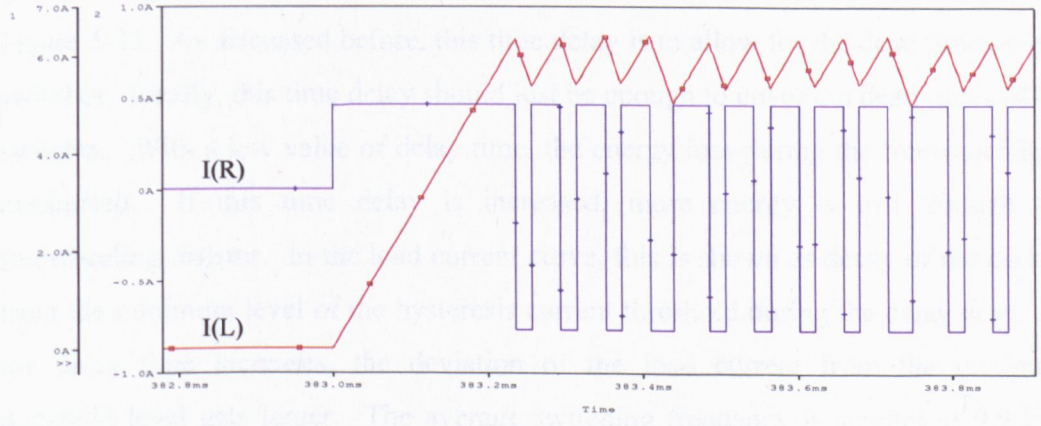


Figure 5-32– I(L) and I(R) when a 1kΩ freewheeling resistor

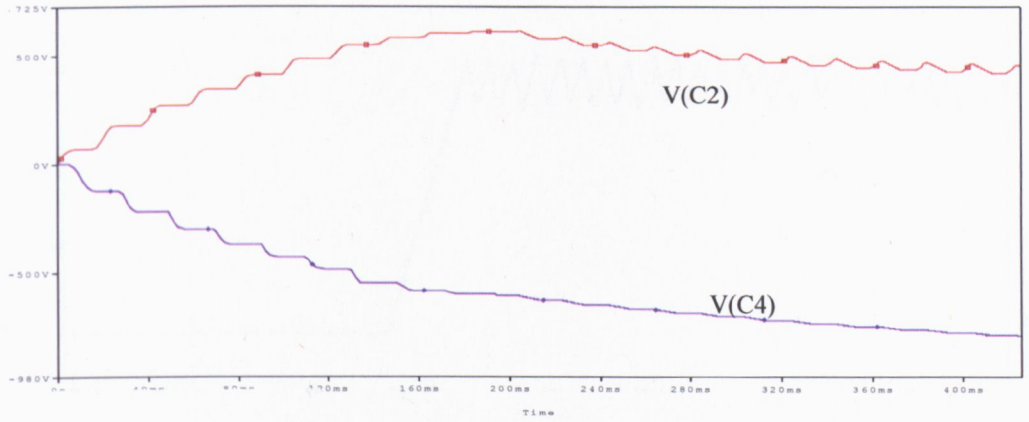
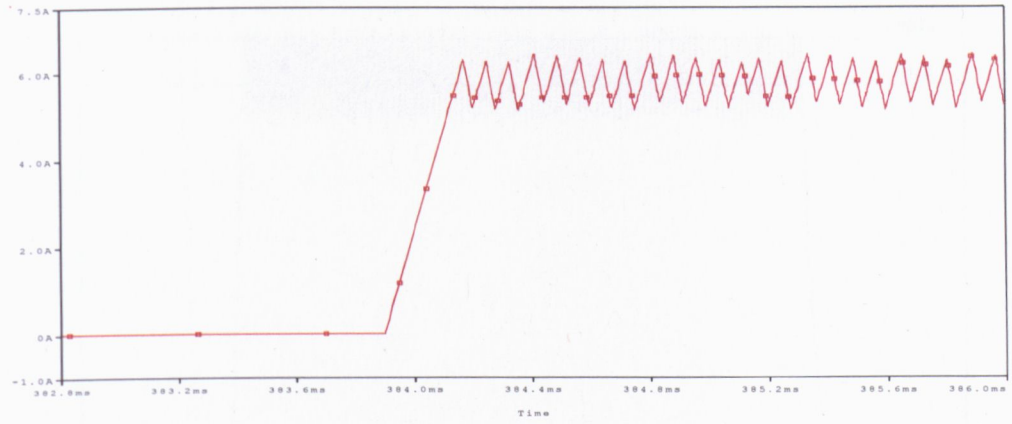


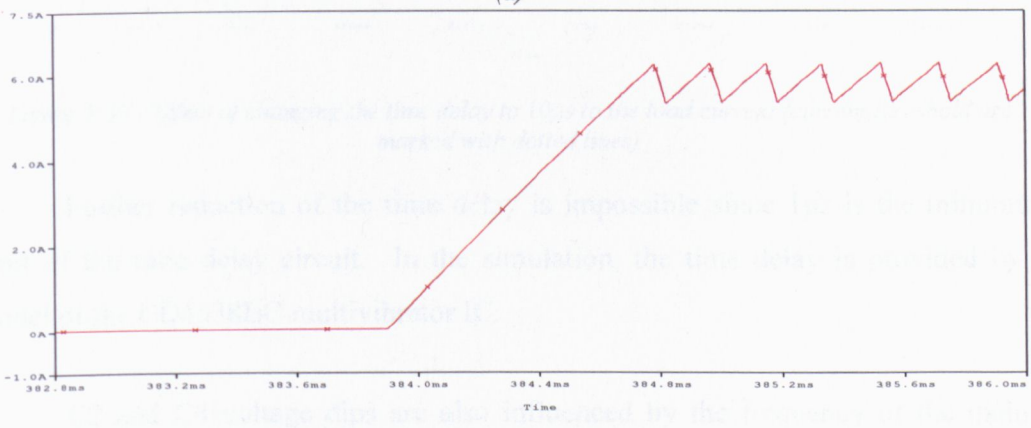
Figure 5-33– Voltage ripples in C2 and voltage increase in C4

Figure 5-34 shows the *I(L)* curve (over the same time period) for the three different values of the freewheeling resistor. The different di/dt can be observed, and this also results in different switching frequencies between the three freewheeling resistor values. The largest resistor used results in the fastest di/dt and faster switching frequency, while the smallest freewheeling resistor used results in the slowest di/dt and slowest switching frequency.

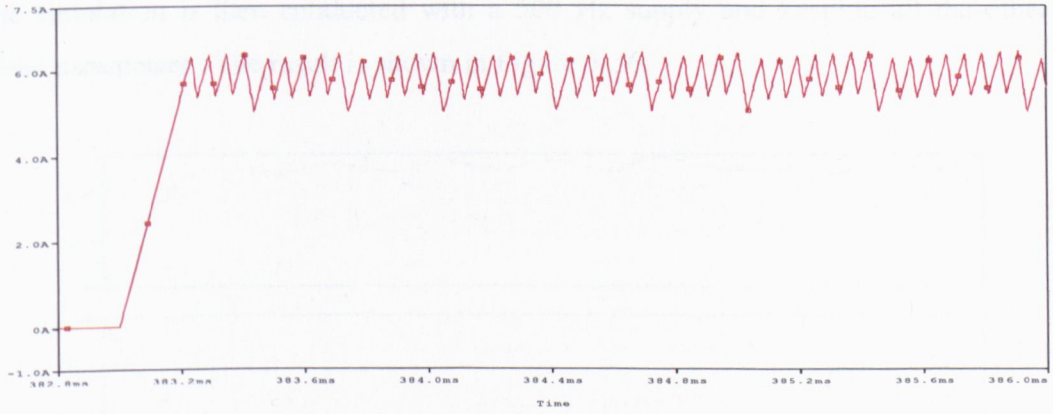
All the results are obtained using a simulation time delay of 1μs. To see the effect of changing the time delay, the time delay is changed to 10μs while keeping the freewheeling resistor the same as the initial value at 110Ω. The result is shown in Figure 5-35. As discussed before, this time delay is to allow for the dead times of the switches. Ideally, this time delay should just be enough to cover the dead times of the switches. With a low value of delay time, the energy loss during the freewheeling is minimised. If this time delay is increased, more energy is lost through the freewheeling resistor. In the load current curve, this is shown as decay of the current from the minimum level of the hysteresis current threshold during the delay time. As the delay time increases, the deviation of the load current from the minimum threshold level gets larger. The average switching frequency is smaller at 9.9 kHz (reduction by 24% from the initial switching frequency), which is expected because the delay times after each switching event causes the next switching to be delayed.



(a)



(b)



(c)

Figure 5-34– I(L) curves when different values of freewheeling resistor is used: showing the different di/dt and switching frequencies (a)110Ω (b)10Ω (c)1kΩ

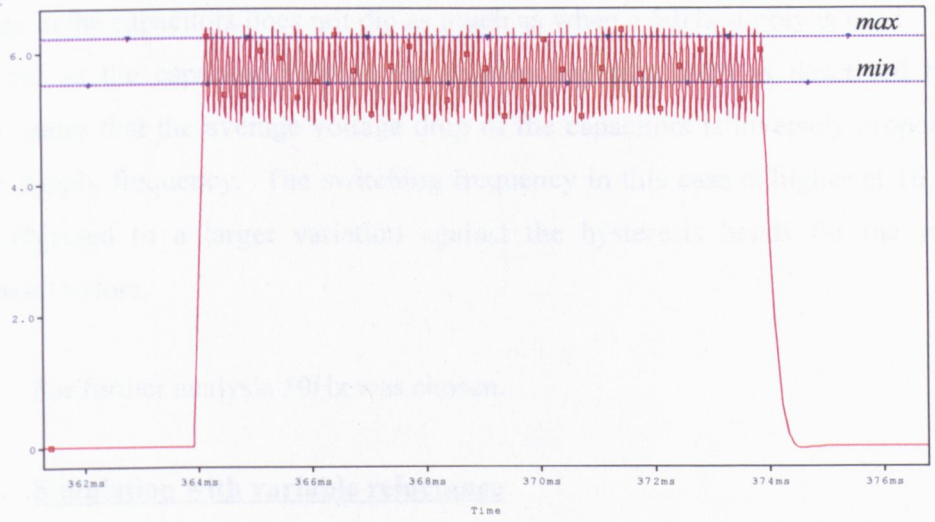


Figure 5-35 - Effect of changing the time delay to 10μs to the load current (current threshold are marked with dotted lines)

Further reduction of the time delay is impossible since 1μs is the minimum limit of the time delay circuit. In the simulation, the time delay is provided by a model of the CD4538BC multivibrator IC.

C2 and C4 voltage dips are also influenced by the frequency of the mains. The simulation is then conducted with a 500 Hz supply and keeping all the other initial parameters. The result is shown in Figure 5-36.

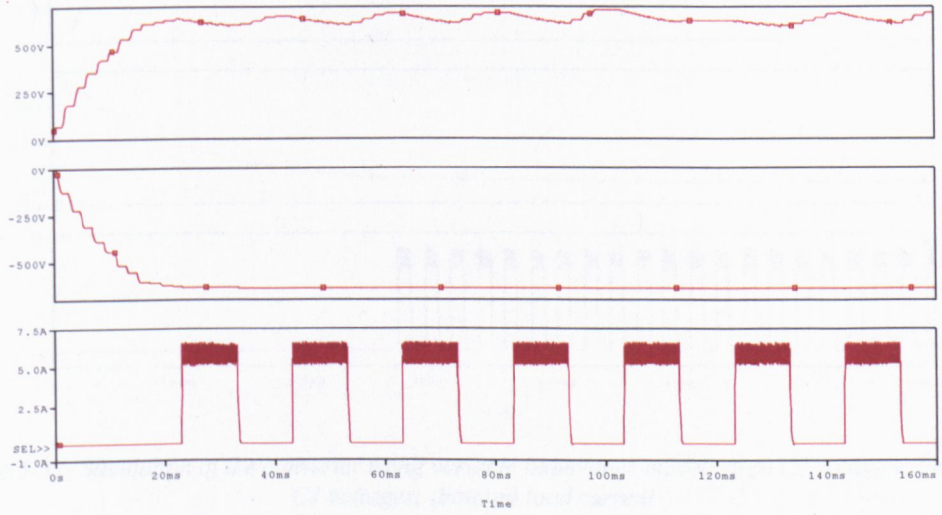


Figure 5-36 - Voltage output of capacitors C2 (top) and C4 (middle), and load current (bottom) with a 500Hz supply

As seen in the simulation result, the capacitors charge up much faster (in about 20ms) since each cycle of the mains has shorter periods. It is also observed that the

voltage in the capacitors does not dip as much as when a 50Hz supply is used. This is expected as the capacitor voltage dip follows equation 5-26 as described before, which states that the average voltage drop of the capacitors is inversely proportional to the supply frequency. The switching frequency in this case is higher at 16.4 kHz and subjected to a larger variation against the hysteresis bands for the reasons discussed before.

For further analysis 50Hz was chosen.

5.6.2. Simulation with variable reluctance

The same simulation settings have been applied, but this time, a variable inductance model as described in Chapter 2 is used. The value of minimum inductance is 11.7mH, and the maximum inductance is 30mH. This has been selected to be the same as the values used in Chapter 2 for ease of comparison. Figure 5-37 shows the simulation result for the proposed converter using a variable inductance model with minimum (L_{min}) and maximum (L_{max}) values of inductance. Voltages of capacitors C2 and C4 with the load current are shown.

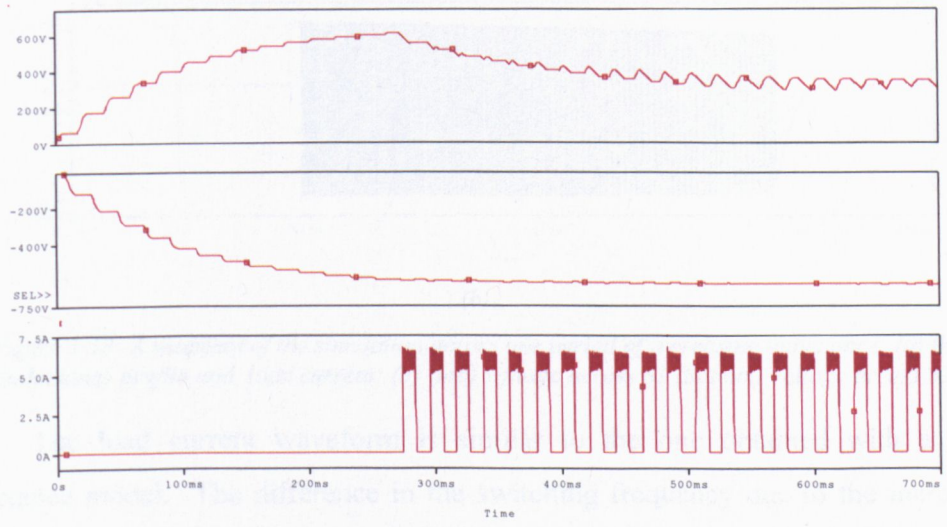
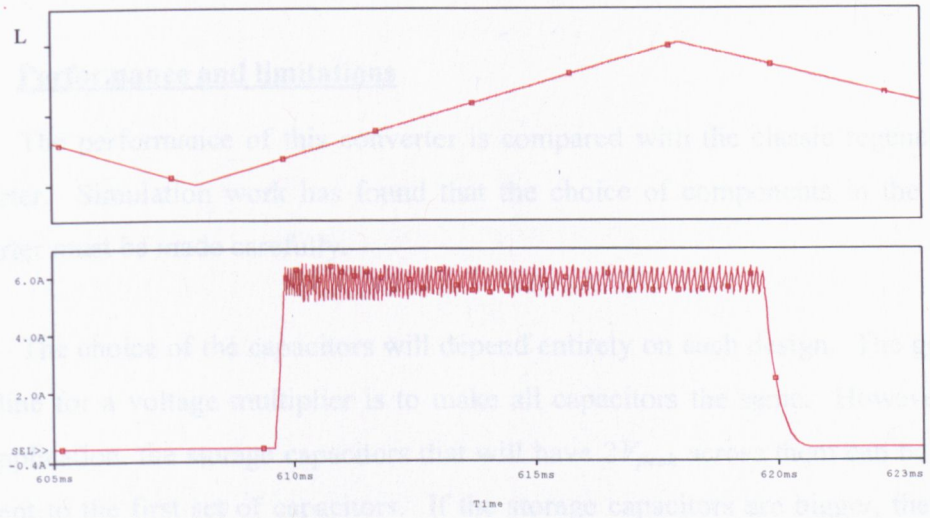


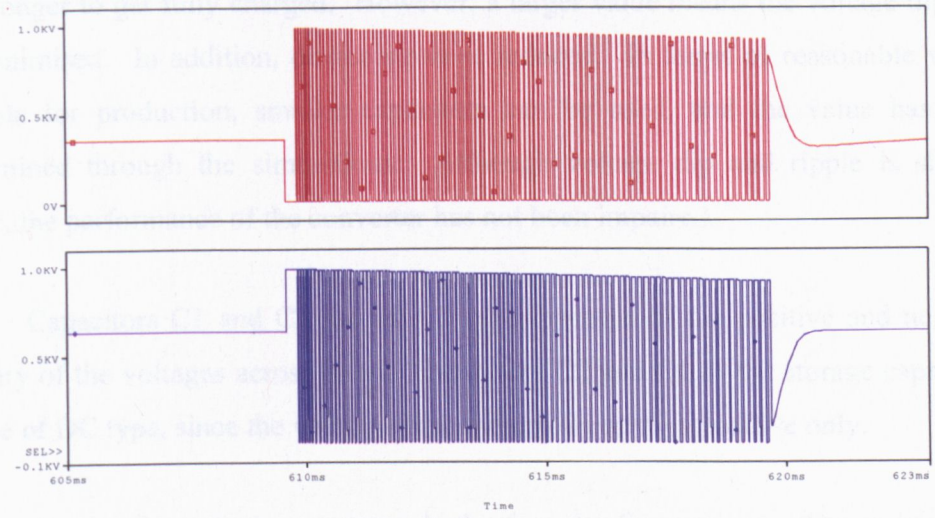
Figure 5-37- Simulation of the converter using variable inductance model; (top) C2 voltages; (middle) C4 voltages; (bottom) load current

To enable the changes in the switching frequency to be seen clearly, the simulation results are presented only during the time of increasing inductance or the machine turn-on time. The value used here is the same as the machine turn-on time calculated in Chapter 4. During the 10ms, the inductance is assumed to rise linearly

from L_{min} to L_{max}. Figure 5-38 shows a section of the load current and voltage stresses across the switches during one period of the increasing inductance.



(a)



(b)

Figure 5-38- A snapshot of the simulation across one period of increasing inductance; (a) the inductance profile and load current; (b) (top) voltage across S1 (bottom) voltage across S2

The load current waveform is similar to the one obtained with a static inductance model. The difference in the switching frequency due to the increasing value of inductance can be clearly seen. At the beginning of conduction where the inductance value is minimum, the switching frequency is 15.4 kHz; while at the end of the conduction where the inductance value is maximum, the switching frequency is 8.8 kHz. As for the voltage across the switches, the result shows similar values from the previous simulations with a static inductance model. The voltage across the switches during conduction is $2V_{peak}$.

It can be observed that the current rise time is faster than the current fall time due to the different values of inductance at the start and the end of the phase conduction.

5.7. Performance and limitations

The performance of this converter is compared with the classic regeneration converter. Simulation work has found that the choice of components in the novel converter must be made carefully.

The choice of the capacitors will depend entirely on each design. The general guideline for a voltage multiplier is to make all capacitors the same. However, for this application, the storage capacitors that will have $2V_{peak}$ across them can be made different to the first set of capacitors. If the storage capacitors are bigger, they will take longer to get fully charged. However, a larger value means the voltage dip will be minimised. In addition, device stress is reduced. In terms of reasonable values suitable for production, smaller capacitors can be used, and the value has been determined through the simulations. Although voltage dip and ripple is slightly larger, the performance of the converter has not been impaired.

Capacitors C1 and C3 are of AC type, because of the positive and negative polarity of the voltages across them. Capacitors C2 and C4 or the storage capacitors can be of DC type, since the voltages across them are always positive only.

Another important component is the freewheeling resistor. The resistor size will determine the losses as energy is dissipated during the freewheeling mode. This will effect the deviation from the desired current threshold band.

Another design criterion is the voltage dip of the capacitor voltages. As mentioned before, the simulation was done with the worst case scenario as the rotor position signal has a 50% duty cycle. In reality, this is never adopted. Using a lower duty cycle, for example, 10% will enable the capacitors to be charged up much faster between each machine stroke. Therefore, the voltage dip and ripple will be minimised.

The simulation work also recommends that the converter is used for higher speed machines. This is because, at higher speeds, the capacitors do not lose energy as rapidly compared to slow running machines. Therefore, the converter becomes highly efficient. The capacitor voltage ripples are also improved.

Simulation with a static inductor and a variable inductor has shown no difference in performance, except the changes in switching frequency and di/dt. This has been expected based on the simulation work on SP-SRM converters in the previous chapter. The switching frequency change is due to the different values of inductance at the start and end of each commutation.

Based on simulations, a few suggested values to be used to achieve optimum performance of the converter connected to a standard single-phase grid (V_{supply} = $230Vac, 50Hz$):

$R_{freewheel} = 110\Omega$ $\qquad$ $t_{delay} = 1\mu s$

$C1 = C3 = 200\mu F$ $\qquad$ $C2 = C4 = 100\mu F$

Clock period = 2ms (for 15000 rpm SP-SRM speed)

5.8. Advantages and disadvantages

Section 5.2 has discussed the processes of achieving the new converter concept. Based on that, a new converter design has been proposed in this chapter. Section 5.4 then justifies whether each process has been met. The next task is to justify the advantages and disadvantages of the proposed converter compared to state-of-the-art topologies taking into account whether the converter has achieved the desired criteria.

Firstly, all state-of-the-art converter topologies for SP-SRM are able to produce unipolar current in pulses based on the feedback from rotor position sensors. The new converter concept has also this ability. The controller used in the simulation accepts an input from the rotor position sensors and uses this information to determine the switching.

The new converter has the ability to supply double the peak supply voltage to the machine winding. In addition, the arrangement of the capacitors and diodes in the voltage multiplier means that positive and negative voltage rails can be supplied to the machine. In an SP-SRM, this is most useful. Previous work mentioned in Chapter 3, have tried to achieve this dual rail effect by splitting the DC link [89]. However, this topology requires an even phase machine and reduces the input voltage by half. This also reduces the operating speed range by half. In this circuit, dual voltage at double the supply is possible. Compared to the single supply rail commonly used in prior art of SP-SRM converter topologies, the double voltage rail proposed here can provide high speed operation [110].

The positive high voltage is used for providing the magnetising current for the windings. The negative voltage is applied at the terminal to achieve defluxing. During turn-off, this very high voltage is used to force faster defluxing of the phase windings. Higher voltages means higher rate of change of current can be achieved. The current, therefore, quickly goes down to zero before the next commutation. This is the main advantage of the proposed converter, since achieving zero current at the start of commutation is desirable to maintain the torque. Potentially, the fast rate of change of current during magnetising and defluxing means the converter will enable the machine to work at advance angles, and thus, higher speeds.

Through the arrangements of the capacitors and diodes, the converter is capable to handle recovered energy from the windings. The energy is fed back to the capacitors during one of the operating modes described earlier.

One disadvantage of the circuit, which have to be considered when designing the converter for a particular application, is the charging delay time. This will depend on the values of capacitors used. However, for this application, the delay time is only significant at the start when the machine is not switching.

With the proposed converter arrangement, advance angle control is possible. To achieve this, simple position sensor arrangements cannot be used. The commutation angle must be advanced by several degrees to the aligned position. This enables the machine to achieve higher efficiency.

The simple controller in the simulation uses a fixed dwell angle of 45°. This can be achieved by having a slotted disk and an optical interrupter as described in Section 2.4 in Chapter 2. The position of the slotted disk with respect to the aligned position has been fixed. This means that the speed of the machine will be fixed too.

At high speeds the firing angle is critical to determine the current waveform of the machine. Most importantly, T_{off} needs to be carefully selected so that it does not happen beyond the full alignment rotor position producing negative torque. If this happens, the machine efficiency is compromised. It is desirable to achieve a precision of 0.5° or even 0.25° [31]. The use of a more advanced control scheme with online monitoring of machine speed and precise calculation of the dwell angles is recommended to enable the machine to be used at higher speeds and highest performance.

Table 5-1 show the comparison between the proposed converter and the direct regeneration converter in terms of peak voltage ratings of the converters at steady state. From the tables, it is clear that only the capacitors from the first stage that is rated to withstand V_{peak}. This is clearly a difference with the classic direct regeneration converter where all the components are rated at V_{peak} because all components never have to withstand any voltage larger than the supply rail.

In Table 5-2, the comparison of rms current rating between the classic direct regeneration converter and the novel converter is provided. The rating is expressed in per unit value with the classic converter as the benchmark; all capacitors are compared to the DC ink capacitor, and all diodes are compared to the rectifier diodes (D_{rect1} to D_{rect4}). The freewheeling resistor receives the full unit value because there is no comparable component in the classic direct regeneration converter. For identifying the components, the table refers to the component labelling as in Figure 5-19.

From the tables, it can be seen that the rms current rating for the proposed converter is much lower or similar to the ratings of the classic direct regeneration converter. The voltage ratings are for the highest voltage stresses during worst case operation. This takes into account the charging of the capacitors up to its maximum value possible (controllable) as well as the switching spikes.

	Direct regeneration converter	Proposed SP-SRM converter
C1 , C3	-	1
D1 , D3	1	1
C2 , C4	-	2
D2, D4	1	1
S1 , S2	1	4
$r_{freewheeling}$	-	4
D_{rect1} to D_{rect4}	1	-
DC link capacitor	1	-

Table 5-1- Voltage ratings (per unit) for the direct regeneration converter and the proposed converter

	Direct regeneration converter	Proposed SP-SRM converter
DC link capacitor	1	-
C1	-	0.66
C2	-	0.61
C3	-	0.35
C4	-	0.26
D_{rect1} , D_{rect3}	1	-
D_{rect2} , D_{rect4}	1	-
D1	1	2.23
D2	1	2.30
D3	-	1
D4	-	0.91
S1	1	2.18
S2	1	0.17
$r_{freewheeling}$	-	1

Table 5-2- RMS current ratings (per unit) for the direct regeneration converter and the proposed converter

The RMS current ratings for diodes D1 and D2, as well as switch S1 are about twice the ratings of similar components in the classic direct regeneration converter. The reason for the large rating for the diodes is because the diodes are used in the path where current is flowing to charge up capacitor C2. C2 voltage is constantly being charged and recharged as the energy is being used for switching. Therefore, large currents are seen across the two diodes. As for the switch, when switch S2 is on, switch S1 sees the full $2Vpeak$ across its terminals. Therefore, the switch has to withstand the high voltage, and the ratings become higher.

To further justify the design, a comparison was made between the proposed converter and the classic regeneration converter in terms of VA ratings of the

components (obtained from the simulations) as well as cost of major converter components. Table 5-3 shows the comparison between the two converters.

Proposed converter

Component	V_{max}	I_{max}	VA rating	Cost
D1	336.890	1.649	555.40	0.40
D2	336.887	1.730	582.81	0.40
D3	333.870	1.120	373.93	0.40
D4	306.450	1.109	339.91	0.40
C1	336.890	0.957	322.30	3.40
C2	607.163	0.918	557.38	10.00
C3	337.887	0.138	46.63	3.40
C4	620.106	0.112	69.45	10.00
S1	1216.00	0.914	1111.42	5.00
S2	1216.00	0.511	621.89	5.00
$r_{freewheeling}$	616.085	3.19	1965.31	2.00
Total			**6546.44**	**40.40**

Direct regeneration converter

Component	V_{max}	I_{max}	VA rating	Cost
$D_{rect}1$	239.140	0.261	62.34	0.40
D_{rect2}	239.141	0.293	70.00	0.40
D_{rect3}	239.141	0.298	71.26	0.40
D_{rect4}	239.140	0.286	68.49	0.40
D1	238.563	2.757	657.77	0.40
D2	238.563	2.757	657.77	0.40
DC link capacitor	238.565	17.205	4104.51	60.00
S1	239.140	2.90	693.03	3.00
S2	238.079	2.87	683.29	3.00
Total			**7068.45**	**68.40**

Table 5-3 - The comparison between the proposed converter and the classic regeneration converter in terms of VA ratings and cost of major converter components

From the analysis above, the advantage of the proposed converter can be justified compared to the classic regeneration converter. The VA rating for the proposed converter is marginally lower.

As for the total cost of each converter, the price represents the average price obtained from three major electronic distributors. This cost comparison is based on optimised design of the proposed converter. For the proposed design, the prices for capacitors C1 and C3 are quite high since the capacitors are of AC type. For capacitors C2 and C4, the cost is based on having four capacitors arranged in series to

obtain the desired voltage rating. This arrangement still allows for normal operation of the converter. MOSFET cost is quite high due to the high voltage rating. Also, enhancement of the switch is not an option since there are always two switching devices used in the circuit, and replacing the switches with IGBTs would cost higher.

For the classic regeneration converter, the main component which contributes to the high cost would be the capacitor. From the design and operating conditions, it is found that there must be a single capacitor at the stated ratings to function as the DC link.

Based on the analysis done, it can be concluded that both the converters can operate at the same conditions, but the proposed converter does have an advantage in terms of cost and VA ratings. Although the proposed converter seems to have higher rated components, there is potential for the converter to be used for machines of higher speeds. At such speeds, the machine can be configured to achieve better efficiency, and this in turn could result in better economy.

5.9. Conclusion

The work in this chapter has proposed a novel converter topology for an SP-SRM. Some simulation work and analysis have been provided to confirm that the circuit is suitable for an SP-SRM operation.

The next chapter describes the design of a prototype converter to investigate the operation and limitations of the converter. The performance of the converter will then be analysed and compared with the simulations.

CHAPTER 6
ASSESSMENT OF PROPOSED CONVERTER – EXPERIMENTAL ARRANGEMENTS

Chapter 5 has described a novel topology for SP-SRM converter. A detailed analysis of the circuit has been provided to enable clear understanding of the topology. Further investigation has to involve experimental analysis which will enable direct comparison to the simulated results, as well as comparison with the classical direct regeneration converter. This chapter will discuss the experimental arrangements for the proposed novel converter. The results will be presented accordingly to evaluate the converter performance.

This chapter is sub-divided into six sections. Section 6.1 describes in general the experimental setup of the converter circuit. Section 6.2 describes the power converter technology. This includes the converter input and output sides. The next sections, Section 6.3 to 6.5 discuss the control electronics, load configuration and test equipment. Section 6.6 gives detailed information on the measurements made and includes a summary of the measured data. More detailed circuit diagrams are given in Appendix B for the power converter, the controller and the additional electrical and electronic circuits. A pictorial view of the converter is available in Appendix D.

6.1. Experimental arrangements of the drive set-up

Ideally, the components of the SP-SRM drive system are the electrical power converter, the SP-SRM, the mechanical load, and the control electronics. However, as with the simulations, it is decided that a static load is used initially. This is so that the performance of the converter can be evaluated before continuing further. Each of the components in the drive system will be described in detail in the next sections.

The converter is connected to the AC mains supply as the input, and to an inductive load. The converter is controlled by an analogue electronic control system. Figure 6-1 shows the converter circuit and experimental test circuit arrangement of the converter.

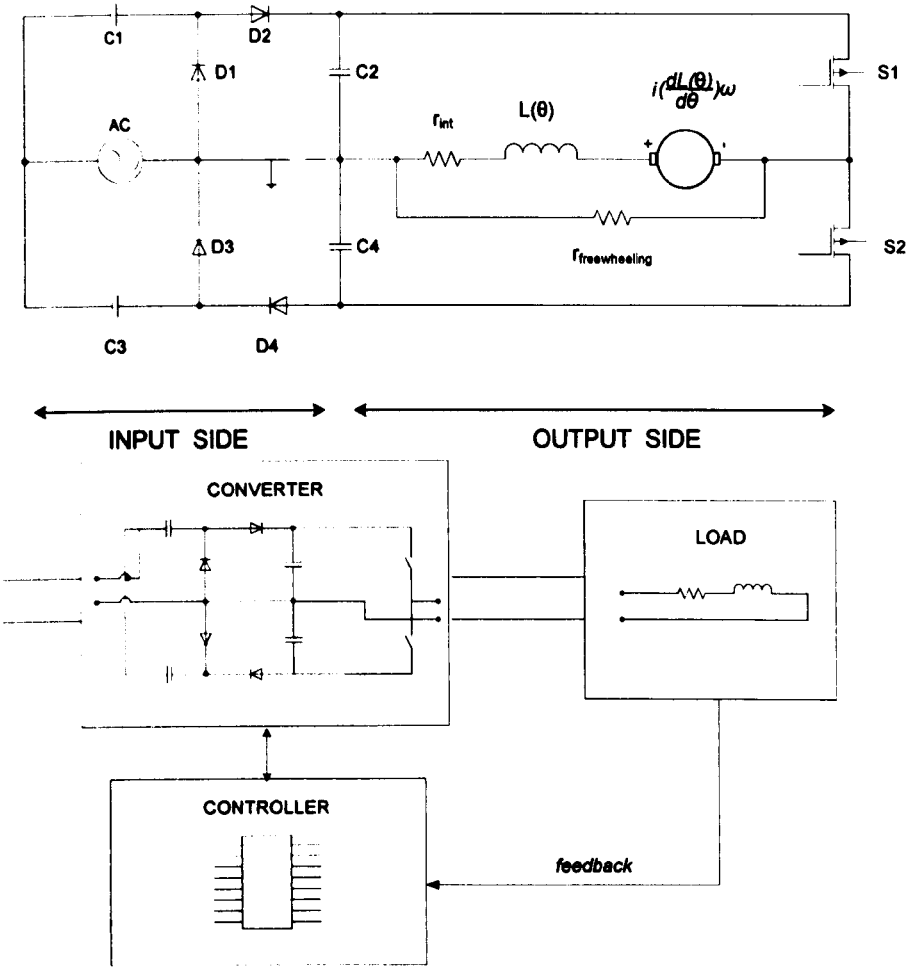


Figure 6-1- (a) Converter circuit and (b) Experimental test circuit arrangement of the converter

6.2. Power converter configuration

A 1kW converter has been developed for comparative study. Figure 6-2 shows the general setup for the converter. The converter has two main elements: the voltage doubler stage including the storage capacitors, and the inverter.

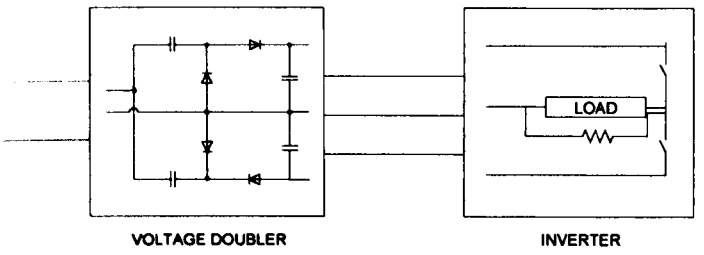


Figure 6-2– Converter arrangement

6.2.1. Input side

The input from the mains supply is doubled using the voltage doubler circuit. The rated input voltage of 230V rms (340 peak) allows a peak voltage in the storage capacitors to be 680V. The rated power line current is 10A. A resistor is placed at the supply line to limit the large in-rush current during startup. This resistor also limits the current into the devices during the period when the capacitors are charging.

To protect the mains from any spikes, an isolation transformer is used. The isolation transformer is then connected to a single phase variable AC supply. Therefore, it is possible to control the input voltage to the converter. This enables the tests to be done from a lower voltage and then increased slowly.

For capacitors C1 and C3, the capacitors used are 200μF B3236 series AC capacitors by EPCOS rated at 250Vac. Capacitors C2 and C4 are 1mF ALS30 series DC capacitors by BHC rated at 500V. Since the voltage rating is insufficient to provide for 600V as required, two capacitors are connected in series to provide a rating of 1000V at the same capacitance. For each of capacitors C1 and C3, a 1kΩ, 150W resistor is connected in parallel to allow for discharging when the experiment is stopped. For capacitors C2 and C4, the discharging resistor used 4.7kΩ, 50W each. The discharging process ensures the capacitors are empty before the start of consecutive tests. Capacitor C2 is connected to a voltmeter panel to give a visual indicator of the voltage level.

As for the diodes, two diodes from IXYS DSEP 15-12CR are used. There are two diodes in each module. The diodes are mounted onto a heatsink to provide cooling.

6.2.2. Output side

A bank of inductors is connected to the inverter. The inverter involves one upper and one lower MOSFET. The MOSFET used is model 2SK2349 from Sanyo, rated at 1500V (drain-to-source voltage) and 10A (drain current). With the proposed converter, the problem that is faced is to find a suitable component to withstand the high voltage, high current and high speed operation of the converter. Currently, in the power electronics devices market, only a handful of MOSFETs are available for such high working voltage. The decision to use the MOSFET from Sanyo is due to its high voltage rating, as well as high drain current. Also based on the device current rise and fall time, the device can be operated at high frequencies (more than 500 kHz).

However, the device is quite recent in the market, and operation at such voltage is not common. The device is rated at 1500V when the operation of the inverter requires a voltage of 1200V across the MOSFETs during turn-off. It is calculated that the device would not be able to withstand the turn-off voltage as well as any voltage spikes (due to the back EMF from the load). Therefore, a decision was made initially to lower the voltage to half the required voltage. When the input voltage is doubled, the voltage would only be up to 300V peak. Once this is successful, then the input voltage would be increased.

The MOSFET is to be controlled by HCPL-316J from Agilent Technologies. This 2A gate drive allows isolation between low and high side voltages, integrated desaturation (V_{CE}) detection and fault detection feedback. Also, the TTL input logic levels allows direct interface with the Digital Signal Controller (DSC) module.

All the components from the input and output sides (diodes, capacitors, discharging resistors, transceiver ICs, MOSFETs and MOSFET drivers) are mounted onto a big piece of PCB to eliminate any noise propagation from cables.

6.2.3. Other circuits

Other circuits associated with the power converters are: Hall effect voltage transducers for voltage measurements of the storage capacitors; Hall effect current transducer for phase current measurements; power switch gate drive circuit including

the driver module HCPL-316J; communication systems with the controller; protection circuits; and auxiliary power supplies.

The voltage measurements are provided by two separate Hall effect voltage transducers capable of measuring voltages up to 1000V. The Hall effect current transducer uses a 6A nominal current device with a bandwidth from DC to 200 kHz. The gate drive circuits for the MOSFETs allow 2A isolated gate pulses to flow into and out of the gate. The gate driver includes voltage saturation detection, fault protection feedback, power supply under-voltage lockout and 'soft' turn off of the MOSFETS in case of any fault. The driver communicates with the controller via bi-directional transmission lines. Transceivers on the driver and the controller allow noise-free transmission of data.

Circuits have also been included for safety and protection. Protection circuits are overvoltage and undervoltage protection of the storage capacitor voltages, overcurrent protection of the output current, input current limitation, driver faults and overtemperature protection of the MOSFETs. The overvoltage prohibits the capacitor voltages to increase more than the maximum voltage ratings. Undervoltage protection eliminates the case of generating an inrush current during the short circuit of the storage capacitors. Overcurrent protection is necessary to exclude any overheating of the devices or man failure. A temperature sensor is mounted on the heatsink at the vicinity of the MOSFETs to monitor the heatsink temperature. A maximum temperature of 100°C is recognised as a fault, and all gate drives and mains supply are then shut down.

The MOSFET drivers have each a DC-to-DC converter supplied by an external isolated DC power supply. This provides isolation between the high side and low side voltages. The control systems also has another external isolated DC power supply.

6.3. Control electronics

The control electronics are mounted in a separate enclosure, with connections to the power converter. In this arrangement, the control electronics provides; pre-setting of the hysteresis thresholds; display of the voltages, temperature and current;

visual indication of any fault via LEDs; and a manual converter start switch. There are cable connections which permits data transfer from the voltage and current measurement cards and to the MOSFET drivers in the power converter box.

The Digital Signal Controller (DSC) used is 40-pin dsPIC30F3011 by Microchip. The device has the capability to operate up to a speed of 30 Millions Instructions Per second (MIPs). The controller takes advantage on some of the peripheral features of the device such as high current sink/source I/O pins up to 25mA/25mA, timer module with programmable prescaler and I^2C module (for using I^2C LCD display). The device also has 10-bit Analog-to-Digital Converter (ADC) for recording of the measurements. The capability of the device for In-Circuit Serial Programming (ICSP) makes it flexible enough for debugging while online.

The control is based on the hysteresis current control. The control loop can be described in Figure 6-3. The hysteresis current control receives the user set reference values via the potentiometers. In an ideal situation, the value is compared to the current measured at the load to determine the switching pattern. Switching can only commence during the dwell angles. Rotor position is fed back to the controller to enable the converter to determine the dwell angles precisely. However, since a static load is used, the dwell angle is fixed at a pre-set value.

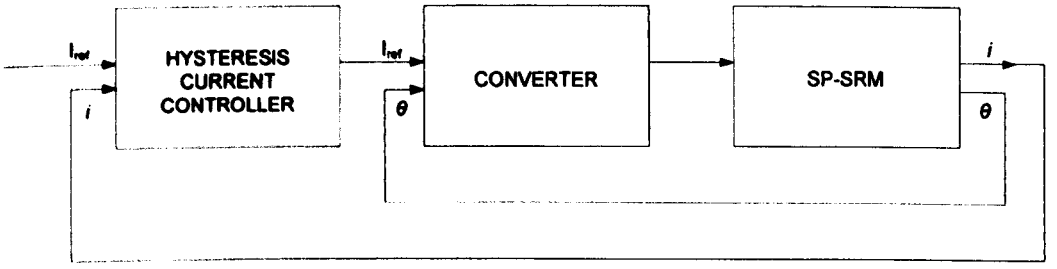


Figure 6-3- Control loop for the proposed converter

At the start of the converter operation, the capacitors are charged, and when the voltage reaches double the input voltage, a manual converter start switch has to be turned on. Two voltage transducer cards which monitor both the voltage doublers feed the analog readings to the DSC. The DSC converts the values to digital, and compares to the software pre-set values. LED indicators are used to indicate that the

pre-set values have been reached. Once the manual converter start switch is turned on, switching will commence.

S1 on the converter will turn on resulting in the load current to increase, and S1 will be turned off when the current reaches the upper current threshold value. Then, after allowing for a short delay (for the switch dead time) switch S2 is turned on. The current decays as the inductive load demagnetises through S2. When the current reaches the lower current threshold value, S2 will switch off, and S1 switches on again. This repeats throughout the time when the rotor is between the dwell angles. When the rotor goes past the dwell angles all switching will stop.

6.3.1. Set-up of the controller

During main operation of the controller, the DSC is set to be in idle mode. The DSC is woken up by interrupts that are executed according to the interrupt priorities. This ensures the efficiency of the DSC.

There will be three external interrupt sources which are all user-selected as priority level 7 (highest priority): External Interrupt 0 (INT0) and External Interrupt 1 (INT1) are both the respective driver error signal from the two MOSFETs used, while External Interrupt 2 (INT2) is the position sensor signal from the rotor position transducer. When either INT0 or INT1 happens, a fault signal will be generated by the controller and thus, all switching will be halted. When INT2 occurs, the controller will commence switching off the MOSFETs.

Other interrupt sources are Analog-to-Digital Conversion and Timer1. At the end of each Analog-to-Digital Conversion, the data in the buffer will be stored in appropriate variables to be read by the controller at a later point. If necessary, some calculations will also be performed so that the values will be suitable for display. Timer1 interrupt source is executed every 50ms and this has the least priority. This interrupt source is to enable the display of the current thresholds and the measured current value. The program flow for the DSC is available in Appendix C.

6.4. Load configuration

The static load consists of three inductors wired in series to match the maximum inductance of an SP-SRM. This maximum inductance represents the worst case scenario. The value of the inductor used is 100mH.

6.5. Test equipments

High voltage measurements were performed using differential voltage probes from UNIVERSAL PROBES. Current measurements were carried out using current probes from LEM. All the test equipment was tested and adjusted and offsets were recorded in case of any latter need for theoretical calculations. Cable lengths between the probe and oscilloscope were adjusted to ensure equal propagation delays for both voltage and current measurement set-ups. This is critical in case of losses between devices. Measured data were captured using Tektronix oscilloscope 4000 series (1GHz/ 5GS/s). This data is then transferred to the PC for manipulation and processing if later required.

6.6. Experimental measurements

From the simulation, it is found that using the full mains voltage as the input supply, the MOSFET ratings would be $4V_{pk}$. However, the actual voltage ratings of the 2SK2349 MOSFET used in the experimental work is only up to 1500V.

Initially, the supply is adjusted so that the $2Vpk$ value is 300V. This is to investigate the voltage spike across the MOSFET during turn off. From the test result, it is found that it would be safe to increase the supply voltage to 230V rms and therefore obtain $2Vpk$ at across the storage capacitors.

6.6.1. Input stage

At the start of the experimental analysis, once the rig has been set up, tests were conducted to investigate the input stage. At this point, the output stage is not connected. The controller is configured to allow only for charging of the storage capacitors. When the charging is successful, an LED is lit as an indicator. Therefore, the operation of the circuit as a voltage doubler can be confirmed.

Figure 6-4 below shows the voltages across the capacitors during the charging up period. Capacitors C1 and C3 has been charged up to *Vpk*, while capacitors C2 and C4 has been charged up to twice the *Vpk*. As mentioned in the previous chapter, it takes a few cycles of the mains before the capacitors are fully charged. The results show good agreement with the simulations (Figure 6-5).

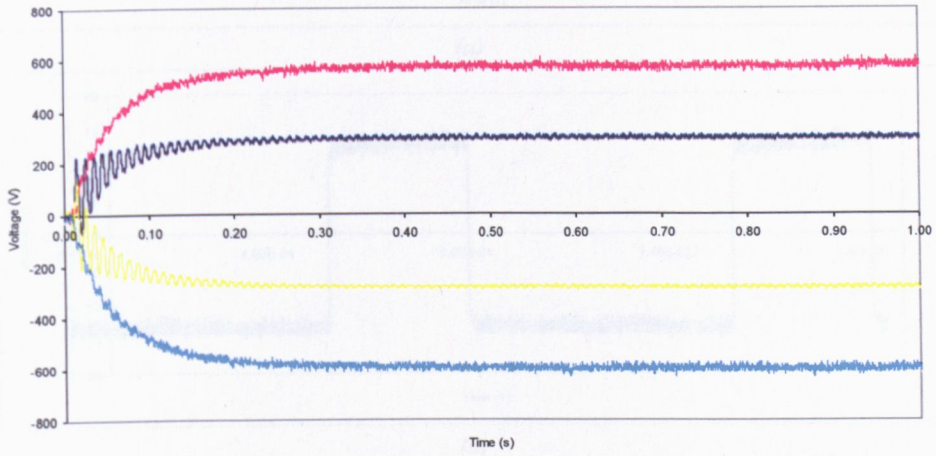


Figure 6-4 – Charging of capacitors: C3 (topmost), C1 (middle upper), C2 (middle lower) and C4 (bottom)

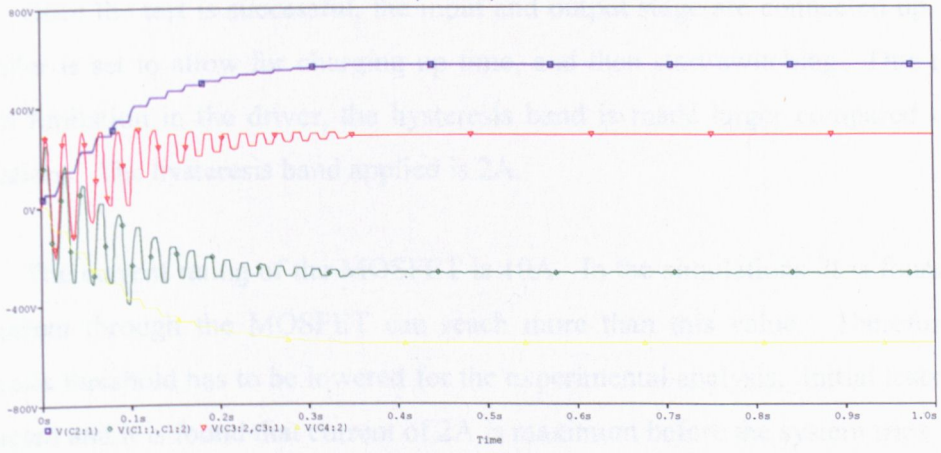
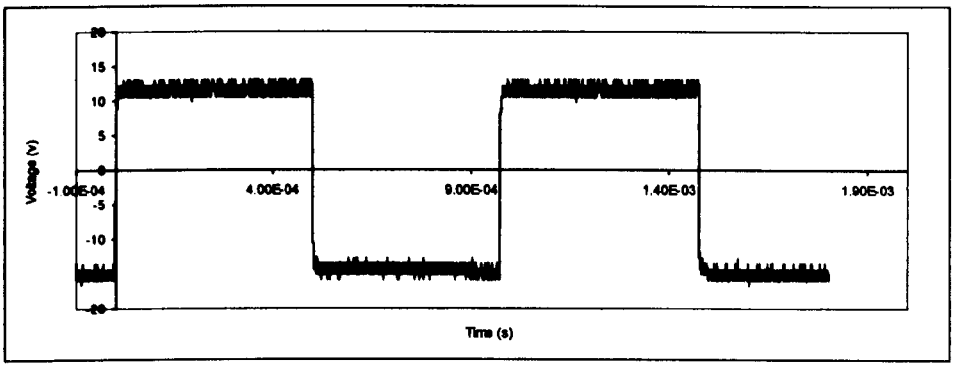


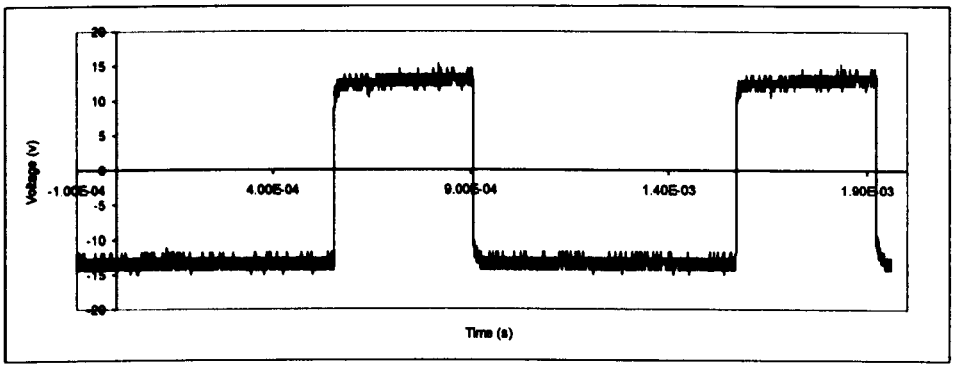
Figure 6-5 - Charging of capacitors from the simulations: C3 (topmost), C1 (middle upper), C2 (middle lower) and C4 (bottom)

6.6.2. Output stage

Before testing the converter stage, a critical step is to ensure driver signal is available to drive the MOSFETs. This is because the MOSFETs are very recent in the market, and there are no recommended drivers available yet. Figure 6-6 shows the MOSFET S1 and S2 V_{GS} signal showing the switching of the MOSFET. The driver is providing ±15V signal to the MOSFET gate. S1 and S2 are switched alternately.



(a)



(b)

Figure 6-6 – MOSFET V_{GS} signal (a) from S1 (b) from S2, showing the alternate gate signal

Once the test is successful, the input and output stage are connected up. The controller is set to allow for charging up time, and then start switching. Due to the current limitation in the driver, the hysteresis band is made larger compared to the simulations. The hysteresis band applied is 2A.

The current rating of the MOSFET is 10A. In the simulations, it is found that the current through the MOSFET can reach more than this value. Therefore the hysteresis threshold has to be lowered for the experimental analysis. Initial tests were conducted and it is found that current of 2A is maximum before the system trips.

Figure 6-7 shows the experimental load current waveform showing current hysteresis for one conduction period, compared with Figure 6-8 from the simulations. The threshold is set at 1.8A with delta of 0.5A. The switching frequency is 3.3 kHz. The simulated switching frequency for similar converter arrangements is 3.7 kHz. Figure 6-9 and Figure 6-10 show the voltage across capacitor C1 during the switching, obtained experimentally and through simulation, respectively. The capacitor voltage has been reduced to 66% of the initial voltage before switching commenced and the value stabilizes during converter operations. The simulation

however, shows that the voltage continues to decay with each cycle of the mains and stabilizes further on during the converter operations. Voltage across capacitor C2, however, stays the same during this period. Figure 6-11 shows the experimental result while Figure 6-12 shows the simulated version. Both results show good agreement.

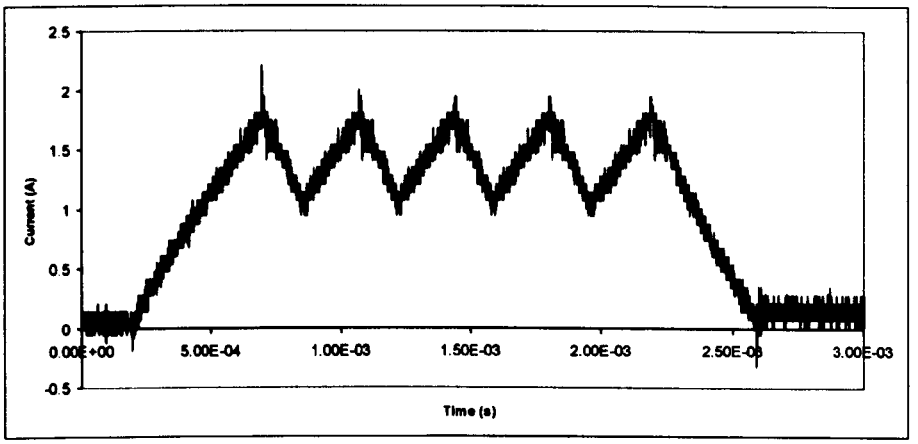


Figure 6-7– Load current

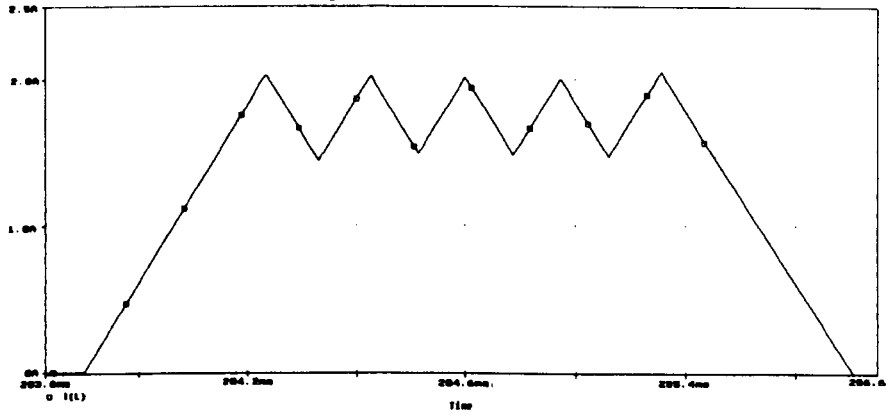


Figure 6-8 – Load current from the simulation

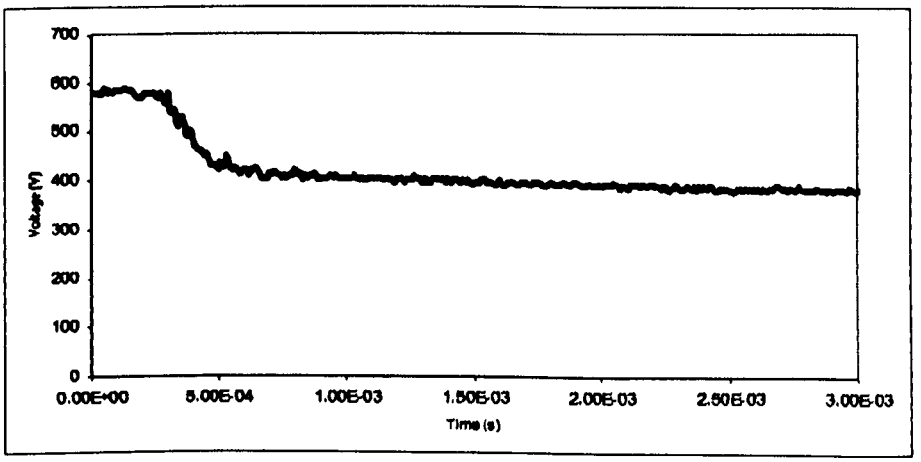


Figure 6-9 – Voltage across capacitor C1

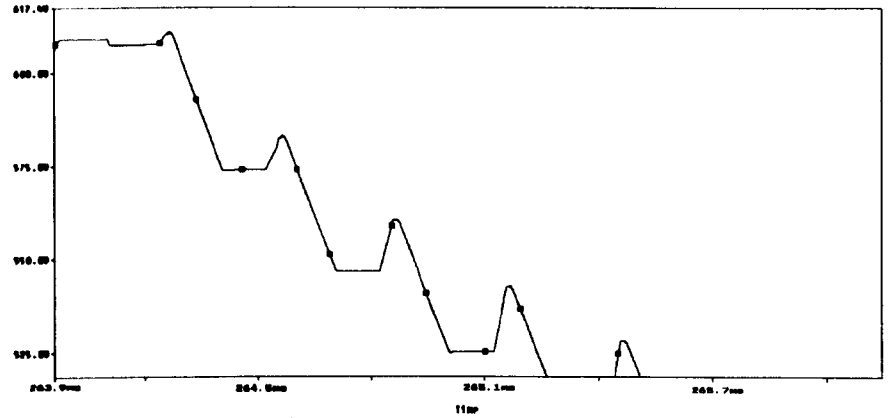


Figure 6-10- Voltage across capacitor C1 through simulations

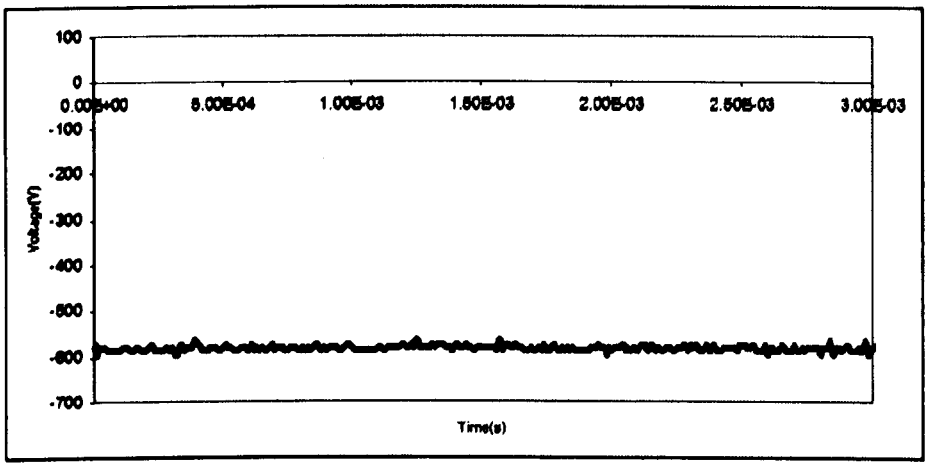


Figure 6-11 – Voltage across capacitor C2

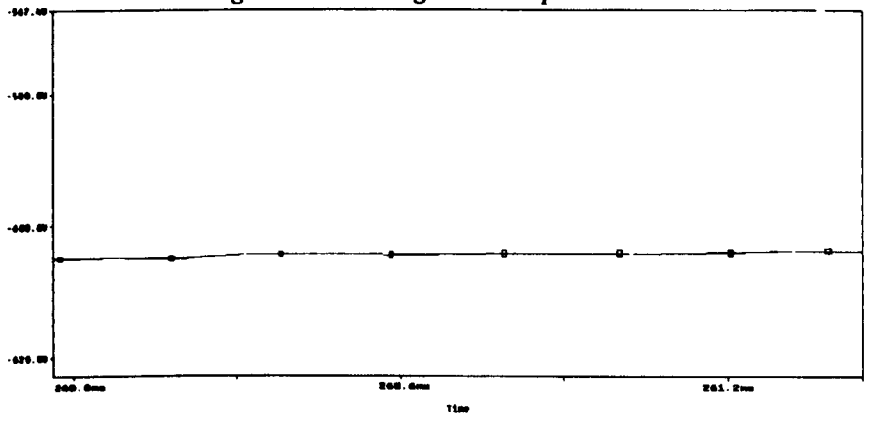


Figure 6-12- Voltage across capacitor C2 through simulations

6.7. Analysis and summary of the measured data

For the input stage, the experimental results have confirmed the operation of the voltage doubler. The results obtained are similar to the simulations. The storage capacitors are capable of supplying $2Vpk$ voltage to the converter.

The limitation in the output stage comes from the MOSFET. As have been mentioned before, it is found from the simulations that the MOSFETs need to have very high voltage and current ratings. In the power electronics market, the only available MOSFET is the 2SK2349 from SANYO. However, the current rating is not enough for use in the experimental work as the simulations have found. For the experimental set up, the average current for hysteresis threshold has to be lowered.

The switching frequency achieved from the experimental work is not as high as the simulations due to the bigger hysteresis band. However, the experimental work has verified the converter prototype.

6.8. Conclusion

In this chapter, a further analysis of the proposed converter has been conducted. The experimental analysis is done based on a few different parameters from the simulations due to some component limitations. Also, the unavailability of an SP-SRM means only a static load can be used. However, similar to what has been concluded from the simulation work, from the experimental results, it can be concluded that the converter is capable of driving the SP-SRM.

CHAPTER 7
CONCLUSIONS

The work presented in this thesis provides a comprehensive and critical assessment of a novel converter topology for controlling SP-SRMs with power ratings up to 1kW. All the major classes of SP-SRM converter topology are investigated by using a combination of theoretical and simulation work. The modes of operation of all topologies have been studied and fundamental performance limitations have been identified. The results of the study have allowed a critical assessment and comparison of the many converter topologies to be presented in a coherent form. The comparison has shown that cost reduction of SP-SRMs was always driven by reducing numbers of switches by changing the inverter topology only. Although cost can be reduced all circuits show performance reduction. The work proposed here shows a new SP-SRM topology using a new rectifier and inverter stage. The new topology reduces size, weight and cost of capacitors compared to all published SP-SRMs. Experimental results from a 1kW SP-SRM converter using the proposed topology have been presented showing good agreement with theoretical and simulation results.

7.1. Overview of SP-SRM Converter Topologies

A detailed literature survey of SP-SRM converter topologies has been presented. Distinguishing operational features have been identified and used to construct a family tree encompassing all available SP-SRM converter types. Converter topologies which have speed control and cost (large number of components) disadvantages (e.g. Hybrid Regeneration and Self-commutated Regeneration converters) have been classed as unattractive for further analysis.

All converter topologies are classed based on the management of stored energy. One branch of the converter family tree involves converters which dump all

the energy from the windings resulting in high losses and low efficiency. This group of converters is classed as 'Energy Dumping' converters.

The other main group of the converters recovers all the energy from the machine windings at the end of each commutation. This is achieved either directly to the supply or via an intermediate stage which acts as a temporary energy storage. This group of converters is classed as 'Energy Recovery' converters.

7.2. Assessment of SP-SRM Converter Topologies

Each class of the converter topologies discussed is subjected to further analysis using simulation software. The results of the simulations are used in order to assess converters for SP-SRMs in terms of efficiencies, voltage and current stresses, control complexity and cost. The Hybrid Regeneration and the Self-commutated Regeneration converters have been excluded because of their disadvantages in speed control and cost as already discussed in Chapter Three.

The assessment was conducted using a constant inductance value, and when variable inductance was used, the results were found to be similar. Although the topologies in the Energy Dumping group have simple structures they are considered as unattractive due to the amount of energy lost. The Resistor Dump converter uses a resistor to dissipate all the energy from the windings. High values of the resistor will result in high switching frequency due to the fast rate of current rise and fall. Also with high resistor values, there will be high component stress and high power ratings. The resistor will require adequate cooling due to the high energy dissipation. With the Zener Diode Dump converter, although the current decay time will be reduced, the current never reaches zero, which is undesirable. This will cause braking torque to be produced in the SRM and hence affects speed. One of the suggested solutions is the inclusion of a dump resistor to allow the current to decay down to zero at the end of each commutation. This increases the losses.

Among the three converter classes in the Energy Recovery converter group, the Magnetic (Bifilar) Regeneration converter has possibly the simplest configuration. However, this is assuming perfect coupling between the two bifilar windings. Otherwise, the leakage inductance will cause overvoltage resulting in the need to add

a snubber. The Direct Regeneration converter offers flexibility in terms of the switching angles and turn-off times. However, there is high conduction loss since there are always two switching devices in series. The Capacitor Boost converter would be advantageous compared to the Direct Regeneration converter if the capacitor voltage can be controlled to achieve rapid evacuation of the stored magnetic energy during the off going phase. More complex control scheme would not be economical compared to the other topologies.

It is found that what is still lacking is a topology which combines fast demagnetisation of the windings before subsequent commutation, control flexibility in terms of the switching angles, and minimal number of components whilst maintaining high efficiencies and better performance under most load conditions. These are the criteria which have been addressed when proposing the new converter concept.

7.3. Novel SP-SRM Converter Topology

Based on the analysis of existing converter topologies, it has been concluded that any new converter concept must fulfill a list of criteria. Consequently, a new converter design has been proposed. The new design involves a new converter topology based on rearrangement and size reduction of the circuit capacitors.

The proposed converter has two sections; an input rectifier and an output inverter. The input rectifier is connected to the AC mains feeding two storage capacitors to provide double the peak supply voltage to the output side. The output stage is made up of the storage capacitors, a freewheeling resistor and the power switches connected to the load. The new design enables functional dual voltage supply to the machine, provided via rearrangement of the capacitors. The proposed design can also be further optimised, for example, to reduce voltage ripple on the capacitors and the use of switching devices in parallel that can provide higher current carrying capabilities.

A detailed analysis and simulation of the proposed converter has been conducted. This enabled a design guideline for the proposed converter to be laid out. To further investigate the performance of the converter, a prototype has been built.

The performance of the prototype has been evaluated experimentally, and compared to the simulation results showing very good agreement.

Based on the simulation work and the experimental prototype, it is found that the converter has managed to perform as expected. The only limitation to the prototype is the controller used which does not allow for variation of the dwell angle. Therefore, the performance of the converter on variable speed and torque could not be investigated. However, the experimental work has been sufficient to confirm the suitability of the proposed converter as an SP-SRM drive.

The new SP-SRM has reduced cost which is a key driver in today's single-phase drives. The reduction in cost was achieved by reducing the capacitor cost with the new topology.

7.4. Suggestions for further work

The most advanced form of SP-SRM control involves the ability to vary the firing angles as the speed and torque vary. The performance of the machine will depend on the precise values of these angles and therefore, a more accurate shaft position feedback is necessary for maximum performance. The shaft position signal also needs to be available for use in commutation without any delay. Modified design of the controller could be implemented to achieve this advanced form of SP-SRM control. A more advanced form of microprocessor with the capability to process large amount of data at a higher speed can be used.

There also exist an economic incentive for the integration of the voltage doubler and the switches into a single power module. The application of the proposed converter for domestic appliances will then be more favourable.

The most significant advances in the novel converter topology will come from the power devices themselves. In this work, the experimental work is limited by the ratings of the switching device used. Thus, investigation into devices which could stand higher voltage and current ratings would be worthwhile.

REFERENCES

1 KRISHNAMURTHY, M., EDRINGTON, C. S., EMADI, A., ASADI, P. A.-A., P., EHSANI, M. A.-E., M., and FAHIMI, B. A.-F., B., "Making the case for applications of switched reluctance motor technology in automotive products," *IEEE Trans. Power Electronics*, 21, pp. 659-675, 2006.

2 GREG, P.:' The Rise of VSR Motors', Mechanical Engineering. 1998. p. 86-87.

3 EMADI, A., RAJASHEKARA, K., WILLIAMSON, S. S., and LUKIC, S. M. A.-L., S.M., "Topological overview of hybrid electric and fuel cell vehicular power system architectures and configurations," *Vehicular Technology, IEEE Transactions on*, 54, pp. 763-770, 2005.

4 RAHMAN, K. M., FAHIMI, B., SURESH, G., RAJARATHNAM, A. V. A.-R., A.V., and EHSANI, M. A.-E., M., "Advantages of switched reluctance motor applications to EV and HEV: design and control issues," *IEEE Trans. Ind. Appl.*, 36, pp. 111-121, 2000.

5 ALAEE, M. M., AFJEI, E., and ATAEI, S., "A New Resonant Driver for Switched Reluctance Motor", *Electrical Engineering, 2007. ICEE '07. International Conference on Electrical Engineering, 2007. ICEE '07. International Conference on VO -*, 2007, pp. 1-3

6 YANG, A. Y., ZHANG, B. Y., and WANG, C. S., "Four-Quadrant Control of DSP-based Switched Reluctance Drives for EV", *Industrial Electronics and Applications, 2007. ICIEA 2007. 2nd IEEE Conference on Industrial Electronics and Applications, 2007. ICIEA 2007. 2nd IEEE Conference on VO -*, 2007, pp. 2162-2167

7 CAI, W., PILLAY, P., TANG, Z., and OMEKANDA, A. M. A.-O., A.M., "Low-vibration design of switched reluctance motors for automotive applications using modal analysis," *IEEE Trans. Ind. Appl.*, 39, pp. 971-977, 2003.

8 POLLOCK, C., and WU, C.-Y., "Acoustic noise cancellation techniques for switched reluctance drives," *IEEE Trans. Ind. Appl.*, 33, pp. 477-484, 1997.

9 RADUN, A. V., "High-power density switched reluctance motor drive for aerospace applications," *IEEE Trans. Ind. Appl.*, 28, pp. 113-119, 1992.

10 NAAYAGI, R. T., and KAMARAJ, V., "Shape optimization of switched reluctance machine for aerospace applications", *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEEIndustrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE VO -*, 2005, pp. 4 pp.

11 FORREST, S. J., WANG, J., JEWELL, G. W., JOHNSON, C. M. A.-J., C.M., and CALVERLEY, S. D. A.-C., S.D., "Analysis of an AC fed direct converter for a switched reluctance machine in aerospace applications", *Power Electronics and Motion Control Conference, 2006. IPEMC '06. CES/IEEE 5th InternationalPower Electronics and Motion Control Conference, 2006. IPEMC '06. CES/IEEE 5th International VO - 2*, 2006, pp. 1-6

12 AYAZ, M., and YILDIZ, A. B., "Control of Switched Reluctance Motor Containing a Linear Model", *Control and Automation, 2006. MED '06. 14th Mediterranean Conference onControl and Automation, 2006. MED '06. 14th Mediterranean Conference on VO* -, 2006, pp. 1-6

13 QIONG-ZHONG, MO, C. Y.-F., and MENG, G., "Dymola-based modeling of SRD in aircraft electrical system," *IEEE Trans. Aerospace & Electronic Syst.*, 42, pp. 220-227, 2006.

14 INDERKA, R. B., MENNE, M., and DE DONCKER, R. W. A. A., "Control of switched reluctance drives for electric vehicle applications," *IEEE Trans. Ind. Electronics*, 49, pp. 48-53, 2002.

15 MILLER, T., *Electronic Control of Switched Reluctance Machines*, first, Reed Educational and Professional Publishing Ltd, 2001.

16 GALLEGOS-LOPEZ, G., and RAJASHEKARA, K., "Peak PWM current control of switched reluctance and AC machines", *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the*, 2002, pp. 1212-1218 vol.2

17 'Fairchild Semiconductor Introduces the Industry's First Smart Power Module (SPM™) for Switched Reluctance Motors', Fairchild Semiconductor (NYSE: FCS) Press Room, 2005. [Online].Available: http://www.fairchildsemi.com/news/2005/0502/fcas50sn60.htm [Accessed] March 18, 2007

18 YO-CHAN, S., KI-YOUNG, J., and BUM-SEOK, S.:' Powering SR Motors', Power Electronics Europe. 2005. p. 42-47.

19 LOVATT, H. C., MCCLELLAND, M. L., and STEPHENSON, J. M., "Comparative performance of singly salient reluctance, switched reluctance, and induction motors", *Electrical Machines and Drives, 1997 Eighth International Conference on (Conf. Publ. No. 444)*, 1997, pp. 361-365

20 YUEN-CHUNG, K., YONG-HO, Y., BYOUNG-KUK, L., JIN, H., and CHUNG-YUEN, W., "A New Cost Effective SRM Drive using Commercial 6-Switch IGBT Modules", *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-7

21 KRISHNAN, R., S-Y, P., and HA, K., "Theory and operation of a four quadrant switched reluctance motor drive with a single controllable switch- the lowest cost four quadrant brushless motor drive", *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, 2004, pp. 1610-1617 vol.3

22 KRISHNAN, R., and MATERU, P. N., "Analysis and design of a low-cost converter for switched reluctance motor drives," *IEEE Trans. Ind. Appl.*, 29, pp. 320-327, 1993.

23 LE-HUY, H., VIAROUGE, P., and FRANCOEUR, B., "A novel unipolar converter for switched reluctance motor," *Power Electronics Specialists Conference, 1989. PESC '89 Record., 20th Annual IEEE*, pp. 3-10 vol.1, 1989.

24 BARNES, M., and POLLOCK, C., "Power electronic converters for switched reluctance drives," *IEEE Trans. Power Electronics*, 13, pp. 1100-1111, 1998.

25 GORDON, B. M., RAJAMANI, H. S., and MCMAHON, R. A., "An investigation of bifilar wound three-phase induction motor drives operating with only low side switches", *Power Electronics and Variable Speed Drives, 1996. Sixth International Conference on (Conf. Publ. No. 429)*, 1996, pp. 413-418

26 STALEY, A. M., and KRISHNAN, R., "Single controllable switch power converter for SRM drive systems", *Industrial Electronics Society, 2005. IECON 2005. 32nd Annual Conference of IEEE*, 2005, pp. 6 p.p.

27 VUKOSAVIC, S., and STEFANOVIC, V. R., "SRM inverter topologies: a comparative evaluation," *IEEE Trans. Ind. Appl.*, 27, pp. 1034-1047, 1991.

28 HA, K., LEE, C., KIM, J., KRISHNAN, R., and OH, S.-G., "Design and Development of Low-Cost and High-Efficiency Variable-Speed Drive System With Switched Reluctance Motor," *IEEE Trans. Ind. Appl.*, 43, pp. 703-713, 2007.

29 COCKROFT, J. D., and WALTON, E. T. S., "Experiments with High Velocity Positive Ions. (I) Further Developments in the Method of Obtaining High Velocity Positive Ions," *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character*, Vol. 136, pp. pp. 619-630, 1932.

30 IET. 'Archives - Michael Faraday', The Archives of the Institution of Engineering and Technology. [Online].Available: http://www.iee.org/TheIEE/Research/Archives/Histories&Biographies/Faraday.cfm [Accessed] 20 March 2007

31 MILLER, T., *Switched Reluctance Motors and Their Control*, Magna Physics Publishing, 1993.

32 NASAR, S. A., "DC Switched Reluctance Motors," *Proceedings of the Institution of Electrical Engineers (IEE)*, 116, pp. 1048-1049, 1969.

33 General Electric Company, "Compatible Permanent Magnet or Reluctance Brushless Motors and Controlled Switch Circuits", United States Patent Patents, 'Patent No. 3,678,352, 1970

34 General Electric Company, "Compatible Brushless Reluctance Motors and Controlled Switch Circuits", United States Patent Patents, 'Patent No. 3,679,953, 1971

35 LAWRENSON, P. J., STEPHENSON, J. M., FULTON, N. N., BLENKINSOP, P. T., and CORDA, J., "Variable speed switched reluctance motors.," *IEE Proceedings B (Electric Power Applications)*, 127, pp. 253-265, 1980.

36 BRIVIT. B. S. DATABASE, 'Number of Published Switched Reluctance Papers and Theses', Fleadh Electronics Limited, Leeds, UK. [Online].Available: http://ldn.fleadh.co.uk/brivit/database/mainframe.asp [Accessed] 28 April 2005

37 FIEDLER, J. O., KASPER, K. A., and DE DONCKER, R. W., "Acoustic noise in switched reluctance drives: an aerodynamic problem?" *Electric Machines and Drives, 2005 IEEE International Conference on*, 2005, pp. 1275-1280

38 KRISHNAN, R., and MATERU, P. N., "Design of a single-switch-per-phase converter for switched reluctance motor drives," *IEEE Trans. Ind. Electronics*, 37, pp. 469-476, 1990.

39 KRISHNAN, R., PARK, S.-Y., and HA, K., "Theory and operation of a four-quadrant switched reluctance motor drive with a single controllable switch-the lowest cost four-quadrant brushless motor drive," *IEEE Trans. Ind. Appl.*, Volume 41, pp. Page(s):1047 - 1055, 2005.

40 SRINIVAS, P., and PRASAD, P. V. N., "Voltage control and hysteresis current control of a 8/6 switched reluctance motor", *Electrical Machines and Systems, 2007. ICEMS. International Conference on*, 2007, pp. 1557-1562

41 HWU, K. I., and LIAW, C. M., "DC-link voltage boosting and switching control for switched reluctance motor drives," *Electric Power Applications, IEE Proceedings -*, 147, pp. 337-344, 2000.

42 HAVA, A. M., BLASKO, V., and LIPO, T. A., "A modified C-dump converter for variable-reluctance machines," *IEEE Trans. Ind. Appl.*, 28, pp. 1017-1022, 1992.

43 EHSANI, M., BASS, J. T., MILLER, T. J. E., and STEIGERWALD, R. L., "Development of a unipolar converter for switched reluctance motor drives", *IEEE Transactions for Ind. Applications*, 1987, pp. 545-553

44 MIR, S., HUSAIN, I., and ELBULUK, M. E., "Energy-efficient C-dump converters for switched reluctance motors," *IEEE Trans. Power Electronics*, Volume 12, pp. Page(s):912 - 921, 1997.

45 KING-JET, T., SHUYU, C., and JIJIU, W., "A new hybrid C-dump and buck-fronted converter for switched reluctance motors," *IEEE Trans. Ind. Electronics*, 47, pp. 1228-1236, 2000.

46 HUIJUN, W., DONG-HEE, L., and JIN-WOO, A., "A Modified Multi-Level Converter for Low Cost High Speed SR Drive", *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 1790-1795

47 DONG-HEE, L., HUIJUN, W., and JIN-WOO, A., "An advanced multi-level converter for four-phase SRM drive", *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 2050-2056

48 DAHMANE, A., MEEBODY, F., and SARGOS, F.-M., "A novel boost capacitor circuit to enhance the performance of the switched reluctance motor", *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, 2001, pp. 844-849 vol.2

49 "Regenerative unipolar converter for switched reluctance motors using one main switching device per phase", US patent Patents, 'Patent No. 4,684,867, 1978

50 BARNES, M., and POLLOCK, C., "Selecting power electronic converters for single phase switched reluctance motors," *Power Electronics and Variable Speed Drives, 1998. Seventh International Conference on (IEE Conf. Publ. No. 456)*, pp. 527-531, 1998.

51 WOONG, L. E., "Present and result of single phase switched reluctance motor", *Electrical Machines and Systems, 2003. ICEMS 2003. Sixth International Conference on*, 2003, pp. VII-XII vol.1

52 LIM, J.-Y., KIM, H.-S., OH, J.-Y., CHEONG, D.-H., and KIM, J.-C., "A performance of single phase switched reluctance motor having both radial and axial air gap," *Industrial Electronics Society, 1998. IECON '98. Proceedings of the 24th Annual Conference of the IEEE*, 2, pp. 905-910 vol.2, 1998.

53 Ford Motor Company (Dearborn, MI), "Variable Reluctance Motor Pump", United States Patent Patents, 'Patent No. 3932069, 1976

54 Switched Reluctance Drives, Ltd. (GB), "Apparatus and method for starting a single-phase variable reluctance motor", United States Patents, 'Patent No. 5808389, 1998

55 Switched Reluctance Drives, Ltd. (Harrogate, GB), "Single-phase variable reluctance motor having permanent magnets embedded within a phase winding", United States Patents, 'Patent No. 5,650,682, 1997

56 JENKINSON, G. C., and STEPHENSON, J. M., "Starting of a single-phase switched reluctance motor," *Electrical Machines and Drives, 1999. Ninth International Conference on (Conf. Publ. No. 468)*, pp. 391-395, 1999.

57 Assignee: Switched Reluctance Drives Limited (Harrogate, GB), "Apparatus and method for starting a single-phase variable reluctance motor", United States Patent Patents, 'Patent No. 5,753,984, 1998

58 Emerson Electric Co. (St. Louis, MO), "Shifted pole single phase variable reluctance motor", United States Patents, 'Patent No. 5,294,856, 1994

59 LEE, J.-H., LEE, E.-W., and KIM, J.-H., "Design of the single phase SRM for the blower considering self-starting", *Electrical Machines and Systems, 2005. ICEMS 2005. Proceedings of the Eighth International Conference on*, 2005, pp. 667-670 Vol. 1

60 KRISHNAN, R., STALEY, A. M., and SITAPATI, K., "A novel single-phase switched reluctance motor drive system," *Industrial Electronics Society, 2001. IECON '01. The 27th Annual Conference of the IEEE*, 2, pp. 1488-1493 vol.2, 2001.

61 HIGUCHI, T., FIEDLER, J. O., and DE DONCKER, R. W., "On the design of a single-phase switched reluctance motor," *Electric Machines and Drives Conference, 2003. IEMDC'03. IEEE International*, 1, pp. 561-567 vol.1, 2003.

62 FLETCHER, J. E., HELAL, A., and WILLIAMS, B. W., "Starting the Single-Phase Switched Reluctance Motor Using Rotor Shorting Rings," *Energy Conversion, IEEE Transaction on*, 21, pp. 848-854, 2006.

63 KRISHNAMURTHY, M., EDRINGTON, C. S., and FAHIMI, B., "Prediction of rotor position at standstill and rotating shaft conditions in switched reluctance machines," *IEEE Trans. Power Electronics*, 21, pp. 225-233, 2006.

64 LIU, T.-H., and CHEN, C.-G., "Implementation of sensorless techniques for switched reluctance drive systems", *Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE*, 2004, pp. 1867-1872 Vol. 2

65 HUSAIN, I., and EHSANI, M., "Rotor position sensing in switched reluctance motor drives by measuring mutually induced voltages," *IEEE Trans. Ind. Appl.*, 30, pp. 665-672, 1994.

66 ERTUGRUL, N., and CHEOK, A. D., "Indirect angle estimation in switched reluctance motor drive using fuzzy logic based motor model," *IEEE Trans. Power Electronics*, 15, pp. 1029-1044, 2000.

67 KOSAKA, T., and MATSUI, N., "Position sensorless control of general purpose inverter-fed fully-pitched winding reluctance motor drives", *Industry Applications Conference, 2000. Conference Record of the 2000 IEEE*, 2000, pp. 1745-1750 vol.3

68 BECERRA, R. C., EHSANI, M., and MILLER, T. J. E., "Commutation of SR motors," *IEEE Trans. Power Electronics*, 8, pp. 257-263, 1993.

69 ACARNLEY, P. P., HILL, R. J., and HOOPER, C. W., "Detection of Rotor Position in Stepping and Switched Motors by Monitoring of Current Waveforms," *IEEE Trans. Ind. Electron.*, IE-32, pp. 215-222, 1985.

70 GALLEGOS-LOPEZ, G., KJAER, P. C., and MILLER, T. J. E., "A new sensorless method for switched reluctance motor drives," *IEEE Trans. Ind. Appl.*, 34, pp. 832-840, 1998.

71 LUMSDAINE, A., and LANG, J. H., "State observers for variable-reluctance motors," *IEEE Trans. Ind. Electronics*, 37, pp. 133-142, 1990.

72 XU, L., and BU, J., "Position transducerless control of a switched reluctance motor using minimum magnetizing input", *Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE*, 1997, pp. 533-539 vol.1

73 MESE, E., and TORREY, D. A., "An approach for sensorless position estimation for switched reluctance motors using artifical neural networks," *IEEE Trans. Power Electronics*, 17, pp. 66-75, 2002.

74 REAY, D. S., and WILLIAMS, B. W., "Sensorless position detection using neural networks for the control of switched reluctance motors", *Control Applications, 1999. Proceedings of the 1999 IEEE International Conference on*, 1999, pp. 1073-1077 vol. 2

75 GRBO, Z., VOKOSAVIC, S., and LEVI, E., "A novel power inverter for switched reluctance motor drives," *Facta Universitatis (Nis) - Series: Elec. Energ.*, 18, pp. 453-465, 2005.

76 BOSE, B. K., "Energy, environment, and advances in power electronics," *IEEE Trans. Power Electronics*, 15, pp. 688-701, 2000.

77 KRISHNAN, R., and MATERU, P., "Analysis and design of a low cost converter for switched reluctance motor drives," *Industry Applications Society Annual Meeting, 1989., Conference Record of the 1989 IEEE*, pp. 561-567 vol.1, 1989.

78 LE-HUY, H., VIAROUGE, P., and FRANCOEUR, B., "Unipolar converters for switched reluctance motors," *Industry Applications Society Annual Meeting, 1989., Conference Record of the 1989 IEEE*, pp. 551-560 vol.1, 1989.

79 DAVIS, R. M., RAY, W. F., and BLAKE, R. J., "Inverter drive for switched reluctance motor: circuits and component ratings", *Proc. Ins. Elec. Eng.*, 1981, pp. pp. 126-136

80 THONG, W. K., and POLLOCK, C., "A novel low-cost RCD snubber for bifilar-wound motors," *IEEE Trans. Ind. Appl.*, 38, pp. 688-694, 2002.

81 THONG, W. K., and POLLOCK, C., "A novel low cost RC snubber", *Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE*, 2001, pp. 1743-1748 vol.3

82 REINERT, J., and SCHRODER, S., "Power-factor correction for switched reluctance drives," *IEEE Trans. Ind. Electronics*, 49, pp. 54-57, 2002.

83 KIM, Y.-H., LIM, S.-B., and LEE, J., "Optimal Design of Single Phase Switched Reluctance Motor Considering Driving Converter", *Electromagnetic Field Computation, 2006 12th Biennial IEEE Conference on*, 2006, pp. Page(s):413 - 413

84 Emerson Electric Co. (St. Louis, MO), "Power Converter for Switched Reluctance Motor", US Patents, 'Patent No. 5115181, 1992

85 "Control circuit and system for a switched reluctance machine a d method of operating", US Patents, 'Patent No. 5,764,019, 1998

86 CHAN, S., and BOLTON, H. R., "Performance enhancement of single-phase switched-reluctance motor by DC link voltage boosting," *IEEE Proc. Electr. Power Appl.*, 140, pp. 316-322, 1993.

87 LEWIS, J. D., BOLTON, H. R., and PHILLIPS, N. W., "Performance Enhancement of single and two phase SR drives using a capacitor boost circuit", *EUropean Power ELectronics and Applications Conf. Recs.*, 1995, pp. 229-232

88 BARNES, M., and POLLOCK, C., "Power converter for single phase switched reluctance motors," *IEEE Power Electron Lett.*, 31, pp. 2137-2138, 1995.

89 Ford Motor Company Limited, "Reluctance motor", UK Patents, 'Patent No. 1,295,103, 1972

90 AN, Y.-J., HONG, S.-I., JOE, C.-J., CHOO, Y.-B., and NOH, C.-J., "Performance of switched reluctance motor driven by novel C-dump inverter", TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering.1993 IEEE Region 10 Conference on, 1993, pp. 585-588 vol.5

91 YOON, Y.-H., SONG, S.-H., LEE, T.-W., WON, C.-Y., and KIM, Y.-R., "High performance switched reluctance motor drive for automobiles using C-dump converters", *Industrial Electronics, 2004 IEEE International Symposium on*, 2004, pp. 969-974 vol. 2

92 RIM, G.-H., KIM, W.-H., KIM, E.-S., and LEE, K.-C., "A choppingless converter for switched reluctance motor with unity power factor and sinusoidal input current", *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE*, 1994, pp. 500-507 vol.1

93 CHAN, C. C., "Single-Phase Switched Reluctance Motors," *IEE Proc. -B Electr. Power Appl.*, 134, pp. 53-56, 1987.

94 KRISHNAN, R., ARUMUGAN, R., and LINDSAY, J. F., "Design procedure for switched-reluctance motors," *IEEE Trans. Ind. Appl.*, 24, pp. 456-461, 1988.

95 RAJARATHNAM, A. V., RAHMAN, K. M., and EHSANI, M., "Improvement of hysteresis control in switched reluctance motor drives", *Electric Machines and Drives, 1999. International Conference IEMD '99*, 1999, pp. 537-539

96 POLLOCK, H., POLLOCK, C., WALTER, R. T., and GORTI, B. V., "Low cost, high power density, flux switching machines and drives for power tools", *Industry Applications Conference, 2003. 38th IAS Annual Meeting. Conference Record of the*, 2003, pp. 1451-1457 vol.3

97 CHANCHAROENSOOK, P., and RAHMAN, M. F., "Modification of a switching strategy for asymmetric half-bridge converters for switched reluctance motor drives", *Power Electronics and Drive Systems, 2003. PEDS 2003. The Fifth International Conference on*, 2003, pp. 932-937 Vol.2

98 MACMINN, S. R., and JONES, W. D., "A very high speed switched-reluctance starter-generator for aircraft engine applications", *Aerospace and Electronics Conference, 1989. NAECON 1989., Proceedings of the IEEE 1989 National*, 1989, pp. 1758-1764 vol.4

99 "Current Chopping Strategy for Switched Reluctance Machine", United States Patents, 'Patent No. 4,933,621, 1990

100 TSENG, K.-J., CAO, S., and WANG, J., "A new hybrid C-dump and buck-fronted converter for switched reluctance motors," *IEEE Trans. Ind. Electronics*, 47, pp. 1228-1236, 2000.

101 BORG, I. S.: 'Experiment 19 - BlazeLabs Resonant Multipliers', [Online].Available: http://www.blazelabs.com/e-exp19.asp [Accessed] 23/06/05

102 IQBAL, S., SINGH, G. K., and BESAR, R., "A Dual-Mode Input Voltage Modulation Control Scheme for Voltage Multiplier Based X-Ray Power Supply," *IEEE Trans. Power Electron.*, 23, pp. 1003-1008, 2008.

103 HWANG, F., SHEN, Y., and JAYARAM, S. H., "Low-Ripple Compact High-Voltage DC Power Supply," *IEEE Trans. Ind. Appl.*, 42, pp. 1139-1145, 2006.

104 SHUTE, D. W., "A Hybrid Cockroft Walton Multi-Dynode Photomultiplier Supply for Space Applications," *IEEE Trans. Nucl. Sci.*, 17, pp. 130-137, 1970.

105 MALESANI, L., and PIOVAN, R., "Theoretical performance of the capacitor-diode voltage multiplier fed by a current source," *IEEE Trans. Power Electron.*, 8, pp. 147-155, 1993.

106 RASHID, M. H., *Power Electronics Handbook*, Academic Press, 2001, pp. 227.

107 KJAER, P. C., NIELSEN, P., ANDERSEN, L., and BLAABJERG, F., "A new energy optimizing control strategy for switched reluctance motors," *IEEE Trans. Ind. Appl.*, 31, pp. 1088-1095, 1995.

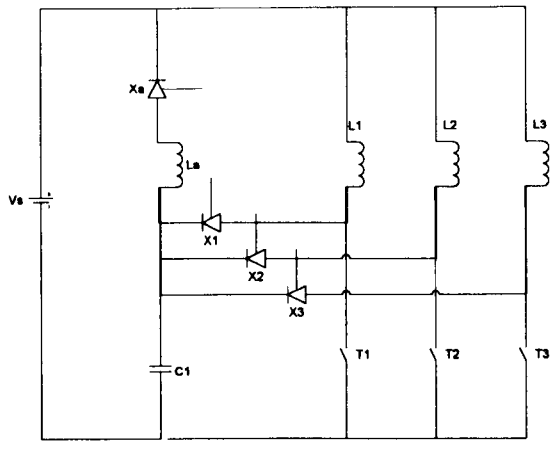
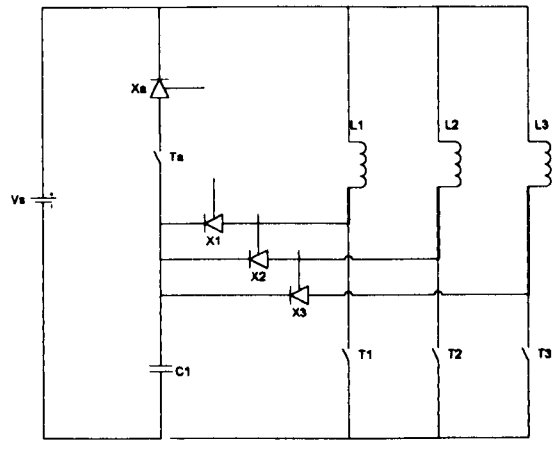
108 BECK, J. M.: 'Using rectifiers in Voltage Multiplier Circuits', Vishay Semiconductors Application Notes No. 88842. [Online].Available: http://www.vishay.com/docs/88842/voltage_.pdf [Accessed] 11 April 2006

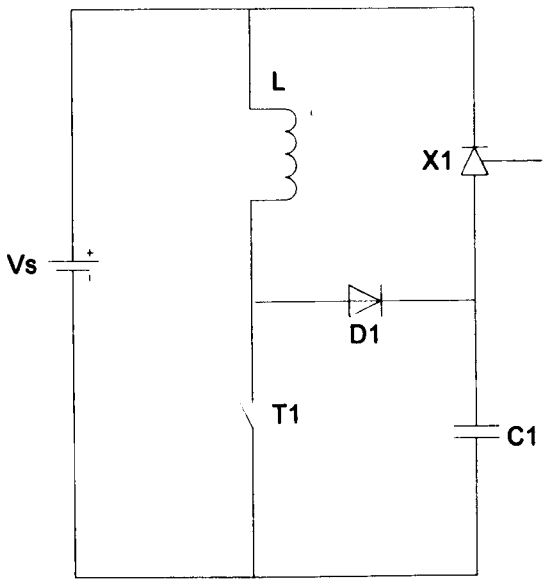
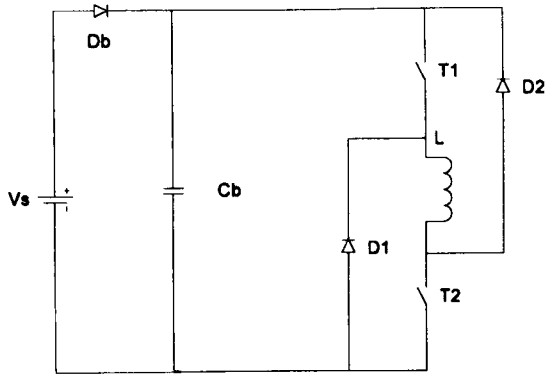
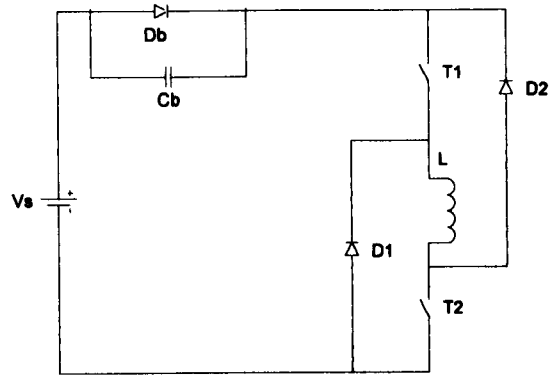
109 YAN, W., and DAWSON, F. P., "DC ignition circuits for a high pressure vortex-water-wall argon arc lamp", *Industry Applications Conference, 1996. Thirty-First IAS Annual Meeting, IAS '96., Conference Record of the 1996 IEEE*, 1996, pp. 2211-2218 vol.4

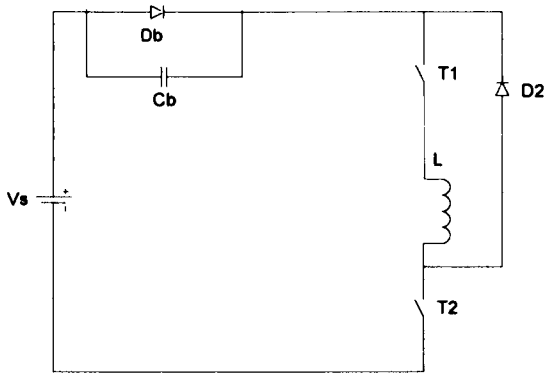
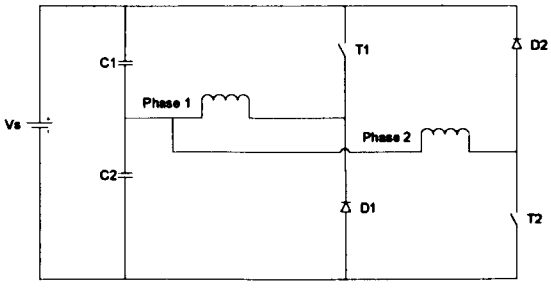
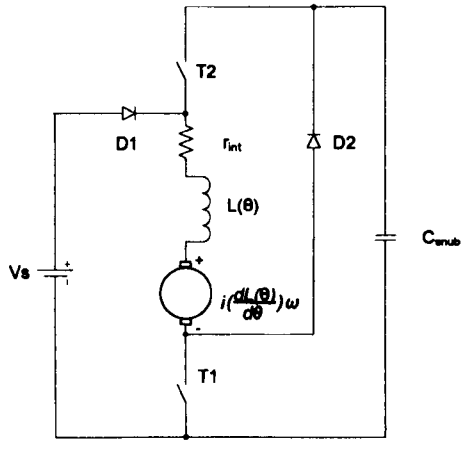
110 CONSOLI, A., TESTA, A., AIELLO, N., GENNARO, F., and LO PRESTI, M., "Unipolar converter for switched reluctance motor drives with power factor improvement," *Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE*, 2, pp. 1103-1108 vol.2, 2001.

APPENDIX A
CAPACITOR BOOST CIRCUITS

This appendix shows the circuit representation the Capacitor Boost converters based on literature search in Chapter 3.

Reference number	Circuit description	Circuit representation
[49]	**Early design of C-dump converter for polyphase machine (Vs representing DC link)**	
[27,84]	**Variation of [49] with DC link eliminated (Vs representing the rectifier output)**	

[85]	**Capacitor controlled by an SCR, without DC link (Vs representing the single phase output)**	
[86]	**Modification of the direct regeneration by adding an auxiliary capacitor parallel to the DC link (Vs representing the DC link)**	
[87]	**As in [86] but with the auxiliary capacitor in series with the DC link (Vs representing the DC link)**	

[88]	**Similar topology with one less diode (Vs representing the DC link)**	
[89]	**Split DC link topology (Vs representing the single phase output)**	
[42,84]	**Boost capacitor switched on and off using additional switch and diode (Vs representing the DC link)**	

APPENDIX B
ELECTRICAL AND ELECTRONICS CIRCUIT

This appendix describes in detail the experimental implementation of the proposed power converter. The experimental setup for the novel converter can be divided into individual components that will be described in detail in separate sections. The circuit diagrams given in this appendix shows only the functional aspect of the circuit, and do not reflect the actual design of the circuit board.

B.1 Power converter

The complete power converter is contained in a grounded metal enclosure of the size (300mm x 500mm x 450mm). The metal enclosure also acts as a shield to reduce electromagnetic emissions and interference to the environment. The converter is earthed in one point only to reduce noise from the power supply lines. All metal objects inside the converter are also earthed to eliminate floating potentials. Power is provided from single phase mains supply. The auxiliary power circuit is fed from an isolated 30V DC supply.

B.1.1 Input side and input protection

The input side of the converter includes an input protection circuit, the voltage doubler circuit and the capacitor discharge circuit. A general circuit diagram of the input side is given in Figure B- 1.

The autotransformer is capable to provide AC voltages up to the mains voltage. This is to enable the converter to be tested at lower AC voltages. There is a circuit breaker across the main line before the converter circuit. This circuit breaker acts as a fuse which trips and disconnects the converter and mains supply when there is overcurrent. The circuit breaker used is by Moeller rated at 10A, 230V (medium speed). The reason why a circuit breaker is used rather than a ceramic fuse is so that

the fuse is resettable. To disconnect the input side of the converter to the mains supply, a contactor is used as the main switch and emergency fault switch. In case the contactor control detects a fault, the contactor disconnects and thus removes the input power to the converter. The contactor coil is energised by 230V AC, and controlled by a signal from the controller. The contactor has two normally open switches, which connect to the converter and one normally close switch, which connects to the capacitor dump mechanism.

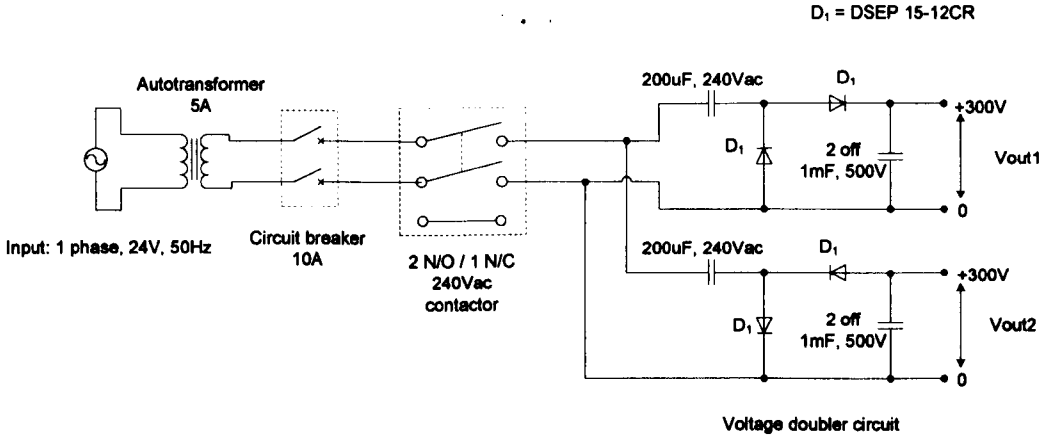


Figure B- 1– Input side of the power converter

The control to the contactor is provided from the controller board. The circuit is built onto a relay card and is shown in Figure B- 2. It uses a Dual-In-Line (DIL) Reed relay package. By pressing the start button, the relay coil is energised. However, this is only possible when there is an enable signal from the controller. Once the relay coil is energised, it is maintained that way unless it receives a disable signal from the controller or the stop button is pressed which disconnects the supply to the coil. During the time when the relay coil is energised, the relay switch will complete the mains contactor coil circuit, thus energising it. The mains contactor then operates to connect the supply to the converter. The converter start and stop button are supplied by an external regulated 12V DC supply.

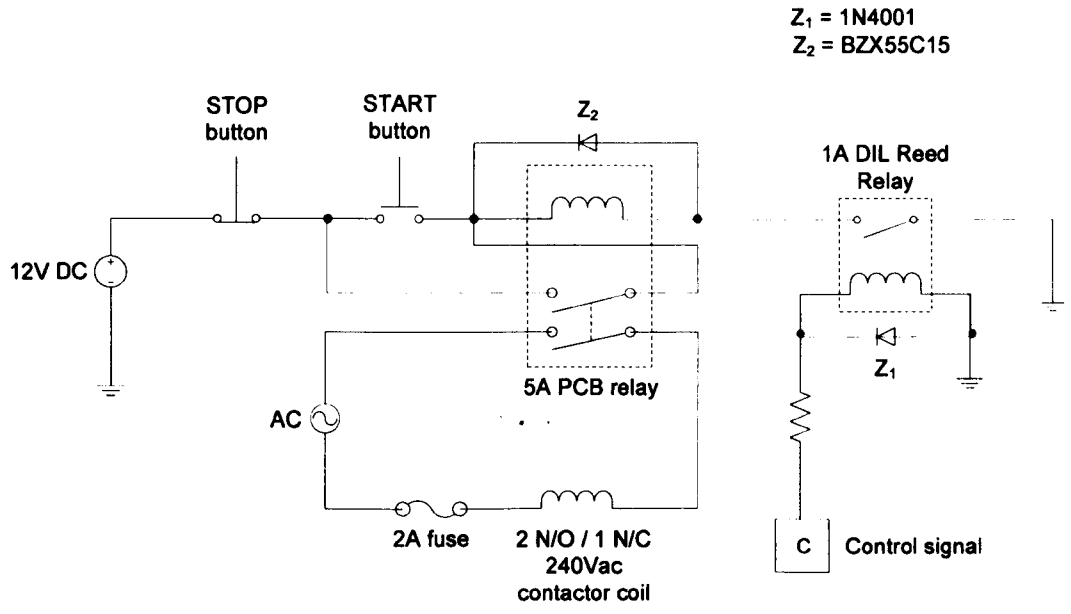


Figure B- 2 – Control circuit to the contactor

Diodes used for the voltage doubler circuit are from IXYS model DSEP 15-12CR, rated at 15A/ 1200V. Both capacitor C1 and C3 have capacitances of 200μF, rated at 230V AC. However, capacitor C2 and C4 both are made up of two similar EPCOS electrolytic capacitors in series. This is to achieve a higher voltage rating at the capacitance value required. The total capacitance for C3 and C4 respectively, is 1mF, rated at 1000V DC. The capacitors have a ripple rating of 6.7A at 100Hz.

When the converter system is switched off, there are safety concerns due to the energy stored in the capacitors. Therefore, to comply with safety requirements, resistors are connected in parallel to the capacitors. The discharge mechanism is connected to the mains contactor, and is automatically connected when the supply is disconnected. For C1 and C3, the resistor value is 10kΩ contributing to a discharge time of 2s. The resistors are rated at 150W. For C2 and C4 (each comprises of two capacitors in series), the resistor value is 10kΩ as well contributing to a discharge time of 10s. The resistors are rated at 14W. The discharge circuit is shown in Figure B- 3.

For capacitors C2 and C4, the discharge resistors are not connected to the contactor, but are always in the circuit. This is because the same resistors are used for ensuring the equal charge distribution across the two capacitors that are in series. The

values are made big so that no large current is drawn and thus reducing the amount of voltage available for the load.

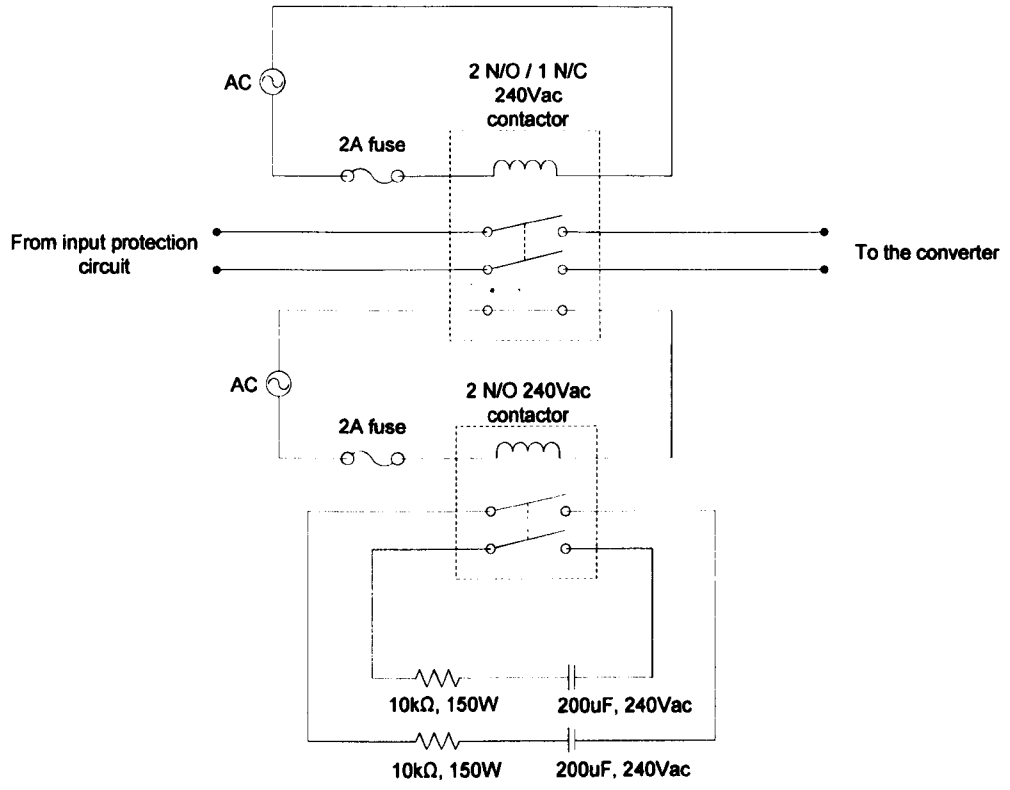


Figure B- 3 – Capacitor discharge circuit

All capacitors, diodes and resistors are mounted on to the same PCB with the MOSFETs to ensure proper connection and to eliminate noise due to long lines.

B.1.2 Voltage measurement circuit

It is vital to know the value of voltages in particularly capacitors C2 and C4 to enable the converter to start switching. Therefore, a reliable method of measuring the voltage is needed. Two voltage measurement cards are used to measure the voltages in C2 and C4 respectively.

The voltage card consists primarily of an LEM voltage transducer. The voltage transducer LV-25P is rated to measure up to 1000V requiring only 10mA. The transducer provides the isolation between the high voltage and the low voltage measured output. The supply to the voltage measurement card is obtained directly

from the controller. The measured output is fed directly into the control system. The circuit configuration of the voltage card is shown in Figure B- 4.

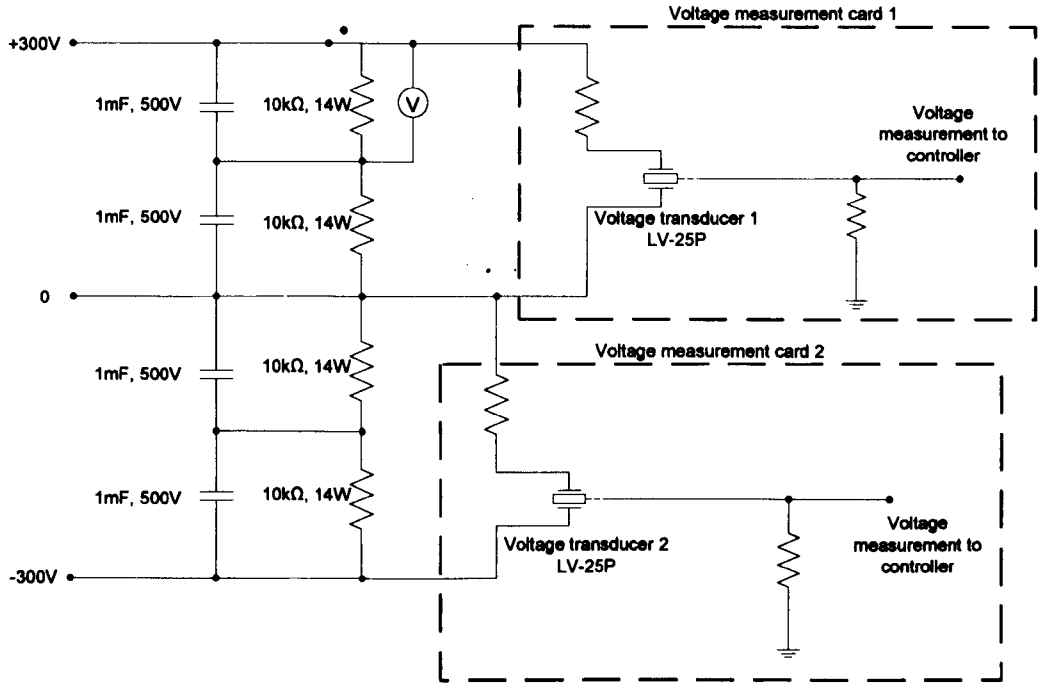


Figure B- 4 – Voltage measurement circuit

The control system will read this output value, and once the capacitors are fully charged, switching can commence. LED indicators on the controller enclosure will turn on once the storage capacitors are full, and a manual switch needs to be pressed before switching starts. At the same time, throughout the converter operation, the control system also checks whether the voltages are have reached overvoltage or undervoltage thresholds. Once this happens, a fault signal is generated, and the switching is disabled. The controller sends a fault signal to the DIL Reed relay to trip the mains contactor, and disconnects the mains supply to the converter. In this case, the appropriate LED will turn on indicating the fault.

B.1.3 Phase current measurement

The phase output current is measured using a Hall effect transducer, LTS-6-NP. The current measurement is set to measure a peak current rating of up to 8A, bandwidth of 150 kHz DC current and provides isolation from the power circuit. The current transducer is supplied by the controller. R_m is the measurement resistor which enables the output voltage to be measured. The measured value is then transferred to

the control system via a BNC cable. The use of a BNC cable ensures that the signal is protected from any noise by the shielded cable.

Once at the control board, the signal goes through an active low pass filter. The active filter uses OP470-GP, an amplifier with very low input offset current, voltages for precision operation and low drift, sufficient gain bandwidth for the application, and reduced errors due to ground noise and power supply fluctuations. This is very important because an accurate measured current signal is critical to the operation of the converter. The filter limits any transmitted noise primarily from the power lines. The signal is then transferred directly to the analog-to-digital port of the DSC. All resistors involved have a precision of 1% to allow accurate current measurements. The current measurement circuit is shown in Figure B- 5.

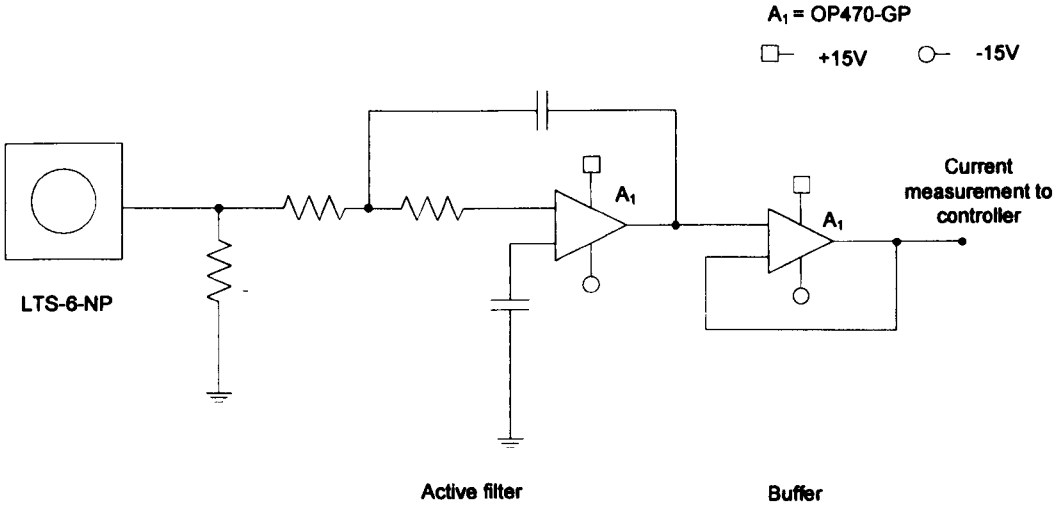


Figure B- 5– current measurement circuit

B.1.4 Overcurrent, overvoltage and undervoltage protection

Overcurrent, overvoltage and undervoltage protection is monitored and controlled by the DSC. In the control program, the overcurrent is set at 8A. This is the current measured through the load as measured by the current measurement card. The overvoltage and undervoltage protection are set at 800V and 300V respectively. These are measured as the voltages across the storage capacitors.

Once any fault happens, a fault signal is generated, and any switching will be stopped. The whole system then trips. The faults are indicated by appropriate LEDs at the front panel of the controller enclosure.

B.1.5 Overtemperature measurement

Temperature measurement is obtained through a precision centigrade temperature sensor, LM35. The output sensitivity is 1mV per degree Celsius. The measured voltage is fed into the control system, and is monitored so that it does not exceed 100°C. Once that happen, an overtemperature fault signal is generated, and result in switching to be halted, and the system to trip. This will be indicated by an overtemperature LED at the front panel. The temperature sensor is attached to the heatsink at the vicinity of the MOSFETs.

B.1.6 Output side

The output side consists of two MOSFETs, a freewheeling resistor, and the load. The MOSFET used is from SANYO, model 2SK2349. The MOSFET is rated at 1500V (drain-to-source) with maximum drain current of 10A. This is a high reliability MOSFET, with a low on resistance, and is chosen for use due to the high voltage requirement of the converter.

The freewheeling resistor has the value of 100Ω. The resistor is rated for power ratings of 75W, although no large power loss is predicted since the freewheeling resistor is only in use in very short time period. The output side is shown in Figure B- 6.

The switches and the resistor are all connected on the same PCB as the input side. The MOSFETs are mounted on a large heatsink with a thermal resistance of 0.4°C/W. Since limited data can be obtained from the datasheet (due to the device newly developed nature), a cooling fan is also added for cooling of the heatsink. Own estimations have shown that this would be sufficient for cooling of the system.

The load is enclosed in a grounded metal cage to ensure no exposed terminals. The load is three inductors connected in series having a total inductance of 100mH.

The converter is being tested using static load rather than a real SP-SRM due unavailability of a suitable SP-SRM.

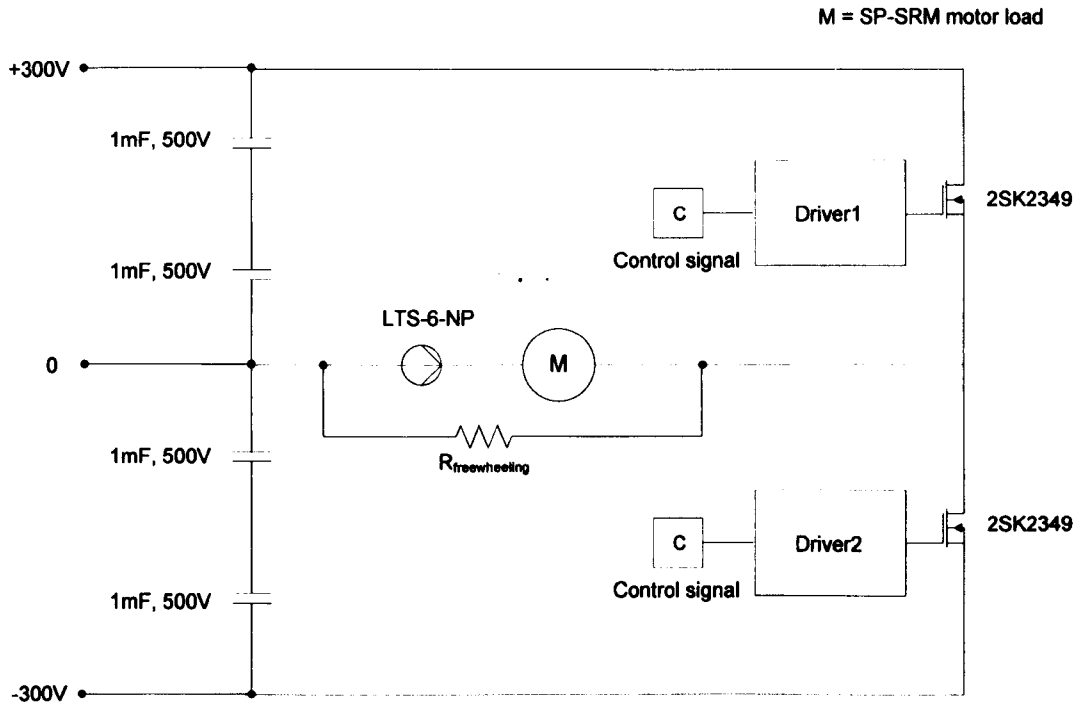


Figure B- 6 – the output side

B.1.7 MOSFET driver

The drivers for the MOSFETs are mounted on the same PCB as the other power components. The driver used is a gate drive autocoupler model HCPL-216J from Agilent Technologies. The driver is chosen because it has integrated desaturation detection and fault status feedback. The driver provides optical isolation between the high voltage path and the low voltage path of the controller.

The fault status feedback is sent to the controller to disable the switching in the event of a fault occurring. This is set as a high priority interrupt that is triggered instantly. In addition, the contactor then disconnects the power lines between the supply and the converter. Since there will be two drivers for the two MOSFETs used, separate LED indicators will indicate which driver is having the fault.

The driver allows fast turn-on and turn-off of the MOSFETs. The output of the driver is supplied by an isolated DC-DC converter model TEL15-1223 by

TRACOPOWER fed by an external DC supply. This provides total isolation from the high voltage side.

Transceivers SN75C1168N are used in between the driver and the controller to ensure error-free transmission of the data. This prevents unnecessary noise from the long lines between the power converter enclosure and the controller enclosure. One driver circuit is shown in Figure B- 7. Two similar circuits are needed for both MOSFETs.

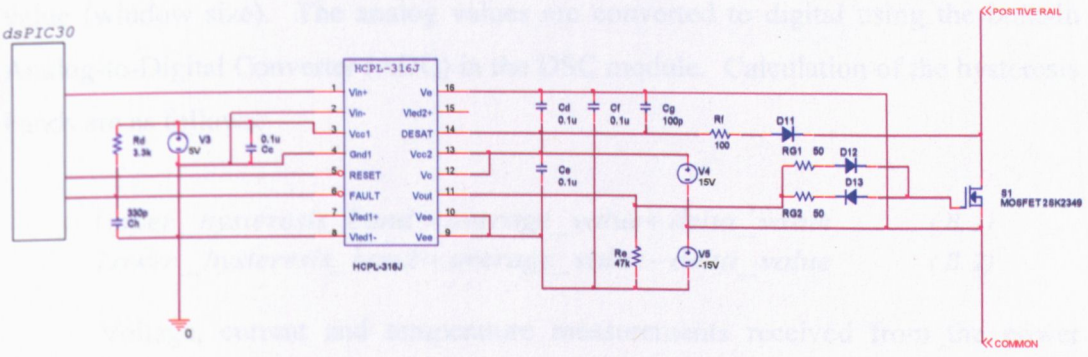


Figure B- 7 – One MOSFET driver circuit

B.2 Controller

The controller is contained in a grounded metal enclosure of the size (300mm x 200mm x 55mm). The metal enclosure also acts as a shield to reduce electromagnetic emission and interference to the environment. Power is provided from an external regulated 30V DC supply.

B.2.1 Power supply

The supply to the controller is obtained from a regulator board, which is supplied by the 30V DC supply. The regulator board has five outputs: +5V, +12V, +15V, -15V and GND. The regulator board provides supply to the current measurement board, voltage measurement boards, position sensor, temperature sensor, relay board and the controller.

B.2.2 Control system

The controller operation is implemented by using a Microchip 16-bit Digital Signal Controller (DSC) from the dsPIC30F family. The 'C' language is used as the

form of communication between the user and the DSC. The DSC operates at 30 MHz supplied by an external clock crystal.

The whole of the control system is mounted onto a PCB. The controller is connected to the power converter via standard connectors. The block diagram which shows the controller main connections and functions is shown in Figure B- 8.

Two potentiometers are provided to enable the determination of the hysteresis thresholds. One is to provide the average value, and the other, to provide the delta value (window size). The analog values are converted to digital using the built-in Analog-to-Digital Converter (ADC) in the DSC module. Calculation of the hysteresis bands are as follows:

$$Upper\_hysteresis\_band = average\_value + delta\_value \quad (B.1)$$

$$Lower\_hysteresis\_band = average\_value - delta\_value \quad (B.2)$$

Voltage, current and temperature measurements received from the power converter are also connected to the built-in ADC. The voltage measurements are compared to the capacitor full value determined in the software and the respective LED indicator will turn on. A manual converter start switch then needs to be turned on once all storage capacitors are fully charged. MOSFET switching is only allowed if this switch is turned on. The voltage measurements are also compared with overvoltage and undervoltage values pre-determined in the software. This enables any fault to be indicated.

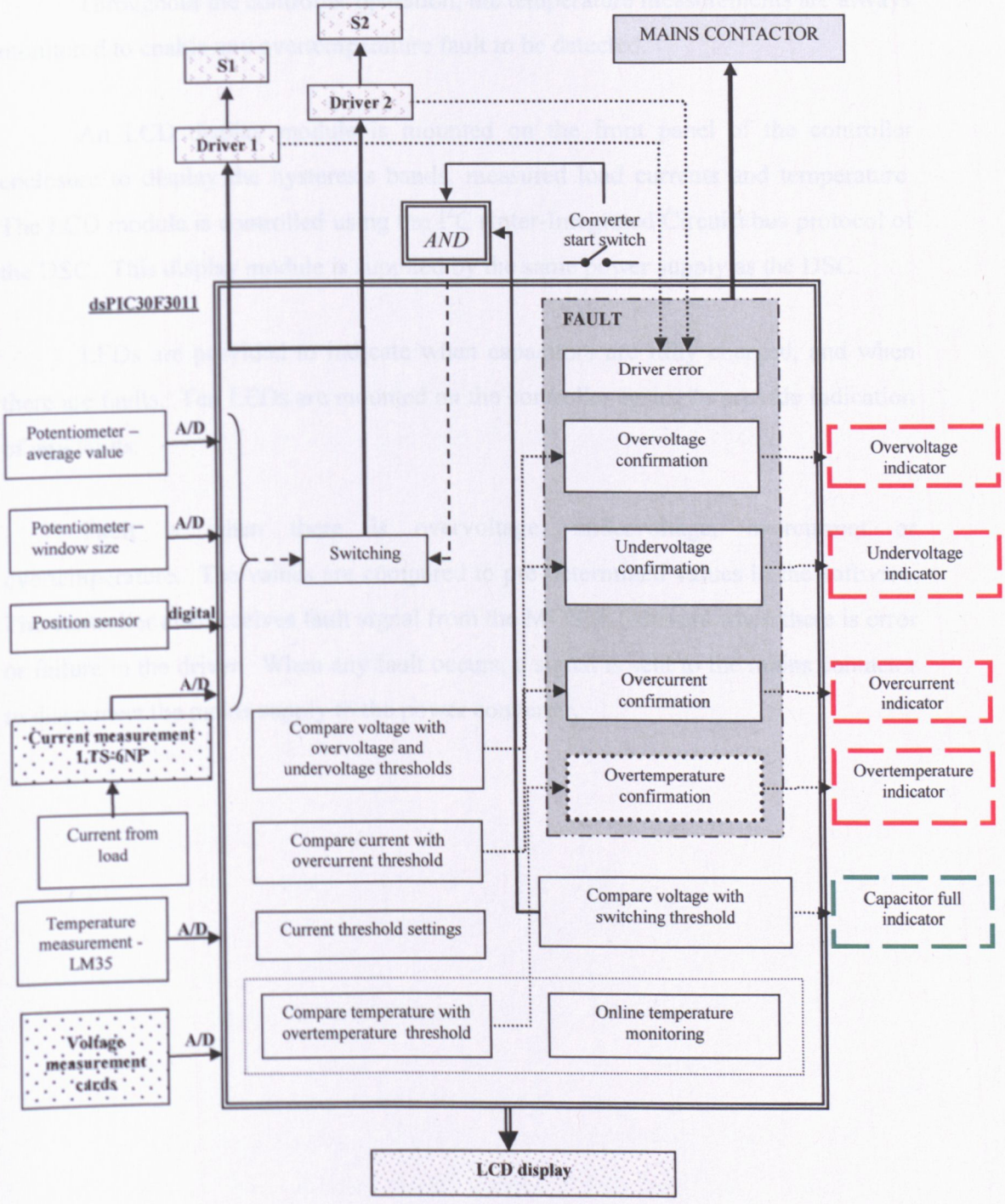


Figure B- 8 – Controller connections and functions

The current measurement will be compared with the current hysteresis bands to enable switching of the MOSFETs. The measurements are also compared with a pre-determined overcurrent value to indicate overcurrent fault.

Throughout the controller operation, the temperature measurements are always monitored to enable any overtemperature fault to be detected.

An LCD display module is mounted on the front panel of the controller enclosure to display the hysteresis bands, measured load currents and temperature. The LCD module is controlled using the I^2C (Inter-Integrated Circuit) bus protocol of the DSC. This display module is supplied by the same power supply as the DSC.

LEDs are provided to indicate when capacitors are fully charged, and when there are faults. Ten LEDs are mounted on the controller casing to provide indication of any faults.

Fault is when there is overvoltage, undervoltage, overcurrent or overtemperature. The values are compared to pre-determined values in the software. The controller also receives fault signal from the MOSFET drivers when there is error or failure in the driver. When any fault occurs, a signal is sent to the mains contactor to disconnect the mains supply to the power converter.

APPENDIX C
CONTROLLER SOFTWARE PROCESS

The controller operation is implemented by using a Microchip 16-bit Digital Signal Controller (DSC) from the dsPIC30F family. The 'C' language is used as the form of communication between the user and the DSC. Therefore, all tasks are written in 'C' language.

The program code is divided into file sections to ensure neat flow of the program. The main part of the program is located in *main.c*. There are other header and include files which complements the main program. The most important of these files is where all the Interrupt Service Routines (*ISRs.c*) are stored. The program file sections are briefly described below:

Header (defining macros for Configuration Fuse Registers)

This section invokes the macros to setup the device configuration fuse registers. The fuses selects the for example oscillator source, the power-up timers and the watchdog timer. The macros are defined within the device header files. The configuration fuse registers reside in the flash memory.

Header (defining addresses and constant values)

This header allocates the global vectors to the physical addresses. In addition, constant values are also defined. In the last part of the program, constant values specifically used in the setup of the LCD display are included.

Header (global values)

This section defines all global parameters and values. Vectors are allocated to physical addresses and comprehensible names are given.

Main

The main program starts by reading the headers. Next step is the initialisation and setup of all input and output ports, analog-to-digital conversion ports, timer and the LCD display. Then all interrupts are defined, and the priority levels determined. The hysteresis band for the hysteresis current control is then calculated. Then the program waits for the capacitors to be fully charged. The user then has to press a manual converter start switch, before any switching can happen. The dsPIC then goes into idle mode while waiting for interrupts to be generated.

Interrupt Routine

As soon as any interrupt is generated, the program runs the appropriate code in the Interrupt Service Routines. The interrupts are classified into different priority levels in order to determine the precedence. There are five interrupts which involves: (1) external interrupt from driver 1 fault signal, (2) external interrupt from driver 2 fault signal, (3) external interrupt based on the position sensor signal, (4) interrupt on every analog-to-digital (ADC) conversion, (5) timer1 interrupt at every 1ms to update the LCD display. The execution time of each interrupt service routine has been confirmed by using an oscilloscope to ensure that the time length is less than the interrupt time or an error is generated.

The watchdog timer in the program is a built-in timer running independently to the program clock. The dsPIC will reset everytime the timer overflows. Therefore, this is another safety feature to the program to ensure that the program never gets stuck indefinitely in any of the Interrupt Service Routines.

/*Interrupt Service Routine*/

External Interrupt 0 (Triggers when there is a fault signal from Driver 1)

{

Turn on 'Driver 1 Fault' LED indicator;
Turn off all MOSFETs;
Reset the relay to disconnect the mains supply and discharge all capacitors;
Stay in this loop forever;

}

External Interrupt 1 (Triggers when there is a fault signal from Driver 2)

{

Turn on 'Driver 2 Fault' LED indicator;
Turn off all MOSFETs;
Reset the relay to disconnect the mains supply and discharge all capacitors;
Stay in this loop forever;

}

External Interrupt 2 (Triggered by the position sensor signal)

{

Clear watchdog timer;
While the position sensor signal is high,
{
Turn on MOSFET 1;
Turn off MOSFET 2;
Reset lower_flag;

If the actual current is bigger than the upper limit of the hysteresis threshold,
{
Turn off both MOSFETS;
Allow for freewheeling time;
Keep MOSFET 1 off;
Turn on MOSFET 2;
Reset lower_flag;
}

While lower_flag is reset;
{
If actual current is lower than the lower limit of the hysteresis threshold,
Lower_flag is high;
Turn off both MOSFETs;
Allow for freewheeling time;
}
}

Turn off both MOSFETS;
Clear interrupt flag;

}

AtoD conversion Interrupt (Triggered by the completion of AtoD sampling and convert)

{

Allocate all AtoD buffers as follows:
Buffer0 – Current reference value provided by potentiometer 1;
Buffer1 – Current delta value provided by potentiometer 2;
Buffer2 – Temperature measurement;
Buffer3 – Actual current measurement;
Buffer4 – Top storage capacitor voltage;
Buffer5 – Bottom capacitor voltage;

Compare all values in the buffer for cases of:
Overcurrent – Limit at continuous 8A;
Overtemperature – Limit at 90 degrees;
Overvoltage – Limit at 650V continously;
Undervoltage – Limit at 300V continously;

If any of the compared values reaches the set limit,
Turn on the appropriate LED indicators;
Turn off all MOSFETs;
Reset the relay to disconnect the mains supply and discharge all capacitors;
Stay in this loop forever;

Clear the interrupt flag;

}

Timer1 interrupt (used for LCD display)

{

Initialise the LCD display;
Clear the screen;
Display temperature;
Display hysteresis thresholds;
Display actual current;
Clear the interrupt flag;

}

Non-maskable interrupts (when there is address error, stack error or arithmetic error)

{

Turn off all MOSFETs;
Reset the relay to disconnect the mains supply and discharge all capacitors;
Stay in this loop forever;

}

APPENDIX D
SP-SRM CONVERTER VISUALISATION

This appendix enables visualisation of the power converter and all test arrangements described in the thesis. A brief description of each picture is included.

D.1 Power converter

Figure D- 1 shows the test bench for the power converter. On the far left is the grounded metal enclosure of the converter. All measurement equipments and probes are also shown. The next figure, Figure D- 2 shows the load (caged) and the input autotransformer. Figure D- 3 shows the freewheeling resistor (left-hand-side of figure), the load resistor and the isolation transformer (far right).

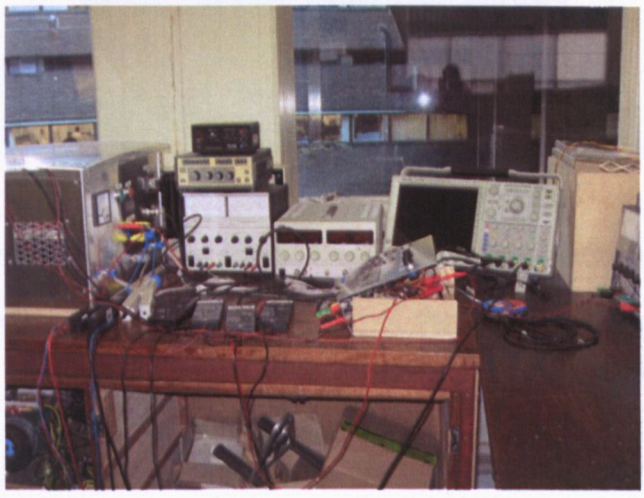


Figure D- 1-Test bench

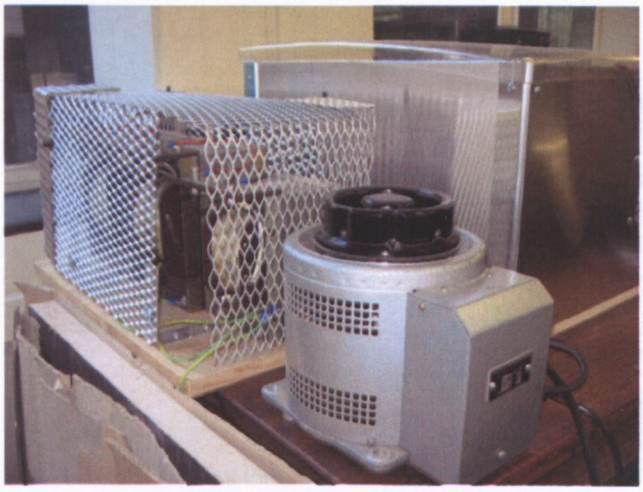


Figure D- 2- Load and the autotransformer

Figure D- 3- Freewheeling resistor, load resistor and isolation transformer

Figure D- 4 shows the internal layout of the converter. The main converter parts (capacitors, heatsink and voltage measurement card) are labeled in (a) and (b).

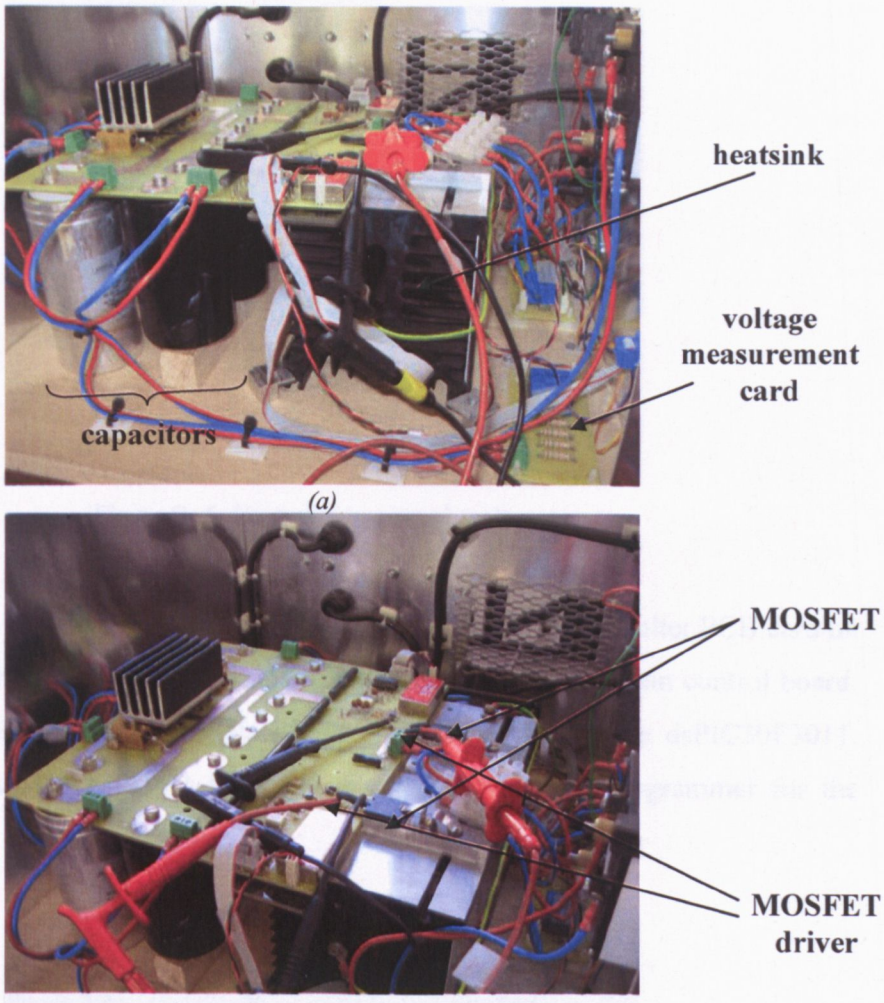


Figure D- 4- Internal layout of the converter

D.2 Controller

Figure D- 5 shows the controller in a metal enclosure connected to a regulated external 30V DC power supply. The front panel of the enclosure consists of an LCD display and 10 LEDs to indicate fully charged capacitors, overvoltage, undervoltage, overtemperature, overcurrent and driver faults. There are also two control knobs to allow for setting of the hysteresis current thresholds.

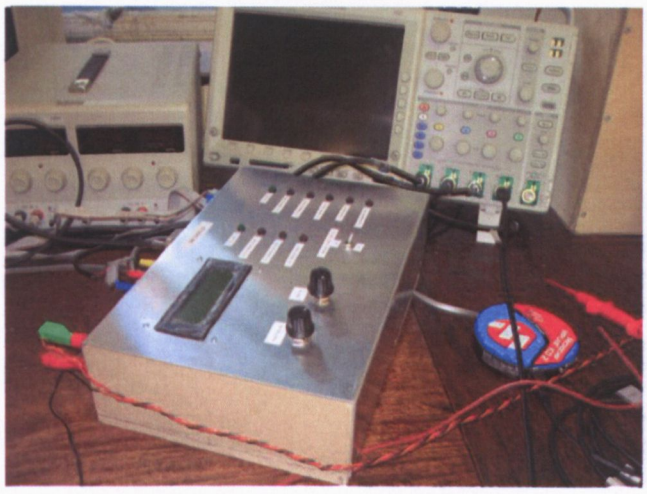


Figure D- 5- Controller in a metal enclosure

Figure D- 6 shows the internal part of the enclosure. The smaller PCB card on the left is the voltage regulator card. The larger PCB card is the main control board. The largest IC shown in the middle of the PCB is the Microchip dsPIC30F3011. Figure D-7 shows the MPLAB ICD2 in-circuit debugger and programmer for the dsPIC30F3011.

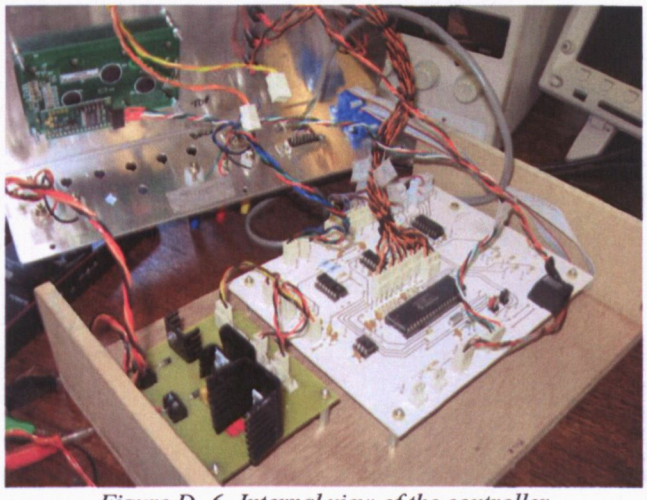


Figure D- 6- Internal view of the controller

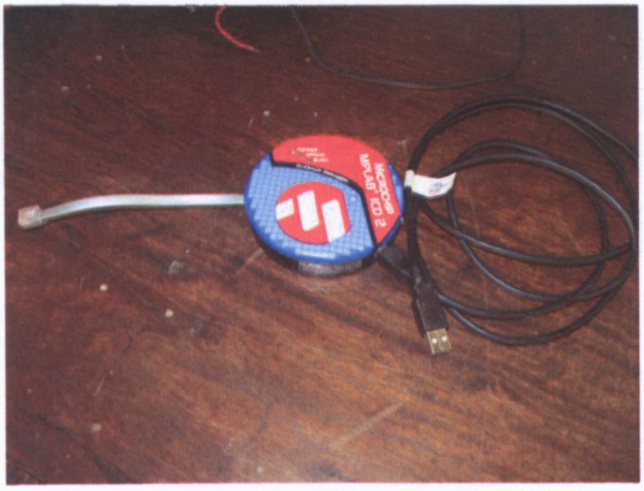


Figure D-7- MPLAB ICD2 in-circuit debugger and programmer

AUTHOR PUBLICATION

1. AYOB, A. , PICKERT, V. and SLATER, H. "Overview of low cost converters for single-phase switched reluctance motors", *2005 European Conference on Power Electronics and Applications (EPE)*, 2005, pp. 10.