High Gain Non-isolated DC-DC Converter Topologies for Energy Conversion Systems

Musbahu Muhammad
B.Eng., M. Eng.

A thesis submitted for the degree of

Doctor of Philosophy

February, 2017

School of Electrical Electronic Engineering
Newcastle University
United Kingdom

Abstract

Emerging applications driven by low voltage level power sources, such as photovoltaics, batteries and fuel cells require static power converters for appropriate energy conversion and conditioning to supply the requirements of the load system. Increasingly, for applications such as grid connected inverters, uninterruptible power supplies (UPS), and electric vehicles (EV), the performance of a high efficiency high static gain power converter is of critical importance to the overall system. Theoretically, the conventional boost and buck-boost converters are the simplest non-isolated topologies for voltage step-up. However, these converters typically operate under extreme duty ratio, and severe output diode reverse recovery related losses to achieve high voltage gain. This thesis presents derivation, analysis and design issues of advanced high step-up topologies with coupled inductor and voltage gain extension cell. The proposed innovative solution can achieve significant performance improvement compared to the recently proposed state of the art topologies.

Two unique topologies employing coupled inductor and voltage gain extension cell are proposed. Power converters utilising coupled inductors traditionally require a clamp circuit to limit the switch voltage excursion. Firstly, a simple low-cost, high step-up converters employing active and passive clamp scheme is proposed. Performance comparison of the clamps circuits shows that the active clamp solution can achieve higher efficiency over the passive solution. Secondly, the primary detriment of increasing the power level of a coupled inductor based converters is high current ripple due to coupled inductor operation. It is normal to interleaved DC-DC converters to share the input current, minimize the current ripple and increase the power density. This thesis presents an input parallel output series converter integrating coupled inductors and switched capacitor demonstrating high static gain. Steady state analysis of the converter is presented to determine the power flow equations. Dynamic analysis is performed to design a closed loop controller to regulate the output voltage of the interleaved converter. The design procedure of the high step-up converters is explained, simulation and experimental results of the laboratory prototypes are presented. The experimental results obtained via a 250 W single phase converter and that of a 500 W interleaved converter prototypes; validate both the theory and operational characteristics of each power converter.

Acknowledgements

First and foremost, all praise is due to Allah (God), who gives me the wisdom, health and patience to complete this work.

It is a pleasure always to thank the many people who have made this research work and thesis possible. The author would like to thank the Petroleum Technology Development Fund (PTDF) Nigeria; this work would not have been carried out without their funding. I would like to thank them for their financial support and the invaluable PhD Scholarship award.

I acknowledge wholeheartedly with deepest appreciation the outstanding guidance, intellectual support and encouragement provided by my supervisors, Dr Matthew Armstrong and Dr Mohammed Ali Elgendy. The successful completion of this work would not have been possible without their indefatigable patience and persistence in keeping us on schedule. I am extremely grateful for having the privilege to work with Dr Matthew Armstrong and learn from his expertise. What I learned from him is beyond just solving the research problems. He has always been and would be an inspiration to me.

Many thanks are also due to the academic and technical support staff within the school; Jack, Allan and Chris in helping with the construction of the equipment for performing the experimental work. I would like to acknowledge the support of Darren Mackie throughout the project and printed circuit board (PCB) design. Special thanks go to James Richardson and Gordon for their valuable help and guidance. Thanks to the Postgraduate Research Coordinator Gillian Webber and the remaining administrative staff for their assistance.

I am also indebted to my colleagues in the UG lab (Electrical Power Group). It has been an exciting and great pleasure to work with creative, dedicated and talented colleagues. We had many interesting discussions during the past years, and I will always remember the time we spent together and the friendship.

My heartfelt appreciation goes to my mum for her moral support and encouragement throughout my life and further education. I would like to thank my family members and relatives who have inspired and continued to motivate me. Finally, I would like to appreciate

the endless support I received from my family, especially my wife for her encouragement, prayer and understanding in this research work and future endeavour.

Finally, I am grateful to my children, Fatima, Khadija and Muhammad. They have been behind me throughout this research work. I would like to thank them for their patience during the moments when they needed me most and the research work keeps me away from them.

Contents

Figures

Tables

Symbols

AC	Alternating Current
ADC	Analogue to Digital Converter
CCM	Continuous Conduction Mode
DC	Direct current
DCM	Discontinuous Conduction Mode
DPG	Distributed Power Generation
DSP	Digital Signal Processor
EMI	Electro-Magnetic Interference
ESS	Energy Storage System
EV	Electric Vehicle
HID	High Intensity Discharge
HEV	Hybrid Electric Vehicle
IGBT	Insulated Gate Bipolar Transistor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LTI	Linear Time Invariant
MOSFET	Metal Oxide Field Effect Transistor
MPPT	Maximum Power Point Tracking
PFC	Power Factor Correction
PHEV	Plug-in Hybrid Electric Vehicle
PI	Proportional-Integral
PV	Photovoltaic
PWM	Pulse Width Modulation
RCD	Resistor-Capacitor-Diode
RES	Renewable Energy Sources
RMS	Root-Mean-Square
UPS	Uninterruptible Power Supply
(ZCS)	Zero Current Switching
ZCT	Zero Current Transition
(ZVS)	Zero Voltage Switching
ZVT	Zero Voltage Transition

Chapter 1
Introduction

1.1 Background

The growing use of renewable energy sources (RESs) and Energy storage systems (ESS), due to global environmental concern, brings new challenges to the energy conversion technology. Because some devices that store or produce electrical energy (e.g., batteries, ultra-capacitors, fuel cells and solar photovoltaic) is often realized using multiple low voltage cells, which are usually connected in series to produce sufficient voltages for the intended application. Unfortunately, series connection of cells degrades the system performance, adds complexity to the system, and possible temperature rise due to fabrication variation and different operating conditions between cells. In batteries, this may be related to the state of charge of a cell. In solar arrays, it may be due to a change in solar irradiance or partial shading of the array.

Many green power supply system calls for a high efficiency, high step-up DC-DC converter in the power conversion stage. Typical applications include grid-connected inverters [1-4], motor drive [5], uninterruptible power supply system (UPS) [6, 7], telecommunication/network server power systems [8], electric vehicle (EV) [9], high intensity discharge (HID) lamps [10, 11] and distributed power generation (DPG) system [12]. Furthermore, high voltage step-up gains usually ten times or higher are increasingly required when the system is powered by low voltage energy sources such as Li-ion batteries, solar arrays and fuel cells. It is necessary or customary to use a relatively high and stable DC voltage in these applications. Besides, considering that the overall cost of a renewable energy system is high, the use of high-efficiency power electronic converter is necessary.

The boost and buck-boost converters are the simplest non-isolation topologies that produce an output voltage that is greater in magnitude than the source voltage [13, 14]. However, the conventional boost and buck-boost converters must operate at extreme duty ratio to achieve high voltage gain (in particular ten times). This is an undesirable operating point since the

output diode sustains short pulse, high amplitude, current pulses which result in severe reverse recovery losses. Besides, as the output voltage increases so must the voltage rating of the semiconductor switching devices and at high duty ratio the conduction losses of the semiconductor device can make a more significant impact to the performance of the system. Furthermore, as the duty ratio approaches unity, the output voltage approaches zero, and the efficiency decreases to zero [14]. Consequently, the converter may suffer poor dynamic response to system parameter changes and potential load variations. This behaviour is typical of converters having boost or buck-boost characteristics. The challenge for any high step-up DC-DC converter is to avoid extreme duty ratio operation.

Rather than a conventional single stage boost converter, a cascade boost converter is an attractive solution to enlarge the voltage gain without extreme duty ratio operation. However, the controllers must be synchronized, and the stability of the converter is another concern [15]. Moreover, the second stage may experience severe reverse recovery related losses in high power applications. Furthermore, the energy has to be converted twice, which obviously has an impact on overall efficiency.

Classical converters with magnetic coupling such as flyback or push-pull converters can easily achieve higher conversion ratio, by proper choice of the transformer turns ratio. One of the most commonly understood transformer based topologies is the flyback converter. The main drawback of the transformer based topologies is high turn off voltage spike seen by the primary switch, due to the transformer leakage inductance interaction with parasitic capacitor of the switch. To go some way to mitigating these effects, energy recycling techniques must be adopted to recycle the leakage energy [16]. Moreover, the transformer volume and weight is another problem that inhibits developing a compact, high power density converter. Thus, whilst functional, these types of converters do not offer an optimal solution in cost sensitive power supply applications.

This thesis is concerned specifically with research into high step-up DC-DC boost converter topologies. There is increasing interest in the use of high step-up DC-DC boost converters for harvesting all available energy, typical applications call for high-efficiency high step-up converters. These two features are the focus of this research. Basic boost and buck boost converters operate with extreme pulse width modulation (PWM) duty ratio to achieve higher conversion ratio of (ten times or higher). Appropriate duty ratio is desirable since extreme duty ratio operation have long been recognised as causing some operational drawbacks to the high step-up converters.

Some of the major shortcomings of extreme duty ratio operation include reverse recovery loss of the output diode as a result of short pulse current with large amplitude. Furthermore, the output diode reverse recovery problem can lead to higher turn-on switching loss for the power switch. For this reason, there is considerable motivation to improve the performance of high step-up boost converters by alleviating the diode reverse recovery loss so that switching loss can be significantly reduced. Literature has revealed that the power device voltage rating in conventional boost converter is the same as the converter output voltage. Another concern related to the efficiency of high step-up converters is power device rating. A high voltage rated device is not a good choice for the steady state operation because of the high input current (as the power MOSFET rating increases, so does the on-state resistance R_{ds_on} resulting in conduction losses which also degrade the efficiency). The challenge for a high step-up converter is to dramatically reduce the conduction losses. Appropriate duty ratio operation, conduction losses reduction and alleviation of diode reverse recovery problem can greatly improve the efficiency of power conversion. It is the aim of this thesis to investigate methods of improving the performance of high step-up converters.

1.2 High Step-up DC-DC Converters Applications

Many applications powered by RESs call for a high-efficiency high step-up DC-DC converter in the power conversion stage. Typical examples include grid connected inverters [1-4], high-intensity discharge lamp (HID) [10], electric drives [17] and uninterruptible power supply system (UPS) [6, 7]. Some emerging applications that require high step-up DC-DC power converters are briefly described in the following section.

1.2.1 Grid Connected Photovoltaic Inverter

One of the most important applications of solar photovoltaic (PV) is electricity generation, particularly in countries having a considerable amount of solar radiation. The application could be a stand-alone or grid-connected system. The PV grid-connected power system is a fast growing segment in Europe, with record addition of 1.9 gigawatts in Germany, 2.4 gigawatts for the United Kingdom, 0.9 and 0.4 GW for France and Italy respectively in 2014 [18]. Countries like Japan, China and the U.S have added 9.7, 10.6 and 6.2 GW respectively for the same year under review. This addition brings the total global installed capacity to 177 GW [18].

Figure 1.1 shows the block diagram of a typical grid connected PV power system. PV panels

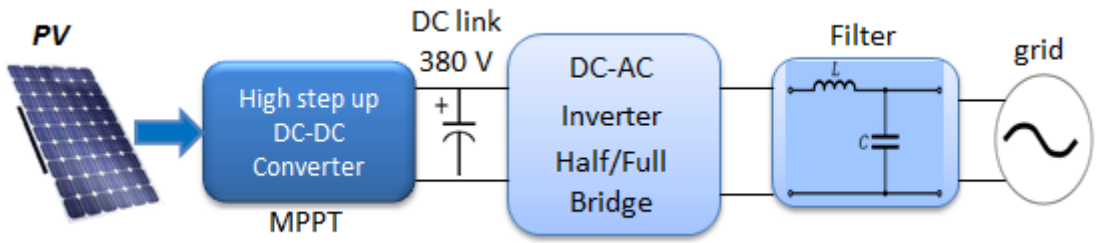

Figure 1.1 Single phase grid connected renewable energy system

are often connected in series to obtain the DC link voltage along with the power converter to track the maximum power point (MPP) range of the PV. However, when partial shading occurs or mismatch, the MPP losses increase significantly. Another configuration is to use a modular approach to reduce the cost and improve the system MPPT efficiency; in this case, an independent module integrated DC-DC converter is used for each PV panel. Thus, decoupling every panel from others to make the system configuration flexible and maximizes the output power. Nevertheless, the topology normally has two power electronic converters. The first converter is the high step-up boost converter that is required to raise the relatively low solar panel DC voltage to a certain level suitable for synthesizing the alternating current AC line voltage, which is typically 380 - 400 V DC. The second converter is the DC-AC inverter that injects sinusoidal current into the grid. The high step-up DC-DC converter along with maximum power point tracking (MPPT) algorithm stabilise the DC bus voltage level and make full utilization of the PV array. The performance of the high step-up DC-DC converter is crucial to the performance of the whole PV system because the DC-DC converter is the core element that interfaces the solar photovoltaic with the DC-AC inverter and manages the power flow.

The main shortcoming of a grid-connected power system is power contributed by the system to the grid is available only during part of each day since solar energy is available only during the daylight hours. To overcome this problem an energy storage system ESS such as battery is usually employed in the photovoltaic inverter systems to improve the system performance and supply availability [19]. The objective of utilising the ESS is to provide a back-up function, transferring the solar energy to the ESS during the sunny time, whilst delivering energy to the DC bus when the solar energy is not available. As a result, stable and fast response AC power can be provided to the grid. Integrating the grid connected PV system with ESS is achievable with the aid of bidirectional DC-DC converter that has power flow in both forward and reversed directions (boost and buck).

1.2.2 High Intensity Discharge (HID) Lamp

High-intensity discharge (HID) lamp are preferable, instead of conventional halogen lamps for use as automobiles headlamps due to its superior performance and numerous advantages, such as higher efficiency, longer life, good light beam focus and superior colour rendering capability. Although the HID lamp has significant advantages, its operation is similar to the other discharge lamps and requires a ballast to control the lamp power during steady state operation.

Figure 1.2 shows typical ballast circuit for powering and igniting the lamp. The ballast consists of high step-up DC-DC converter, an inverter and an igniter. The HID are powered using the automobile 12 V battery, which provide an input voltage much lower than the operational voltage of the ballast. For this reason, a high step-up DC-DC converter is required in the ballast to step-up the battery voltage to (380 V - 400 V) during start up and in the (60-135 V) range during steady state operation [10, 11]. Therefore, a high step-up DC-DC converter with about tenfold voltage gain is critical for the operation of the lamp.

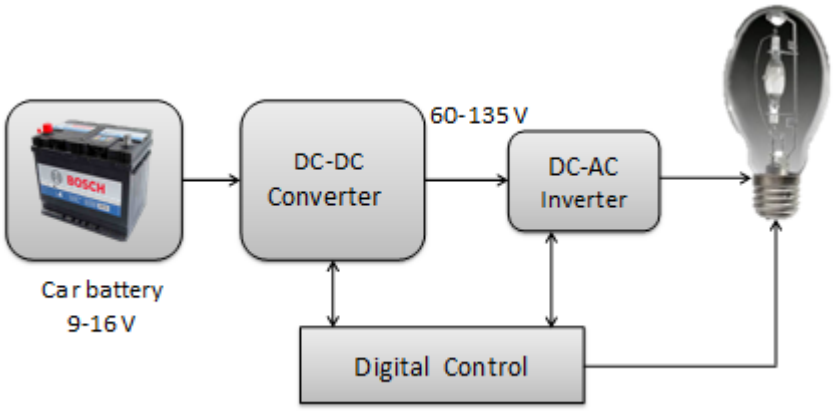

Figure 1.2 High Intensity discharge lamp ballast block diagram

1.2.3 Electric Vehicle

The automotive companies are focused on electric vehicles (EV), hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV) and fuel cells vehicles to meet the demand for emission-free vehicles with improved fuel economy, comfort and safety. However, the key challenge lies in the efficiency, cost, size of power electronic converter and machine. In particular, the high step-up DC-DC converter to interface the fuel cell voltage with the battery packs.

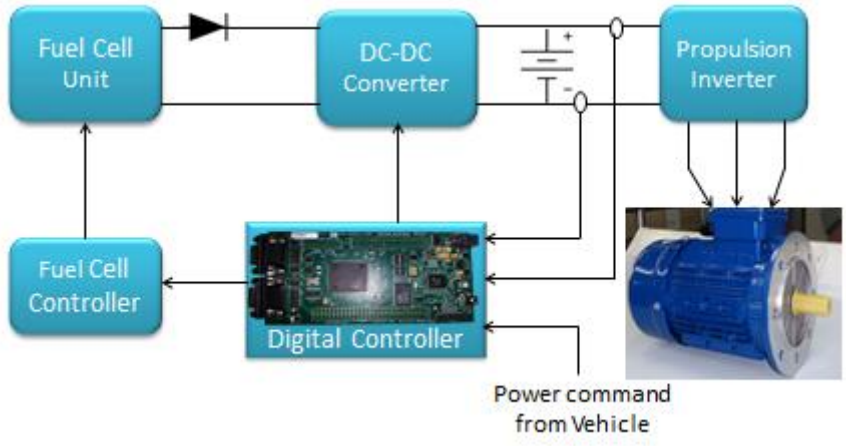

Figure 1.3 Electric vehicle drive train

Figure 1.3 illustrates a typical fuel cell vehicle propulsion system. A high step-up DC-DC boost converter is usually employed to step-up the relatively low DC voltage of the fuel cell to a typical DC link voltage of 400V which is also compatible with the battery. An inverter is then used to drive the propulsion motor. ESS such as: Li-ion batteries are often used to provide supplementary power during vehicle starting, acceleration and hill climbing. Different configurations and classifications of electric vehicle propulsion system can be found in [9]. The use of bidirectional DC-DC converter along with ESS in electric vehicle to achieve power transfer in either direction is demonstrated in [20] The regenerative energy fed back by the electric machine during breaking is absorbed by the battery. Whilst the capacitive energy source is step-up by the converter to compliment vehicle starting and acceleration.

1.2.4 Uninterruptible Power Supply UPS

The growing use of Uninterruptible power supply (UPS) to supply power to the sensitive loads and protect them during mains outages under normal or abnormal utility power conditions is well documented [6, 7]. UPS has been widely used to supply seamless power to critical loads, such as medical equipment, communication systems computers and servers. All UPS uses specific DC-DC power electronics converters to interface different sources and load. For example, the UPS topology consists of power factor correction (PFC) circuit, which is typically an AC-DC front-end converter that convert the ac-line voltage ($90 - 265\ V_{rms}$) and provides a regulated DC link voltage of (380 - 400 V) required by the inverter. During the mains or utility outage, the UPS enters the backup mode, and the UPS generate AC voltage from the 48 V back-up batteries to supply the load. A high step-up converter is necessary to raise the battery bank voltage to that required by the DC bus.

1.2.5 Telecommunication Power System

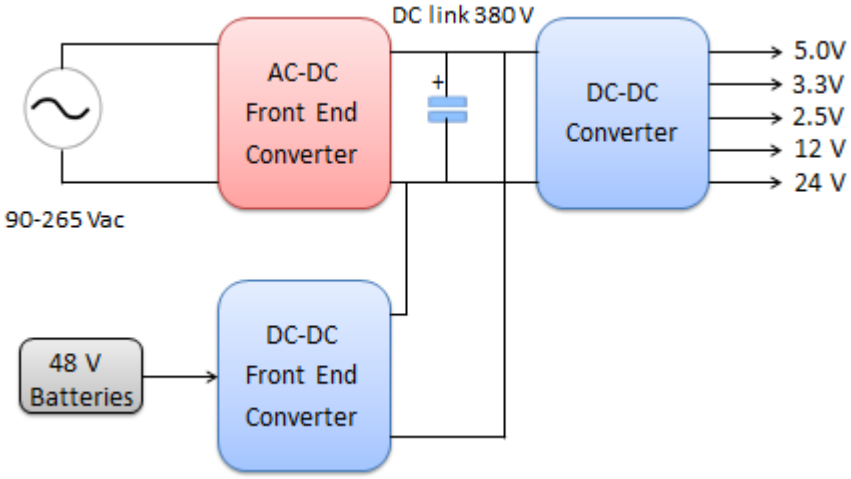

Figure 1.4 Dual front end telecom power system

Typically, UPS provide up to 30 minutes of reserve time; this is far shorter than the reserved time needed by telecommunication power systems. Consequently, using 48 V DC telecom bus has become a natural choice of powering data processing equipment installed in the telecom environment [10]. Figure 1.4 shows a typical Power supply system of telecommunication equipment. The power supply is characterised by high power density, efficiency and has several stages [8]. Traditionally the first stage is AC-DC system powered from AC-line voltage $(90 - 265\ V_{rms})$ and provides a high step-up DC bus voltage of up to (400 V). The AC-DC converter serves as a power factor correction circuit for suppressing the harmonic level. The nominal 380 V bus voltage is converted to a tightly regulated lower voltage of 5, 3.3, 12 and 24 V respectively for the logic circuits. However, during the mains outage the telecommunication industries uses 48V DC battery bank as a conventional choice to provide back-up. In this case, a DC-DC high step-up back-up converter is required to provide a simple and efficient solution of raising the 48V DC battery bank voltage to the 400 V DC link voltage. A high step-up DC–DC converter that generates 400 V DC from 48 V DC batteries is necessary in the telecommunication server power supply system.

1.2.6 Distributed Power system

Distributed power generation (DPG) systems are considered to be the key components of future power grids due to its ability to produce and distribute energy to various loads. For the purpose of robust control, monitoring, power quality improvement, fault detection/isolation and stabilization, DPG uses Microgrids in combination with renewable energy sources such as batteries, photovoltaic panels, fuel cells and loads [12]. Microgrids can operate

autonomously or grid connected depending on the configurations, and there is no doubt that DPG is the building blocks of a smart grid.

Figure 1.5 shows the DPG block diagram. The system requires specific power electronics converters to convert and regulate the generated power before interconnection with the utility grid and/ or onward supply to consumer loads [21, 22]. It is necessary to employ DC-DC converters with various power levels to exploit the locally produced power to meet the requirement of various local loads. In a nutshell, the quality and efficiency of the overall system depend on the performance of these power electronic converters.

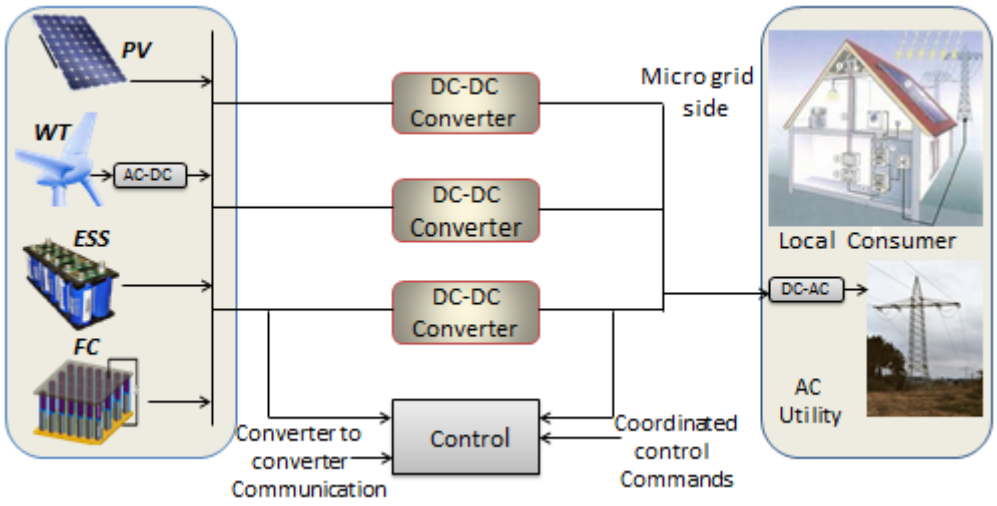

Figure 1.5 Distributed power system

1.3 Characteristics of High Step-up Converters

In general, the performance of high step-up DC-DC converters exhibits high output voltage and large input current. The large input current emanates from low input voltage. Therefore, some of the desirable characteristics of high step-up converters are briefly described in the subsequent sections.

1.3.1 High Conversion Ratio

Many applications powered by RESs or ESS call for high step-up DC-DC converters. For example, the output voltage level of the PV array in the grid-connected inverter is typically low 16- 43 V and the DC bus voltage suitable for synthesizing the AC line voltage is 380 - 400 V DC. About ten times (10X) or higher voltage gain is required to raise the array voltage to DC link voltage for steady state operation.

1.3.2 High-Efficiency

The large input current is a major concern related to the efficiency of the high step-up DC-DC converters. Low input voltage results in large input current. Therefore, higher peak and root-mean-square (RMS) current stress suffered by the switching components is a primary detriment to increasing the efficiency. To enhance the efficiency of DC-DC converters low rated devices with low on-state resistance are desirable to reduce the conduction loss. In high voltage applications, the reverse recovery problem of the output diode is another concern. Lower rated diodes typically recover faster.

1.3.3 Low Voltage/Current Ripple

Power electronic converters have an inherent switching characteristic, which causes the current and voltage to fluctuate. For example, in DC-DC boost converter, the switching action of the power MOSFET or IGBT causes the inductor current to have a triangular waveform with a DC offset. The DC component of this inductor current flows through the load and AC components via the output capacitor. A capacitor ripple voltage is produced due to time-varying current through the capacitor. The input current or the output voltage contains some ripple on top of the steady state value. Power electronic converter designers consider the ripple magnitude to be a key parameter in designing such systems. Minimization of the current/ voltage ripple (AC component in the system) which decreases the efficiency lifetime of the converter is essential. In an ideal situation, only DC components should be present at the output.

1.3.4 Fast Response

In a DC-DC converter operating under closed loop control, the duty ratio is determined by the converter nominal operating point based on converter dynamics. Likewise the load resistance, which is also based on DC loads requirement. The load resistance and duty ratio are exogenous quantities that require compensation scheme due to pole-zero variation. The converter should exhibit a fast response in the presence of load/source changes, other external disturbances and must be able to operate in adverse environmental conditions.

1.4 Motivation

Theoretically, conventional boost and buck-boost converters are the simplest PWM controlled topologies for voltage step-up. However, these converters must operate under extreme duty

ratio to achieve high voltage gain which severely penalizes the efficiency. In addition, the high output voltage requires higher rated device with large on-state resistance. As the power device rating increases so does the conduction loss which further degrade the efficiency. Furthermore, the output diode sustains a short pulse current with the high amplitude that result in reverse recovery related losses. One of the main challenges of high step-up DC-DC converters is to avoid extreme duty ratio operation so that both switching and conduction losses can be substantially reduced. Finding a way to avoid extreme duty ratio operation in high step-up converters is one of the motivations of this thesis.

One of the simplest solutions for avoiding extreme duty ratio operation is by using cascade structure. In cascade structure, both stages can achieve step-up function and switch conduction loss is low in the first stage. However, the high output voltage still affects the efficiency of the second stage. Transformers or coupled inductor based converters such as flyback and forward converters can provide higher conversion ratio without extreme duty ratio operation by utilising the transformer turns ratio. A drawback to the use of a transformer is high voltage stress seen by the power device, due to the interaction between the leakage inductance and switch capacitance conventionally requires a snubber. A resistor-capacitor-diode (RCD) snubber can suppress the device voltage stress, but the leakage energy dissipates within the snubber contributing to the losses. A passive lossless or active clamp circuit can recycle the leakage energy and reduce the device voltage stress. Evaluating the performance of leakage energy recycling schemes on the same power converter is another motivation.

1.5 Aim and Objectives

Power electronics converters are key components for interfacing and conditioning the power level of source and load in many applications. Direct connection to various voltage levels requires utilizing advanced topologies combined with low-rated high- performance power semiconductor devices.

The aim of this research is to develop a high step-up DC-DC power conversion system to meet the requirement of emerging power supply system in energy delivery and management.

The main objectives and research contributions are:

- To propose a new single phase non-isolated DC-DC boost converter based on coupled inductor and capacitor charge transference with high conversion ratio.

- To propose a new high step-up high-efficiency interleaved non-isolated coupled inductor DC-DC boost Converter with ten times (10X) static gain or higher.
- Application of capacitor charge transference and a coupled inductor turns ratio in high step-up converters to avoid extreme PWM duty ratio operation.
- To develop models of the interleaved high step-up converter suitable for control design implementation.
- Experimental assessment of the performance of the proposed single phase and interleaved high step-up converters using a digital signal processor (DSP) platform.

In order to achieve the above goals the thesis proposes the following approach:

a. Application of active clamp circuit to depress the coupled inductor leakage energy and realize zero voltage switching (ZVS) technique so as to minimize the switching losses under high-frequency operation.
b. Assess the performance of active and passive clamping schemes in recycling the leakage inductor energy with regards to single phase high step-up converter.
c. Utilize an interleaved technique to increase the power density and improve the efficiency of high step-up converter.
d. Utilizing the inherent leakage inductance of the coupled inductor to alleviate the reverse recovery related losses of the diodes.
e. Present a comprehensive steady-state operational analysis and design guidelines of the converters.

1.6 Thesis layout

The thesis is structured as follows:

Chapter 2: Literature Review- A background description and review of the methods of developing the state of the art high step-up boost converters is presented to define firstly the work and its novelty. The main challenges related to the current state of the art non-isolated high step-up DC-DC boost converters are identified. The improved system platform is then proposed with the advantages of higher efficiency, simple circuit and low cost.

Chapter 3: This chapter proposes a new single phase high step boost converter employing coupled inductor and voltage gain extension cell. A description is also given on how the topology is developed based on the concept of two capacitors charged in parallel and discharged in series. The capacitors are integrated into coupled inductor boost converter to

configure the voltage gain extension cell. The state of the art solution of alleviating the reverse recovery problem of the output diode is to control the current falling rate with the aid of an auxiliary circuit. In this approach the diodes are always in series with the coupled winding when the diodes turn off. This makes the leakage inductance available to control the current falling rate of the diodes. Thus, the diode reverse recovery problem is alleviated. The power stage model is fully investigated and developed. Experimental test results of a 250 W implemented prototype are given to verify the operational principles.

Chapter 4: The performance evaluation of clamp circuits has been carried out in this chapter by replacing the active clamp solution in chapter 3 with passive clamp scheme. On one hand, the passive clamp approach achieves similar function of active clamp circuit in depressing the leakage inductance energy with low level of circulating current in the clamp circuit, cost reduction and higher reliability. On the other hand, the passive clamp converter has the advantage of achieving zero current switching (ZCS) of the primary switch. Experimental results revealed that the active clamp converter achieves higher efficiency than the passive clamp converter.

Chapter 5: The main drawback of the coupled inductor in a high step-up application is a large current ripple. This issue is addressed by proposing an interleaved high step-up boost converter with high voltage gain. The topology demonstrates how the high input current is shared between the interleaved phases and minimizes the current ripple. It further illustrates that by appropriate current sharing the passive components size is reduced, which improves the thermal distribution and the transient response. Detailed steady state analysis including design consideration is presented. A 500 W laboratory prototype have been developed, and the experimental results are given to validate the theoretical analysis.

Chapter 6: In this section, the modelling of the proposed interleaved high step-up boost converter is demonstrated. It also highlights the steps in obtaining the full and reduced order models of the converter based on state space averaging. The reduced order model is linearized and various linear time invariant (LTI) transfer functions are derived. Furthermore, a block diagram model is developed suitable for dual loop average current mode control. The dual loop controller is implemented with Texas Instrument TMS320F28335 digital signal processor (DSP). The controller provides smooth power flow control.

Chapter 7: Conclusion- deals with the summary of the whole work and the extent to which the research aim and objectives have been met. Conclusions are drawn from the study and potential areas of further investigation are equally suggested.

1.7 Research Impact

The Proposed Interleaved high step-up boost converter developed in this thesis has attracted Industrial Consortium under the project known as HICO. The 500 W converter prototype have been installed and currently running in a car as a technology demonstration on electric vehicle EV battery charging application. The interleaved high step-up converter is used as an interface for charging the automotive traction batteries (Li-ion batteries) from a low voltage source (12 V car battery). In this application, the maximum voltage required is 100.1 V. Therefore, the duty ratio is adjusted to obtain the desired voltage level. In addition, there is future plan to develop a 2 KW converter for use in the same application.

1.8 Publications Arising from this Research

The research work carried out in this thesis has resulted in publication in IEEE journal of emerging and selected topics in power electronics (JESTPE):

- Muhammad M., M. Armstrong, and M. A. Elgendy, "A Non-isolated Interleaved Boost Converter for High voltage Gain Applications." IEEE Journal of Emerging and Selected Topics in Power Electronics, 2016. 4(2): pp. 352-362,
- Muhammad M., M. Armstrong, and M. A. Elgendy, "Analysis and Implementation of a High Gain Non-isolated DC-DC Boost Converter" Submitted for peer review in: IET Power Electronics.

In addition, the following conference papers stemmed from the research

(1) Muhammad, M., M. Armstrong, and M. Elgendy. "Non-isolated DC-DC converter for high-step-up Ratio Applications", in Power Electronics and Applications (EPE'15 ECCE-Europe), 2015, 17th European Conference on. 2015

(2) Muhammad, M., M. Armstrong, and M. Elgendy. "Non-isolated, high gain, boost converter for power electronic applications." in 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016). 2016.

(3) Muhammad, M., M. Armstrong, and M. A. Elgendy, "Modelling and Control of Non-isolated High Voltage Gain Boost Converter Employing Coupled Inductor and Switched Capacitor." in 2016 International Conference for Students on Applied Engineering (ICSAE). 2016.

1.9 Summary

This section provides a general background of the high step-up DC-DC conversion and their typical applications, in particular, it demonstrate the rapid increase in the use of DC-DC converters and their roles as an interface for connecting various voltages levels and managing the power flow. Following this, the motivation of the whole work is presented. The aim of the research is then defined; to develop a high efficient, high step-up DC-DC power converter system based on current commercially available power semiconductors to meet the requirement of emerging applications in providing future energy delivery and management.

Chapter 2

High Step-up DC-DC Conversion Techniques -A Literature Review

2.1 Introduction

High step-up DC-DC boost converters are widely used as an interface to transfer power between the low voltage sources to a higher DC bus. In many modern applications, such as HID lamp [10], EV [9] and grid-connected PV systems [2] powered by RESs; it is necessary to utilise converters with high static gain, usually ten times or higher. Since most of these RESs provide a low output voltage, a conventional boost or buck-boost converter can be employed to step-up the source voltage to the voltage level required by the load. However, the conventional boost and buck-boost converters suffer extreme PWM duty ratios to achieve high voltage gains. The output diode sustains short pulse current with high amplitude, which results in severe reverse recovery losses. In addition, as the output voltage increases so must the voltage rating of the semiconductor switching device and because of the high input current that results from the low input voltage, the conduction losses of the semiconductor device can make a more significant impact on the performance of the system. Furthermore, as the duty ratio approaches unity, the converter may suffer poor dynamic response to system parameter changes and potential load variations [23, 24].

Various techniques for high step-up conversion have been reported in the literature [10, 23, 25-46]. Depending on the application, they are either isolated [25-35, 47] or non-isolated [10, 23, 36, 37, 39, 41, 43, 44, 46, 48-50] topologies. Transformer based converters can easily achieve high voltage gain by adjusting the turns ratio and utilises low rated devices to reduce the conduction losses. However, the leakage inductor induces high voltage stress to the power device and traditionally requires a snubber. Either RCD snubber circuit or a clamp circuit must be used to handle the leakage energy. To address the demand for high step-up high power density in DC-DC converters, the power electronics community and industries have

been reacting in two different ways; developing semiconductor technology and or developing new converter topologies. This work addresses the later by proposing new converter topologies.

The high-frequency operation has been explored in the literature due to significant advantage of reducing the volume and weight of the converter. Miniaturization of power converter circuits is possible if they operate at a higher switching frequency. However, the switching losses are proportional to switching frequency. To design a compact converter, a way to minimise or eliminate the switching losses must be conceived. Resonant and soft switching techniques are applied to high step-up converters to mitigate the switching losses.

This chapter presents an overview of techniques of developing high step-up non-isolated DC-DC boost converters. The first section of this chapter describes the characteristics of conventional boost converter being the most popular topology and its major limitations in high step-up application. The subsequent section evaluates different techniques aimed at overcoming the limitations of the boost converter and improving the conversion ratio. The main advantages and drawback regarding each technique is highlighted, and the rationale for choosing the magnetically coupled converters and voltage gain extension cell in this work is explained clearly. Furthermore, some soft switching techniques and methods of alleviating the diode reverse recovery related losses are also reviewed.

2.2 DC-DC Boost Converter

2.2.1 General Structure of DC-DC Boost Converters

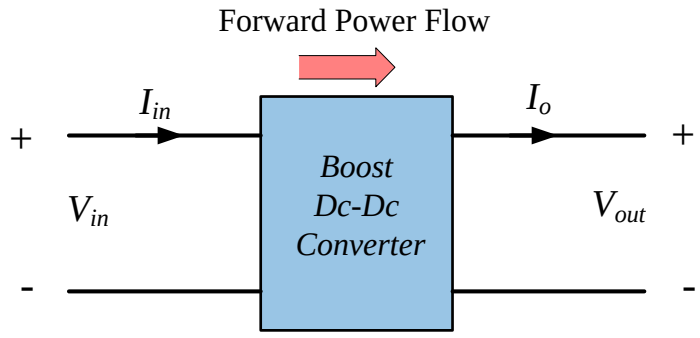

Figure 2.1 Boost converter unidirectional power flow

Figure 2.1 illustrate the generic structure of the DC-DC boost converter. Depending on the configuration, the input side can be current fed or voltage fed. The input voltage can be a battery, fuel cell or solar photovoltaic. The load is placed on the output side; this could be an

inverter in stand-alone or grid-connected power system. The converter has a unidirectional power flow. The active switch is typically implemented with semiconductor devices such as MOSFET or IGBT. The term step-up and boost are used interchangeably to imply a converter whose output voltage is always higher in magnitude than the input voltage [14, 51]. In most cases, boost refers to converters without wide conversion ratio, whilst high step-up usually refers to converter with wide voltage gain. DC-DC converters are further classified as isolated or non-isolated

2.2.2 Isolated DC-DC Boost Converters

The high-frequency transformer based system is an attractive solution for providing galvanic isolation and impedance matching between the source and load. As an example, isolation is usually required by regulatory agencies in off-line power supply applications. Classical converters with galvanic isolation such as flyback, current-fed push-pull converters can easily achieve high voltage gain by adjusting the turns ratio. However from an efficiency standpoint, the high-frequency transformer implies additional cost, losses and inhibits developing a compact converter. Thus, the volume weight and losses are the main limitations of isolated converters in embedded applications. Isolated boost converters are either current-fed [26-28] or voltage-fed [34, 52]. Some typical examples of isolated DC-DC converters topologies include flyback [16, 53], forward [54], full bridge [26, 27], half bridge [28-30, 55], push-pull converters [31-33] or their variations.

A flyback converter is the most widely understood topology due to its relative simplicity. Theoretically, the transformer reduces the magnetic components count by providing energy storage and galvanic isolation. However, the semiconductor devices incur current and voltage stress which limit its use to low power applications. The interaction between the parasitic capacitor of the switch and transformer leakage inductance induces high voltage spike during turn off which necessitates the use of clamp circuit. The simplified circuit of flyback converter is shown in Figure 2.2. Note that a red colour is chosen for the power switch, load resistor, blue for the power diode and green for the capacitor. The colour convention is adopted throughout this thesis for easy recognition of one passive component from the other.

The full bridge DC-DC converter is considered one of the famous isolated topologies, with more component counts when compared with the half bridge converter. The operation of the circuits involves utilisation of the transformer leakage inductance for transferring energy from source to the load. Prominent advantages of full bridge converter include immunity from

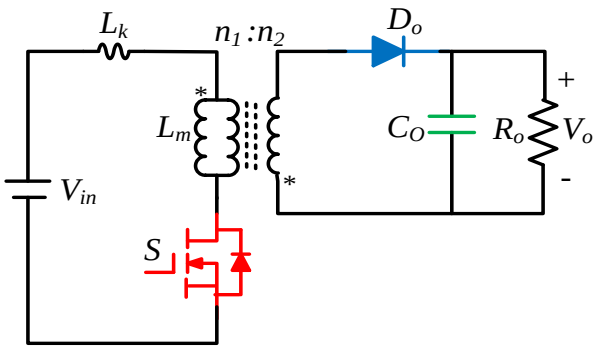

Figure 2.2 Flyback converter

transformer flux imbalance and absence of output inductor. A fundamental shortcoming of the voltage fed full bridge converter is the voltage spike across the output diode, due to the leakage inductance of the transformer. The voltage spikes are exacerbated by increasing the switching frequency [52]. Other problems include duty cycle loss and pulse current at the input which increases the filter size.

2.2.3 Non-isolated DC- DC Boost Converter

Rather than the isolated converters, non-isolated DC-DC converters can be used to improve the efficiency. Consequently, the volume, weight and losses associated with the high-frequency transformer are reduced. Furthermore, in the high power application where weight size is the main concern, the transformer-less structure is the most attractive [23]. It is becoming a more suitable solution to employ non-isolated converters to reduce the system cost and improve the efficiency. Since the passive components size and weight of non-isolated converters vary inversely with frequency, the components then operate at converter switching frequency in tens of kilohertz (KHz) range or higher. This high frequency leads to dramatic reduction in converter size and weight. In summary, for applications that require isolation between source and load based on safety measures, the isolated topologies are the right choices. However, in high power applications where volume weight is the main concern, the non-isolated topologies are the best option. The basic non-isolated DC-DC step-up topologies that produce an output voltage higher in magnitude than the input voltage are the boost and buck-boost converters.

2.2.4 Conventional Non-isolated DC-DC Boost Converter

The conventional non-isolated DC-DC boost converter is shown in Figure 2.3. As the name implies the output voltage V_O is always higher in magnitude than the input voltage V_{in}. Higher

output voltage can be accomplished by controlling the operation of the switch using the PWM signal. Accordingly, the states of the switch (ON/OFF) are changed periodically with the period equal to T_{sw} (switching period) and duty ratio equal to D. The level of the converted voltage depends on the magnitude of the applied input voltage and the duty ratio.

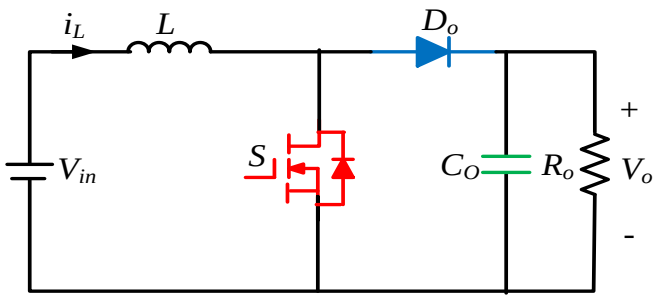

Figure 2.3 Conventional boost Converter

During the switch turn on instant, the diode D_O is reversed biased, and the input source charges the inductor L. When the switch turns off, the load receives energy from the input as well as the inductor. The capacitor C_O removes the switching harmonics from the applied input signal. Noticeably, the energy transfer in a step-up (boost) converter is between a voltage and current source. Since in a steady state, the capacitor or inductor can be represented by their instantaneous voltage or currents as an equivalent voltage and current sources respectively.

The steady state operation described is known as continuous conduction mode (CCM), since the inductor passes a current continuously without a break. However, if the inductor current became zero for part of the cycle as duty ratio D comes out of conduction, then this operation is called discontinuous conduction mode (DCM).

2.2.5 Limitations of Conventional Converters in High step-up Applications

The boost and buck-boost converters are the simplest PWM controlled topologies for voltage step-up. However, these converters typically operate under extreme duty ratio to achieve high voltage gain. As a consequence, significant voltage and current stresses are incurred by the power converter devices and poor dynamic characteristics can result in the controlled output response. Besides, the power device rating is proportional to the output voltage and a high rated power device potentially increases the conduction losses which also degrade the efficiency. Furthermore, the output diodes often sustain short, but high amplitude, current pulses due to the narrow turn off time; which induces reverse recovery losses.

2.3 Topology Evaluation for High step-up DC-DC Boost Converter

The major obstacle of improving the efficiency of the basic DC-DC converters such as boost and buck-boost in a high step-up application is extreme PWM duty ratio, conduction losses emanating from high rated power devices and reverse recovery related loss of the output diode. In view of these limitations, several work have been carried out to explore numerous topologies with potentials of improving the limitations of basic topologies such as static gain, power devices voltage stress, power density and efficiency. The next section focuses on evaluating these topologies and stating their advantages or disadvantages.

2.3.1 Cascade Converter

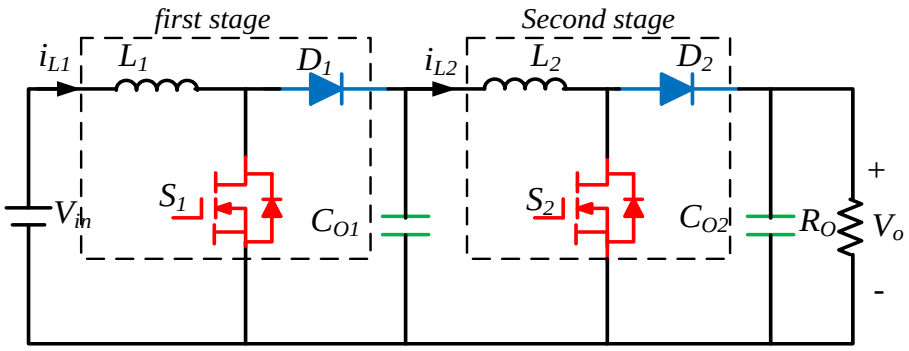

Figure 2.4 Cascade boost converter

The use of two DC-DC boost converters in cascade is an effective method of improving the static voltage gain [56]. It mainly involves connecting the output stage of a boost converter to the input of another boost converter, such that an intermediate bus voltage is developed around capacitor C_{O1} as illustrated in Figure 2.4. Effectively the cascade structure produces an output voltage which is a product of individual boost stages resulting in a higher static gain. By utilising the cascade structure each stage can achieve step-up function without extreme duty ratio operation, thus the conduction and switching losses are substantially reduced. The conduction loss of the first stage can be low, even though the input current is high. For the second stage, the input current is low due to the boost in voltage received from the intermediate bus voltage. However, the device voltage stress in the second stage is the same as the output voltage, and the reverse recovery loss of the output diode can be severe in high power applications. Another major drawback from the efficiency point of view is the energy is converted twice, which obviously has an impact on overall efficiency. Moreover, the interaction between the individually designed boost converters may cause instability in the

cascade converter from a small signal point of view [15].

Application of passive or active snubber cell to the cascade converter to implement (ZVS) for active switches as demonstrated in [36, 57], does not in any way improve the static gain of the original structure. The devices voltage stress usually remains the same with the original cascade structure despite (ZVS) soft switching performance.

2.3.2 Quadratic Boost Converter

In order to overcome the instability issue associated with the cascade connection of two individually designed boost converters, a quadratic converter is proposed in [37, 39, 58], by simply replacing switch S_1 in Figure 2.4 with a diode D_3. The quadratic converter operates as two conventional boost converters in series utilising a single switch as shown in Figure 2.5. The quadratic boost converter can achieve wide conversion ratio and, therefore, operate without extreme duty ratio, since the overall voltage gain is the product of the gain of the multiple stages.

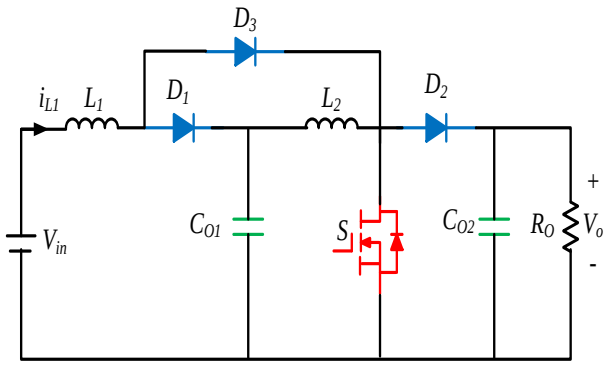

Figure 2.5 Quadratic boost converter

The main drawback of the quadratic boost converter is that the energy is converted twice similar to cascade converter. Furthermore, the power switch S and output diode D_2 voltage stress is the same with the output voltage; thus high rated devices are necessary in the converter which lead to conduction losses. In high power application, the reverse recovery problem of the output diode is a major concern. The use of quasi resonant cell in the power stage to implement soft commutation can be found in [59].

2.3.3 Three Level Boost Converter

Figure 2.6 shows the three level converter [38, 60, 61], and the circuit has an advantage of voltage stress distribution among the power devices. The device voltage stress is half of the

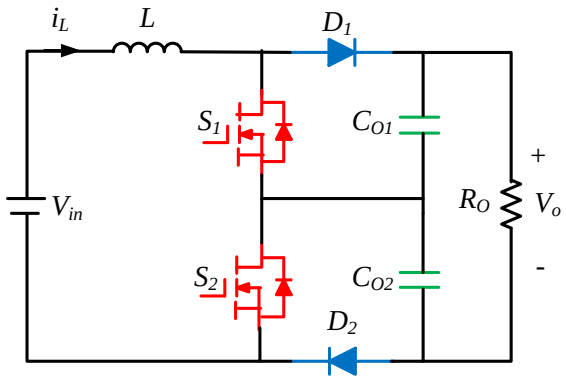

Figure 2.6 Three level boost converter

converter output voltage. Furthermore, the topology allows a significant reduction in inductor volume. These typical characteristics make it more suitable than the conventional boost converter in voltage step-up applications. With low voltage stress across the device, a high-performance MOSFET with low on state resistance can be employed to reduce the conduction loss. The switching loss is significantly reduced being a function of the voltage across the device and electro-magnetic interference (EMI) noise is suppressed.

The main drawback of this topology is that the voltage gain is the same as conventional boost converter as such it is not adequate in many modern applications that require higher conversion ratio of ten times or higher. For this reason, the converter must operate at extreme duty ratio to achieve higher conversion ratio and the diodes reverse recovery losses is another concern. Furthermore, the ripple current is large in high power applications.

2.3.4 Voltage Multiplier Cell

An alternative technique to overcome the limitation of classical boost and buck-boost DC-DC converters for high performance and high conversion ratio applications is by use of voltage multiplier cells [23]. The use of voltage multiplier in both low and high frequency isolated DC-DC converters can be traced to Travelling Wave Tube Amplifiers (TWTA), mainly for high voltage gain [62]. The inclusion of the voltage multiplier cell is to reduce the problems of mass, volume and losses associated with the high voltage power transformers. Figure 2.7 shows the basic structure of voltage multiplier cell.

The voltage multiplier cell is another classical use of capacitor charge transference which produces an output voltage higher in magnitude than the input voltage without the use of the magnetic element. The voltage multiplier cell can be inserted into classical converters such as buck, boost and buck-boost to implement high step down or high step-up converters [23]. The

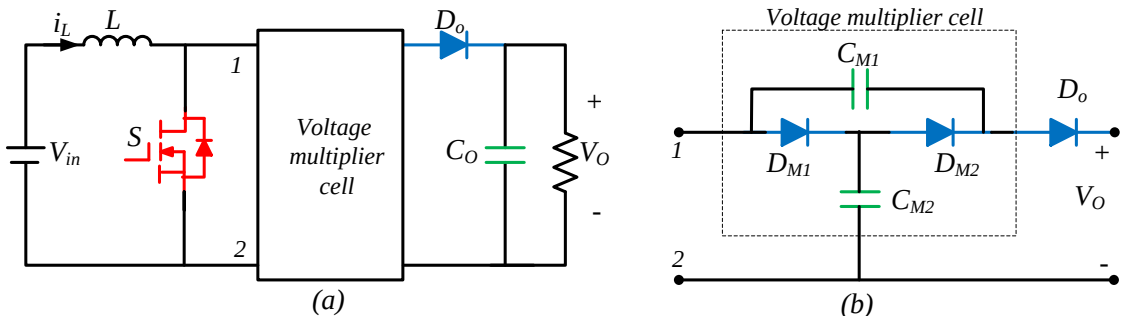

Figure 2.7 Boost converter with voltage multiplier cell
(a) Converter structure (b) voltage multiplier cell

new structure obtained is the same with all basic topologies. It is worth mentioning that insertion of the voltage multiplier cell in buck converter does not offer any practical advantage. When the power switch turns on, the input inductor stores energy and when the power switch turns off, the inductor releases its energy to the output via capacitor C_{M1}. Thus, C_{M1} and C_{M2} discharges in series to the output. The power switch voltage stress depends on the number of voltage multiplier cells and reduces as the number of the cells increases. The maximum voltage stress in the multiplier diodes and power switch is equal to half of the output voltage. Higher static gain is possible by employing more voltage multiplier cells at the expense of complexity, cost and a quite substantial amount of diode forward voltage drop. It is worth mentioning that insertion of the voltage multiplier cell in buck converter does not offer any practical advantage.

2.3.5 Switched Capacitor/Switched Inductor Techniques

The switched capacitor/ switched inductor technique [40] allow achieving steep voltage gain in classical converters. The method uses capacitor/ inductor charge transference to step-up the input voltage. A switching cell formed by either two capacitors and two-three diodes, or two inductors and two-three diodes are combined with classical converters to get a steep function. Depending on the cell configuration, the structures can be of two types: step-up and step down, only step-up is considered here. When the converter primary switch is conducting, the two inductors in the switch inductor cell are charged in parallel, or the capacitors in the switch capacitor cell are discharged in series. When the converter primary switch turns-off, the two inductors are discharged in series or the two capacitors are charged in parallel.

Figure 2.8(a) shows the switched capacitor converter structure and the switched capacitor cell is shown in Figure 2.8(b). The switched capacitor circuit can provide a step-up function of the input voltage based on capacitor charge transference, when inserted in classical boost or buck-

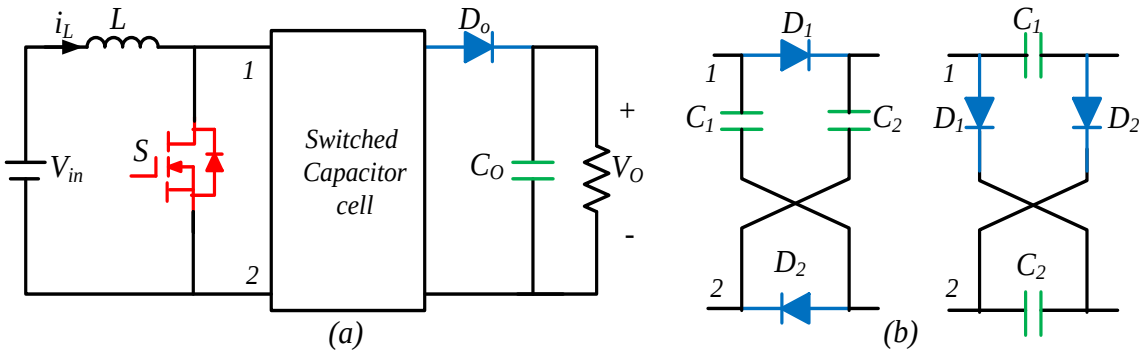

Figure 2.8 Switched capacitor structure
(a) Converter structure (b) Switched capacitor cell topologies

boost converters [40, 63]. The diodes in the cell are forward conducting when the converter switch is turned off, thus, the two capacitors in the switch cell are charged in parallel by the converter input voltage. During the switch turn on instant, the diodes are reverse blocking, and the capacitors are discharged in series. Switched capacitor cell can increase the voltage gain and reduced the device voltage stress [64].

Another famous circuit that utilises switched capacitor circuit is the charge pump and has been used in DC-DC power conversion for a long time especially in the management of integrated circuits. Charge pumps circuit operate based on capacitor charge transference and do not contain inductors [49, 64, 65]. The operation of the power switches in the converter is dictated by PWM duty ratio. Switched capacitor technique permit developing compact, lightweight converter, and the output voltage depends on the number of capacitors used. The efficiency of the converter is significantly reduced when a constant output voltage is required; due to a high pulse current which occurs at switching transient and raise the EMI labels [66]. In high step-up application, the circuit becomes complex with more diode forward voltage drops. Moreover, the number of active devices and their associated gate drives increases both the cost and complexity and the converter is limited to low power application.

On the other hand, the switched inductor cell is formed by two inductors instead of capacitors and 2-3 diodes [40]. The switch inductor cell can as well provide step-up of the input voltage when combined with classical converters such as boost, buck-boost, zeta and sepic converters to create a new power supply. Figure 2.9(a) shows the structure of boost converter with switched inductor cell. Figure 2.9(b) illustrates a typical switched inductor cell. When the converter active switch is on, the diodes D_1 and D_2 became forward biased and the two inductors in the switch inductor cell are charged in parallel. During the switch turn off instant, the diodes D_1 and D_2 became reversed biased whilst D_3 become forward biased. Thus, the two inductors discharged in series. Incorporation of switched inductor cell in the classical

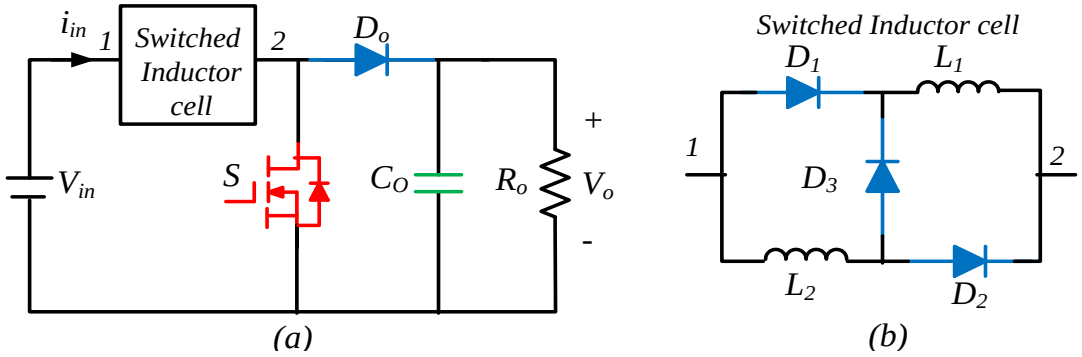

Figure 2.9 Switched inductor structure
(a) Converter structure (b) switched inductor cell

converters provides a means of increasing the voltage gain, however, static gains of ten times or higher is not feasible without higher duty ratio. In addition, the device voltage stress is the same as the converter output voltage resulting in dominant conduction losses and severe reverse recovery problems limiting its use to low power applications.

2.3.6 Voltage Lift Circuit

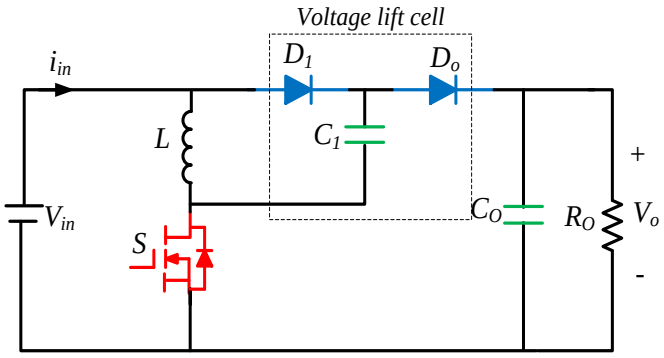

Figure 2.10 Voltage lift converter

Voltage lift technique has been successfully applied in DC-DC converters to implement a series of high voltage and wide conversion ratio [41, 42, 67-69]. The output voltage of a DC-DC converters employing voltage lift technique increases in stage by stage along arithmetic progression [42]. Figure 2.10 shows the voltage lift cell inserted in a conventional boost converter. Boost converter consisting of a single voltage lift cell has a simple structure and fewer components.

In simple term the inductor and the capacitor in the voltage lift cell are charged by the input voltage during the switch on period and both of the capacitors and inductor discharge their respective stored energy in series to the output when the converter switch turns off. The main drawback is that the converter has lower static gain and operates with higher duty ratio

operation. Although it is possible to combine multiple lift circuits to push up the static gain, however, the increase in the voltage transfer gain in all cases is obtainable with a significant increase in the number of passive components. Furthermore, the switch voltage stress is the difference between the output and input voltages.

Super lift [41, 67] is another technique of making the output voltage of DC-DC converter increasing in stages along geometric progression with either positive [41] or negative [67]. Effectively the voltage conversion ratio is achieved via power series. Further improvement in voltage gain along a power law is demonstrated in [68] by splitting a capacitor or an inductor. Similar work of improving the static gain in positive output super lift Luo converter by replacing the inductor with switched inductor is presented in [69]. This modification permits realising double increase in the line-to-output voltage ratio at the high values of the duty cycle. However, extreme duty cycle operation results in narrow turn off period of the switch. The output diode conducts a pulse current with high amplitude leading to severe reverse recovery related losses [14].

2.3.7 Active Network

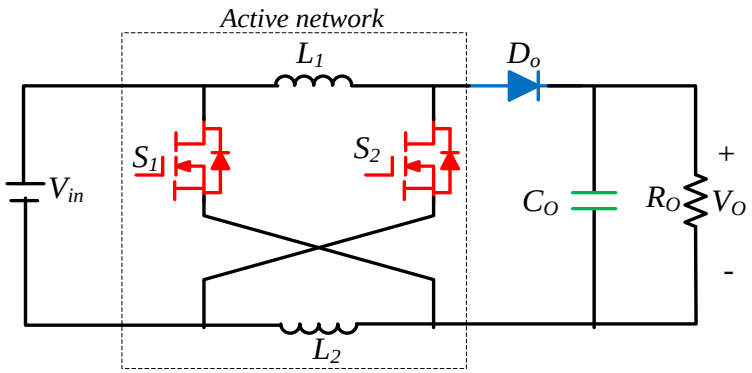

Figure 2.11 Active network converter

The operation of the active network converter is similar to the switch inductor cell [40]. The modification arose from eliminating diode D_3 from the switched inductor cell in Figure 2.9 (switched inductor converter) and replacing the remaining diodes D_1 and D_2 with an active switch as shown in Figure 2.11. The active network converter makes use of two inductors which can be integrated on the same magnetic core resulting in simpler and compact topology. The two inductors are charged in parallel when the active switches turns-on and discharged in series during the switches turn-off period, hence the name active network. The two active switches operate with the same PWM duty ratio [42].

The main drawback of this technique is that the switched inductor converters left alone cannot provide wide conversion ratio. This is related to the fact that the two inductors stores energy similar in magnitude to the input voltage. Therefore, the active network converter provides an output voltage which is only three times higher than the input voltage [42]. This voltage gain is far less than the gain required by many applications. In addition, the output diode voltage stress is more than the output voltage, which can lead to reverse recovery losses in high power application. Besides, utilising active switches that are not connected to the same reference node makes the drive circuitry complex.

Extending the static gain of the converter is demonstrated in [42] by integrating the active network converter with a voltage lift cell [41]. Others include switched capacitor active network converter [70], substituting the conventional inductors with coupled inductors in an active network converter [71] and multi-cell switched-inductor/switched-capacitor combined active-network converters [72] mainly to extend the voltage gain.

2.3.8 Transformer Based DC-DC Converters

The transformer is widely used in electrical circuits to step-up or step-down voltage from one level to another and transfer energy between the source and the load with or without galvanic isolation. In the majority of applications, transformers provide an impedance matching between the source and the load. In many applications, it is desired to incorporate a transformer into the switching DC-DC converter to obtain a series of step-up wide range voltage conversion ratio. By adjusting the turns ratio of the magnetic element extreme duty ratio operation can be avoided. Another advantage is that the transformer based converter makes the power switch voltage stress far less than the output voltage. This feature allows low voltage rated power devices with low on state resistance to be employed in order to reduce the conduction loss. The inherent leakage inductance can be used to control the current falling rate of the diode, thus minimising the reverse recovery related loss. Adding multiple secondary winding provide a means of obtaining multiple DC outputs. In some DC-DC converters (such as flyback and forward) a transformer performs a dual function; one is energy storage and two is voltage step-up using the transformation ratio. Theoretically, reducing the magnetic components count. Nevertheless, a transformer provides means of enlarging the voltage gain in other topologies (such as full and half bridge converters).

Various high step-up topologies using magnetic means were reported in the literature [10, 43, 44, 48, 50, 73-75]. High static gain (ten times or higher) can be achieved by adjusting the

turns ratio. However, higher turns ratio implies winding losses and volume. Besides, the volume, weight and losses of the transformer are the limiting factors of producing compact and efficient converter. Furthermore, the leakage inductance of transformers induces high turn off voltage spike on the power device which increases the switching losses, EMI problems which consequently degrades the converter efficiency. The transformer primary current is large in high power application. In addition, the output diode voltage stress is very high leading to the use of high rated power diodes with low switching speed [10, 73, 74]

2.3.9 Stacked DC-DC Converters

DC-DC converter stacking is the technique of arranging the capacitor voltages of a converter in series to obtain a higher output voltage which is the sum of nominal capacitor voltages connected in series. Many isolated converters such as current fed converter have been proved as suitable candidates for a high step-up application. A new non-isolated converter topology can be configured from the isolated converter to produce higher conversion ratio by stacking the secondary output side upon the primary output side [44, 76-81]. A high static gain is obtained because the output is in series. The advantages of this concept include distribution of the voltage stress on the semiconductor devices, direct leakage inductance energy recycling to the output side and high static gain. In addition, the secondary side voltage stress is also reduced significantly, since the power diodes voltage stress is the difference between the input voltage and the overall output voltage. This configuration allows part of the power to be directly transferred from the source to the output, leaving the rest of the power to be handled by the converter. The overall efficiency of the converter is improved when the converter manages the power.

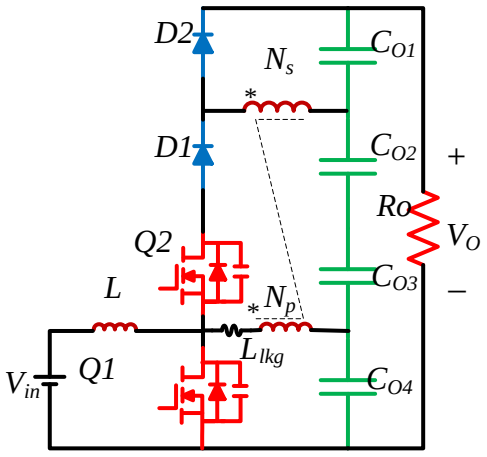

Figure 2.12 Non-isolated stacked converter structure [82]

Figure 2.12 illustrate the stacked converter structure.The simplest topology is the boost flyback converter proposed in [82], derived by combining the conventional boost converter with the flyback converter. Both converters use single a switch and the boost inductor, and the transformer of the flyback are replaced with a coupled inductor. The boost converter acts as clamp circuit to depress the leakage inductance energy. A similar approach of stacking boost converter with sepic converter is described in [78]. Sepic integrated boost converter provides an additional step-up gain with the help of an isolated sepic converter since both the boost and sepic converters share the filter inductor and single power switch.

Other solutions that supplement the insufficient static gain and distribute the voltage stress are demonstrated in [4, 46, 83]. A voltage multiplier cell is usually incorporated to enlarge the voltage gain.

The major drawback of this approach is when a higher static gain is required the voltage stress distribution in the secondary side is no longer the case since most of the voltage stress is impressed on the secondary side. Besides, the audio susceptibility is high due to the direct connection of the input source to the output. Another concern is voltage balance of the output capacitors due to series connection.

2.3.10 Integrated Converters

At higher output voltage level, the CCM high step-up boost converter is the preferred topology for implementing a front-end converter. It has been mentioned in the preceding sections that high-efficiency is the most needed performance in all applications. It is worth noting that neither the capacitive nor the magnetic means can achieve higher conversion ratio without certain shortcomings. The former technique is based on capacitor charge transference and is successfully applied in voltage multiplier, voltage lift, switched capacitor, etc., mainly for increasing the voltage gain. Moreover, the increase in the voltage gain in all cases is obtainable with a significant increase in the number of passive components. Series connection of cells makes the whole circuit complex with additional current stresses. Whilst the latter (magnetic means) requires higher secondary turns ratio which implies volume, weight, losses which are inimical to achieving highly efficient converter. High-efficiency, high step-up converters have been the focus for many researchers, and a significant number of techniques/topologies have been proposed to this end. Majority of these topologies have been focused on integrating or combining the magnetic means and capacitive means to realise high static gain. The benefits of integrating the two techniques can be explained in threefold. First,

lower turns ratio could be used to configure the gain extension cell with appropriate duty ratio since proper duty ratio operation can result in achieving desired operating point without incurring excessive current or voltage stresses. Second, the integration allow utilisation of low power rated devices with low on-state-resistance to reduce the conduction losses. Third, the inherent leakage inductance of the transformer could be used to control the current falling rate of the output diodes and achieve soft switching operation. It is well established in the literature that minimising the reverse recovery characteristics of the diode enhances the conversion efficiency and electromagnetic interference (EMI) significantly [13, 14]. The integrated converter would, therefore, result in simple, compact converter with low parts count. So far, many high step-up boost converters using magnetic and capacitive means have been proposed. They include high step-up boost converters with coupled inductor and voltage multiplier cells [47, 50, 84-86], coupled inductor and switched capacitor techniques [76, 87-89], integrating three-state switching cell and auto transformer [90], three-state switching cell and voltage multiplier cell [91].

The main caharcteristics of the integrated topologies are:

1. Proper duty ratio operation is made possible using the transformation ratio of the magnetic elements, and the output voltage can be further step-up by adjusting the turns ratio.
2. The converter passive components including the transformer operate at the converter switching frequency which permits a reduction in weight and volume.
3. By proper choice of the turns ratio, voltage stress across the devices is far less than the output voltage, allowing low rated power devices with low on-state resistance to reduce the conduction losses. Likewise the current stress imposed on the power devices is also minimized, leading to improved efficiency.
4. The turn off voltage spike caused by the leakage inductance energy interaction with parasitic capacitance of the primary switch conventionally required a snubber.
5. The current falling rate of the diode can be controlled using inherent leakage inductance of the magnetic element.

Literature shows that the active and passive clamp solutions are the most widely employed approach for recycling the transformer leakage energy in DC-DC converters. Note that the main advantage of active clamp circuits is recycling the leakage inductance energy and also provides a mecahnism of achieving (ZVS) of the main and clamp switch [48, 50, 73, 74]. Sometimes, zero voltage transition (ZVT) of all the active devices can be achieved [50]. The

passive clamp circuits are effective in depressing the power device voltage excursion due to leakage energy. Nevertheless, the passive circuits [43, 70, 75, 76] do not offer (ZVS) of the main switch. However, this does not in any way compromise the conversion efficiency. The downside of the transformer/coupled inductor based converters is large input current ripple in high power applications due to the operation of the coupled inductor.

To increase the power density of the state of the art high step-up boost DC-DC converters, multiphase current interleaving technique has been reported [4, 23, 45, 46, 83, 92-103]. It has been demonstrated that interleaved converters have the advantage of lower device current stress and better efficiency. Interleaved structure is an effective solution of reducing the current ripple, miniaturising the passive components and improving the transient response of a converter. The interleaved structure can only share the converter input current so as to increase the power density, but not to enlarge the voltage gain. High static gain is possible in interleaved DC-DC converters by utilising switched capacitor cell, voltage multiplier cell, transformer turns ratio or their combinations [23, 46].

2.4 High Step-up DC-DC Converters Platforms

This section outlines the general platform for developing high step-up converters with wide conversion ratio. The platform consists of voltage gain extension cell that integrates capacitor charge transference and magnetic means. For example, a switched capacitor and coupled inductor can be integrated to configure the voltage gain extension cell. This cell can be inserted between the power switch and diodes of the conventional boost converter to realize high step-up boost converter platform. The typical platform is shown in Figure 2.13.

Due to this voltage extension cell, the main limitations of a basic converter in a high step-up application such as extreme duty ratio operation can be overcome. By proper choice of the turns ratio, the current or voltage stresses imposed on power devices can be dramatically reduced. Consequently, low rated MOSFET with low on-state-resistance can be employed to reduce the conduction losses. In order to increase the power density of high step-up converter, the voltage gain extension cell can as well be inserted in an interleaved structure as shown in Figure 2.14. This platform for the high step-up converter is deduced from proposed concepts introduced in [47, 50, 76, 84-89] and [4, 23, 45-47, 83, 92-103] for single phase and interleaved converters respectively. Also, this platform can be utilised to drive the future high step-up boost converters.

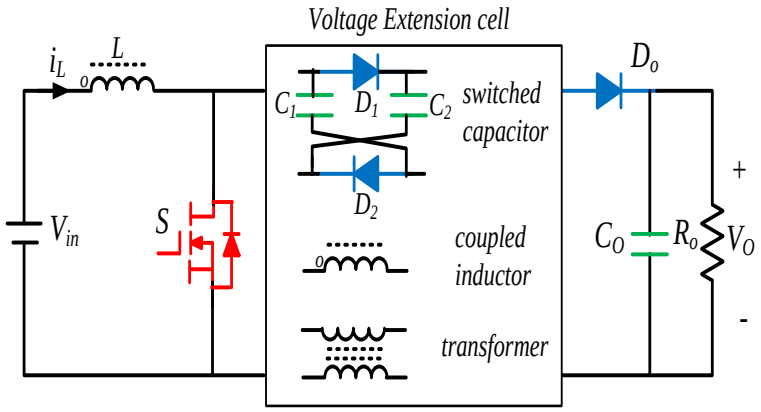

Figure 2.13 Typical circuit for high step-up dc-dc conversion

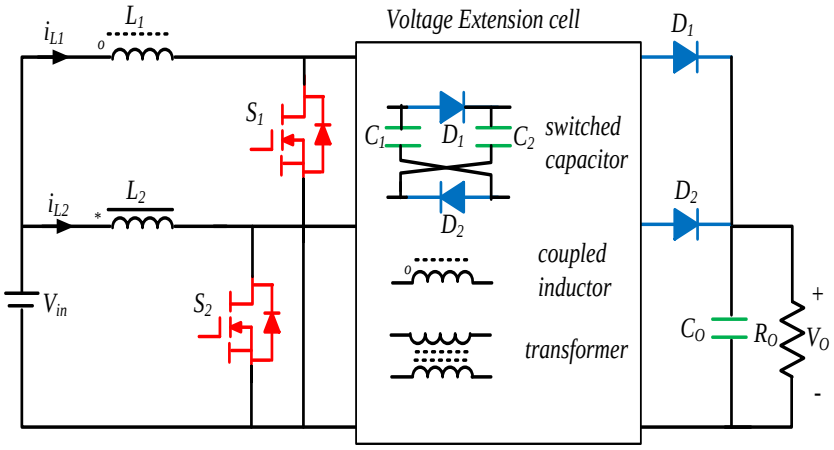

Figure 2.14 Typical circuit for interleaved high step-up dc-dc conversion

2.5 Classification of Non-isolated DC-DC Boost Converters

Several high step-up DC-DC converters have been proposed in the literature for the purpose of improving key issues associated with conventional topologies, such as efficiency, static gain and power handling capability. State of the art techniques include interleaving, magnetic/capacitor charge transference and their variations. Coveters can be further classified as those with or without wide voltage conversion ratio.

2.5.1 Step-up Converters without Wide Voltage gain

Basic boost and buck boost converters are the typical topologies without wide conversion ratio. They have only one degree of freedom (duty cycle) to enlarge the voltage gain. Other topologies without wide conversion ratio includes conventional interleaved, three level boost converters. Figure 2.15 shows the classification of the converters without wide voltage gain.

2.5.2 Step-up Converters with Wide Voltage gain

Wide conversion ratio non-isolated boost converters possess bi-degree of freedom to enlarge the voltage gain. DC-DC converters with wide conversion ratio usually employ magnetic or capacitive means. Integrating magnetic and capacitor charge transference is another technique of realising topologies with wide conversion ratio. Figure 2.15 illustrates the family tree of high step-up converters with wide conversion ratio.

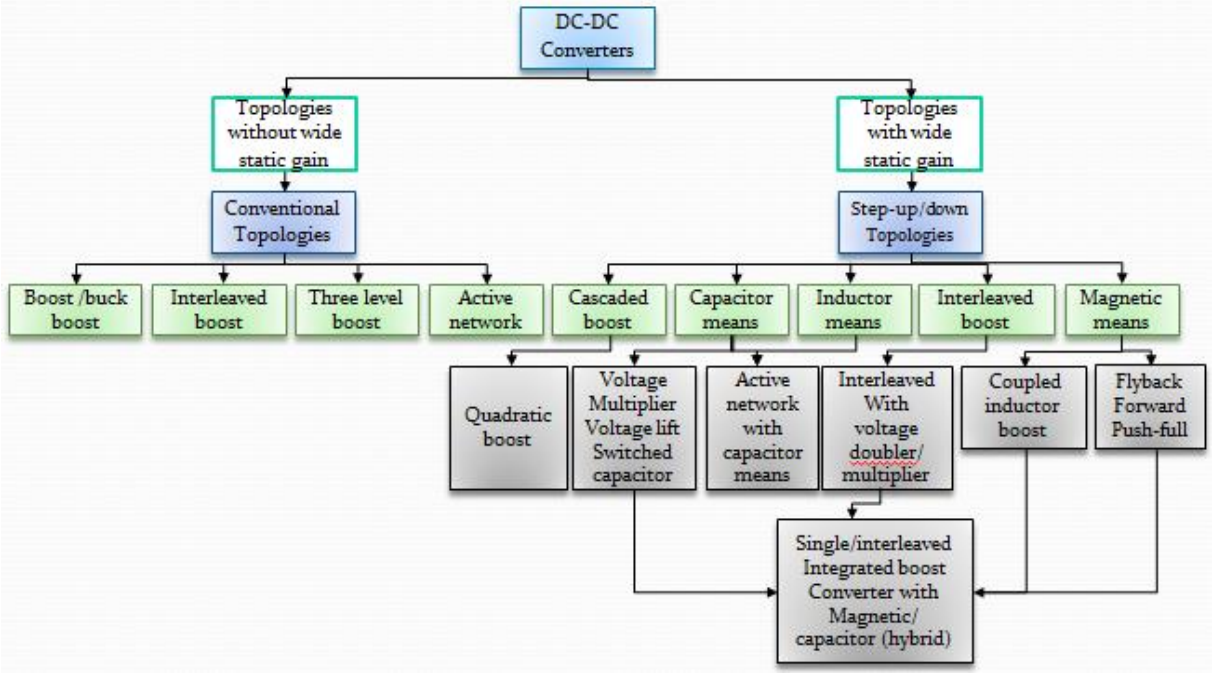

Figure 2.15 Classification of step-up converters

2.6 High Switching Frequency Operation

To accommodate the ever-increasing demand for compact and high efficient power supply, there is need to push the operating frequency of the switch-mode power supply. Since the volume and weight of all the passive components are function of switching frequency. High-frequency operation ultimately reduces the passive components size such as transformer, inductor and capacitor drastically. Increased speed, higher voltage or current ratings and a relatively low cost of these devices are the other factors that have contributed to the emergence of switch mode power supply. However, these benefits of switch-mode power converter come at the cost of higher complexity, hard switching operation which involves higher switching losses and EMI noise. These problems are the major factors that inhibit PWM converters from operating at higher operating frequency. Any attempt to push the operating frequency to design compact, high-performance system, the switching loses are

further aggravated which ultimately compromises the converter efficiency. Although the power devices are capable of being operated at a higher frequency, these problems pose a practical upper limit on the operating frequency.

However, reducing the operating frequency is not a good solution regarding power density and cost. As the operating frequency increases so does the switching losses. The switching losses are mainly caused by abrupt turn-on of the switch which causes the energy store in the parasitic capacitance of the device to dissipate within the device. In practice, when a power device makes an instantaneous switching transition (from on to off and vice versa), an overlap exist between current and voltage waveforms [13, 51]. A typical switching trajectory of hard switching power device is shown in Figure 2.16.

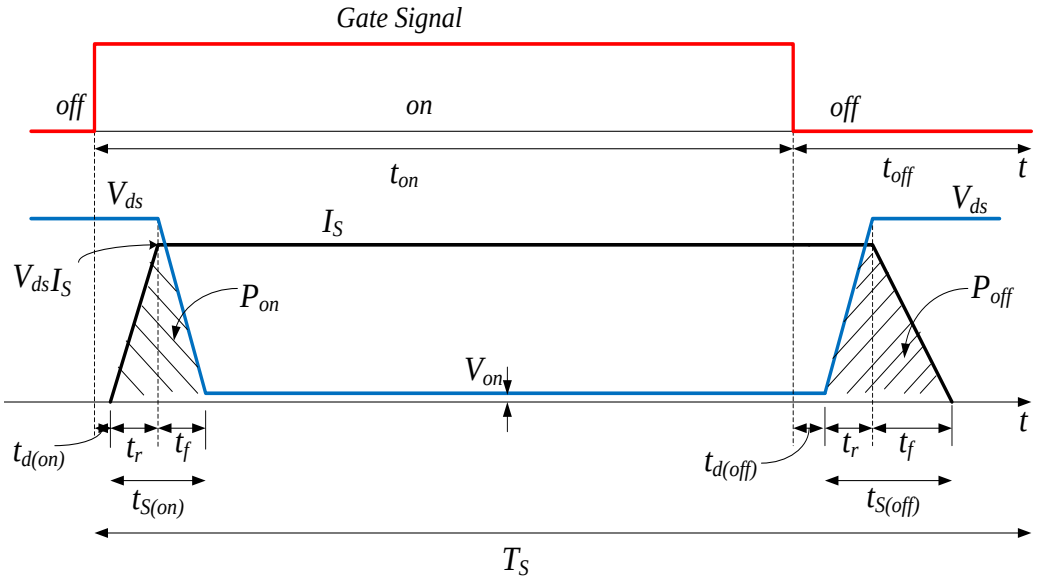

Figure 2.16 Typical linearized switching trajectory of power device

By applying a positive gate signal to the switch; during turn on instant the current build up consist of a short delay $t_{d(on)}$ followed by the rise time t_r. After a finite time duration the current flow through the switch and the switch voltage drop to a small on state value V_{on} with a fall time t_f. The shaded area indicates an overlap of switch voltage and current during switching transition $t_{S(on)}$, $t_{S(off)}$, which denotes power loss during each period. Since power loss depends on the product of voltage and current. The energy dissipated within the device during the switching transition is denoted by P_{on} and P_{off} respectively. These losses are referred to as switching losses and are proportional to the switching frequency.

Since the efficiency of the power converter is the most needed performance and to achieve higher efficiency, a way to reduce or eliminate the switching losses must be conceived.

Passive turn-on and turn-off snubbers are used to control the rate of rising of voltage or current during switching transitions, clamp voltage overshoot and minimize switching losses. However, snubbers only transfer the losses from switch to the snubber capacitor, and, therefore, do not result in overall reduction of the losses [10, 16]. Switching condition of semiconductor devices in switch mode power supply can be further improved by incorporating certain resonant circuit in PWM converter [59, 104-106]. This modification reduces the switching loss and allows the converter to operate with higher switching frequency. But at the expense of increased circulating current which further increases conduction losses. Another major drawback of the resonant converters is variable frequency operation which makes the design of the passive components difficult [105].

Soft switching is a compromise between the PWM and resonant converter and is targeted towards minimizing the switching losses without a significant increase in circulating current. Soft switching combines the resonant and PWM technique to soften the switching transition and reduce circulating current with fixed switching frequency operation [16, 57, 73, 107]. Soft switching performance is realized with energy recovery snubbers, in which the energy stored in the snubber capacitor or inductor is transferred to the source or load, instead of being dissipated. At any instant the switch is made to change its state (from off to on and vice versa) when either voltage across it or current through it is zero, which minimizes the power loss in the device; such switching action is termed as the soft switching. In zero-voltage-switching (ZVS), the switch changes its state when the voltage across it is zero, whereas in zero-current-switching (ZCS), the switch changes its state when current through it is zero. The (ZVS) or (ZCS), are collectively referred to as soft switching, and can be realized in different ways, which are further described in the subsequent section.

2.7 Soft Switching Performance in High Step-up Converters

In switch mode power converters, the power semiconductors turn-on and turn-off under hard switching condition resulting in switching losses and stress. The switching loss is proportional to the switching frequency, overcoming the problem of switching loss allows higher switching frequency operation in power converters. Various techniques such as passive snubbers, resonant and soft switching techniques can be implemented in the power stages to improve the efficiency of the converters. The concept of soft switching is built around combining the advantages of conventional PWM technique and resonant technique. The soft-switched converter utilizes the resonance in a controlled manner, such that the resonance

occurs prior to the turn-on and turn-off instances so as to create (ZVS) and (ZCS) conditions. At all other instances, the converter behaves like a conventional PWM converter. A soft switching technique provides an effective solution of suppressing EMI and has been successfully applied to converters, inverters and rectifiers. (ZVS), (ZCS) and voltage clamping are the emphasis of the next sections [108, 109].

2.7.1 Zero Voltage Switching (ZVS) Technique

The objective of the technique is to use resonance to force the voltage across the device to zero prior to its turn-on or turn-off. A (ZVS) turn-on is implemented by discharging the parasitic capacitor and subsequently forcing the antiparallel diode of the device to conduct prior to the application of the gate signal. Therefore, the switch turns-on with only antiparallel diode voltage drop. A (ZVS) turn-off is achieved sometimes by adding a capacitor across the switch to limits the overlap between the voltage and current during turn-off. If the switch voltage waveform is shaped during turn-on and turn-off period (i.e. switching transition) to create a (ZVS) condition, such phenomenon is called zero voltage transition (ZVT).

MOSFET is used in a medium power, suitable for high switching frequency applications and have significant drain source capacitance; they are mostly used in (ZVS) circuits. An external snubber capacitor is often added to drain-source capacitance to ensure (ZVS) turn-off. To ensure (ZVS) turn-on of the device a negative current usually discharges the snubber capacitor and makes the antiparallel diode conduct so that the device can turn-on with (ZVS) condition.

2.7.2 Zero Current Switching (ZCS) Technique

(ZCS) is another technique similar to (ZVS) that uses resonance to force the current following through the switch to zero during turn-on or off. A (ZCS) turn-on is implemented by including a small inductor in series with the switch that controls the rise of the current when the switch turn-on. During turn-on, the switch current increases linearly from zero. Finally, the switch can be commutated at the next zero current duration. Likewise, if the switch current waveform is shaped during turn-on and turn-off period (i.e. switching transition) to create a (ZCS) condition, such phenomenon is called zero current transition (ZCT). The major drawback of MOSFET when used to implement (ZCS) is the capacitive turn-on losses and high current stress. IGBT is a minority carrier device, have large tail current in the turn-off process. Thus, (ZCS) are useful particularly in minimizing the switching loss for power

devices such as IGBT.

2.7.3 Voltage Clamping

In a transformer based DC-DC converter, the interaction between leakage inductance and the parasitic capacitor of the switch induces high voltage stress to the primary switch and traditionally requires a snubber. RCD snubber can be used to limit to switch voltage excursion, however, the energy recovered is dissipated as heat within the snubber. To overcome the limitation of the RCD snubber, a clamp circuit can be incorporated in the power stage to limit the turn-off voltage spike of the switch and recycle the leakage energy. This approach makes use of either passive clamp circuit (composed of a diode and a capacitor) [10, 55] or the active clamp circuit (composed of a switch and a capacitor) [46, 48, 50, 73, 110]. The leakage inductance energy is transferred to the clamp capacitor during the primary switch turn-off period and subsequently recycled to the output. The clamp circuit is always off during boost mode and in series with the primary converter switch. The active clamp circuit not only resets the leakage energy but also realizes (ZVS) for all the active switches [46, 48, 50, 73, 110]. The downside of this method is a significant amount of conduction loss due to circulating current flowing through the clamp switch or its antiparallel diode.

2.8 Reverse Recovery Characteristic of Output Diode

The CCM of operation is the preferred method of operating boost converter. However, if a boost converter operates under CCM, the reverse recovery current of the output diode has a detrimental effect on the performance of the converter. This is related to fact that once a diode is conducting, and suddenly its forward current reduces to zero (as a result of application of reverse voltage), the diode continues to conducts due to the minority carriers that remain stored within the p-n junction (depletion region of the junction) and bulk semiconductor material. This phenomenon requires a certain time for the minority carriers to recombine with the opposite charges and become neutralized [13]. The reverse recovery time induces more turn on loss to the power switch, which consequently, increases the switching losses and compromises the converter efficiency.

Significant efforts have been made in recent years to improve the efficiency of the high step-up boost converters. One of the key focuses is on alleviating the adverse effect of output diode reverse recovery problem on the conversion efficiency and electromagnetic interference EMI.

The efficiency of CCM boost converter can be significantly improved if the output diodes could be turned off softly [111]. The recent state of the art solutions involve turning the diode off softly by controlling the current falling rate of the diode during turn off with the aid of additional components to form active snubber [104, 112, 113] or passive snubber [114, 115]. The active snubber employs an active auxiliary switch and passive components such as capacitors, inductors, and diodes whilst the passive snubber uses only the passive components.

Besides soft switching turn off of the diode, the active snubber has another advantage of implementing (ZVS) of the main switch. However, adding a snubber circuit with active switch increases the complexity of the converter. Also the active snubber exhibit voltage and current stresses on the devices. The passive snubber behaves in a similar way with the active counterpart with exception of (ZVS) soft switching performance. The main drawback of the snubber circuits is significant current and voltage stresses are incurred by the primary switch which necessitates the use of higher rated components [114, 115].

Another approach involves shifting the output diode current to another branch with additional switch and passive component to form an active snubber [111]. The snubber uses only three components to offer soft switching of both the output diode and the added switch at no extra current or voltage stress. This technique produces higher efficiency, because the power loss in the branch is less. The main drawback of this approach is the circulating current in the auxiliary switch increases the conduction loss. Also overlapping between the driver signal of the main switch and auxiliary switch usually leads to short circuit and the overall failure of the circuit.

A simple and effective method to control the current falling rate of the output diode in CCM boost converter is proposed in [116]. The technique suggests shifting the diode current to a new branch. The new branch consists of a diode and secondary winding of a coupled inductor. Literature shows that a boost converter can achieve current steering using the leakage inductance of the coupled inductor. The current falling rate of both diodes is controlled with no additional current or voltage stresses.

2.9 Summary

The major concern related to efficiency of basic non-isolated converters in high step-up applications, such as boost and buck-boost, is the extreme duty ratio operation. Consequently,

high voltage and current stresses are incurred by the semiconductor devices which ultimately compromise the efficiency. Within this context, this chapter presented an extensive review of the techniques of achieving a high static gain in non-isolated DC-DC boost converters.

Various methods used in developing high step-up boost converters have been described, considering that the increase in the output voltage of the boost based converters must not rely on the duty cycle. Three level converter, cascade boost converter and quadratic converter can avoid extreme duty operation. However, their applications are limited to low power level. With capacitor charge transference methods it is possible to achieve high voltage gain, but a trade-off is necessary regarding part count and efficiency. Converters with coupled inductors can easily achieve high output voltage by utilising the transformer function. However, a clamp circuit is necessary to handle the leakage energy. The high step-up conversion techniques are demonstrated and explained using their respective circuit diagram, the voltage extension cell or both.

In practice, the most widely used methods of achieving high voltage gain in DC-DC converters are magnetic and capacitive means. Nevertheless, the aforementioned methods can be integrated to configure a higher voltage gain DC-DC converter. For the state of the art high step-up boost DC-DC converters to increase its power density, multiphase current interleaving technique is usually employed.

In order to produce a compact converter high switching frequency operation has been suggested in the literature. However, higher switching frequency operation introduces switching losses. In order to reduce the switching losses and improve the efficiency, an active or passive soft switching scheme can be employed to achieve (ZVS) or (ZCS). The reverse recovery current of the output diode has a detrimental effect on the performance of the converter. State of the art solutions involves turning the diode off softly by controlling the current falling rate of the diode during turn off with the aid of additional components. Based on the preceding revision, the major challenges in high step-up converters are: extreme duty cycle operation, high voltage and current stresses, switching losses and reverse recovery problem of the output diode. The concept of developing high-efficiency, high step-up boost converters is reviewed, and a clear picture and platforms of the future non-isolated high step-up DC-DC converter is made in this chapter.

Chapter 3

Single phase Converter Steady State Analysis and Design

3.1 Introduction

A non-isolated high step-up converter can be developed by incorporating a voltage gain extension cell which integrates switched capacitor and a transformer [23, 43, 48, 50] see a typical platform in Figure 2.13. The use of voltage gain extension cell is to overcome the limitations of basic topologies in high step-up DC-DC conversion. Depending on the configuration, the voltage gain extension cell is a classical use of capacitor charge transference in conjunction with transformer turns ratio. This structure usually produces a static gain of ten times or higher required by many emerging applications. High-frequency operation permits reduction of the passive components size, but at the expense of increased switching losses. Soft switching techniques can be implemented in the power stage to improve the efficiency [23, 43, 48, 50, 117, 118] since the converter efficiency is the most desirable performance in all applications. As previously explained, the application of passive or active clamping schemes in the converter power stage circuit to implement soft switching performance does not alter the performance of the original structure regarding the static gain.

This chapter presents a single-phase DC-DC converter topology proposed with the objective of achieving ten times voltage gain and low voltage stress on semiconductors. In order to achieve this goal, a voltage gain extension cell configured by integrating coupled inductor and switched capacitor is inserted in a conventional boost converter. The topology introduced in this chapter is deduced from the high step-up converter platform in chapter 2. The coupled inductor perform dual function, energy storage and voltage gain extension. The voltage extension cell comprises of two capacitors, coupled inductor secondary winding, a diode and auxiliary switch. The two capacitors are charged in parallel and discharged in series to enlarge the voltage gain when the coupled inductor operates as a transformer in flyback and forward

mode. Furthermore, the leakage inductance of the coupled inductor is utilised in alleviating the reverse recovery problem of the diodes and achieving (ZVS) for all active devices. An active clamp circuit is employed to suppress the leakage energy of the coupled inductor and to clamp the voltage level of the active switches. The operating principles along with the design example are described in detail. Experimental results from a 250 W prototype are included to validate the effectiveness of the proposed topology in a high step-up application.

3.2 Proposed Converter and Operational Principle

3.2.1 Circuit Configuration and Description

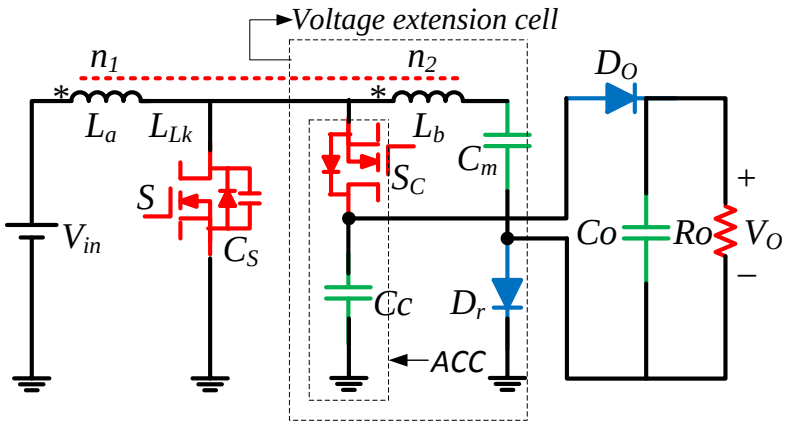

Figure 3.1 Circuit configuration of the proposed converter

Figure 3.1 shows the circuit configuration of the proposed soft-switching single phase high-step-up DC-DC boost converter. Low voltage sources such as battery pack, ultra-capacitor, photovoltaic or fuel cell can be placed on the input voltage side to drive the converter. The output high voltage DC bus serves as the main power bus that provides power output to the load which is typically an inverter for grid connected system. Effectively, the converter serves as an interface for energy transfer between a low voltage source and high voltage DC bus. In many applications, the low voltage source suffers quick start up, load changes and also during transient conditions. In this case, the high side voltage has to be regulated using appropriate control techniques to produce a steady output voltage despite these variations. The converter employs one coupled inductor denoted as L. The primary and secondary windings of the coupled inductor were denoted as L_a and L_b respectively. The primary winding L_a serve as a filter inductor as in conventional flyback converter and is coupled to its corresponding secondary winding L_b. The primary and secondary windings of the coupled inductor is represented by n_1, n_2 and the coupling reference denoted by ‘’*’’. The converter primary

switch is denoted by S. The active clamp circuit consists of clamping switch S_C and the clamp capacitor C_C. The voltage extension cell comprises the secondary winding of the coupled inductors L_b, the clamp switch S_C, clamp capacitor C_C, regenerative diode D_r and the switched capacitor C_m. D_O, C_O are the output diode and filter capacitor and R_O denotes the load resistor.

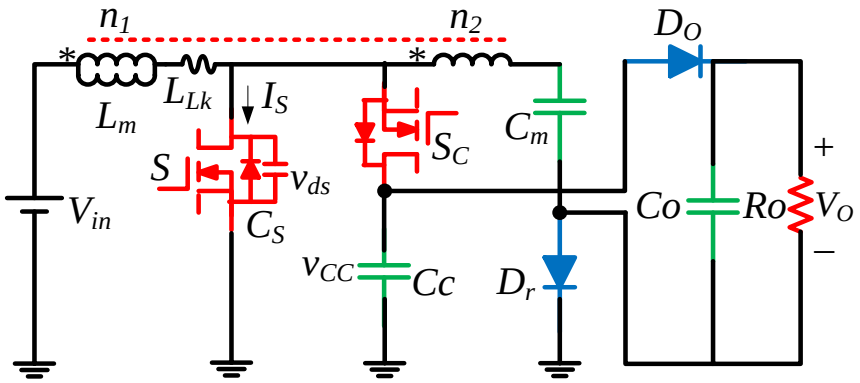

Figure 3.2 Equivalent circuit of the high step-up boost converter

Figure 3.2 illustrates the equivalent circuit of the proposed high step-up boost converter. C_S denotes the parallel capacitor of the main switch S, including the parasitic capacitor of the main switch and the possible added parallel capacitor to implement (ZVS). The drain-source voltage of the primary switch is represented as v_{ds}. V_{in}, V_O are the input and output voltages of the converter respectively. The coupled inductor can be modelled as an ideal transformer with define turns ratio. The ideal transformer primary winding is in parallel with magnetizing inductor L_m and then in series with a leakage inductance L_{Lk} [48, 73, 119]. The turns ratio N and coupling coefficient of the ideal transformer can be expressed as

$$N = \frac{n_2}{n_1} \tag{3.1}$$

$$k = \frac{L_m}{L_{Lk} + L_m} \tag{3.2}$$

3.2.2 Converter Principle of Operation

The proposed converter design is based on (CCM), and such operation is guaranteed throughout the full range of duty ratio variation under resistive loads. The gate signal of the clamp switch S_C is complimentary to that of the main switch S. The steady state waveform of the proposed converter is shown in Figure 3.3. There are eight modes of operation in one switching cycle. For completeness, the equivalent circuits corresponding to each operational stage are illustrated in Figure 3.4.

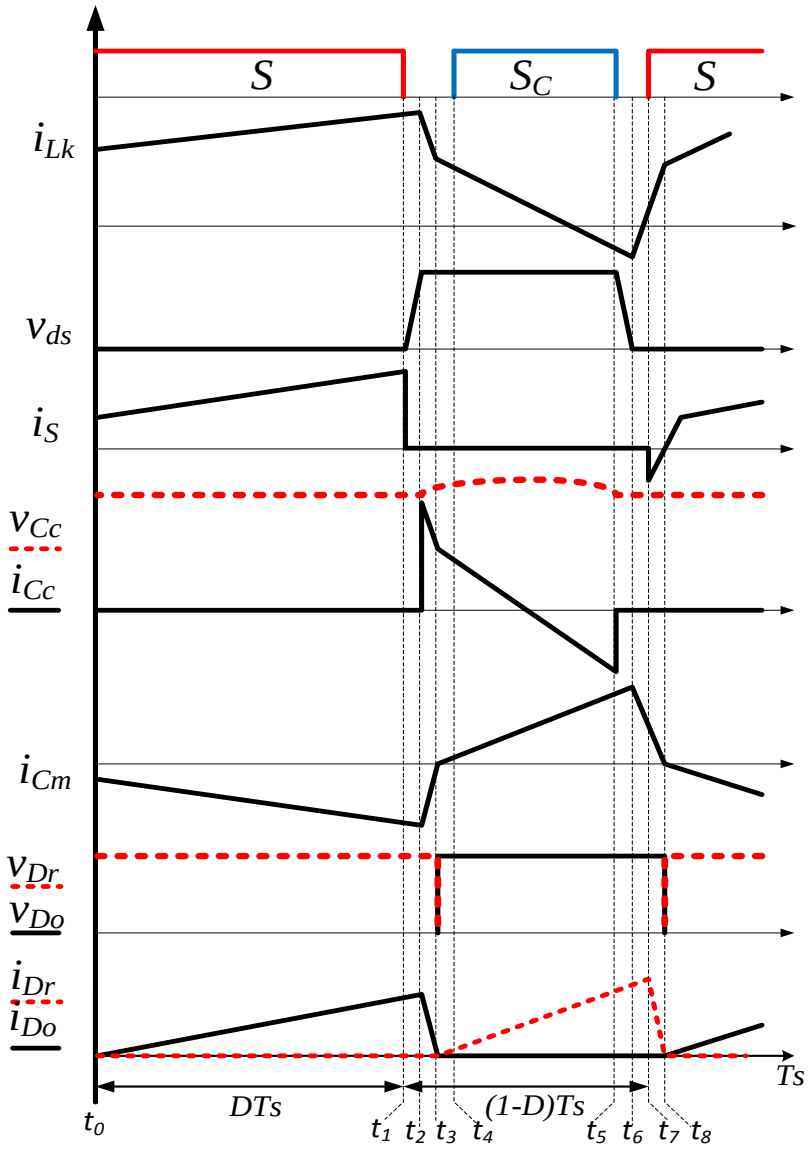

Figure 3.3 Steady state theoretical waveforms

Mode 1 $[t_0 - t_1]$ (figure 3.4a): Before t_1 the main switch S is conducting, whilst the clamp switch S_C is turned off. Magnetizing inductance L_m is charged linearly by the input voltage V_{in}. The regenerative diode D_r is reversed biased and the output diode D_O is forward biased. During this time, the clamp capacitor C_C, the switched capacitor C_m and the coupled inductor secondary winding n_2 are in series to enlarge the voltage gain. The coupled inductor magnetizing and leakage currents during this instant are

$$i_{Lm}(\mathrm{t}) = I_{\mathrm{Lm}}(t_0) + \frac{V_{in}}{(L_m)}(t - t_0) \tag{3.3}$$

$$i_{Lk}(\mathrm{t}) = i_{Lk}(t_0) + \frac{V_{in} - (V_{out} - V_{Cm} - V_{CC})/N}{L_{Lk}}(t - t_0) \tag{3.4}$$

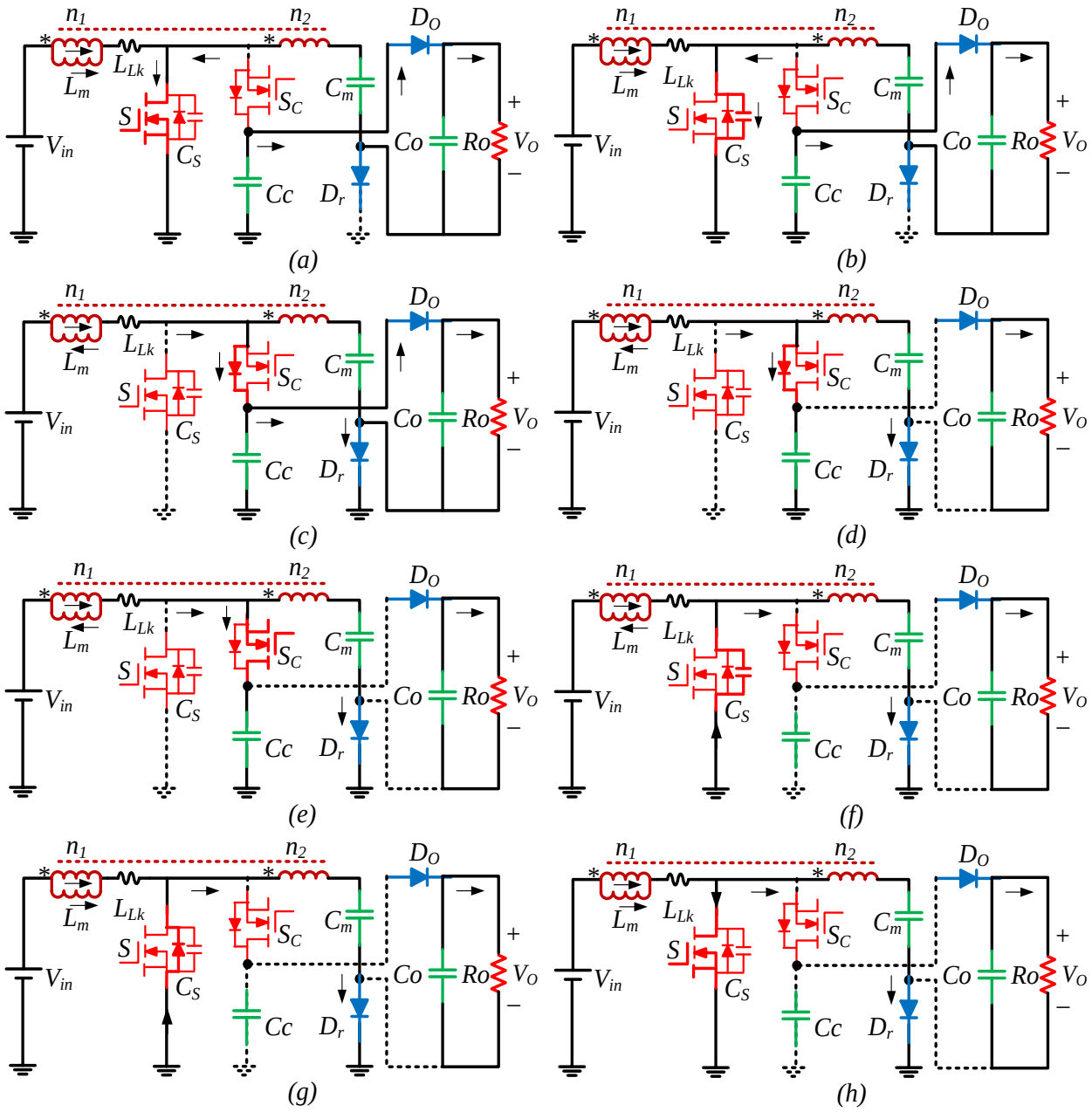

Figure 3.4 Operational stages equivalent circuits
(a)Mode 1($t_0 - t_1$), (b) Mode2 ($t_1 - t_2$), (c) Mode 3($t_2 - t_3$), (d) Mode 4($t_3 - t_4$)
(e) Mode 5 ($t_4 - t_5$), (f) Mode 6 ($t_5 - t_6$), (g) Mode 7 ($t_6 - t_7$), (h) Mode 8 ($t_7 - t_8$)

Mode 2 $[t_1 - t_2]$ (figure 3.4b): At time t_1 the main switch turns off, the parallel capacitor C_S resonate with leakage inductance L_{LK}. The parallel capacitor C_S of the main switch is charged continuously by the leakage inductor current i_{Lk} towards clamp capacitor voltage V_{Cc}. Because i_{Lk} is relatively large and C_S is small, the drain-source voltage v_{ds} of the main switch rises with a constant slope from zero. The turn-off loss of the main switch S is reduced because of parallel capacitor C_S. The drains-source voltage v_{ds} of the primary switch is derived as:

$$v_{dS} \approx \frac{I_{LK}(t_1)}{C_s}(t - t_1) \tag{3.5}$$

Mode 3 $[t_2 - t_3]$ (figure 3.4c): At time t_2, the voltage across the main switch rises to the clamp capacitor voltage which makes the antiparallel diode of the clamp switch S_C to conduct. The leakage inductance energy is released to the clamp capacitor C_C. Therefore, the drain-source voltage v_{ds} of the primary switch is clamped to clamp capacitor voltage v_{CC} and the leakage current i_{LK} is commutated to the antiparallel diode of the clamp switch. The output diode current i_{Do} decreases toward zero and the leakage inductance controls its current decrease rate thus alleviating reverse recovery loss. The leakage inductance current decreases in approximately linear rate given by

$$i_{LK}(\mathrm{t}) \approx i_{LK}(t_2) - \frac{V_{CC}}{L_{LK}}(t - t_2) \tag{3.6}$$

Mode 4 $[t_3 - t_4]$ (figure 3.4d): The output diode D_O turns off softly at t_3 with (ZCS), and the output capacitor supplies the load. Conversely, the voltage across the regenerative diode falls to zero and therefore becomes forward biased. The clamp and switched capacitors are now charged in parallel by the input voltage V_{in}. During this period, the leakage inductance L_{LK} resonates with clamp and switched capacitors. The leakage inductance decreases linearly given by

$$i_{LK}(\mathrm{t}) \approx i_{LK}(t_3) - \frac{V_{Cc} - [V_{Cm} - V_{Cc}]/N - V_{in}}{L_{LK}}(t - t_3) \tag{3.7}$$

Mode 5 $[t_4 - t_5]$ (figure 3.4e): The turn on gate signal of the clamp switch can be applied at time t_4 to implement the (ZVS) whilst its antiparallel diode is conducting.

Mode 6 $[t_5 - t_6]$ (figure 3.4f): At time t_5 the clamp switch S_C is turned off, the clamp circuit is disconnected. The regenerative diode D_r is still conducting and switched capacitor is charged through the coupled inductor secondary winding. A resonance is formed between the leakage inductance L_{Lk} and the switch parallel capacitor C_S. The parallel capacitor of the switch is discharged by the magnetizing inductor current and the reflected secondary winding current. The drain-source voltage of the main switch decreases with constant slope and is given by

$$v_{dS} = V_{Cc} + \frac{I_{LK}(t_5)}{C_s}(t - t_4) \approx V_{Cc} \tag{3.8}$$

Mode 7 $[t_6 - t_7]$ (figure 3.4g): This mode begins when the voltage across the parallel capacitor drops to zero at time t_6. The leakage inductor current i_{Lk} forces the antiparallel

diode of the main switch S to conduct. The leakage inductance and parallel capacitor stop resonating. The leakage inductance current rising rate is given by

$$i_{Lk}(\mathrm{t}) = \frac{V_{Cm} + NV_{in}}{NL_{Lk}}(t - t_6) \tag{3.9}$$

Mode 8 $[t_7 - t_8]$ (figure 3.4h): the turn on gate signal of the main switch S can be applied at time t_7 to implement the (ZVS) of the main switch when its antiparallel diode is conducting. The main switch S turns on under (ZVS) condition. The regenerative diode current i_{Dr} decreases toward zero, and its current decrease rate is controlled by the leakage inductance thus alleviating the reverse recovery loss. At the end of this stage, i_{Dr} reaches zero and the output diode D_O becomes forward biased, and new switching cycles ensue.

3.3 Steady State Performance Analysis

3.3.1 Voltage Gain

Under ideal conditions, the coupled inductor is assumed to be well coupled, and the leakage inductance is considered to be zero. The power switches are ideal with zero conduction voltage drops, all capacitors are large enough and their voltages assumed to be constant in one switching cycle. The MOSFET parallel capacitors are ignored. When the main switch turns-on, the magnetizing inductor is charged by the input voltage, and based on Kirchhoff's voltage law (KVL) the voltage across the magnetizing inductor can be denoted as

$$V_{Lm} = V_{\mathrm{in}} \tag{3.10}$$

The induced voltage across the secondary winding of the coupled inductor is given by

$$V_{Lb} = NV_{Lm} \tag{3.11}$$

During the same instant, the diode D_r is reversed blocking and the output diode D_O is forward conducting, the clamp capacitor and switched capacitor discharges in series, the power is transferred from the source to the load. The output voltage is given by

$$V_O = V_{Cm} + V_{CC} + NV_{\mathrm{in}} \tag{3.12}$$

Applying the inductor volt-second balance principle to the magnetizing inductor, the voltage across the clamp capacitor can be expressed as

$$V_{Cc} = \frac{V_{in}}{(1 - D)} \tag{3.13}$$

When the main switch S turns off, the clamp switch turns on after finite time delay, the clamp and switched capacitors are charged in parallel, the voltage across the switched capacitor is derived as

$$V_{Cm} = N(V_{CC} - V_{in}) + V_{CC} \tag{3.14}$$

From (3.12), (3.13) and (3.14) the ideal voltage gain is given by

$$M_{ideal} = \frac{V_o}{V_{in}} = \frac{N+2}{(1-D)} \tag{3.15}$$

From (3.15), the numerator consists of coupled inductor turns ratio N, which provides another degree of freedom to enlarge the voltage gain other than the PWM duty cycle. The curve of the ideal voltage gain M_{ideal} as a function of duty cycle under various turns ratio of the couple inductor is plotted as shown in Figure 3.5. When the turns ratio increases, the voltage gain also increases. The increase in the voltage gain corresponds to a specific value of the duty cycle; the choice of a particular voltage gain is usually guided by this relationship.

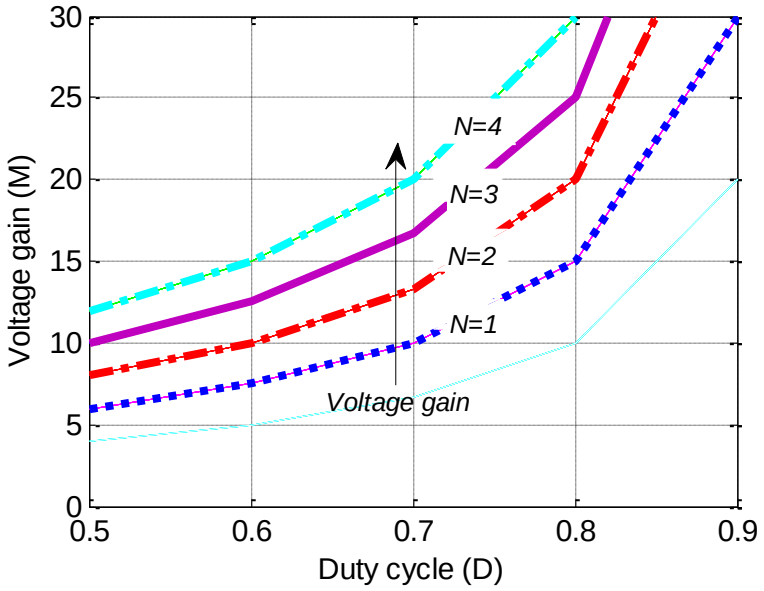

Figure 3.5 Ideal voltage gain characteristic for various *D* and *N* values

In practice, it is almost impossible to achieve 100% coupling between the coupled inductor primary and secondary windings. From the steady state analysis in section 3.2.2, to achieve the (ZVS) for both the main and clamp switches over a useful operating range, the leakage inductance is considered in the analysis. Besides, the inherent leakage inductance of the coupled inductor can also be used as a means of controlling the current falling rate of the diodes. Consequently, the leakage inductance is considered and the voltage conversion ratio is derived as follows:

The simplified steady state waveform used for the derivation is shown in Figure 3.6. As explained in section 3.2.2, the operational interval $[t_1 - t_4]$, $[t_5 - t_8]$ are very short and therefore neglected in the analysis. The resonant waveform of the leakage inductor current is also ignored. However, it is assumed to be piecewise linear with a straight line during subintervals. The complete switching cycle is now represented by the on state $[t_0 - t_2]$ and off state $[t_2 - t_7]$.

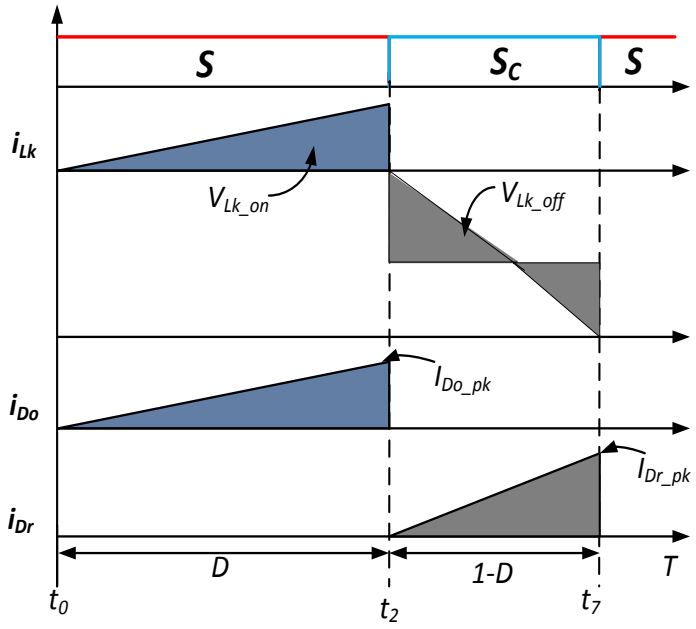

Figure 3.6 Simplified waveform for voltage gain derivation

The average current through the output and regenerative diodes are equal to the load current. Whereas the peak value of the regenerative and output diode currents is given by

$$I_{Dr_{pK}} = \frac{2I_O}{(1-D)} \tag{3.16}$$

$$I_{Do_{pK}} = \frac{2I_O}{D} \tag{3.17}$$

The voltage across leakage inductance during the main switch on period is denoted by

$$V_{Lk\_on} = \frac{L_{Lk}N\, I_{Do\_pk}}{\mathrm{D}} = \frac{2L_{Lk}N\, I_O\, f_S}{D^2} \tag{3.18}$$

When the main switch turns off and the clamp switch turns on. The voltage across the leakage inductance can be expressed as

$$V_{Lk\_off} = \frac{L_{Lk}N\, I_{Do\_pk}}{(1-\mathrm{D})} = \frac{2L_{Lk}N\, I_O\, f_S}{(1-D)^2} \tag{3.19}$$

Based on KVL, the voltage across the switched capacitor and the output voltage are given by (3.20) and (3.21)

$$V_{Cm} = N\left(V_{CC} - V_{in} - V_{Lk_{off}}\right) + V_{CC} \tag{3.20}$$

$$V_{out} = V_{Cm} + V_{CC} + N\left(V_{in} - V_{Lk_{on}}\right) \tag{3.21}$$

From (3.12), and (3.13) - (3.21) the voltage gain is obtained as

$$M_{real} = \frac{V_o}{V_{in}} = \frac{N+2}{(1-D)} \cdot \frac{1}{1 + 2 \cdot Q \cdot N^2/D^2 + 2 \cdot Q \cdot N^2/(1-D)^2} \tag{3.22}$$

Where$Q = (16 \cdot f_S \cdot L_k)/R_O$

Once the leakage inductance is considered to be zero in equation (3.22), then it is exactly the same as equation (3.15). Beside coupled inductor turns ratio and the duty cycle D, the voltage gain is related to switching frequency f_S load resistor R_o and the leakage inductance L_{Lk}. The curve of the voltage gain versus duty cycle and the leakage inductance is shown in Figure 3.7, with a fixed turns ratio N equal to 2. It is apparent that the leakage inductance degrades the voltage conversion ratio.

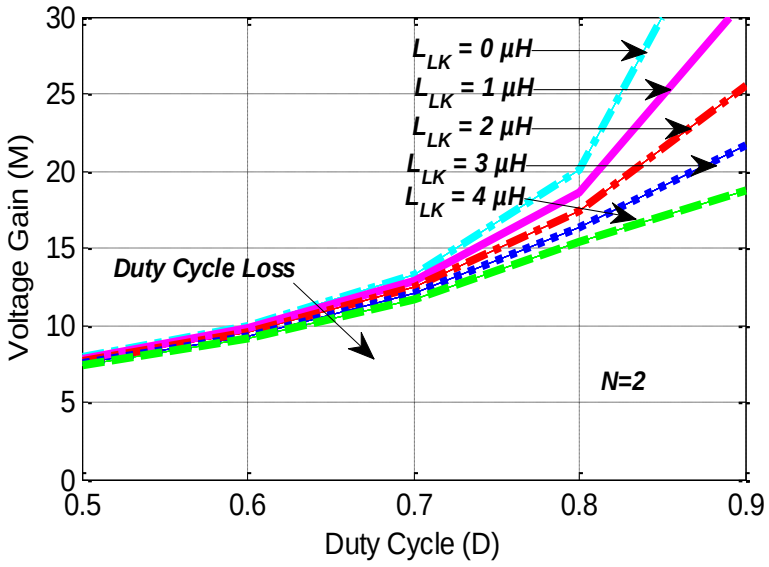

Figure 3.7 Voltage gain characteristic of the converter for various Q values

3.3.2 Voltage Stress Analysis

The voltage stress regarding the converter active switches (main and clamp) are the same and are derived from (3.15), by neglecting the voltage ripple on the clamp capacitors. The voltage stress of the switches is given by

$$V_S = V_{SC} = \frac{V_{in}}{(1-D)} \tag{3.23}$$

The voltage stress of the output diode D_O and the regenerative diode D_r is the same and increases as the turns ratio of the coupled inductor increases. However, it is always less than the output voltage and is expressed as

$$V_{DO} = V_{Dr} \cong V_O - V_{CC} = \frac{(N+1)V_{in}}{(1-D)} \tag{3.24}$$

The curve relating the normalized semiconductors voltage stress and coupled inductor turns ratio is plotted in Figure 3.8, using (3.23) and (3.24). It can be seen that the voltage stress on main and clamp switch decreases with an increase in turns ratio. Whereas the diodes voltage stress increases with an increase in the coupled inductor turns ratio. Usually, there is a design trade-off in selecting the turns ratio and components rating.

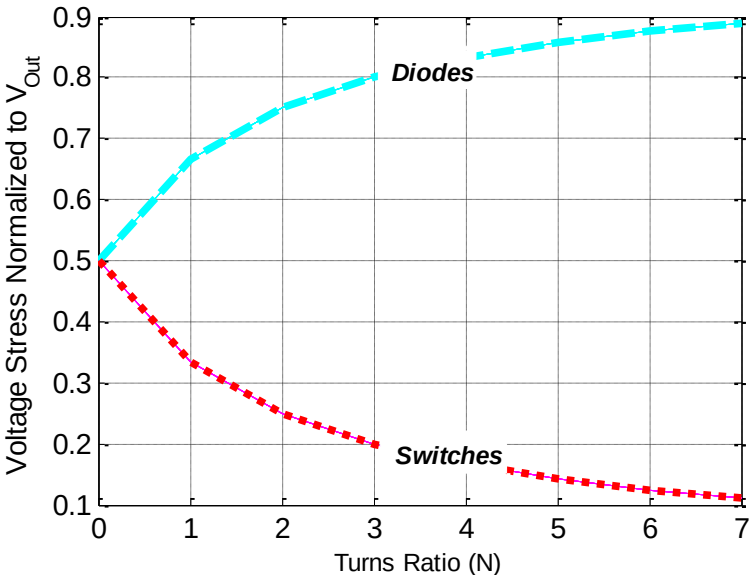

Figure 3.8 Normalized semiconductors voltage stress as function of turns ratio

3.3.3 Current Stress Analysis

In order to obtain the power device current stress easily the short switching transitions are ignored, only the on and off period of the main and clamp switches are considered. The coupled inductor is assumed to be perfectly coupled and current through the leakage inductor L_{LK} is considered to be linear. Likewise, the clamp switch current is also perceived linear. With the aforementioned assumptions, the steady state operation is now simplified to two stages as shown in Figure 3.9.

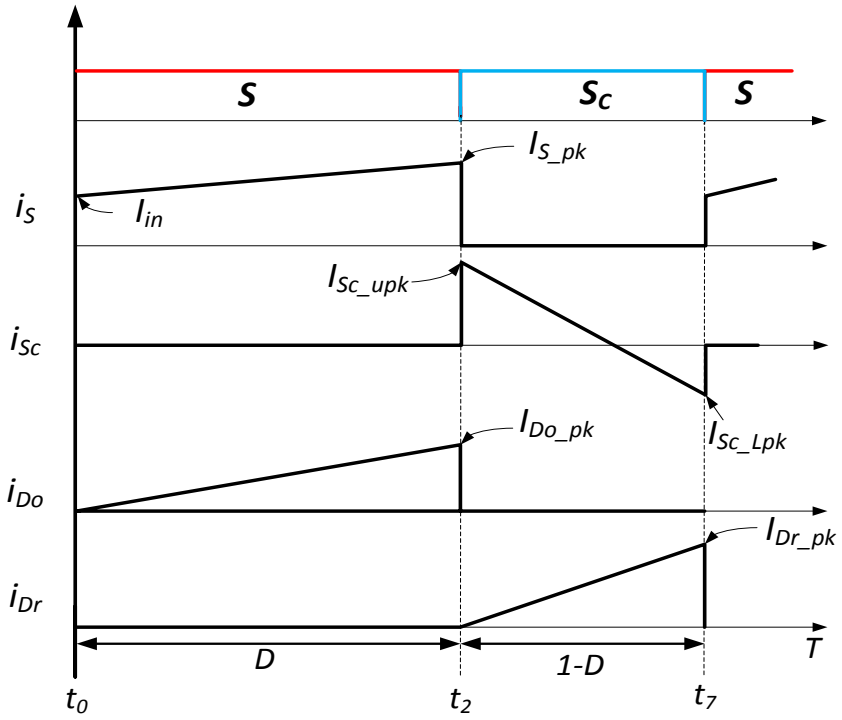

Figure 3.9 Simplified converter waveforms for current stress analysis

From steady state analysis in section 3.2.2, the average current of the output diode D_o, the regenerative diode D_r are equal to the output current and is given by

$$I_{Dr\_avg} = I_{Do\_avg} = I_{O\_avg} \tag{3.25}$$

The current rising rate of regenerative and output diode is approximately linear. The peak currents of the diodes are expressed in (3.16) and (3.17) respectively. The current of the main switch S at the turn on instant is the input current, and during turn off, is the summation of the input current and the reflected secondary winding current, given by

$$I_{S\_pk} = I_{in} + \frac{2NI_O}{D} \tag{3.26}$$

Assuming the conversion efficiency of the power converter to be 100% (i.e. lossless), the input and output current relationship can be expressed as

$$I_{in} = \frac{(N+2)I_O}{(1-D)} \tag{3.27}$$

Therefore, the RMS current of the main switch is given by

$$I_{RMS\_S} = \sqrt{\frac{\int_0^{DT_s} {i_S}^2(t)dt}{T_S}} = I_{in}\sqrt{D + \frac{2N(1-D)}{(N+2)} + \frac{4N^2(1-D)^2}{3D(N+2)^2}} \tag{3.28}$$

$$I_{RMS\_S} = \frac{(N+2)I_O}{(1-D)}\sqrt{D + \frac{2N(1-D)}{(N+2)} + \frac{4N^2(1-D)^2}{3D(N+2)^2}} \tag{3.29}$$

The current through the clamp switch during the turn on instant is the turn-off current of the main switch S. Whilst the clamp switch current during the turn off instant is the difference between the input current and the reflected current of the regenerative diode. The current through the clamp switch during turn off is expressed mathematically as

$$I_{SC\_OFF} = I_{in} - \frac{2NI_O}{(1-D)} \tag{3.30}$$

Similarly, the RMS current of the clamped switch is given by

$$\begin{aligned} I_{RMS\_SC} &= \sqrt{\frac{\int_{DTs}^{(1-D)T_s} {i_{Sc}}^2(t)dt}{T_S}} \\ &= I_{in}\sqrt{\frac{4N^2(1-D^3)}{3(N+2)^2D^2} - \frac{(2N+D-ND)(N-2)(1-D)}{D(N+2)}} \end{aligned} \tag{3.31}$$

$$I_{RMS\_SC} = \frac{(N+2)I_O}{(1-D)}\sqrt{\frac{4N^2(1-D^3)}{3(N+2)^2D^2} - \frac{(2N+2D-ND)(N-2)(1-D)}{D(N+2)}} \tag{3.32}$$

According to (3.29) and (3.32), the current stress of the active devices is a function of the coupled inductor turns ratio and duty cycle. By proper choice of the coupled inductor turns ratio, the current stress imposed on the primary switch can be minimized, leading to improved efficiency.

3.3.4 (ZVS) Soft Switching Performance

The (ZVS) turn off of the main and clamp switch is achieved due to the existence of parallel capacitor C_s. The (ZVS) turn on of the main and clamp switches are realized naturally because the antiparallel diodes of the clamp switches are conducting before the application of their corresponding gate signal. To ensure (ZVS) of the main switch, the drain-source voltage of main switch S should be decreased to zero before a turn-on gate signal is applied. In other words, the energy stored in the parallel capacitor should be less than the energy stored in the leakage inductance when the main switch turns off. The parallel capacitor C_S is discharged by the coupled inductor primary current I_{La} at time t_6 see (Figure 3.4f), to ensure (ZVS) of the main switch the following relation should be satisfied

$$L_{Lk}I_{La}^2(t_6) \geq C_S V_{ds}^2 \tag{3.33}$$

Equation (3.33) can be simplified using the ideal circuit of the nonisolated auto-transformer shown in Figure 3.10. The transformer has only one winding with primary and secondary turns $n_1$and n_2 respectively [92]. N is defined as the turns ratio like in conventional transformer. The voltage and current relationship in the isolated and nonisolated structure are the same given by

$$v_2 = N\, v_1$$

$$i_1 = N\, i_2$$

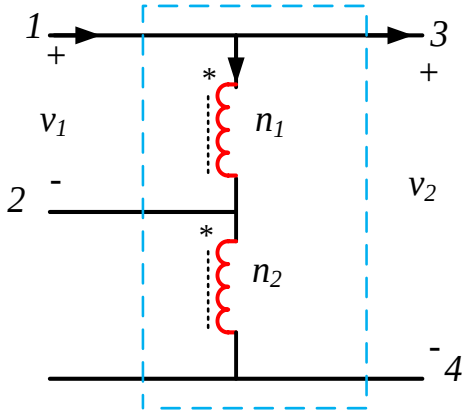

Figure 3.10 Current and voltage relationship of a non-isolated transformer [92]

The current through the primary side is given by

$$i_{La} = i_p = i_1 - i_2 = (N-1)\, i_2 \tag{3.34}$$

To ensure (ZVS) of the main switch the following equation should be satisfied

$$L_{Lk}((N-1)\, I_o)^2 \geq C_S \frac{{V_o}^2 (1-D)^2}{(N+2)^2} \tag{3.35}$$

The (ZVS) boundary of the main switch as a function of the input voltage and output power is plotted in Figure 3.11 using (3.35). It can be seen that as the output power increases, the current required to implement the (ZVS) also increases. It is worth mentioning the (ZVS) soft switching performance of the main switch can be easily realized under high output power condition. Note that the (ZVS) boundary of the main switch becomes wider with a smaller value of the parallel capacitor of MOSFET. Effectively with a parallel capacitor of 2.2 nF, the (ZVS) of the main switch can be achieved when output power is 75 W.

The parallel capacitor is normally selected from (3.35). In general, a larger value of parallel capacitor allows greater reduction of turn-off loss. However, it may introduce more turn-on losses.

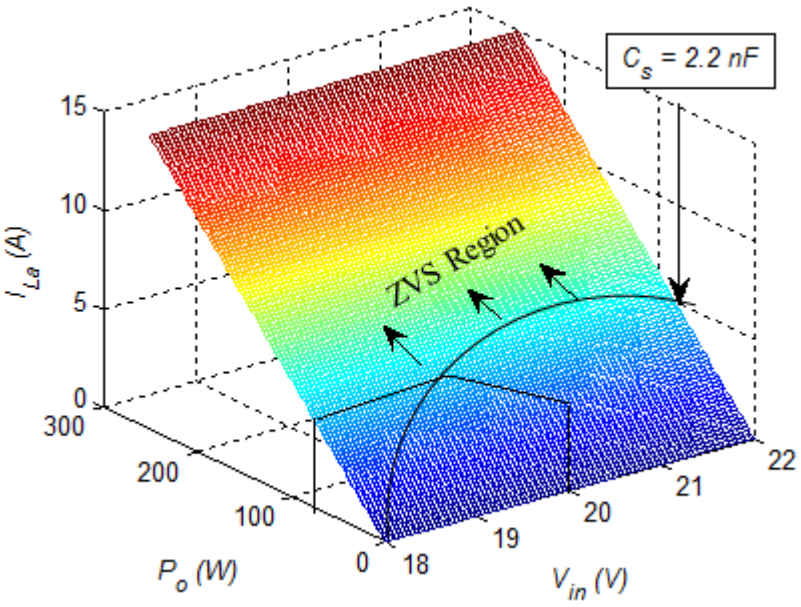

Figure 3.11 ZVS boundary of main switch as a function of input voltage and output power

The trade-off in parallel capacitor selection lies on the minimization of the turn-on and turn-off losses. It can be seen that sufficient leakage inductor energy is required to discharge the parallel capacitor during the dead time interval to ensure (ZVS) turn-off. This argument may allow the use of small parallel capacitor or complete elimination. Likewise, the (ZVS) of the clamp switch is also a function of the output power and tends to increase with increase in output power. The (ZVS) turn-on condition of the clamp is achieved easily over the entire load range.

3.4 Performance Comparison

A performance comparison is made between coupled inductor boost converter with buck-boost active clamp (BBAC) [73] Figure 3.12, an active clamp coupled inductor converter with extended voltage doubler cell (ACCIB) [48] Figure 3.13, and the proposed converter to appreciate the merits of the proposed topology. Table 3.1 shows the comparison regarding the semiconductors voltage stress, parts count, switching loss and static gain.

As can be seen in Table 3.1, the proposed converter can achieve the same or higher voltage conversion ratio with a lower turns ratio of the coupled inductor, when compared to the other two topologies, lower turns ratio reduces the copper loss and coupled inductor size. The power switches in BBAC suffers highest voltage stress followed by the ACCIB converter.

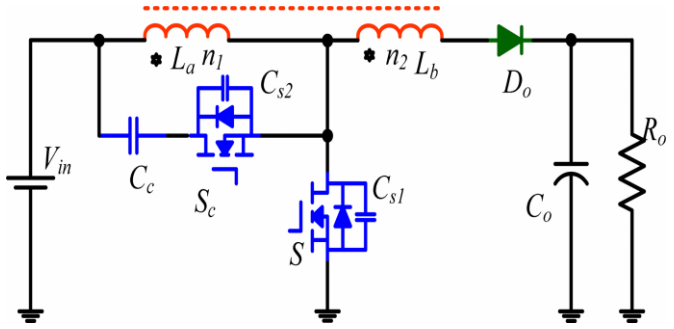

Figure 3.12 Buck-boost active clamp converter [73]

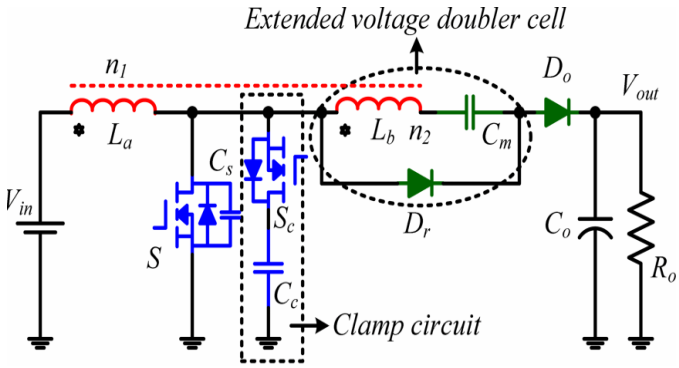

Figure 3.13 Active clamp coupled inductor boost converter [48]

Table 3.1 Performance comparison between (BBAC), (ACCIB) Converters and Proposed Converter

Topology	**BBAC Converter**	**ACCIB Converter**	**Proposed Converter**
Active Switches	2	2	2
Diodes	1	2	2
Voltage gain	$\frac{(1+ND)}{(1-D)}$	$\frac{(1+N)}{(1-D)}$	$\frac{(2+N)}{(1-D)}$
Voltage stress of active switches	$\frac{V_O}{(1+ND)}$	$\frac{V_O}{1+N}$	$\frac{V_O}{2+N}$
Voltage stress of diodes	$\frac{(1+N)V_O}{(1+ND)}$	V_O	$\frac{(1+N)V_O}{(2+N)}$
Soft switching	(ZVS)	(ZVS)	(ZVS)
Switching Losses	Low	Low	Low

The proposed converter suffers least voltage stress regarding power switches. Likewise, the diode voltage stress in the BBAC is the highest of all the three converters and the diode reverse recovery losses is significant. In the case of ACCIB, the voltage stress of the diode is the same as the output voltage. However, in the proposed topology the diode voltage stress is

always less than the output voltage, and low voltage rated diodes typically recover faster leading to the alleviation of the diode reverse recovery losses even under high power application. It is worth mentioning that the proposed converter does not require any start up-up circuitry. However, a start-up process is necessary for ACCIB to limit the inrush current.

3.5 Design Consideration

3.5.1 Coupled Inductor Turns Ratio Design

The key design step is to choose either the coupled inductor turns ratio that guarantee a modest duty cycle of the power device or the duty cycle that realizes low turns ratio and achieves the required voltage gain. As previously explained, the turns ratio determine the switch voltage and current requirements. Proper turns ratio selection; ultimately avoid extreme duty ratio operation. The coupled inductors turns ratio and duty cycle are both obtained from (3.15), and expressed as

$$N = \frac{n_2}{n_1} = \left[\frac{V_o}{V_{in}}(1-D) - 2\right]$$
$$D = 1 - \frac{V_{in}}{V_o}(N+2) \tag{3.36}$$

A turns ratio of $N = n_2/n_1 = 1.8$ is chosen which gives a corresponding duty cycle of 0.6.

3.5.2 Leakage Inductance Design

The coupled inductor should be well coupled to minimize the leakage inductance value since it has been established in section 3.3.1, that the leakage inductance degrades the conversion efficiency of the converter. Consequently, the leakage inductance should be carefully designed. From (3.22), the leakage inductance can be expressed as

$$L_{LK} = \frac{R_0 D^2(1-D)[(N+1) - M(1-D)]}{2N^2 M f_s(1-2D+2D^2)} \tag{3.37}$$

The leakage inductance plays a role in achieving the (ZVS) soft switching performance of the active devices over a useful operating range, and also controls the current falling rate of the diodes. Hence, the leakage inductance should be selected carefully.

3.5.3 Magnetizing Inductor Design

A good criterion for designing the magnetizing inductance is to maintain the continuous

inductor current mode and set an acceptable current ripple in the magnetizing inductor. The ripple magnitude of the magnetizing inductor current is given by

$$\Delta I_{Lm} = \frac{V_{in} D}{L_m f_s} \tag{3.38}$$

From (3.38) the magnetizing inductor can be expressed as

$$L_m = \frac{V_{in} D}{\Delta I_{Lm} f_s} \tag{3.39}$$

Where ΔI_{Lm} is the magnetizing inductor current ripple. A current ripple up to 20% of the magnetizing inductor current is used in the coupled inductor design.

3.5.4 Magnetic Core Selection

The magnetic core is selected based on the required inductance and peak inductor current. The magnetic component size is calculated using the core geometry method of [120]. The inductance required with DC bias and the DC current are the two parameters required. Following this method, a Kool Mμ ® toroidal core (77100-A7) from Magnetic Incorporation is selected. The Kool Mμ powdered cores have advantages of low losses at a higher frequency. The coupled inductor is implemented on the toroid (77100-A7), the primary winding has 32 turns with one strand of 175/40 Litz wire, and the secondary winding has 58 turns with one strand of 100/40 Litz wire. The measured magnetizing inductance is 83 μH, and the measured leakage inductance on the primary side is 1.3 μH.

3.5.5 Clamp Capacitor Design

As previously explained, the clamp circuits provides the benefits of recycling the coupled inductor leakage energy whilst minimizing the switch voltage stress. The main function of the clamp capacitor is to suppress the high voltage spikes and avoid excessive resonant ringing of the primary switch caused by the interaction of the leakage inductor of the coupled inductor and parallel capacitor of the switch. The clamped capacitor is linearly discharged by the secondary reflected magnetizing current of the coupled inductor. Assuming that the magnetizing inductor current is ripple-free, the clamping capacitor needs to maintain a balance between charging and discharging. As demonstrated in [16], the reasonable compromise for the clamp capacitor selection is to choose the closest value so that one-half of the resonant period exceeds the maximum turn-off time of the main switch. From [16], the clamp capacitor can be selected using equation (3.40).

$$C_C \geq \frac{(1-D)^2}{\pi^2 L_{LK} {f_s}^2} \tag{3.40}$$

3.5.6 Switched Capacitor Design

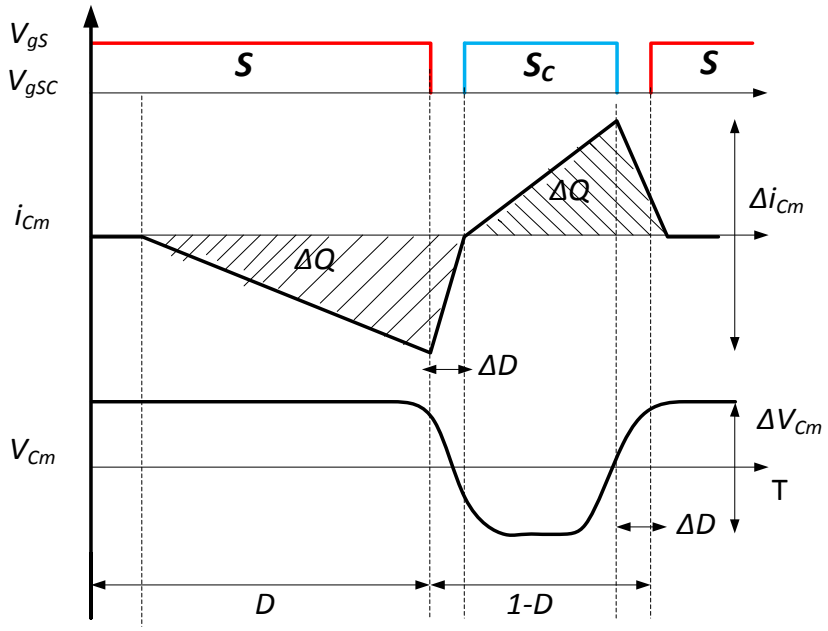

Figure 3.14 Voltage and current waveform of switched capacitor

Considering the assumptions made in section 3.3.1, the switched capacitor serves as a voltage source in the converter, the ripple voltage should be limited to reasonable value during selection. The peak-peak switched capacitor ripple voltage can be calculated by considering the waveform shown in Figure 3.14. The shaded area Q represents the energy stored in the switched capacitors C_m in one switching cycle. The peak-to-peak voltage ripple Δv_{Cm} is obtained by considering the area charged by the switched capacitor C_m, which is given by

$$\Delta V_{Cm} = \frac{\Delta Q}{C_m} = \frac{1}{C_m} * \frac{1}{2} * \frac{\Delta I_{CM}}{2} * (1 - D + \Delta D) T_S \tag{3.41}$$

The ripple magnitude of the switched capacitor current is given by

$$\Delta I_{CM} = \frac{4 I_O}{(1 - D + \Delta D)} \tag{3.42}$$

From (3.41) and (3.42) the switched can be selected from (3.43)

$$C_m = \frac{I_O}{\Delta V_{Cm} f_s} \tag{3.43}$$

Where ΔV_{Cm} is the voltage ripple of the switched capacitor. A voltage ripple of 10% is used in both the clamp and switched capacitors during component selection.

3.5.7 Output Capacitor Design

The major criteria guiding the choice of output capacitor is utilizing enough capacitance to satisfy the allowable output voltage ripple. In a CCM, it is assumed that all the ripple components of the diode current I_{Do} flow through the capacitor and the average value flows through the load resistor. Therefore, the average diode current can be expressed as

$$I_{Do\_avg} = \frac{I_O}{(1-D)} \tag{3.44}$$

Based on Kirchhoff's current law (KCL) the average diode current can be denoted by

$$I_{Do} = C_O \frac{dv_o}{dt} - I_O \tag{3.45}$$

From (3.44) and (3.45)

$$C_O \frac{dv_o}{dt} = \frac{I_O}{(1-D)} - I_O \tag{3.46}$$

$$C_O dv_o = \frac{I_O D}{(1-D)} dt \tag{3.47}$$

From section 3.2.2, dt represent the main switch off time interval in which the output current flowed through the load via the output diode and expressed mathematically as $(1-D)T_s$ (see Figure 3.3). dv_o is the peak-peak ripple voltage of the output capacitor. Using this relation the output capacitor value can be chosen from (3.49) by allowing appropriate voltage ripple in the output capacitor.

$$C_O = \frac{I_O D}{\Delta v_o (1-D)} * (1-D)T_s \tag{3.48}$$

$$C_O = \frac{I_O D}{\Delta v_o f_s} \tag{3.49}$$

3.5.8 Power Device Selection

The power devices can be selected from (3.24) and (3.27) by considering an acceptable voltage and current margins.

3.5.9 Time Sequence Design

The approximate dead time between the turn-off of the main switch and the turn-on of the corresponding clamp switch is to implement (ZVS) turn on condition of the clamp switch. The gate signal of the clamp switch can be applied whilst its antiparallel diode is conducting. The approximate time delay is

$$\Delta t_{S1\_off\ SC1\_On} = \frac{V_{Cc1} C_{S1}}{I_{Lm}} \tag{3.50}$$

Likewise the dead time between the turn off of the clamp switch and turn-on of the corresponding main switch is to ensure (ZVS) turn on condition of the main switch. The best criterion is to allow for a one-quarter of the resonant time between the leakage inductance and the parallel capacitor [16]. This is expressed as

$$\Delta t_{SC1\_off\ S1\_On} = \frac{\pi}{2}\sqrt{L_{Lk1} C_{S1}} \tag{3.51}$$

The major advantage of the dead time design is to prevent an overlap of the main and clamp switch gate signals. Any accidental overlap could lead to short circuit and failure of the circuit

3.6 Simulation Results

A Matlab-Simulink environment is used to investigate the performance of the converter with a 20 V input voltage, 190 V output voltage and an output power of 250 W. A detail description of the closed loop model is contained in Appendix A. The switching frequency is 50 KHz, the components selection is based on the analysis presented in section 3.3 and design criteria of 3.5 respectively. The converter parameters are listed in Table 3.2.

Table 3.2 Converter Simulation Parameters

Components	**Symbol**	**Parameters**
DC Input voltage	V_{in}	20 V
DC Output voltage	V_O	190 V
Output power	P_O	250 W
Switching Frequency	f_s	50 KHz
Magnetizing Inductance	L_m	*82* µH
Leakage Inductance	L_{LK}	1.3 µH
Turns Ratio	$N\ (n_1/n_2)$	1:1.8
MOSFETS (Power switches)	S, S_c	CSD19536KCS ($R_{DS\_on} = 2.3\ m\Omega. C_{0ss} = 2.3\ nF$)
Diodes	$D_r\ , D_O$	MBUR42050G ($V_F = 0.86\ V, V_R = 250\ V$)
Capacitors	C_C	4.7 µF
	C_m	10 µF
	C_O	50 µF

Figure 3.15 shows the simulation results of the converter. The (ZVS) of the main and clamp switch are shown in Figure 3.15(a) and Figure 3.15(b), the voltage stress of the converter active switches is 60V, which is far lower than the converter output voltage. Therefore, low rated power devices can be utilised to reduce the conduction losses. Figure 3.15(c) illustrates the clamp circuit performance; note that the voltage stress on the clamp capacitor is also 60 V, which coincides with the active devices voltage stress. As can be seen, when the main switch turns off the leakage energy is released to the clamp capacitor such that the switch voltage is clamped.

Figure 3.15(d) and Figure 3.15(e) shows the secondary and primary winding currents of the coupled inductor respectively. The (ZCS) turn off of the diodes as well as their current and voltage stress are illustrated in Figure 3.15(f) and Figure 3.15(g). The maximum voltage stress of the diodes is exactly 140V, which is less than the output voltage of the converter, a key operational advantage of the proposed circuit. Importantly, the simulation results validate the converter analysis described in section 3.3.

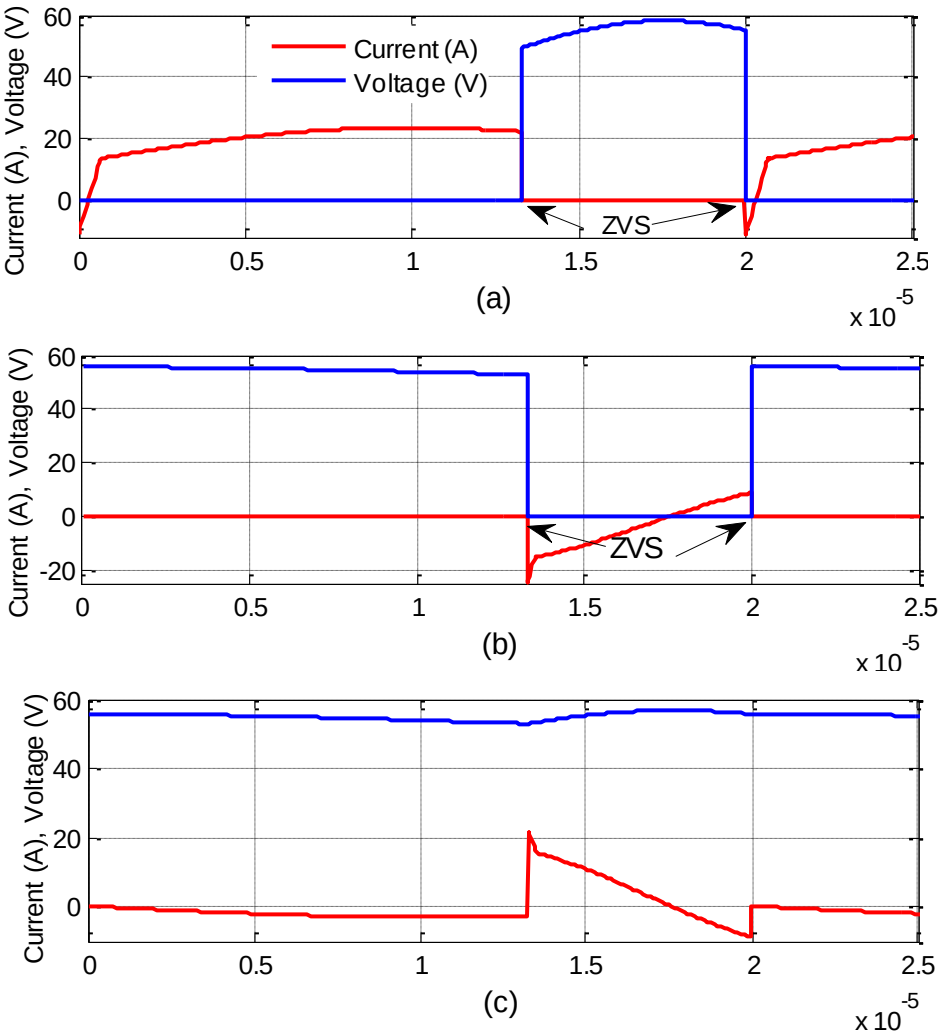

Figure 3.15 Simulation Results

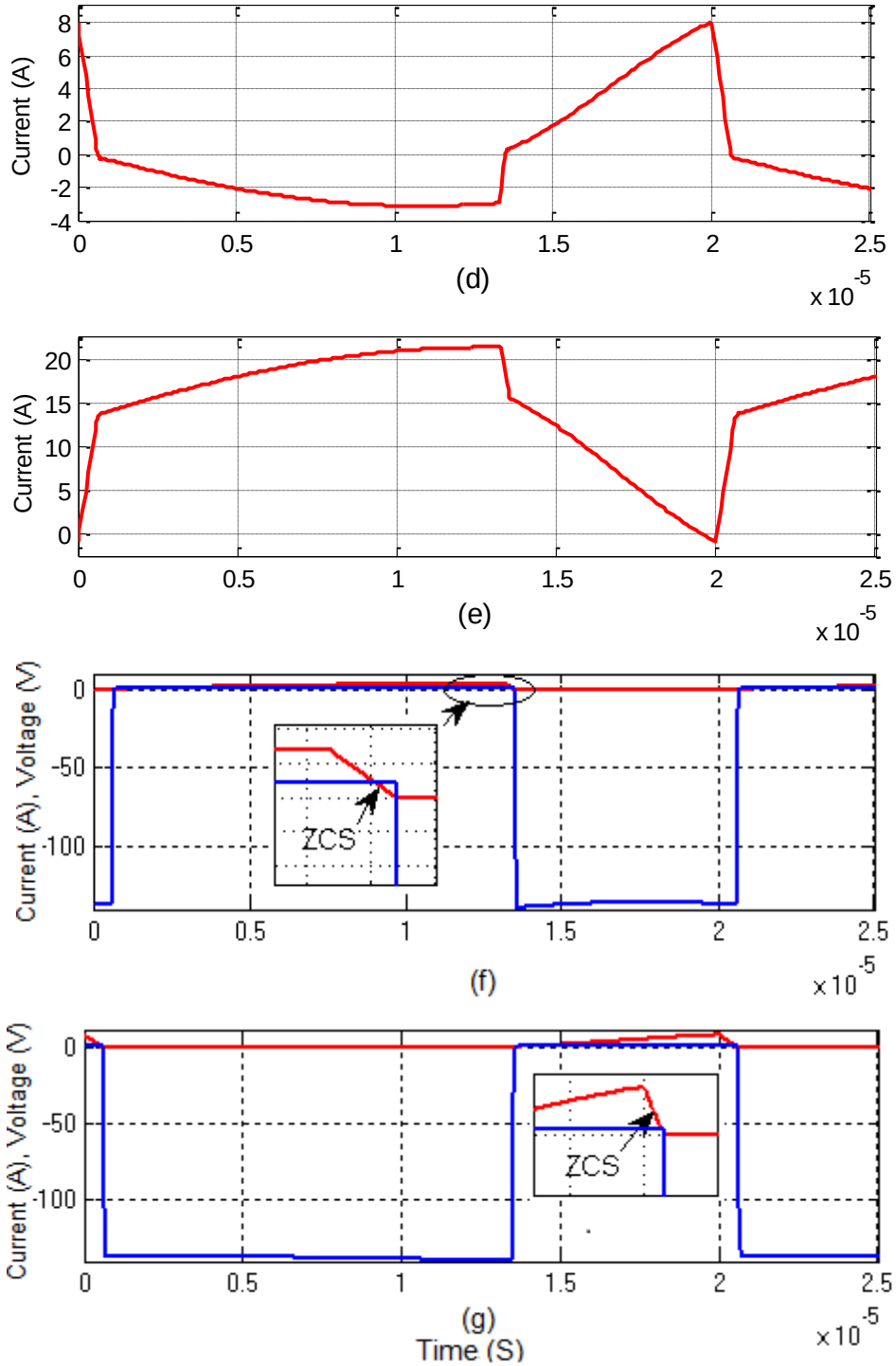

Figure 3.15 (Continuation) Simulation results

3.7 Experimental Verification

3.7.1 High Step-up Active Clamp Boost Converter Prototype

To verify the performance of the high step-up converter a 250 W prototype has been implemented in the laboratory. The parameters of the converter along with the component

ratings are derived from section 3.5 and are as listed in Table 3.2 for reference. The parameters used in the simulation are the same with that of the experimental prototype, in order to make a comparison.

Figure 3.16 shows the photograph of the experimental prototype, detail explanation of the hardware can be found in Appendix B. Other details describing the control overview including the microcontroller, gate drive sensor measurements and complete experimental set-up are explained in Appendix C and Appendix D respectively.

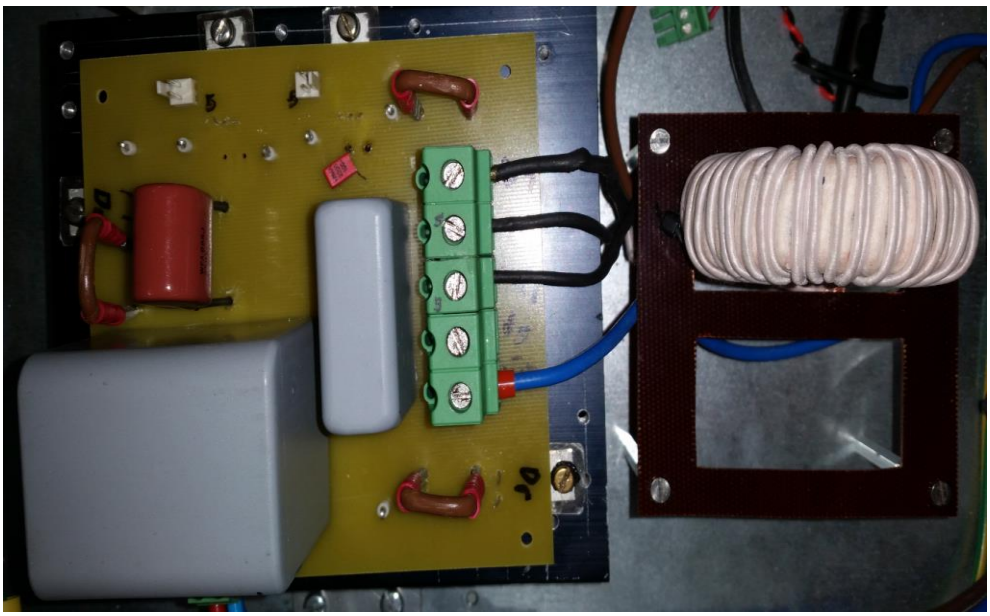

Figure 3.16 Photograph of the experimental prototype

3.7.2 Measured Experimental Waveforms

The proposed single phase converter prototype has been tested. The test is conducted under $250\,W$ full load condition with $20\,V$ input voltage. The magnitude of the output voltage is now proportional to the duty cycle since the input voltage and turns ratio are now selected. With reasonable coupled inductor turns ratio design, extreme PWM duty ratio can be avoided in a high step-up converter. Figure 3.17 illustrate the complimentary gate signals of the main and clamp switches.

From the gate signals V_{gs}, the duty ratio D of the main switch is approximately 0.64 and the off time duration $(1-D)$ is 0.36 respectively. V_{gsc} is the gate signal of the clamp switch and is complimentary to that of the main switch V_{gs}. As can be seen, the gate signal of the main switch is complimentary to that of corresponding clamp switch.

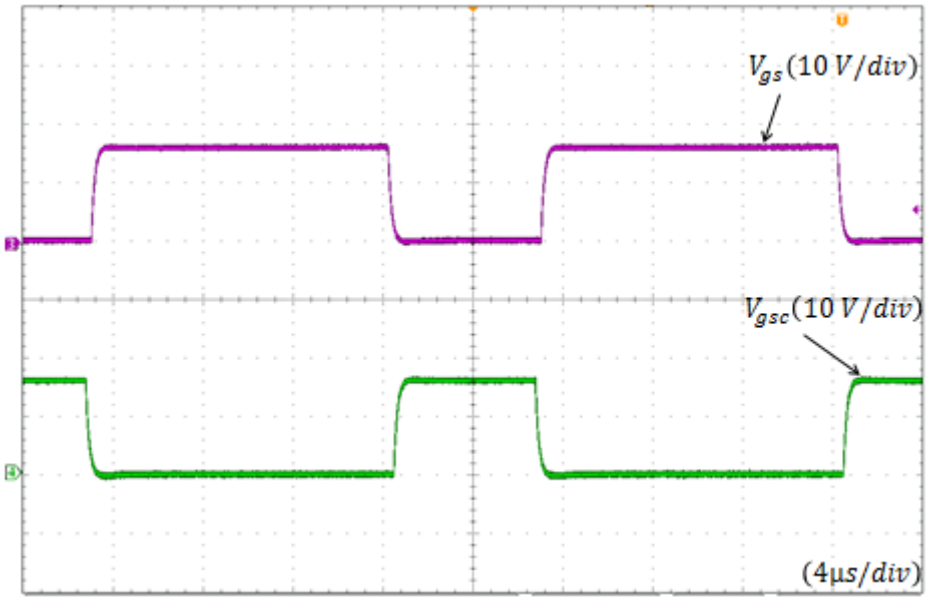

Figure 3.17 Complimentary gate signals of the main switch and clamp switch
Main switch gate signal (purple), clamp switch gate signal (green)

These gating signals are the required PWM duty ratio signal to derive the converter switches as explained in section 3.2.2. Furthermore, the gate signals indicate proper PWM duty ratio utilization by the switches.

Figure 3.18 illustrates the measured waveform of the leakage inductor current (i.e. primary current of the coupled inductor). The leakage inductor current is continuous throughout the entire switching cycle without a break. Hence, this operation can be described as continuous conduction mode CCM. The leakage inductor current ripple is large, specifically due to the

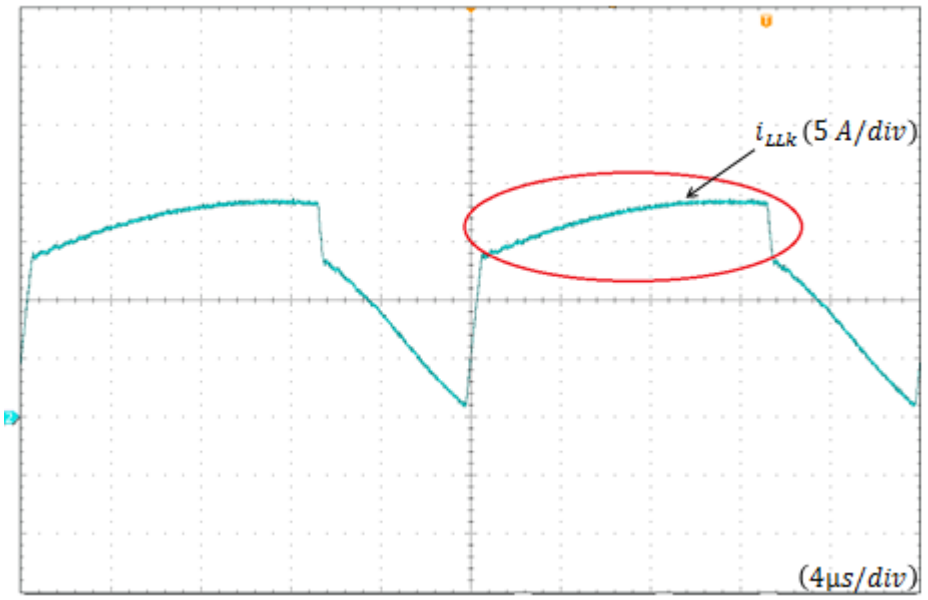

Figure 3.18 Leakage inductor current waveform

net effect of the magnetizing inductor current and secondary winding reflected current when the converter primary switch turns off. The marked area represents the secondary winding reflected current contribution to the current ripple. The measured peak-peak leakage inductor current is $20\ A$ in simulation and $19\ A$ in the experiment. In comparison with the simulation results in Figure 3.15(e), it is apparent that the experimental leakage inductor current waveform matches closely with the simulation.

Figure 3.19 shows the measured drain-source voltages of the active switches v_{ds}, v_{dsc} and their corresponding switch currents I_s, I_{sc} respectively. The voltage stress of the active switches is $60\ V$, this also validates the simulation results shown in Figure 3.15a and Figure 3.15b. Now referring to the theoretical analysis (see equation (3.23)); it is fair to conclude that the experimental results validates the simulation results closely and in agreement with the analysis. Likewise, the measured switch currents match closely in both simulation and experiment. Pertinent to illustrating the active switches voltage stress, Figure 3.19 demonstrates the (ZVS) soft switching characteristics of the main and clamp switches. However, details of the soft switching performance of both active switches are further illustrated with the aid of Figure 3.20 and Figure 3.21 respectively. As can be seen in Figure 3.20, before the main switch turns on, its drain source voltage drops to zero and the main switch apparently turns on with (ZVS) condition. After the main switch turns on, the switch current rises almost linearly to zero and becomes positive, similar to the simulated behaviour shown in Figure 3.15a. This further illustrates the operation of active clamp circuit, in which

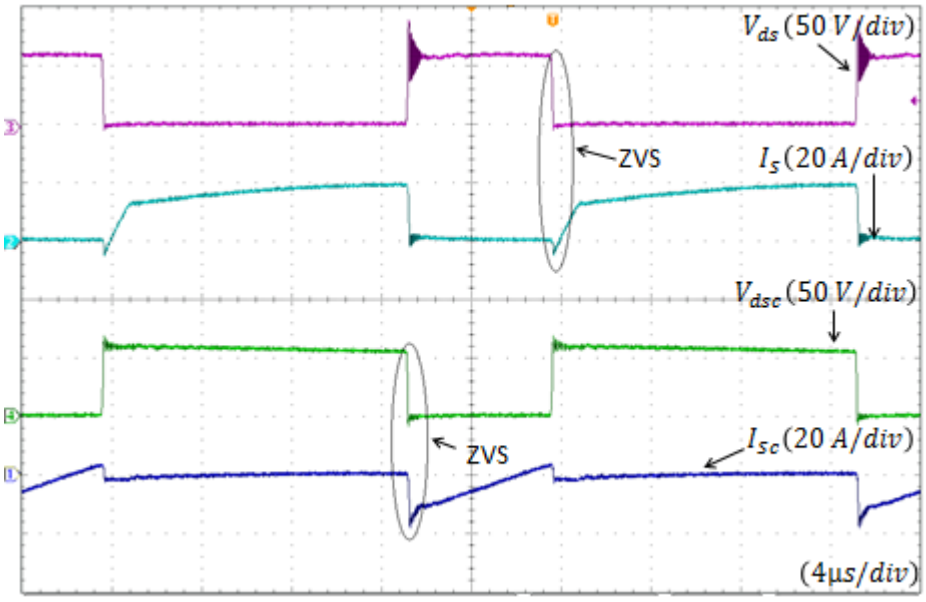

Figure 3.19 Main and clamp switch current and voltage waveforms

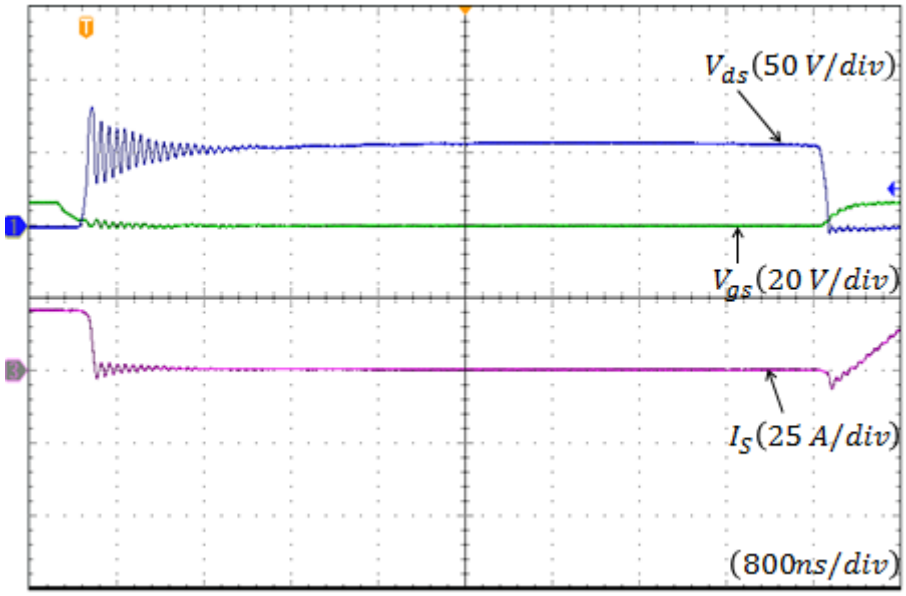

Figure 3.20 (ZVS) details of main switch

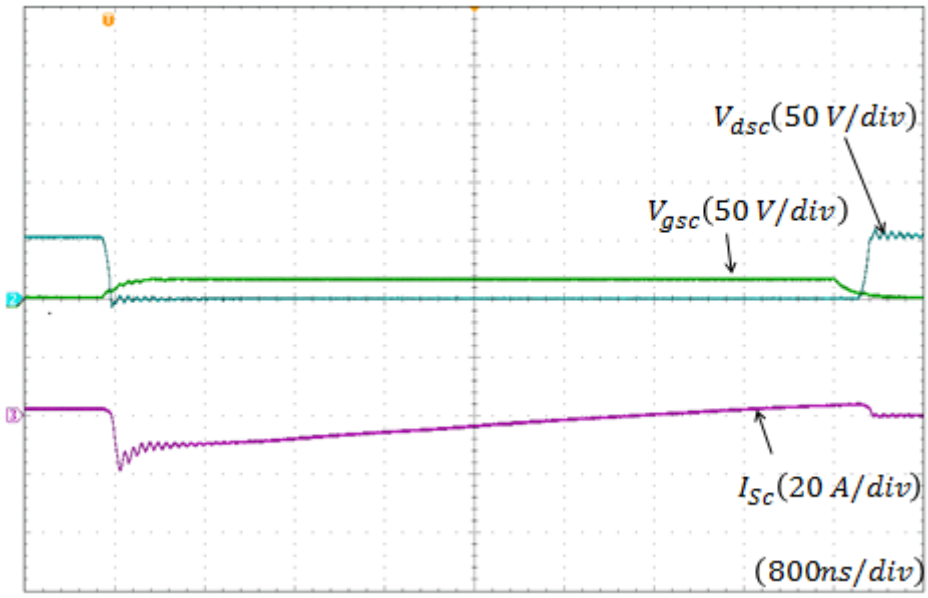

Figure 3.21 (ZVS) details of clamp switch

the bidirectional magnetizing current is used to achieve (ZVS). Here bidirectional magnetizing current meant that the coupled inductor ripple current is allowed to become negative relative to magnetizing current for a portion of each switching period. There is resonant ringing across the main switch during turn off. The ringing is largely due to the resonant frequency formed by the clamp capacitor and leakage inductor.

In order to significantly reduce the ringing, the resonant frequency should be sufficiently low by using large value of clamp capacitor. However, using a large value of clamp capacitor to supress the ringing yields no improvement in the clamp circuit performance and result in a

bulky capacitor. Figure 3.21 shows close up of (ZVS) performance of clamp switch; this trace clearly displays the clamp switch transition from on to off and vice versa.

The clamp circuit performance is shown in Figure 3.22. The measured waveforms comprises of the drain-source voltage of primary switch, the voltage across and current flowing through the clamp capacitor. As can be seen, when the main switch turns off, the clamp switch conducts and the voltage spikes of the main switch due to the leakage inductor energy is suppressed by the clamp capacitor. The voltage stress of the primary switch is the same as the voltage across the clamp capacitor (i.e. 60 V) and is far lower than the converter output voltage. This allows low-rated high-performance power device to be utilised to reduce the conduction loss. Furthermore, in comparison with the simulated result in Figure 3.15(a) and Figure 3.15(c), it is clear that the clamp circuit behaviour is the same in both simulation and experiment. It is worth noting that the peak current of the clamping capacitor is $20\ A$ in both simulations and experimentally measured waveform.

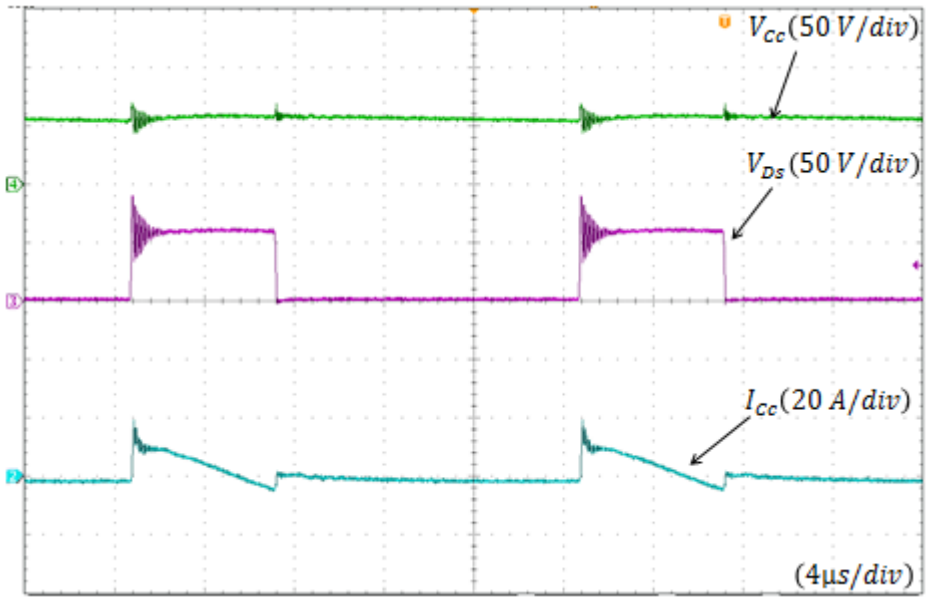

Figure 3.22 Clamp circuit performance

Figure 3.23 illustrates the regenerative and output diode measured current and voltage waveforms. It can be seen both diodes turn off softly with (ZCS), leading to alleviation of the reverse recovery related losses and EMI. As previously explained the leakage inductor is in series with the diodes and, therefore, control their current decrease rate during turn off. The reverse recovery problem of the diodes is solved, even though the converter has high output voltage.

The voltage stress of output and regenerative diodes is 155 V approximately. Here there is a

discrepancy of 15 V between the experimental and the simulation results in Figure 3.15(f) and Figure 3.15(g). However, the voltage stress of the diodes is less than the converter output voltage. This experimental result further confirms that the diodes voltage stress is less than the converter output voltage. Close up of (ZCS) turn-off performance of the diodes is shown in Figure 3.24, the reverse recovery time (a finite duration of time in which the minority carriers recombine with opposite charges and become neutralized) is very short which clearly indicates that the reverse recovery related loss is alleviated.

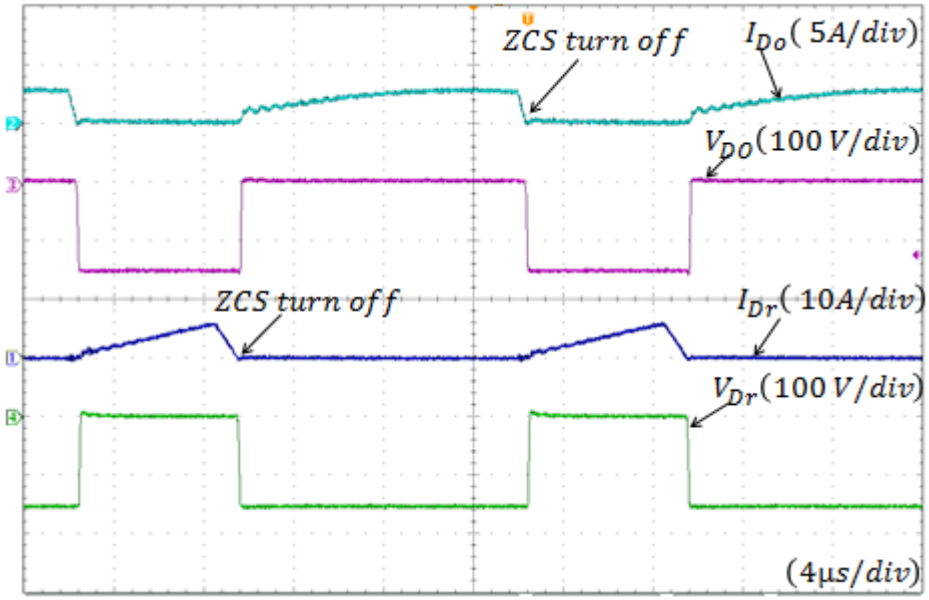

Figure 3.23 Diodes voltage and current waveforms

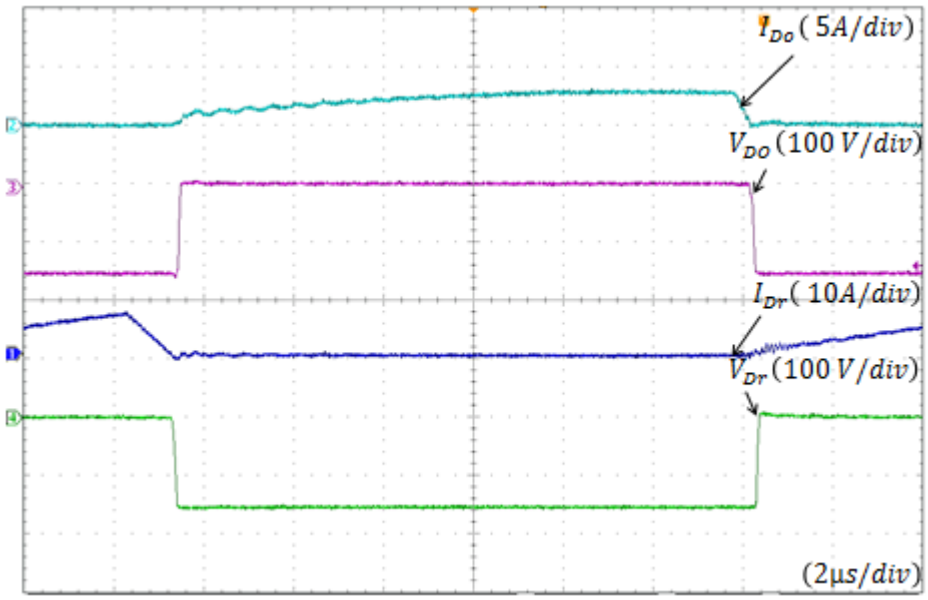

Figure 3.24 Close up of diodes (ZCS) turn off and reverse recovery alleviation

3.8 Efficiency Measurement and Power Loss Analysis

Figure 3.25 shows the simulated and measured efficiency curves of the proposed converter. The maximum simulated efficiency of the converter is 96.8%, whilst good performance is achieved for the entire load range. For instance, the full load efficiency is 95%. The peak measured efficiency of 94.7% is recorded whilst good performance is also achieved for the entire load range. The measured full load efficiency is 93.5%.

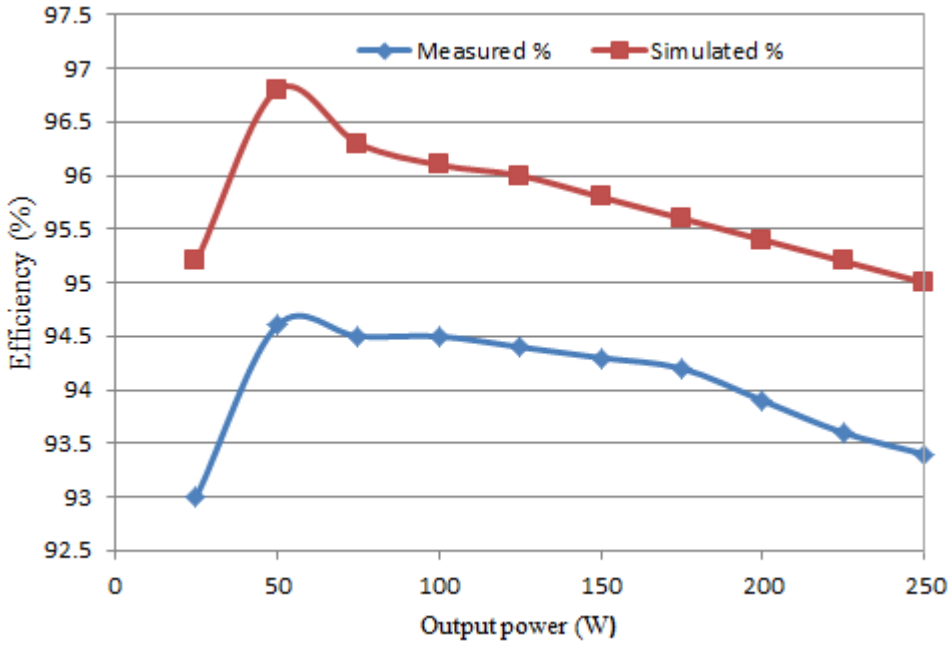

Figure 3.25 Measured Efficiency

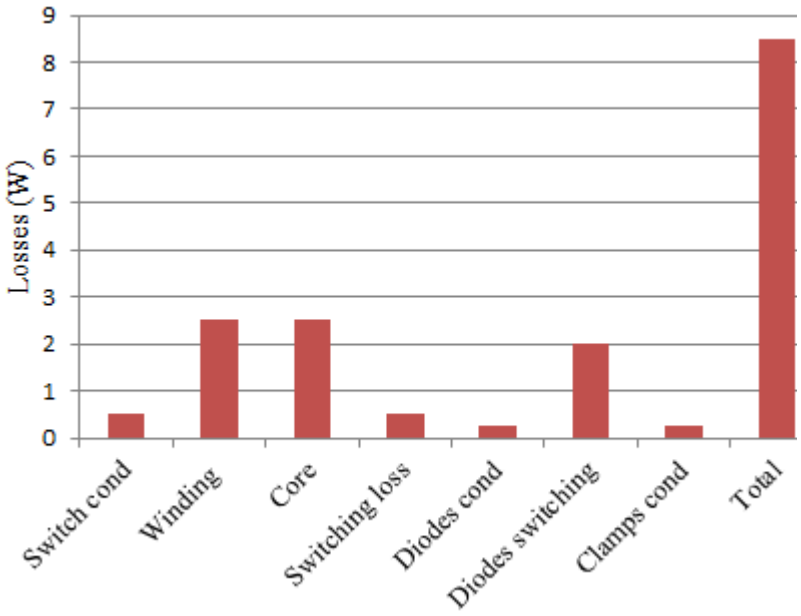

Figure 3.26 Converter loss distribution

Figure 3.26 illustrates the theoretical analysis of the converter losses at full load. The total loss of the converter is 8.5 W. Significant amount of the losses comes from coupled inductor core and iron losses. The iron and core loss of the inductor each contribute 29% of the total converter losses. Power switch and diode conduction losses account for 9% and 24% of the total losses respectively. The switching loss of the main and clamp switches is negligible due to (ZVS) performance. The diodes switching losses and associated reverse recovery related losses are also negligible as a result of (ZCS) turn off operation. Refer to appendix D for detail power loss analysis or calculations of the converter.

3.9 Summary

This chapter presents the theoretical analysis and performance of a new single phase high-step-up boost converter integrating coupled inductor and switched capacitor. The experimental results obtained from the built prototype validate both the theory and operational characteristic of the converter. It is shown that the converter achieved the desired ten times (10X) voltage gain with lower transformation ratio, thereby reducing the volume and losses associated with the coupled inductor. Furthermore, the conversion ratio can be further increased by adjusting the coupled inductor turns ratio. It is also shown that the converter has the advantage of achieving (ZVS) of all the active switches and low circulating current in the clamp circuit. Unlike many of power converters presented in literature, the proposed topology exhibit low devices voltage stress which allow low rated high performance power devices to be used to reduce the conduction loss. The diodes voltage stress is significantly less than the converter output voltage and the low-rated power diodes typically recover faster. The diodes turn off softly with ZCS by utilizing the inherent leakage inductance of the coupled inductor to control their current falling rate. The leakage inductor energy is recycled to the output thus improving the overall efficiency.

Importantly, the results demonstrate that the circuit is capable of achieving high voltage conversion ratio and does not require extreme PWM modulation signals. Such characteristics are desirable features of power converters operating in high step-up applications. The proposed converter is well suited to many industrial applications, such as renewable energy power converters and electric vehicle systems, where high gain power converter technology is becomingly increasingly important.

Chapter 4
Utilization of Passive Clamp Circuit in High Step-up Converter

4.1 Introduction

A high turn-off voltage spike seen by the primary switch of coupled inductor converter (as a result of parasitic oscillation between the coupled inductor leakage inductance and MOSFET parallel capacitor) traditionally requires the use of resistor-capacitor-diode RCD snubber to limit the switch voltage spike. However, the recovered leakage inductance energy dissipates as heat within the snubber. The shortcomings of the RCD snubber can be largely overcome to greater extent by employing clamp circuits (active and passive clamps). Active clamp method has been explored in [16, 48, 50, 73, 84]. The benefits of active clamp circuit include recycling the leakage inductance energy with minimal voltage stress on the power devices. Furthermore, the active clamp circuit (ACC) provides a means of achieving zero voltage switching (ZVS) and lowers the current decrease rate of the output diode. The main drawback of the ACC solution is added complexity, besides cost increase and losses related to the clamp circuit [10, 43]. In addition, any overlap between the main and clamp switch gate signals could lead to short circuit and failure of the circuit.

For this reason, to improve reliability and reduce circuit complexity and cost, a passive clamp circuit (PCC) is sometimes employed. A passive clamp solution is introduced in [10], to reset the leakage inductor energy with minimal circulating current. The operation of the PCC is similar to that of the active clamp counterpart, but it only uses a single switch. From a reliability point of view, converters utilizing a single switch not only reduce the circuit cost and complexity but also increase the lifetime of the converter. Whilst literature shows that the active and passive clamp solutions are the most widely employed approach for recycling the transformer leakage energy in dc-dc converters, a true performance evaluation of the clamp circuits when applied to the same power converter is rarely discussed.

This chapter investigates the performance of passive clamping circuit applied to single phase high step-up converter with voltage extension cell proposed in chapter 3 and compare its performance with that of the active clamp counterpart. The features of the converter employing passive clamp circuit are the same as the active clamp converter, the only distinction being that the passive clamp is employed to replace the active clamp. Therefore, there is no need for additional active device and is isolated gate driver circuit; thus the converter is simplified. The operating principles along with the steady state analysis are described in detail. Simulation, as well as experimental evidence from a 250 W prototype is provided to validate the theoretical results.

4.2 Converter Operational Analysis

4.2.1 Circuit Description

The analysis in section 3.2.2 shows that the antiparallel diode of the clamp switch provides a discharge path naturally for the leakage inductance energy before the application of the gate signal (see figure 3.4c). Therefore, the clamp switch providing the discharge path to the clamp capacitor can be replaced with a diode to form a PCC. The incorporation of a PCC into a single phase high-step-up DC-DC boost converter with voltage extension cell is illustrated in Figure 4.1.

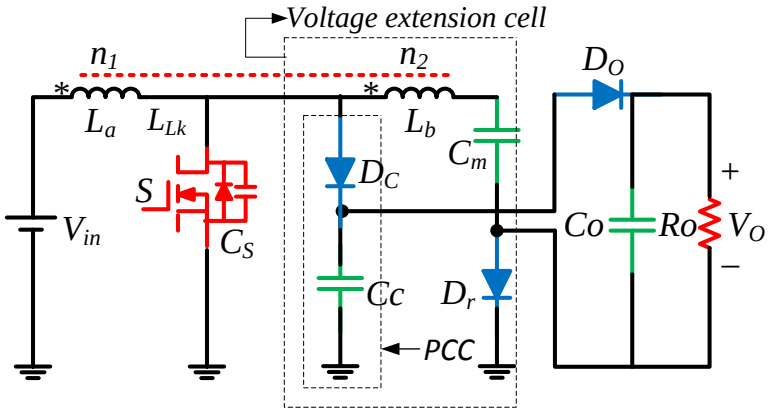

Figure 4.1 Single phase non-isolated DC-DC boost converter with passive clamp

The converter employs one coupled inductor denoted as L. The primary and secondary windings of the coupled inductor were denoted as L_a and L_b respectively. The primary winding L_a serve as filter inductor as in conventional boost converter and is coupled to its corresponding secondary winding L_b. The primary and secondary windings of the coupled inductor is represented by n_1, n_2, and the coupling reference denoted by ‘’*’’. The main

switch is denoted by S. The passive clamp circuit consists of clamping diode D_C and the clamp capacitor C_C. The voltage extension cell consists of the secondary winding of the couple inductors L_b, the clamp diode D_C, clamp capacitor C_C, regenerative diode D_r and the switched capacitor C_m. D_O, C_O are the output diode and filter capacitor; R_O represents the output resistive load.

Figure 4.2 shows the equivalent circuit of the proposed high step-up boost converter. The coupled inductor can be modelled as an ideal transformer with defined turns ratio. The ideal transformer primary winding is connected in parallel with magnetizing inductor L_m and then in series with a leakage inductance L_{Lk} [48, 73, 84]. V_{in}, V_O are the input and output voltages of the converter respectively.

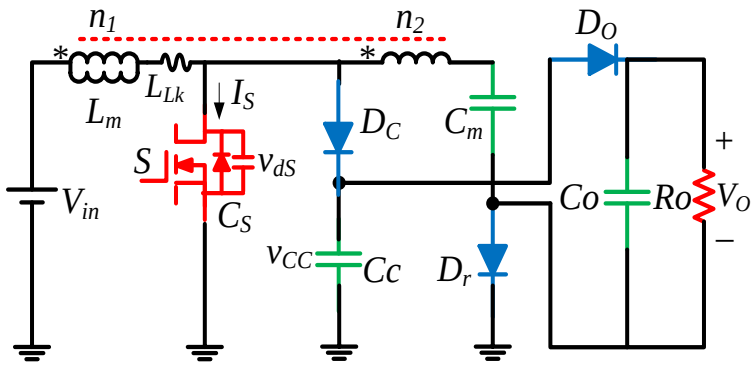

Figure 4.2 Equivalent circuit of the high step-up boost converter

To simplify the converter analysis the following assumptions are made:

- The power switch is ideal, but the parasitic capacitor is considered in the analysis.
- Capacitors C_C, C_m and C_O are large enough. Thus, their voltages are constant in one switching cycle.
- The coupled inductor turns ratio N is defined as n_2/n_1, and the coupling coefficient k is expressed as $L_m/(L_{Lk}+L_m)$.

4.2.2 Modes of Operation

The following discussion is confined to CCM operation since the converter design is based on CCM and such operation is guaranteed throughout the full range of the duty cycle variation under resistive loads similar to the one with active clamping. The clamp diode D_C turns on and turns off naturally. Some typical steady state waveforms of the proposed converter in CCM operation are shown in Figure 4.3. There are five modes of operation in one switching

cycle; the equivalent circuits along with the current flow path corresponding to each operational stage are illustrated in Figure 4.4. The converter operation in CCM is analysed as follows:

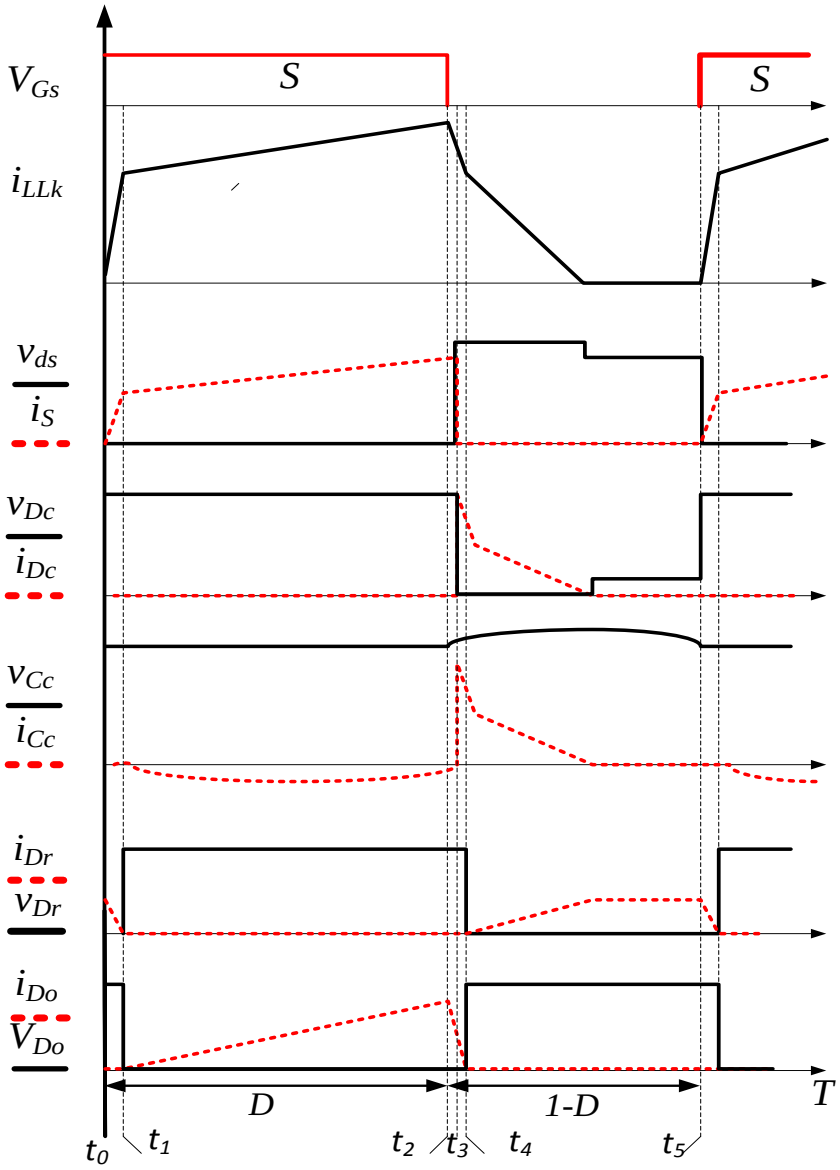

Figure 4.3 Some typical steady state waveforms in CCM operation

Mode 1 $[t_0 - t_1]$ (figure 4.4a): Before time t_1, the main switch S is conducting. The clamp diode D_C and output diode D_O are reversed biased whilst the regenerative diode D_r is forward biased. The current through regenerative diode decreases linearly. The current decrease rate is controlled by the leakage inductance L_{LK}. Magnetizing inductance L_m is charged by the input voltage V_{in} whilst the switched capacitor is charged through the coupled inductor secondary winding. The leakage inductance L_{Lk} resonates with the parallel capacitor of the switch C_S. The output capacitor supplies the load at this time.

$$i_{Lm}(t) = I_{Lm}(t_0) + \frac{V_{in}}{L_m}(t - t_0) \quad (4.1)$$

$$i_{LLk}(t) = i_{LLk}(t) + Asin[\omega(t - t_0) + \phi] \quad (4.2)$$

Where $\omega = (1/N\sqrt{L_{Lk}C_S})$

$$A = \sqrt{\left[\frac{V_{in} - V_{Cs}(t_0)/N}{L_{Lk}} - \frac{V_{in}}{L_m}\right]^2 \Big/ \omega^2 + I_{LLk}(t_0)^2}$$

$$\phi = tan^{-1}\frac{I_{LLk}(t_0)}{\{[V_{in} - V_{Cs}(t_0)/N/L_{Lk} - V_{in}/L_m]\}/\omega}$$

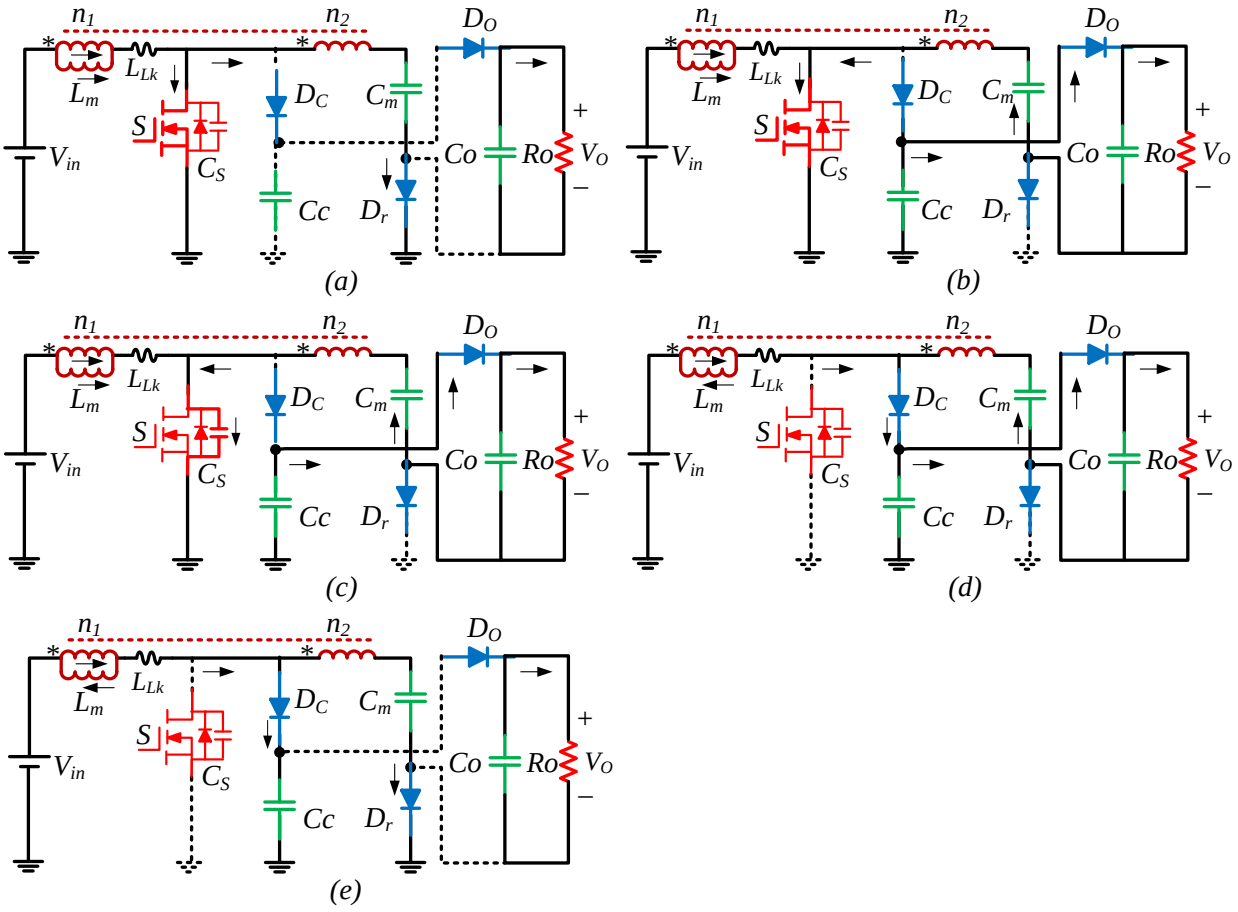

Figure 4.4 Operational modes equivalent circuits showing current flow path
(a) Mode 1 $[t_0 - t_1]$, (b) Mode 2 $[t_1 - t_2]$, (c) Mode 3 $[t_2 - t_3]$, (d) Mode 4 $[t_3 - t_4]$, (e) Mode 5 $[t_4 - t_5]$

Mode 2 $[t_1 - t_2]$ (figure 4.4b): The regenerative diode D_r turns off softly at time t_1 under (ZCS) condition. The output diode D_O becomes forward biased. During this time the clamp capacitor C_C, the switched capacitor C_m and the coupled inductor secondary winding are connected in series to enlarge the voltage gain. Meanwhile, the converter operates in flyback mode to supply the load. A new resonance is formed between the clamp capacitor C_C the switched capacitor C_m and the leakage inductance L_{LK}. The magnetizing inductance and leakage inductance currents can be expressed as follows

$$i_{Lm}(\mathrm{t}) = I_{Lm}(t_1) - \frac{\left(V_{out} - V_{Cm}(t_1) - V_{Cc}(t_1)\right)}{NL_m}(t - t_1) \tag{4.3}$$

$$i_{LLk}(\mathrm{t}) = i_{LLk}(t_1) + A_1 sin[\omega_1(t - t_1) + \phi_1] + \frac{C_c + C_m}{(N+2)C_c + C_m}.i_{Lm}(\mathrm{t}) \tag{4.4}$$

Where $\omega_1 = (1/N\sqrt{L_{Lk}C_cC_m/[(N+2)^2.C_m + C_c]})$

A_1

$$= \sqrt{\left[i_{LLk}(t_1) - \frac{C_c + C_m}{(N+2)C_c + C_m}I_{Lm}(t_1)\right]^2 + \left[\frac{C_c + C_m}{(N+2)C_c + C_m}.\frac{(V_{out} - V_{Cm}(t_1) - V_{Cc}(t_1))}{NL_m} + \frac{V_{Lm}(t_1)}{L_{Lk}}\right]^2 /\omega^2}$$

$$\phi_1 = \pi - tan^{-1}\left\{\frac{\omega_1.(I_{LLk}(t_1) - (C_c + C_m).I_{Lm}(t_1)/[(N+2).C_c + C_m])}{(C_c + C_m).(V_{out} - V_{Cm}(t_1) - V_{Cc}(t_1))/(NL_m(N+2).C_c + C_m) + V_{Lm}(t_1)/L_{Lk}}\right\}$$

Mode 3 $[t_2 - t_3]$ (figure 4.4c): At time t_2 the main switch S turns off, diode D_C and D_r are reversed biased whilst D_O is forward biased. The magnetizing inductor current charges the parasitic capacitor of the switch. This mode is very short and ended when $V_{ds} = V_{Cc}$.

Mode 4 $[t_3 - t_4]$ (figure 4.4d): The voltage across the switch S rises to the clamp capacitor voltage and the clamp diode D_C become forward biased. The leakage inductor current i_{LLk} is commutated to the clamp diode, and the leakage inductance energy is released to the clamp capacitor C_C. The voltage across the switch S is clamped to the clamp capacitor voltage v_{Cc}. During this time, the leakage inductance current and that of output diode D_O decreases linearly. The current decrease rate of the output diode is controlled by the inherent leakage inductance of the coupled inductor.

$$i_{LLK}(\mathrm{t}) = I_{LLk}(t_2) + \frac{V_{Cc}}{L_{Lk}}(t - t_2) \tag{4.5}$$

$$v_{ds}(\mathrm{t}) = V_{ds}(t_2) + \frac{I_{Lm}(t_2)}{C_C}(t - t_2) \tag{4.6}$$

Mode 5 $[t_4 - t_5]$ (figure 4.4e): The output diode turns off softly under (ZCS) condition at time t_4. The regenerative diode D_r begins to conduct; the diode current rises linearly, and that of the leakage inductance decreases linearly. The clamp and switched capacitor are now charged in parallel by the input voltage source V_{in}. The output capacitor supplies the load during this time. At the end of this mode, the clamp diode D_C turns off naturally at time t_5, and the main switch S turns on with (ZCS) performance. Magnetizing inductance i_{Lm} is given by

$$i_{Lm}(\mathrm{t}) = I_{Lm}(t_3) - \frac{\left(V_{Cm}(t_3) - V_{Cc}(t_3)\right)}{NL_m}(t - t_3) \tag{4.7}$$

4.3 Steady State Converter Analysis

4.3.1 Voltage Conversion Ratio

The initial development of static gain expression is considered under an ideal condition in which parasitic elements inherent in the power devices and passive components are not included in the analysis. The magnetizing inductor current is considered linear; the switching period consists of only on and off period. During the power switch turn on instant, the magnetizing inductor is charged linearly by the input voltage. Based on (KVL), the voltage across the primary and secondary windings of the coupled inductor is given by

$$V_{Lm} = V_{\text{in}} \tag{4.8}$$

$$V_{Lb} = NV_{Lm} \tag{4.9}$$

During the same time instant, the diode D_r is reversed biased and the output diode D_O is forward biased, the clamp and switched capacitors discharge in series, the power is transferred to the load; the output voltage can be described by

$$V_o = V_{Cm} + V_{Cc} + NV_{\text{in}} \tag{4.10}$$

Applying the inductor volt-second balance principle for the coupled inductor primary winding L_a, the voltage across the clamp capacitor C_C becomes

$$V_{Cc} = \frac{V_{in}}{(1-D)} \tag{4.11}$$

When the main switch *S* turns off, the clamp and regenerative diodes turns on, the clamp and switched capacitors are charged in parallel by the input voltage, the voltage across the switched capacitor is derived as

$$V_{Cm} = N(V_{Cc} - V_{in}) + V_{Cc} \tag{4.12}$$

From (4.10) - (4.12) the ideal voltage gain is derived

$$M_{ideal} = \frac{V_o}{V_{in}} = \frac{N+2}{(1-D)} \tag{4.13}$$

The static gain of the converter can be enlarged by adjusting the coupled inductor turns ratio N. Extreme duty cycle can be avoided by proper turns ratio design to achieve the desired voltage conversion ratio. In the derivation of the ideal static gain in (4.13), the leakage inductance is neglected. However, it is practically impossible to achieve hundred percent coupling between the primary and secondary windings of the coupled inductor. The passive clamp circuit is usually employed to limit the switch voltage excursion. The ZCS turn on

performance of the switch is achieved due to leakage inductance. Furthermore, to control the current falling rate of the diodes which results in decreased switching loss and EMI noise, the inclusion of the leakage inductance in the analysis is necessary. For this reason, the leakage inductance is considered in the voltage gain derivation. Neglecting the short operating intervals, the voltage V_O across the output capacitor during on and off intervals is given by

$$C_O \frac{dv_O}{dt} = \frac{v_O - v_{cm} - v_{Cc} - Nv_{in}}{NL_K} - \frac{v_O}{R_O} \tag{4.14}$$

$$C_O \frac{dv_O}{dt} = -\frac{v_O}{R_O} \tag{4.15}$$

Now using state space average method [99], the average equation that describes equation (4.14) and (4.18) is given by

$$\langle \frac{dv_O}{dt} \rangle = \frac{(NL_K f_s(N + dN) + dR_o)d'v_o}{NL_K C_o R_o d} - \frac{v_{in}(N+2)}{NL_K C_o} \tag{4.16}$$

Where $d' = (1 - d)$. The state space average DC model that describe the equilibrium point of the output voltage can be obtained by letting the left-hand side (LHS) of equation (4.19) equal to zero. From which the voltage gain is obtained after making M the subject of the equation.

$$M = \frac{V_o}{V_{in}} = \frac{N+2}{(1-D)} \cdot \frac{DR_o}{(NL_K f_s(N + DN) + DR_o)} \tag{4.17}$$

The relationship between the static gain, duty cycle, turns ratio and leakage inductance is plotted in Figure 4.5 . As can be seen, the voltage gain increases significantly with increased turns ratio. Conversely, the leakage inductance degrades the voltage gain of the converter.

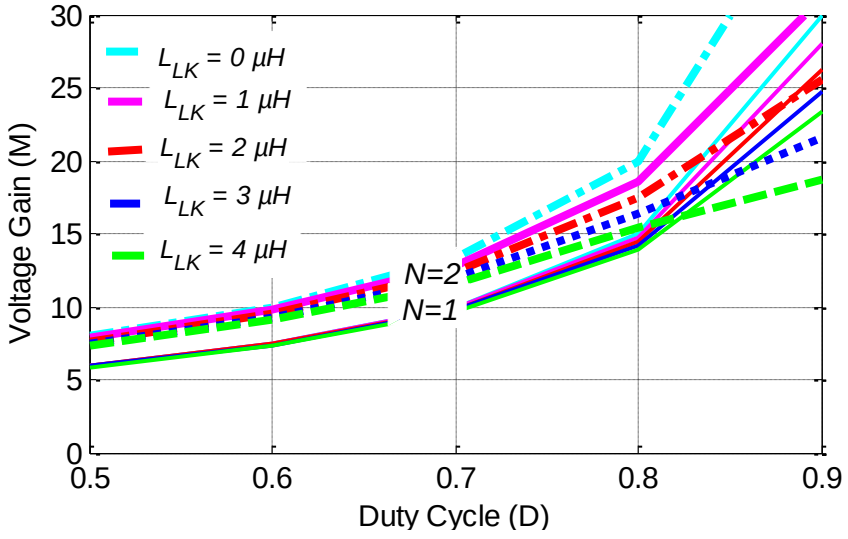

Figure 4.5 Voltage conversion ratio as a function of *D* and *N* values

Based on the preceding analysis, the leakage inductance causes duty cycle loss which leads to the static gain loss given by

$$\Delta D = \frac{2I_{in}L_{LK}f_S}{V_{in}D + NDV_O} \tag{4.18}$$

From (4.18) it can be concluded that the duty cycle loss is proportional to the input current, leakage inductance and switching frequency.

4.3.2 Power Devices Voltage Stress

By neglecting the voltage ripple on the clamp capacitor, the voltage stress of the switch S and clamp diode D_C are obtained from (4.13). The switch and clamp diode voltage stress are the same and are equal to the clamp capacitor voltage. The switch voltage V_{ds} is given by

$$V_{ds} = V_{Dc} = \frac{V_{in}}{(1-D)} = \frac{V_O}{(N+2)} \tag{4.19}$$

The voltage stress of the output diode D_O is the same with that of the regenerative diode, which is equal to the difference between the output voltage and the clamp capacitor voltage. However, it is always lower than the output voltage and is expressed as

$$V_{DO} = V_{Dr} \cong V_O - V_{CC} = \frac{(N+1)V_{in}}{(1-D)} = \frac{(N+1)V_O}{(N+2)} \tag{4.20}$$

From (4.19) and (4.20), the curve relating the normalized semiconductor devices voltage stress to $V_O$and the coupled inductor turns ratio is plotted in Figure 4.6. When the turns ratio is zero, the switch voltage stress is equal to half of the output voltage. And the switch voltage stress decreases significantly when the turns ratio increases. Therefore, low-rated high-performance power device can be employed to improve the circuit efficiency. Likewise, the voltage stress of the regenerative and output diode increases as the turns ratio increases.

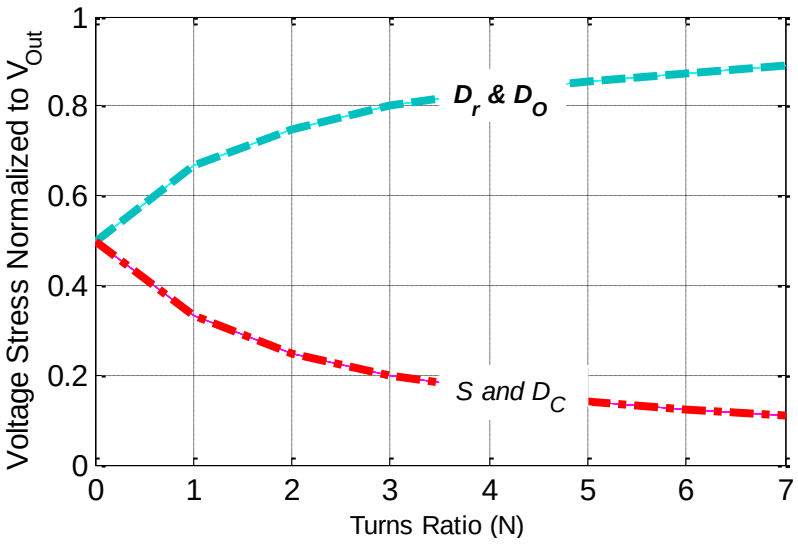

Figure 4.6 Semiconductors devices voltage stress reduction effect

4.3.3 Current Stress

The current stress of the converter main switch is similar to the active clamp counterpart. For detail derivation, refer to Section 3.3.3. However, the current stress of the clamp diode is derived with the aid of Figure 4.3. It is assumed that the clamp diode conducts during half period of the off time duration. The peak current of the clamp diode during the turn on instant is the turn-off current of the main switch S. The clamp diode RMS current can be derived considering the clamp diode current to be piecewise linear for the half of the off time interval and is obtained as

$$I_{RMS\_Dc} = \sqrt{\frac{1}{T_S}\int_0^{(1-D)T_s/2} {i_{Dc}}^2(t)dt} = I_o\left(\frac{2(N+D)}{(1-D)D} + \frac{N}{(1-D)}\right)\sqrt{\frac{(1-D)}{6}} \tag{4.21}$$

4.3.4 Diodes Reverse Recovery Alleviation

The current falling rate of the output diode is controlled by the leakage inductance of the coupled inductor during mode 3 and is given by

$$d\frac{i_{Do}}{dt} = \frac{v_{Lk}(t)}{NL_{Lk}} \tag{4.22}$$

And the voltage across the leakage inductor v_{Lk} is derived as

$$v_{Lk}(t) = V_{Cc} - V_{in} + \frac{(V_O - V_{Cm} - V_{Cc})}{N} \tag{4.23}$$

From (4.22) and (4.23), the current falling rate of the output diode can be simplify as

$$d\frac{i_{Do}}{dt} = \frac{V_O}{N(N+2)L_{Lk}} \tag{4.24}$$

For the regenerative diode, its current falling rate is equally controlled by the leakage inductance at the end of mode 4 and is given by

$$d\frac{i_{Dr}}{dt} = \frac{v_{Lk}(t)}{NL_{Lk}} \tag{4.25}$$

And v_{Lk} during this instant is obtained as

$$v_{Lk}(t) = V_{in} + \frac{(NV_{Cc} - NV_{in} + V_{Cc})}{N} \tag{4.26}$$

From (4.25) and (4.26), the current falling rate of the regenerative diode becomes

$$d\frac{i_{Dr}}{dt} = \frac{(N+1)V_O}{N(N+2)L_{Lk}} \tag{4.27}$$

From (4.24) and (4.27), it can be concluded that the reverse recovery problem can be alleviated effectively by using the inherent leakage inductance of the coupled inductor to control the current falling rate of the diodes. Furthermore, as the turns ratio increases, a small leakage inductance is sufficient to alleviate the reverse recovery problem.

4.4 Circuit Design

As previously explained, one of the motivations of this work is to investigate the performance of energy recycling schemes (the passive and active clamp circuits) when applied to the same high step-up converter topology. Fair evaluation and comparison between both schemes would be easy under similar topology with the same specification. For this reason, the design procedure and component selection of the components of the active clamp converter in chapter 3 section 3.5 are maintained. However, the active switch is replaced with the passive diode that can withstand similar voltage and current stress (see equation 4.16 and 4.18).

4.5 Simulation Verification

A Matlab-Simulink platform is used to investigate the performance of the converter and to verify the analytical model. A 250 W closed loop converter has been modelled and simulated under full load condition with 20 V input voltage. The closed loop control scheme is an average current mode controller comprising of two digital PI controllers in voltage and current loops. There is time separation between the controllers to allow the current to change quickly than the voltage. Refer to Appendix A for detail description of the closed loop model of the converter. Converter parameters used for simulation are listed in Table 3.2.

The drain-source voltage and current waveform of the main switch are shown in Figure 4.7(a). It is clear that (ZCS) turn on is achieved by the main switch which reduces the switching losses during turn on. Figure 4.7(b) presents the waveforms of the clamp diode, and that of clamp capacitor is illustrated in Figure 4.7 (c). Note that, the voltage stress of the main switch, the clamp diode and clamp capacitor is the same. The maximum voltage stress is 60 V, which is by far less than the output voltage. It is worth noting from the clamp diode current in Figure 4.7(b), that only half of the main switch off period is used to recover the leakage inductor energy and suppress the voltage spikes. Figure 4.7(d) shows the leakage inductor current, which is the net magnetizing inductor current and the reflected secondary current. The current and voltage stress of the diodes are shown in Figure 4.7(e) - (f) featuring (ZCS)

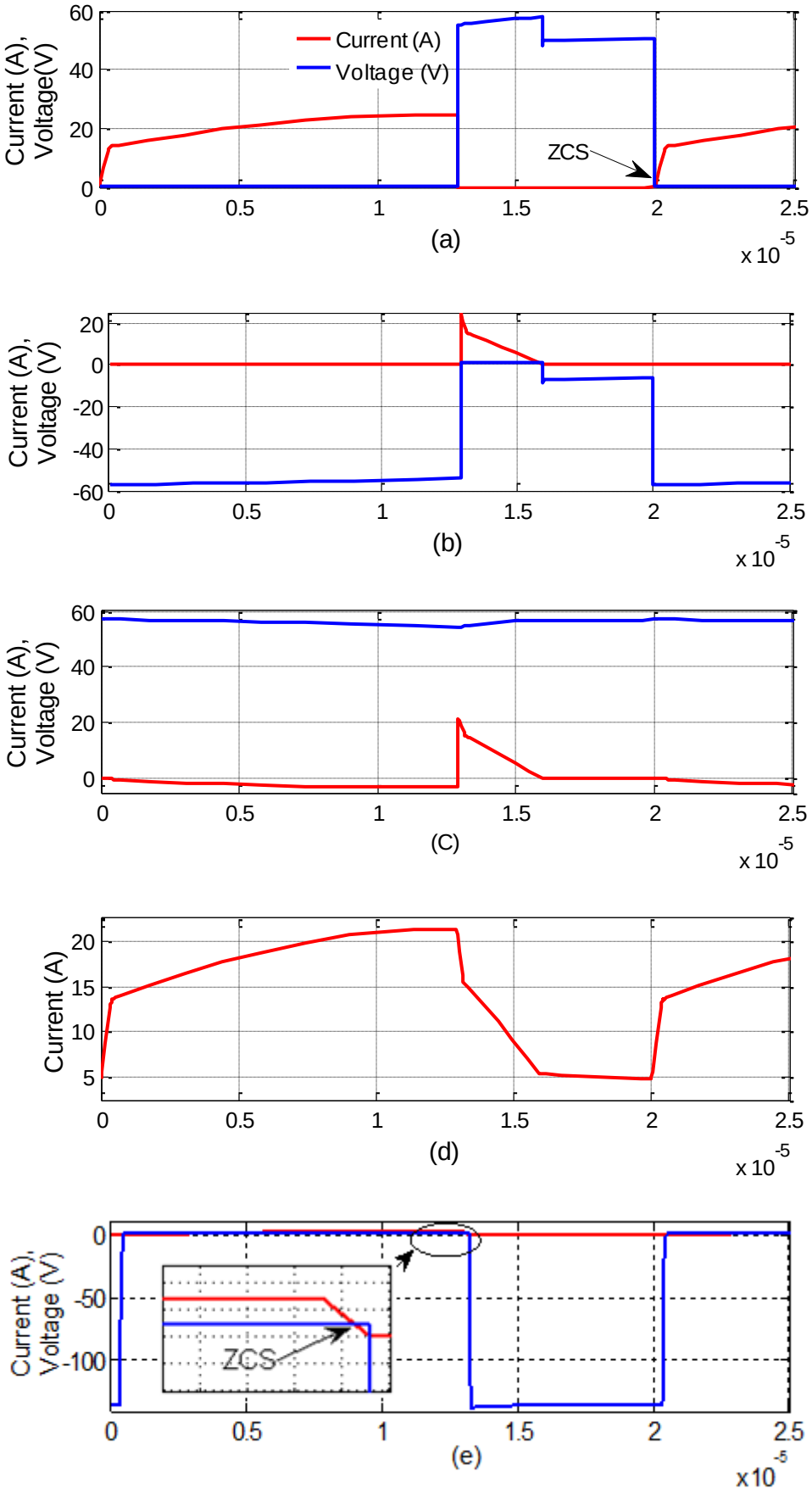

Figure 4.7 Simulation Results
(a) primary switch waveforms (b) clamp diode waveforms (c) passive clamp circuit performance
(d) leakage inductor current (e) regenerative diode voltage and current stress

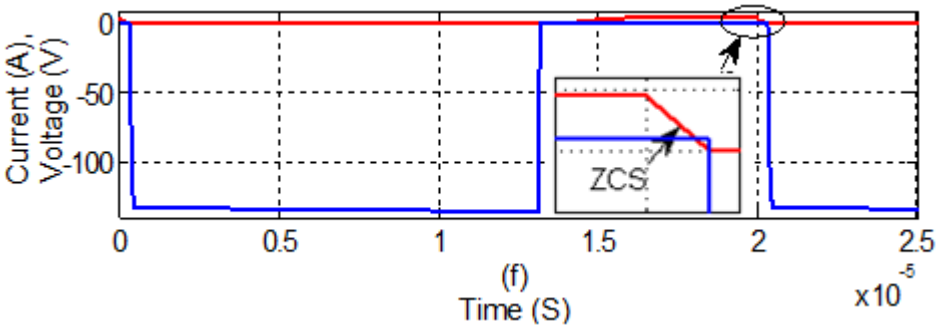

Figure 4.7 (Continued) Simulation results
(f) output diode voltage and current waveform

turn-off, the voltage stress is 140 V, which is less than the converter output voltage. The simulation results presented so far are in agreement with the analysis in section 4.3 and further highlight the advantages of the proposed topology and passive clamp scheme. Experimental Validation

4.5.1 High Step-up Passive Clamp Boost Converter Prototype

In order to verify the operation and evaluate the performance of the converter, a 250 W prototype has been implemented in the laboratory and tested. The parameters of the converter along with the component ratings are derived from Section 3.5. The specifications are listed in Table 3.2. Figure 4.8 shows the photograph of the power converter prototype, the dimension is (120 x 110 x 45) mm. As can be seen, there is only one provision of gate drive signal.

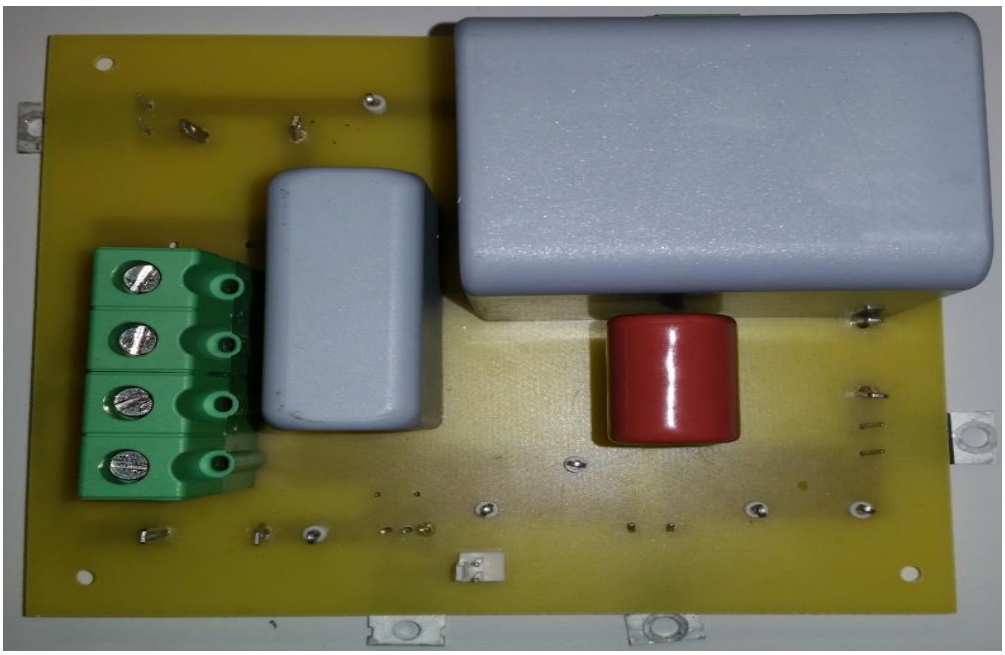

Figure 4.8 Photograph of the experimental prototype

The experimental set-up is the same with that of active clamp boost converter in section 3.7.1. The coupled inductor is also the same toroidal Kool mμ magnetic core 0077110A7 from Magnetics© Inc used in Chapter 3 (see section 3.7.1). Refer to Appendix B for detail hardware description, Appendix C for details description of the control overview including the microcontroller, gate drive sensor measurements and complete experimental set-up and Appendix D for the gate drive interface and measurements.

4.5.2 Experimental Results

The converter prototype has been tested under $250\,W$ full load condition with $20\,V$ input voltage. The measured drain-source voltage of the power switch v_{dS} and the switch currents I_s are shown in Figure 4.9. (ZCS) soft switching performance of the switch is achieved during turn on instant, which reduces the switching losses significantly. It can be seen that before the switch turns on, the switch current is zero and rises almost linearly from zero during turn on. Unlike the active clamp circuit, the magnetizing current to achieve (ZCS) is not bidirectional. Furthermore, the maximum voltage across the switch is approximately $60\,V$, which is far lower than the output voltage. Based on this, low rated device with low on-state resistance can be employed to reduce the conduction loss. The key advantage of passive clamp approach is, only one power switch is utilized. Therefore, only one isolated gate drive is required, and the reliability is increased. The power switch off period $(1-D)$ is 0.34, and this clearly indicate a proper duty cycle operation is obtained due to reasonable coupled inductor turns ratio design.

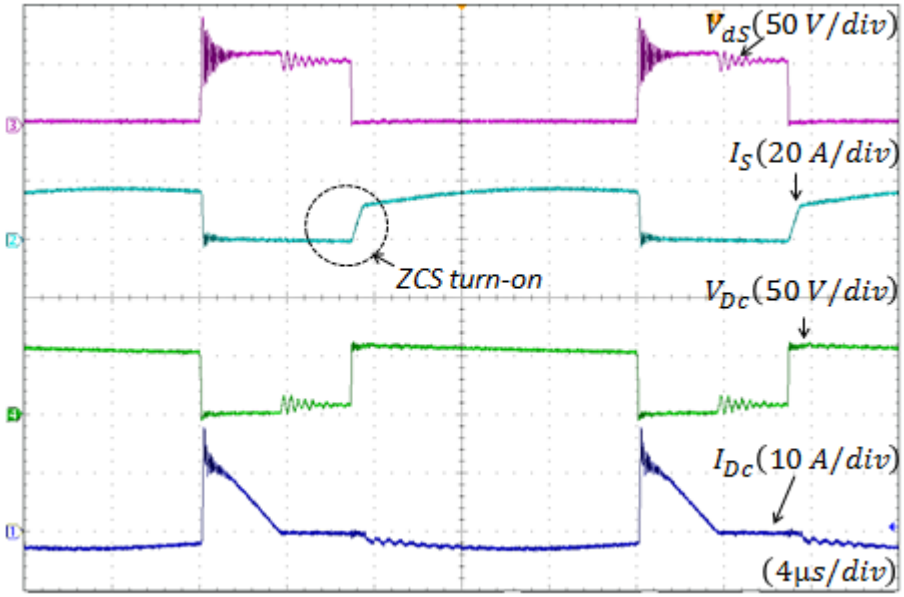

Figure 4.9 Main switch and clamp diode current and voltage waveforms

The current and voltage stress of the clamp diode are also shown in Figure 4.9. As can be seen, the maximum voltage stress of the clamp diode is the same with that of the primary switch. Details of (ZCS) soft switching performance of the switch is further illustrated in Figure 4.10.

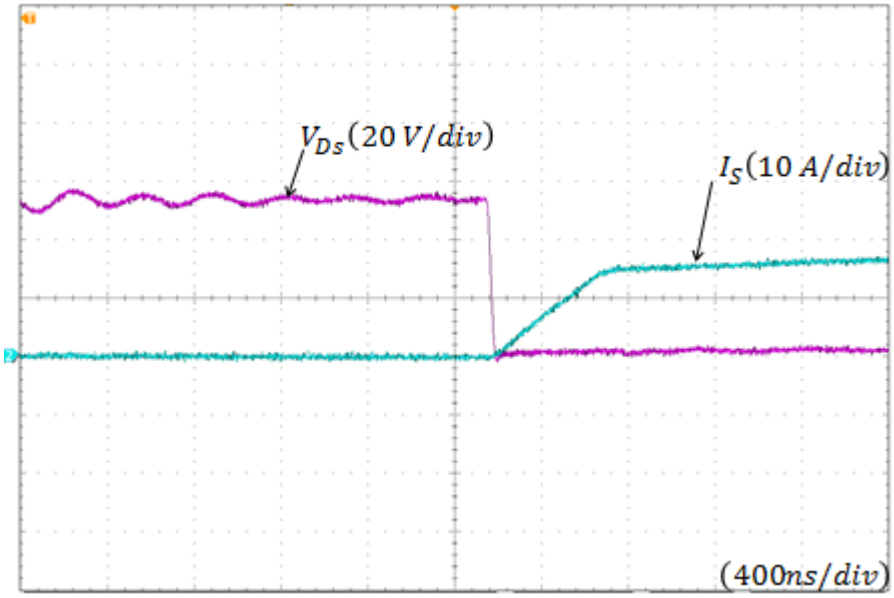

Figure 4.10 (ZCS) turn on detail of the main switch

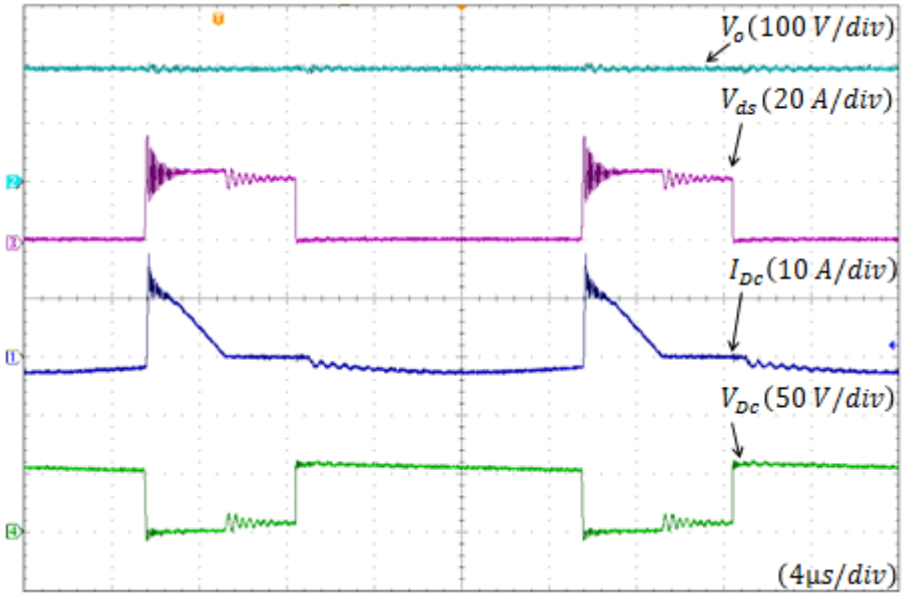

Figure 4.11 Passive clamp circuit performance

Figure 4.11 illustrate the clamp circuit performance. The waveforms comprise the measured output voltage, drain-source voltage of the primary switch and clamp diode waveforms. As can be seen, the PCC achieves a similar level of performance of the active clamp counterpart by suppressing the voltage spikes of the switch when the main switch turns off. However,

only part of the off duration period is used for resetting the leakage inductor energy. More details of clamp circuit performance are shown in Figure 4.12, which include the clamp capacitor voltage instead of drain-source voltage of the primary switch. The voltage stress of these devices is 60 V, a good agreement of both the simulation and steady state analysis.

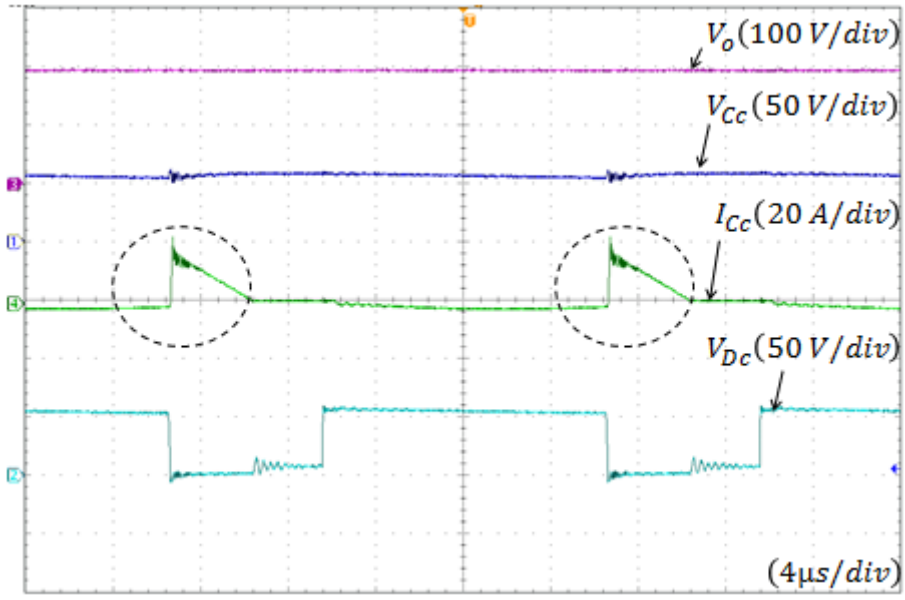

Figure 4.12 Clamp Capacitor current and voltage waveforms

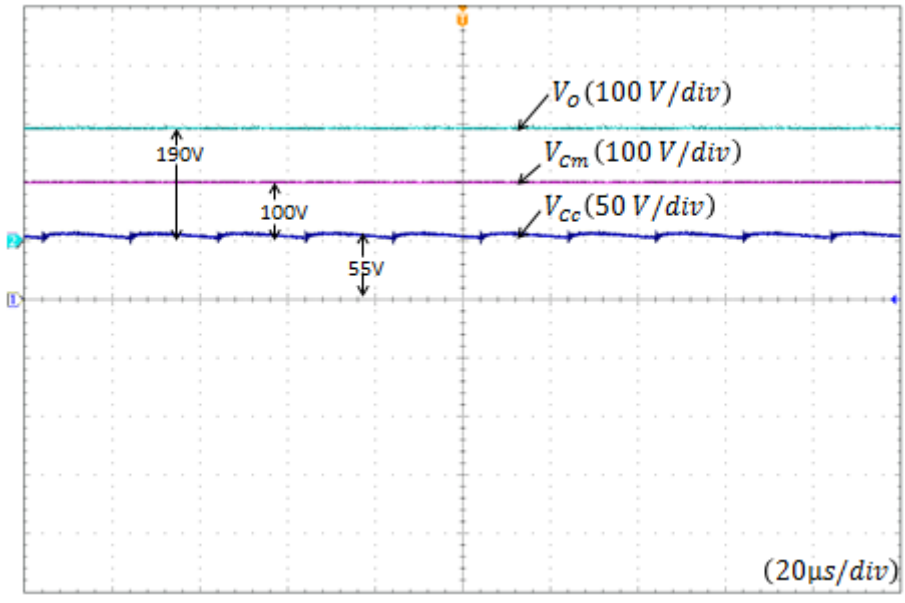

Figure 4.13 Capacitors voltage stress

Figure 4.13 illustrates the voltage across the capacitors (clamp, switched and the output capacitors) of the converter. The experimental result validates the initial assumption of considering the capacitors as constant voltage sources.

Figure 4.14 shows the measured waveforms of regenerative and output diodes. It can be seen

both diodes turn off softly with (ZCS) leading to alleviation of the reverse recovery related losses. Because both diodes are in series with the secondary windings of the coupled inductor, the leakage inductor controls the current decrease rate of the diodes. The reverse recovery problem of the diodes is completely solved, even though the converter has high output voltage. As shown in Figure 4.14, the voltage stress of the regenerative and output diodes is 155 V approximately. Figure 4.15 shows the close up trace of the (ZCS) turn off of diodes.

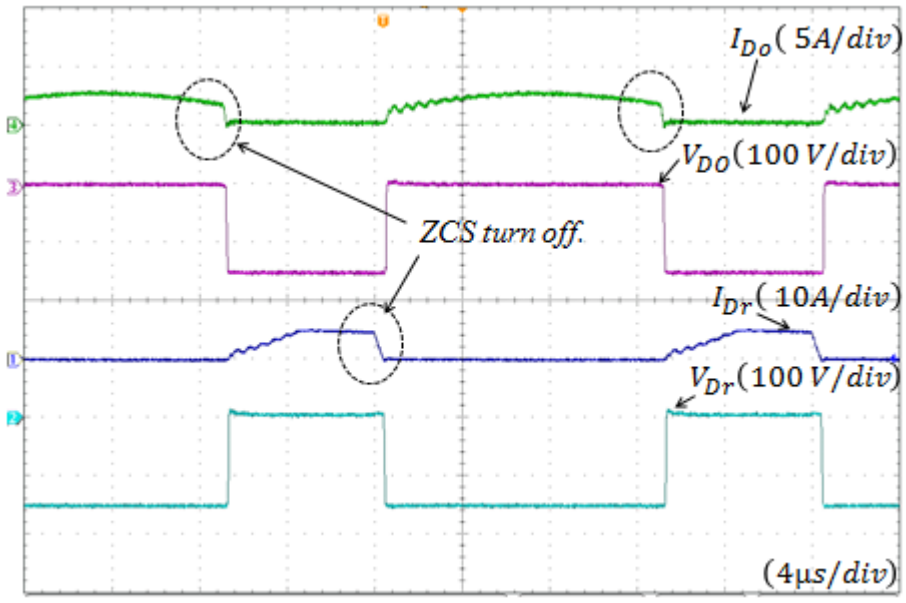

Figure 4.14 Diodes measured current and voltage waveforms

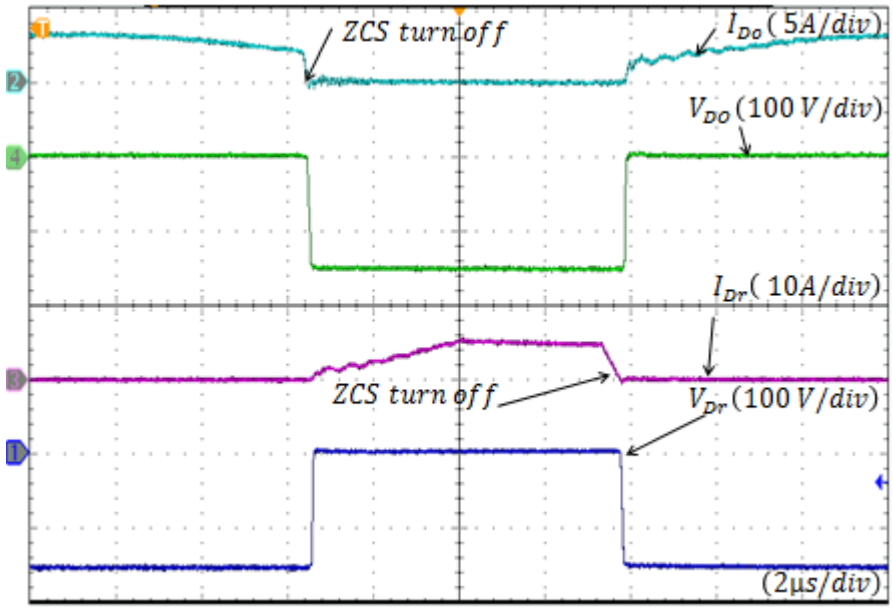

Figure 4.15 Diodes (ZCS) turn off and reverse recovery alleviation

Figure 4.16 illustrate the leakage inductor current (the coupled inductor primary current). The measured peak to peak ripple current is 19 A, As previously explained, the large ripple is

related to the operation of the coupled inductor; which is basically the summation of the magnetizing inductor current and secondary winding reflected current. The leakage inductor current is continuous for the entire switching cycle; it is fair to conclude that the theoretical analysis and the simulation results of the leakage inductor current are in agreement with the experimental result.

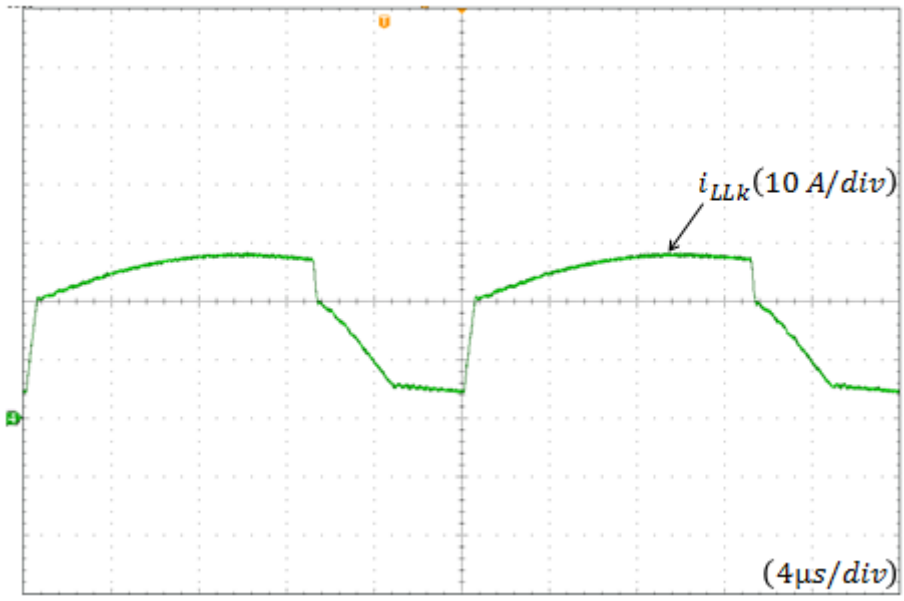

Figure 4.16 leakage inductor current waveform

4.6 Performance Comparison

In this section, the simulated results of the proposed high step-up PCC and the measured experimental results are compared with the calculated results. The comparison is performed under full load rated conditions. The comparison covers power devices voltage and current stresses, operating duty cycle etc., and the results are listed in Table 4.1. The calculated duty cycle is 0.6 whereas the simulated and measured duty cycles are 0.65, 0.66 respectively. This is related to the fact that the calculation is based on the ideal components. Whilst in practice, the components are non-ideal, loses due to coupled inductor (core and copper), power devices (switching and conduction) diodes conduction and forward voltage drop are inherent in the devices.

Note also, the slight variation between the measured, simulated and calculated current and voltage stress on the converter power devices. Overall, the results agree closely with one another.

Table 4.1 Comparison between the simulated, measured and calculated results of PCC

Topology		Simulated	Measured	Calculated
Operating duty cycle		0.65	0.66	0.6
Turns ratio		1:1.8	1:1.8	1:1.8
Power switch	V_{pk}	58 V	60 V	50 V
	I_{pk}	24 A	19 A	25 A
Clamp diode	V_{pk}	58 V	60 V	50 V
	I_{pk}	24 A	19 A	25 A
Regenerative diode	V_{pk}	140 V	155 V	140 V
	I_{pk}	5 A	5 A	6 A
Output diode	V_{pk}	140 V	155 V	140 V
	I_{pk}	3 A	3 A	4 A
Capacitors	Clamp	58 V	60 V	50 V
	Switched	104 V	100 V	104 V
	Output	190 V	190 V	190 V

4.7 Topologies Comparison

In order to clearly distinguish between the performances of the clamp schemes (active and passive) and demonstrate the advantages of one scheme over the other, performance evaluation and comparison is made between high step-up converter with active clamping and the high step-up converter employing passive clamping described to this end.

4.7.1 Power Devices Voltage Stress

Table 4.2 shows the voltage stress comparison of the power devices in both the passive and active clamp converters. Although the two converters use different clamping approach, however, the voltage stress of both circuits appears to be the same. (i.e. the voltage stress of the clamp switch is the same with that of the clamp diode). All other semiconductors in the two circuits have the same voltage stresses (regenerative and output diode). The only distinction is related to the active components used. Active clamp converter has two active switches and two diodes whereas the passive clamp circuit has one active switch and three diodes respectively.

Table 4.2**:** Devices voltage stress comparison between passive and active clamp converters

Topology	Passive Clamp Converter	Active Clamp Converter
Number of active switches	1	2
Number of Diodes	3	2
Voltage gain	$\frac{(N+2)}{(1-D)}$	$\frac{(N+2)}{(1-D)}$
Voltage stress of main switch	$\frac{V_O}{(N+2)}$	$\frac{V_O}{(N+2)}$
Voltage stress of clamp switch	-	$\frac{V_O}{(N+2)}$
Voltage stress of clamp diode	$\frac{V_O}{(N+2)}$	-
Voltage stress of regenerative and output diodes	$\frac{(N+1)V_O}{(N+2)}$	$\frac{(1+N)V_O}{(N+2)}$

4.7.2 Current Stress

Table 4.3 illustrate the current stress comparison of the passive and active clamp converters considering unity conversion efficiency. The main switch of both converters exhibits the same current stress, likewise the clamp switch, clamp diodes and the output diodes. The regenerative diode of passive clamp converter suffers a slightly higher current stress when compared with active clamp counterpart.

Table 4.3**:** Semiconductors current stress comparison between passive and active clamp converters

Topology	Passive Clamp Converter	Active Clamp Converter
Current gain	$\frac{(N+2)}{(1-D)}$	$\frac{(N+2)}{(1-D)}$
Current stress of main switch	$I_{in}+\frac{2NI_O}{D}$	$I_{in}+\frac{2NI_O}{D}$
Current stress of clamp switch	-	$I_{in}+\frac{2NI_O}{(1-D)}$
current stress of clamp diode	$I_{in}+\frac{2NI_O}{(1-D)}$	-
Current stress of regenerative diode	$\frac{I_{in}}{N}$	$\frac{2I_{in}}{(N+2)}$
Current stress of output diode	$\frac{2I_O}{D}$	$\frac{2I_O}{D}$

4.7.3 Clamp Circuits Performance

The ACC provides a mechanism of recycling the leakage inductance energy and minimizes the switch voltage stress. However, the loss related to the active clamp switch could be significant in some applications [10, 16]. The current through the clamp switch is the high input current and consequently increases the conduction loss. In addition, the active clamp solution requires two switches and their corresponding isolated gate drivers.

Figure 4.17 shows a typical active clamp capacitor charge and discharge current waveform (see Figure 3.15(c) and Figure 3.22) assuming linear clamp current waveform with equal but opposite end points. As can be seen, the ACC utilizes the entire off period of the main switch to reset the leakage inductor energy. Half of the switch off period (t_1-t_2) is used to transfer the leakage inductance energy to the clamp capacitor whilst the remaining half (t_2-t_3) is used in recycling the leakage energy to the output. The forward charging current and reverse discharging current is the converter input current, which flows either through the active clamp switch S_C or its antiparallel diode. This circulating current results in high conduction loss in the clamp switch. However, in the proposed topology the reverse discharge current is the secondary reflected magnetizing current (I_{Lm}/N) and is much smaller than the primary magnetizing current. The discharging current becomes much smaller if the turns ratio is increased. In essence, there is low circulating current flowing through the switch during clamp capacitor discharge period.

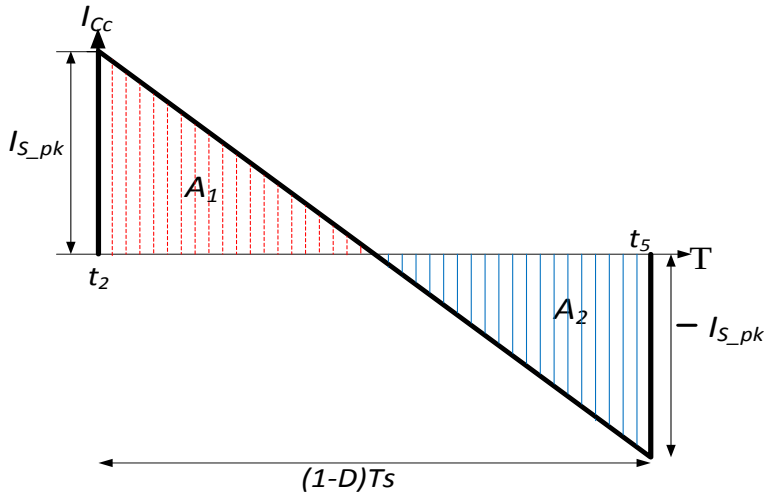

Figure 4.17 Typical active clamp circuit current waveform

Figure 4.18 shows a typical current waveform of passive clamp circuit (see also Figure 4.7(c) and Figure 4.11). The clamp diode provides a natural charging path of the clamp capacitor after the main switch turns off whilst the secondary reflected current serve as the discharge

paths of the clamp capacitor. The time required to recover the leakage energy stored in L_{LK} by the clamp capacitor is denoted by $(t_1 - t_2)$. The dotted area B_1 denotes the clamp capacitor stored energy during charging. The area is much smaller than that of the active clamp counterpart. There is no discharge path of the clamp capacitor energy via the clamp diode, and the energy goes directly to the output. There is no loss related to the clamp capacitor discharge.

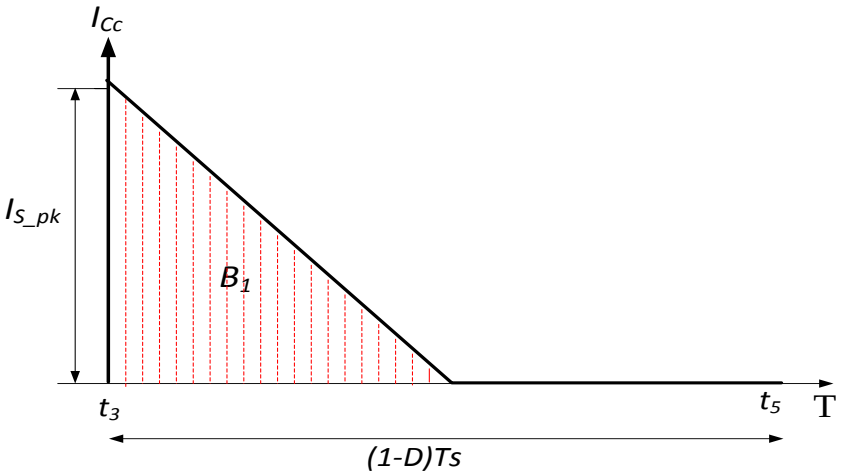

Figure 4.18 Passive clamp circuit current waveform

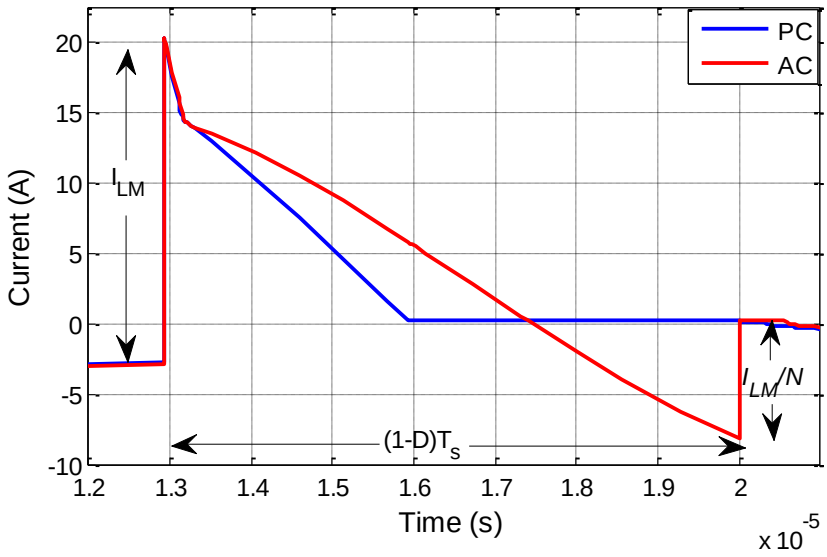

Figure 4.19 Simulated clamp circuits behaviour

Figure 4.19 compare the simulation results of passive and clamp circuits incorporated on the same high step-up converter (see Figure. 3.1 and Figure 4.1). It is apparent that the ACC utilizes the entire off period to reset the leakage inductor energy and more than half of the off period is used in charging the clamp capacitor and the remaining in recycling the leakage energy to the output. The forward charging current is the primary current of the coupled

inductor whilst the reverse discharge current is the secondary reflected magnetizing current (I_{Lm}/N) and is much smaller than the primary magnetizing current. On the contrary, the passive clamp solution requires less than half of the off time duration to recycle the leakage inductor energy. However, the forward charging current stress in both schemes is identical.

4.7.4 Loss Break down Comparison

Analogous to active clamp converter in Chapter 3, the parasitic elements contributes significantly to losses in the converter, in particular, the converter efficiency. The method of estimating the losses regarding each component is explained in Appendix E.

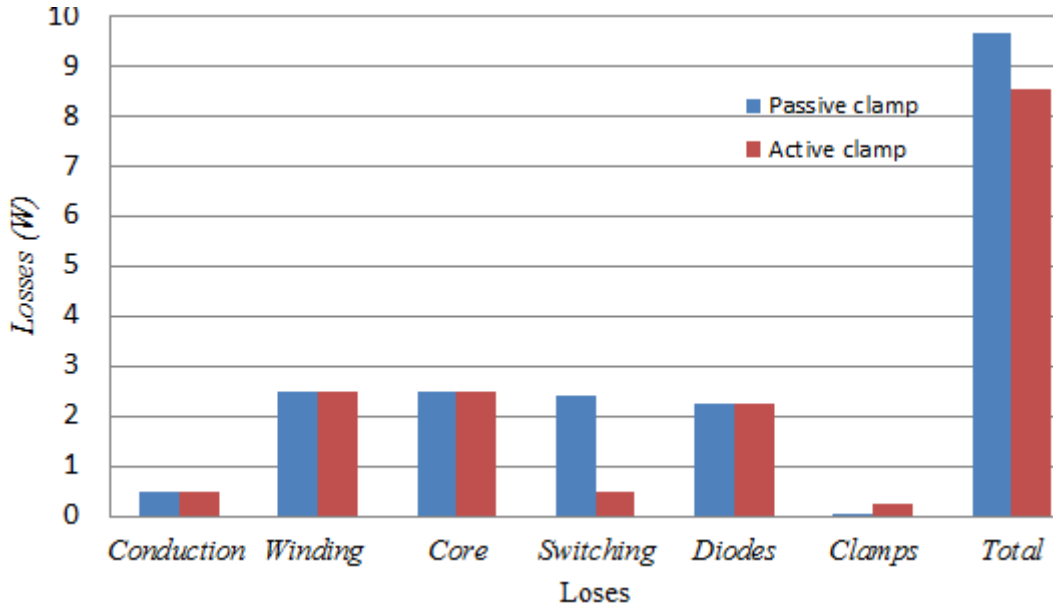

Figure 4.20 Loss breakdown comparison

Figure 4.20 demonstrates the loss breakdown comparison of the passive and active clamp converters under the same operating conditions. The active clamp converter has an advantage of less switching losses as a result of (ZVS) of active devices. The passive clamp exhibits less conduction loss because there is discharge path of the clamp capacitor energy via the clamp diode. The clamp capacitor is discharged by the secondary current of the coupled inductor and the leakage energy is directly recycled to the output. Whereas in the ACC, the clamp switch and is antiparallel diode conducts both the forward charging and reverse discharging current resulting in a two way conduction loss.

4.7.5 Efficiency

The efficiency of the proposed circuits are measured with a (YOKOGAWA WT 310) digital

power meter. Figure 4.21 shows the efficiency comparison between the active and passive clamp converters under different loads condition. The highest efficiency of the active clamp converter is 94.7%, and the overall efficiency is higher than 94% over a wide load range. Compared with the passive clamp converter, there is approximately 1% efficiency difference at both full and light load conditions.

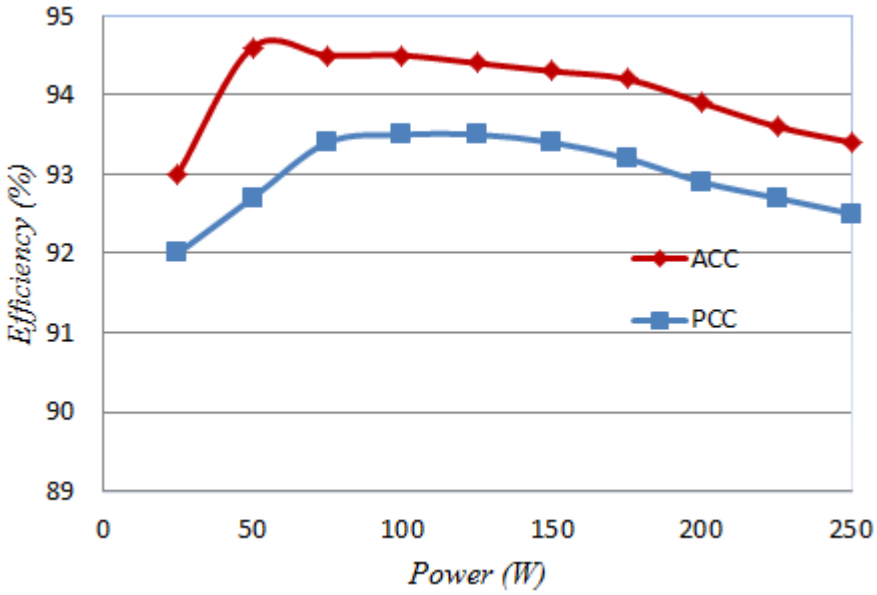

Figure 4.21 Efficiency curves

4.8 Closed Loop Response

Figure 4.22 illustrates the control strategy used for investigating the dynamic performance of the converter in a closed loop. It is a typical dual loop control, comprising the inner current loop and outer voltage loop. The output voltage changes as the load shift and the detected feedback signal are processed via proportional-integral (PI) controller. The outer voltage loop provides the reference of the inner current loop, and this reference is compared with the measured input current, and the error is processed via the inner current loop PI controller [121]. The compensator gains are tuned manually using the Zeigler-Nichols method in [122]. The inner voltage loop has faster dynamics than the inner current loop. In other words, the inner current changes more quickly than the outer voltage loop (time separation). The (PWM) gate signal is generated from the ePWM module of Texas Instrument DSP board TMS320F2833 (see Appendix C). Hall effect sensors are used to measure the converter output voltage and currents.

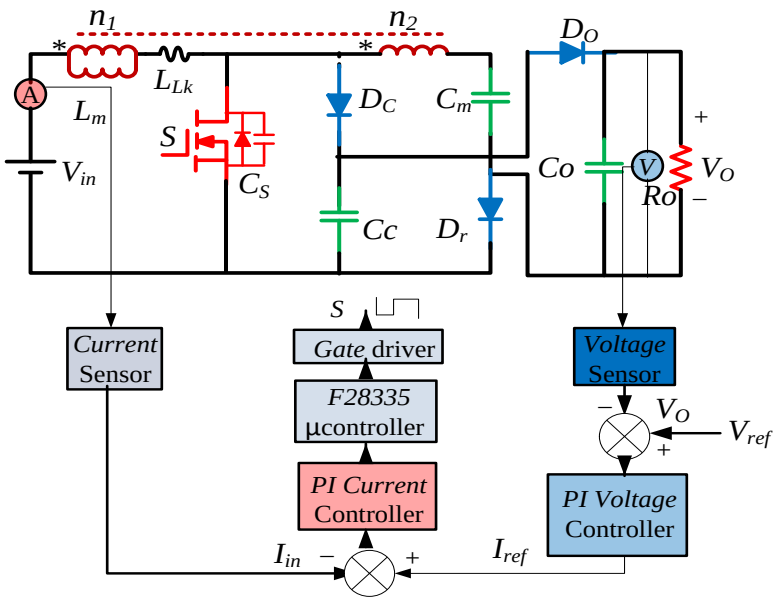

Figure 4.22 Control architecture

Figure 4.23 and Figure 4.24 demonstrates the closed loop transient and steady state performance of the converter. In Figure 4.23, a step change in load resistance is applied, causing a step decrement in output power from 250 W to 125 W and vice versa at fixed input voltage of 20 V. The results clearly show that the desired output voltage is well regulated, with zero steady state error. Likewise, at the point of a load change, there is no overshoot or undershoot in the output voltage waveform. The output current settles at the next steady-state value due to duty ratio adjustment to regulate the converter output voltage.

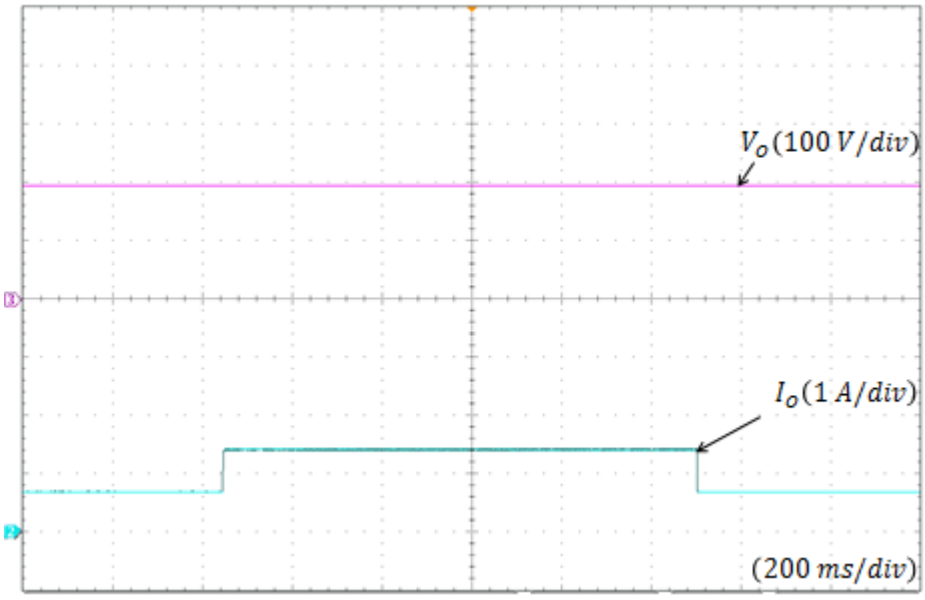

Figure 4.23 Step change in load from half load to full load and vice versa
output voltage (pink),output current (green)

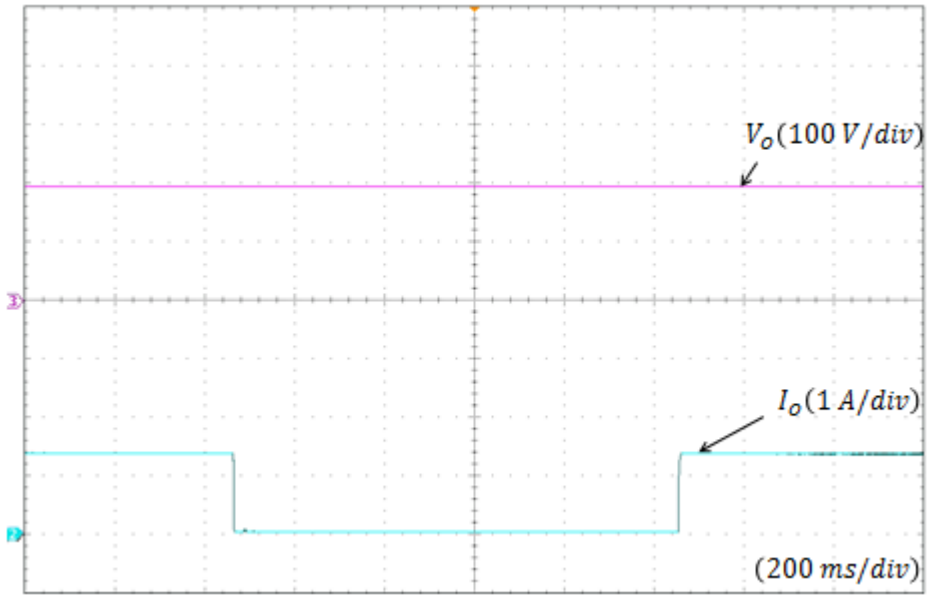

Figure 4.24 Load change from full load to no load and back to full load
output voltage (pink),output current (green)

Another change in load resistance is applied in Figure 4.24, causing a step decrement in output power from full load to no load and vice versa. Once more, the dynamic characteristics indicate that the output voltage stays constant, with zero steady state error.

4.9 Summary

Transformer and coupled inductor based DC-DC converters traditionally require a snubber to limit the the turn-off voltage spike seen by the primary switch due to leakage inductance. Literature shows that the active and passive clamp solutions are the most widely employed approach for recycling the transformer leakage energy in DC-DC converters. However, a true performance evaluation of the clamp circuits when applied to the same power converter is rarely discussed. This chapter presents the theoretical analysis and clamp schemes (active and passive) performance comparison applied to the proposed high step-up DC-DC converter. The experimental results, obtained via the two prototype circuits, validate both the theory and operational characteristics of each power converter. It is shown that the active clamp converter has the advantage of achieving (ZVS) of all the active switches and achieves 1% higher efficiency than its passive clamp counterpart. On the other hand, the passive clamp converter offers low cost, simple structure, low level of circulating current and higher reliability; thus increasing the lifetime of the converter. The operation of the passive clamp converter is almost similar to that of the active clamp counterpart, but with a single power switch.

Importantly, unlike many of power converters presented in the literature, both of the proposed topologies in this chapter exhibit low power switch voltage stress (one third of the converter output voltage approximately). Low device voltage stress allow high performance device with low on state resistance to reduce the conduction loss. The diodes voltage stress is significantly less than the converter output voltage and low-voltage diodes typically recover faster. The diodes turn off softly with (ZCS) by utilizing the inherent leakage inductance of the coupled inductor to control their current falling rate.

Chapter 5
Interleaved High Step-up Converter Analysis and Design

5.1 Introduction

The coupled inductor based converters have long been attractive in high step-up DC-DC converters because of their relative simplicity. The advantage or simplicity of utilising the coupled inductor to configure voltage gain extension cell can be explained in twofold. One is, the coupled inductor primary winding provide energy storage just like in conventional converters. Two is voltage transformation by adjusting the turns ratio of the coupled inductor, thus minimizing the magnetic component count. However, a drawback exist which include high peak and RMS current incurred by the switching components due to coupled inductor operation (see Figure 3.16 or Figure 4.15) and, in fact, a primary detriment of increasing the converter output power. In addition, the switching component suffered a high turn-off voltage spike (as a result of parasitic oscillation between the leakage inductor energy and parallel capacitor of the switch); if no means of recycling the leakage energy is adopted.

In order to increase the power density of a converter, it is desirable to reduce the power device current stress. In this regard, it is necessary to interleave multiple phases to share the input current and minimize the input source current ripple (AC component) that will decrease the efficiency lifetime of the converter. Interleaving is usually adopted as an effective solution in high power applications to share the input current, reduce the passive component size, increase the power level, minimize the current ripple, improve the transient response, and realize thermal distribution. The use of interleaving to minimize the current ripple is well documented [23, 45, 47, 83, 93, 98, 102, 123, 124]. Since the efficiency of the converter is the most desirable performance for many applications. Many energy recycling techniques with soft switching performance can be implemented in the power stage to improve the efficiency [23, 45, 47, 83, 93, 98, 102, 123]. These techniques are either active or passive in nature.

In this chapter, a new (ZVS) interleaved, non-isolated, high step-up boost converter with active clamping circuit is proposed. The converter uses two coupled inductors in both forward, and flyback mode and a switched capacitor to achieve high conversion ratio. Interleaving is adopted on the primary side to share the input current and cancel the current ripple of the coupled inductors and reduce the switch conduction losses. Importantly, a low turns ratio can be employed to achieve high conversion ratio which reduces the copper loss and leakage inductance of the coupled inductor. The secondary windings of the coupled inductor are connected in series to achieve winding coupled configuration and sustain the high voltage at the output. Furthermore, the voltage stress of the active switches and diodes are reduced. By using active clamping, (ZVS) is achieved for all the switches. The diode reverse recovery problem is alleviated for all the diodes; hence switching losses are further reduced.

5.2 Interleaved High Step-up Converter Overview

5.2.1 Circuit Topology Description

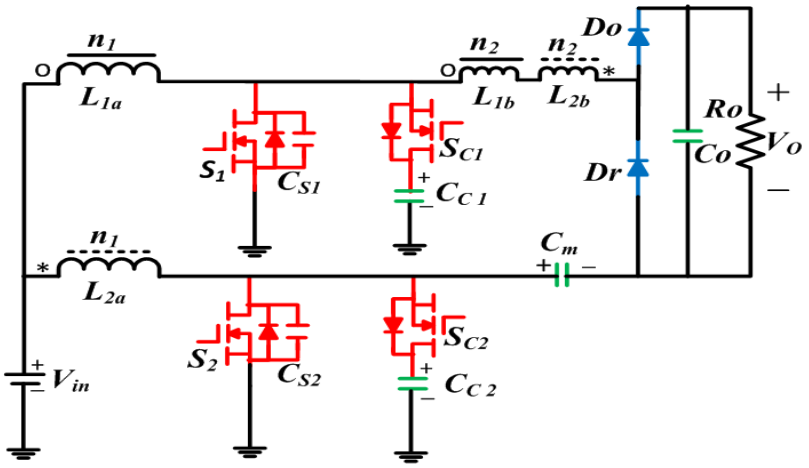

Figure 5.1 Circuit diagram of the interleaved non-isolated DC-DC boost converter

Figure 5.1 shows the structure of the proposed soft-switching high-step-up interleaved DC-DC boost converter with coupled inductors and voltage extension cell. The converter employs two coupled inductors ($L_1$and L_2) with the same number of turns in the primary and secondary sides. The primary winding of the coupled inductor L_{1a} and L_{2a} serve as filter inductors like in conventional interleaved boost converter and are coupled to their corresponding secondary windings L_{1b} and L_{2b}. The primary and secondary windings are denoted by n_1, n_2, and the coupling references denoted by ‘’o’’ and ‘’*’’. The primary windings are in parallel to handle the large input current on the low voltage side. The secondary windings are in series on the

high voltage side to achieve winding coupled configuration and enlarge the voltage gain. There are two sets of active clamp circuits, with S_{C1} and S_{C2} as the corresponding clamp switches. The voltage multiplier cell comprises of secondary windings of the coupled inductor L_{2a}, L_{2b}, the output and regenerative diodes D_O, D_r and the switched capacitor C_m.

Figure 5.2 shows the equivalent circuit of the proposed converter. The coupled inductors can be modelled as an ideal transformer with defined turns ratio. The primary winding is in parallel with the magnetizing inductor and then in series with leakage inductance [102, 125] . L_{m1}, L_{m2} are the magnetizing inductance of the coupled inductors. L_{Lk1}, L_{Lk2} represent the leakage inductances of the coupled inductors. S_1 , S_2 are the main switches, whereas S_{C1} , S_{C2} are the active clamp switches. C_{C1}, C_{C2} are the clamp capacitors. C_{S1}, C_{S2} represent the parasitic capacitance of the MOSFET and include the added parallel capacitors to implement (ZVS). C_O is the output capacitor whereas V_{in}, V_O represent the input and output voltages respectively.

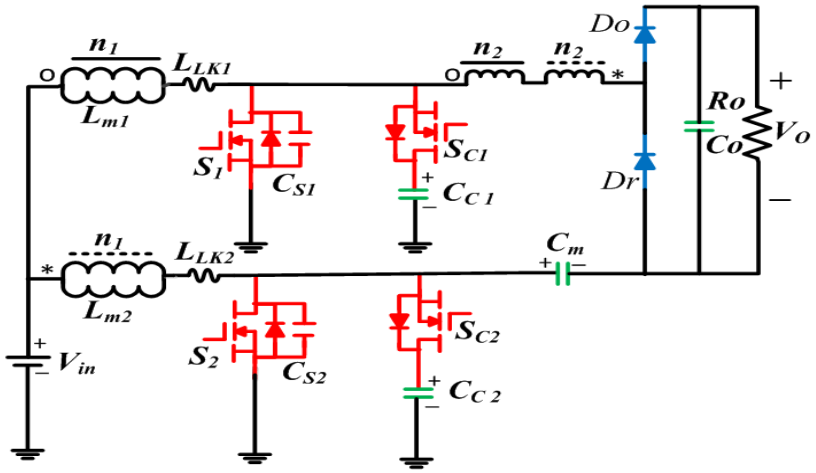

Figure 5.2 Equivalent circuit of the interleaved DC-DC boost converter

5.2.2 Circuit Operational Principle

The converter design is based on CCM operation, and this mode is guaranteed throughout the full range of duty cycle variation under purely resistive load. The duty cycle D of the main switches S_1 and S_2 are the same but phase shifted 180°. During steady state operation, the duty cycle is higher than 0.5. The gate signals of the clamp switch S_{C1} and S_{C2} are complementary to their corresponding main switches S_1 and S_2. Some steady state current and voltage waveforms of the converter are shown in Figure 5.3. There are sixteen modes of operation in one switching cycle. The topological states corresponding to each mode of

operation and current flow paths are shown in Figure 5.4. In order to simplify the analysis, the leakage inductances L_{Lk1} and L_{Lk2} were reflected from primary to the secondary side as equivalent leakage inductance and denoted by L_k. N is defined as the turn's ratio of the coupled inductor (n_2/n_1).

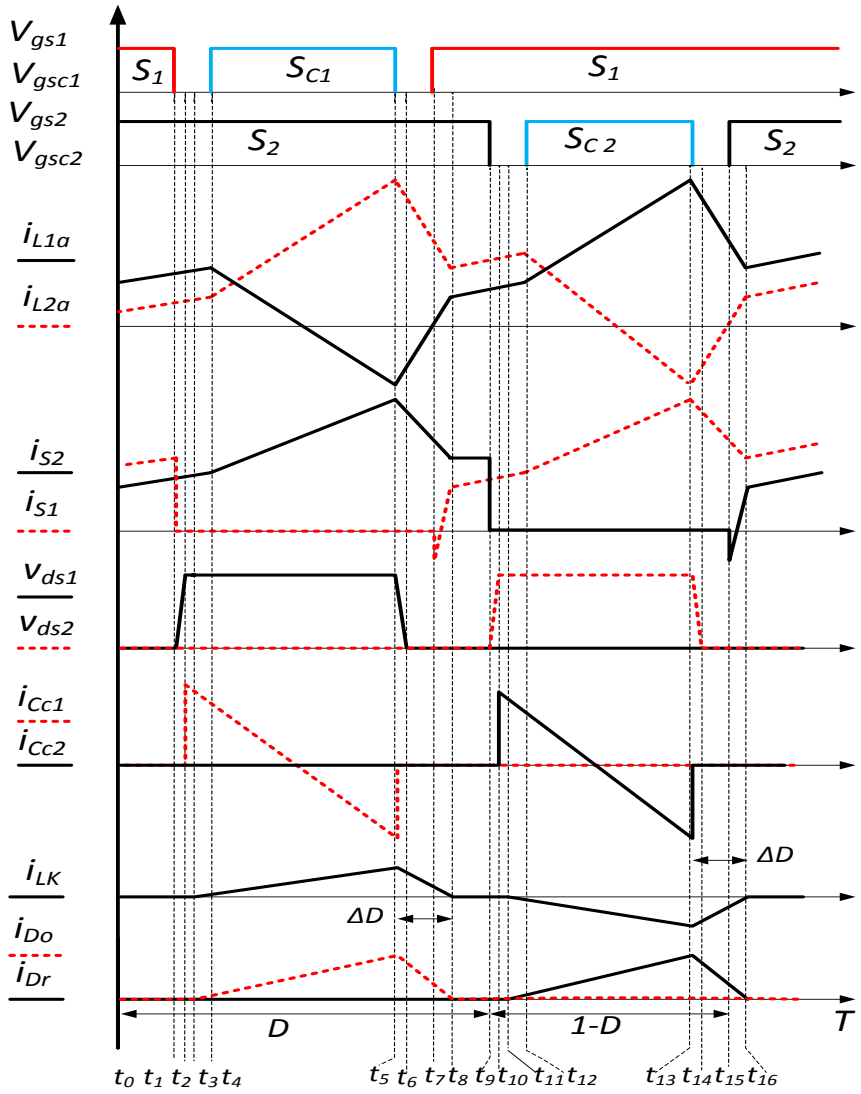

Figure 5.3 key steady state waveforms

Mode 1 $[t_0 - t_1]$ (Figure 5.4a): Before time t_1, the main switches S_1 and S_2 are on, the clamp switches S_{C1} and S_{C2} are off. The output and regenerative diodes D_O, D_r are reversed biased. Magnetizing inductances L_{m1} and L_{m2} are charged linearly by the input voltage. The load is supplied by the energy in the output capacitor. Magnetizing inductor currents are given by

$$i_{Lm1}(t) = I_{Lm1}(t_0) = \frac{V_{in}}{L_{m1}}(t - t_0) \tag{5.1}$$

$$i_{Lm2}(t) = I_{Lm2}(t_0) + \frac{V_{in}}{L_{m2}}(t - t_0) \tag{5.2}$$

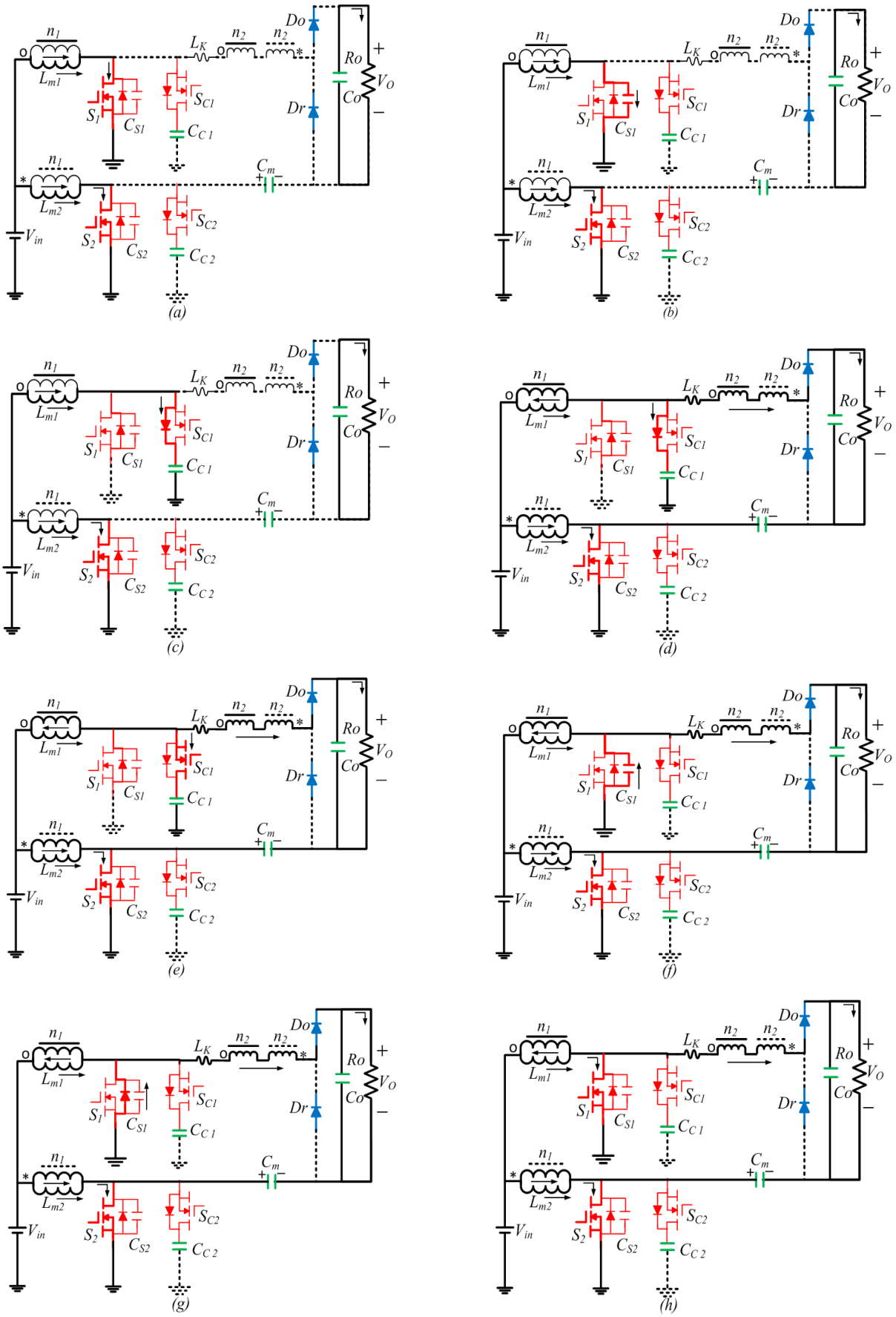

Figure 5.4 Topological states of the interleaved DC-DC boost converter
(a) Mode 1[t_0 - t_1], (b) Mode 2 [t_1 – t_2], (c) Mode 3 [t_2 – t_3], (d) Mode 4 [t_3 – t_4], (e) Mode 5 [t_4 – t_5], (f) Mode 6 [t_5 – t_6], (g) Mode 7 [t_6 – t_7], (h) Mode 7 [t_7 – t_8],

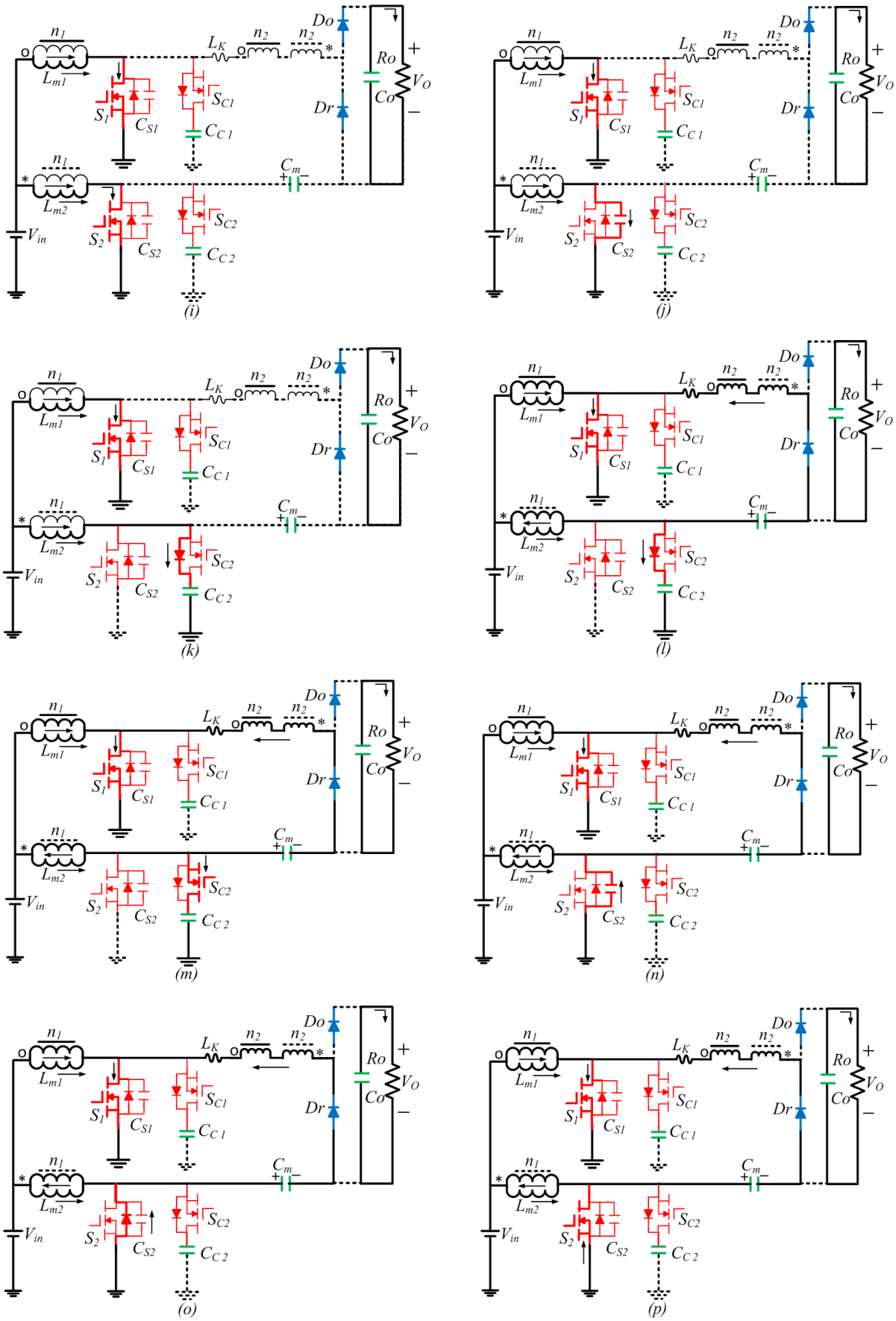

Figure 5.4 (Continued) Topological states of the interleaved DC-DC boost converter
(i) Mode 8[$t_8 - t_9$], (j) Mode 9 [$t_9 - t_{10}$], (k) Mode 10 [$t_{10} - t_{11}$], (l) Mode 11 [$t_{11} - t_{12}$],
(m) Mode 12 [$t_{12} - t_{13}$], (n) Mode 13 [$t_{13} - t_{14}$], (o) Mode 14 [$t_{14} - t_{15}$], (p) Mode 15 [$t_{15} - t_6$].

Mode 2 $[t_1 - t_2]$ (Figure 5.4b): The main switch S_1 turns off at time t_1, the drain-source voltage increases linearly, due to parallel capacitor C_{S1}, the switch S_1 turns off with (ZVS). The magnetizing inductor current is high and requires very short time to charge the capacitor C_{S1}. The equivalent leakage inductance current I_{Lk} rises linearly. v_{ds1} can be expressed as

$$v_{ds1}(t) \approx \frac{I_{Lm1}(t_1)}{C_{S1}}(t - t_1) \tag{5.3}$$

Mode 3 $[t_2 - t_3]$ (Figure 5.4c): At time t_2, the drain-source voltage of main switch S_1 reaches the clamp capacitor voltage V_{Cc1}, and the drain-source voltage of the clamping switch S_{C1} reduces to zero which causes the antiparallel diode to conduct. The magnetizing inductor current is commutated to the antiparallel diode, and current begins to flow through the clamping capacitor C_{C1} since it is much larger than C_{S1}. The voltage of the main switch S_1 is clamped to the voltage of clamp capacitor C_{C1}. During this time, v_{ds1} is given by

$$v_{ds1}(t) \approx V_{ds1}(t_2) + \frac{I_{Lm1}(t_2)}{C_{C1}}(t - t_2) \tag{5.4}$$

Mode 4 $[t_3 - t_4]$ (Figure 5.4d): The output diode D_O start conducting at t_3, the energy is transferred to the load. Consequently the coupled inductor L_1, act as a filter inductor and L_2 act as a transformer. The secondary windings of the coupled inductors and the switched capacitor C_m serve as voltage sources to enlarge the voltage gain. The rate of change of current through the output diode is controlled by the equivalent leakage inductance L_K. The input voltage still charges the magnetizing inductor L_{m2} linearly. During this stage

$$i_{Lm1}(t) = I_{Lm1}(t_3) - \frac{\left[\left(V_O - V_{Cm}(t_3)\right)\right]/N - V_{in}}{L_{m1}}(t - t_3) \tag{5.5}$$

$$i_{Lk}(t) = i_{Cm}(t) = \frac{[N+1]V_{Cc1} + V_{Cm} - V_O}{L_K}(t - t_3) \tag{5.6}$$

Mode 5 $[t_4 - t_5]$ (Figure 5.4e): The gate signal of S_{C1} can be applied at t_4 to implement the (ZVS) turn-on condition since its antiparallel diode is conducting. The magnetizing inductor current i_{Lm1} continues to charge the clamping capacitor C_{C1}.

Mode 6 $[t_5 - t_6]$ (Figure 5.4f): At time t_5, the clamp switch S_{C1} turns off, and the clamp circuit is therefore disconnected. The drain-source voltage of switch S_1 decreases and that of the clamp switch S_{C1} increases from zero at the same rate. Therefore, the turn of loss of the clamp switch is reduced due to parallel capacitor and S_{C1} turns off with (ZVS) condition. The equivalent leakage inductor current i_{Lk} reaches its peak and starts to decrease linearly at the end of this mode.

Mode 7 $[t_6 - t_7]$ (Figure 5.4g): At time t_6, the voltage of C_{s1} reduces to zero, and its antiparallel diode begins to conduct. The output diode current decreases linearly, and the current falling rate is controlled by the leakage inductance L_{LK1}. i_{Lk} during this stage is expressed as

$$i_{Lk}(t) = I_{LK}(t_6) = \frac{V_O - V_{Cm}(t_6)}{L_K}(t - t_6) \tag{5.7}$$

Mode 8 $[t_7 - t_8]$ (Figure 5.4h): The gate signal of main switch S_1 can be applied at this instant since its antiparallel diode is conducting to implement (ZVS) turn-on condition. Output diode D_O is still conducting, at the end of this mode, D_O turns off softly with zero-current-switching (ZCS) and the equivalent leakage inductance current i_{Lk} reaches zero.

Mode 9 $[t_8 - t_9]$ (Figure 5.4i): Before t_9, main switches S_1 and S_2 are conducting, the clamp switches S_{C1} and S_{C2} are off. The regenerative and output diode D_r, D_O are reverse biased. Magnetizing inductors L_{m1} and L_{m2} are charged linearly by the input voltage V_{in}. The output capacitor supplies the load. The equivalent circuit of this mode is the same with that of Figure 5.4(a).

Mode 10 $[t_9 - t_{10}]$ (Figure 5.4j): The main switch S_2 turns off at t_9. The parallel capacitor C_{S2} is then charged by the magnetizing current of i_{Lm2}. Due to parallel capacitor C_{S2}, the turn off losses is reduced and the main switch S_2 turns off with (ZVS) condition.

Mode 11 $[t_{10} - t_{11}]$ (Figure 5.4k): At time t_{10}, the drain-source voltage of the main switch S_2 reaches the clamp capacitor voltage V_{Cc2}, and forces the antiparallel diode of S_{C2} to conduct. The current through the main switch S_2 is commutated to the antiparallel diode of clamp switch S_{C2}. The drain-source voltage S_2 is clamped to the clamp capacitor voltage V_{Cc2}. The voltage across the equivalent leakage inductance is derived as

$$V_{Lk} = V_{Cm} - (N + 1)V_{Cc2} \tag{5.8}$$

Mode 12 $[t_{11} - t_{12}]$ (Figure 5.4l): At time t_{11} the regenerative diode D_r begins to conduct. Consequently, the coupled inductor L_1 works as a filter inductor and L_2 works as a transformer. Thus, the switched capacitor C_m is charged by the input voltage source. The magnetizing inductor L_{m1} is still charged by the input voltage.

Mode 13 $[t_{12} - t_{13}]$ (Figure 5.4m): The turn on gate signal to S_{C2} is applied at t_{12} to implement (ZVS) turn on condition of S_{C2} whilst the antiparallel diode is conducting.

Mode 14 $[t_{13} - t_{14}]$ (Figure 5.4n): The clamp switch S_{C2} turns off at t_{13}. The active clamp circuit is disconnected. Due to the parallel capacitor C_{S2}, the clamp switch S_{C2} turns off under (ZVS) condition.

Mode 15 $[t_{14} - t_{15}]$ (Figure 5.4o): At t_{14}, the parallel capacitor of main switch S_2 is discharged by the coupled inductor primary current and reflected leakage inductor current. Therefore, its antiparallel diode starts conducting.

Mode 16 $[t_{15} - t_{16}]$ (Figure 5.4p): The turn on gate signal of S_2 is applied at t_{15}, to implement (ZVS) condition whilst its antiparallel diode is conducting. At the end of this mode, the equivalent leakage inductor current decreases to zero and the regenerative diode turns off with (ZCS) condition. A new switching cycle then ensues in a similar fashion.

5.3 Interleaved Converter Steady State Analysis

5.3.1 Static Gain

Under ideal conditions, the coupled inductors are assumed to be well coupled, and the leakage inductance is considered to be zero. The power switches are lossless with zero conduction voltage drops; the MOSFETS parallel capacitors are ignored. The voltages across all capacitors are assumed to be constant. Applying inductor volt-second balance principle to coupled inductor L_{1a} and L_{2a} the voltage across the clamp capacitors V_{Cc1} and V_{Cc2} becomes

$$V_{Cc1} = V_{Cc2} = V_{Cc} = \frac{V_{in}}{(1-D)} \tag{5.9}$$

When the main switch S_1 turns off, the other main switch S_2 is on, the energy is delivered to the load, and the output voltage can be expressed as

$$V_O = V_{Cc1} + NV_{in} + N1(V_{Cc} - V_{in}) + V_{Cm} \tag{5.10}$$

Applying inductor volt-second balance equation to the equivalent leakage inductance during modes [2-8], the voltage across the switched capacitor is derived as

$$V_{Cm} = \frac{V_O}{2} \tag{5.11}$$

From (5.9) - (5.11) the ideal voltage gain is given by

$$M_{ideal} = \frac{V_O}{V_{in}} = \frac{2N+2}{(1-D)} \tag{5.12}$$

From (5.12), it is evident that a high conversion ratio can be obtained without extreme duty

ratio operation. Two degrees of freedom exist to enlarge the voltage gain (duty ratio and coupled inductor turns ratio). These features make the converter suitable for high step-up applications. The curve relating the voltage gain with the coupled inductor turns ratio as a function of the duty cycle is sketched in Figure 5.5. When the duty cycle is 0.6, corresponding to turns ratio N of 1 the voltage gain is exactly ten times (10X).

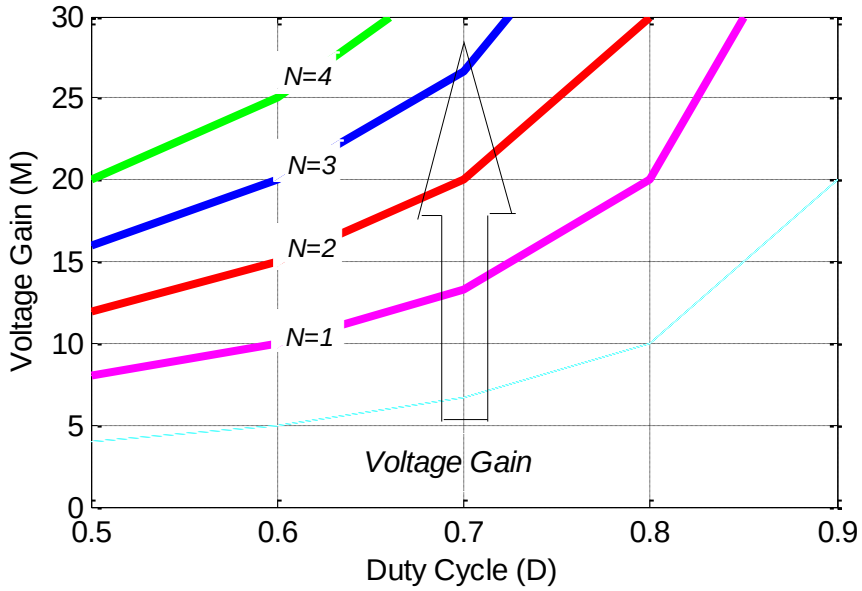

Figure 5.5 Voltage gain characteristic of the converter for various D and N values

However, the inherent leakage inductance of the coupled inductors is responsible for achieving the (ZVS) of both main and clamp switches and control the current falling rate of the regenerative and output diodes. The leakage inductance should not be ignored, once it is considered the non-ideal voltage gain can be derived.

In Figure 5.3 a parameter ΔD is defined as the time interval $(t_5 - t_8)$ which represent the time it takes the equivalent leakage inductor current to fall from its peak value to zero. Using this parameter and applying the inductor volt-second balance equation to the equivalent leakage inductor L_K, during the interval $(t_3 - t_8)$ gives

$$\frac{V_{Cm}}{V_{Cc}} = \frac{(1-D)(N+1)}{(1-D+\Delta D)} \tag{5.13}$$

From (5.9), (5.11) and (5.13) the voltage gain is derived as in (5.14).

$$M = \frac{V_O}{V_{in}} = \frac{2N+2}{(1-D+\Delta D)} \tag{5.14}$$

In Figure 5.3, the peak value of the regenerative and output diode currents can be derived from the slope of the equivalent leakage inductor current waveform as

$$I_{Do\_pK} = I_{Dr\_pK} = \frac{[N+1]V_{Cc} + V_{Cm} - V_O}{L_K}(1-D)T_s \tag{5.15}$$

Where T_s is the switching period. The average output current is the same with the average diode currents. Therefore, the peak diode current can be denoted by

$$I_{Do\_pK} = I_{Dr\_pK} = \frac{2I_O}{(1-D+\Delta D)} \tag{5.16}$$

Now equating (5.15) and (5.16) gives

$$\frac{[N+1]V_{Cc} + V_{Cm} - V_O}{L_K}(1-D)T_s = \frac{2I_O}{(1-D+\Delta D)} \tag{5.17}$$

Making appropriate substitution using equations (5.9), (5.11), (5.13) and (5.17), the duty cycle loss (ΔD) is derived as

$$\Delta D = \frac{4I_O L_{LK} f_S}{2(N+1)V_{in} - V_O(1-D)} - (1-D) \tag{5.18}$$

Substituting (5.18), into (5.14) gives (5.20) as follows:

$$\left(\frac{4\,(N+1)}{M} - (1-D)\right)^2 = (1-D)^2 + \frac{16 \cdot f_s \cdot L_K}{R_O} \tag{5.19}$$

Making M the subject of equation (5.19) gives the voltage gain equation of the converter.

$$M = \frac{V_O}{V_{in}} = \frac{4(N+1)}{(1-D) + \sqrt{(1-D)^2 + Q}} \tag{5.20}$$

Where $Q = (16 \cdot f_s \cdot L_k)/R_O$. Q denotes the equivalent leakage inductance, the load resistance R_O and switching frequency. If the leakage inductance is zero in equation (5.20), it becomes the same as equation (5.12). The relationship between several Q and N value as a function of duty ratio D from (5.20) is sketched in Figure 5.6.

In practice, the conversion efficiency is also affected by the conduction losses caused by the parasitic elements of the converter, unlike the ideal characteristics. In order to evaluate the effect of the parasitic elements (coupled inductor winding resistance, on-state resistors of MOSFET and diode forward voltage drop), the leakage inductance of the coupled inductors is considered as zero to simplify the analysis. Therefore, the clamp circuits can be removed. The equivalent series resistor (ESR) of capacitors is also neglected; the voltage gain is derived as

$$M = \frac{V_o}{V_{in}} = \frac{\frac{2(N+1)}{(1-D)} - \frac{2V_d}{V_{in}}}{(1+A+B)} \tag{5.21}$$

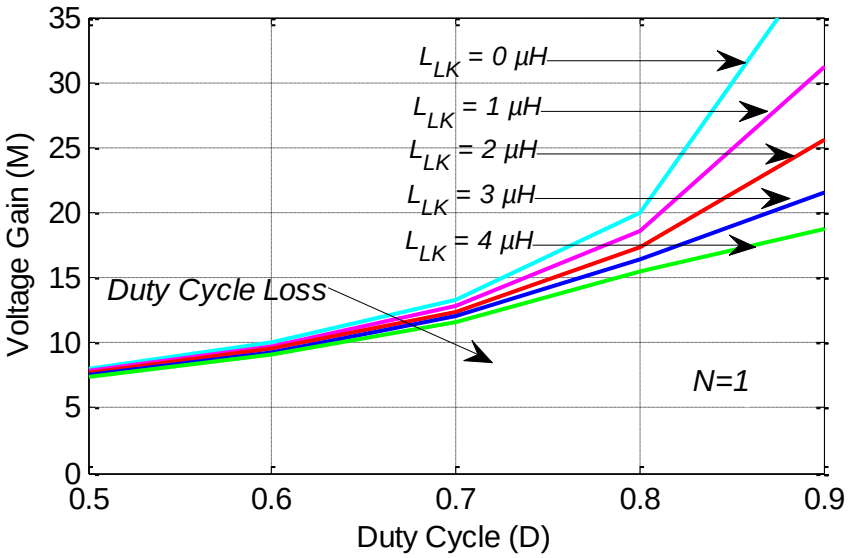

Figure 5.6 Voltage gain characteristic of the converter

Where $A = \frac{2(N+1)^2}{(1-D)R_o}\ (R_1 + 2R_{ds} + 2R_2 + R_D)$, $B = -\frac{2(N+1)^2}{(1-D)^2R_o}(R_{ds} + DR_1)$ and V_d, R_d is the diode forward voltage drop and diode parasitic resistance respectively. R_1, R_2 denotes the winding resistance of the primary and secondary windings. R_{ds} is the one state resistance of the power MOSFET.

5.3.2 Power Semiconductors Voltage Stress

The voltage stress of the main and clamp switches of the converter are the same and is derived from (5.9) by neglecting the voltage ripple on the clamp capacitors. The voltage stress related to the output voltage is given by

$$V_{ds1} = V_{ds2} = V_{dsc1} = V_{dsc2} = \frac{V_O}{2(N+1)} \tag{5.22}$$

The voltage stress of the diodes is equal to the output voltage and expressed as

$$V_{Do} = V_{Dr} = V_O \tag{5.23}$$

5.3.3 Current Stress Analysis

The average current through each diode is equal to the average output current. The conduction period of each diode equal to $(1-D)T_s$. Hence, the average current of the diodes D_r and D_O is the same given by

$$I_{Dr\_avg} = I_{Do\_avg} = \frac{I_O}{(1-D)} \tag{5.24}$$

By considering conversion efficiency to be unity, the relationship between the input and output currents is

$$I_{in} = \frac{2(N+1)I_O}{(1-D)} \tag{5.25}$$

Due to interleaving, each of the magnetizing inductors L_{m1} and L_{m2} share half of the input current. Therefore, the magnetizing inductor current is

$$I_{Lm1} = I_{Lm2} = \frac{I_{in}}{2} = \frac{(N+1)I_O}{(1-D)} \tag{5.26}$$

The peak switch current is equal to the sum of the magnetizing current and reflected output diode current is given by

$$I_{S1} = I_{S2} = I_{Lm} + NI_{Do} = \frac{(2N+1)I_O}{(1-D)} \tag{5.27}$$

The clamp switch current is the magnetizing inductor current given in (5.26). It is worth noting from (5.26) and (5.27) that the current stress of the switches increases as the coupled inductor turns ratio increase. From (5.26) and (5.27), the RMS current of the main and clamp switches becomes

$$I_{RMS-S} = \sqrt{\frac{\int_0^{T_s} {i_{S1}}^2(t)dt}{T_S}} = \frac{(N+1)I_O}{(1-D)}\sqrt{\frac{10-7D}{3}} \tag{5.28}$$

$$I_{RMS-SC} = \sqrt{\frac{\int_0^{(1-D)T_s} {i_{Sc}}^2(t)dt}{T_S}} = \frac{(N+1)I_O}{\sqrt{3(1-D)}} \tag{5.29}$$

5.3.4 (ZVS) Soft Switching performance

The (ZVS) turn-on and turn-off is due to the existence of the clamp circuit and parallel capacitors C_{s1} and C_{s2}. To ensure (ZVS) of the main switch, the drain-source voltage of S_1 should be decreased to zero before it turn-on gate signal is applied. The parallel capacitor C_{S1} is discharged by coupled inductor primary current I_{L1a} before the turn on gate signal is applied (see Figure 5.4f). To ensure (ZVS) of the main switch at time t_7, equation (5.30) should be satisfied

$$L_{Lk1}I_{L1a}^2(t_7) \geq \frac{C_{S1}V_{Cc}^2}{2N^2} \tag{5.30}$$

The coupled inductor primary current I_{L1a} is the difference between the equivalent leakage inductor current and magnetizing inductor current, which is derived as

$$I_{L1a}(t) = I_{LK}(t) - I_{Lm1}(t) \tag{5.31}$$

The peak value of the equivalent leakage inductor current is derived in (5.6). And the magnetizing inductor current at time (t_7) is given by

$$I_{Lm1}(t_7) = \frac{P_o}{2\,V_{in}} - \frac{V_{in}D}{2L_{m1}f_s} \tag{5.32}$$

From (5.6), (5.31) and (5.32), the coupled inductor primary current is obtained as

$$I_{L1a} = \frac{V_{in}^2\big(L_kD + 2L_{m1}(N+1)\big) - V_{in}V_OL_{m1}(1-D) - P_o\,L_{m1}\,L_k\,f_s}{2\,V_{in}\,L_{m1}\,L_kf_s} \tag{5.33}$$

5.4 Design Procedure

5.4.1 Coupled Inductor Turns Ratio Design

The coupled inductor turns ratio design has a significant impact on the converter performance, such as the device voltage and current stress as demonstrated in section 5.3. Proper turns ratio selection allows low voltage rated devices to be used and avoid extreme duty cycle operation over the input line range. Once the duty cycle is chosen, the coupled inductor turns ratio can be determined from (5.34)

$$N = \frac{n_2}{n_1} = \frac{1}{2}\left[\frac{V_O}{V_{in}}(1-D) - 2\right] \tag{5.34}$$

5.4.2 Leakage Inductance Design

The leakage inductance serves a dual purpose of achieving (ZVS) characteristic over a wide operating range as well as limiting the current falling rate of the diodes. Achieving (ZVS) require inherent leakage inductance L_{Lk} of sufficient size to discharge the parallel capacitor of the switch before the main switch turns on. In high voltage gain DC-DC converters; it is desirable to turn off the output diodes softly to reduce switching loss. Therefore, the leakage inductance design is a trade-off between (ZVS) of the active device and (ZCS) turn off characteristic of the diodes. From (5.20) the voltage gain equation can be re-written as

$$M = \frac{V_O}{V_{in}} = (N+1)\frac{\sqrt{R_0(1-D)^2 + 16R_0L_kf_S} - R_0(1-D)}{4L_kf_S} \tag{5.35}$$

Making the equivalent leakage inductance L_K the subject of (5.35) gives

$$L_k = \frac{2R_0(N+1)^2 - MR_0(N+1)(1-D)}{2M^2 f_s} \tag{5.36}$$

Assuming that all the coupled inductors have the same leakage inductance, and reflecting it to the primary side gives

$$L_{Lk1} = L_{Lk2} = \frac{L_k}{2N^2} \tag{5.37}$$

5.4.3 Magnetizing Inductor Design

A usual criterion for designing the magnetizing inductance is to maintain the continuous inductor current mode and allow an acceptable current ripple (expressed as a percentage of the maximum average magnetizing inductor current). The ripple current magnitude has an influence on the peak and RMS current of the switch. But, the presence of the clamp circuit does not alter the switch current significantly. The magnetizing inductor can be designed from (5.38)

$$L_{m1} = L_{m2} = \frac{V_{in}D}{\Delta I_{Lm} f_s} \tag{5.38}$$

Where ΔI_{Lm} is the magnetizing inductor current ripple.

5.4.4 Clamp Capacitor Design

The primary function of the clamp capacitor is to suppress the voltage spikes of the main switch caused by the leakage energy of the coupled inductor and avoid excessive resonant ringing. The simplified clamp capacitor current waveform during the main switch turn-off period is shown in Figure 5.7 assuming that the clamp capacitor current is piecewise linear.

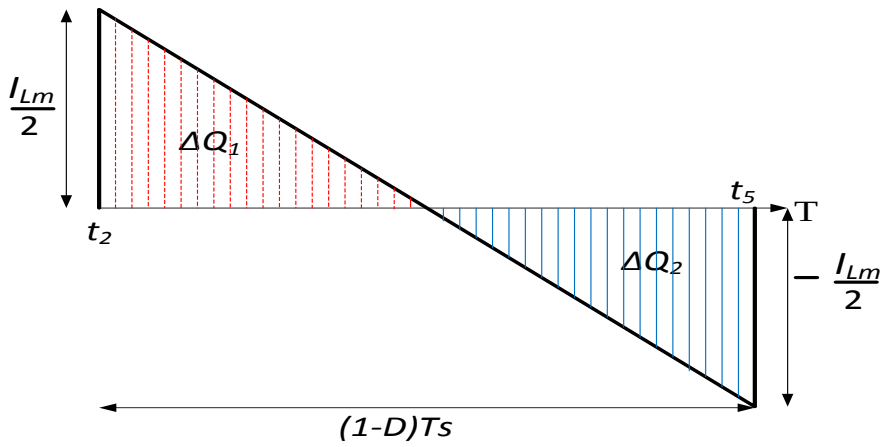

Figure 5.7 Clamp capacitor current waveform

The clamp capacitor needs to maintain a balance between charge and discharge. By considering the charge area ΔQ_1 equal to the discharge area ΔQ_2, the following relationship is obtained.

$$\Delta V_{CC} = \frac{\Delta Q}{C_C} = \frac{1}{C_C} \cdot \frac{1}{2} \cdot \frac{(N+1)I_O}{2(1-D)} \cdot (1-D)T_S \tag{5.39}$$

Where ΔQ represent the charge stored in the capacitor and ΔV_{Cc} is the voltage ripple of the clamp capacitor. From (5.39) the clamp capacitor can be selected as

$$C_C = \frac{(N+1)I_O}{4\Delta V_{Cc} f_s} \tag{5.40}$$

5.4.5 Switched Capacitor Design

Figure 5.8 shows the simplified current and voltage waveform of the switched capacitor. The switched capacitor serve as a voltage source in the converter and the ripple voltage on the capacitor should be limited to reasonable value during selection. Considering the voltage waveform shown in Figure 5.8, the shaded area Q represents charge stored in the switched capacitor C_m in one switching cycle.

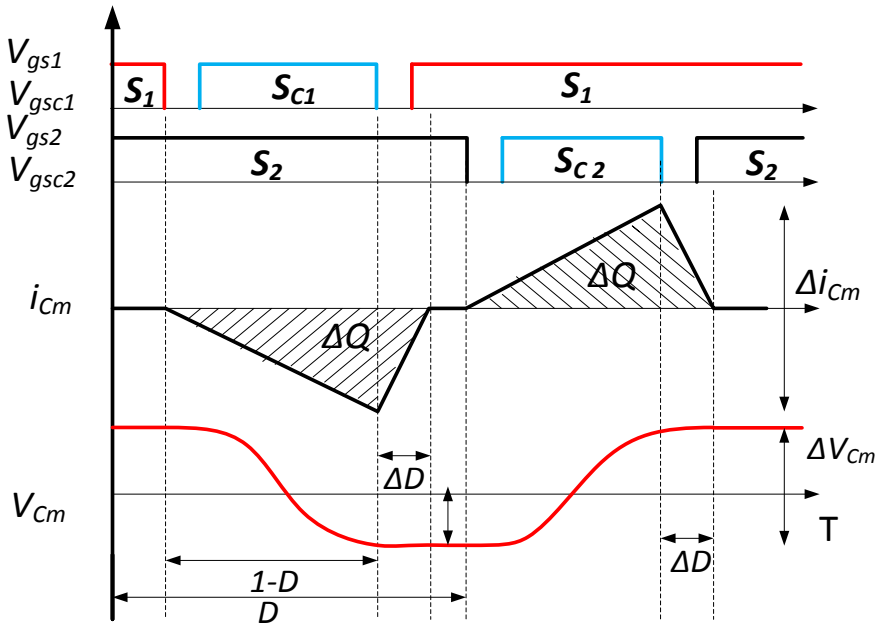

Figure 5.8 Simplified voltage and current waveform of switched capacitor

The peak-to-peak voltage ripple of switched capacitor Δv_{Cm} is obtained by considering the area charged by the switched capacitor C_m, which is given by

$$\Delta V_{Cm} = \frac{\Delta Q}{C_m} = \frac{1}{C_m} \cdot \frac{1}{2} \cdot \frac{\Delta I_{CM}}{2} \cdot (1 - D + \Delta D) T_S \tag{5.41}$$

The ripple magnitude of the switched capacitor current is given by

$$\Delta I_{CM} = \frac{4 I_O}{(1 - D + \Delta D)} \tag{5.42}$$

Substituting (5.42) into (5.41), the switched capacitor value can be obtained

$$C_m = \frac{I_O}{\Delta V_{Cm} f_s} \tag{5.43}$$

5.4.6 Output Capacitor Design

For a CCM operation, it is assumed that all the ripple components of the diode current I_{DO} follow through the capacitor and the average value (DC components) follows through the load resistor. Therefore, the average diode current is expressed as

$$I_{Do\_avg} = \frac{I_O}{(1 - D)} \tag{5.44}$$

From KCL the average output diode current can be denoted by

$$I_{Do} = C_O \frac{dv_o}{dt} - I_O \tag{5.45}$$

Making the C_O the subject of (5.45) and performing appropriate substitution yields

$$C_O = \frac{I_O D}{dv_o (1 - D)} dt \tag{5.46}$$

From steady state analysis in section 5.3, dt is defined as the time interval in which the output current flow through the load denoted as $(1 - D)T_s$ and dv_o is the peak-peak ripple voltage of the output capacitor. From the above relation, the output capacitor value can be selected from (5.47)

$$C_O = \frac{I_O D}{\Delta v_o f_s} \tag{5.47}$$

5.4.7 Dead Time design

Dead time between the turn-off of the main switch and the turn-on of the corresponding clamp switch is to accomplish (ZVS) turn-on condition of the clamp switch. The gate signal of the

clamp switch can be applied whilst its antiparallel diode is conducting. The time delay is

$$\Delta t_{S1\_off\ SC1\_On} = \frac{V_{Cc1} C_{S1}}{I_{Lm1}} \tag{5.48}$$

Likewise the approximate dead time between the turn off of the clamp switch and turn on of the corresponding main switch is to ensure (ZVS) turn-on condition of the main switch. The best criterion is to allow for a one-quarter of the resonant time between the leakage inductance and the parallel capacitor [16]. This is expressed as

$$\Delta t_{SC1\_off\ S1\_On} = \frac{\pi}{2}\sqrt{L_{Lk1} C_{S1}} \tag{5.49}$$

The main advantage of the dead time design is to prevent an overlap of the main and clamp switch gate signals. Any accidental overlap could lead to short circuit and failure of the circuit

5.5 Simulation

To verify the theoretical analysis, a 0.5 kW converter has been designed and simulated in Matlab-Simulink environment. Detail description of Simulink model is given in Appendix A. The simulation parameters are selected based on section 5.4. The specifications of the converter and the selected components are listed in Table 5.1. The simulation parameters including their parasitic values are the same with that of the experimental prototype.

Table 5.1 Converter Parameters

Output Power (P_O)	500 W
Input Voltage (V_{in})	12-14 V
Output Voltage (V_O)	120 V
Switching Frequency (f_s)	50 KHz
Main Switches (S_1 and S_2)	FDP047AN
Clamp Switches (S_{C1} and S_{C2})	FDP047AN
Output & Regenerative Diodes (D_O and D_r)	MBUR42050G
Clamp capacitors (C_{C1} and C_{C2})	10 µF
Switched Capacitor (C_m)	10 µF
Output capacitor (C_O)	22 µF
Turns Ratio (n_2/n_1)	13:13
Magnetizing Inductance (L_{m1} and L_{m2})	34.5 µH
Leakage Inductance (L_{Lk1} and L_{Lk2})	1.6 µH

Figure 5.9 illustrates the simulation results obtained under full load condition with 12 V input voltage. The input current I_{in}, and the current through the primary inductor I_{L1a} and I_{L1b} are shown in Figure 5.9(a). Although, the current ripple of each coupled inductor is relatively large. The input current ripple is very small as a result of current ripple cancelation caused by the interleaving operation. The (ZVS) soft switching performances of the active switch S_1 and S_{C1} are shown in Figure 5.9(b) and Figure 5.9(c) respectively. (ZVS) soft switching performance is achieved for both the main and clamp switches, which reduces the switching loss significantly. The (ZVS) of main switch S_2 and clamp switch S_{C2} is the same with S_1 and S_{C1} and therefore not repeated. The voltage stress of the power devices is 38 V, which is lower than the converter output voltage. In essence, low rated devices with low on-state resistance can be employed to reduce the conduction losses.

The active clamp circuit behaviour is illustrated with the aid of Figure 5.9(d). When the main switch turns off, the magnetizing inductor current is commutated to the antiparallel diode of the clamp switch and the leakage inductance energy is subsequently released to the clamp capacitor. The clamp capacitor currents I_{Cc1} and I_{Cc2} illustrate the flow of current through the corresponding clamp circuit when either of the main switch turns off.

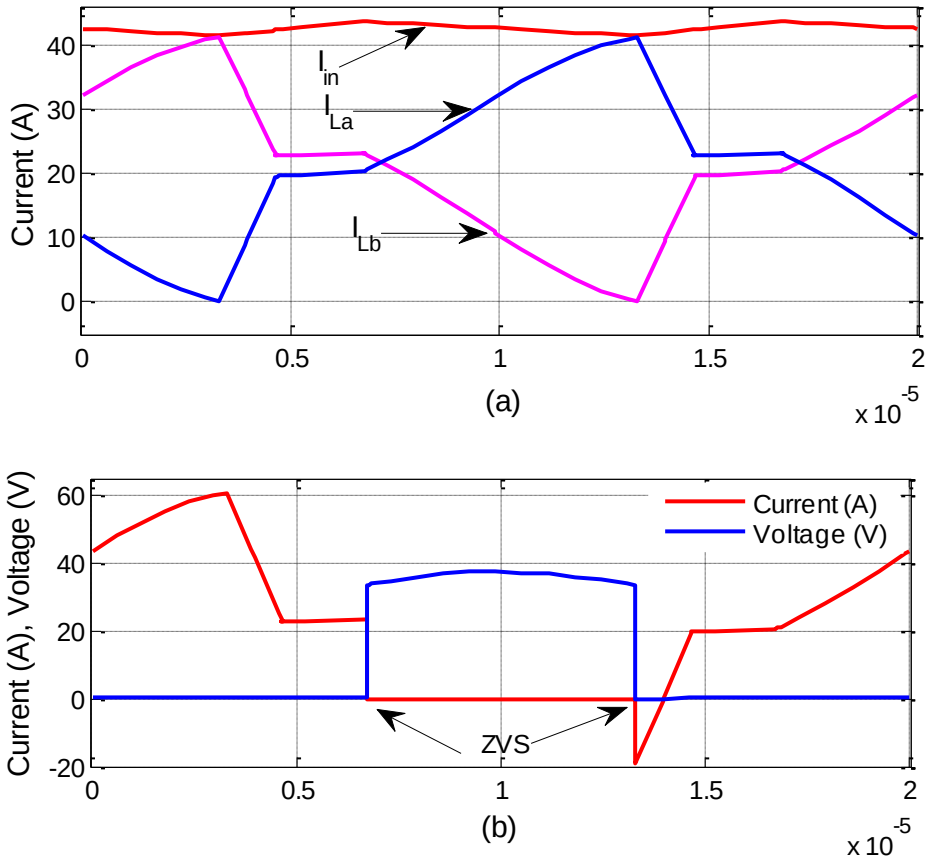

Figure 5.9 Simulation results

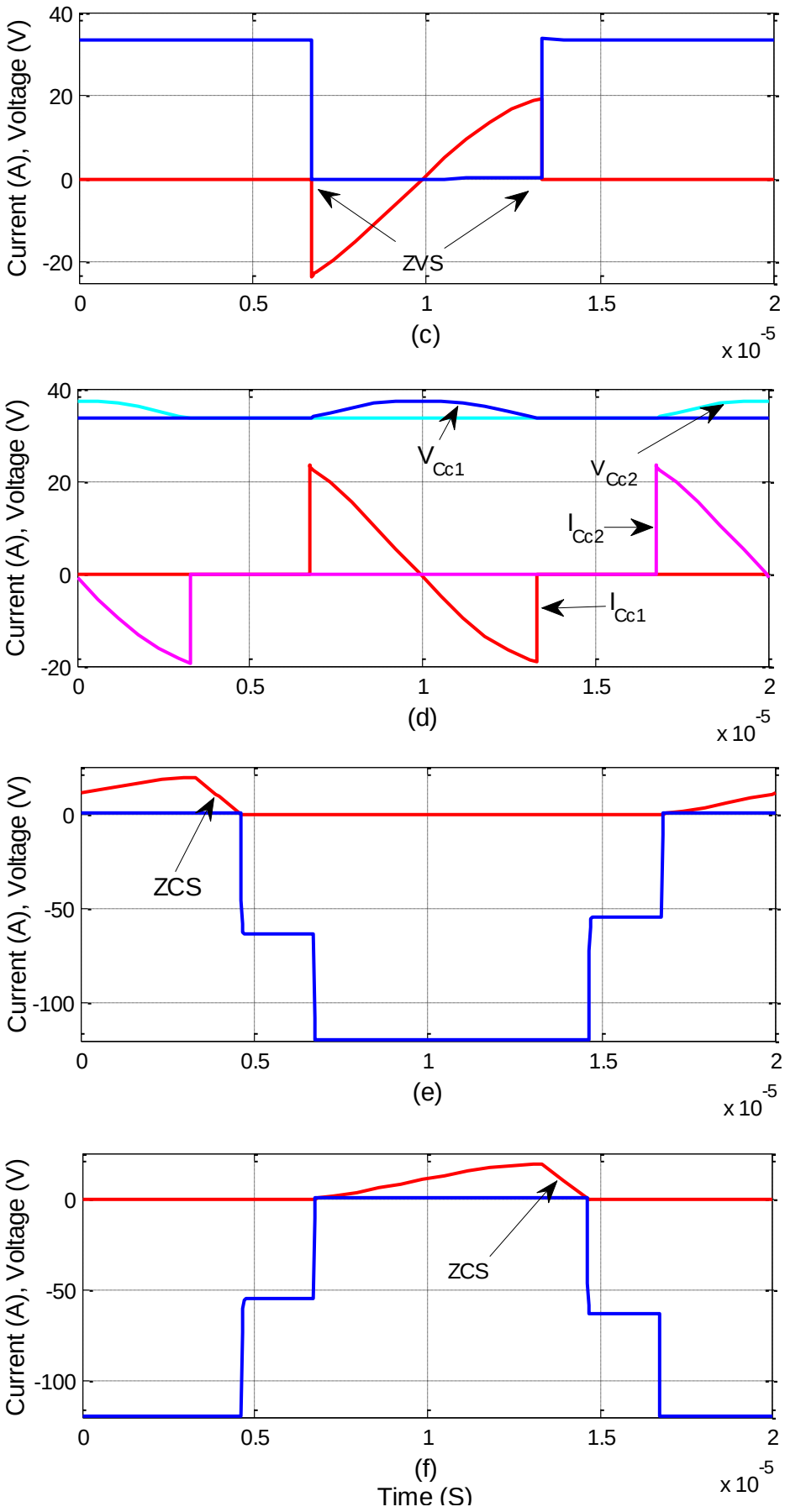

Figure 5.9 (Continued) Simulation results

The clamp circuit, therefore, limits the primary switch voltage excursion (due to leakage inductor interaction with the parasitic capacitor of the switch). The leakage inductance energy is recycled to the output. The voltage and current stress of the output and regenerative diodes are shown in Figure 5.9(e) and Figure 5.9(f) respectively, showing the (ZCS) turn off. The voltage stress of the diodes is equivalent to the converter output voltage (i.e. 120 V). The diode reverse recovery problem is solved because its current falling rate is controlled by the inherent leakage inductance of the coupled inductors.

In summary, the simulation results are clearly in agreement with the analysis presented in section 5.3, for both current and voltage stress of all the semiconductor devices. Furthermore, it gives an insight of the typical behaviour of the converter.

5.6 Experimental Validation

5.6.1 High Step-up Interleaved Boost Converter Prototype

To validate both the theoretical analysis and simulation results, a 500 W converter prototype with $12\,V$ input and $120\,V$ output voltages has been built in the laboratory and tested. The parameters of the converter along with the component ratings are derived from section 5.4 and are shown in Table 5.1. Figure 5.10 shows the photograph of the experimental prototype. All the components of the power converter (power semiconductors, clamp capacitors, switched capacitor and output capacitor) are placed on the same board measuring (120 x 110 x 45) mm.

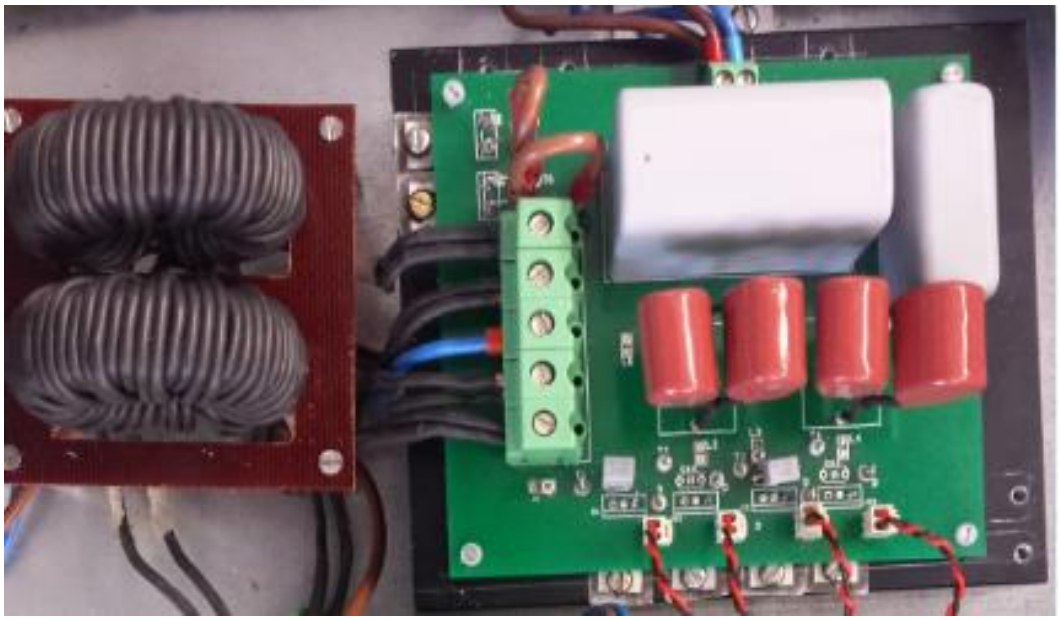

Figure 5.10 Photograph of the experimental prototype

The coupled inductors are placed very close to the main converter board and connected via 5-way PCB terminal block. For details of complete experimental set-up, gate drives circuits and measurement board; refer to Appendix B- to -D.

5.6.2 Measured Experimental Waveforms

The entire system with two-phase interleaved operation has been tested. The test carried out is under $500\ W$ full load condition with $12\ V$ input voltage. The complementary gate signals of the main and clamp switches are shown in Figure 5.11. V_{gS1} and V_{gS2} are the main switch gate signals that are phase shifted 180^o. The duty ratio of the main switches is 0.7, which show that a proper duty ratio is obtained due to reasonable coupled inductor turns ratio design.

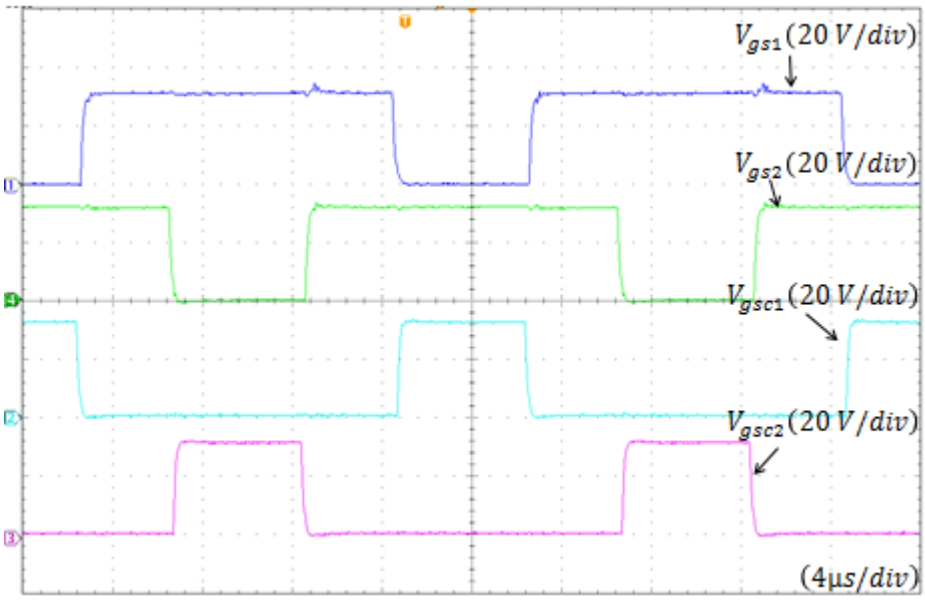

Figure 5.11 Gate signals of the main and clamp switches

Figure 5.12 shows the measured input current and coupled inductors primary currents I_{L1a} and I_{L1b} illustrating the interleaving effect. Although the current ripple on the coupled inductors primary side is large, but the input current ripple is extremely small. The measured peak to peak input current is $4.8\ A\ (12)\%$. At this load condition, the difference in the input current swings is small. The reliability of the input power source and the converter is increased by decreasing the current (AC component). The interleaved scheme also shares the input current and thus relieves the current stress of the input side components. Now comparing the experimental result with the simulation, it can be seen that both the measured peak-peak primary currents of the coupled inductors $I_{L1a} = I_{L1b} = 40\ A$ and the average input current is $I_{in} = 41\ A$. Therefore, it is fair to conclude that both results are in agreement.

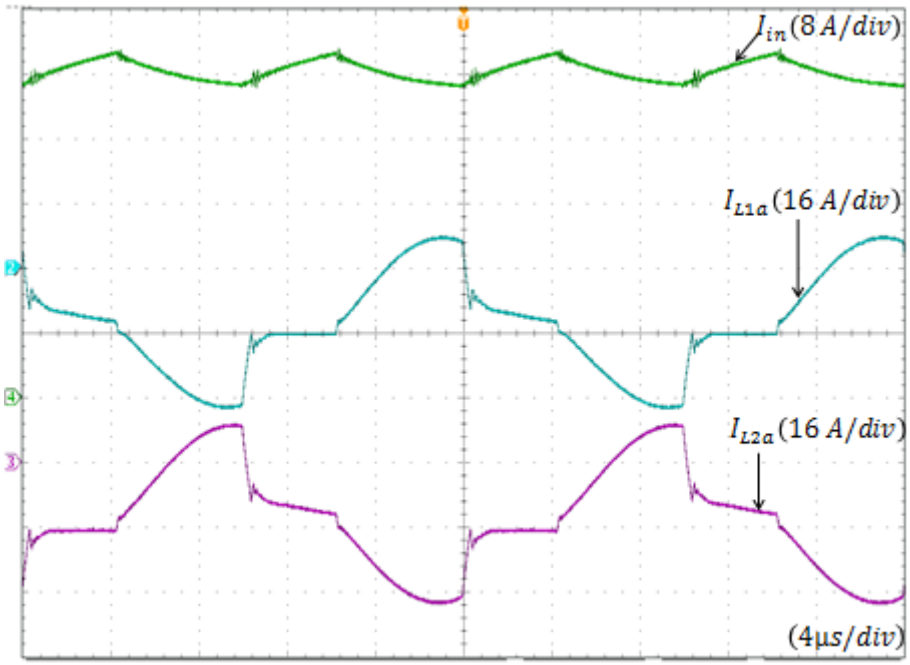

Figure 5.12 Input current and coupled inductor primary current waveforms

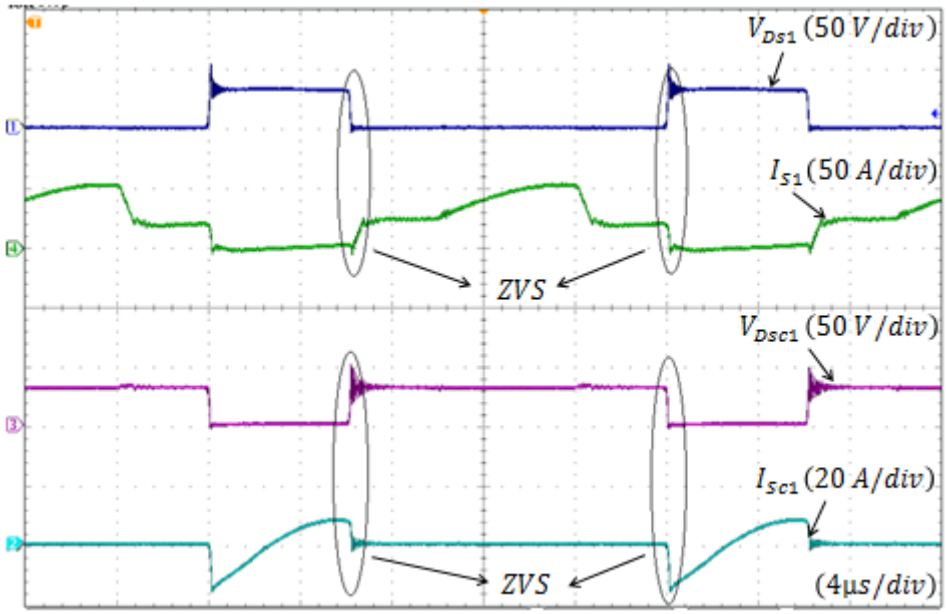

Figure 5.13 Main switch S_1 and clamp switch S_{C1} waveforms

Figure 5.13 shows the drain-source voltages v_{ds1} , v_{dsc1} of the main and clamp switch in one converter leg with their corresponding switch currents I_{S1} , I_{SC1} respectively. The drain-source voltages v_{ds2} , v_{dsc2} of the main and clamp switch in the other leg with their corresponding switch current I_{S2} , I_{SC2} are also illustrated in Figure 5.14. The measured voltage across all the active devices is $32\ V$, which means that the devices voltage stress is approximately one-quarter of the converter output voltage. Lower power switch voltage stress permits low rated power devices to be employed to reduce the conduction losses.

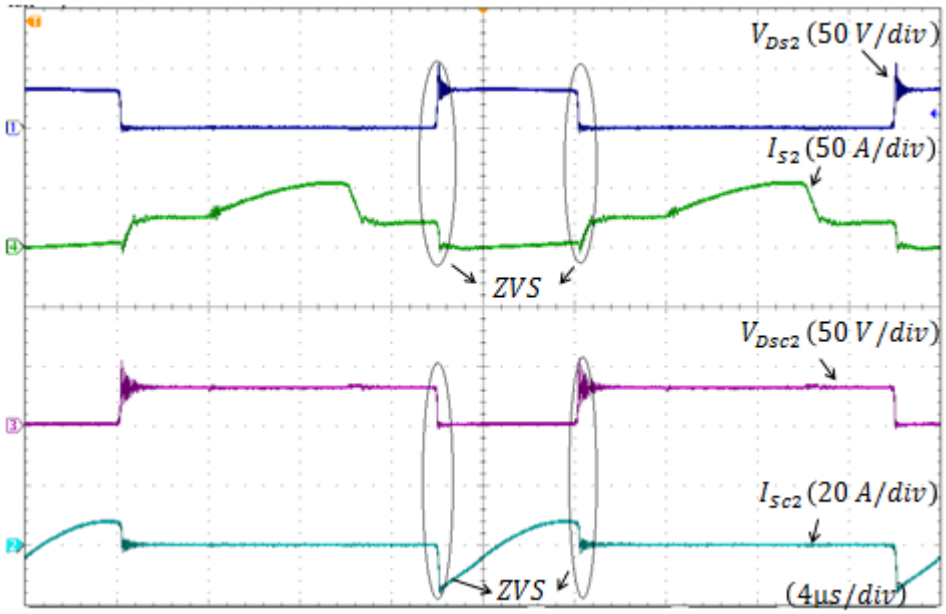

Figure 5.14 Main switch S_2 and clamp switch S_{C2} waveforms

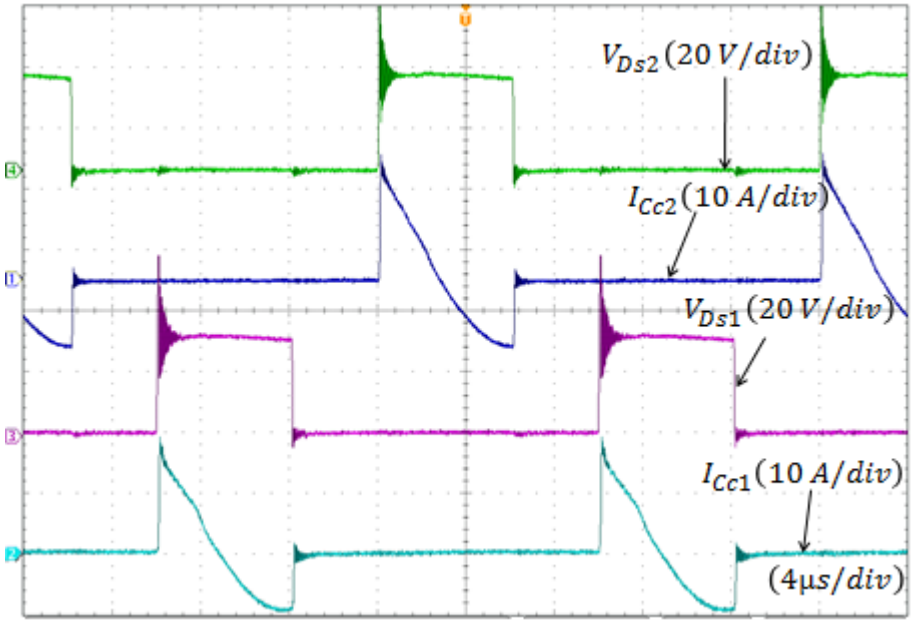

Figure 5.15 Clamp circuit waveforms

It is worth noting that the (ZVS) switching behaviour of all the active switches is achieved. Now comparing the analysis in section 5.3, the simulation in section 5.5 and the experimental results, it is can be concluded that the experimental result validates both the theory and the simulation results.

Figure 5.15 demonstrates the clamp circuit performance in limiting the switch voltage excursion. The drain-source voltage v_{ds1}, v_{ds2} of the main switches and the clamp capacitor current I_{Cc1}, I_{Cc2} are used in illustrating the ACC performance. As can be seen, when either of

the main switches turns off, the leakage inductance energy is released to the clamp capacitors. The drain-source voltages of the main and clamp switches are then clamped to that of clamp capacitor and the voltage spikes of the leakage inductance energy are suppressed. Note also, the active clamp circuit use the entire off time duration to recycle the leakage energy.

To further demonstrate that the voltage stresses of the switches have the same magnitude with the voltage on the clamp capacitors C_{C1}, C_{C2} during either of the switch turns off period, the clamp capacitors waveforms are shown along with the clamp capacitor currents I_{Cc1}, I_{Cc2} in Figure 5.16. At can be seen that when the current begins to follow through either of the clamp capacitors, the corresponding clamp capacitor voltage stress is the same as the drain-source voltage of that particular power switch.

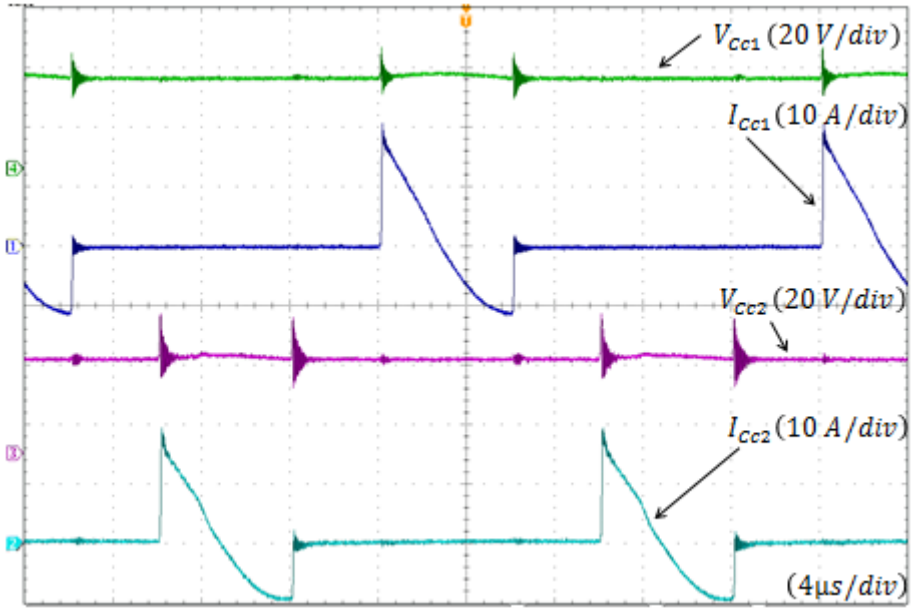

Figure 5.16 Clamp capacitors C_{C1} and C_{C2} waveforms

Figure 5.17 illustrates the regenerative and output diode waveforms. It can be seen both diodes turn off softly with (ZCS) leading to alleviation of the reverse recovery related losses and EMI noise. Because the diodes are in series with the inherent leakage inductance of the coupled inductor, the leakage inductor controls their current decrease rate during turn off. The reverse recovery problem of the diodes is reduced significantly, even though the converter output voltage is high. The maximum power diodes voltage stress is 120 V, which is the same as the converter output voltage as highlighted in the simulation. Figure 5.18 shows a close-up trace of (ZCS) turn off of the diodes, it can be seen that there is no overlap between the diode voltage and current during reverse blocking. The experimental results are consistent with the theoretical analysis and validate both the simulation and theoretical analysis.

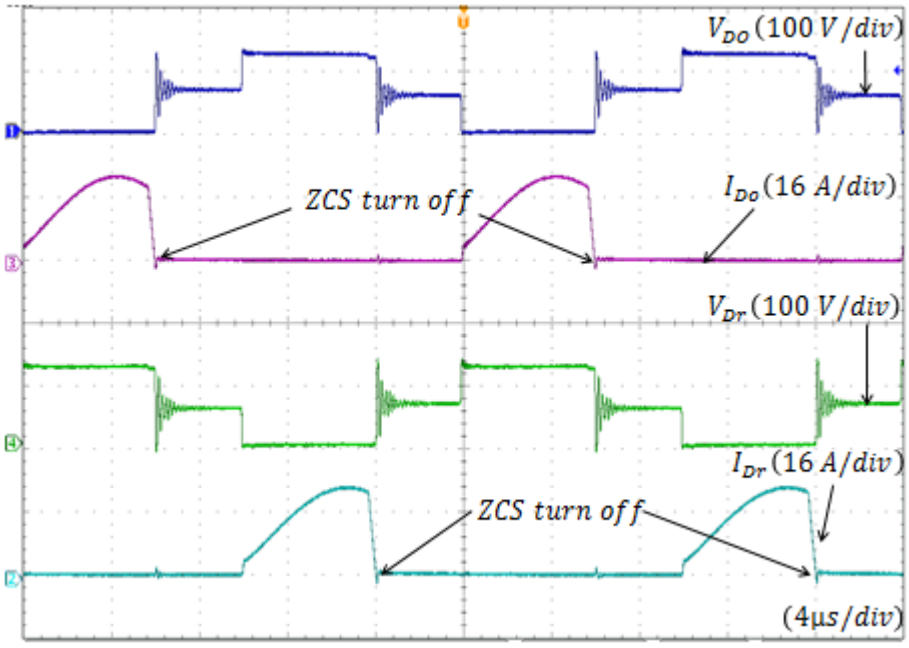

Figure 5.17 Voltage and current stress of the diodes

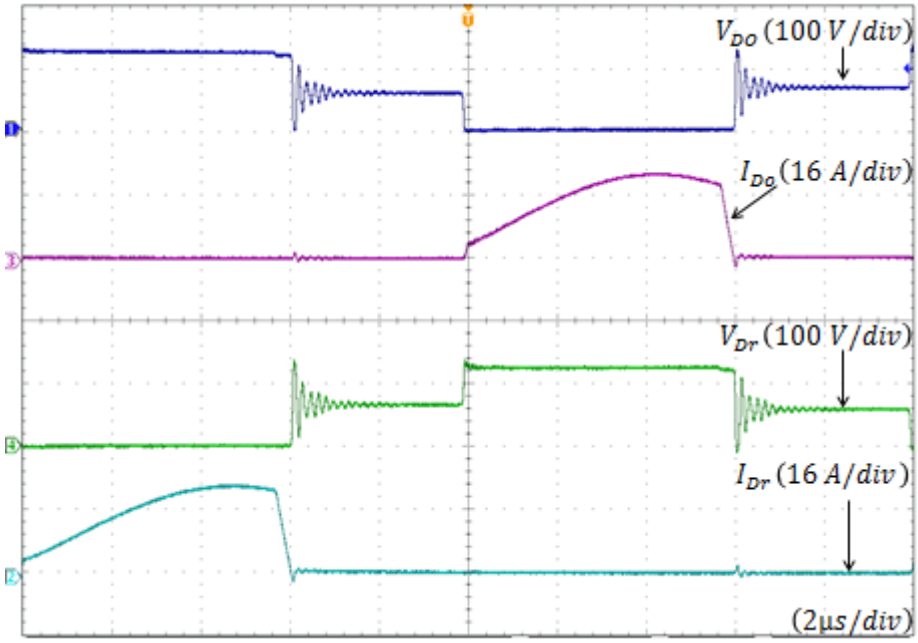

Figure 5.18 (ZCS) turn off of diodes and reverse recovery problem alleviation

5.7 Measured Efficiency

Figure 5.19 shows the measured efficiency of the converter prototype. The measured efficiency data correspond to different load conditions. A maximum efficiency of 96.8% is recorded at 150 W, and the minimum is 91.2% at 500 W. The full load efficiency suffers because of the non-optimal coupled inductors design. Higher efficiency is possible if the

coupled inductors would be optimized.

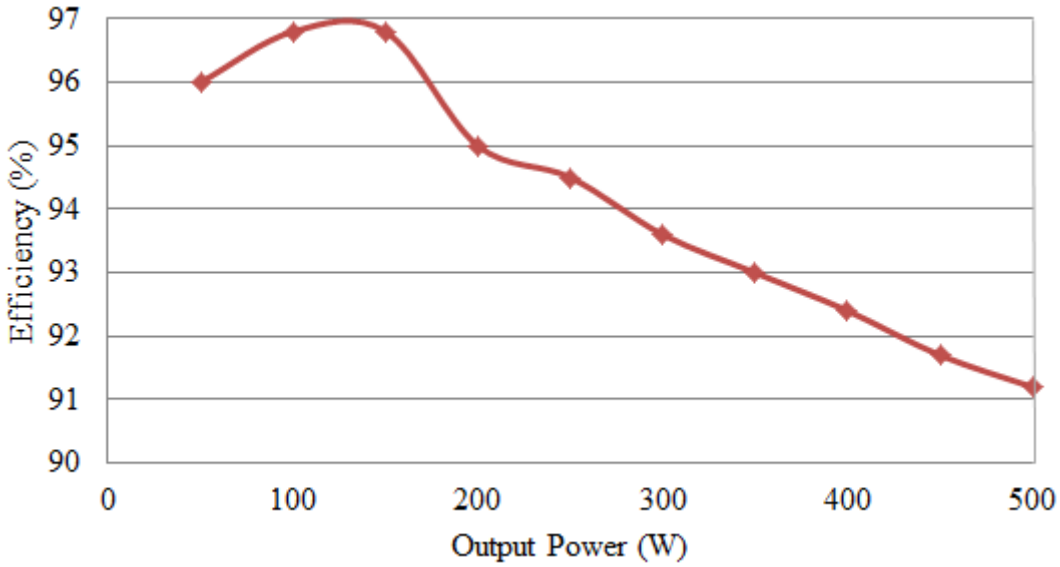

Figure 5.19 Measured Efficiency of the converter

5.8 Summary

Interleaved technique is an effective solution of increasing the power density of DC-DC converters and provides means of minimising the input current ripple. This chapter describes the theoretical analysis, principle of operation, design consideration and experimental results of a new interleaved, non-isolated, (ZVS) converter; based around integrating coupled inductor and switched capacitor approach. The interleaved operation cancels the large coupled inductor current ripple and makes the input ripple very small. Minimising the current/voltage ripple (AC component in the system), ultimately increases the efficiency lifetime of the converter.

The circuit is specifically designed for high voltage gain applications, which are becoming increasingly more widespread. The experimental results, obtained from the 500 W prototype circuits, validate both the theory and operational characteristics of the interleaved power converter. It is shown that the converter has achieved ten times voltage gain with a unit coupled inductor turns ratio($N = 1$), lower turns ratio reduces both the coupled inductor volume and copper loss. Unlike boost, buck-boost and conventional interleaved boost converters, the proposed circuit does not require extreme PWM modulation signals to achieve high conversion ratios. It is also shown that by employing active clamping, the converter has the advantage of achieving (ZVS) of all the active switches, thereby reducing switching losses

significantly.

The proposed topology exhibit low power switch voltage stress (one quarter of the output voltage), which is far lower than the output voltage. Unlike many power converters presented in literature, this unique feature show that lower rated devices can potentially be adopted to reduce the conduction loss. The diodes turn off softly with (ZCS) by utilizing the inherent leakage inductance of the coupled inductor to control their current falling rate. The leakage energy of the coupled inductor is recycled to the output to further enhance the efficiency. The proposed converter is well suited to many industrial applications, such as renewable energy power converters and electric vehicle systems, where high gain power converter technology is becomingly increasingly important.

Chapter 6
Small Signal Modelling and Stability Analysis

6.1 Introduction

Power converters usually consist of passive components and solid state switches. The switching action of the converter as a function of time under the PWM control signal(s) guidance makes the converter a non-linear time-varying system. The circuit may also have a load which contains nonlinear characteristics. However, it is possible to model such a system using computer simulations. A computer simulation such as Matlab-Simulink, Saber, and Pspice are some of the typical simulation environments for analysing the behaviour of a system. This is usually achieved using the built-in library function that represents the behaviour of passive and active components. It is always easier to study the influence of parameter on the system behaviour in simulation, as compared to accomplishing the same on a hardware platform. The overall understanding of the system is improved in simulation and the design process is shortened.

Although the component based model leads to improved understanding of the behaviour of a system under various operating conditions via simulation, but, it does not give an account of the stability of the converter or its transient analysis when the operating points are perturbed. The analytical model, on the other hand, provides a better understanding of the system and its experimental behaviour which facilitates the overall design. It is sometimes difficult to derive an accurate mathematical model that describes the behaviour of a system at various operating conditions. However, there is always a compromise between the accuracy of the mathematical model and its simplicity.

Under constant input voltage, appropriate switching on and off the power devices by decreasing or increasing the control parameter, the system operate around an equilibrium point and the signals involved may be considered as the small signals around the equilibrium.

Then a linearized analytical model characterising the behaviour of the converter around an equilibrium point can be derived. The average model is usually derived by taking the average of the two instants (on and off) in one switching cycle. The average equation is then linearized about the equilibrium point by expanding into Tylor's series and keeping only the linear terms. The higher order terms are therefore neglected, with the assumption that the variables deviate only slightly from the operating condition.

This chapter presents a small signal analysis of high step-up interleaved boost converter and controller design.

6.2 Modelling Assumptions

To simplify the state space averaging method the following assumptions are made:

1. Mode of Operation: there are two operating modes in DC-DC converters; continuous and discontinuous conduction modes. A converter operates in the CCM if its inductor current flows continuously without break and is non-zero during the entire switching period. Otherwise, it operates in DCM in which the inductor current falls to zero. In this work the inductor current is continuous and non-zero for the entire switching duration.
2. Equal Current Sharing between Interleaved Phases: the magnetising inductance and their corresponding leakage inductance design is evenly distributed. Therefore, equal current sharing is assumed to exist between the phases.
3. Negligible Dead Time: the dead time between turning on of the main switch and its corresponding clamp switch in which the (ZVS) occurs is short compared to the total switching period and thus neglected.
4. Ideal Components: In reality, the components of any power converter such as inductors, capacitors, switches and diodes contain parasitic components. For example, the windings resistance of an inductor, the MOSFET on-state resistance, ESR of capacitors and forward voltage drops of diodes are the main parasitic that affects the converter dynamics. However, for simplicity, all the components are considered lossless. Thus, their parasitic elements are not included in the analysis.
5. During the main switch on time, the current through the primary winding of the coupled inductor rises linearly, whilst the secondary current remain zero. This means only the primary winding produces the flux in the magnetic core. However,

during the switch off time instance a current flows through both primary and secondary windings. The flux linkage is continuous but cannot be used as a state variable. Instead a magnetizing inductor current is adopted to be the state variable of the coupled inductors [126-128].

6.3 Small Signal Analysis Using State space Averaging

6.3.1 Interleaved Converter Model

The averaged model of the interleaved circuit can be derived by averaging the state equations of both on and off-states using Kirchhoff's laws. There are seven energy storage elements, magnetising inductor $L_{m\,1}$, $L_{Lm\,2}$and clamping capacitors C_{C1}, C_{C2}. Others include the equivalent leakage inductance of the secondary side L_K, switched capacitor C_m and the output capacitor C_O. These storage elements determine the system order. The currents through the magnetising inductors and capacitor voltages are adopted to be the state vectors as this is usually convenient and customary in electrical networks [47, 99, 129]. The state space model of the converter can be written using general state space equations:

$$\begin{aligned} \dot{\mathbf{x}} &= A\mathbf{x} + Bu \\ y &= C\mathbf{x} + Du \end{aligned} \tag{6.1}$$

State variables defined include currents through the magnetising inductors i_{Lm1}, i_{Lm2}, the voltage across clamp capacitors v_{Cc1}, v_{Cc2} leakage inductor current i_{LK} and output voltage v_O. Considering that i_{Lk} is discontinuous and its average value in one switching cycle is zero and the steady state value of $v_{Cm} = v_o/2$ (see equation 5.11). Therefore, the state variables reduces to

$$\times = [i_{Lm1}\ \ i_{Lm2}\ \ v_{Cc1}\ \ v_{Cc2}\ \ v_o\ ]^T \tag{6.2}$$

And the input is defined as

$$u = V_{in} \tag{6.3}$$

6.3.2 Averaging

To fully develop the state space average model of the converter, it is important to consider the high step-up boost converter modes of operation [47, 99, 129], (see Figure 5.3). The average model of the circuit can be developed by averaging the state equations of the on-period and off-period (neglecting short operating intervals). The state space equations for each sub-

interval of operation are described by Kirchhoff laws (voltage and current laws). The state space average equations are given by:

$$\begin{cases} L_{m1}\dfrac{d\overline{\bar{i}_{Lm1}}}{dt} = v_{in} - (1-d_{s1})v_{Cc1} \\ L_{m2}\dfrac{d\bar{i}_{Lm2}}{dt} = v_{in} - (1-d_{s2})v_{Cc2} \\ C_{C1}\dfrac{d\bar{v}_{Cc1}}{dt} = (1-d_{s1})i_{Lm1} - \dfrac{T_s}{2L_k}\left((N+1)v_{Cc1} - \dfrac{v_o}{2}\right)(1-d_{s1})^2 \\ C_{C2}\dfrac{d\bar{v}_{Cc2}}{dt} = (1-d_{s2})i_{Lm2} - \dfrac{T_s}{2L_k}\left((N+1)v_{Cc1} - \dfrac{v_o}{2}\right)(1-d_{s1})^2 \\ C_o\dfrac{d\bar{v}_o}{dt} = \dfrac{(1-d_{s1}+d')i_{Lm1}}{(N+1)} - \dfrac{v_o}{R} \end{cases} \tag{6.4}$$

Where d_{s1} and d_{s2} are the duty cycles of main switch S_1 and S_2 respectively and d' is the period between the peak value of the leakage inductor current to its zero crossing during the positive half cycle which is the same as ΔD (see Figure 5.3). T_s denotes the converter switching time. Representing (6.4) in the form of (6.1) gives

$$A = \begin{bmatrix} 0 & 0 & -\dfrac{(1-d_{s1})}{L_{m1}} & 0 & 0 \\ 0 & 0 & 0 & -\dfrac{(1-d_{s2})}{L_{m2}} & 0 \\ \dfrac{(1-d_{s1})}{C_{c1}} & 0 & -\dfrac{T_s(1-d_{s1})^2(N+1)}{2L_kC_{c1}} & 0 & \dfrac{T_s(1-d_{s1})^2}{4L_kC_{c1}} \\ 0 & \dfrac{(1-d_{s2})}{C_{c2}} & 0 & -\dfrac{T_s(1-d_{s2})^2(N+1)}{2L_kC_{c2}} & \dfrac{T_s(1-d_{s1})^2}{4L_kC_{c2}} \\ \dfrac{(1-d_{s1}+d')}{(N+1)C_o} & 0 & 0 & 0 & -\dfrac{1}{R_oC_o} \end{bmatrix}$$

And the input, output and state transition matrices of the system are given by

$$B = \begin{bmatrix} \dfrac{1}{L_{m1}} & \dfrac{1}{L_{m2}} & 0 & 0 & 0 \end{bmatrix}^T \quad C = [0 \quad 0 \quad 0 \quad 0 \quad 1] \quad D = [0]$$

Equation (6.4) represents the average model of the converter.

6.3.3 Steady State

The state space averaged DC model that describe the converter in equilibrium is obtained by letting the left-hand side (LHS) of each state equation in (6.4) equal to zero, from which

$$\mathrm{X} = -A^{-1}BU \tag{6.5}$$

And the set of attainable equilibrium points are:

$$\times = \begin{bmatrix} I_{Lm1} \\ I_{Lm2} \\ V_{Cc1} \\ V_{Cc2} \\ V_o \end{bmatrix} = \begin{bmatrix} \dfrac{2T_s V_{in}(N+1)^2}{4L_k(N+1) + R_o T_s(1+d^2+d'-2d-dd')} \\ \dfrac{2T_s V_{in}(N+1)^2}{4L_k(N+1) + R_o T_s(1+d^2+d'-2d-dd')} \\ V_{in}/(1-d) \\ V_{in}/(1-d) \\ \dfrac{2T_s R_o V_{in}(N+1)(1-d+d')}{4L_k(N+1) + R_o T_s(1+d^2+d'-2d-dd')} \end{bmatrix} \tag{6.6}$$

From (6.6) the voltage gain expression can be written as

$$\frac{V_o}{V_{in}} = \frac{2T_s R_o(N+1)(1-d+d')}{4NL_{Lk}(N+1) + R_o T_s(1+d^2+d'-2d-dd')} \tag{6.7}$$

Equation (6.7) is a non-ideal static gain expression which takes into account the equivalent leakage inductance of the coupled inductors and is more precise than (5.18)

6.3.4 Model Transfer Function

It is possible and also desirable to derive the transfer function of the interleaved high step-up converter from the state space model. The equation converting state space models to Laplace transfer functions is given by

$$G(s) = \frac{\begin{vmatrix} SI - A & -B \\ C & D \end{vmatrix}}{|SI - A|} \tag{6.8}$$

From (6.8), the line to output transfer function result in the following equation

$$G_v(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{p_1 s + p_2}{s^3 + q_1 s^2 + q_2 s + q_3} \tag{6.9}$$

Where

$p_1 = (1-d+d') \cdot s/(N+1)C_o L_m$

$p_2 = T_s(1-d)^2(1-d+d')/2L_k C_c L_m$

$q_1 = \dfrac{T_s(1-d)^2(N+1)}{2L_k C_c} + \dfrac{1}{R_o C_o}$

$q_2 = \dfrac{T_s(1-d)^2(N+1)}{2L_k C_c R_o C_o} + \dfrac{(1-d)^2}{L_m C_c}$

$q_3 = \dfrac{T_s(1-d)^2(1-d+d')}{4(N+1)L_m L_k C_c C_o} + \dfrac{(1-d)^2}{L_m C_c R_o C_o}$

6.3.5 Model Validation with Simulink

The line to output transfer function derived in (6.9) is verified with direct simulation in Matlab-Simulink with switch model. The parameters used in the simulation and that of the averaged model are those listed in Table 5.1. The simulations have been performed under full load condition with 12 V input voltage.

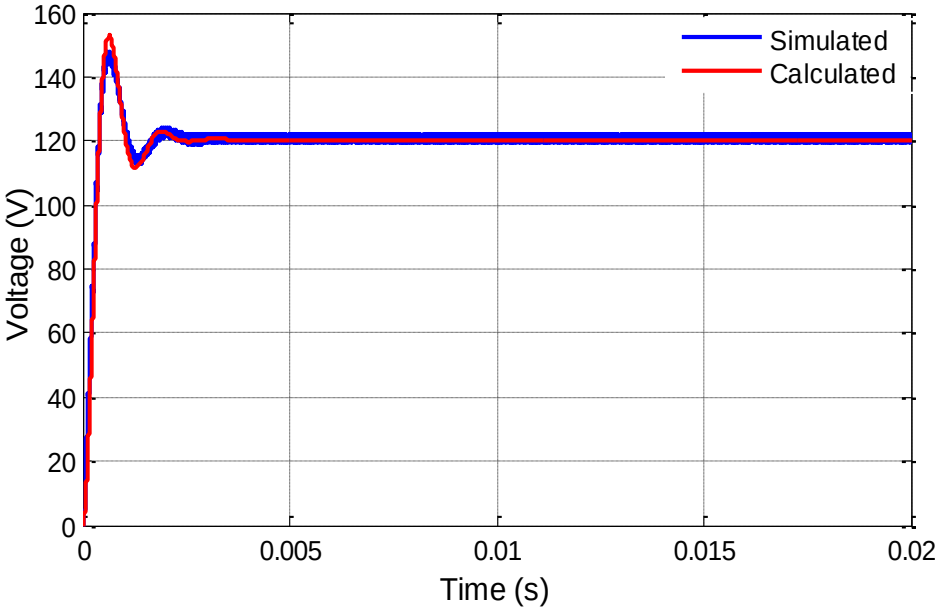

Figure 6.1 Direct simulation in Matlab

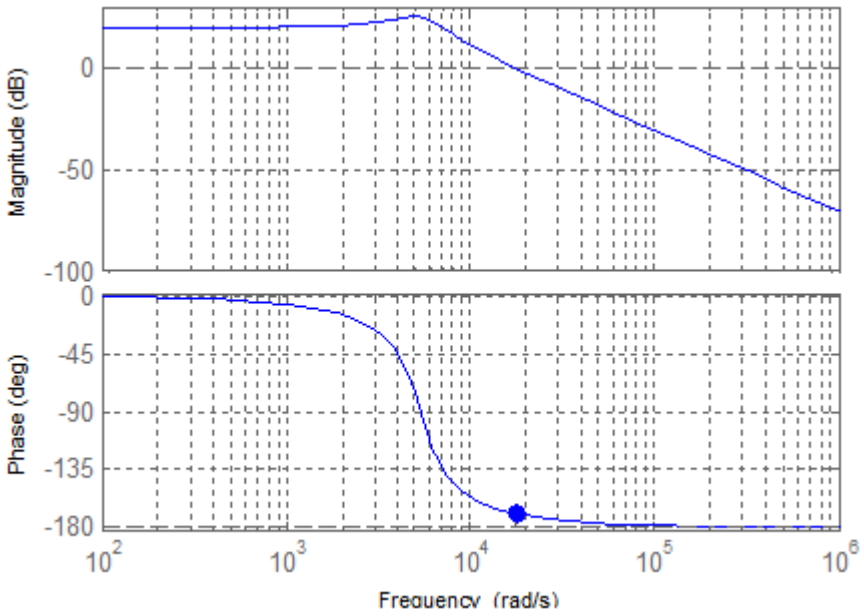

Figure 6.2 Bode diagram of transfer function

Figure 6.1 illustrates the output voltages response of the switch model and the calculated model of (6.9), it is reasonable to conclude that a good agreement exists between the models. The agreement indicates that the derived averaged models can be used for the real system frequency domain analysis and controller design. The frequency response of the static gain transfer function is shown by the Bode plot of Figure 6.2. The system has an infinite gain margin (GM) and a phase margin (PM) of 11^{o} at the gain crossover frequency of 17.5 Krad/sec. The log magnitude curve has a slope of 40dB/dec.

6.3.6 Perturbation

A linearized system can be develop by introducing perturbation around the steady state value of the averaged model calculated in (6.4), containing the steady state dc value (nominal component) represented by uppercase letter and a superimposed ac variation represented by lowercase symbol with circumflex. For instance the perturbation definitions for the state variable are: $i_{Lm} = I_{Lm} + \hat{\imath}_{Lm}$, $v_{in} = V_{in} + \hat{v}_{in}$, $v_o = V_o + \hat{v}_o$ and $d = D + \hat{d}$. The following expressions are obtained

$$\begin{cases} L_{m1}\dfrac{d(I_{Lm1}+\hat{\imath}_{Lm1})}{dt} = V_{in} + \hat{v}_{in} - (V_{Cc1} + \hat{v}_{Cc1})\left(1 - D - \hat{d}_{s1}\right) \\ L_{m2}\dfrac{d(I_{Lm2}+\hat{\imath}_{Lm2})}{dt} = V_{in} + \hat{v}_{in} - (V_{Cc2} + \hat{v}_{Cc2})\left(1 - D - \hat{d}_{s2}\right) \\ C_{C1}\dfrac{d(V_{Cc1}+\hat{v}_{Cc1})}{dt} = (I_{Lm1} + \hat{\imath}_{Lm1})\left(1 - D - \hat{d}_{s1}\right) - \dfrac{T_s\left(1 - D - \hat{d}_{s1}\right)^2}{2L_k}\left((N+1)(V_{Cc1} + \hat{v}_{Cc1}) + \dfrac{(V_o + \hat{v}_o)}{2}\right) \\ C_{C2}\dfrac{d(V_{Cc2}+\hat{v}_{Cc2})}{dt} = (I_{Lm2} + \hat{\imath}_{Lm2})\left(1 - D - \hat{d}_{s2}\right) - \dfrac{T_s}{2L_k}\left((N+1)(V_{Cc2} + \hat{v}_{Cc2}) + \dfrac{(V_o + \hat{v}_o)}{2}\right) \\ C_o\left\langle\dfrac{d(V_o+\hat{v}_o)}{dt}\right\rangle = \dfrac{I_{Lm1} + \hat{\imath}_{Lm1}}{(N+1)}\left(1 - D - \hat{d}_{s1} + D' + \hat{d}'\right) - \dfrac{(V_o + \hat{v}_o)}{R_o} \end{cases} \tag{6.10}$$

6.3.7 Linearization

Finally, by assuming that the components of the converter have the same values (i.e. $L_{m1} = L_{m2} = L_m$ and $C_{C1} = C_{C2} = C_C$), the linearized model of the converter can be obtained. The duty cycle of the main switches S_1 and S_2 are the same in both phases, which means $d_{s1} = d_{s2} = d$, but phase shifted 180^o. The system is linearized about this steady state operating point by expanding and neglecting the higher order perturbation terms, then removing the steady-state quantities [99, 126]. Therefore, the following sets of equations are obtained.

$$\begin{cases} L_m \dfrac{d\hat{\imath}_{Lm1}}{dt} = \hat{v}_{in} - V_{Cc}\hat{d} - (1-D)\hat{v}_{Cc} \\ L_m \dfrac{d\hat{\imath}_{Lm2}}{dt} = \hat{v}_{in} - V_{Cc}\hat{d} - (1-D)\hat{v}_{Cc} \\ C_C \dfrac{d\hat{v}_{Cc1}}{dt} = (1-D)\hat{\imath}_{Lm} - I_{Lm}\hat{d} - \dfrac{T_s}{2L_k}\left((N+1)\hat{v}_{Cc1} - \dfrac{\hat{v}_o}{2}\right)(1-D)^2 + \dfrac{T_s(1-D)\hat{d}}{L_k}\left((N+1)V_{Cc1} - \dfrac{V_o}{2}\right) \\ C_C \dfrac{d\hat{v}_{Cc2}}{dt} = (1-D)\hat{\imath}_{Lm} - I_{Lm}\hat{d} - \dfrac{T_s}{2L_k}\left((N+1)\hat{v}_{Cc2} - \dfrac{\hat{v}_o}{2}\right)(1-D)^2 + \dfrac{T_s(1-D)\hat{d}}{L_k}\left((N+1)V_{Cc2} - \dfrac{V_o}{2}\right) \\ C_o \dfrac{d\hat{v}_o}{dt} = \dfrac{\hat{\imath}_{Lm}(1-D+D')}{(N+1)} - \dfrac{I_{Lm}\hat{d}}{(N+1)} + \dfrac{I_{Lm}\hat{d}'}{(N+1)} - \dfrac{\hat{v}_o}{R_o} \end{cases} \tag{6.11}$$

Applying modelling assumption that there is an equal current sharing between the interleaved phases of the converter such that $i_{Lm1} = i_{Lm2} = i_{Lm}$, $i_{Lm1} + i_{Lm2} = i_{In}$ and the clamp capacitor voltages are equal $V_{Cc1} = V_{Cc2} = V_{Cc}$ [99, 130]. Equation (6.11) can be simplified to

$$\begin{cases} L_m \dfrac{d\hat{\imath}_{in}}{dt} = 2\hat{v}_{in} - V_{Cc}\hat{d} - 2(1-D)\hat{v}_{Cc} \\ C_C \left\langle \dfrac{dv_{Cc}}{dt} \right\rangle = (1-D)\hat{\imath}_{Lm} - I_{Lm}\hat{d} - \dfrac{T_s(1-D)^2}{2L_k}\left((N+1)\hat{v}_{Cc} - \dfrac{\hat{v}_o}{2}\right) + \dfrac{T_s(1-D)\hat{d}}{L_k}\left((N+1)V_{Cc} - \dfrac{V_o}{2}\right) \\ C_o \dfrac{d\hat{v}_o}{dt} = \dfrac{\hat{\imath}_{in}(1-D+D')}{2(N+1)} - \dfrac{I_{Lm}\hat{d}}{2(N+1)} + \dfrac{I_{Lm}\hat{d}'}{(N+1)} - \dfrac{\hat{v}_o}{R_o} \end{cases} \tag{6.12}$$

6.3.8 Transfer function

Now taking Laplace transform of (6.12) and replacing s with d/dt. Then eliminating $\hat{d}'$ yield the small signal low-frequency model of the interleaved high step-up DC-DC converter.

$$\begin{bmatrix} \hat{\imath}_{in}(s) \\ \hat{v}_{CC}(s) \\ \hat{v}_o(s) \end{bmatrix} = [A(s)]^{-1} \begin{bmatrix} b_1(s) \\ b_2(s) \\ b_3(s) \end{bmatrix} \hat{d}(s) + [A(s)]^{-1}[C(s)]\hat{v}_{in}(s) \tag{6.13}$$

Where:

$$A = \begin{bmatrix} s & \dfrac{2(1-D)}{L_m} & 0 \\ -\dfrac{(1-D)}{C_c} & s + \dfrac{(N+1)(1-D)^2}{2f_s L_k C_c} & -\dfrac{(1-D)^2}{4L_k C_c} \\ -\dfrac{(1-D+D')}{2(N+1)C_o} & \dfrac{2I_{Lm}(1-D)}{C_o V_o} & s + \dfrac{1}{R_o C_o} + \dfrac{2I_{Lm}(1-D+D')}{(N+1)C_o V_o} \end{bmatrix}$$

$$B = \left[\frac{2V_{Cc}}{L_m}, \quad \frac{(1-D)\left((N+1)V_{Cc} - \frac{V_o}{2}\right)}{f_s L_k C_c} - \frac{I_{Lm}}{C_c}, \quad -\frac{2I_{Lm}V_{Cc}}{V_o C_o}\right]^T, \qquad C = (0 \quad 0 \quad 1)$$

Various transfer functions can be obtained from (6.13), such as control-to-output or line -to-output transfer functions. The model can as well be used for closed loop control design of the converter.

6.3.9 Duty Ratio Control

By setting $\hat{v}_{in}(s) = 0$ in (6.13), the direct duty ratio control (control-to-output transfer function) can be obtained, and is given by

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{1}{|A(s)|}[A_{31} \quad A_{32} \quad A_{33}]\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} \tag{6.14}$$

Where b_1, b_2, b_3 are the elements of the input matrix B above. From (6.14), the control-to-output transfer function is found to be

$$G_{vd} = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{a_1 s^2 + a_2 s + a_3}{p_1 s^3 + p_2 s^2 + p_3 s + p_4} \tag{6.15}$$

Where

$a_1 = L_m C_c b_1$

$a_2 = \frac{(1 - D + d')C_c}{2(N+1)} \cdot b_1 + \frac{2I_{Lm}L_m(1-D)}{V_o} \cdot b_2 + \frac{(1-D)^2 L_m}{f_s L_K} \cdot b_3$

$a_3 = (1-D)^2\left(\frac{(1-D+D')}{2f_s L_K} + \frac{2I_{Lm}(1-D)}{V_o}\right) \cdot b_1 - \frac{2(1-D+D')(1-D)}{(N+1)} \cdot b_2 + 2(1-D)^2 \cdot b_3$

$p_1 = L_m C_c C_O$

$p_2 = \frac{L_m C_O (1-D)^2}{f_s L_K} + L_m C_c\left(\frac{1}{R_O} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o}\right)$

$p_3 = \frac{L_m(1-D)^2}{f_s L_K}\left(\frac{1}{R_O} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o}\right) + 2C_O(1-D)^2$

$p_4 = 2(1-D)^2\left(\frac{1}{R_O} + \frac{2I_{Lm}(1-D+D')}{(N+1)V_o} + \frac{(1-D)(1-D+D')}{f_s L_K (N+1)^2}\right)$

Where D' represents the steady state dc value (nominal component) of d' denoted by uppercase letter. The transfer function coefficients of (6.5) can be calculated by substituting the system parameters values depicted in Table 5.1. The effect of duty ratio perturbation on the converter can then be determined from (6.15). The control-to-output transfer function describes a standard third order system and has a negative real pole at $s = -5.65e05$, two

complex conjugate poles at $s = -7.57 \pm j1.3e03$, and two zeros at $s = -5.65e05$ and $s = 1.34e04$ respectively. The control-to-output transfer function exhibit a non-minimum phase system, which is typical behaviour of converters with boost or buck-boost characteristics

The calculated control-to-output transfer function is verified in simulation by perturbing duty cycle set point with sinusoids of different frequencies and stores the corresponding output voltage. A discrete point can be found from the frequency response that describes how the system responds to the magnitudes and phase of the injected sinusoids. Therefore, a control-to-output transfer function can be estimated from the measured data. Figure 6.3 illustrates the Bode plots of both the calculated and estimated response of the control-to-output transfer function. The system PM and GM are negative (-73 and -29.9), which makes the system unstable under the influence of disturbance in input voltage or load variation.

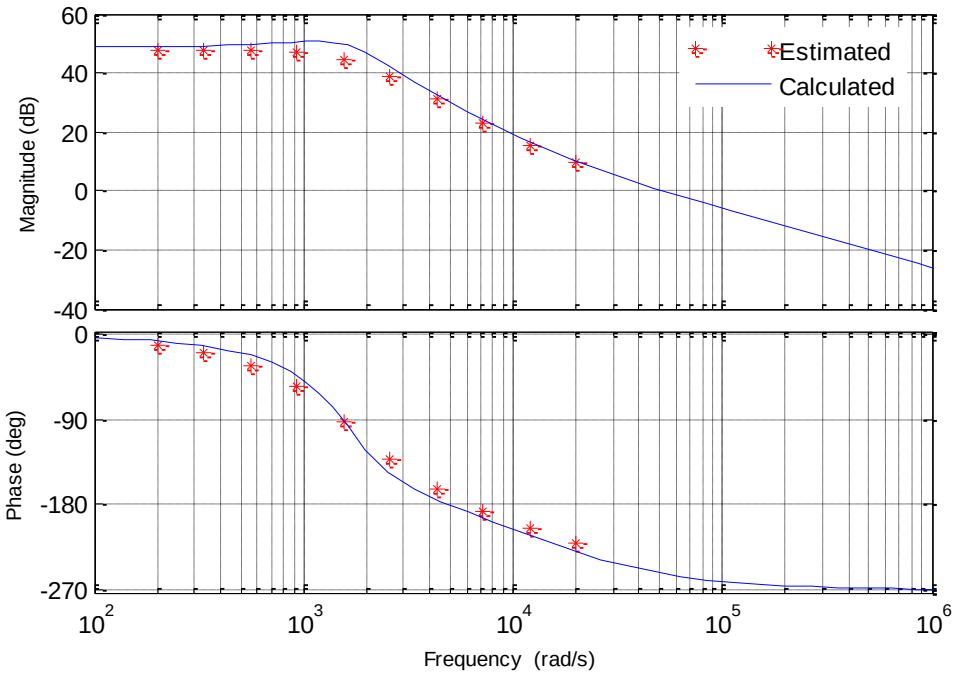

Figure 6.3 Calculated and estimated control to output transfer function

The duty ratio selection is not explicitly control, but rather accepted as influenced by the converter nominal operating point due to the control function. Likewise the load resistance range, which is also based on DC loads requirement. The load resistance and duty ratio are exogenous quantities that requires compensation scheme due to pole-zero variation. Figure 6.4 and Figure 6.5 shows the Bode plot of the small signal model as the duty cycle D and load resistor R_O are varied over their nominal operating points.

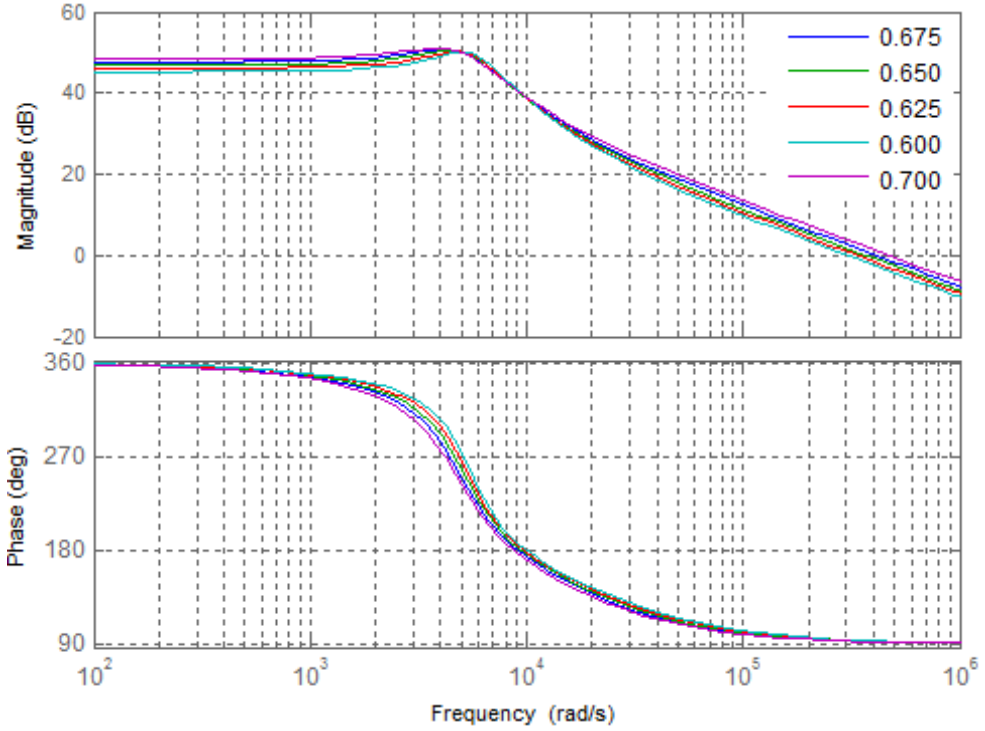

Figure 6.4 Variation in DC gain with duty ratio

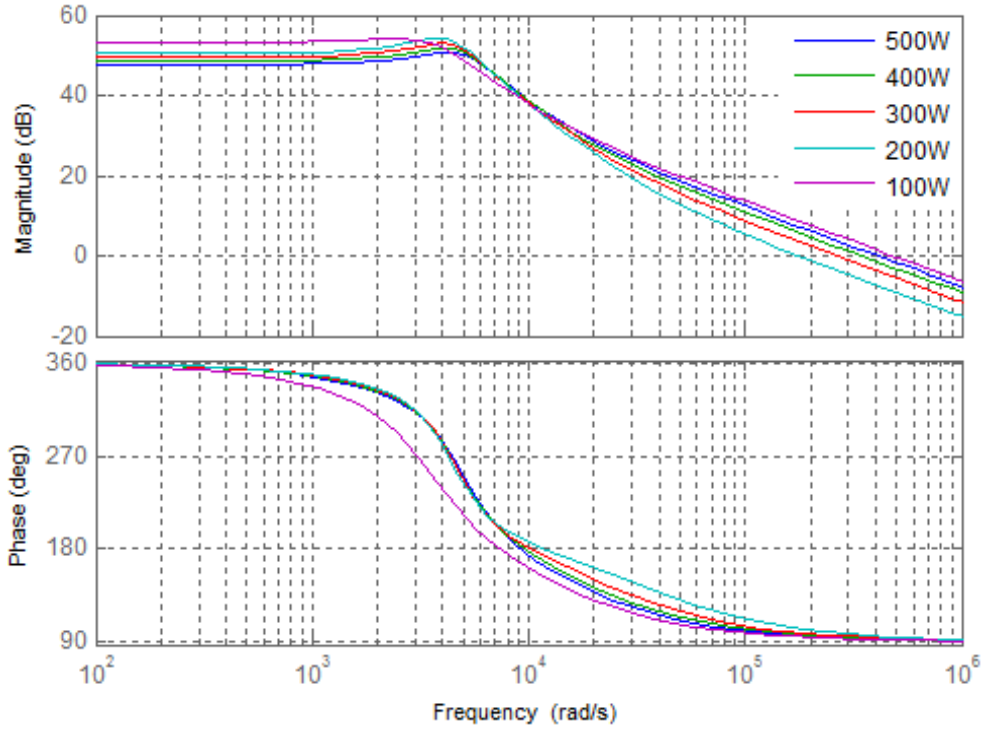

Figure 6.5 Load change effect

Figure 6.4 shows a frequency response curve, illustrating the effects of varying the duty cycle of the high step-up converter at full load condition. Here the duty cycle is varied from $0.6 \leq D \leq 0.7$, the right-half plane (RHP) zero effect on both magnitude and phase plots are apparent.

Figure 6.5 shows the frequency response curve, illustrating the effect of varying the load resistor R_O at a constant duty ratio of 0.65. The variation of the load resistor also causes variation in the magnitude of the RHP zero above the pole. Change in the phase of the RHP zero above the pole is expected when the load resistor is shifted further to the high end of its range.

6.4 Current Mode Control

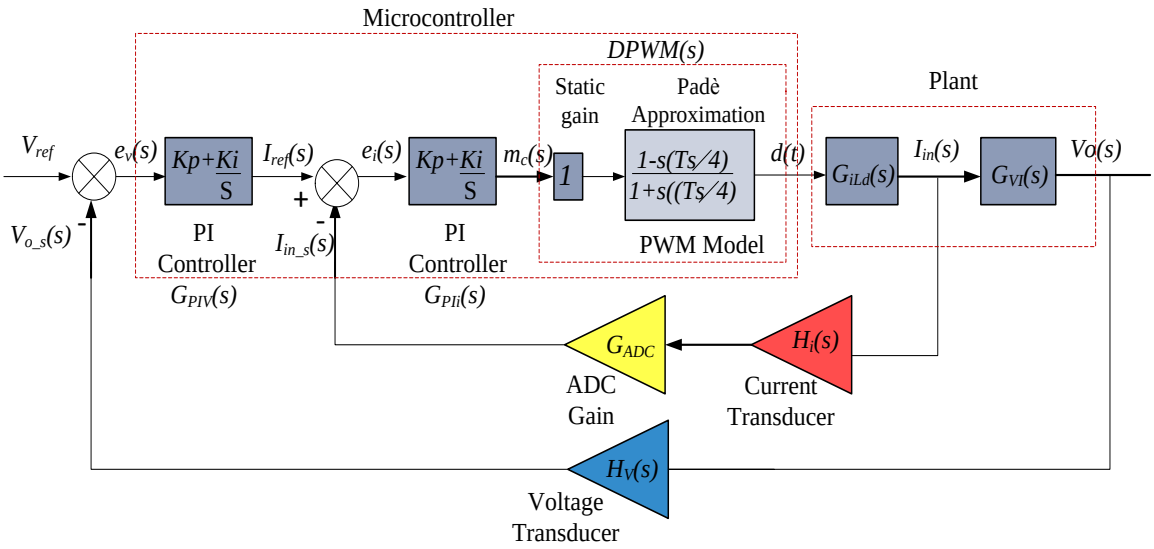

Figure 6.6 Block diagram of dual loop feedback control diagram of high step-up interleaved boost converter in continuous domain

Figure 6.6 shows the block diagram of the current mode control. The control architecture is a typical cascade controller comprising of outer voltage and inner current control loops. The presence of the RHP zero in the control-to-output transfer function tends to destabilize the traditional single-loop feedback control. Furthermore, it is difficult to obtain an adequate phase margin, because during transient the phase lag of the RHP zero causes the output to change initially in the wrong direction. The loops are usually defined to satisfy certain design criteria of PM and bandwidth. The outer voltage loop has slow dynamics whilst the inner current loop has fast dynamics. This is done to allow the input current to change more quickly than the converter output voltage [99, 131].

The feedback control system uses proportional-integral (PI) controller in both loops. The outer voltage loop determines the current reference of the inner current loop, whilst the control signal is determined by the inner current controller. The control signal generates the gating signals of the main switches S_1 and S_2 with the same duty ratio with the aid of ePWM

submodule. Two modulators shifted in phase by 180^0 are used to produce the gating signals. Note that the gate signal of the clamp switches S_{C1} and S_{C2} are complementary to their corresponding primary switches. The current and voltage transducers presence has been taken into account with their respective gains H_i and H_v respectively and this is usually implemented in practice by Hall effect sensors.

6.4.1 Inner Current Control Loop

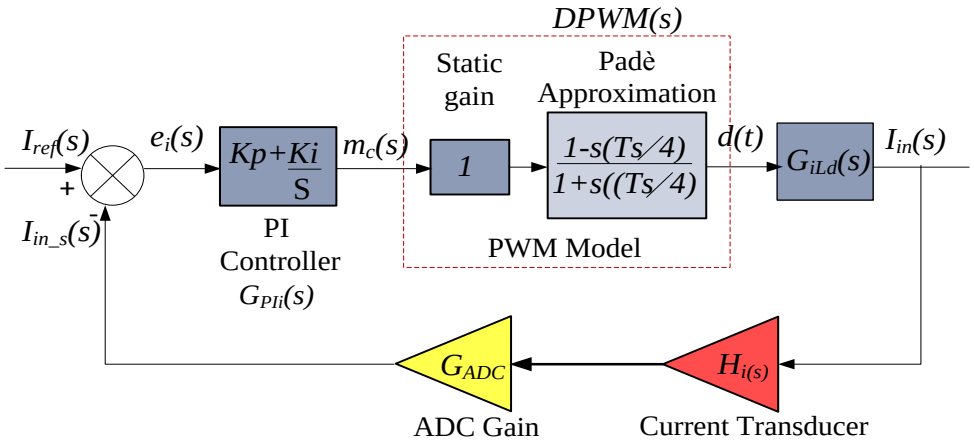

Figure 6.7 Block diagram of current control loop in continuous domain

Figure 6.7 illustrates the block diagram of inner current loop. Each of the components is represented by their respective transfer functions. In particular, the controller is typically represented by PI compensator, whose proportional gain K_p and integral gain K_I are determined in this section. As previously explained, once the outer voltage loop sets the current reference of the inner current loop, the error between the actual and desired current is processed in the PI controller. The controller output produces a modulating signal that drives the digital pulse width modulation DPWM block. The DPWM block can be modelled as a cascade connection of two blocks: the first block been the modulator static gain and the second block is the Padè approximation PWM module. The sampling process by the on-chip ADC and the PWM module together form a sample and hold device and can be represented with zero order hold (ZOH) [131, 132]. The s domain transfer function of ZOH can be expressed as

$$ZOH = \frac{1}{s}(1 - e^{-sT_s}) \tag{6.16}$$

Here the modulator gain is represented with unity gain, since in digital implementation; the modulator transfer function is represented by a numerical scale factor that converts the digital

controller binary code $m(k)$ to the corresponding duty cycle $d(t)$. $m(k)$ is usually coded such that its maximum binary value equal to one. This means that the modulator gain is also unity and $m(k)$ directly represents the duty cycle without scale factor [132]. This further explained that a full-scale input value of the ADC is also unity. Under these assumptions, the static gain of DPWM is equal to unity and the sample and hold effect of single update triangular carrier PWM can be modelled by assuming $C_{PK} = 1$ (where C_{PK} represent the peak value of the triangular carrier modulation signal). The inclusion of the Padè approximation block is to account for the response delay of the modulator between the ADC sampling instant and subsequent duty cycle update. The response delay of the DPWM is on average considered to be half of the modulation period duration and therefore modelled with its first order padè approximation. The next block represents the control to input current transfer function $G_{iLd}(s)$, which relates the variation of the converter input current I_{in} to the consequent variation of the duty cycle d. This relation is derived from (6.13) by setting $\hat{v}_{in}(s) = 0$ and found to be

$$G_{id}(s) = \frac{\hat{\imath}_{in}(s)}{\hat{d}(s)} = 2 \cdot \frac{\hat{\imath}_{Lm}(s)}{\hat{d}(s)} = \frac{q_1 s^2 + q_2 s + q_3}{p_1 s^3 + p_2 s^2 + p_3 s + p_4} \tag{6.17}$$

Where

$$q_1 = b_1 \cdot s^2 + \left(\frac{1}{R_O C_O} + \frac{(N+1)(1-D)^2}{2 f_s L_K C_c} + \frac{2 I_{Lm}(1-D+D')}{(N+1)V_o}\right) \cdot b_2\, s + \frac{(N+1)(1-D)^2 \cdot b_3}{2 f_s L_K C_c}\left(\frac{1}{R_O C_O} + \frac{2 I_{Lm}(1-D+D')}{(N+1)V_o}\right) + \frac{2 I_{Lm}(1-D)^3}{4 f_s L_k C_c C_o V_o} \cdot b_3$$

$$q_2 = -2(1-D) Co \cdot b_1 - 2(1-d)\left(\frac{1}{R_O} + \frac{2 I_{Lm}(1-D+D')}{(N+1)V_o}\right) \cdot b_2$$

$$q_3 = -\frac{(1-D)^3}{(N+1) f_s L_K} \cdot b_3$$

Using the block diagram of Figure 6.7, the design of the PI controller is straightforward. However, the loop gain of the block diagram is required, which is simply a cascade connection of all blocks given by

$$G_{oL}(s) = \frac{K_p(s + K_i/K_p)}{s} \cdot \frac{(1 - s\,T_s/4)}{(1 + s\,T_s/4)} \cdot H_i(s) \cdot G_{id}(s) \tag{6.18}$$

Now, the continuous time system in (6.17) is first discretized with ZOH given by

$$G_{id}(z) = Z\{\frac{1}{s}(1 - e^{-sTs}) H(s) \cdot G_{id}(s)\} \tag{6.19}$$

Once this is available, the digital PI controller is designed directly in the discrete time domain using methods similar to continuous time frequency response. The compensator design is driven by certain specifications concerning the closed loop performance (such as speed of response or tracking error with respect to the reference signal). These specifications are usually turned into equivalent closed loop specifications of bandwidth and phase margin. To ensure enough stability around equilibrium point due to parameter variation influence, a gain margin of 45^{o} or higher at gain cross over frequency would be desirable. For this reason, a closed loop bandwidth f_{CL} of one tenth of the switching frequency f_s is intended to be achieved with at least phase margin PM of 60^{o}. The subsequent step is to determine the proportional gain K_p and integral gain K_I that guarantee compliance with these specifications. The controller is designed in Matlab using "sisotool" graphical user interface based on Zeigler-Nichols tuning that allows the closed loop frequency response to be interactively changed by modifying the pole-zero location of the PI compensator. The corresponding feedback compensator gains from the same interface are $K_p = 0.0151$ and $K_I = 0.0025$ respectively. Figure 6.8 illustrate the Bode diagram of the inner current loop, showing compliance with design specifications. The system has a gain margin of 11.2 dB at phase crossover frequency of 157 Krad/sec and a phase margin of 59^{0} at the gain crossover frequency of 29.6 Krad/sec. These margins are sufficient to ensure stability against variation in set point values around the equilibrium point.

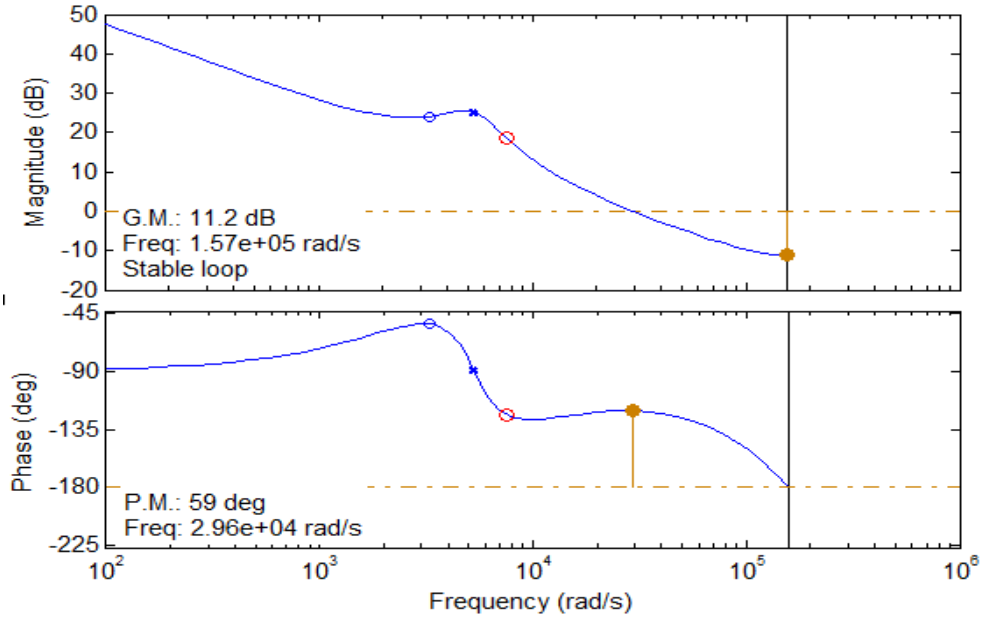

Figure 6.8 Bode Diagram of current control loop with discrete PI controller

For the controller just designed, the modulator delay represented by the Padè approximation block is assumed to be negligible and therefore neglected. However, this is not the case in digital implementation. To properly characterize the model a digital PWM delay, which on average equals to half of the modulation period delay is considered. The plant transfer function $G_{id}(z)$ is recalculated to reflect this delay. The plant transfer function is given by

$$G_{id}(z) = Z\{\frac{1}{s}(1 - e^{-sTs})H(s) \cdot e^{-sTd} \cdot G_{id}(s)\} \tag{6.20}$$

Where $T_d = 0.5\,T_S$. Figure 6.9 shows the corresponding digital PWM delay effect on the controller. It is apparent that the delay in ADC sampling instant and subsequent duty ratio update results in a reduced PM of 16.3^o at the gain crossover frequency of 28.5 Krad/sec and reduced gain margin of 0.7 dB at phase crossover frequency of 74.6 Krad/sec for the latter system with the same controller.

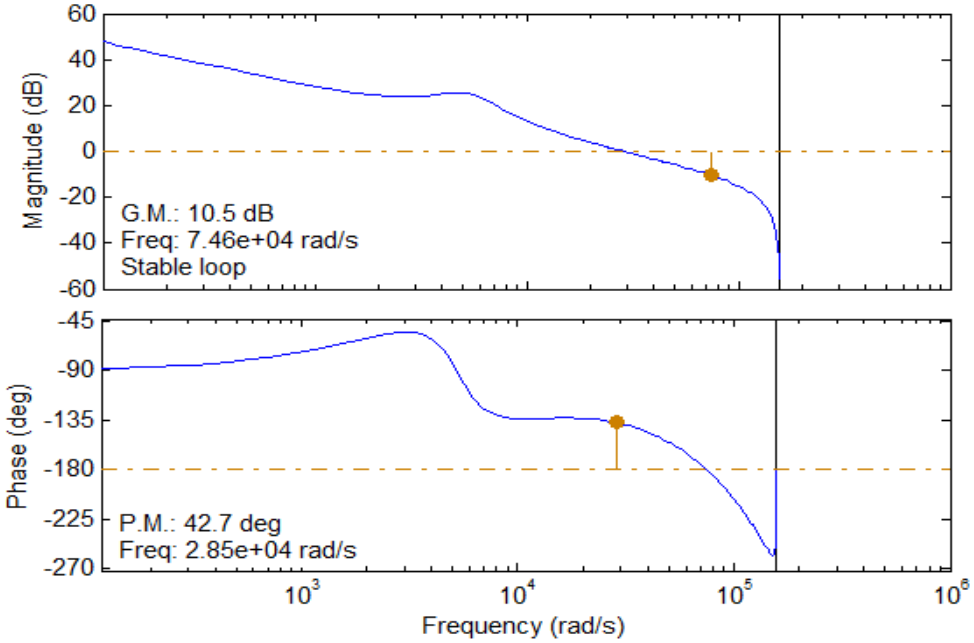

Figure 6.9 Digital PWM delay effect

The reduction in phase margin is as a result of time delay which is on average half of the modulation period associated with the DPWM block. The time delay amount to a phase lags in the system given by

$$\angle G_{oL} = 360 \cdot f \cdot T_S/2 = 16.3^0 \tag{6.21}$$

Where $f = 74.6$ Krad/sec is the frequency at which the phase lag is calculated. Despite this delay, it is clear that the system is stable and has sufficient margins to ensure stability around equilibrium point due to parameter variation influence.

6.4.2 Outer Voltage Control Loop

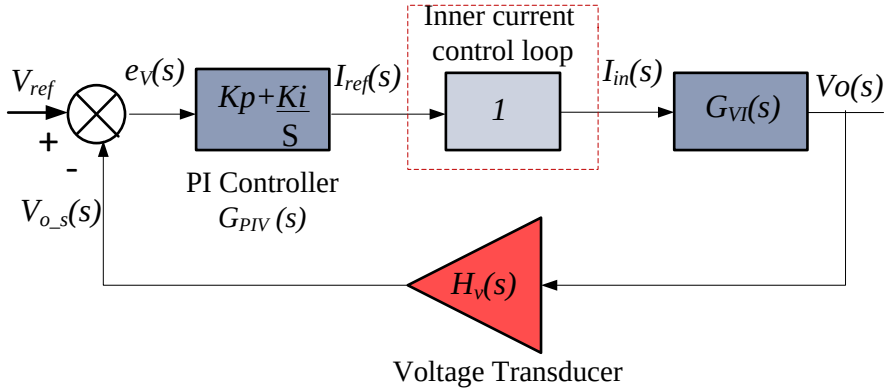

Figure 6.10 Block diagram of voltage control loop in continuous domain

Figure 6.10 shows the block diagram of the voltage control loop; all the components were represented with their respective transfer functions. The control objective of the outer loop is to set the current reference for the inner current loop. Similar to inner current loop, a PI compensator is employed to maximize the compensator bandwidth and slow outer loop dynamics. However, any compensator with integral part acting on the voltage error can as well be utilised. The voltage loop PI controller, whose proportional gain K_p and integral gain K_I is determined in this section, processes the error between the actual and desired output voltage. The controller output produces a current that serve as a reference for the inner current loop.

Note that the inner current control loop has been replaced by a unit gain. This replacement is influenced by the fact that the inner current control loop has a much faster dynamic response than the voltage loop [99, 131]. $G_{vi}(s)$ is the output to input current transfer function relating the output voltage variation due to consequent variation of input current derived from (6.13). This transfer function is given by

$$G_{vi}(s) = \frac{\hat{v}_o(s)}{\hat{I}_{in}(s)} = \frac{\hat{v}_o(s)}{\hat{d}(s)} \cdot \frac{\hat{d}(s)}{\hat{I}_{in}(s)} = \frac{a_1 s^2 + a_2 s + a_3}{q_1 s^2 + q_2 s + q_3} \tag{6.22}$$

Where $a_1 = L_m C_c b_1$

$$a_2 = \frac{(1 - D + d')C_c}{2(N+1)} \cdot b_1 + \frac{2I_{Lm}L_m(1-D)}{V_o} \cdot b_2 + \frac{(1-D)^2 L_m}{f_s L_K} \cdot b_3$$

$$a_3 = (1-D)^2 \left(\frac{(1 - D + D')}{2 f_s L_K} + \frac{2I_{Lm}(1-D)}{V_o} \right) \cdot b_1 - \frac{2(1 - D + D')(1-D)}{(N+1)} \cdot b_2 + 2(1-D)^2 \cdot b_3$$

$$q_1 = b_1 \cdot s^2 + \left(\frac{1}{R_O C_O} + \frac{(N+1)(1-D)^2}{2 f_s L_K C_c} + \frac{2 I_{Lm}(1-D+D')}{(N+1)V_o}\right) \cdot b_2\, s + \frac{(N+1)(1-D)^2 \cdot b_3}{2 f_s L_K C_c}\left(\frac{1}{R_O C_O} + \frac{2 I_{Lm}(1-D+D')}{(N+1)V_o}\right) + \frac{2 I_{Lm}(1-D)^3}{4 f_s L_k C_c C_o V_o} \cdot b_3$$

$$q_2 = -2(1-D)Co \cdot b_1 - 2(1-d)\left(\frac{1}{R_O} + \frac{2 I_{Lm}(1-D+D')}{(N+1)V_o}\right) \cdot b_2$$

$$q_3 = -\frac{(1-D)^3}{(N+1) f_s L_K} \cdot b_3$$

The PI controller gains can be determined from the open loop gain of Figure 6.10, which is simply a cascade connection of all the blocks given by

$$G_{oL}(s) = \frac{K_p(s + K_i/K_p)}{s} \cdot H_v(s) \cdot G_{vi}(s) \tag{6.23}$$

$H_V(s)$ is the voltage transducer gain and $G_{vi}(s)$ is the output to input current transfer function. Equation (6.23) is first discretised and the compensator design of the outer loop is equally influenced by certain specifications concerning the closed loop performance (such as speed of response). However, the cut-off frequency of the outer voltage loop should be much smaller than the inner current loop to consider the latter as having unity gain and zero phase when designing the former [99, 131]. To ensure sufficient stability around equilibrium point due to parameter variation influence, a closed loop bandwidth f_{CL} of one tenth of the inner current loop is intended to be achieved with at least phase margin PM of 60^o.

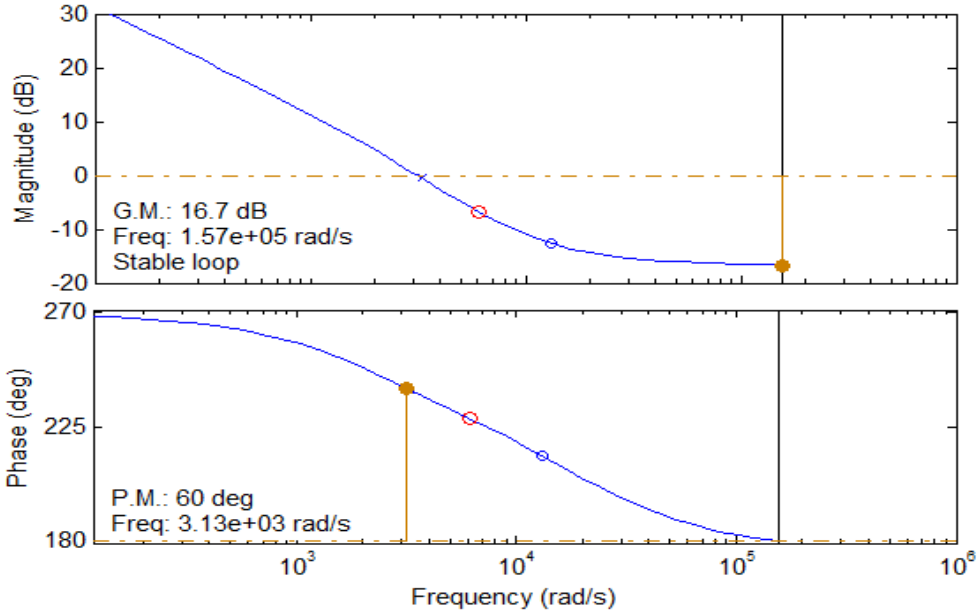

Figure 6.11 Bode plot of the voltage control loop with discrete PI controller

Following the same method described in the current loop the proportional gain K_p and integral gain K_I of the voltage loop that guarantees compliance with these specifications are $K_p = 0.1987$ and $K_I = 0.0258$ respectively. Figure 6.11 shows the Bode plot of the voltage control loop with the discrete controller. The desired specifications of phase and gain margins were achieved and the low-frequency gain is improved.

6.1 Simulation and Experimental Results

The dynamic performance of the closed loop system is verified by computer simulation based on the foregoing analysis. Figure 6.12 illustrates the step change in load resistance from full load to twenty percent load (i.e. 500W to 100W) and vice versa. The peak overshoot is 20% of the steady state output voltage and the settling time is 30ms.

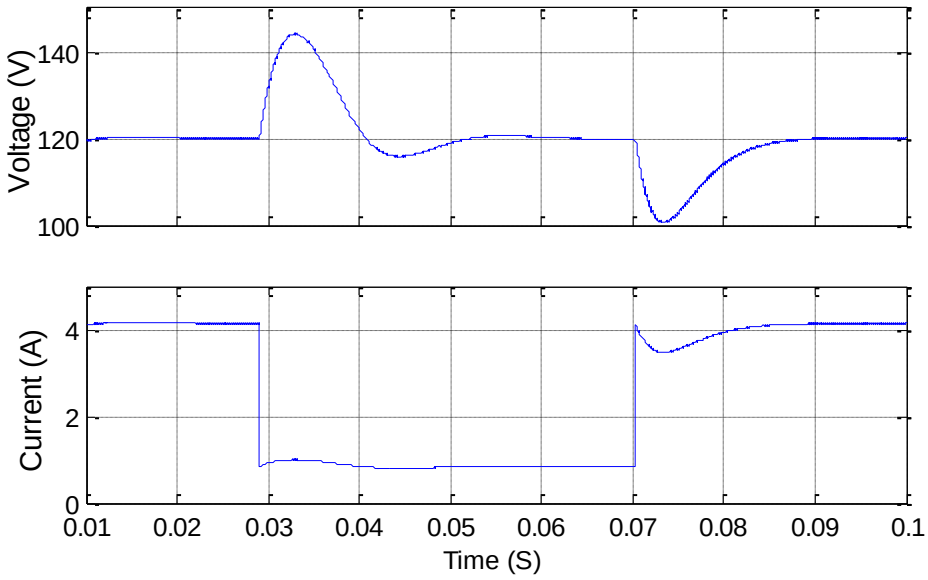

Figure 6.12 Simulated response to load changes from 500W to 100 W

The dynamic response of the controller is further verified experimentally with 500 W prototype shown in Figure 5.10. The nominal operating points of the converter are listed in Table 5.1. Refer to Appendix A, for more details on the hardware used for testing the control algorithm and the experimental set-up. The control routines were implemented with a TMS320F28335 Texas Instruments Microcontroller. The Microcontroller has a sufficient processing capacity to perform the control routines and provide six pairs of PWM signals with proper phase. Comprehensive description of the control hardware popularly known as digital signal processor DSP board is provided in Appendix B. The gate drives and interface board specifically designed for isolation and generating appropriate gate signals required by the

power switches can be found in Appendix D. When performing the laboratory experiments, the controller gains were further tuned to obtain the desired response with minimal overshoot. However, the calculated values were taken as starting point.

Figure 6.13 shows a time domain dynamic performance of the converter. Here, a step change in load resistance is applied, causing a step increment/decrement in output power from 100 W to 500 W. The results clearly show the performance of the current mode controller in terms of settling time and overshoot. The converter output voltage settles within $20\ ms$. There is an overshoot and undershoot on the voltage waveform during load changes. The output voltage variation (undershoots) and overshoots are approximately 5 V (4.1%) of the steady state value. The waveforms clearly indicate that despite the change in load the output voltage is well regulated with no steady state error.

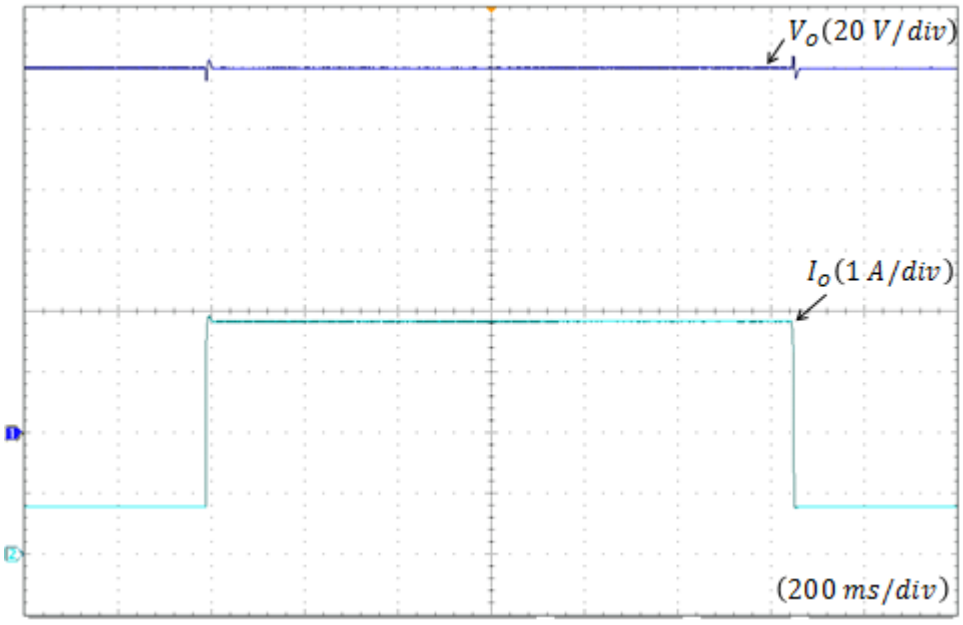

Figure 6.13 Experimental response to step change from light load $P_O = 100\ W$ and full load

Additional load disturbance compensation performance of the converter in both simulation and experiment are further carried out. Figure 6.14 illustrates the transient and steady state response of the system when a step change in load resistance is applied causing an increment in output power from half load to 400 W. Unlike the previous case, the output response settle faster within 15ms and the overshoot/undershoot reduces to 6.6% of the steady state values.

Figure 6.15 shows the experimental closed loop performance of the converter when subjected to a step change in load resistance from 250 W to 400 W and vice versa, the converter settles within $15\ ms$. The output voltage variation (undershoots and overshoot) is approximately 4

V (3.3%) of the steady state response and the output voltage is well regulated with no steady state error. Further tuning of the controller gain in the experiment, results in sharp reduction in the peak overshoot/undershoot and the output response settle faster.

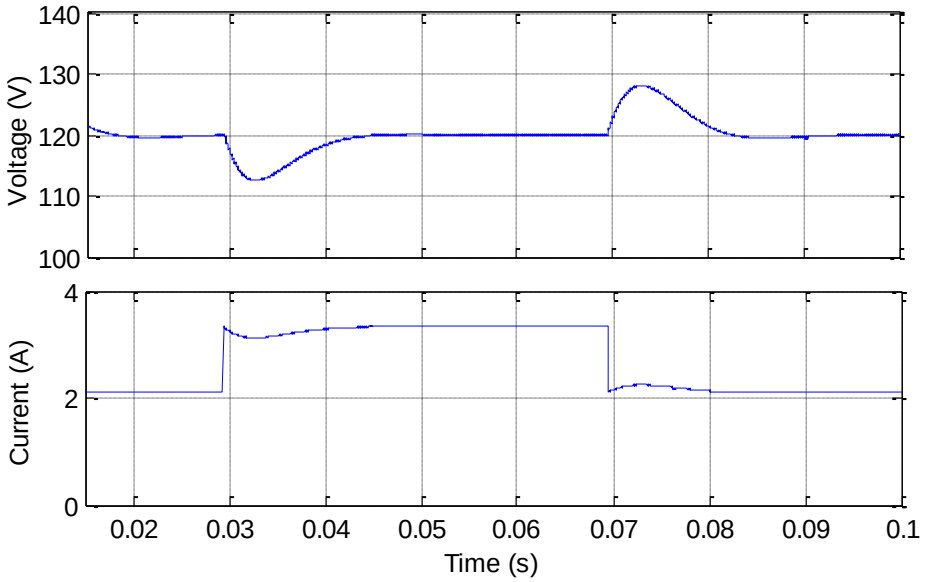

Figure 6.14 Simulated response to load changes from 250W to 400 W

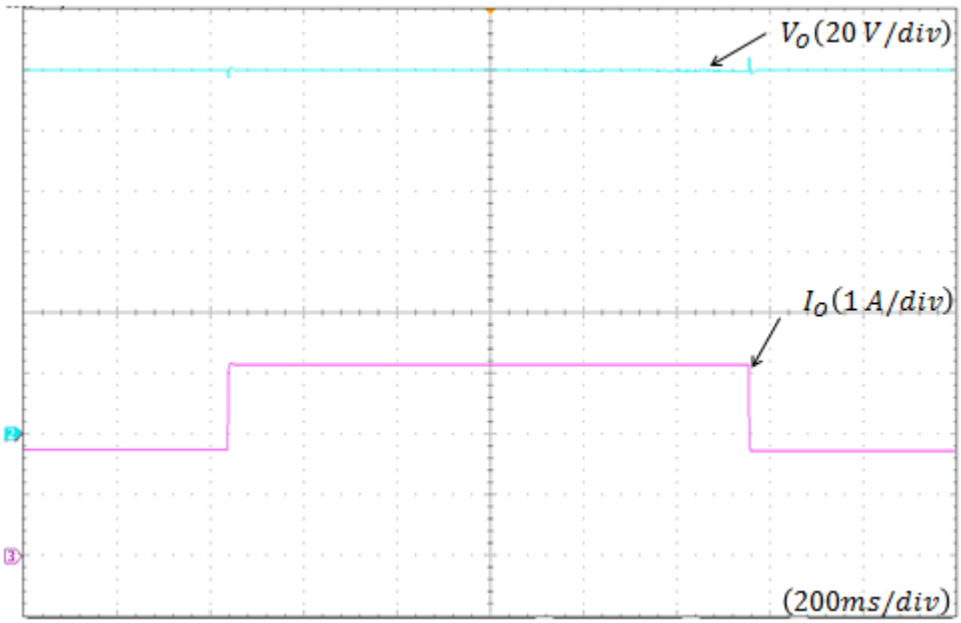

Figure 6.15 Experimental response of load variation between $P_O = 250\,W$ and $P_O = 400\,W$

6.2 Manual Tuning of Discrete PI Controller

This section describes a manual controller tuning method, in particular the digital PI controller implemented on the high step-up converter. The basic principle is to act upon a plant to be controlled in this case (DC-DC converter) through a combination of two elements:

Proportional part: this produces an actuating signal proportional to the error signal. Proportional part reduces the rise time and the steady state error but cannot eliminate it.

Integral part: this produces an actuating signal proportional to integral of the error signal. The integral part eliminates the steady state error. However, it makes the transient response worse.

It is possible to apply various design techniques or tuning algorithms to determine the controller parameters that will satisfy the transient and steady state specification of closed loop system if the mathematical model of the system is known or can be derived. However, if the mathematical model cannot be easily derived, then application of analytical or computational method to the design of the PI controller is impossible. Therefore, it becomes necessary to resort to manual approach of tuning the PI controller.

The process of selecting the controller parameters to satisfy given performance specification is known as controller tuning. The most widely understood method of controller tuning is Zeigler-Nichols method, which is based on the proportional gain K_P that result in marginal stability when only proportional control action is used. The method is useful in selecting the controller parameters when the mathematical model is not known. Likewise, the rules can also be applied to the systems with known mathematical models. The Zeigler-Nichols tuning rules provide an educational guess for the controller parameters and provide a starting point for the tuning, rather than the final setting for the parameters in a single shot.

The method involves setting the integral control action to zero, using only the proportional control action. The proportion gain is slightly increased from zero to a critical value K_C at which the output exhibits sustained oscillation. Zeigler and Nichols suggested that the controller parameters K_P and K_I are now set according to the formula shown in Table 6.1.

Table 6.1 Manual Tuning of PI controller based on Zeigler-Nichols method

Control Type	**Proportional Part** K_P	**Integral Part** K_I
Proportional Integral (PI)	$0.45K_C$	$P_C/1.2$

Where P_C is the period of sustained oscillation. The manual tuning method relies on the person tuning the controller to make several judgements throughout the tuning process. Algorithmic tuning methods exist which aim to minimize this decision making process, thereby making it easier to tune the controller without the need to reach the critical value K_C.

6.3 Summary

The derivation of the small signal model of a high step-up interleaved boost converter using state space averaging is described in this chapter. The model is used in the design of the dual loop current mode controller. A complete step by step design procedure is presented. The similarity of the converter components and symmetry of the operation were explored to simplify and reduce the complexity of the model. Experimental results for step change in load at fixed input voltage are presented. The designed controller show good performance for variations in input voltage and load conditions. The results clearly show that the desired output voltage is well regulated, with zero steady state error. Likewise, at the point of a load change, the transient characteristics are well within acceptable limits. The frequency response and domain plots of the digitally controlled high step-up interleaved converter demonstrate the validity of the MATLAB based design approach.

Chapter 7
Conclusion and Further Work

7.1 Introduction

It is likely that significant amount of global future energy requirement could come from RESs; such as solar photovoltaic and ESS such as Li-ion batteries. From this viewpoint, research and development in alternative energy sources has been given utmost importance. This is related to the fact that these RESs and ESS are among the cleanest methods of generating and storing energy. However, the growing use of RESs and ESS brings other challenges to the energy conversion technology; because devices that store or produce electrical energy are often realized using multiple low voltage storage cells, which are usually connected in series to produce sufficient voltages for the intended applications. These challenges make RESs very expensive and inhibit their widespread application. Literature studies have revealed that the major areas of research in energy conversion are improvement of the system efficiency and lowering the system cost. A target area of reducing the power system cost is to eliminate, combine or simplify as many conversion steps as possible. Therefore, the aim of the research in this thesis is to contribute towards lowering the cost, raising the conversion ratio and improving the efficiency of high step-up converter system. Four areas have been highlighted where performance improvements can be made which include:

i) Avoiding extreme duty ratio operation,
ii) Minimizing the voltage or current stress imposed on power semiconductors,
iii) Lowering the current falling rate of the diodes
iv) Soft switching performance.

A single phase and interleaved high step-up boost converter has been proposed to address the above issues. The proposed innovative solutions have achieved significant performance improvements and higher conversion ratio over the state of the art topologies.

Firstly, higher conversion ratio is realised in all the proposed converter topologies by integrating coupled inductor and switched capacitor to configure a voltage gain extension cell. This integration permits achieving higher voltage gain with lower turns ratio, thus reducing the volume and copper loss associated with the coupled inductor. Furthermore, the coupled inductor turns ratio provides another degree of freedom to enlarge the converter static gain in conjunction with the duty ratio. The extreme duty ratio operation is simply avoided by proper choice of coupled inductor transformation ratio. In addition, the voltage stresses imposed on power devices are minimized. As a result, low voltage rated power devices with low on-state resistance are employed to reduce the conduction loss; leading to improved efficiency.

Secondly, the turn-off voltage spike seen by the primary switch due to leakage inductance energy traditionally requires a snubber. Literature shows that the active and passive clamp circuits are the most widely employed approach for recycling the transformer leakage energy in a transformer based DC-DC converters. However, a true performance evaluation of the clamp circuits when applied to the same power converter is rarely discussed. This thesis presents the theoretical analysis and clamp schemes performance comparison on the proposed high step-up DC-DC converter. The experimental results, obtained via two prototype circuits, validate both the theory and operational characteristics of each power converter. It is shown that the active clamp converter has the advantage of achieving (ZVS) of all the active switches and achieves 1% higher efficiency than its passive clamp counterpart. On the other hand, the passive clamp converter offers low cost, simple structure, low level of circulating current and higher reliability; thus increasing the lifetime of the converter. Importantly, unlike many power converters presented in literature, both of the proposed topologies in this thesis exhibit low devices voltage stress. The diodes voltage stress is significantly less than the converter output voltage and the low-voltage diodes typically recover faster. The diodes turn off softly with (ZCS) by utilizing the inherent leakage inductance of the coupled inductor to control their current falling rate.

Interleaving is usually adopted as an effective solution in high power applications to reduce the passive component size, increase the power level, minimize the current ripple, improve the transient response, and realize thermal distribution. In this work, a new (ZVS) interleaved, non-isolated, high step-up DC-DC boost converter with active clamping circuit is proposed. The converter uses two coupled inductors in both forward and flyback mode and a switched capacitor to achieve high conversion ratio. Interleaving is adopted on the primary side to share the input current and cancel the current ripple of the coupled inductors and increase the power

level. The secondary windings of the coupled inductor are connected in series to achieve winding coupled configuration and sustain the high voltage at the output. Importantly, unity turns ratio is utilised to achieve ten times (10X) voltage gain; which reduces the copper loss and leakage inductance of the coupled inductor. Furthermore, the voltage stress of the active switches and diodes are reduced. By adopting active clamping, (ZVS) is achieved for all the switches. The diode reverse recovery problem is alleviated for all the diodes, hence switching losses are further reduced yielding an efficient green power supply solution.

In many DC-DC boost converters, deriving a state space average model of the system is a key step towards predicting the (RHP) zero and consequent design of feedback control system having wide bandwidth and adequate (PM). The derived model must be able to respond to the characteristic of the system. In this work, a fifth-order state space average model of the high step-up interleaved boost converter is derived. A reduced third-order model is later developed from the fifth-order to represents a dynamics model of the current in one phase, voltage on one of the clamping capacitors and the output voltage. This is achieved with the assumption that the other phase of the converter behaves symmetrically. In addition to the symmetry of the phases, the coupled inductors and the clamping capacitors in each phase are considered to be the same. Hence the duty cycle is assumed to be the same in the converter primary switches. A Matlab simulation is used to validate the models; the switching model and the averaged model show a good agreement. After linearizing the model, the control-to-output transfer function is once again verified in simulation using Matlab system identification method. The control-to-output transfer function estimated from the measured data after perturbing duty cycle set point with sinusoids of different frequencies, agrees closely with the calculated control-to-output transfer function. A dual loop controller is designed based on the derived power stage model to control the power flow.

Each concept have been analysed designed and tested by constructing appropriate hardware. The experimental results obtained are presented in this thesis. In this chapter, a conclusion of the work carried out so far is presented and relevant areas that require further investigation are described.

7.2 Single Phase High Step-up Converter

Utilising a coupled inductor is a simple solution of avoiding extreme PWM ratio in high step-up converters. However, the leakage inductance of the coupled inductor induces high voltages

stress to the power switch and traditionally requires a snubber. The use of RCD snubbers can reduce the voltage stress, but the recovered leakage inductance is dissipated as heat within the snubber. The limitation of RCD snubbers is largely overcome by either active clamp circuit or passive clamp. The clamp circuits have been explored with the benefit of recycling the leakage inductance energy of the coupled inductor whilst minimising the turn- off voltage spike of the power switch. In this thesis, the non-isolated coupled inductor with active clamping is first introduced. The active clamp circuit is then replaced with the passive clamp consisting of only a diode and clamp capacitor. The passive clamp circuit achieves a level of operation similar to the active clamp circuit.

Theoretical analysis and clamp circuits performance comparison of a new set of high step-up DC-DC boost converters are presented in this thesis. The experimental results, obtained via two prototype circuits, validate both the theory and operational characteristics of each power converter. It is shown that the active clamp converter has the advantage of achieving (ZVS) of all the active switches and achieves 1% higher efficiency than its passive clamp counterpart. On the other hand, the passive clamp converter offers low cost, simple structure, low level of circulating current and higher reliability; thus increasing the lifetime of the converter. Importantly, unlike many of power converters presented in literature, both of the proposed topologies in this thesis exhibit low devices voltage stress. The diodes voltage stress is significantly less than the converter output voltage and the low-voltage rated diodes typically recover faster. The diodes turn off softly with (ZCS) by utilizing the inherent leakage inductance of the coupled inductor to control their current falling rate.

7.3 Interleaved High Step-up Converter

In high step-up interleaved boost converter system, each converter phase is synchronised to the common input voltage source. Consequently, reducing the large current ripple produced by each converter due to coupled inductor operation. The phase shift between the interleaved converter phases is straight forward to implement in software and does not in any way affect the processor execution time. Increasing the number of phases, provides more opportunity for input current ripples reduction. However, it is also reasonable to predict that a point is reached whereby employing the multiple phases in interleaved form can no longer reduce the current ripple in the system. Further study would be required to investigate the limit of increasing the converter phases and extent of the benefit of reducing the current ripple.

The addition of phases in an interleaved form does not in any way increase the static gain of a converter rather than sharing the input current and increasing the power level. Interleaving provides a mechanism of minimizing the input current ripple; improve thermal distribution and reduces the passive component size.

In a single phase high step-up converter system, there is no opportunity for current ripple minimization. Any attempt to push the power level further amounts to relatively high current stress incurred by the switching device (a major detriment of increasing the power density). The winding couple configuration of the secondary side permits achieving ten times (10X) voltage gain even with a unity turns ratio. Unlike the single phase converter and many interleaved converters which require some transformation ratio to realise similar voltage gain.

The coupled inductor of the interleaved high step-up converter serves a dual purpose, energy storage and means of enlarging the voltage gain. The primary windings behave like a conventional inductor at the input and therefore, serve as a constant current source. Theoretically, reduces the number of magnetic component in the converter. The (ZVS) performance of the entire active switches, as well as reverse recovery alleviation of the output diodes, depends on the leakage inductance. Meaning that, the leakage inductance should be design carefully, since higher leakage inductance value degrades the conversion efficiency. It is also worth mentioning that careful attention to the design of the coupling inductor is key to achieving optimum circuit performance; higher efficiency and excellent coupling between the windings is essential to reduce the duty cycle loss cause by the leakage inductance which degrade the efficiency.

7.4 Further Work

Literature shows that many works have been carried out in identifying suitable, often novel high step-up converters topologies covering a broad range of applications with improved efficiency. However, further investigation is required in high power density, high step-up DC-DC converters. The future trend is high power density low cost and low profile power electronic converters. The development of miniaturised converter provides the possibility of pushing further the switching frequency to increase the power density. Increasing the switching frequency makes the passive components smaller, but the limit of the switching frequency and extent of the benefits needs further investigation. Increasing the switching frequency exacerbate the switching loss. Another thought is magnetic element integration

could, of course, produce a compact converter. Further study of the coupled inductor interleaved power converters and performance improvement via design optimisation, as well as comparison with the current state of the art topologies, would be an interesting research topic.

Literatures have further revealed that current state of the art topologies for high step-up applications employ capacitor charge transference or magnetic elements. Nevertheless, integrating capacitive and magnetic means mainly for voltage gain is another popular method. However, further research on gain extension cells could lead to new topologies with the potential of improving the efficiency.

The control structure of the proposed converters utilises a classical current mode PI controller and has a smooth regulation. But for all other applications, a certain control scheme needs to be developed and investigated. For example, in particular, battery charging application requires the controller to switch at one point from a voltage controlled to the current controlled mode depending on the state of the charge (SOC) of the battery. In essence, the transition between current mode to voltage mode battery charging and mode transition between voltage mode battery charging and battery voltage discharging.

The traditional averaging method has been used in this thesis to obtain information about the stability of the high step-up interleaved boost converter and its dynamic behaviour. However, literature has shown that averaging method itself is accurate up to about one tenth of switching frequency. Furthermore, whilst the averaging technique can capture the instabilities that occur on a slow time scale, it did not account for all phenomena that occur at switching frequency. At switching frequency, the fast scale instabilities that may develop in the converter waveforms can lead to subharmonic oscillation and chaos. Further study of analysing and prediction of such instabilities would be another interesting research topic.

Appendix A

Simulink Model of the Proposed High Step-up Converters

A.1 Introduction

This section presents the closed loop Matlab/Simulink model used in simulating the behaviour of the proposed high step-up DC-DC converters (single phase and interleaved).

A.2 Single Phase Active Clamp Converter Simulink Model

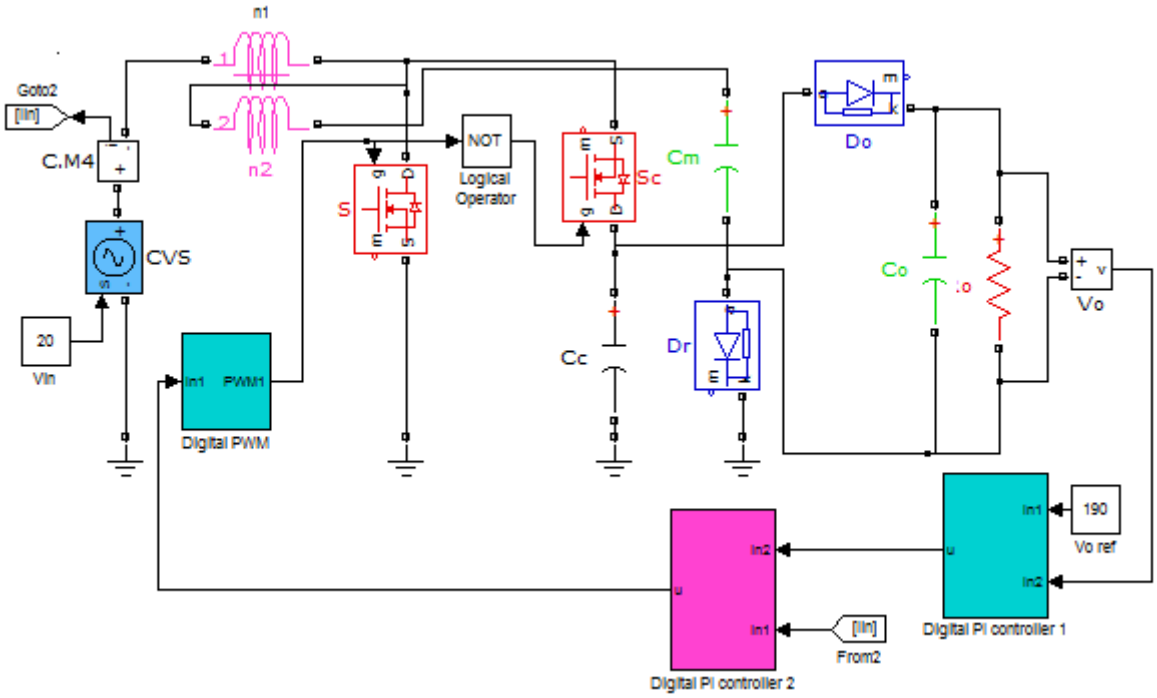

Figure A.1 Simulink model of the single phase active clamp converter

Figure A.1 shows the Matlab\Simulink model of the proposed single phase active clamp converter (ACC). It comprises a dc source V_{in}, primary switch S, voltage gain extension cell and a dc output voltage V_O. In this circuit, the coupled inductor serves dual purpose, energy storage and means of enlarging the voltage gain. The primary winding serves as a filter inductor (similar to a conventional boost converter) and is coupled to the corresponding

secondary winding. The number of turns in the primary and secondary windings of the coupled inductor is represented by n_1 *and* n_2 respectively. S is the converter primary switch. The (ACC) comprise of clamping switch S_C and a clamp capacitor C_C. The voltage extension cell consists of the coupled inductor secondary winding n_2, the (ACC), regenerative diode D_r and the switched capacitor C_m. D_O is the output diode, C_O is the filter capacitor and R_O is the resistive load.

A.3 Single Phase Passive Clamp Converter Simulink Model

Figure A.2 illustrate the Matlab\Simulink model of the proposed single phase passive clamp converter (ACC). The only difference in the circuits is substitution of the clamp switch S_C with a clamp diode D_C.

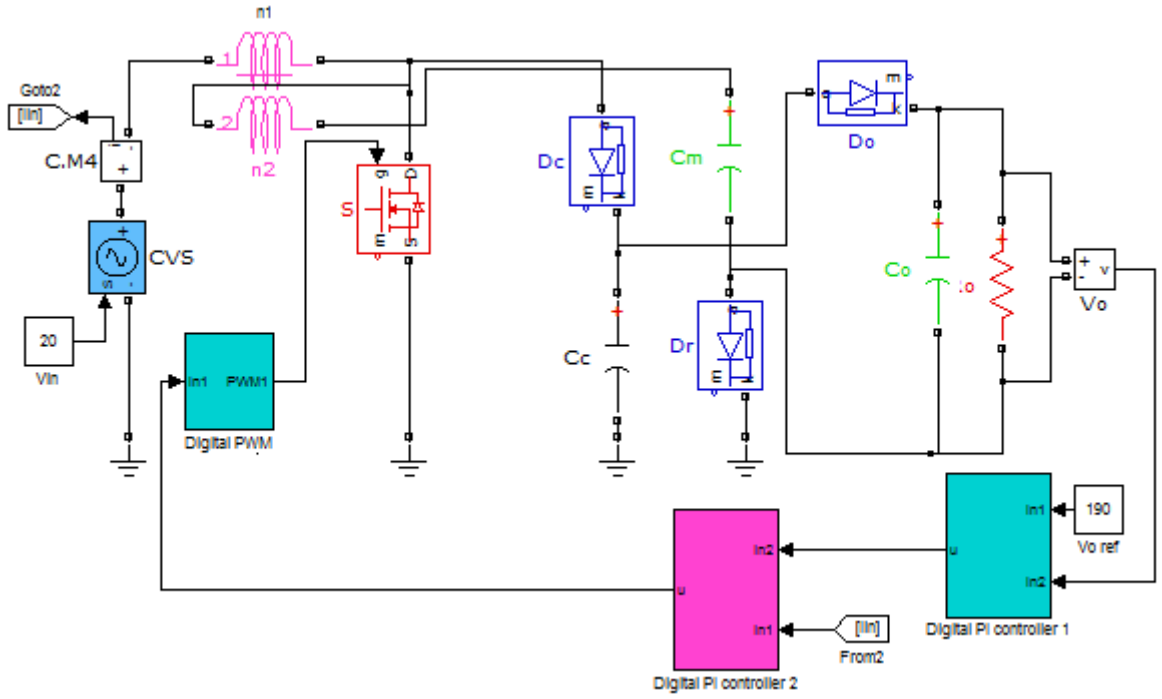

Figure A.2 Simulink model of the single phase passive clamp converter

A.4 Interleaved Active Clamp Converter Simulink Model

Figure A.3 shows the Matlab/Simulink structure of the proposed interleaved high step-up converter with coupled inductors and voltage multiplier cell. The converter employs two coupled inductors ($L_1$and L_2) with the same number of turns in the primary and secondary sides. The primary winding of the coupled inductor $L_{1a}$and L_{2a} serve as filter inductors like a

conventional interleaved boost converter and are coupled to their corresponding secondary windings L_{1b} and L_{2b}. The primary and secondary windings are denoted by n_1 and n_2, and the coupling references denoted by ''o'' and ''*''. The primary windings are in parallel to handle the large input current on the low voltage side. The secondary windings are in series on the high voltage side to achieve winding coupled configuration and enlarge the voltage gain. There are two sets of active clamp circuits, with S_{C1} and S_{C2} as the corresponding clamp switches. The voltage multiplier cell comprises of secondary windings of the coupled inductor L_{2a} and L_{2b}, the output and regenerative diodes D_O and D_r and the switched capacitor C_m.

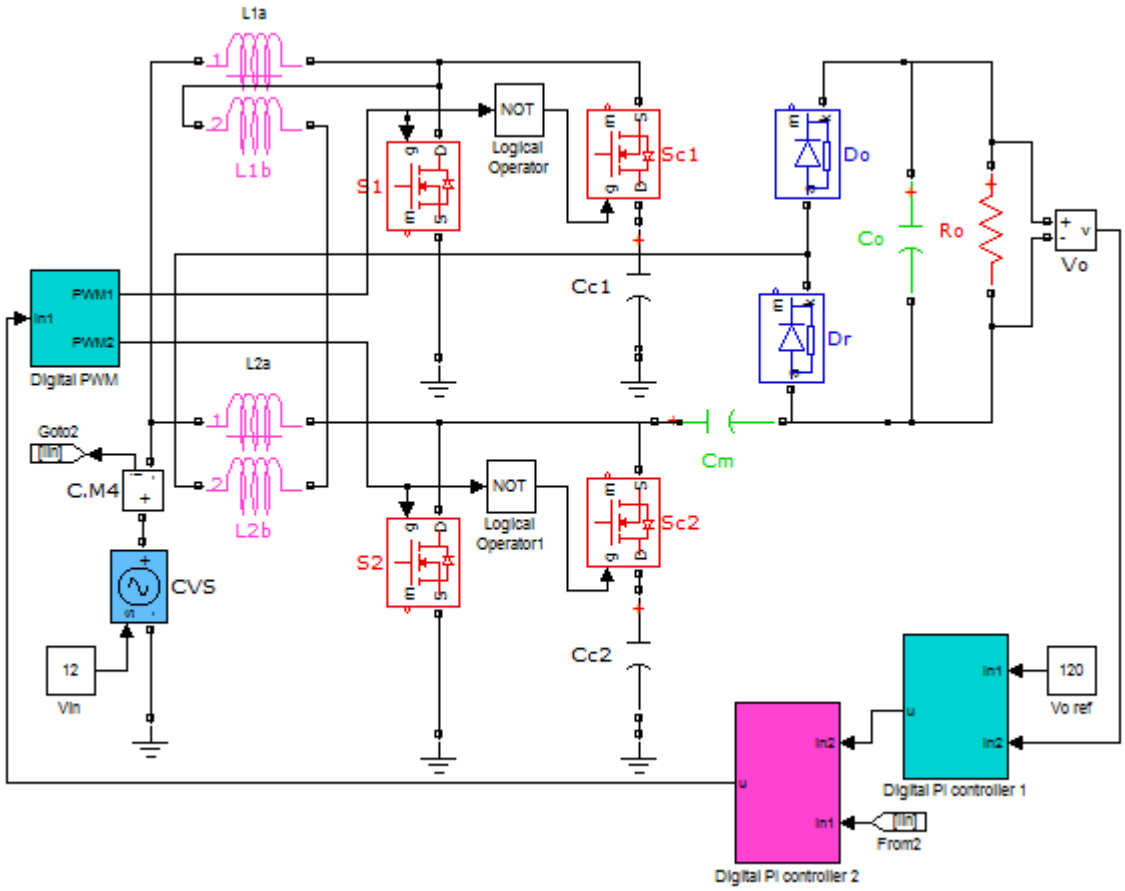

Figure A.3 Simulink model of the proposed high step-up interleaved converter

The digital PI controller 1 and 2 represent the average current mode control scheme adopted in this work.

Appendix B

High Step-up Converters Hardware

B.1 Introduction

This appendix describes in details the power electronics hardware used in testing the high step-up DC-DC converters (single phase and interleaved) in this thesis.

B.2 Single Phase Active Clamp High Step-up Converter Circuit

Figure B.1 shows the photograph of the single phase high step-up boost converter with active clamp circuit. The converter has been designed and built for the purpose of testing the performance and soft switching technique discussed previously. The converter consist of the coupled inductor, main and clamp switch, clamp capacitor, switched capacitor and output capacitor. The dimension of the power stage board comprising all components excluding the coupled inductor is (120 x 110 x 45) mm.

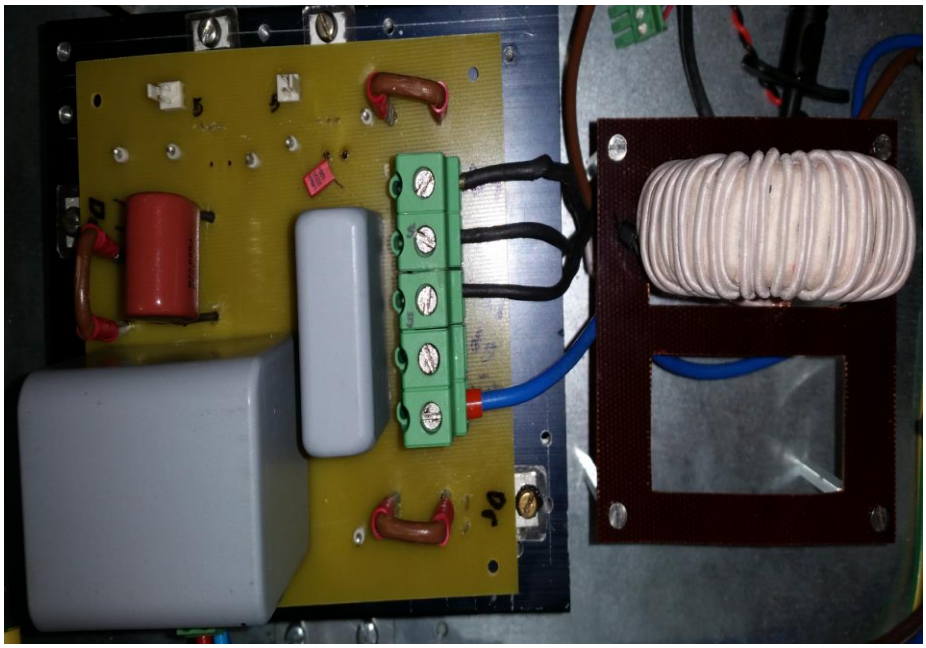

Figure B.1 High step-up converter with active clamp circuit

The coupled inductor is located closed to the main converter board. A toroidal Kool mμ magnetic core 0077110A7 from Magnetics© Inc is selected to assemble the coupled inductor.

The primary winding has 32 turns with one strand of 175/40 litz wire, and the secondary winding has 58 turns with one strand of 100/40 litz wire. The measured magnetizing inductance is 82 µH. The leakage inductance reflected to the primary side is 1.3 µH.

B.3 Single Phase Passive Clamp High Step-up Converter Circuit

In order to evaluate the performance of the passive clamp circuit, new converter hardware is required. The new hardware provides the means of comparing the clamp circuit performance and measuring their efficiencies. For this reason, a single phase high step-up boost converter employing passive clamp circuit has been designed and built in the laboratory. Figure B.2 shows the photograph of the converter. As can be seen from Figure B.1 and Figure B.2 both prototypes are the same. The only difference is the clamp switch is replaced with a clamp diode.

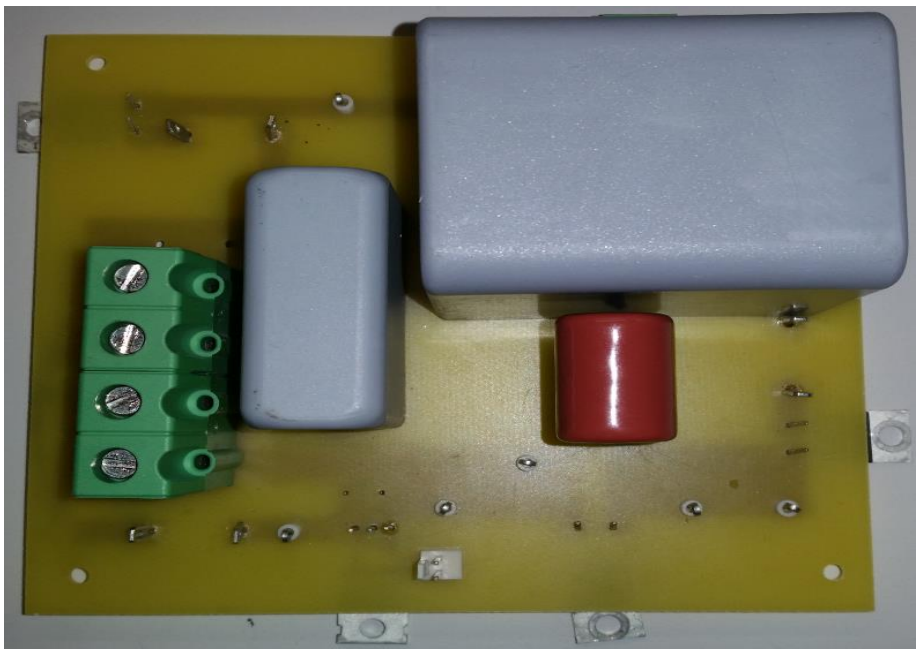

Figure B.2 High step-up converter with passive clamp circuit

B.4 Interleaved Converter

An interleaved converter has been constructed in order to test the concept. The converter is populated on the printed circuit board (PCB) Figure B.3. The coupled inductors and power connections are possible via the PCB terminal connectors as shown Figure B.4. Gate drive signals of each switch are made possible via the 2 way straight PCB header with friction lock.

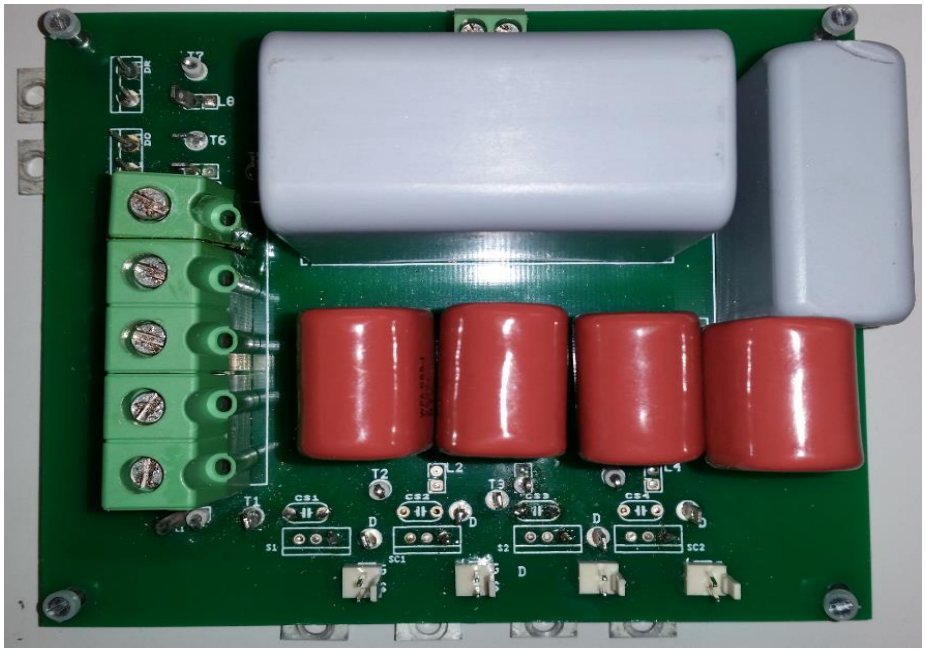

Figure B.3 Interleaved converter photograph

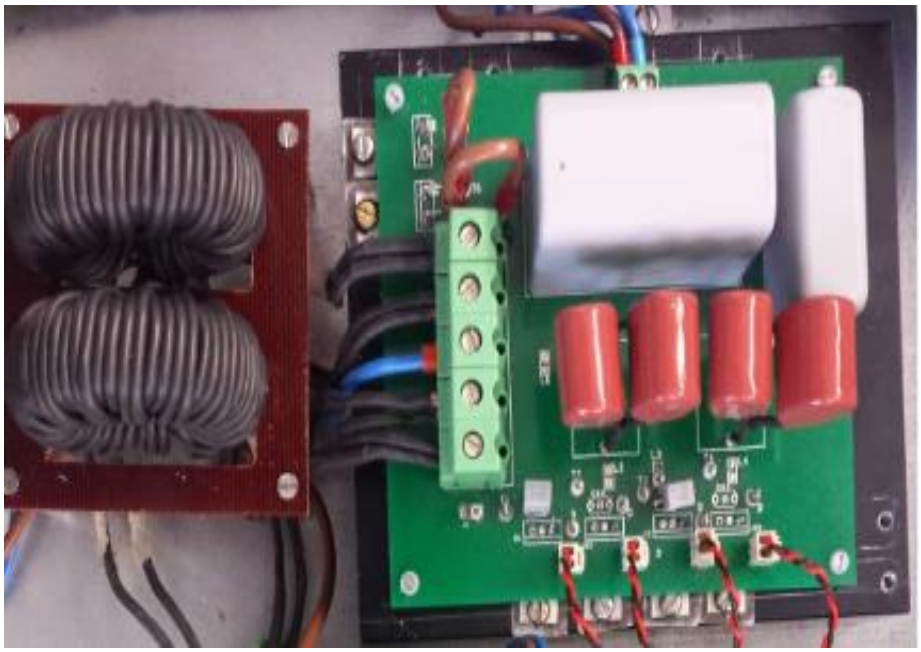

Figure B.4 Complete interleaved converter prototype

Appendix C

Controller Overview

C.1 Introduction

In this appendix a comprehensive description of the control hardware popularly known as digital signal processor (DSP) board is provided. The board is used in all the research work carried out in this thesis.

C.2 Digital Signal Processor (DSP) Board

A power electronics converter traditionally requires PWM signals to operate. The converters are typically controlled by DSP, which is based on electronics/semiconductor chips. The controller used in this is Texas Instrument ® TMS320F28335 (DSC) [133]. The DSP board consist of many parts such as analogue to digital converter (ADC) module with 16 input channels, PWM peripheral comprising six pairs of (ePWM) module [134]. The card has four communication ports which can be configured to allow data transfer between the code composer studio (CCS) environment from the host computer to the target via JTAG interface [135]. Detail information and specifications of TMS320F28335 DSP board can be found in [136]. Figure C.1 shows the TMS320F28335 DSP card and a block diagram of the converter control architecture is shown in Figure C.2

Figure C.1 Texas instrument TMS320F28335 DSP Board

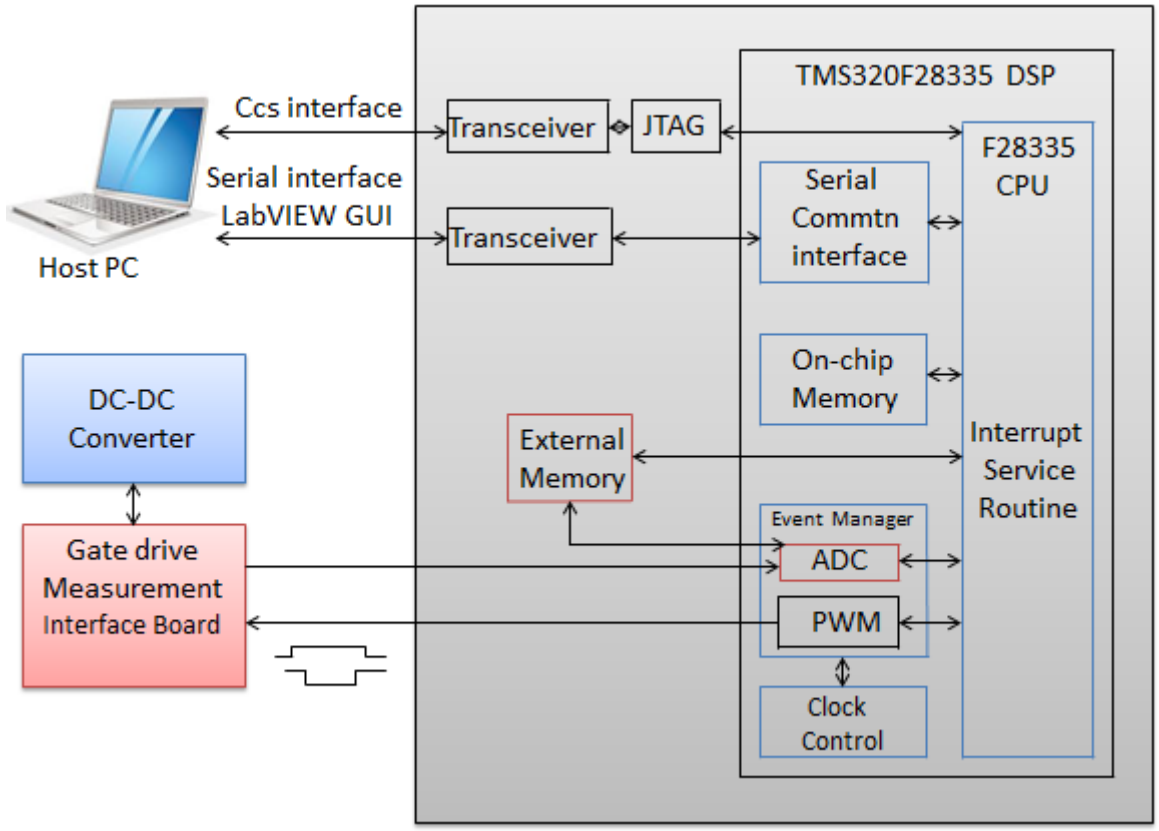

Figure C.2 Control overview

The control structure involves some LabVIEW data exchange loop to allow continuous communication with graphical user interface (GUI) via the RS232 port. This is possible on the F28335 DSP using serial communication interface SCI-A. The GUI allow continuous monitoring and control of the power converter even if the JTAG communication is lost , since JTAG controller is more susceptible to noise than the RS232 interface.

C.3 Software Implementation

The basic structure of the code consists of functions initialisation code followed by LabVIEW data exchange loop which continuously communicate with the DSP via Serial Communication Interface. The main codes (background loop) consist of TMS320F28335 peripheral initialisation such as PLL, PWM module, ADC module, Watchdog, and Event Manager. The entire application software is driven by a primary interrupt service routine (ISR), which contains all the control codes and is triggered from the PWM module of the DSP board. The ISR is invoked every 20 µS (50 KHz) by the period event flag of the Event manager submodule.

The major feature of this implementation is the DSP integration to obtain the reference voltage, configuring the voltage and current loop PI controllers with anti-windup capabilities. Timers 1 is used as the time base for the PWM output generations with compare A and compare B sub modules. The ADC timing is based on ADCCLK (25MHz) derived from SYSCLKOUT and the ADCCLK is used to time the sampling period. To ensure that the samples are acquired before the commencement of the control code execution, the ADC sequencer start of conversion (SOC) is triggered on the apex of PWM carrier. When the ADC sampling process is complete, an interrupt is generated which contains all the control codes. The flow chart of this software implementation is shown in Figure C.3

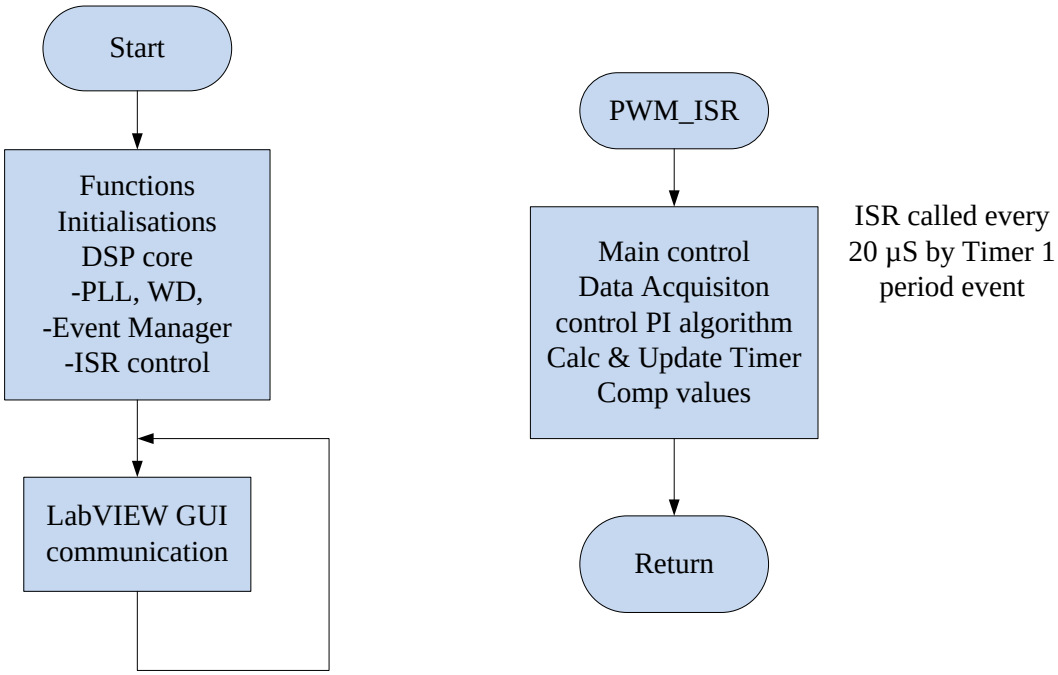

Figure C.3 Program flow chart

Appendix D

Gate Drives and Sensors Interface Board

D.1 Introduction

The gate drive/sensors measurement board is a dedicated isolation and conditioning board, which has been specifically designed for the purpose of generating appropriate gate signals required by the converter switches and also for measuring converter input current and output voltage. Furthermore, the board provide an interface between the spectrum digital F28335 (eZdsp) board and hardware (power converter). The board sit on top of the F28335 DSP board and very close to the power converter board. A comprehensive description of this board is described in this appendix.

D.2 Gate Drive Interface

The ePWM module of F28335 (Figure C.1) represent one complete PWM channel, each channel composed of a pair of PWM signals ePWM1A and ePWM1B respectively. The PWM peripheral can derive up to 12 IGBT's/MOSFETs. The gate drive interface permits the DSP PWM outputs to derive the power converter switches. Two ePWM module output of F28335 microcontroller are chosen and therefore 4 interface circuits are provided. Each interface is for only one PWM signal. The interface caters for single switch with 15V power requirement. This is possible with 5-15 V DC-DC converters. Transmitting PWM signals at 15V is desirable to improve the noise immunity. Figure D.1 shows the interface board, which consist of two parts the gate drive part and the measurement section.

To eliminate the risk of noise or interference between the power converter and DSP board, an isolation interface is provided to completely isolate the analogue circuitry from the digital. This isolation is provided by means of optocoupler (FOD3184). Four optocouplers are therefore used to allow for driving up to 4 switches. Once again to minimise noise pick up, the gate drive signals are transmitted to the power converter board via twisted pair cable.

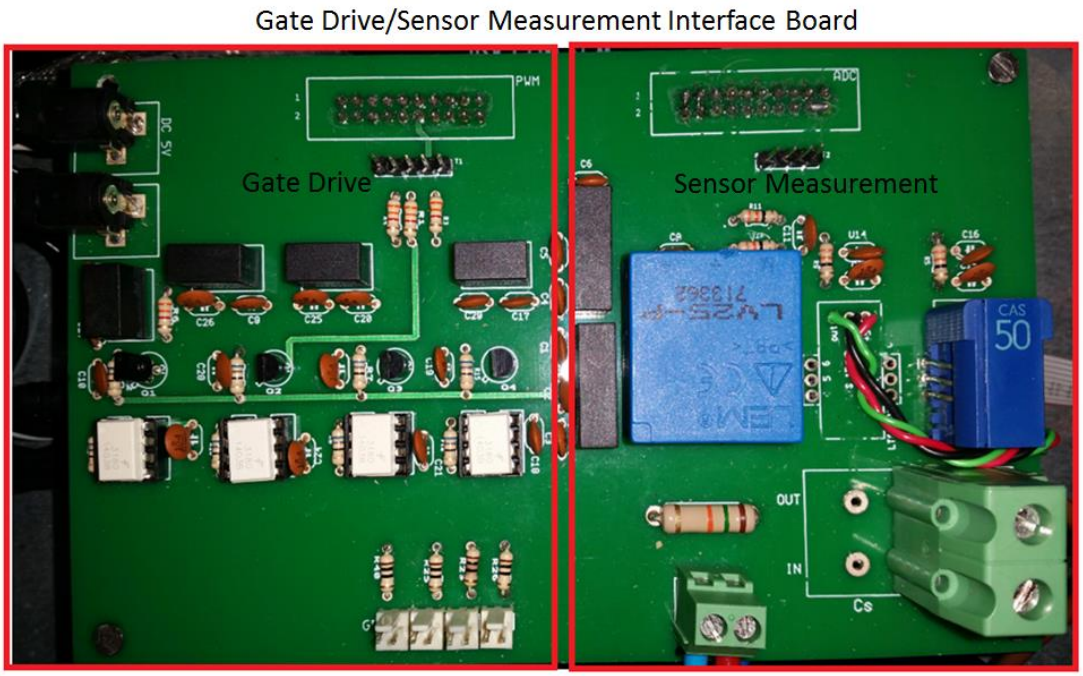

Figure D.1 Interface board

D.3 Sensor Interface

The LEM® current transducer (CAS 50-NP) and voltage transducer (LV-25p) are placed on the interface board (Figure D.1) to allow connection to the microprocessor ADC input. The current transducer is for measuring the input current flowing through the converter. The output current is an analogue voltage within the range of 0-5V with a 2.5V nominal output voltage. The transducer measure the DC input current with galvanic isolation between the power converter and ADC circuit (primary and secondary circuit). On the other hand, the voltage transducer is for measuring the output voltage of the converter by using a load resistor to convert a current to a voltage. The voltage transducer also has galvanic isolation between analogue and digital circuits. The voltage from the load resistor is then routed to a potential divider to ensure that the signal range is compatible with (0-3V) ADC input voltage range.

The sensors are positioned very close to the ADC input of the DSP board such that the track length from the sensor output to the ADC input is very short, to reduce the level of the noise or interference that might creep into the analogue signal.

Appendix E

Power Loss Analysis and Efficiency

E.1 Introduction

The losses in DC-DC converters are due to the parasitic elements inherent in the components for example MOSFET on state resistance, inductor winding resistance, core loss, capacitor ESR and diode forward resistance. Unlike the ideal characteristics, in practice, these parasitic elements limit the voltage gain that a converter can produce. This behaviour is typical in boost converters. In this section, further illustration for the formulae used in estimating the losses regarding the components used in implementing the prototypes.

E.2 Switch Conduction Loss

As explained previously, the conduction losses in MOSFET occur when the device fully conducts and current passing though the on state resistor R_{DS_on} generate a power loss. The main switch conduction loss is calculated using the switch on state resistance from the data sheet and the switch RMS current given by

$$P_{S\_con} = I_{S\_RMS}^2 \cdot R_{DS\_on} \tag{E.1}$$

E.3 Switching Loss

Power devices experience a transition from on-state to off-state and vice versa due to application of PWM gate signals. During this interval a significant amount of voltage and current coexist within the device and resulted in switching losses. The average switching power loss P_S dissipated in the switch during this transition can be estimated from (E.2) [51] as

$$P_S = \frac{f_s}{2} . I_{S\_avg} . V_S \left(t_{C\_on} + t_{C\_off}\right) \tag{E.2}$$

Where:

t_{C_on} is the on-state transit time,

t_{C_off} is the off- state transit time,

I_{S_avg} , V_S is the current through and voltage across the device

The switching losses during turn on and turn off is usually taken as zero if the converter power devices achieve (ZVS) soft switching performance.

E.4 Diode Conduction and Switching Losses

The estimated conduction loss of a diode is

$$P_{DC-cond} \cong V_{D-F}.I_{DC_{avg}} \tag{E.3}$$

Where V_{D-F} is the forward voltage drop of the diode and $I_{DC_{avg}}$ is the average diode current calculated as follows:

$$I_{DC\_avg} \cong \frac{1}{T_s}\int_0^{(1-D)T_s} i_d\,(t)dt \tag{E.4}$$

Considering that the diodes conduction time is the switch off period $(1-D)T_s$, and i_d is the current flowing through the diode.

E.5 Coupled Inductor Copper and Core Loss

The power dissipated per unit of winding volume in either the primary or secondary windings of the coupled inductor due to its DC resistance is obtained using the following relation

$$P_{L\_CU} = \frac{\rho \cdot N_L \cdot l_t \cdot I_{L\_RMS}^2}{n_L \cdot S_f} \tag{E.5}$$

Where ρ is the copper resistivity at 100ºC; N_L is the number of turns in the primary side; S_f is the cross sectional area of the copper wire; n_L is the number of wires in parallel;l_t is the length per turn and I_{L_RMS} is the RMS current in the winding.

The approximate core loss regarding the coupled inductor is calculated based on the most widely used Steinmetz equation [137], that characterizes the core losses in the power equation expressed as

$$PL = aB_{pk}^b f^c \tag{E.6}$$

Where a, b, c are constants determine from curve fitting, B is the magnetic flux variation, f is the operating frequency of the coupled inductor and PL is the time average power loss per unit volume.

E.6 Theoretical Efficiency

The estimated total power loss of the converter is

$$P_T = PL + P_{L\_CU} + P_{S\_con} + P_S + P_{D\_con} \tag{E.7}$$

And the estimated theoretical converter efficiency η_T under the rated load condition can be obtained from (E.8) based on the calculated losses.

$$\eta_T = \frac{P_o}{P_o + P_T} \cdot 100 \tag{E.8}$$

References

1. Armstrong, M., et al., *Low order harmonic cancellation in a grid connected multiple inverter system via current control parameter randomization.* IEEE Transactions on Power Electronics, , 2005. **20**(4): p. 885-892.
2. Armstrong, M., et al., *Auto-Calibrating DC Link Current Sensing Technique for Transformerless, Grid Connected, H-Bridge Inverter Systems.* IEEE Transactions on Power Electronics,, 2006. **21**(5): p. 1385-1393.
3. Bialasiewicz, J.T., *Renewable Energy Systems With Photovoltaic Power Generators: Operation and Modeling.* IEEE Transactions on Industrial Electronics,, 2008. **55**(7): p. 2752-2758.
4. Kuo-Ching, T., H. Chi-Chih, and S. Wei-Yuan, *A High Step-Up Converter With a Voltage Multiplier Module for a Photovoltaic System.* IEEE Transactions on Power Electronics,, 2013. **28**(6): p. 3047-3057.
5. Green, S., et al., *Fault tolerant, variable frequency, unity power factor converters for safety critical PM drives.* Electric Power Applications, IEE Proceedings -, 2003. **150**(6): p. 663-672.
6. Branco, C.G.C., et al., *A Nonisolated Single-Phase UPS Topology With 110-V/220-V Input-Output Voltage Ratings.* IEEE Transactions on Industrial Electronics, , 2008. **55**(8): p. 2974-2983.
7. Torrico-Bascope, R.P., et al., *A UPS With 110-V/220-V Input Voltage and High-Frequency Transformer Isolation.* IEEE Transactions on Industrial Electronics,, 2008. **55**(8): p. 2984-2996.
8. Sung-Sae, L., C. Seong-Wook, and M. Gun-Woo, *High-Efficiency Active-Clamp Forward Converter With Transient Current Build-Up (TCB) ZVS Technique.* IEEE Transactions on Industrial Electronics,, 2007. **54**(1): p. 310-318.
9. Emadi, A., L. Young Joo, and K. Rajashekara, *Power Electronics and Motor Drives in Electric, Hybrid Electric, and Plug-In Hybrid Electric Vehicles.* IEEE Transactions on Industrial Electronics,, 2008. **55**(6): p. 2237-2245.
10. Qun, Z. and F.C. Lee, *High-efficiency, high step-up DC-DC converters.* IEEE Transactions on Power Electronics,, 2003. **18**(1): p. 65-73.
11. Yuequan, H. and M.M. Jovanovic. *High-Intensity-Discharge Lamp Ballast With Igniter Driven by Dual-Frequency Inverter*. in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*. 2007.
12. Dragicevic, T., et al., *DC Microgrids-Part I: A Review of Control Strategies and Stabilization Techniques.* IEEE Transactions on Power Electronics, , 2015. **PP**(99): p. 1-1.
13. Rashid, M.H., *Power Electronics Circuits, Devices, and Applications.* Third Edition, 2004(Pearson Education Inc,).
14. R.W. Erickson, D.M., *Fundamental of Power Electronics.* Second Edition, 2004(Kluwer Academic Publishers).
15. Xiaogang, F., L. Jinjun, and F.C. Lee, *Impedance specifications for stable DC distributed power systems.* IEEE Transactions on Power Electronics,, 2002. **17**(2): p. 157-162.

16. Watson, R., F.C. Lee, and G.C. Hua, *Utilization of an active-clamp circuit to achieve soft switching in flyback converters.* IEEE Transactions on Power Electronics,, 1996. **11**(1): p. 162-169.
17. Crescimbini, F., et al., *High-Speed Electric Drive for Exhaust Gas Energy Recovery Applications.* IEEE Transactions on Industrial Electronics,, 2014. **61**(6): p. 2998-3011.
18. REN21, *Renewables 2015 Global Status Report.* REN21 Renewables Energy Policy Network For the 21st Century, 2015.
19. Wuhua, L. and H. Xiangning, *Review of Nonisolated High-Step-Up DC/DC Converters in Photovoltaic Grid-Connected Applications.* IEEE Transactions on Industrial Electronics,, 2011. **58**(4): p. 1239-1250.
20. Khan, M.A., et al., *Performance Analysis of Bidirectional DC-DC Converters for Electric Vehicles.* IEEE Transactions on Industry Applications, , 2015. **51**(4): p. 3442-3452.
21. Luo, S., *A review of distributed power systems part I: DC distributed power system.* Aerospace and Electronic Systems Magazine, IEEE, 2005. **20**(8): p. 5-16.
22. Shiguo, L. and I. Batarseh, *A review of distributed power systems. Part II. High frequency AC distributed power systems.* Aerospace and Electronic Systems Magazine, IEEE, 2006. **21**(6): p. 5-14.
23. Prudente, M., et al., *Voltage Multiplier Cells Applied to Non-Isolated DC-DC Converters.* IEEE Transactions on Power Electronics,, 2008. **23**(2): p. 871-887.
24. Sanghyuk, L., K. Pyosoo, and C. Sewan, *High Step-Up Soft-Switched Converters Using Voltage Multiplier Cells.* Power Electronics, IEEE Transactions on, 2013. **28**(7): p. 3379-3387.
25. Spiazzi, G., P. Mattavelli, and A. Costabeber, *High Step-Up Ratio Flyback Converter With Active Clamp and Voltage Multiplier.* IEEE Transactions on Power Electronics,, 2011. **26**(11): p. 3205-3214.
26. Jiann-Fuh, C., C. Ren-Yi, and L. Tsorng-Juu, *Study and Implementation of a Single-Stage Current-Fed Boost PFC Converter With ZCS for High Voltage Applications.* IEEE Transactions on Power Electronics,, 2008. **23**(1): p. 379-386.
27. Kong, X. and A.M. Khambadkone, *Analysis and Implementation of a High Efficiency, Interleaved Current-Fed Full Bridge Converter for Fuel Cell System.* IEEE Transactions on Power Electronics,, 2007. **22**(2): p. 543-550.
28. Jang, S.J., et al., *Fuel Cell Generation System With a New Active Clamping Current-Fed Half-Bridge Converter.* IEEE Transactions on Energy Conversion, , 2007. **22**(2): p. 332-340.
29. Sang-Kyoo, H., et al., *A new active clamping zero-voltage switching PWM current-fed half-bridge converter.* IEEE Transactions on Power Electronics,, 2005. **20**(6): p. 1271-1279.
30. Quan, L. and P. Wolfs, *A Current Fed Two-Inductor Boost Converter With an Integrated Magnetic Structure and Passive Lossless Snubbers for Photovoltaic Module Integrated Converter Applications.* IEEE Transactions on Power Electronics,, 2007. **22**(1): p. 309-321.
31. Gopinath, R., et al., *Development of a low cost fuel cell inverter system with DSP control.* IEEE Transactions on Power Electronics,, 2004. **19**(5): p. 1256-1262.
32. Blaabjerg, F., C. Zhe, and S.B. Kjaer, *Power electronics as efficient interface in dispersed power generation systems.* IEEE Transactions on Power Electronics,, 2004. **19**(5): p. 1184-1194.
33. Jung-Min, K., et al., *High-Efficiency Fuel Cell Power Conditioning System With Input Current Ripple Reduction.* IEEE Transactions on Industrial Electronics,, 2009. **56**(3): p. 826-834.
34. Sung-Ho, L., et al., *Hybrid-Type Full-Bridge DC/DC Converter With High Efficiency.* IEEE Transactions on Power Electronics,, 2015. **30**(8): p. 4156-4164.

35. Wuhua, L., et al., *High-Step-Up and High-Efficiency Fuel-Cell Power-Generation System With Active-Clamp Flyback-Forward Converter.* IEEE Transactions on Industrial Electronics, , 2012. **59**(1): p. 599-610.
36. Lin, B.R. and J.J. Chen, *Analysis and implementation of a soft switching converter with high-voltage conversion ratio.* IET Power Electronics,, 2008. **1**(3): p. 386-394.
37. Wijeratne, D.S. and G. Moschopoulos, *Quadratic Power Conversion for Power Electronics: Principles and Circuits.* IEEE Transactions on Circuits and Systems I: Regular Papers,, 2012. **59**(2): p. 426-438.
38. Shahin, A., et al., *High Voltage Ratio DC-DC Converter for Fuel-Cell Applications.* IEEE Transactions on Industrial Electronics,, 2010. **57**(12): p. 3944-3955.
39. Leyva-Ramos, J., et al., *Switching regulator using a quadratic boost converter for wide DC conversion ratios.* IET Power Electronics,, 2009. **2**(5): p. 605-613.
40. Axelrod, B., Y. Berkovich, and A. Ioinovici, *Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC–DC PWM Converters.* IEEE Transactions on Circuits and Systems I: Regular Papers, 2008. **55**(2): p. 687-696.
41. Fang Lin, L. and Y. Hong, *Positive output super-lift converters.* IEEE Transactions on Power Electronics, , 2003. **18**(1): p. 105-113.
42. Lung-Sheng, Y., L. Tsorng-Juu, and C. Jiann-Fuh, *Transformerless DC-DC Converters With High Step-Up Voltage Gain.* IEEE Transactions on Industrial Electronics,, 2009. **56**(8): p. 3144-3152.
43. Yan, D., et al., *Single-Switch High Step-Up Converters With Built-In Transformer Voltage Multiplier Cell.* IEEE Transactions on Power Electronics,, 2012. **27**(8): p. 3557-3567.
44. Shih-Kuen, C., et al., *Novel High Step-Up DC-DC Converter for Fuel Cell Energy Conversion System.* IEEE Transactions on Industrial Electronics,, 2010. **57**(6): p. 2007-2017.
45. Wuhua, L., et al., *Interleaved Converter With Voltage Multiplier Cell for High Step-Up and High-Efficiency Conversion.* IEEE Transactions on Power Electronics,, 2010. **25**(9): p. 2397-2408.
46. Sungsik, P., et al., *Soft-Switched Interleaved Boost Converters for High Step-Up and High-Power Applications.* IEEE Transactions on Power Electronics,, 2011. **26**(10): p. 2906-2914.
47. Ching-Ming, L. and L. Yi-Hung, *Modeling, Analysis, and Design of an Interleaved Four-Phase Current-Fed Converter With New Voltage Multiplier Topology.* IEEE Transactions on Industry Applications,, 2013. **49**(1): p. 208-222.
48. Yi, Z., L. Wuhua, and H. Xiangning, *Single-Phase Improved Active Clamp Coupled-Inductor-Based Converter With Extended Voltage Doubler Cell.* IEEE Transactions on Power Electronics,, 2012. **27**(6): p. 2869-2878.
49. On-Cheong, M., W. Yue-Chung, and A. Ioinovici, *Step-up DC power supply based on a switched-capacitor circuit.* IEEE Transactions on Industrial Electronics,, 1995. **42**(1): p. 90-97.
50. Wuhua, L., et al., *Single-Stage Single-Phase High-Step-Up ZVT Boost Converter for Fuel-Cell Microgrid System.* IEEE Transactions on Power Electronics,, 2010. **25**(12): p. 3057-3065.
51. N. Mohan, T.M.U., W. P. Robbins, *Power Electronics Converter, Applications, and Design.* Third Edition, 2006(John Wiley & Sons, Inc).
52. Pahlevaninezhad, M., et al., *A Novel ZVZCS Full-Bridge DC/DC Converter Used for Electric Vehicles.* IEEE Transactions on Power Electronics,, 2012. **27**(6): p. 2752-2769.

53. Yao-Ching, H., C. Ming-Ren, and C. Hung-Liang, *An Interleaved Flyback Converter Featured With Zero-Voltage Transition.* IEEE Transactions on Power Electronics,, 2011. **26**(1): p. 79-84.
54. Hongfei, W. and X. Yan, *Families of Forward Converters Suitable for Wide Input Voltage Range Applications.* IEEE Transactions on Power Electronics,, 2014. **29**(11): p. 6006-6017.
55. Tsang, C.W., et al., *Analysis and Design of LLC Resonant Converters With Capacitor Diode Clamp Current Limiting.* IEEE Transactions on Power Electronics, 2015. **30**(3): p. 1345-1355.
56. Huber, L. and M.M. Jovanovic. *A design approach for server power supplies for networking applications*. in *Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE*. 2000.
57. Tsai-Fu, W. and L. Sihh-An, *A systematic approach to developing single-stage soft switching PWM converters.* IEEE Transactions on Power Electronics,, 2001. **16**(5): p. 581-593.
58. Tsai-Fu, W. and Y. Te-Hung, *Unified approach to developing single-stage power converters.* IEEE Transactions on Aerospace and Electronic Systems,, 1998. **34**(1): p. 211-223.
59. Barreto, L.H.S.C., et al., *A quasi-resonant quadratic boost converter using a single resonant network.* IEEE Transactions on Industrial Electronics,, 2005. **52**(2): p. 552-557.
60. Mahdavikhah, B. and A. Prodic, *Low-Volume PFC Rectifier Based on Nonsymmetric Multilevel Boost Converter.* IEEE Transactions on Power Electronics,, 2015. **30**(3): p. 1356-1372.
61. Zhang, M.T., et al. *Single-phase three-level boost power factor correction converter*. in *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual*. 1995.
62. Barbi, I. and R. Gules, *Isolated DC-DC converters with high-output voltage for TWTA telecommunication satellite applications.* IEEE Transactions on Power Electronics, , 2003. **18**(4): p. 975-984.
63. Ismail, E.H., et al., *A Family of Single-Switch PWM Converters With High Step-Up Conversion Ratio.* IEEE Transactions on Circuits and Systems I: Regular Papers, , 2008. **55**(4): p. 1159-1171.
64. Abutbul, O., et al., *Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit.* IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,, 2003. **50**(8): p. 1098-1102.
65. Chun-Kit, C., et al., *On Energy Efficiency of Switched-Capacitor Converters.* IEEE Transactions on Power Electronics,, 2013. **28**(2): p. 862-876.
66. Fan, Z., et al., *A New Design Method for High-Power High-Efficiency Switched-Capacitor DC-DC Converters.* IEEE Transactions on Power Electronics, , 2008. **23**(2): p. 832-840.
67. Fang Lin, L. and Y. Hong, *Negative output super-lift converters.* IEEE Transactions on Power Electronics,, 2003. **18**(5): p. 1113-1121.
68. Fang Lin, L. and Y. Hong, *Hybrid split capacitors and split inductors applied in positive output super-lift Luo-converters.* IET Power Electronics,, 2013. **6**(9): p. 1759-1768.
69. Berkovich, Y., et al., *Improved Luo converter modifications with increasing voltage ratio.* IET Power Electronics,, 2015. **8**(2): p. 202-212.
70. Yu, T., W. Ting, and H. Yaohua, *A Switched-Capacitor-Based Active-Network Converter With High Voltage Gain.* IEEE Transactions on Power Electronics, , 2014. **29**(6): p. 2959-2968.

71. Yu, T., et al., *Analysis of Active-Network Converter With Coupled Inductors.* IEEE Transactions on Power Electronics,, 2015. **30**(9): p. 4874-4882.
72. Yu, T., W. Ting, and F. Dongjin, *Multicell Switched-Inductor/Switched-Capacitor Combined Active-Network Converters.* IEEE Transactions on Power Electronics, , 2015. **30**(4): p. 2063-2072.
73. Tsai-Fu, W., et al., *Boost Converter With Coupled Inductors and Buck & Boost Type of Active Clamp.* IEEE Transactions on Industrial Electronics,, 2008. **55**(1): p. 154-162.
74. Inaba, C.Y., Y. Konishi, and M. Nakaoka, *High frequency PWM controlled step-up chopper type DC-DC power converters with reduced peak switch voltage stress.* Electric Power Applications, IEE Proceedings -, 2004. **151**(1): p. 47-52.
75. Rong-Jong, W. and D. Rou-Yong, *High-efficiency power conversion for low power fuel cell generation system.* IEEE Transactions on Power Electronics,, 2005. **20**(4): p. 847-856.
76. Tsorng-Juu, L., et al., *Ultra-Large Gain Step-Up Switched-Capacitor DC-DC Converter With Coupled Inductor for Alternative Sources of Energy.* IEEE Transactions on Circuits and Systems I: Regular Papers,, 2012. **59**(4): p. 864-874.
77. Ki-Bum, P., M. Gun-Woo, and Y. Myung-Joong, *Nonisolated High Step-Up Stacked Converter Based on Boost-Integrated Isolated Converter.* IEEE Transactions on Power Electronics,, 2011. **26**(2): p. 577-587.
78. Ki-Bum, P., M. Gun-Woo, and Y. Myung-Joong, *Nonisolated High Step-up Boost Converter Integrated With Sepic Converter.* IEEE Transactions on Power Electronics,, 2010. **25**(9): p. 2266-2275.
79. Hyun-Lark, D., *A Soft-Switching DC/DC Converter With High Voltage Gain.* IEEE Transactions on Power Electronics, , 2010. **25**(5): p. 1193-1200.
80. Moises Tanca, V. and I. Barbi. *Nonisolated high step-up stacked dc-dc converter based on boost converter elements for high power application*. in *IEEE International Symposium on Circuits and Systems (ISCAS), 2011*. 2011.
81. Araujo, S.V., R.P. Torrico-Bascope, and G.V. Torrico-Bascope, *Highly Efficient High Step-Up Converter for Fuel-Cell Power Processing Based on Three-State Commutation Cell.* IEEE Transactions on Industrial Electronics,, 2010. **57**(6): p. 1987-1997.
82. Tseng, K.C. and T.J. Liang, *Novel high-efficiency step-up converter.* IEE Proceedings on Electric Power Applications,, 2004. **151**(2): p. 182-190.
83. Kuo-Ching, T. and H. Chi-Chih, *High Step-Up High-Efficiency Interleaved Converter With Voltage Multiplier Module for Renewable Energy System.* IEEE Transactions on Industrial Electronics,, 2014. **61**(3): p. 1311-1319.
84. Yi, Z., et al., *Single-Phase High Step-up Converter With Improved Multiplier Cell Suitable for Half-Bridge-Based PV Inverter System.* IEEE Transactions on Power Electronics,, 2014. **29**(6): p. 2807-2816.
85. Rong-Jong, W., et al., *High-Efficiency Power Conversion System for Kilowatt-Level Stand-Alone Generation Unit With Low Input Voltage.* IEEE Transactions on Industrial Electronics,, 2008. **55**(10): p. 3702-3714.
86. Hyun-Lark, D., *Improved ZVS DC-DC Converter With a High Voltage Gain and a Ripple-Free Input Current.* IEEE Transactions on Circuits and Systems I: Regular Papers,, 2012. **59**(4): p. 846-853.
87. Yi-Ping, H., et al., *Novel High Step-Up DC-DC Converter With Coupled-Inductor and Switched-Capacitor Techniques for a Sustainable Energy System.* IEEE Transactions on Power Electronics,, 2011. **26**(12): p. 3481-3490.
88. Shih-Ming, C., et al., *A Boost Converter With Capacitor Multiplier and Coupled Inductor for AC Module Applications.* IEEE Transactions on Industrial Electronics, , 2013. **60**(4): p. 1503-1511.

89. Xuefeng, H. and G. Chunying, *A High Voltage Gain DC-DC Converter Integrating Coupled-Inductor and Diode-Capacitor Techniques.* IEEE Transactions on Power Electronics,, 2014. **29**(2): p. 789-800.
90. Cajazeiras Silveira, G., et al., *A Nonisolated DC-DC Boost Converter With High Voltage Gain and Balanced Output Voltage.* IEEE Transactions on Industrial Electronics,, 2014. **61**(12): p. 6739-6746.
91. Tofoli, F.L., et al., *Novel Nonisolated High-Voltage Gain DC-DC Converters Based on 3SSC and VMC.* IEEE Transactions on Power Electronics,, 2012. **27**(9): p. 3897-3907.
92. Wuhua, L., et al., *General Derivation Law of Nonisolated High-Step-Up Interleaved Converters With Built-In Transformer.* IEEE Transactions on Industrial Electronics,, 2012. **59**(3): p. 1650-1661.
93. Dwari, S. and L. Parsa, *An Efficient High-Step-Up Interleaved DC-DC Converter With a Common Active Clamp.* IEEE Transactions on Power Electronics,, 2011. **26**(1): p. 66-78.
94. Henn, G.A.L., et al., *Interleaved-Boost Converter With High Voltage Gain.* IEEE Transactions on Power Electronics,, 2010. **25**(11): p. 2753-2761.
95. Ching-Tsai, P., C. Chen-Feng, and C. Chia-Chi, *A Novel Transformer-less Adaptable Voltage Quadrupler DC Converter with Low Switch Voltage Stress.* IEEE Transactions on Power Electronics,, 2014. **29**(9): p. 4787-4796.
96. Yungtaek, J. and M.M. Jovanovic, *New two-inductor boost converter with auxiliary transformer.* IEEE Transactions on Power Electronics,, 2004. **19**(1): p. 169-175.
97. Ching-Ming, L., P. Ching-Tsai, and C. Ming-Chieh, *High-Efficiency Modular High Step-Up Interleaved Boost Converter for DC-Microgrid Applications.* IEEE Transactions on Industry Applications,, 2012. **48**(1): p. 161-171.
98. Wuhua, L., et al., *High Step-Up Interleaved Converter With Built-In Transformer Voltage Multiplier Cells for Sustainable Energy Applications.* IEEE Transactions on Power Electronics,, 2014. **29**(6): p. 2829-2836.
99. Garcia, F.S., J.A. Pomilio, and G. Spiazzi, *Modeling and Control Design of the Interleaved Double Dual Boost Converter.* IEEE Transactions on Industrial Electronics, , 2013. **60**(8): p. 3283-3290.
100. Yungtaek, J. and M.M. Jovanovic, *Interleaved Boost Converter With Intrinsic Voltage-Doubler Characteristic for Universal-Line PFC Front End.* IEEE Transactions on Power Electronics,, 2007. **22**(4): p. 1394-1401.
101. Weichen, L., et al., *Interleaved High Step-Up ZVT Converter With Built-In Transformer Voltage Doubler Cell for Distributed PV Generation System.* IEEE Transactions on Power Electronics,, 2013. **28**(1): p. 300-313.
102. Dong, W., H. Xiangning, and R. Zhao, *ZVT Interleaved Boost Converters with Built-In Voltage Doubler and Current Auto-Balance Characteristic.* IEEE Transactions on Power Electronics,, 2008. **23**(6): p. 2847-2854.
103. Wuhua, L., et al., *Interleaved High Step-Up Converter With Winding-Cross-Coupled Inductors and Voltage Multiplier Cells.* IEEE Transactions on Power Electronics, , 2012. **27**(1): p. 133-143.
104. Hua, G., et al., *Novel zero-voltage-transition PWM converters.* IEEE Transactions on Power Electronics, , 1994. **9**(2): p. 213-219.
105. Chao-Cheng, W. and Y. Chung-Ming, *New ZVT-PWM DC/DC converters using active snubber.* IEEE Transactions on Aerospace and Electronic Systems,, 2003. **39**(1): p. 164-175.
106. Yungtaek, J., et al., *High-power-factor soft-switched boost converter.* IEEE Transactions on Power Electronics,, 2006. **21**(1): p. 98-104.

107. Junhong, Z., et al., *High-Power Density Design of a Soft-Switching High-Power Bidirectional dc–dc Converter.* IEEE Transactions on Power Electronics,, 2007. **22**(4): p. 1145-1153.
108. Gang, Y., et al. *An Improved ZVT PWM Three Level Boost Converter for Power Factor Preregulator*. in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*. 2007.
109. Hongyang, W. and H. Xiangning, *Single phase three-level power factor correction circuit with passive lossless snubber.* IEEE Transactions on Power Electronics, , 2002. **17**(6): p. 946-953.
110. Bor-Ren, L. and H. Fang-Yu, *Soft-Switching Zeta-Flyback Converter With a Buck-Boost Type of Active Clamp.* IEEE Transactions on Industrial Electronics,, 2007. **54**(5): p. 2813-2822.
111. Jovanovic, M.M. and J. Yungtaek, *A novel active snubber for high-power boost converters.* IEEE Transactions on Power Electronics, 2000. **15**(2): p. 278-284.
112. Jovanovic, M.M., *A technique for reducing rectifier reverse-recovery-related losses in high-power boost converters.* IEEE Transactions on Power Electronics,, 1998. **13**(5): p. 932-941.
113. Duarte, C.M.C. and I. Barbi, *An improved family of ZVS-PWM active-clamping DC-to-DC converters.* IEEE Transactions on Power Electronics,, 2002. **17**(1): p. 1-7.
114. Smith, K.M., Jr. and K.M. Smedley, *Lossless passive soft-switching methods for inverters and amplifiers.* IEEE Transactions on Power Electronics,, 2000. **15**(1): p. 164-173.
115. Chen, C.L. and C.J. Tseng, *Passive lossless snubbers for DC/DC converters.* IEE Proceedings on Circuits, Devices and Systems,, 1998. **145**(6): p. 396-401.
116. Qun, Z., et al., *A simple and effective method to alleviate the rectifier reverse-recovery problem in continuous-current-mode boost converters.* IEEE Transactions on Power Electronics,, 2001. **16**(5): p. 649-658.
117. Sang-Hoon, P., et al., *Analysis and Design of a Soft-Switching Boost Converter With an HI-Bridge Auxiliary Resonant Circuit.* IEEE Transactions on Power Electronics,, 2010. **25**(8): p. 2142-2149.
118. Mishima, T., Y. Takeuchi, and M. Nakaoka, *Analysis, Design, and Performance Evaluations of an Edge-Resonant Switched Capacitor Cell-Assisted Soft-Switching PWM Boost DC-DC Converter and Its Interleaved Topology.* IEEE Transactions on Power Electronics,, 2013. **28**(7): p. 3363-3378.
119. Muhammad, M., M. Armstrong, and M. Elgendy. *Non-isolated DC-DC converter for high-step-up ratio applications*. in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*. 2015.
120. Powder Cores, *Core Selection Procedure.* Magnetics Incorportion Powder Core Catalogue, 2002.
121. Muhammad, M., M. Armstrong, and M.A. Elgendy. *Modelling and control of non-isolated high voltage gain boost converter employing coupled inductor and switched capacitor*. in *2016 International Conference for Students on Applied Engineering (ICSAE)*. 2016.
122. Ogata, K., *Modern Control Engineering.* Fifth Edition, 2010(Pearson Education Inc,).
123. Kui-Jun, L., et al., *Nonisolated ZVT Two-Inductor Boost Converter With a Single Resonant Inductor for High Step-Up Applications.* IEEE Transactions on Power Electronics,, 2012. **27**(4): p. 1966-1973.
124. Muhammad, M., M. Armstrong, and M.A. Elgendy, *A Nonisolated Interleaved Boost Converter for High-Voltage Gain Applications.* IEEE Journal of Emerging and Selected Topics in Power Electronics, 2016. **4**(2): p. 352-362.

125. Muhammad, M., M. Armstrong, and M.A. Elgendy. *Non-isolated, high gain, boost converter for power electronic applications*. in *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*. 2016.
126. Dwari, S., et al. *Dynamics Characterization of Coupled-Inductor Boost DC-DC Converters*. in *Computers in Power Electronics, 2006. COMPEL '06. IEEE Workshops on*. 2006.
127. Yu, F. and M. Xudong, *A Novel PV Microinverter With Coupled Inductors and Double-Boost Topology.* IEEE Transactions on Power Electronics,, 2010. **25**(12): p. 3139-3147.
128. Restrepo, C., et al., *Current-Mode Control of a Coupled-Inductor Buck Boost DC-DC Switching Converter*. IEEE Transactions on Power Electronics,, 2012. **27**(5): p. 2536-2549.
129. Rathore, A.K., et al., *Small signal analysis and closed loop control design of active-clamped zero-voltage switched two inductor current-fed isolated DC-DC converter.* IET Power Electronics,, 2011. **4**(1): p. 51-62.
130. Dupont, F.H., et al., *Reduced-Order Model and Control Approach for the Boost Converter With a Voltage Multiplier Cell.* IEEE Transactions on Power Electronics,, 2013. **28**(7): p. 3395-3404.
131. Bibian, S. and J. Hua, *High performance predictive dead-beat digital controller for DC power supplies.* IEEE Transactions on Power Electronics,, 2002. **17**(3): p. 420-427.
132. S. Buso, P.M., *Digital Control in Power Electronics.* First edition, 2006(Morgan & Claypool).
133. TMS320F28335, *Analog-to-Digital Converter (ADC) Module*. Texas Instrument, Reference Guide SPRU812A, 2007.
134. TMS320F28335, T.F., TMS320F28332, *Enhanced Pulse Width Modulator (ePWM) Module.* Texas Instrument, Reference Guide SPRU791D,2007
135. TMS320F28335, *eZdsp F28335.* Texas Instrument, Technical Reference, 2007
136. TMS320F28335, T.F., TMS320F28332, *Digital Signal Controllers (DSCs).* Texas Instrument, Data Manual SPRS439B, 2007.
137. Muhlethaler, J., et al., *Core Losses Under the DC Bias Condition Based on Steinmetz Parameters.* Power Electronics, IEEE Transactions on, 2012. **27**(2): p. 953-963.