Dynamic Performance of Voltage Balancing and Circulating Current Suppression Control for Modular Multilevel Converter

By

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Abstract: Global power consumption has increased by approximately 3% each year over the past 15 years. The growing demand for energy has stimulated the spread of clean and reliable renewable energy networks and power grid interconnections throughout the world. For example, in Europe, there are 23 High Voltage Direct Current (HVDC) Transmission lines under construction which are scheduled for completion before 2024. The Modular Multilevel Converter (MMC) is one of the most attractive candidates for the HVDC transmission system converter technology. Its high flexibility and controllability make it an attractive option for HVDC transmission. However, the higher initial investment and the unfavourable conditions for using associated DC circuit breakers have always been a barrier to further installations. Since ABB successfully developed the HVDC DC circuit breakers in 2012, there is increasing interest in DC grids using the MMC HVDC transmission system. However, one of the common problems existing in the HVDC transmission system is the control of the capacitor voltage in each submodule of the MMC. However, in the transmission systems, especially in the renewable energy systems, there are disturbances existing. The conventional voltage balancing control is weak to the disturbances, such as power and sampling frequency changes. Therefore, the proposed voltage balancing control in this thesis has improved the responding time and precision of the control. It determines the charging state of each submodule by deriving the capacitor voltage variations, thereby ensuring the voltage of each capacitor is within pre-defined range regardless the disturbance. In later study, both simulation and experimental results have shown the proposed control approach has strong immunity to the sampling frequency noise compared to the conventional control. However, even with the proposed voltage balancing control, the capacitor voltage difference cannot be eliminated entirely. They will cause circulating current flowing among the phases of the circuit. Therefore, causing unnecessary pressures to the affected components. The circulating current suppression control proposed in this thesis can eliminate the AC component of the circulating current, by regulating it according to the power going through the converter. It gets rid of the two PID controllers and abc-dq transformation which are commonly used in conventional circulating current control approach. The simulation and experiment results have shown the suppression of the proposed control approach regarding the AC components in the circulating current, and the fast response time taking effect within one control cycle. In this thesis, both proposed control approaches are presented with simulation results and validated with the scaled down experiment model.

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Foremost, I would like to express my sincere gratitude to my supervisor Dr. David Atkinson for his continuous supports to my Ph.D. study and research, for his patience, motivation, enthusiasm, and immense knowledge and his guidance through the completion of this thesis. I am extremely proud of having a supervisor who is experienced, well-acknowledged, and passionate about the project all the time. His understanding and help in the designing and building of the experiment demonstrated the extremely high standard skill level as an electrical engineer which will be helpful in my later career. I would also like to express my appreciation to my second supervisor Dr. James Yu who has been dedicated to the pursuit of the leading technology for his support not only in academic but also in my leisure time set the first step of my Ph.D. study and have been supporting through my whole Ph.D. life. He was the one who made not only the project but my personal goal come true.

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V_{out}: converter output voltage

V_{dc}: DC link voltage

V_{c_up}: upper arm equivalent voltage

V_{c_low}: lower arm equivalent voltage

L_s: arm inductance

I_{up}: upper arm current

I_{low}: lower arm current

e_j: inner imaginary voltage

I_{diff}: differential current

$V_{c\_up}^*$: control signal for the upper arm

$V_{c\_low}^*$: control signal for the lower arm

MI: modulation index

ω_0: fundamental rotating speed

φ: phase angle

$N_{c\_up1} \ldots N_{c\_upn}$: switching states of the submodule in the upper arm

$V_{c\_up1} \ldots V_{c\_upn}$: capacitor voltages of the first submodule in the upper arm

$N_{c\_up1} \ldots N_{c\_upn}$: switching states of the submodule in the low arm

$V_{c\_up1} \ldots V_{c\_upn}$: capacitor voltages of the first submodule in the low arm

I_p: output currents in upper arm

I_n: output currents in lower arm

C_{arm}: arm capacitance

E_{cmax}: rated converter power

P_s: apparent power

EP: energy-power ratio

$C_1 \ldots C_N$: individual capacitance of each capacitor

N: number of the submodule in each arm

ε: capacitor voltage ripple

C_{sub}: capacitance of each capacitor

$\mathrm{Cos}\varphi$: power factor

I_{2f}: maximum value of the circulating current

α: fault current rise rate

N_{on}: number of the turned-on submodule

P_{out}: output power

$V_{dc}{}^{*}$: demanding voltage of capacitors

$i_{diff1}{}^{*}$: calculated different current

V_{C_avg}: average voltage of the capacitors

S_1: the first switch in submodule

S_2: the second switch in submodule

V_{sub}: submodule reference voltage

f: carrier frequency

$\theta_1 \ldots \theta_n$: the switching angle of the submodules

R: load resistance

Ts: sampling period

Chapter 1

Introduction

1.1 Introduction

The three-phase transmission system has been used in energy transmission systems across different power grids since it was first introduced in the early 1870s. The mature technologies of the three-phase transmission systems compared to the single-phase transmission systems determined that the three-phase system was considered more attractive in the power transmission systems. However, the drawbacks such as relatively high distributed capacitance in the transmission lines exist in the three-phase system when considering the economy efficiency. The distributed capacitance can result in the increasing of the reactive power absorbed by the transmission lines for it needs to be charged to the voltage level during normal operation. Therefore, a large amount of transmission losses can be foreseen in long distance power transmission. It is predicted as high as 30-40% of the total losses per 1000km [1], whereas the High Voltage Direct Current (HVDC) transmission system only has around 3.5% transmission losses along the same distance. Because there are only two transmission lines in the HVDC transmission systems compared to the three-transmission lines in three-phase transmission system, and furthermore, the Direct current in the HVDC transmission lines only charges the distributed line capacitance when the system is activated hence the HVDC transmission system can have much lower transmission losses than the three-phase transmission system regarding the transmitting stage [2][3]. The initial investment for HVDC transmission lines is higher than conventional three-phase transmission system. Two major expenses of the original investment are the installations of AC filters and the converters [4]. They have always been the barriers to the further installation of HVDC transmission systems. In the past fifteen years, the global energy consumption has been increasing by 3% each year [5]. The growing demand for energy not only stimulates the spread of more energy networks but also requires the interconnection between different power grids. For example, in Europe, there are 23 HVDC transmission projects under construction and scheduled for completion before 2024 [6]. These systems, which employ subsea cables, are either connected to distant off-shore wind farms or used for interconnecting several countries with different fundamental frequencies. The higher installation cost for three-phase subsea cables and the high-power losses through the long distance subsea three-phase transmission lines determined that the three-phase transmission system will not be the best option in these cases. On the other hand, the

recent rapid development of the power semiconductor switches, such as Insulated-Gate Bipolar Transistor (IGBT) and DC circuit breakers for high voltage applications [7], has made HVDC more attractive for high voltage applications. There is increasing interest in using Modular Multilevel Converter (MMC) based HVDC transmissions systems, considering the lower transmission losses and the installation costs compared to the three-phase transmission system over long distances. MMC based HVDC transmission topology has attracted much attention from researchers in recent years. However, compared to the well documented traditional three-phase transmission technologies, the research regarding MMC HVDC topology is still developing.

In the history of the development of the HVDC transmission system, the Line Commutated Converter (LCC) was initially employed in the HVDC transmission system. The switching device can be either uncontrollable (such as diode) or controllable (such as thyristor). However, because the power rating of the transmission site is getting higher recently and the significant improvement of the switching devices, the Voltage Source Converter (VSC) based HVDC transmission system appears to have a smaller site area and more cost efficient compared to the LCC based HVDC transmission system at the same power rating. The conventional Voltage Source Converter (VSC) based HVDC transmission system typically employs the two-level or three-level converters using thyristor valves, one of the disadvantages in this topology is a large amount of harmonics on the AC side. Therefore, the AC filters are required on the AC side of the converter to lower the high-frequency harmonics before connecting to the grids [8]. In the conventional HVDC transmission topology, the AC side filters can take up to half the space of the substation. The investment of the conventional transmission sites can be significant when using the two-level or three-level converters. In 2001, Prof. R. Marquardt suggested and patented a new structure for the multilevel converter, Modular Multilevel Converter (MMC), which is one of the most attractive candidates for HVDC transmission system [9]. The multilevel series connected structure and the identical submodules not only reduce the converter output harmonics on the AC side but also lower the difficulty of manufacturing. The multilevel structure also leads to the small voltage step across the submodules, which can result in the lower dv/dt across the components inside each submodule, and reducing the electromagnetic emission and the inrush current at given switching frequency. Therefore, by increasing the number of submodule can lower the size and requirement of the components in each submodule. Another benefit of using MMC is the lower converter output harmonics. When increasing the number of submodules in each arm, the converter output voltage steps are getting smaller. Once the number of submodules is sufficient,

the size of the AC harmonic filter is much smaller than the ones in conventional two-level or three-level converter topology, or the AC harmonic filter is not even necessary in some cases [10]. However, as a result of a large number of the submodules, the high initial investment is justified. One of the biggest problems regarding the MMC is the much greater components cost compared to the traditional two-level thyristor-based converter topology. The modular multilevel structure requires a large number of submodules connected in series in each arm to achieve the smaller voltage step changes, hence the lower converter harmonics. In commercial MMC HVDC system [11], the number of submodules in each arm can be up to 200, including the surplus submodules when there are one or more failure submodules [12]. This large number of submodules leads to high component costs even with the half-bridge MMC structure. The initial investment for the substation can be even higher with full-bridge MMC structure. Hence, author has investigated the potentials of lowering the component costs as well as improving the converter performance in different aspect, and provided the advanced voltage balancing control which can have better performance than the conventional voltage balancing control in different sampling frequency condition. In addition, the simplified circulating current suppressing control is also proposed and verified by both simulation and experimental results, showing strong control of the circulating current existing in the upper and lower arm of the MMC. The detailed results are presented in the following chapters and published in [13][14] as well.

1.2 The development of the high voltage transmission system

It is commonly known in the industrial transmission applications that the higher voltage in the transmission lines, the lower current will be conducted through the transmission lines at the same power rating, therefore lowering the losses along the transmission lines. Base on that, the high voltage or even ultra-high voltage is always preferred in long distance transmission systems. The voltage ratings are presented in Table 1. In three-phase transmission systems, the transmission voltage can be boosted up easily by adding transformers between two networks, hence lowering the currents flowing through the transmission lines. However, the transmission losses caused by the aforementioned distributed capacitance can be large in long distance transmission. Therefore, researchers are seeking a more efficient way to further reduce the losses thus improving the efficiency of the overall network. Due to the need for clean energy, the demand for renewable energy such as wind farm, solar power system, and tide energy etc. are growing [16]. One of the drawbacks of using High Voltage Alternating Current

(HVAC) transmission system to transfer the renewable energy is that, because the power generated by the renewable site is highly dependent on the weather condition, the renewable energy networks may not be as stable as traditional electricity generation methods [17]. In that case, the HVDC transmission system offers immunity to the disturbances according to the weather conditions, because the receiving end and the sending end frequencies are independent. Furthermore, the HVDC transmission system is more efficient than the HVAC transmission system when the transmission distance is long.

Table 1: The voltage rating of applications in different voltage range

Voltage rating	**Voltage range**
Lower voltage	100V – 1 kV
Medium voltage	1 kV – 35 kV
High voltage	35 kV – 230 kV
Extra-high voltage	245 kV and above
Ultra-high voltage*	Over 1000 kV (AC), or 800 kV (DC)

*: It is not defined in the IEC 60038, but is commonly recognized as ultra-high-voltage above that voltage range [15].

Usually, the renewable energy site is far away from the load centre, hundreds or thousands kilometers away. To reduce the electricity losses and costs, the DC transmission lines are preferred when the transmission distance is long, and sometimes it might be the only solution, for example, the distant offshore wind farm. However, due to the much higher initial investment for the substations, the HVDC transmission system is less competitive compared to the HVAC transmission system in less than 50 km – 100 km distance depending on the system configurations.

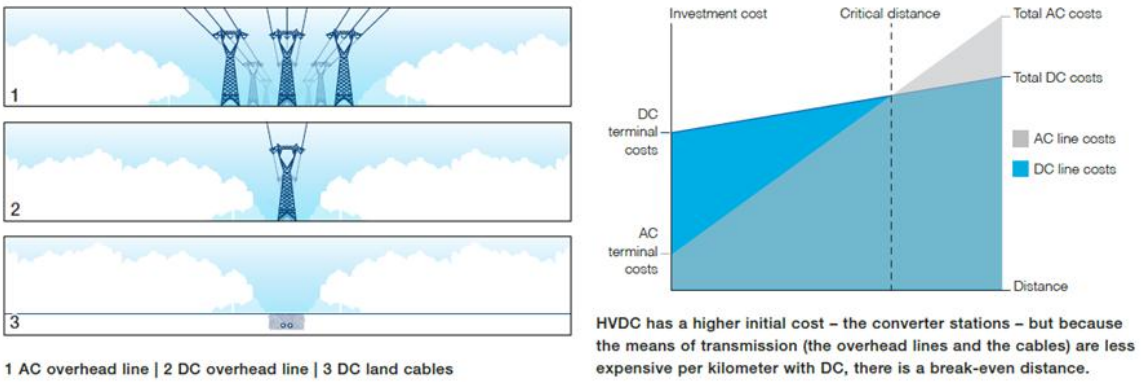


Figure 1: The transmission line setup of the HVAC/HVDC transmission systems, the investment cost along with the transmission distance.

Figure 1 demonstrates the structures of the HVAC/HVDC transmission systems. The number of the transmission lines required for HVDC transmission system is lower than the HVAC transmission system. The HVDC transmission system which employs the DC land cables can reduce the investment for the transmission towers, especially when the DC land cables are used to connect the offshore wind farms. The initial investment cost for the HVDC substations is much higher than the HVAC substations. However, when the transmission distance is increased, the difference between the initial investment of the HVDC and HVAC transmission system is getting smaller. There is a critical point where the costs for both HVDC and HVAC transmission systems are the same, and beyond that point the HVDC transmission system is more cost efficient than the HVAC transmission system. It can be seen in Figure 1 that the initial investment of the AC terminal is lower than the DC terminal. However, the line costs for the AC transmission lines are much higher compare to the DC transmission lines at the same distance. Therefore, the higher initial investment of the DC terminal can be justified by the lower costs of the lines compared to the AC system configurations. Once the distance beyond 150km (50km for subsea cables), the overall investment of the DC transmission system is lower than the AC transmission system. The offshore wind farms connected to the onshore site using subsea cables is considered the most cost efficient application for HVDC transmission system. The break-even distance can be as low as 30 km, which is highly competitive when installing the offshore wind farm [18].

Since the energy consumption is increasing worldwide, the interconnections in different areas or between countries is necessary to bring down the cost. The unique feature of the HVDC transmission system is that it can connect two grids with different fundamental frequencies, and it can provide high immunity to the disturbances generated at one end as the other end is independent. This feature provides a robust system configuration for the multi-terminal connection, which promotes the development of the HVDC transmission projects in Europe [19][20]. In Figure 2, it shows the structure of a four-terminal HVDC transmission system. Because one of the most important factors when considering employ a HVDC transmission system is the distance between the sending end and the receiving end, therefore the HVDC transmission lines are preferred in large continents [21]. However, one of the barriers of realizing the HVDC transmission system is lack of effective fault-tolerant control method, compared to the commonly used half-bridge MMC, the full-bridge MMC based HVDC transmission system can block the DC fault but as the cost of increased investment for semiconductors and power losses [22]. The bi-directional current flowing design for the full-bridge structured

MMC can block the DC fault current by adding appropriate control. Therefore, the popular converters employed in the HVDC transmission systems are investigated and the advantages and disadvantages are listed for guidance when selecting the appropriate converter.

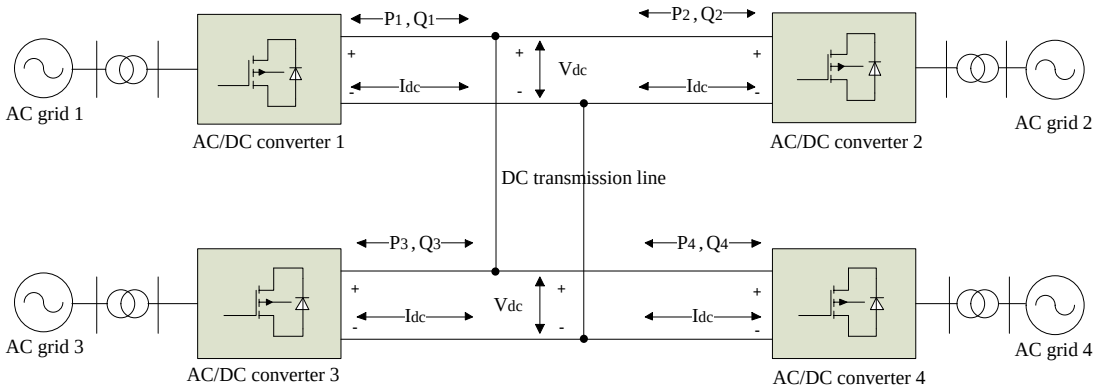


Figure 2: The four-terminal configuration of the HVDC transmission system.

However, the development of the high/ultra-high voltage application never stopped with regard to the large power consumptions at present. M. Candas summarised the ultra-high voltage projects around the world in [160]. By increasing the transmitting voltage to over 800kv, the transmission losses through the long distance can be reduced significantly, which is very attractive when the power consumption center is highly concentrated in a small area and far from the power plants. Therefore, the State Grid Corporation of China (SGCC), the world's largest grid operator, has announced the plan to build 17 UHV transmission lines by 2017 and 27 UHV transmission lines to be constructed by 2020 [161]. Because of the ultra-high voltage ratings of these projects, it enables these transmission lines to transmit power though very long distance with minimal losses. The completed and planned UHV transmission lines in China are shown in Table 2. The power capacity for these transmission lines ranges from 5GW to 12GW. The extreme large power capacity of the transmission lines determined that even a small percentage of efficiency improvement could result in a large amount of power saving. In other words, problems such as computing stress or capacitor voltage deviations with respect to the control approaches could have greater impact on the performance of the UHV transmission lines compared to lower voltage applications.

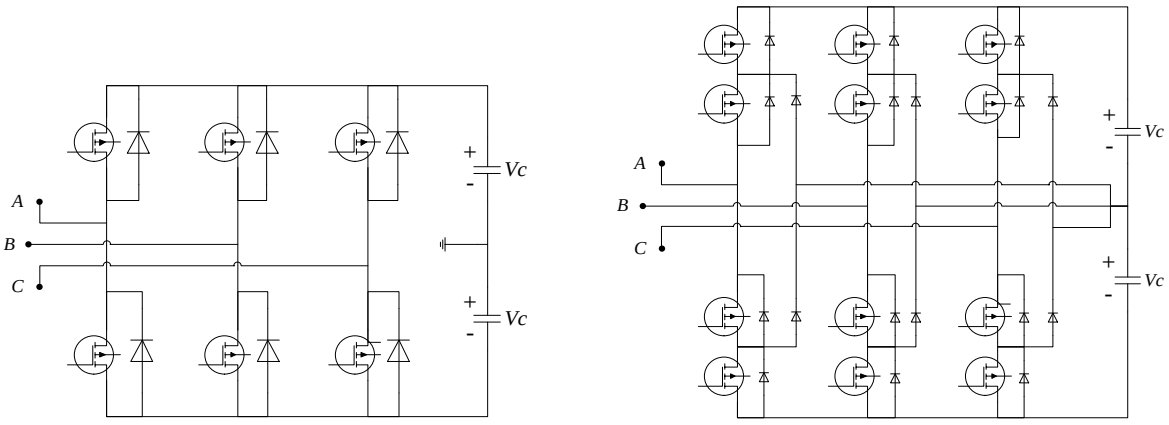
Table 2: The completed/planned UHV transmission lines in China.

Name	Type	Voltage (KV)	Length (km)	Power rating (GW)	Year Completed/to be completed
Jindongnan–Nanyang–Jingmen	UHVAC	1000	640	5	2009
Huainan–Zhejiang North–Shanghai	UHVAC	1000	2×649	8	2013
Zhejiang North - Fuzhou	UHVAC	1000	2×603	6.8	2014
Xilingol League - Shandong	UHVAC	1000	2×730	9	2016
Yunnan - Guangdong	UHVDC	±800	1373	5	2009
Xiangjiaba–Shanghai	UHVDC	±800	1907	6.4	2010
Jinping – Sunan	UHVDC	±800	2059	7.2	2012
Nuozadu - Guangdong	UHVDC	±800	1413	5	2013
Hami – Zhengzhou	UHVDC	±800	2192	8	2014
Xiluodu - Zhejiang West	UHVDC	±800	1653	8	2014
Lingzhou - Shaoxing	UHVDC	±800	1720	8	2016
Shanxi North–Jiangsu	UHVDC	±800	1119	8	2017
Jiuquan–Hunan	UHVDC	±800	2383	8	2017
Xilingol League–Jiangsu	UHVDC	±800	1620	10	2017
Shanghaimiao–Shandong	UHVDC	±800	1238	10	2017
Zhundong–Wannan	UHVDC	±1100	3400	12	2018

1.2.1.Two-level or three-level VSC structure

Because the simple structure and moderate controllability of the two-level and three-level converter, it was commonly used in industrial applications when it first came out in the early 1990s [23], hence it was first employed for HVDC transmission systems in the early stage of the development of the HVDC transmission lines. The two-level and three-level VSC structures were ideal converters for high-voltage applications when the first commercial HVDC transmission line was carried out in 1999 by ABB [24]. Since then, ABB has been developing the design and the structure of the HVDC transmission lines. In the following decades, the completed or incomplete HVDC transmission lines are using the two-level or three-level VSC stricter without exception until 2010 when the first MMC based HVDC transmission lines came out for commercial purpose, the Trans Bay project [11]. However, because of the restraints of the DC circuit breakers in high voltage applications, the development of the HVDC transmission lines has been slow until 2012 when ABB has developed the world's first HVDC DC circuit breaker [7]. The topologies of the two-level and three-level converters are shown in Figure 3. There are two DC link capacitors in both the two-level and three-level converters.

The converter output for the two-level converter shown can be either $+V_{dc}$ or $-V_{dc}$, whereas the converter voltage output of the three-level converter includes the 0 states during normal operations. However, it can be observed that the structure of the three-level converter is more sophisticated than the two-level converter, and more components are required for the three-level converter. Because of the large harmonics on the AC side of the converter, based on the two-level and three-level VSC, the multilevel converters were developed, such as diode-clamped converter [25] or flying capacitor converter [26]. However, compared to the MMC, the aforementioned multilevel converter suffers problems such as multiple dc supplies required and the increased control difficulties when the converter voltage levels are higher than five. In contrast, the voltage level of the MMC can easily increase to over 200 by inserting submodule without adding any dc supplies and the only difference of the control method between the low voltage level MMC and high voltage level MMC is the number of the carrier signals required in the PWM scheme.



(a) (b)

Figure 3: The topology of the conventional (a) two-level converter (b) the three-level converter.

1.2.2.Modular multilevel converter

Nevertheless, when referring to the HVDC transmission system, the MMC based transmission line seems to be the only option for the long distance, low losses power transmission. Considering the highly modular submodules, low switching frequency, and low harmonic, MMC could still be one of the promising candidates for UHV transmission lines. The Trans Bay project has set a great example of implementing the MMC based transmission lines by stacking the modular submodules. Furthermore, one of the advantages of the MMC based

transmission lines is the much lower harmonic and switching frequency due to the series-connected submodules. However, due to the physical limitations of the power switch and capacitor, the number of submodules could be large when implementing the UHV applications, thus increasing the initial investment for the construction of the substation. Because of the desirable features of the MMC in high voltage applications, the MMC based HVDC transmission systems are considered as one of the most attractive candidates for long distance power transmission. With the rapid development of the power electronic devices, the MMC based HVDC transmission line is one of the most attractive topologies for a distance transmission system. A typical three-phase MMC has been shown in Figure 4.

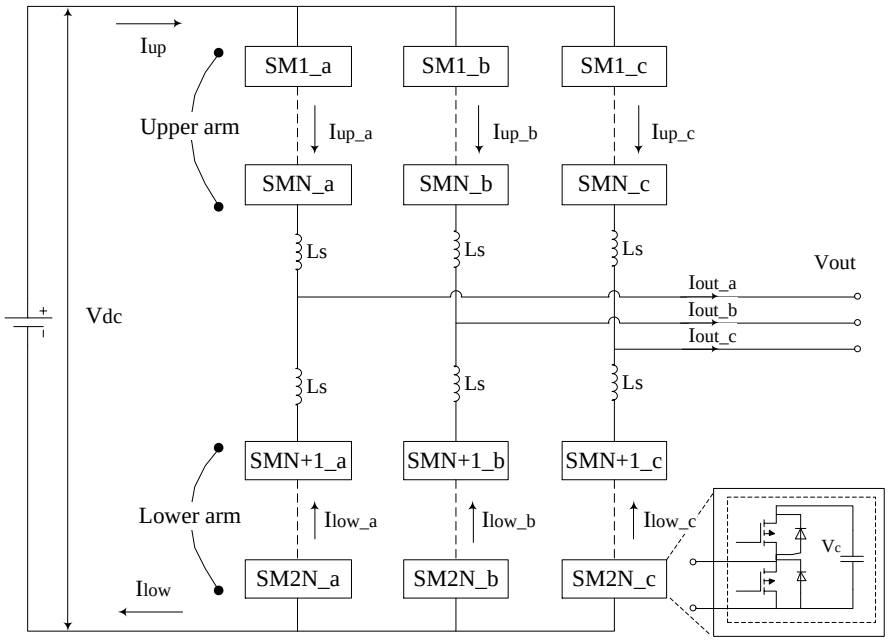
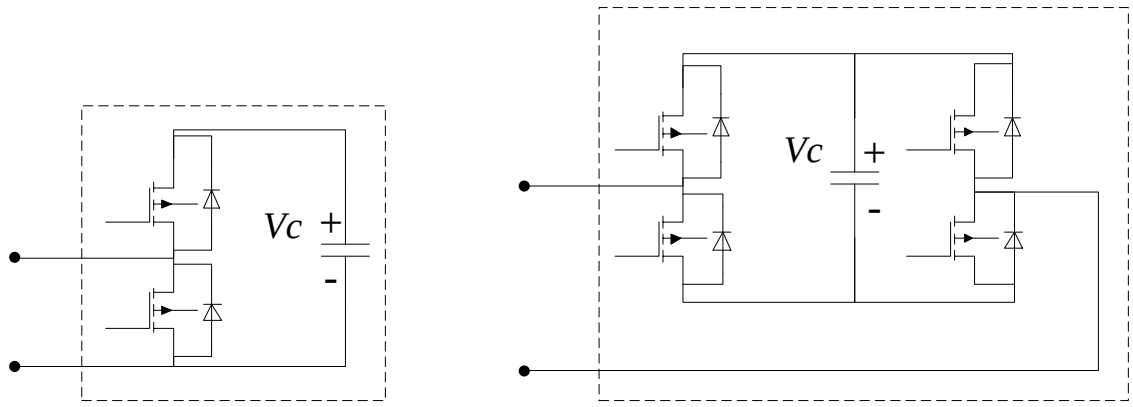


Figure 4: The typical structure of a three-phase MMC.

The modular structure of this converter determines that there are many submodules connected in series in both upper and lower arm. Each arm consists of several identical submodules in order to generate the desired output. The number of the submodule in upper and lower arm are the same. Depending on the structures of the submodules, the implementation of the MMC can have two different topologies as shown in Figure 5.



(a) (b)

Figure 5: The submodule structure of the (a) half-bridge MMC (b) full-bridge MMC.

No matter how many power switches and capacitors are contained within one submodule, as demonstrated in Figure 5, all the submodules in both upper arm and lower arm are connected in series to integrate the converter output. This type of multilevel structure provides higher flexibility and lower control difficulty than conventional two-level or three-level VSC. The performance of the MMC based systems are improved in the following aspects:

a. Lower switching frequency

Because of the series connections in each arm, the converter output voltage is generated by adding and reducing the number of connected submodules in MMC. Therefore, the switching frequency is dependent on the modulation method in the control approach. In the two-level and three-level converter, the Pulse Width Modulation (PWM) is used to generate control signals for the switches [8]. That can cause the frequent switching on and off actions to achieve low harmonic converter output. Nevertheless, in MMC, when the number of submodules is high, the commonly used modulation method is Nearest Level Modulation (NLM), which turns on and off the submodules according to the reference signals by rounding up to the nearest voltage level [27]. Because of the smaller voltage steps of the MMC than the two-level or three-level converter, the NLM approach not only lowers the switching frequency but also maintains the low converter output harmonics. However, the voltage balancing controls are required for the capacitors within all the submodules since they can have voltage deviations if left unattended. In [28], the impact of the control approach on switching frequencies is discussed, and it is shown that the switching frequency of each submodule can be operated less than 150Hz.

b. Low harmonic converter output

Because of the flexible structure of MMC itself, the number of submodules used in each arm does not compromise the control simplicity. With other types of multilevel converters,

such as the diode-clamp multilevel converter or flying capacitor converter, the control patterns can increase exponentially when the number of converter voltage levels is high [29][30]. To extend the benefits brought by increasing the number of submodules, such as the low converter output harmonics, low insulation requirements, etc. The number of submodules for each arm can be as many as 200 or even more. In this case, the converter output is approaching a sinusoidal waveform as increasing the number of submodules, leads to much fewer harmonics than the two or three voltage levels converters. Based on the simulation results, the minimum number of voltage level required to meet the grid code for a 6KV application is 40. However, the number can vary depending on the control approach applied. As a result of the lower AC side harmonics, the size of the AC side filter is reduced, or it is not necessary when the number of submodules is sufficient in each arm [31]-[33].

c. Low component requirement

The voltage distributed on each submodule is smaller than the two-level or three-level converter depending on how many submodules in one arm, which leads to the smaller voltage steps when turning on the submodules. In this case, the voltage differences at the two terminals of the power switches are also small hence reducing the stresses of the power switches in the submodules when the voltage level is high but also generates less electrical magnetic interferences due to the low switching frequency [34][35].

1.2.3.Other potential converters

Depending on the application of the HVDC transmission lines, there are other types of converters that have the potential to be implemented in the HVDC transmission system. In Figure 6, the topology of a multilevel matrix converter is shown. There are many bi-directional power switches connected in each arm to achieve the AC-AC energy conversion. However, in the matrix converter, the power storage components, such as capacitors, are not necessary as stated in [36]-[38]. Because of the rapid development of the power switches, the cost and efficiency are both improved through the past a few years. These converters which are using a large number of power switches are becoming more and more competitive in high voltage applications. Despite the available converters for HVDC applications, the half-bridge structure MMC is widely accepted for its control simplicity and the fewer number of components used than the rest converters.

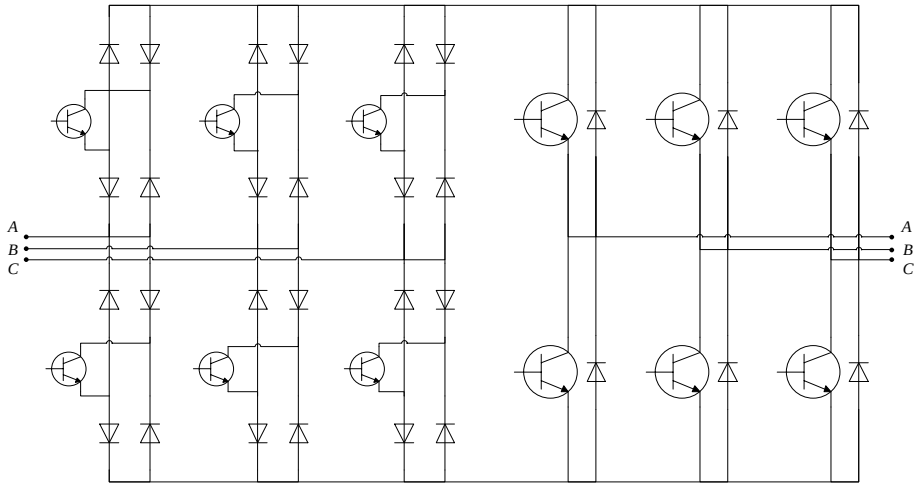


Figure 6: The topology of the matrix converter in a back-to-back application.

1.3 Research background of the MMC

Because the power consumption is increasing over the past decades. It is critical to find a solution to the high losses and low efficiency of the traditional three-phase transmission system. In this case, the HVDC transmission system is the ideal choice for the distant and offshore power transmission. In this chapter, the construction costs for both AC transmission system and DC transmission system is analysed and the idea of critical distance is introduced to demonstrate the point where DC transmission line is more cost efficient than the AC transmission line. In addition, the commonly used types of converters are investigated in this chapter. The modular multilevel has shown a mature structure than the latest matrix converter and it also shows the higher flexibility and better performance than the traditional two-level or three-level converter used in HVDC transmission system. Therefore, the MMC based HVDC transmission system is the one of the most appropriate candidates for distant and low losses transmission system

1.3.1.Mathematical representations of MMC

The mathematical representation of the MMC can precisely describe the behaviour of the MMC during the normal operation. However, the modelling methods of the MMC are different depending on which aspects of converter behaviour are of interest. Fundamentally, the models provide the voltage and current pattern of the converter according to the control approach. Some models are focusing on the switching losses and heat generation for converter efficiency assessment. Song and Liu created a mathematical model in [39] to describe the circuit interactions of the electrical quantities in the MMC. By simplifying to a simple key equation, this mathematical model focuses on the steady states of the MMC. The high-frequency

current components are extracted from the arm currents for voltage balancing control as suggested in [40] by Deng and Chen. However, the PWM method is limited to the Phase-Shifted PWM (PS-PWM) which can significantly increase the computation requirements when the number of submodules is large. To simplify the computation processes, the arm submodules are replaced by the equivalent controllable voltage sources in [41]. Inner voltages are introduced to represent the voltage changes across the submodules. This approach is preferred in the MMC control design when there are a large number of submodules in each arm. The lack of descriptions of the switching actions in this approach makes this modelling method inaccurate when the converter efficiency is of consideration. On the other hand, to describe the detailed model, the sensor delays are considered to control the current within the MMC arms [42]. Disturbances and harmonic compensation control can be injected into the reference signals to achieve the control of the positive, negative, and zero-phase-sequence converter currents control [43].

One of the problems when building the simulation model is that when the number of the submodules in each arm is increased, the computation requirement is also increased. Therefore, accurate and efficient modelling methods for multilevel level converters are required. An average-value-model of the 401-voltage level MMC based HVDC transmission system is given in [31]. The arm submodules are replaced by the controllable current sources to reduce the computation requirement as well as evaluating the converter performance. The Thévenin's equivalent equations for the converter part were given in [35] based on the predefined equations provided by manufacture. It does not require the exact equivalent model of the entire circuit. Therefore, the computation requirement is relatively low in this model. The comparisons among the leading approaches in modeling the MMC has been demonstrated in [44], an improved model is also presented to further improve the computational efficiency regarding the electromagnetic transient simulations. As stated in [44] , while both average model and detailed equivalent model can offer great accuracy regarding the electrical-magnetic analysis, the detailed equivalent model is more accurate than the average in the same conditions and both of them are more accurate than the traditional detailed model. However, the electrical-magnetic interferences are not investigated in the simulation model. The MMC simulation model was designed and tested in MATLAB to validate the proposed control approaches.

1.3.2.Control signal modulation method

The modulation methods for MMC are similar to the traditional modulation methods except that the number of the PWM carriers is more than that for two-level or three-level converters. When the number of submodules is large, the modulation complexity and the computation requirements of the control approach are greatly increased. The Space-Vector PWM (SV-PWM) was initially used to test the MMC [45]. Depending on the number of the submodules, the number of the switching states can be massive when the converter has more submodules than traditional two-level or three-level VSC based systems. The Phase-Shifted PWM (PS-PWM) and Phase-Disposition PWM (PD-PWM) are then employed to simplify the modulation processes. Their effectiveness is validated by both simulation and experimental results. The closed control loops are connected to the submodules to control the capacitor voltages [46]. This approach skips the capacitor voltage sorting, but at the cost of adding more control blocks. The capacitor voltage balancing approach based on the PD-PWM was suggested in [47][48]. However, the voltage sorting process and the monitoring of the arm currents and capacitor voltages are always the barriers of improving the MMC control approaches. In [40], the equations for the high-frequency current components in the arm currents were derived when the PS-PWM is used for modulation. The advantage of this approach is the measuring of the arm current is not necessary to control the capacitor voltages. On the other hand, it has the same problems regarding the computational stress as the conventional voltage balancing approaches when there are a large number of submodules in each arm., The Nearest Level Modulation (NLM) is proposed in [27] to cope with the increased voltage levels taking into account that the PWM effects are not significant as when the converter voltage level is low. The submodule numbers are determined by integrating the closest voltage according to the reference signals. However, the approximation of the NLM can generate many converter voltage harmonics when the number of submodules is insufficient. In [49], the switching states are simplified at the implementation stage of the NLM to shorten the necessary computation period. The comparisons between the Space Vector Pulse Width Modulation (SVPWM) and the NLM are presented in [53]. It has proven that the SVPWM can be equivalent to the NLM approach by selecting the appropriate redundant switching sequence. However, it is easier to modify the SVPWM switching pattern than the NLM to provide more flexibility to the system.

The converter output voltage harmonics exist no matter which PWM scheme is selected. Especially when the converter voltage level is low, the converter harmonics can be significant

depending on the number of the submodules. The Selective Harmonics Elimination (SHE) approach is proposed in [50][51] to minimize the converter output harmonics. However, the look-up table can be sophisticated even with only a low number of submodules connected. In [52], the converter output is increased from N+1 to 2N+1 by interleaving the carriers, which involves shifting the carriers by 180^{o}. The interleaving technology can increase the voltage levels as well as reduce the converter output harmonics without adding more submodules. However, this modulation potentially increases the imbalanced voltage distributions on the arm inductors, hence increasing the power rating of the affected components.

1.3.3.Selection of the arm inductor and submodule capacitor

The one of the major costs of the MMC based system is the cost for the submodules. Because of the modular structure of the MMC, each submodule contains the same number of switches and capacitors. The selection of the capacitor affects both the size and the cost of the converter [55] since the performance of the converter is determined by the capacity of the selected capacitors. Depending on the system requirements, the capacitance selections are focusing on these two factors: the capacitor voltage ripple and the maximum energy stored in the capacitors. The capacitor voltage ripple should be low to reduce the converter output harmonics, and on the other hand, it should be capable of transmitting the rated power from side to side. Besides that, the capacitors are selected considering the maximum capacitor voltage, voltage ripple, current ripple, and the submodule voltage capability of the converter [54]. Hence four equations are derived to suggest the upper and lower margins of the submodule capacitances. On the other hand, the capacitance can be determined based on the voltage ripple generated by the switching actions [9]. The maximum power storage in the submodules is another key factor should be taken into account. In order to illustrate the relationships between the converter rated power and the maximum power transmitted, the energy-power ratio was introduced in [56] to guide the selection of capacitor. The ratio between the power stored in the submodules and the power transferred through the MMC from 10 to 50 produces the best performance. On the other hand, because of the existence of the arm inductors, the resonances are investigated to determine the capacitance and inductance in [57]. The second and fourth harmonics of the arm currents are investigated, and the capacitance and inductance are selected in order to avoid the low-frequency resonances. Because of the low order harmonics generated by the series-connected capacitors and the inductors, the elimination of the resonant current existing in the arm currents can be another determining factor in the arm inductor se-

lection. In [58], it presented the principles of selecting the arm inductances based on the equations for the circulating current at switching frequency when the circulating current suppression control is activated. The resonance current generated by the submodule capacitor and arm inductors are investigated in [56], the system parameters of the other nineteen different projects are presented to illustrate the resonance currents existing at the second and fourth harmonics. However, the arm inductors are also in charge of limiting the fault current whenever there are system failures. The equations for the arm inductance were derived in [59] based on the variation speed of the fault current which is related to the power switches. To further improve the selection of the arm inductance, the fault current limiting effect of the arm inductor and an Active Front-End (AFE) mode of the MMC were suggested in [57] to minimize the use of the passive components, hence reducing the size of the submodule capacitors and the arm inductors. However, in the AFE mode, the arm inductance was compensated by the AC side filter which may lead to the size increasing of the AC filter.

1.3.4.The external control loop

The conventional VSC control loops are well developed, and it can be implemented in the MMC based HVDC transmission systems with little modifications. The AC side dynamics of the MMC based system was deduced in [60], theoretically approved the exterior control design of the traditional two-level VSC can be applied to the AC side of the MMC. Therefore, the active and reactive power decoupling control loops used for two-level VSC are eligible control methods for MMC. The output on the AC side of the MMC is integrated by turning on the submodules one by one according to the reference signals [61]. A large number of the submodules can provide high flexibility when there are one or more submodules failures. In [62], the redundant submodules are inserted into the arms to reduce the switching frequency and the capacitor voltage ripple, and the AC side voltage dynamics are also derived. The control of the AC side of the MMC can be achieved by decoupling the capacitor voltages with 10% redundancy submodules to simplify the switching processes and improve the computational efficiency [63]. As the extension of the MMC-based HVDC transmission lines, the direct power control can be applied to the MMC to enable the bi-directional power flowing through passive networks [64]. Besides the conventional outer VSC power control loop, the circulating currents are considered as the third variable to improve the performance of the MMC in the proposed control technology [65].

1.3.5.The internal control loop

The internal control approach of the MMC is different from the traditional two-level or three-level VSC because of the series-connected submodules. Since the capacitors in the submodules can have voltage differences even with voltage balancing controls, they can cause circulating currents to flow in the arms. Therefore, the capacitor voltage balancing and the circulating current suppression are primary control loops for the internal control of the MMC.

Depending on the measurement of the arm currents, the voltage balancing control is developed on a different basis. One of the approaches is to measure the arm currents of both upper and lower arms, and determine the turn-on and turn-off states of each submodule depending on the arm current directions. In [47], the arm currents are measured to predict the charging and discharging states of the affected submodules to improve the switching patterns. A double-fundamental frequency disturbance is injected into the reference signals to minimize the converter output harmonics. On the other hand, because the capacitor voltages are transferred to the control unit and processed according to the arm current directions, they can have a great impact on the switching frequency of each submodule, hence affecting the converter performance [67]. Therefore, the switching frequency can be reduced by inserting the submodule on and off states as the third variable [68]. This method can be implemented in arm current measurement based voltage balancing control to minimize the switching frequency [69][70]. In [71], the discrete mathematical model is derived, and the cost functions are pre-defined to balance the capacitor voltage. Due to its computational difficulty and the measuring redundancy, the following approaches are proposed to simplify the control process. In conventional voltage balancing control approach, the arm currents are always measured to ensure the balanced voltage distribution among the capacitors. However, it is possible to skip the arm current measuring process by improving the voltage balancing methods, such as the following voltage balancing methods. The DC voltage distribution can be controlled by adding control loops to every submodule, the capacitor voltage variations are restricted within the certain range by the control loops [46]. Because the extra control loops are required for every submodule, the implementation costs can be significant when there are many submodules. The equations for the high-frequency components of the arm currents based on the switching actions were derived in [40] to balance the capacitor voltages. The submodule voltages are controlled according to the power variations caused by the high-frequency current components. The capacitor voltages can be controlled by the energy balancing control from the power transmitting aspect as derived in [72][73]. The differential currents of the positive, negative, and zero sequences at

fundamental and twice-fundamental frequencies can be decoupled to regulate the energy distribution in both upper and lower arms [72]. The DC voltage and the AC side output currents can be measured to estimate the energy distribution among the submodules in the converter to fit different load conditions [73].

The circulating current is one of the side effects caused by the imbalanced DC voltage distributions. Because there are submodules connected in series, the imbalanced DC voltage distributions can generate currents flowing from upper arm to lower arm or from one phase to another phase. It can increase the RMS current ratings of the affected components and increase the switching losses. In [74], it describes the generation of the circulating current based on the instantaneous power flowing and suggests that the circulating current is proportional to the capacitor voltage differences. Therefore, it can be suppressed by decoupling the differential current to generate the corresponding control signals to compensate the capacitor voltage difference. The circulating current model of the MMC was proposed in [75] and it proved that the upper and lower arm controls are independent of each other and hence the communications between these two controls are not required. The paper also showed that the circulating current consists of the Direct current and the phase-to-phase average currents. However, the circulating current suppression methods can be different based on the different arm current decoupling methods. In [76]-[79], the circulating current suppression is focused on eliminating the alternating current by regulating the Direct current components in the circulating current. In [76], repetitive controllers are inserted into the suppression controller to improve the converter immunity to current harmonics and increase the efficiency of the controller. The alternating current components of the circulating current can be decoupled and the corresponding controllers can be designed to reduce the even order harmonics by tuning at the even order frequencies [77][78]. In [79], it improves the circulating currents suppression control under unbalanced grid conditions and further guaranteed the feasibility of this approach in different circumstances. In [80], it proposes the direct circulating current suppression method incorporating the half-delayed operation cycle to suppress the even order harmonics existing in the circulating currents, the results demonstrated the fast responses regarding system dynamics. In [81], it develops the quasi-proportional controller focusing on eliminating the second-order harmonics existing in the circulating currents, which combines the benefits of the AC circulating current suppression and the circulating current decoupling methods. In addition to the approaches of regulating the circulating current to the DC components, the circulating current was decoupled to extract the elements of the circulating current at the specific frequency [82][83]. In [82], it has derived the steady state model of the MMC to describe the circulating

current and the performance of the converter affected by inserting the submodule according to the sinusoidal reference signals. The resonant frequency in the steady state model indicated that the circulating current contains a large component of the AC currents at the twice fundamental frequency. In [83], the circulating current suppression method was designed based on the rotating frame of the arm currents at the fundamental frequency. The suppressing signals are generated and applied to the upper and lower arm separately because the controls of the upper and lower arm are independent of each other as described in [75]. In [84] , it applies the proposed approach in [83] to a 71-level MMC model, and further investigated the performance of the system with the aforementioned approach.

1.3.6.The converter efficiency and performance under fault conditions

A large number of submodules results in the lower switching frequency than the traditional two-level or three-level converters. However, due to the voltage balancing and the circulating current controls, the switching states of each submodule are difficult to track when the system is in operation. In [85], it derives the equations representing the on-state losses for the MMC based on different system capacities. The temperature coefficients of the power switches are presented using curve fitting to calculate the losses. The mathematical analysis of the MMC regarding both conduction losses and the switching losses is presented in [86], and the results are compared to the MATLAB equivalent model. The results are promising in regard to the conduction losses but not the switching losses. The loss calculation is linked to the junction temperature of the switch directly thus affecting the overall system designs. To precisely describe the losses in different frequency ranges, the accurate system model was derived based on the approximate calculation tools provided by the manufacturers [87]. The duty ratio of each submodule is considered and the switching temperature is estimated according to the theoretical maximum switching frequency.

Because of the unfavourable conditions of using the average DC circuit breakers in the HVDC transmission systems [88]-[90], ABB managed to develop the first applicable HVDC DC circuit breaker in 2012. In [91], the line-to-line and line-to-ground faults are investigated and the transient electromagnetic transient of characteristics of the MMC was analysed. The simulation results indicated that the MMC-based HVDC systems have better controllability than the conventional VSC-HVDC systems. The fault-tolerant operation with redundant submodules was proposed in [92] when the failures are detected inside the submodules. The proposed method was carried out based on the PSCAD model and proven to maintain a constant power transfer when the number of faulty submodule exceeds the total number of redundant

submodules. In [93], a clamp circuit structure for the MMC was developed which has the ability to block the DC fault. This is similar to the full-bridge MMC but using 33% fewer semiconductors thus less conduction losses.

1.4 Research contribution

1.4.1.Mathematical model

The mathematical model of the MMC is used to describe the converter behaviour during the regular operation. The proper selected mathematical model can precisely define the switching losses, the junction temperature of the power switches, or the electromagnetic interference generated by the high speed switching action. Since they are derived from the fundamental theoretical model of the MMC, the common mathematical model was derived by inserting controllable voltage or current sources to reveal the controllability of the MMC. It has been proven that the conventional VSC control approach can be used in the control method for MMC. The outer power control loop and inner current loop are provided to guide the design of the MMC modelling and control. The average MMC model is built in MATLAB to verify the proposed mathematical model. The junction temperature and the electromagnetic interferences are not considered in the simplified model**.**

1.4.2.The modulation methods

Because of the series-connected structure of the MMC, the modulation methods are based on the sinusoidal methods. In the PWM methods used for MMC, the number of the carriers can be as same as the number of the submodules depending on the structures of the submodules. Therefore, the computational requirement of generating the PWM is high when there are many submodules in each arm of the MMC. The implementation of the PWM methods is provided, and the comparison among the Phase Shifted Pulse Width Modulation (PS-PWM) and Phase Disposition Pulse Width Modulation (PD-PWM) are presented. The interleaving technology is also discussed to illustrate the benefits and the drawbacks of such modulation methods. The hardware implementation of the PWM is also shown to demonstrate the realization of selected PWM in the control unit for MMC**.**

1.4.3.The capacitor voltage balancing control

A large number of the submodules provide smaller voltage steps and lower converter output harmonics on the AC side of the converter. However, similar to the conventional multilevel converters, such as the diode-clamped converter or flying capacitor converter, the MMC

can have problems caused by the imbalanced voltage distribution among the submodules. The magnitude of the current, the turn-on and turn-off period, and the effects of the sampling frequencies affect the voltage distributions across all the capacitors in the submodules. The dynamic capacitor voltage monitoring of all the submodules and the arm currents are required to balance the energy distributions. Therefore, the conventional voltage balancing processes can be slower when the converter submodules are more than the conventional multilevel converter. However, one of the advantages of the MMC is the large number of the submodules in each arm. Thus the benefits of reducing the complexity of the voltage balancing control can be significant. The predictive voltage balancing control is proposed to further simplify the voltage balancing processes. Compared to the conventional voltage balancing control, the predictive voltage balancing control has a better performance at the same sampling rate and the current measurement is not necessary as the control approach is improved. On the other hand, the effects of the communication delays between the circuit and the control unit can also be minimized. It makes it much more favourable in the Ultra High Voltage (UHV) applications for its fast and simple control approach. However, the arm currents are still required to be monitored to achieve the circulating current regulation in the circulating current suppressing control.

1.4.4.Circulating current suppression control

The circulating current is caused by the imbalanced capacitor voltages of the upper and lower arms and the resonance currents generated by the arm inductor and capacitors. Because this current flows among the arms of the MMC, it can increase the stresses of affected components hence increasing the power rating of the components and initial investment regarding the submodules. The implementation of the arm inductor can suppress the circulating currents, but that will affect both the size and the investment of the power plant. In that case, the generation of the circulating currents according to the mathematical model is investigated, and the suppression method is developed. The proposed circulating current control is based on regulating the circulating current to its DC components to minimize the AC components which are at the double-fundamental frequency. Its simplicity and fast response to the dynamic changes are favourable in MMC when the number of the submodules is significant. As a result of the suppression control, the circulating current harmonics at the switching frequency are observed while most of the AC circulating current at the twice fundamental frequency are eliminated. Both simulation and experiment results demonstrated the effects of the circulating current suppression approach in eliminating the most of the AC components and

reducing the capacitor voltage ripples. Because the voltage ripple in the capacitors are smaller than before applying the suppression control, the converter output can have smoother voltage patterns which lower the converter harmonics on the AC side. This results in further lowering the requirement of the AC side filter and reducing the costs.

1.5 Publications raised from the works

In summary, work has been done to explore the feasibility of improvements to the MMC-based system in high voltage applications. The mathematical model verified that the external control loop and the internal control loop employed in regular VSC-based systems could be applied to the MMC-based system with moderate modifications. The realization of the control signals is achieved by two different types of the PWM, PS-PWM and PD-PWM separately. The results and discussion of the advantage and disadvantage of each PWM methods are published in [13]. Description of the advantages and disadvantages of each PWM method regarding the control logic, sampling frequency, and the implementation difficulty concerning the voltage levels are also presented. The proposed voltage balancing approach focused on the sampling of the voltage readings of the submodule capacitors to improve the accuracy and building strong immunity to the sampling disturbances. The discovery of the proposed capacitor voltage balancing methods is presented in the publications published in [14].To further reveal any potential conflicts between the proposed voltage balancing approach and the other control approaches required in the MMC control system, the two-terminal MMC based HVDC model based on MATLAB was designed and tested. The simulation results for a 40-level MMC-based HVDC system demonstrated the small level of harmonics on the AC side of the converter. The Total Harmonic Distortion (THD) levels are compatible to that as specified in the Grid code. In addition, an experiment model was also designed, and the promising results further demonstrated the suitability of the proposed approach.

The following chapters are arranged as this: In chapter II, the modelling and selection of the vital components are presented and discussed, because the performance of the converter are majorly determined by the capacitor inside the submodule and the in-series connected inductors. In chapter III, both modulation methods are presented and discussed due to they are the most popular modulation methods used in MMC based systems. The results have shown the advantage and disadvantage of each modulation methods regarding the response time, the harmonics generated, and the difficulty of designing. In chapter IV, the capacitor voltage balancing method is proposed. As the improved method, the proposed voltage balancing method

is considered more convenient and precious compared to the traditional voltage balancing method. In chapter V, the investigation of the circulating current is presented to identify the controllable variables, it turns out the power transmitted through the converter is one of the key factor affecting the circulating current. Based on that conclusion, the improved circulating current suppressing control is provided and presented in later chapter. To further verify the validation of the proposed control methods, the design and experiment results are presented in chapter VI, and the conclusion of this thesis are presented in chapter VII.

Chapter 2

Converter modelling and parameter selection

2.1 Introduction

As one of the most attractive candidates for a HVDC transmission system, the MMC has potential to improve the efficiency regarding the control system [94]-[105]. One of the advantages of the half-bridge MMC is that fewer components are required compared to the conventional multilevel converter. The comparisons between the MMC and the other types of multilevel converters indicated that the MMC is 50% more efficient than the best of the other multilevel converters especially when the voltage levels are high. On the other hand, because of the fundamental differences between the MMC and the other types of the multilevel converters, the control approach for other multilevel converters such as the diode-clamped converter or flying capacitor converter are not applicable in MMC. Therefore, a mathematical model was built to examine the control variables for accurate and efficient control. The internal voltage variables for both upper and lower arm are introduced to control the MMC.

2.2 Modelling of the MMC

The half-bridge MMC is one of the multilevel converter topologies using a small number of passive components and power switches but still maintaining a reliable converter output. As shown in Table 3, the numbers of components employed in different types of multilevel converter are listed. The commonly used multilevel converter are divided into three different types, the diode clamp converter, the flying capacitor converter, and the modular multilevel converter, which is a special cascaded multilevel converter. As multilevel converter, the diode-clamped converter is using diode to block and conduct the current flowing. The flying capacitor converter is using power switches to control the current flowing. Similar to the flying capacitor converter, the MMC is manipulating the current following by turning on and off each submodule. As seen in Table 3, the number of the main switching devices and main diodes for all three types of multilevel converters are the same. However, the diode clamp converter uses more clamping diodes than the other two types of converter because of the internal connection of this type of converter. On the other hand, the diode clamp converter can only have half number of the DC bus capacitor than the other two types of converter. The flying capacitor converter has the same problem as the diode clamp converter because it uses more balancing capacitor than the other two types. Therefore, the MMC uses the least number of

component compared to the other two types of multilevel converter. Above all, the sophisticated control approaches of the diode clamp and flying capacitor converter when the output voltage level is large is also one of the important reason why MMC is preferable in high or ultra-high voltage applications.

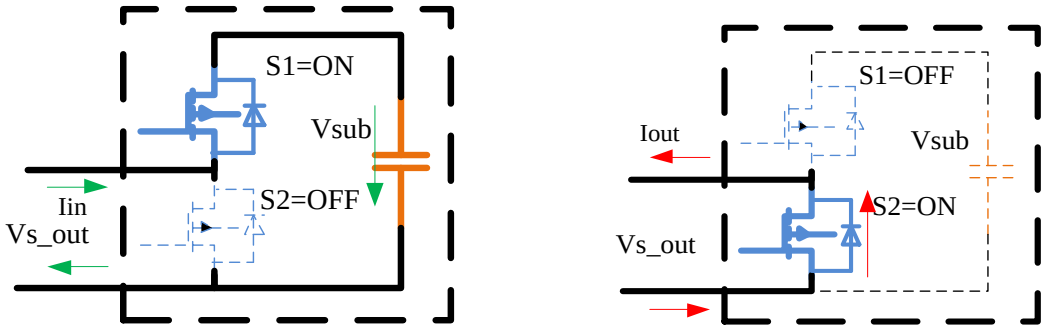
Table 3: the component used in different types of multilevel converter

Converter Type	Diode Clamp Converter	Flying Capacitor Converter	Modular Multilevel Converter
Main Switching devices	$(N_{level}-1)\times 2$*	$(N_{level}-1)\times 2$	$(N_{level}-1)\times 2$
Main diodes	$(N_{level}-1)\times 2$	$(N_{level}-1)\times 2$	$(N_{level}-1)\times 2$
Clamping diodes	$(N_{level}-1)\times(N_{level}-2)$	0	0
DC bus Capacitors	$N_{level}-1$	$(N_{level}-1)\times 2$	$(N_{level}-1)\times 2$
Balancing Capacitors	0	$(N_{level}-1)\times(N_{level}-2)/2$	0

*: N_{level} is the number of the converter output voltage levels.

In each arm of the MMC, the number of the submodules connected in series is N. This is decided by the system requirements regarding the converter output harmonics and the requirements of the components. Inside the half-bridge submodules, there are two power switches, and one power capacitor connected as demonstrated in Figure 7. The I_{in} and I_{out} are the current flowing into the submodule when it is in on mode and the current flowing out the submodule when it is in off mode separately. Also, the directions of the current flowing through the submodule are labelled for the submodule in different mode. Figure 7 demonstrates the currents flowing of the submodules when it is in on and off-states. When the submodule is in on-mode, the capacitor inside the submodule is connected to the circuit in series. Therefore, the output of the submodule V_{s_sub} at this moment is equal to the capacitor voltage V_{sub}. Otherwise, the submodule is in off-mode, and the circuit is bypassing the capacitor. Hence the output of the submodule is zero. In addition to the two normal states of the half-bridge submodule, there is one more state when the capacitor is connected to the circuit in reverse polarity for the full-bridge submodule. Such a connection is providing a state where the output of the submodule is equal to negative capacitor voltage, which provides additional control flexibility [94]. However, it uses twice as many as the power switches to that used in the half-bridge structure hence the initial investment regarding the switching device is doubled. The

primary barrier of completing the other structure, such as hybrid or sharing arm inductors, is the sophisticated structure and the relevant control approaches which require additional effort designing the control strategies compared to the other types of MMC structure [95].



(a) (b)

Figure 7: Arm current flowing when the submodule capacitor is (a) connected to the circuit (b) in bypassing mode.

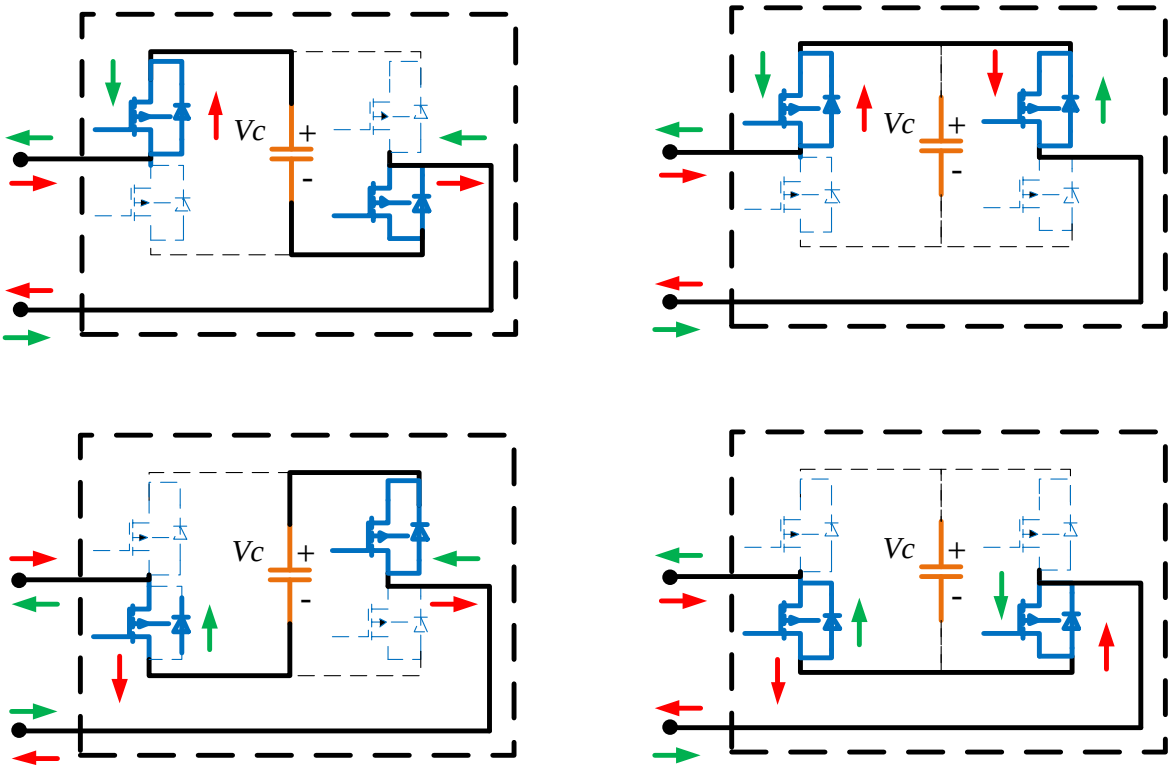


Figure 8: The on/off states of the full-bridge submodule

The control of the MMC depends on the realization of the reference signals and the generation of the gate signals. The mathematical model is developed to describe the voltage and current characters of the MMC as well as to determine the controllable variables in the MMC. However, the detailed model of MMC based on the detailed physics-based models requires much smaller time steps to achieve the accuracy [103]. This type of modelling is not usually employed in power system simulations due to its high computational requirement. The commonly used method involves modelling the converter by replacing the upper and lower arms with the controllable voltage and current sources [104]-[106]. As shown in Figure 9, based on the characters of the PWM control, the upper and lower arm voltage can be approximated as two sinusoidal voltage sources in each phase.

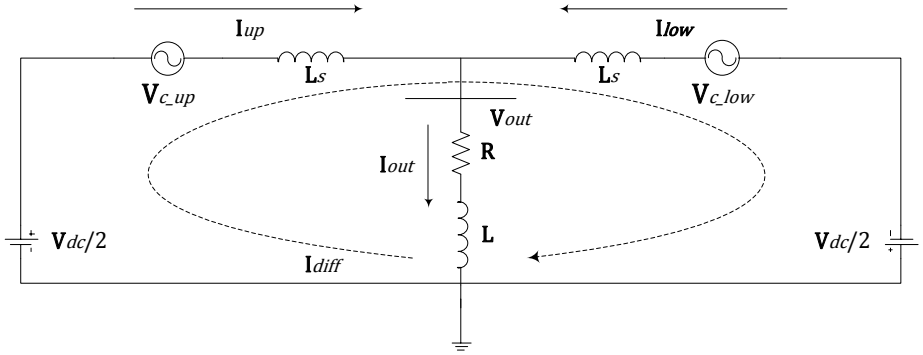


Figure 9: The equivalent model of the MMC

This type of modelling is based on the assumptions that the power switches are ideal, the turning on and off resistances of the power switches are integrated with the arm resistance. Because the turning on and off of power switches are ignored in this model, it is not applicable when the switching loss and junction temperature of the power switches are required. For accurate models, there are other modelling methods such as simplified IGBT-based models and detailed equivalent circuit based models. They are usually used to verify the conduction loss and thermal analysis and required high computation resources.

In Figure 9, the equivalent circuit of the MMC is connected to a passive load consisting of R and L. The upper arm and lower arm of the MMC are linked in parallel with the DC voltage sources which represents the transmission lines. Both of the upper and lower arm submodules are replaced by controllable voltage sources, the mathematical representation of the output voltage V_{out} at the common coupling point is shown in (1) and (2).

$$V_{out} = \frac{1}{2}V_{dc} - V_{c\_up} - L_s \cdot \frac{dI_{up}}{dt} \quad (1)$$

$$V_{out} = -\frac{1}{2}V_{dc} + V_{c\_low} - L_s \cdot \frac{dI_{low}}{dt} \quad (2)$$

In (1) and (2), where V_{out} is the output voltage on the AC side, V_{dc} is the DC voltage on the DC side of the converter, V_{c_up} is the upper arm equivalent voltage, V_{c_low} is the lower arm equivalent voltage, L_s is inductance of the arm inductor, I_{up} is the upper arm current, I_{low} is the lower arm current. Combing (1) and (2), there are

$$V\_out = e_j - \frac{L_s}{2} \cdot \frac{(d(I\_out))}{dt} \quad (3)$$

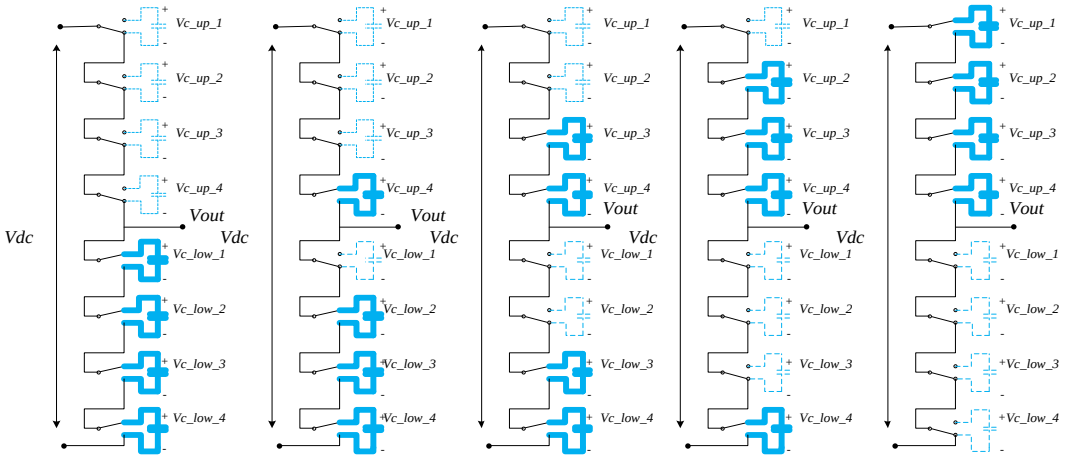
$$V_{dc} = V_{c\_up} + V_{c\_low} - L_s \cdot \frac{d(I_{diff})}{dt} \quad (4)$$

The inner voltage e_j of the MMC is defined to describe the converter output voltage in (3). The differential current flowing among the arms I_{diff} is also shown in (4). The definition of e_j and I_{diff} are shown in (5) and (6):

$$e_j = \frac{V_{c\_up} - V_{c\_low}}{2} \quad (5)$$

$$I_{diff} = \frac{I_{up} - I_{low}}{2} \quad (6)$$

The converter output on the AC side is described in (3), the converter output is affected by the inner voltage e_j and the AC side output current I_{diff}. Hence the conventional outer current loop can be applied to the MMC by manipulating the inner voltage e_j. Derived from (5), assuming the converter output is an ideal sinusoidal waveform, the reference signals for both upper and lower arm controllable voltage sources can be rewritten as demonstrated in (7) and (8).



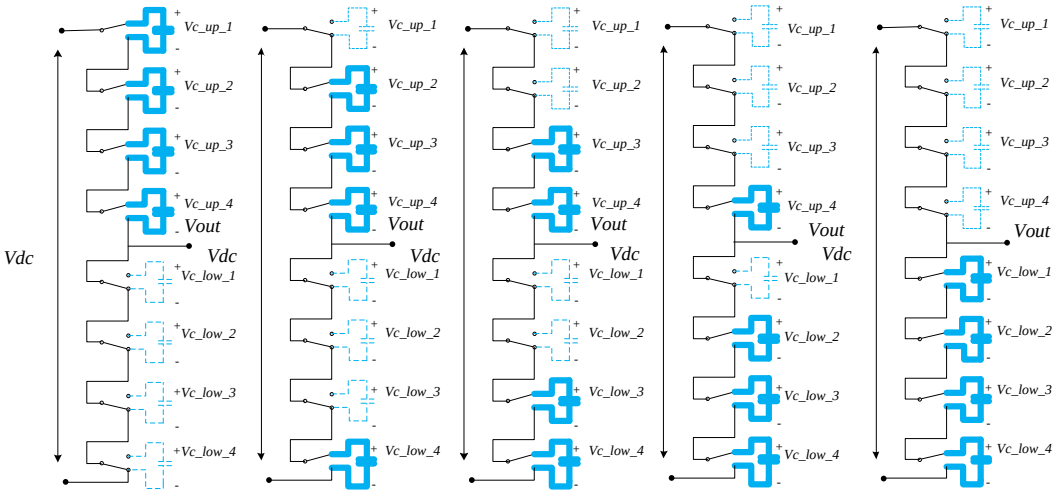


Figure 10: Representation of the voltage steps in MMC

The DC voltage is distributed among the upper and lower arm submodules and the two arm inductors. At any given moment during normal operation, the number of the turning on and the turning-off submodules is constant. Therefore, the DC voltage can be distributed evenly among all the submodules independent of which submodules are turned on and off. However, the interleaving technology which is used to improve the converter output voltage from N+1 to 2N+1 has a modified PWM pattern. The number of the tuning-on submodules and the turning-off submodules is not constant which leads to the imbalanced voltage distribution. Therefore, the constant number of turning on and off submodules provides a more stable system than the interleaving technology. The voltage integration effects of the submodules on the AC side of the converter are demonstrated in (7) and (8).

$$V_{c\_up}^{*} = \frac{1}{2}V_{dc}(1 + MI\sin(\omega_0 t + \varphi)) \quad (7)$$

$$V_{c\_low}^{*} = \frac{1}{2}V_{dc}(1 - MI\sin(\omega_0 t + \varphi)) \quad (8)$$

According to (7) and (8), the reference signals in the upper arm and lower arm are both sinusoidal signals when connected to the passive load. The realizations of the reference signals for the upper and lower arm submodules are depending on the switching states of each submodule. In (7) and (8), where $V_{c\_up}^{*}$ is the control signal for the upper arm, $V_{c\_low}^{*}$ is the control signal for the lower arm, MI is the modulation index, ω_0 is the fundamental rotating speed, and φ is the phase angle. In the single-phase simulation model, (7) and (8) are the reference signals when the converter is connected to passive loads. The reference signals are

obtained based on the outer PQ control loop in the three–phase, two terminals transmission system. Therefore the generation of the reference signals can be different depending on the system configuration.

$$V_{c\_up} = N_{c\_up1}V_{c\_up1} + N_{c\_up2}V_{c\_up2} + \cdots + N_{c\_upN}V_{c\_upN} \quad (9)$$

$$V_{c\_low} = N_{c\_low1}V_{c\_low1} + N_{c\_low2}V_{c\_low2} + \cdots + N_{c\_lowN}V_{c\_lowN} \quad (10)$$

The voltage sources in the upper and lower arm in (1) and (2) can be rewritten as in (9) and (10), where $N_{c\_up1} \ldots N_{c\_up\mathrm{N}}$ are the switching states of the submodule in the upper arm, $N_{c\_low1} \ldots N_{c\_lowN}$ are the switching states of the submodules in the lower arm, $V_{c\_up1} \ldots V_{c\_upN}$ are the capacitor voltages of the submodules in the upper arm, $V_{c\_low1} \ldots V_{c\_lowN}$ are the capacitor voltages of the submodules in the lower arm. In Figure 10, the voltage stepping effect is shown as evident from (9) and (10). The on/off states of each submodule are changing all the time, but the number of the turned-on and turned-off submodules is constant as shown in Figure 10. The voltage integration approach provides the control flexibility. By just adding more submodules to each arm, the voltage level of the converter output can be increased. Therefore, the voltage steps are reduced to lower the converter output harmonics. However, the capacitor voltage is dynamic since the current flowing into the submodule is varying depending on the switching states and the direction of the arm currents.

Initial research shows that, without voltage balancing control, unacceptable deviations of the capacitor voltages are observed, leading to one or more of the capacitors becoming overcharged. Therefore, besides the reference signals provided in (7) and (8), the voltage balancing methods are required to keep the capacitor voltages within limits. According to grid code [107], the nominal voltage level for medium and high voltage applications are to stay within 90% and 110% of their rated voltage. 10% voltage variation on the AC side of the converter reflects that the capacitor voltage in the submodule can have up to 10% voltage difference. The threshold of the capacitor voltage variation is set at 10% to validate the proposed control approaches.

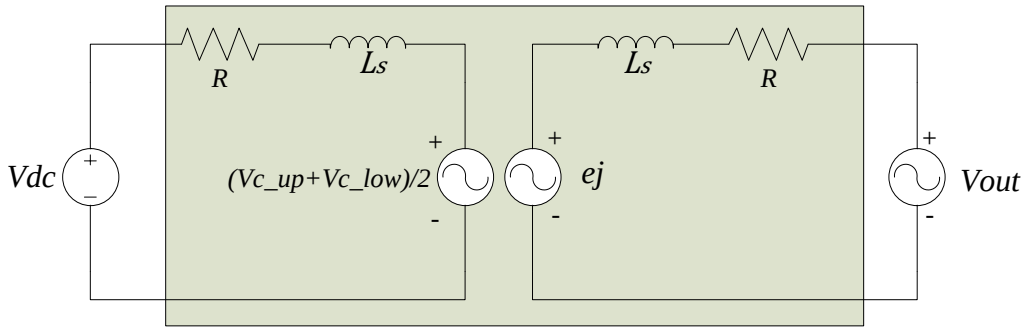


Figure 11: The equivalent decoupling circuit of the MMC.

As demonstrated in Figure 11, the power transmission through the MMC is based on the control of the inner voltage. Combining (1)-(6), the reference signals applied to the upper and lower arm can be rewritten as (11) and (12):

$$V_{c\_up} = V_{dc} - e_j - V_{diff} \quad (11)$$

$$V_{c\_low} = V_{dc} + e_j - V_{diff} \quad (12)$$

The control of the MMC is the realization of the reference signals and the gate signals. Therefore, the reference signals can be controlled by manipulating the inner voltage e_j and the voltage difference V_{diff}. On the other hand, because the generation of the circulating current is caused by the voltage difference between the upper and lower arm, it can be calculated by measuring the capacitor voltages of both upper and lower arm submodules and used to minimize the circulating current as demonstrated in (13):

$$V_{diff} = L_s \cdot \frac{d(I_{diff})}{dt} = \frac{1}{2}(V_{dc} - (V_{c\_up} + V_{c\_low})) \quad (13)$$

According to (13), the voltage difference can be reduced by increasing the inductance of the arm inductors. However, this will lead to more losses in the arm inductors and will also increase the size of the converter. Therefore, a preferred approach is the suppression of the circulating current by inserting compensating control signals as in (13).

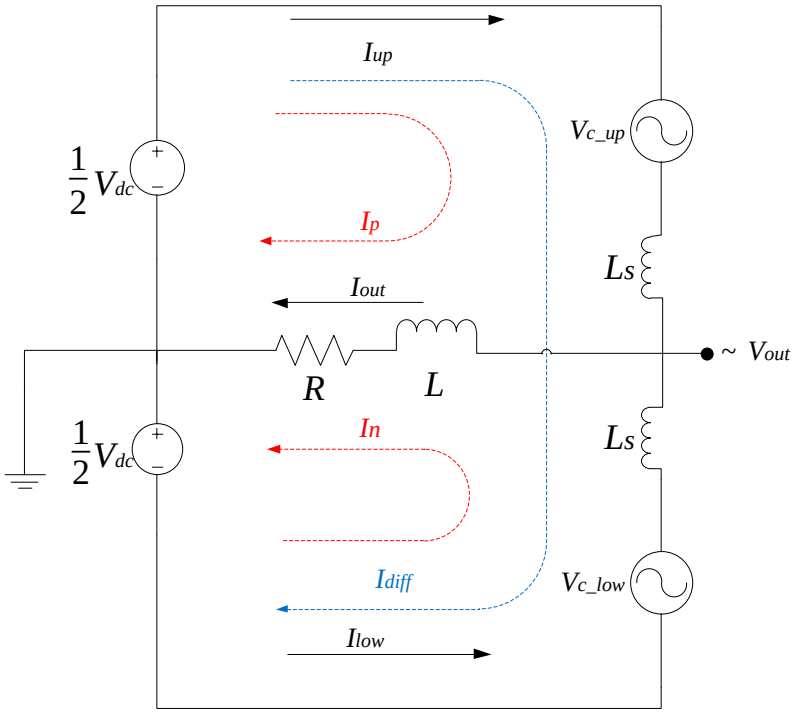


Figure 12: The equivalent model of the single phase MMC

As the results of the voltage imbalance existing between the upper and lower arm, the differential currents I_{diff} are flowing among the arms as shown in Figure 12. Where they are defined as shown in (14)-(16),

$$I_{up} = I_p + I_{diff} \quad (14)$$

$$I_{low} = I_n - I_{diff} \quad (15)$$

$$I_{out} = I_{up} + I_{low} \quad (16)$$

Both upper arm and lower arm currents contain half of the output current I_{out} and the differential current I_{diff}. I_p and I_n are the output currents flowing in upper and lower arm separately. Substitute (14)-(16) into (1)-(4),

$$V_{dc} = V^*_{c\_up} + V^*_{c\_low} - L_s \cdot \frac{d(I_{diff})}{dt} + V_{diff} \quad (17)$$

$$V_{c\_up} + V_{c\_low} = V^*_{c\_up} + V^*_{c\_low} - L_s \cdot \frac{d(I_{diff})}{dt} + V_{diff} \quad (18)$$

Because in (17) and (18), the differential current and voltage are inserted into the reference signals to reduce the circulating current flowing among the arms, the realizations of the control signals are critical in controlling the MMC.

Since the continuous mathematical model was given based on the half-bridge MMC, each submodule is considered as a continuous voltage source. This indicates that the general converter modelling and control can be applied to MMCs, including the widely-used Pulse Width Modulation (PWM) approach shown in Figure 13.

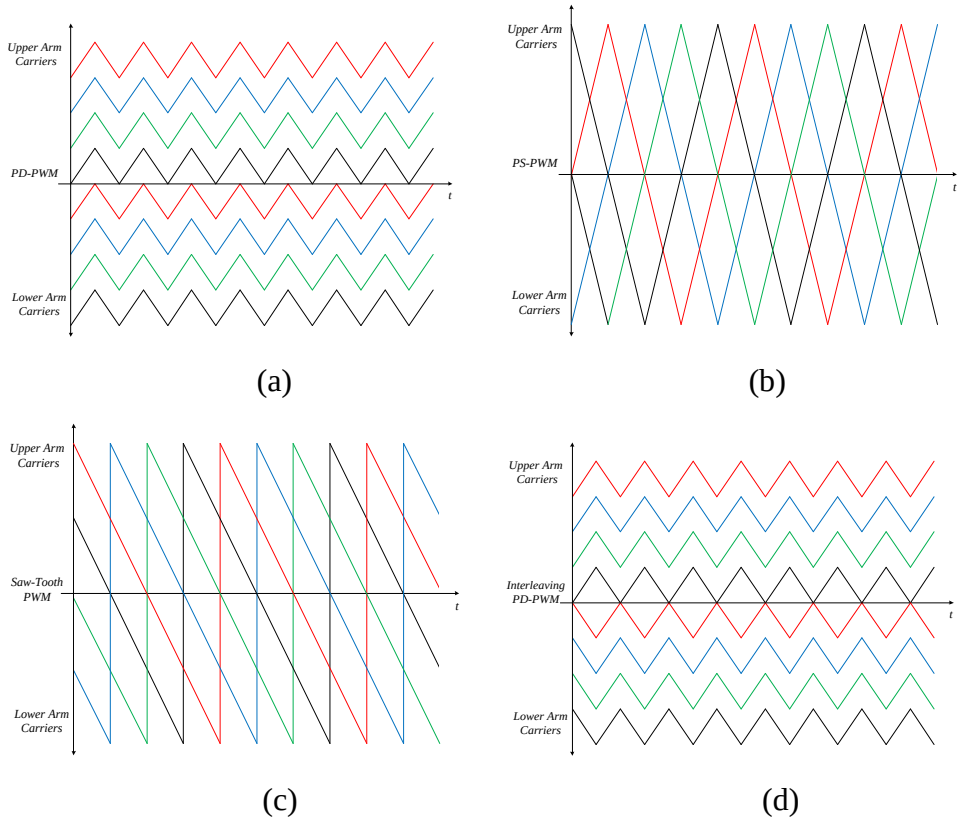


Figure 13: The (a) PD-PWM (b) PS-PWM (c) Saw-Tooth PWM (d) Interleaving PWM patterns for the four-level MMC.

In the traditional two-level converter, there is only one carrier interacting with one reference signal to generate the gate signals. However, in MMC, there are many submodules connected to each arm in series. Hence the number of carriers also increased. For example, if the number of the submodules is N in both upper and lower arm, there must be N carriers to generate the same number of gate signals. On the other hand, the number of the submodules in each arm can have a great impact on the computational requirement of generating the PWM signals in one operation cycle. In this case, the Nearest Level Modulation (NLM) method is

employed when there are many submodules in each arm. Because the NLM is generated according to the approximation of the reference signals, it has drawbacks such as more converter harmonics than the PWM method when the number of submodules is smaller. Regarding the conventional sinusoidal PWM, both PD-PWM and PS-PWM can be modified and applied in the MMC modulation scheme. Therefore, the modulation methods are proposed based on the aforementioned two PWM technologies [97]-[100]. Among them, the interleaving technology stands out by generating 2N+1 voltage levels instead of N+1 using regular PS-PWM or PD-PWM. However, the interleaving technique requires the phases of the carriers to be shifted into different phases which will lead to the imbalanced DC voltage distribution applied to the arm inductors, hence generating excessive current flow in the arms. Furthermore, it increases the current threshold of the arm inductors because of the imbalanced energy distribution. Thus the approach has limited flexibility due to these drawbacks. In [101], the reference signals are modified based on the control signals to avoid the carriers phase shifting. However, as is the case with the interleaving PWM, the number of the submodules turned on/off is not constant. The voltage applied on the arm inductors after interleaving is larger than the conventional PWM methods. In [47], the PS-PWM and PD-PWM are combined with the voltage balancing methods to further increase the precision and performance of the converter.

2.3 Parameter Selection

In the converter used for conventional transmission systems, due to its simple structure, there are not as many capacitors and inductors as employed in the MMC. In additional to the power switches, there are also a significant amount of passive components used in MMC. Because the capacitors in the submodules and the arm inductors are the major elements in the converter, the parameter selections for both capacitors and inductors become critical regarding the costs and the power ratings of these components. In the MMC, the capacitor is used as power storage components to transmit energy from one terminal to another. In [56], the proposed selection of the capacitance is based on the energy-power ratio based on the converter power capacity as shown in (19) and (20).

$$C_{arm} = \frac{E_{cmax}}{3{V_{dc}}^2} = EP\frac{P_s}{3{V_{dc}}^2} \quad (19)$$

$$\frac{1}{C_{arm}} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_N} \quad (20)$$

In (19), C_{arm} is the arm capacitance, E_{cmax} is the rated converter power, V_{dc} is the DC side voltage, EP is the energy-power ratio, and P_s is the apparent power of the converter. The arm capacitance is related to the individual capacitor inside each submodule as shown in (20), $C_1 \ldots C_N$ are the individual capacitance values of each capacitor in the submodules. The apparent power and the DC side voltage are determined from the system specifications, leaving the constant EP to be calculated to derive the arm capacitance. Based on the experiences and the test results [54][102], the EP is selected within the range from 10 to 50 for best converter performance. By selecting a large capacitance, it can reduce the voltage ripple in the capacitor of each submodule hence improving the converter output. On the other hand, larger arm capacitance increases the rating of the components. As a result, both size and cost of the capacitors are increased. However, (19) and (20) have given rise to the idea of selecting suitable arm capacitance from the power transmitting aspect. Other aspects can be investigated to determine the arm capacitance according to the characteristics of the converter, such as the voltage ripple. The arm capacitance selection methods based on the capacitor voltage ripples are shown in [54][102].

$$C_{\text{sub}} = \frac{P_s}{3 \cdot MI \cdot N \cdot \omega_0 \cdot \varepsilon \cdot (V_{dc})^2} \left[1 - \left(\frac{MI \cdot \cos\varphi}{2}\right)^2\right]^{3/2} \quad (21)$$

In (21), C_{sub} is the capacitance of each capacitor, N is the number of the submodule in each arm, ε is the capacitor voltage ripple, $\cos\varphi$ is the power factor of the converter. As stated in [54], the design criteria for the individual capacitor includes but is not limited to, the maximum capacitor voltage, the capacitor voltage ripples, the ripple current, and the voltage capability. It is well described in (21) that the capacitor voltage ripple is the key factor in determining the capacitance value of the individual capacitor. If the capacitor voltage ripple is required to be small, the capacitance should be large according to (21).

The selection of the arm inductors depends on the current rating of the converter. This is because they are connected to the submodules in series to limit the current flowing through the capacitor during the switching states changes. This suppresses the circulating currents, as well as limiting the fault currents. In [58][59], the inductor was selected based on the instantaneous power balancing analysis. Because of the double-fundamental frequency alternating

current flowing among the arms, the disturbances caused by the circulating current also requires suppression. In (22), the inductance is derived from the peak value of the circulating current.

$$L_s = \frac{1}{8\omega_0^2 \cdot C_{sub} \cdot V_c}\left[\frac{P_s}{3I_{2f}} + V_{dc}\right] \quad (22)$$

In (22), L_s is the arm inductance, U_c is the DC component of the capacitor voltage, I_{2f} is the maximum value of the circulating current. As demonstrated in (22), the arm inductance is related to the arm capacitance as well since the resonance effect of generating the circulating current. Therefore, by merely increasing the arm inductance, if the required I_{2f} is small, it also can be compensated by increasing the arm capacitance C_{sub}. However, the arm inductor affects the voltage ripple across the capacitor since it is limiting the current flowing in the submodules. Therefore, the performance of the converter would be different from it described in (19) and (20) due to this effect. In [59], the selection of the arm inductance can be determined based on the restraints of power switches when there is a fault. Therefore, the inductor can be designed based on the maximum rate of change in fault current.

$$L_s = \frac{V_{dc}}{\alpha} \quad (23)$$

In (23), α is the rated change of fault current. Both (22) and (23) can be used to determine the arm inductance. However, the performance of the converter can be different from that described in (19)-(23) depending on the control approaches applied to the converter.

2.4 Conclusion

The structure of the MMC has been investigated, and it is compared to other types of the multilevel converter to demonstrate the control simplicity and efficiency when the number of the converter voltage levels is large. The modelling of the MMC demonstrated that the converter output is achieved by controlling the inner voltage and the number of the turning on submodules by assigning appropriate PWM signals. Depending on the requirements of the system, the PWM method can be conventional PD-PWM and PS-PWM or interleaving technology to increase the number of the output voltage levels. It is considered to be more efficient to use NLM rather than PWM when the number of the submodule is large. The parameter selection process focuses on the capacitors in the submodules and the arm inductors. In addition to the system requirements, the capacitor voltage ripple, maximum converter power rating, etc. are considered to optimize the selections of the capacitor and the inductor.

Chapter 3

Comparison of the modulation methods

3.1 Introduction

The mathematical model indicated that the converter output voltages could be controlled by changing the inner voltage e_j. However, the processing of the reference signals to produce appropriate gate signals is the first step of controlling the MMC. Based on the previous literature review, the conventional PWM methods are combined with the voltage balancing control since the submodule capacitor voltages are stabilized by changing the switching angles. Depending on the arrangement of the carriers, the modulation methods are divided into the two general categories: Phase-Shifter Pulse Width Modulation (PS-PWM) and Phase-Dispositioning PWM (PD-PWM). The major difference between the PS-PWM and the PD-PWM is that, in PS-PWM, the carriers have the same magnitude, but their phases are shifted depending on the number of the submodules. During normal operation, the number of the submodules is determined as demonstrated in Figure 14. In contrast, the carriers in PD-PWM have the same phase but different magnitudes, as shown in Figure 15. The interleaving technology to increase the converter output voltage levels by changing the phase of the carriers by 180^o in the PD-PWM as shown in Figure 16. In conventional PWM methods, the reference signal modulation of the MMC is based on integrating the submodules to generate the desired output voltage, for example, the number of submodules in each arm is $N = 4$. Therefore, there are four different carriers observed in Figure 14. The phase shift is $\frac{2\pi}{N}$ where N is the number of submodules. Therefore, the phase shift between each carrier is $\frac{\pi}{2}$. The switching states in Figure 15 indicated how many submodules are turned on during a full operation cycle. The PS-PWM are employed in [40][129][130] for control of its arm currents. In [40], the equivalent circuit was provided to derive the high-frequency current component existing in the arm current. In order to adjust the capacitor voltages, the high-frequency current components based on the PS-PWM are considered as one of the variables to balance the capacitor voltages. The modulation method which does not require the voltage sorting is proposed in [46]. However, to achieve capacitor voltage balancing, each submodule is provided with two feedback control loops to compensate the capacitor deviations. However, the communication data rate between the control unit and the MMC circuit can be significant when the number of the submodules is increased. The performance of the closed-loop controllers is evaluated and a linear approximation controller is provided to further simplify the control process [130]. Because all the

submodules are independent of each other due to the two different connecting states, the dynamic control of each submodule can be achieved.

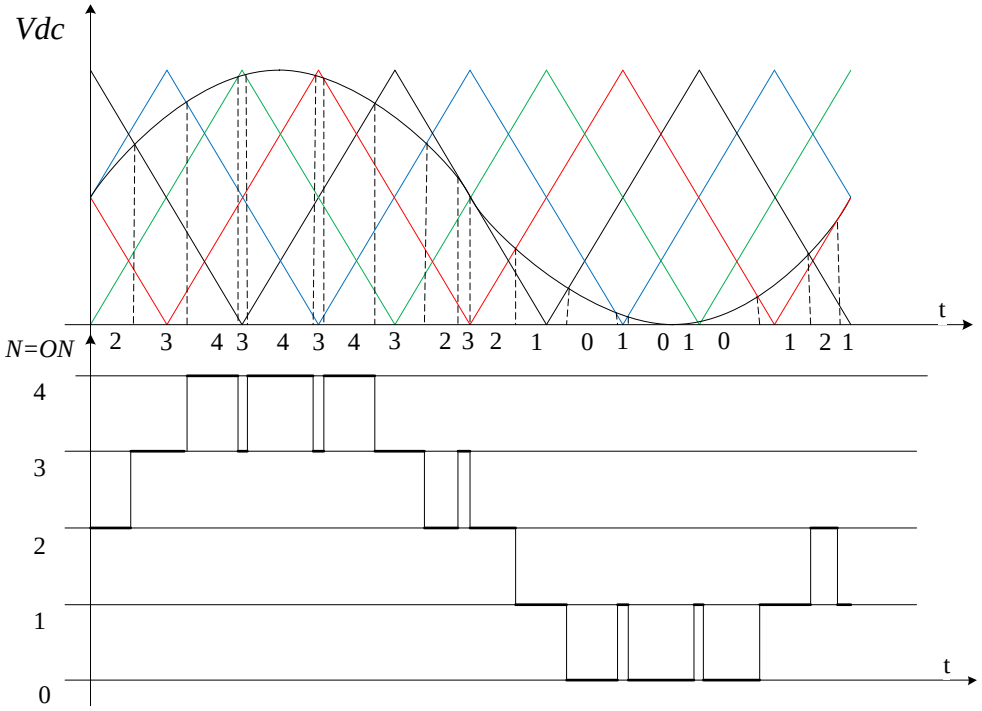


Figure 14: The modulation of the MMC based on PS-PWM

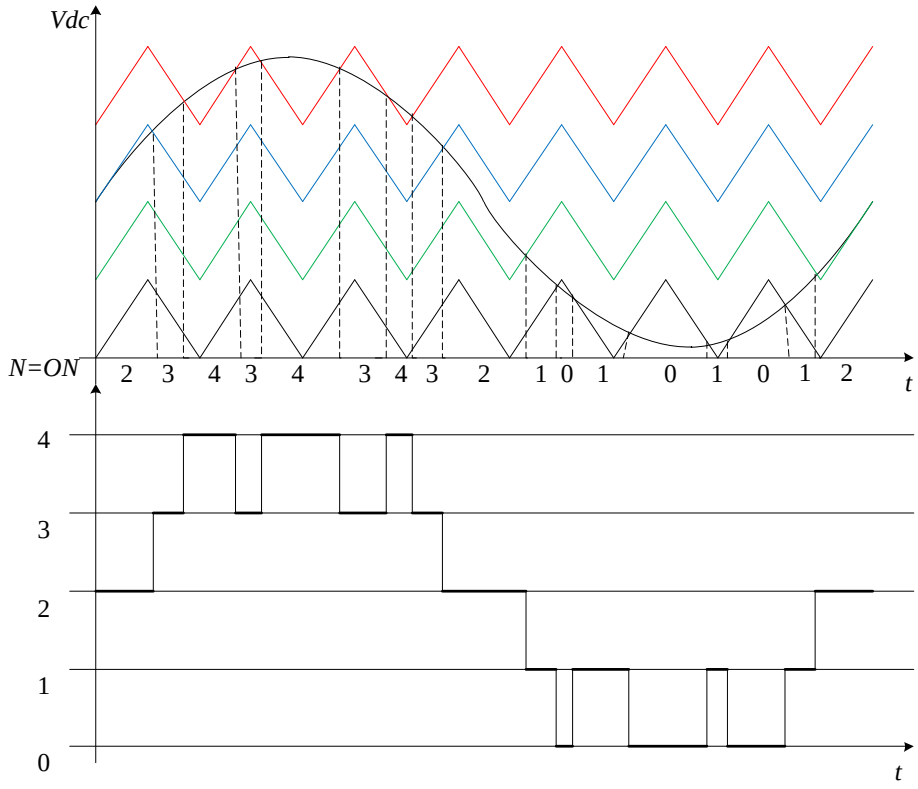


Figure 15: The modulation of the MMC based on PD-PWM.

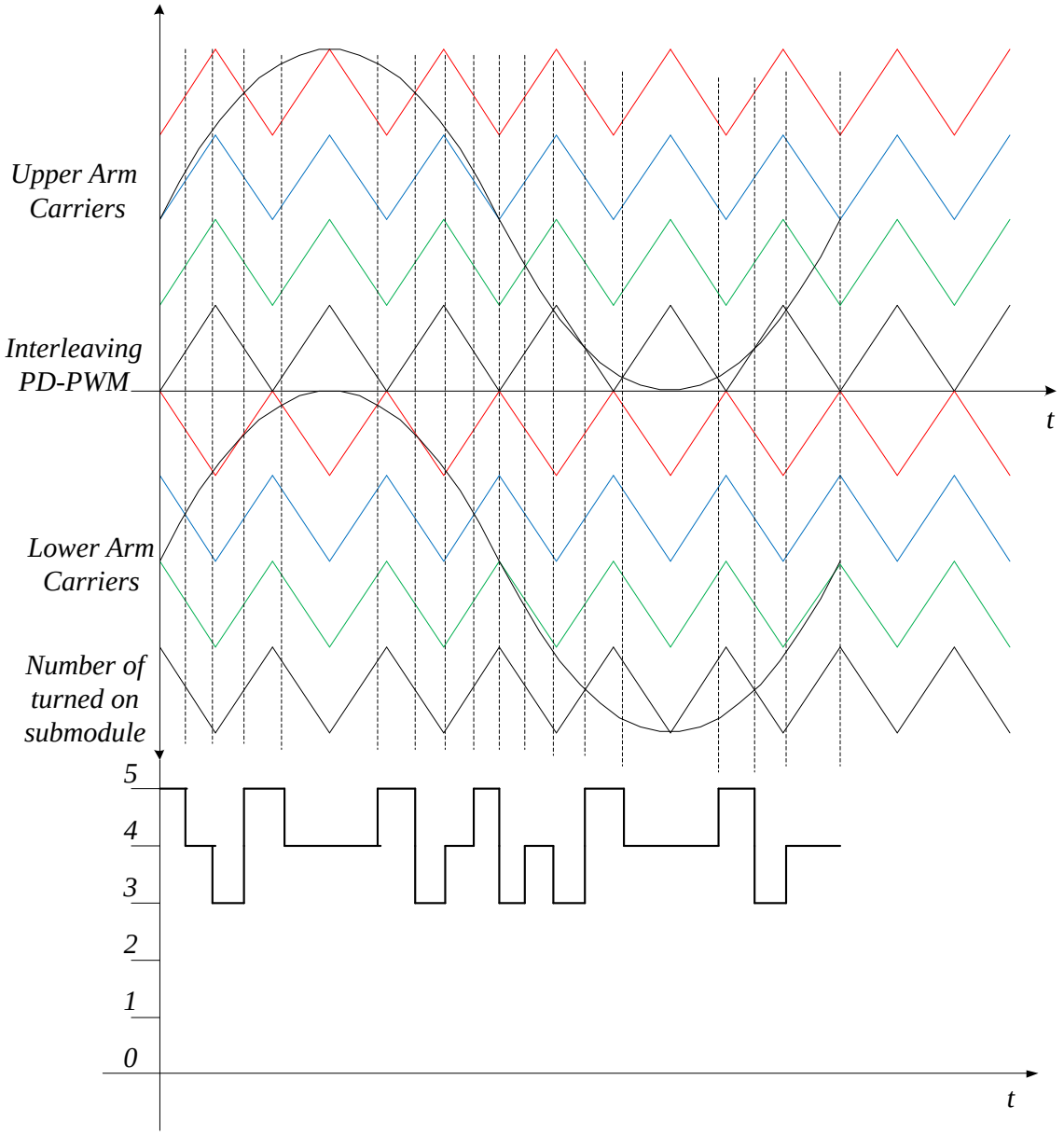


Figure 16: The interleaving technology applied in MMC

Compare the two approaches shown in Figure 14 and Figure 15, the switching states of the submodules are the same without the effects of the voltage balancing control. In combination with the conventional voltage balancing control, changing the switching states of each sub-module is easier to achieve by changing the magnitudes of the carriers instead of changing the phases. The interleaving technology shown in Figure 16 is a modified PD-PWM scheme used to increase the converter output voltage levels. During normal operations, the turned on and turned off submodules should keep constant to minimize the voltage ripples caused by the in-appropriate switching actions.

$$V_{c\_up} = V_{c\_low} = \frac{V_{dc}}{N_{on}} \quad (24)$$

N_{on} is the number of the turned-on submodules in one operation cycle. As shown in Figure 14 and Figure 15, the total number of the turned-on submodules should be constant ideally. However, due to the delay of the switching on and off the submodules, the total turned on number can vary depending on the system characteristics. Whereas the time scale of the gate signal delays is on a us scale, the interleaving technology introduced in [131] is on a ms scale. According to (24), the longer the time delay, the greater the capacitor voltage deviations. Therefore, the interleaving technology is compensated by the circulating current suppression control to eliminate the unnecessary harmonics generated by the imbalanced DC voltage distribution. In this case, the PD-PWM shows better controllability when compared with the PS-PWM and the interleaved PD-PWM.

The key aspects of MMC control lie in the voltage balancing and circulating current controls. The voltage balancing methods are presented with regard to the voltage distributions among the submodules [117]-[120], and [121]. The existence of the circulating currents and control approaches to minimize these currents to lower the stresses of the affected components. However, the realization of the control signals is subjected to the PWM technologies applied. Especially the voltage balancing controls implemented based on the arrangements of the PWM signals corresponding to each submodule.

3.2 Control philosophy

3.2.1. Voltage balancing

One of the important aspects of many types of the multilevel converter is to manage the power flowing in and out of the converter, especially when capacitors are used as an energy storage component. The capacitors will be charged or discharged depending on the power flows. Inappropriate voltage balancing control can generate a lot of harmonics on the AC side of the converter [125]. Therefore, the energy distributions are controlled as demonstrated [117][47]. However, the fundamental principle of balancing the voltage across the capacitors is to ensure the DC voltage is equally distributed among the capacitors and none of the capacitors will be over charged or discharged beyond an acceptable limit. Monitoring the capacitor voltages requires the extra control loops. The voltage of each capacitor is measured and processed through a controller to identify the capacitors with the highest voltage to the lowest voltage. The selected

capacitors will be charged or discharged based on the current direction flowing into each sub-module. In other words, when the current flowing in the arm is charging the capacitor, the sub-module with low voltage capacitor will be turned on to balance the voltage distribution, or vice versa. In that case, the monitoring of the arm currents is necessary to implement the voltage balancing control. Figure 17 shows the flow chart of the voltage balancing control.

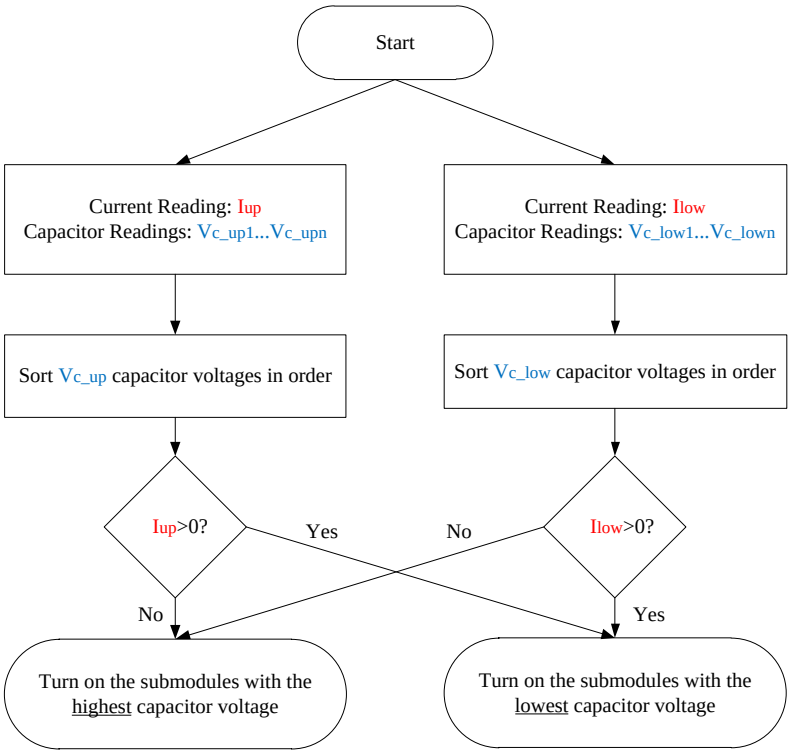


Figure 17: Voltage balancing control.

Two different PWM topologies are used to generate the gate signals, Phase-Disposition PWM (PD-PWM) and Phase-Shifted PWM (PS-PWM). However, they need to be modified in the control for MMC, for example, when there are four submodules in both upper and lower arms, the PD-PWM requires four in-phase carriers, but they have different amplitudes as shown in Figure 18. Each carrier signal has the same phase but with a quarter amplitude disposition. PS-PWM also requires four carrier signals but they have $\frac{\pi}{4}$ phase shift as shown in Figure 19.

According to the simulation results, the differences in the converter output of these two modulation methods is focused on the switching frequencies as illustrated in Figure 22 (a) and Figure 23 (a). However, the PD-PWM is capable of increasing the voltage level without increasing the number of submodules [126] and also has a shorter response time.

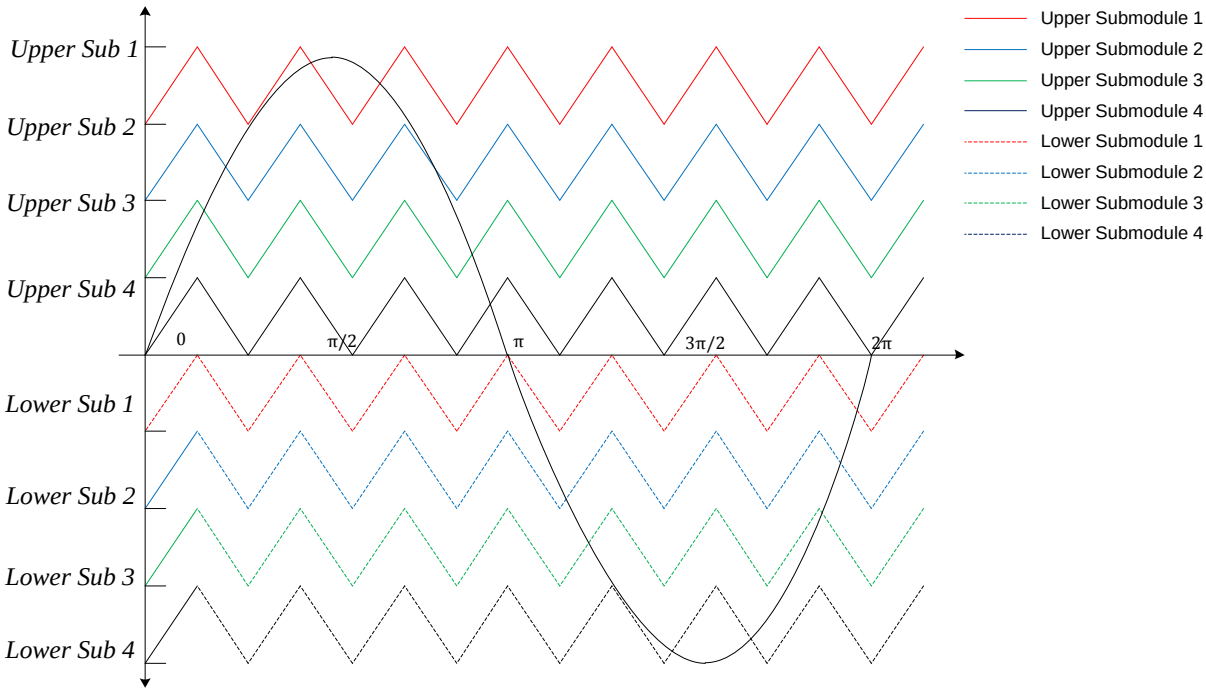


Figure 18: Upper and lower arm carrier waveforms using PD-PWM signal

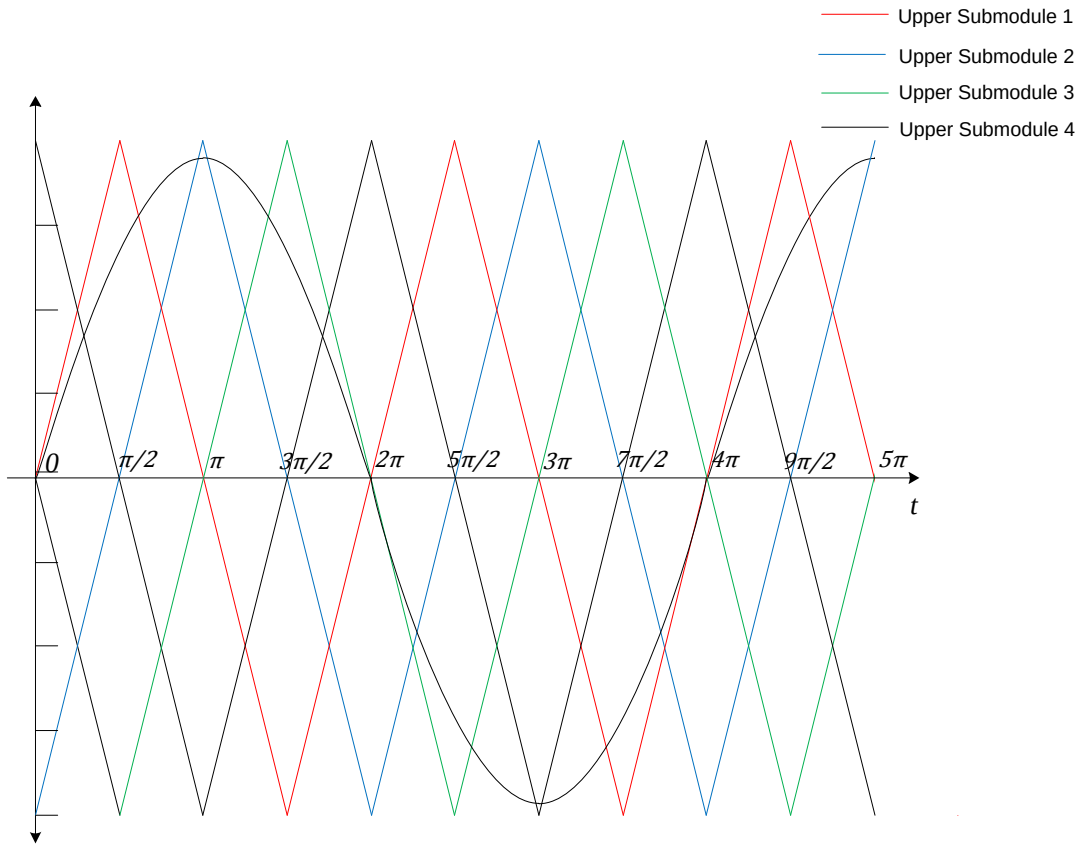


Figure 19: Upper and lower arm carrier waveforms using PS-PWM signal.

3.2.2.Circulating Current

The voltage imbalance existing inside of the converter leads to a self-generated current flowing among the phases and arms inside the MMC. On one hand, the series-connected inductor and the capacitor will generate resonant currents flowing among the submodules and inductor. On the other hand, due to the switching actions, the number of the turned on and off submodules may vary depending on the modulation scheme. Especially when the interleaving technology is employed, the circulating current can be much higher than normal modulation method without circulating current suppression control. However, the popular circulating current suppression methods are separated as two different concepts, one focuses on eliminating the circulating current majorly existing in the twice fundamental frequency, the other focuses on regulating the circulating current to the desire DC value. Both methods are proved to be effective against the circulating current generated by normal operations. However, the effects under fault conditions were not provided.

Figure 12 shows the equivalent MMC circuit of a single-phase MMC. According to *Kirchhoff laws* two equations can be derived in (25) and (26).

$$V_{out} = \frac{V_{up}+V_{low}}{2} \quad (25)$$

$$i_{out} = \frac{i_{up}+i_{low}}{2} \quad (26)$$

In (25), the converter output voltage is V_{out} calculated as the sum of the upper and the lower arm currents, and (26) gives the converter output current i_{out} which is the current flowing into the load. The differential voltage and current could also be derived in (25) and (26).

$$V_{diff} = \frac{V_{up}-V_{low}}{2} \quad (27)$$

$$i_{diff} = \frac{i_{up}-i_{low}}{2} \quad (28)$$

Where V_{diff} is the voltage spreading through the inductors L_s and the differential current i_{diff} is the differential current flowing inside the converter arms.

Circulating current causes several side effects when in operation, such as increasing the power rating requirement of switches, increasing energy losses caused by switches, increasing the voltage ripple across each capacitor, and increasing the response time of MMC. As circulating current and common-mode current are independent to each other, it is possible to control one of them without affecting the other.

Figure 20 shows the control loop of the circulating current. Where i_a is the current in phase a, P_{out} is the power flowing out from the converter, $V_{dc}{}^{*}$ is the demanded voltage on capacitors inside the MMC, $i_{diff1}{}^{*}$ is the calculated different current, V_{C_avg} is the average voltage across the capacitors, and MAF is a moving average filter to stabilize the input [127]. Since the circulating current is caused by the imbalanced power flow, the power P_{out} is calculated by the product of V_{com} and i_a, then P_{out} is divided by the demanded DC voltage to obtain the differential current. The difference of the demanded voltage value and the actual voltage across the capacitors can be processed through a PI controller to have the second circulating current reference. Then the control signals are generated through a proportional gain K_p shown in Figure 20. Then the signal V_{diff} is forwarded to the inner current loop of the converter, which is commonly used in VSC-based converters [128][129].

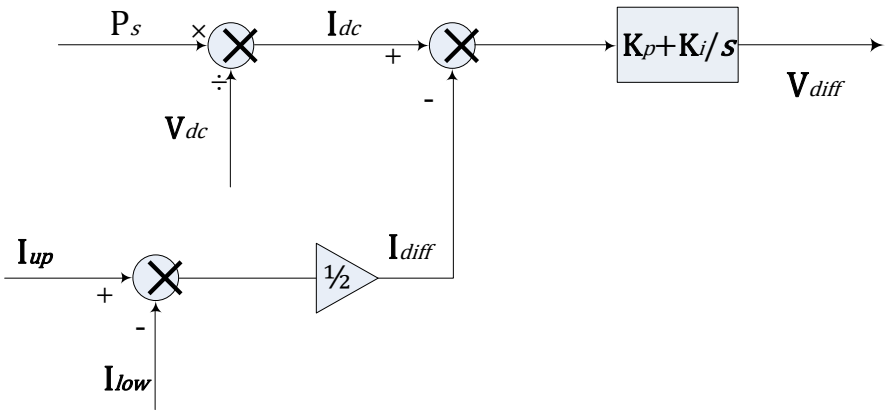


Figure 20: Circulating current suppressing scheme.

3.2.3.Submodule and one phase module

Each submodule consists of a half bridge circuit taking charge of switching and a capacitor as a power storage component, as shown in Figure 21. Generally, for high voltage applications, power switches such as IGBTs are chosen for the higher voltage tolerance and lower switching

losses [122]. Figure 21 also shows the MMC with N submodules in each arm. Each submodule is connected in series to generate voltage steps by manipulating the switches within each submodule. As shown in Table 4, once $S1$ is open and $S2$ is closed, the corresponding V_{out} is zero because it is short circuited internally. When $S1$ is closed and $S2$ is open, the corresponding V_{out} is equal to V_c which is the voltage across the capacitor. Because there is current flowing between each capacitor, the voltage across the capacitor is not constant. Therefore a voltage balancing control is needed.

Table 4: Output of submodules regarding the switching states.

State	S_1	S_2	V_{out}
Connected	On	Off	V_c
Bypassing	Off	On	0

The simulation examines a seven level modular multilevel converter model with four submodules connected in series in each arm, i.e. $N = 4$. As the voltage steps is increased, the output waveform becomes close as a sinusoidal waveform. In MMC commercial applications, the number of submodules can be up to 200 or more [123]. To extend the flexibility of the modular structure, some of the submodules are in standby mode during the regular operation, and are only activated when one or more submodules has malfunctioned. This approach makes the modular multilevel converter more reliable compared to other multilevel converters [124].

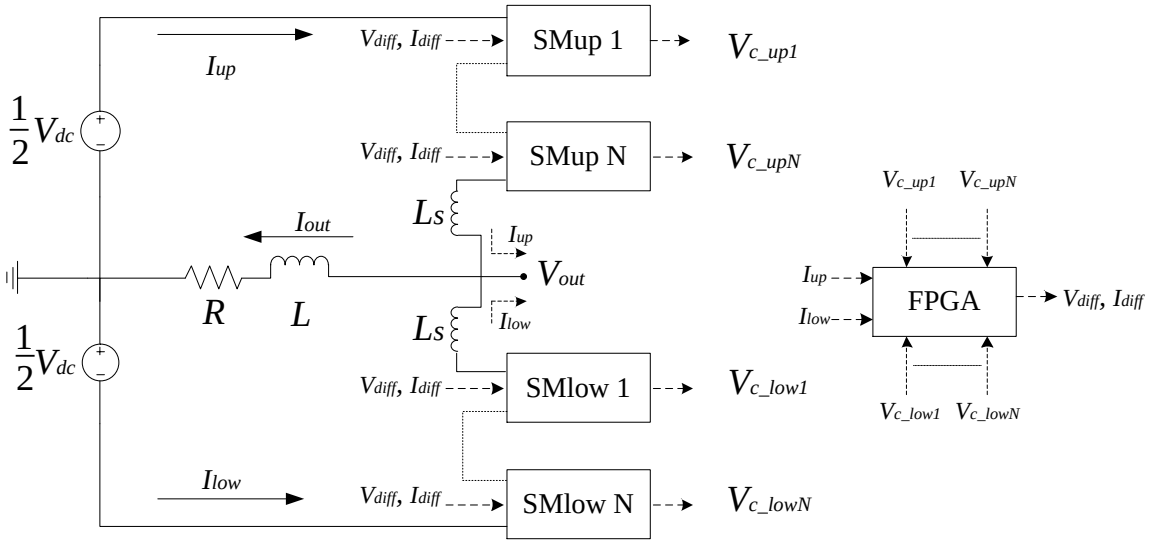


Figure 21: One phase module of the Modular Multilevel Converter

3.3 Simulation results

3.3.1.Comparison between PD-PWM and PS-PWM

The voltage balancing control and the circulating current suppression control are achieved by implementing the inner control loop. However, the modulation methods are required to convert the control signals into appropriate gate signals for each submodule. The half-bridge MMC shown in Figure 21 has been built in Matlab and designed as a 5-level MMC, which has four submodules in each phase. Each submodule has a voltage sensor to monitor the capacitor voltage changes. The voltage signals were then sent to the FPGA along with the arm currents signals to generate corresponding control signals. As shown in Figure 21, the signals are used to generate the corresponding gate signals when the voltage balancing and circulating current suppression control are activated. The PD-PWM and the PS-PWM are compared to each other to demonstrate the performance differences during normal operation. In Table 5, the parameters of the simulation model are listed.

Table 5: Parameters of the PD-PWM/PS-PWM based MMC

Parameters	Values
MMC power rating, P (W)	100
DC-link voltage, V_{dc} (V)	+/-50
Load resistance, $R(\Omega)$	12.5
Load inductance, L(H)	0.001
Phase inductance, L_s(H)	0.001
Capacitance, C(F)	0.002
Submodule reference voltage, V_{sub}(v)	25
No. of submodules in each arm, N	4
Carrier frequency, f (kHz)	1

Figure 22 shows the simulation results of the MMC using PD-PWM to generate control signals. In the simulations, the circulating current suppressing control (CCSC) is used at 0.25s to further stabilize the capacitor voltage inside each submodule. It can be seen from Figure 22 (b) and (c) that a large amount of circulating current causes a significant voltage imbalance of each capacitor before the control is applied. After applying the CCSC, the circulating current is reduced significantly to a low level and the voltage on the capacitors is returned to the required value. Also, Figure 22 (a) shows that when the CCSC is applied, the converter voltage output has smaller ripple than the output without CCSC. Figure 23 shows the simulation results of MMC using PS-PWM as the signal generating method. The same as the simulation using PD-PWM, it has CCSC started at 0.25s. Figure 23 (a) doesn't show much difference after applying the CCSC, but Figure 23 (b) and (c) indicate that the circulating current is reduced due to the

current suppression. Figure 23 (c) shows the capacitor voltage of one of the submodules which remains at a level between 24.2V and 25.8V v. Figure 23 (c) shows one of the capacitor voltage, and it tends to be more stable after applying CCSC. The circulating current shown in Figure 23 (b) is further reduced after the implementation of the suppression control.

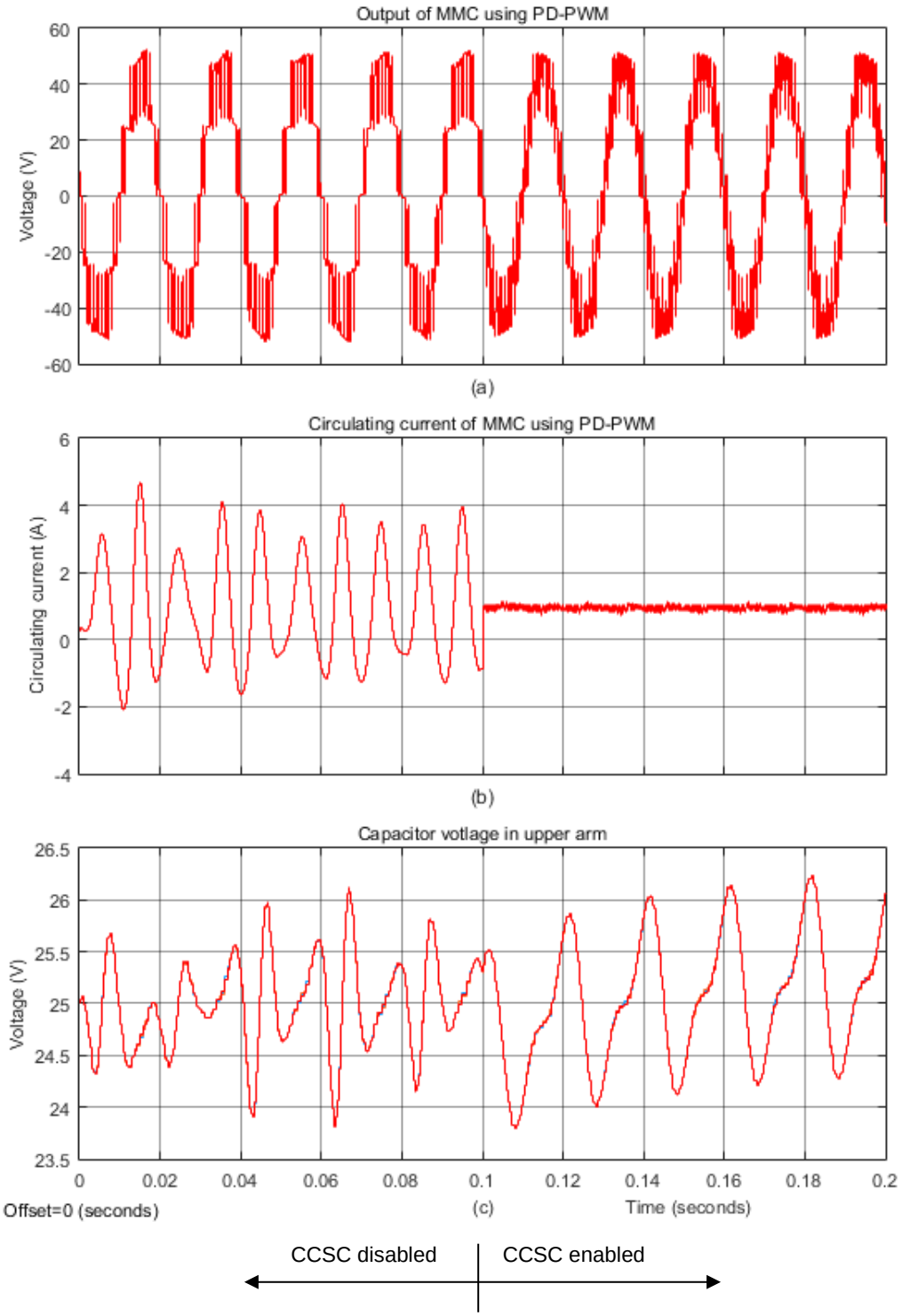


Figure 22: The simulation results of PD-PWM scheme with CCSC, phase-a (a) output voltage (b) Circulating current (c) Capacitor voltage.

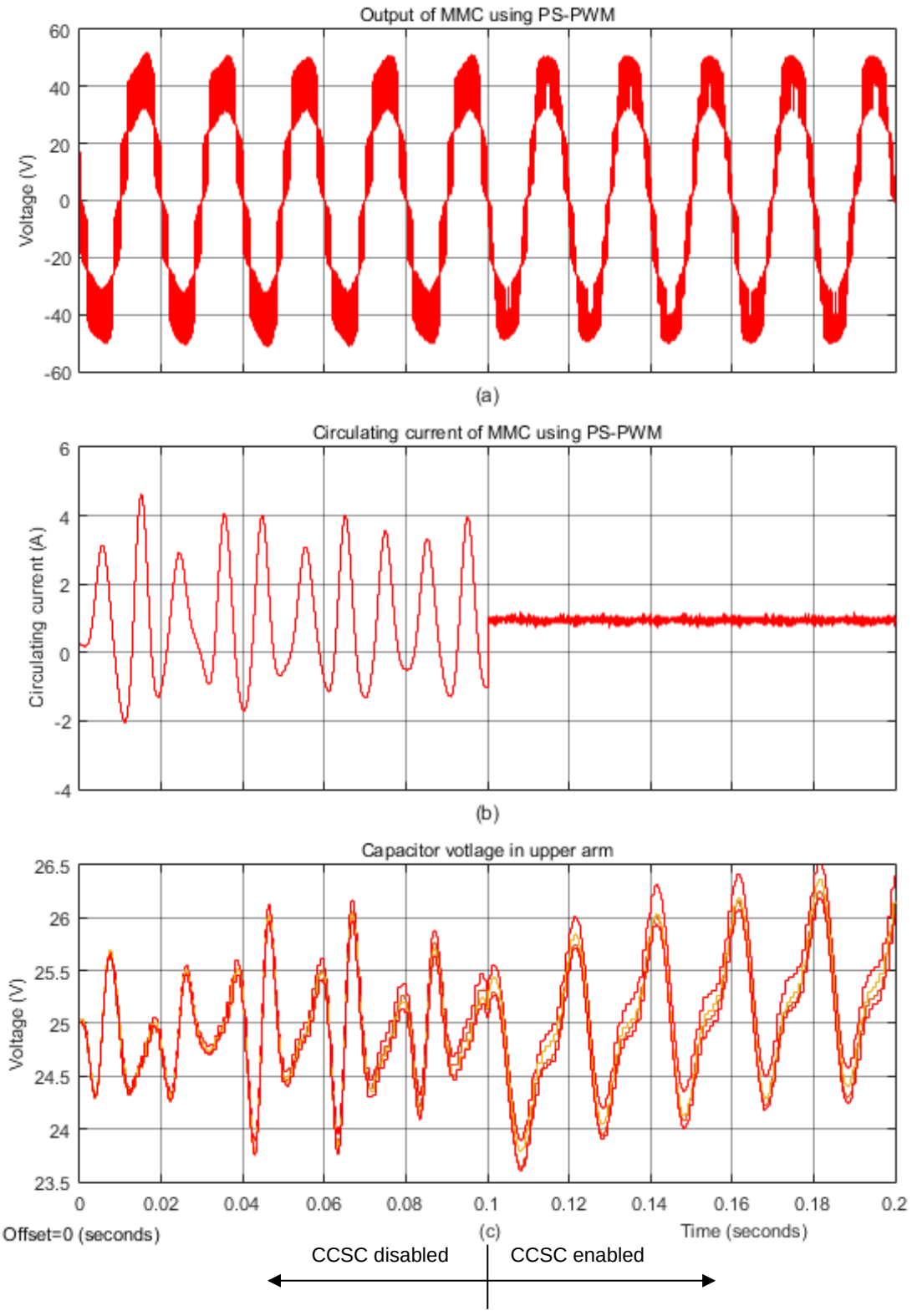
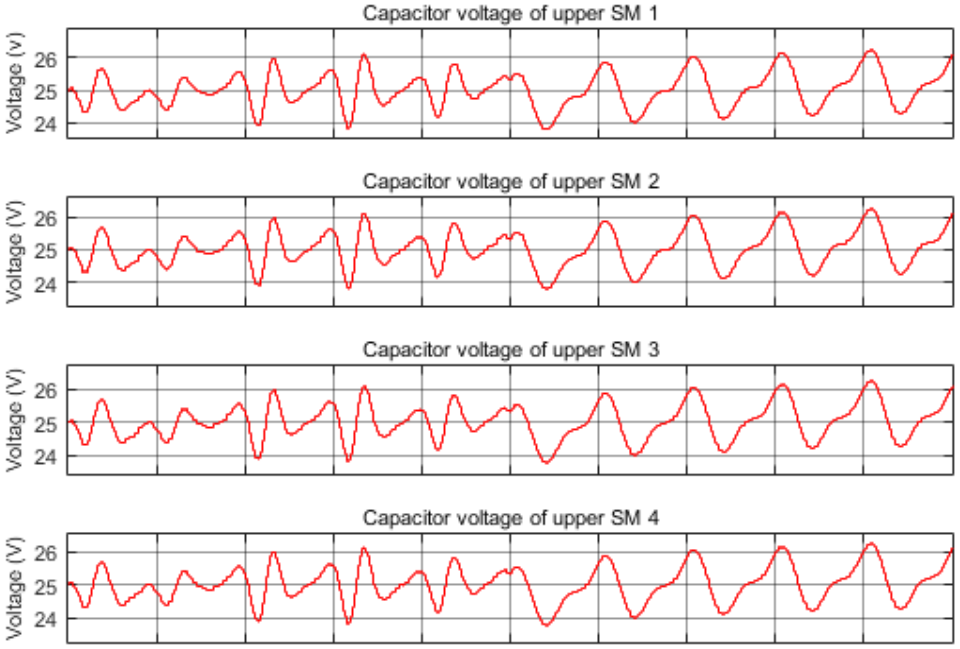
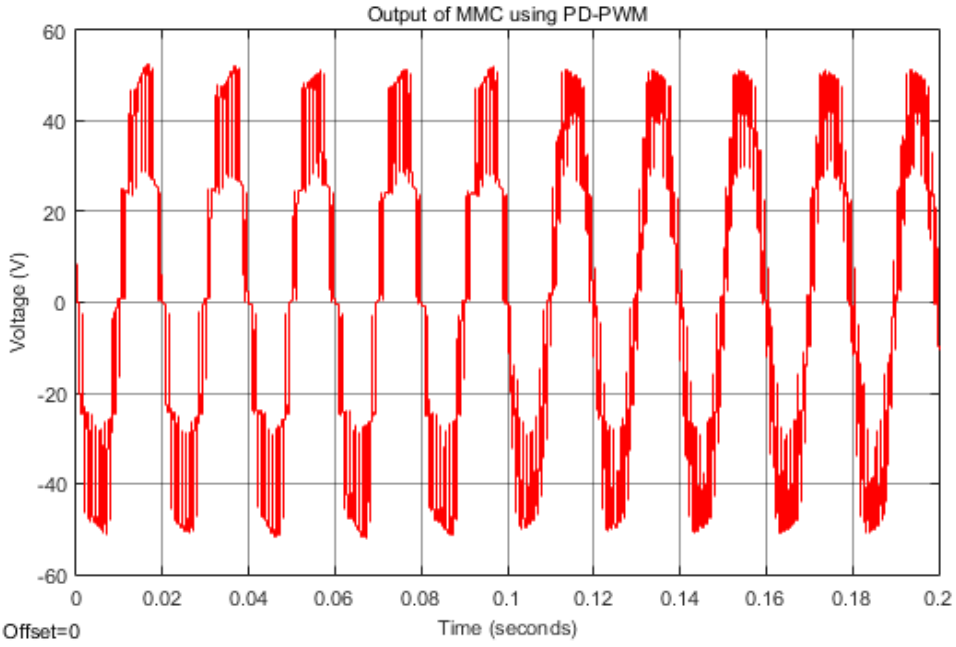


Figure 23: The simulation results of PS-PWM phase-a (a) output voltage (b) Circulating current (c) Capacitor voltage.

Each capacitor voltages and the output voltages for both PD-PWM and PS-PWM are shown in Figure 24 and Figure 25. One of the advantages of the PS-PWM is the capacitor voltage balancing control as demonstrated in Figure 25. The capacitor voltage and the converter output voltage are balanced due to the switching angle of each submodule.

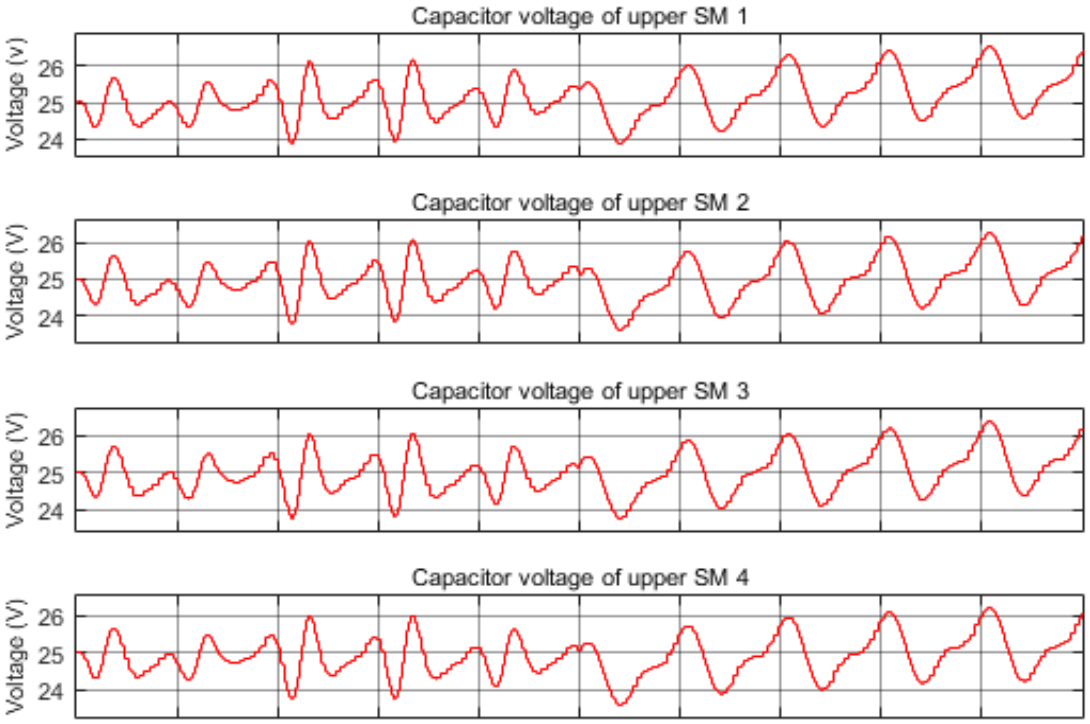


(a)

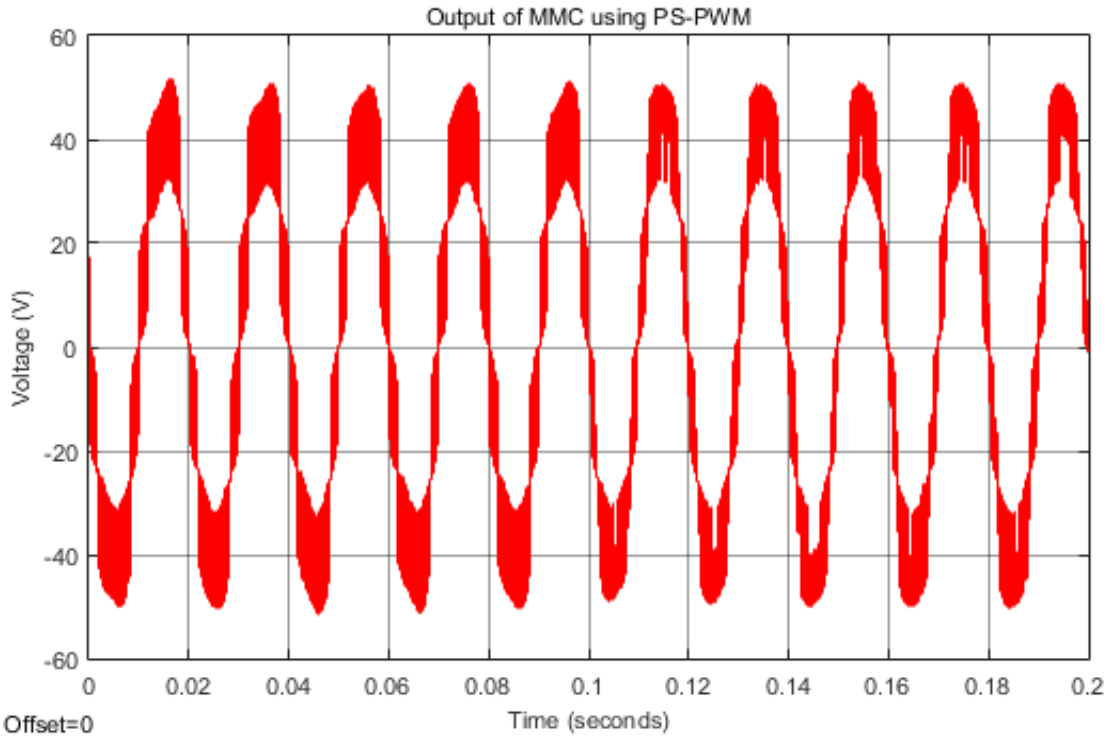


(b)

Figure 24: The output of the MMC using PD-PWM with CCSC applied at 0.1s (a) the upper arm capacitor voltages (b) the output voltage.



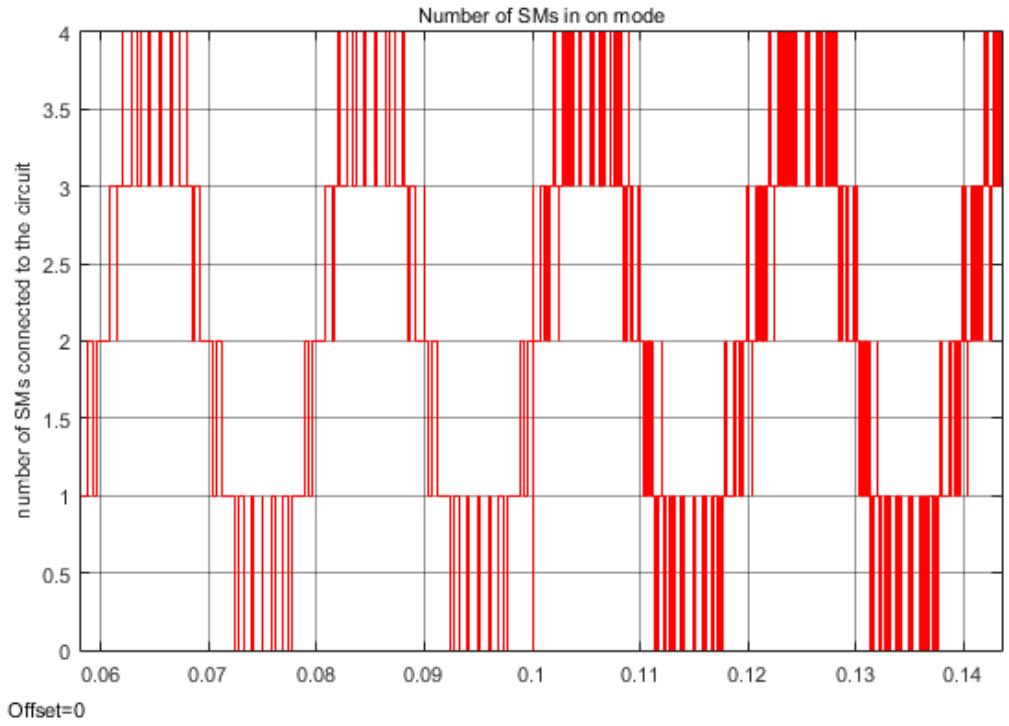
(a)



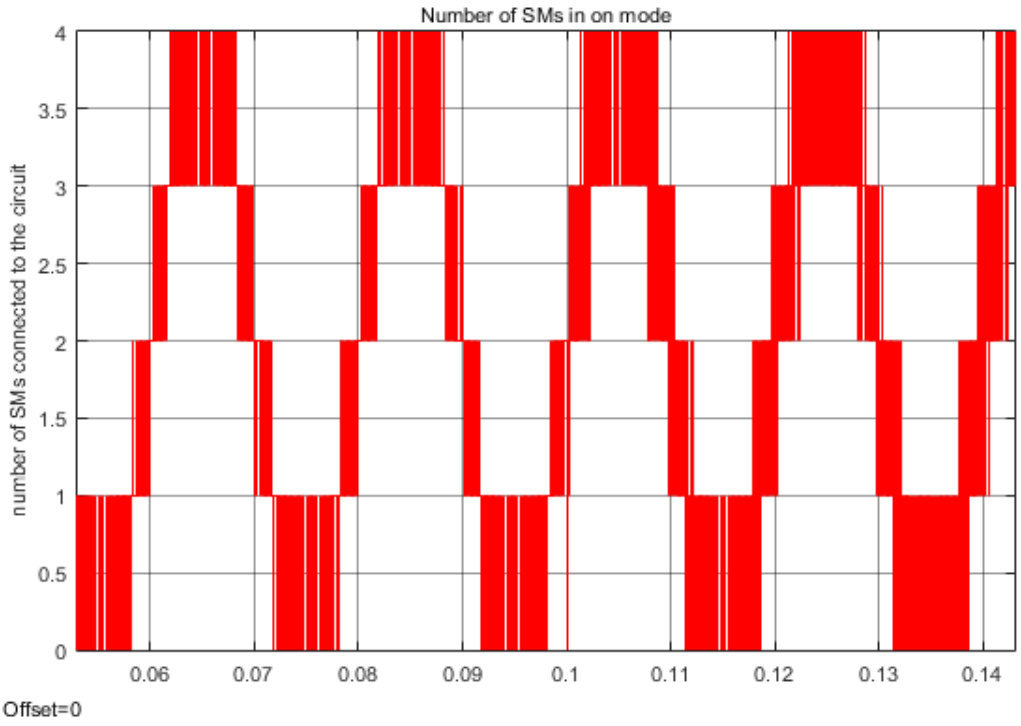
(b)

Figure 25: The output of the MMC using PS-PWM with CCSC applied at 0.1s, (a) the upper arm capacitor voltages (b) the output voltage.

The gate signals are shown in Figure 26, the integration of the on-period is constant during one operation cycle. Therefore, the capacitor voltages are balanced according to the average energy distributions. The capacitor voltage ripple observed in Figure 24 is 8%.



(a)



(b)

Figure 26: The gate signals for the upper submodules using (a) PD-PWM (b) PS-PWM.

However, the number of the submodules in the converter is insufficient. Hence the converter output voltage harmonics are at 19.17% as observed in Figure 27. Most of the converter voltage harmonics are clustered at the effective carrier frequency which is at 4 kHz. However, the 19.3% THD is still higher than the requirement of the grid code for a stable system. The AC filter may be necessary to eliminate the harmonics when the number of the submodule is low.

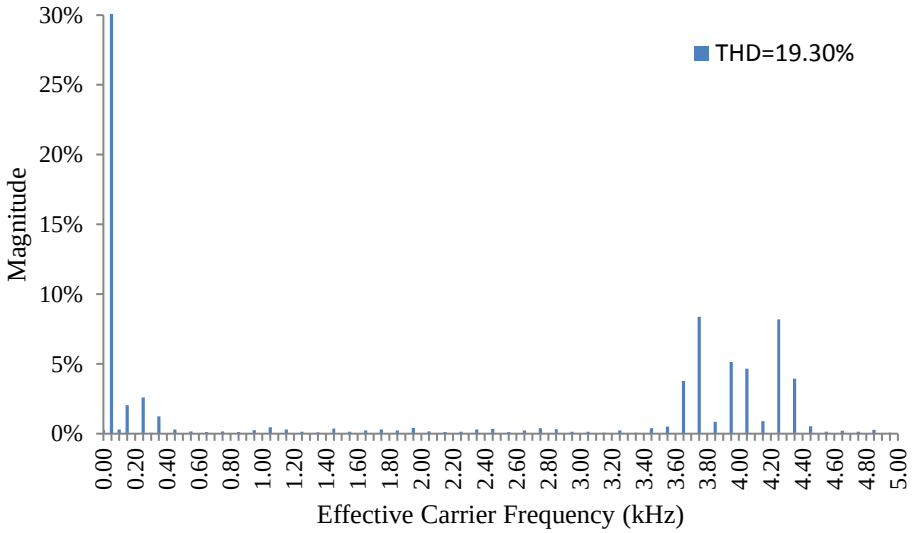


Figure 27: The converter output voltage harmonics.

3.3.2.Converter output harmonics

The number of the submodules in each arm may have a significant impact on the performance of overall system. According to [11], the commercialized MMC based transmission lines are using 200 submodules in each arm for the HVDC transmission systems. [132] evaluated the performance of the MMC based on the different number of the submodules. The voltage variance of the transmission lines is different based on its voltage level. Depending on the requirement of the grids [133][134][107], for the 132kv transmission line, the voltage variances are limited to +/-10%. On the other hand, the converter output harmonics are also defined in [135], if connected to the grid, the harmonic requirement are demonstrated in Table 6. In that case, the minimum number of submodules can be determined according to the harmonic level and the converter voltage levels. Since the designed MMC model is transmitting power at 600kV, the THD level is limited to 3% as shown in Table 8. As in the aforementioned harmonic distributions, the major part of the converter output voltage harmonics is focused on the harmonics clustered around the carrier frequency. Therefore, it is convenient to select appropriate carrier frequency according to the harmonic requirement.

Table 6: Planning harmonic levels for 400V systems

Odd harmonics (Non-multiple of 3)		Odd harmonics (Multiple of 3)		Even harmonics	
Order 'h'	Harmonics Voltage (%)	Order 'h'	Harmonics Voltage (%)	Order 'h'	Harmonics Voltage (%)
5	4.0	3	4.0	2	1.6
7	4.0	9	1.2	4	1.0
11	3.0	15	0.3	6	0.5
13	2.5	21	0.2	8	0.4
17	1.6	>21	0.2	10	0.4
19	1.2			12	0.2
23	1.2			>12	0.2
25	0.7				
>25	0.2+0.5(25/h)				

The Total Harmonic Distortion (THD) level is 5%.

Table 7: Planning harmonic levels for 6.6kV, 11kV, and 20kV systems

Odd harmonics (Non-multiple of 3)		Odd harmonics (Multiple of 3)		Even harmonics	
Order 'h'	Harmonics Voltage (%)	Order 'h'	Harmonics Voltage (%)	Order 'h'	Harmonics Voltage (%)
5	3.0	3	3.0	2	1.5
7	3.0	9	1.2	4	1.0
11	2.0	15	0.3	6	0.5
13	2.0	21	0.2	8	0.4
17	1.6	>21	0.2	10	0.4
19	1.2			12	0.2
23	1.2			>12	0.2
25	0.7				
>25	0.2+0.5(25/h)				

The Total Harmonic Distortion (THD) level is 4%.

Table 8: Planning harmonic levels for systems >20kV, < 145kV

Odd harmonics (Non-multiple of 3)		Odd harmonics (Multiple of 3)		Even harmonics	
Order 'h'	Harmonics Voltage (%)	Order 'h'	Harmonics Voltage (%)	Order 'h'	Harmonics Voltage (%)
5	2.0	3	2.0	2	1.0
7	2.0	9	1.0	4	0.8
11	1.5	15	0.3	6	0.5
13	1.5	21	0.2	8	0.4
17	1.0	>21	0.2	10	0.4
19	1.0			12	0.2
23	0.7			>12	0.2
25	0.7				
>25	0.2+0.5(25/h)				

The Total Harmonic Distortion (THD) level is 3%.

Table 9: Planning harmonic levels for 275kV and 400kV systems

Odd harmonics (Non-multiple of 3)		Odd harmonics (Multiple of 3)		Even harmonics	
Order 'h'	Harmonics Voltage (%)	Order 'h'	Harmonics Voltage (%)	Order 'h'	Harmonics Voltage (%)
5	2.0	3	1.5	2	1.0
7	1.5	9	0.5	4	0.8
11	1.0	15	0.3	6	0.5
13	1.0	21	0.2	8	0.4
17	0.5	>21	0.2	10	0.4
19	0.5			12	0.2
23	0.5			>12	0.2
25	0.5				
>25	0.2+0.5(25/h)				

The Total Harmonic Distortion (THD) level is 3%.

As shown in Table 6-Table 9, the harmonic margin for 5th order is larger than the other harmonics. Hence the carrier frequency can be selected at this level to avoid generating more harmonics at other frequencies. Furthermore, the harmonic margins for odd harmonics are larger than the even order harmonics according to the regulations. One of the advantages of the MMC based HVDC transmission systems is the size of the required AC filter is reduced or even not considered necessary when the number of submodules in each arm is sufficient. In this case, the relation between the number of submodules and the converter output voltage harmonics are investigated. The Fourier representation of the converter output is derived in [50][136], and is shown in (29) and (30):

$$v(\omega t) = \frac{4V_{dc}}{\pi}\sum_{n=1,3,5,7\ldots}[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_N)] \cdot \frac{\sin(n\omega t)}{n} \quad (29)$$

$$H(n) = \frac{4}{\pi n}[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_N)] \quad (30)$$

Where the V_{dc} is the parallel DC voltage, θ_1, θ_2 ... θ_n are the switching angles of the first submodule, second submodule, and the nth submodule respectively. The magnitude of the Fourier coefficient is shown in (30). However, as determined by (31), the harmonics strongly depend on the number of submodules in each arm.

$$THD\% = 100 \cdot \sqrt{\left(\frac{[v(t)]_{RMS}}{[v_1(t)]_{RMS}}\right)^2 - 1} \quad (31)$$

The RMS value of the converter output is shown in (32):

$$[v(t)]_{RMS} = V_{dc}\sqrt{N^2 - \frac{2}{\pi}\sum_{k=1}^{N}(2k-1)\theta_k} \quad (32)$$

and the fundamental value of $v(t)$ is shown in (33)

$$[v_1(t)]_{RMS} = \frac{V_{dc}2\sqrt{2}}{\pi}\sum_{k=1}^{N}\cos(\theta_k) \quad (33)$$

Substituting (33) and (32) into (31), the generalized THD equation can be obtained in (34)

$$\frac{\partial THD^2}{\partial \theta_n} = (2n-1)\sum_{k=1}^{N}\cos(\theta_k) + \left[2\sum\ (2k-1)\theta_k - \pi N^2\right]\sin(\theta_n) = 0 \quad (34)$$

Where n is the nth switching angle of the converter. Considering the integration effects of the MMC converter, the more submodules it contains, the lower harmonic content in the converter output. An MMC model, in Appendix A, was built in Simulink model to verify that the relations between the number of the submodules and the converter output harmonics. The MMC model was designed with 40 submodules connected in series in each arm, hence providing 41 converter voltage levels. The MMC model is connected to the passive RL load beyond the common coupling point. The control approaches are the voltage balancing and circulating current suppression as discussed before. The parameters of the system are displayed in Table 10.

Table 10: The system parameters of the 40 level MMC

Parameters	**Values**
Rated Power, P (MW)	2880
Load Inductance, L (H)	0.001
Load Resistance, R (Ω)	250
Arm Inductance, L_s (H)	0.004
Submodule Capacitance, C_{sub} (F)	0.004
Capacitor Voltage, V_c (kV)	30
DC voltage, V_{dc} (kV)	+/-600
Submodule Number in each arm, N	40
Converter Voltage Levels	41
Modulation Index Range, MI	0.96~1

When the number of submodules is at 40, the harmonics of the converter voltage output is small compared to the conventional two-level or three-level VSC. [137] investigated the harmonic distributions in regard to the different modulation methods, and the results demonstrated in Figure 28 satisfied the predictions in [137]. When the PD-PWM control approach is used, the carrier frequency is selected at the 5th order harmonic frequency, the major part of the converter output voltage is observed at 250Hz when the fundamental frequency is at 50Hz. The second closest harmonic component is observed at the 15th order. The magnitude of the 15th order harmonics is at 0.3% of the fundamental frequency, whereas the planning harmonic level of the grid code is set at 0.32%. However, it can be optimized by assigning proper harmonics elimination methods. The rest of the converter output harmonics are within the limits defined in grid codes as shown in Table 11. When using the PS-PWM, the carrier frequency is selected at the 5th order harmonic frequency as well. The major components of this converter output concentrated at 3rd and 5th order harmonic frequency, which are 1.23% and 1.63% respectively. Compared to the PD-PWM, it has fewer harmonics generated at the 5th order but it can generate more harmonics at the 3rd order frequency. The other significant difference between the PD-PWM and the PS-PWM is the number of the even order harmonics. It can be observed that, when using PS-PWM, the converter output contains even order harmonics as many as ten times of the harmonics generated when using PD-PWM, but the odd order harmonics are much less compared to the PD-PWM. Therefore, the simulation results can guide us when selecting between the PD-PWM and PS-PWM approaches.

Table 11: The comparison between the simulation and the grid code requirements

Odd harmonics (Non-multiple of 3)		Odd harmonics (Multiple of 3)		Even harmonics	
Order 'h'	Harmonics Voltage (%)	Order 'h'	Harmonics Voltage (%)	Order 'h'	Harmonics Voltage (%)
5	2.0 | 1.92,1.63*	3	1.5 | 0.35,1.23	2	1.0 | 0.03,0.8
7	1.5 | 0.03,0.93	9	0.2 | 0.05,0.09	4	0.8 | 0.02,0.2
11	1.0 | 0.05,0.04	15	0.3 | 0.32,0.03	6	0.5 | 0.03,0.62
13	1.0 | 0.08,0.02	21	0.2 | 0.13,0.01	8	0.4 | 0.01,0.29
17	0.5 | 0.14,0.01	>21	0.2 | <0.07,<0.04	10	0.4 | 0.02,0.18
19	0.5 | 0.15,0.01			12	0.2 | 0.02,0.21
23	0.5 | 0.12,0.02			>12	0.2 | <0.04,<0.03
25	0.5 | 0.05,0.04				
>25	0.2+0.3(25/h)				

*: left hand side is the planning harmonics level. Right hand side is the harmonic level of the 40-level converter using PD-PWM and PS-PWM separately. The planned Total Harmonic Distortion (THD) level for the 40-level converter is 3% | 2.48%, 2.93%

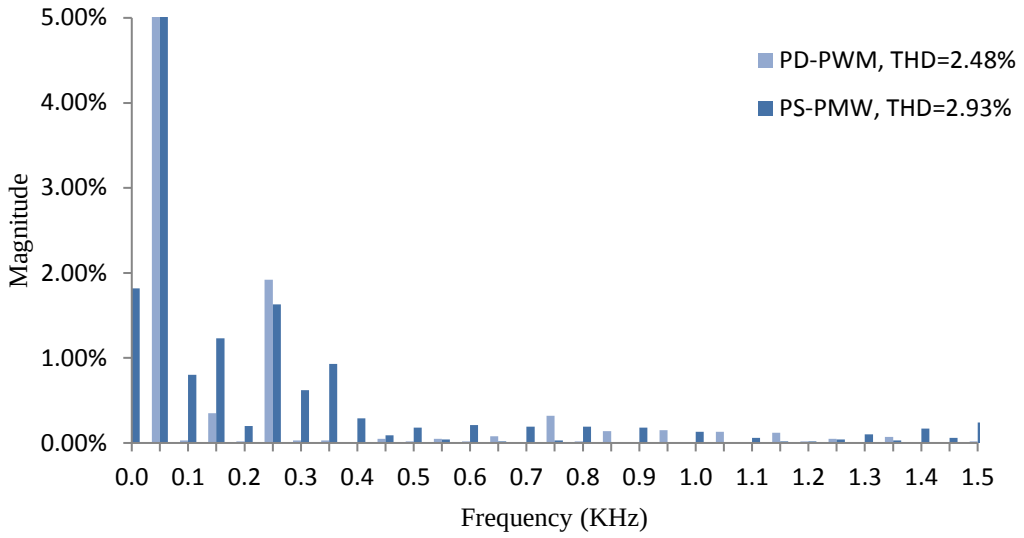


Figure 28: The converter output harmonics regarding the harmonics orders.

3.4 Conclusion

The selections of the PWM method depend on the two primary factors: 1) the realization of the reference signals when the number of the submodules is large. 2) the behaviours of the switches in the submodule according to the switching signal generated by the selected PWM method. Based on the simulation results, the PS-PWM has a better converter output regarding the THD and the capacitor voltage balancing since it does not require the voltage balancing method to balance the energy distribution. However, the realization of the PS-PWM can be difficult when the number of the submodules is large because the carriers are predefined in the control units and the computation requirements are is significantly higher than with the PD-PWM. On the other hand, the PD-PWM shows that it is more flexible when increasing the number of submodules in each arm. The simulation results also verify the feasibility of the PD-PWM when the voltage level of the MMC is high. The converter output harmonics are within the grid codes requirement, which has the potential to reduce the size the AC side filter or consider the AC side filter as not necessary.

This chapter presented voltage balancing and circulating current suppression control methods for the MMC. A 7-level MMC was simulated using Matlab to demonstrate the control results. Both PS-PWM and PD-PWM schemes can precisely generate demanded control signals and eliminate most of the circulating current. A comparison between these two PWM based systems is conducted, and it shows that the PD-PWM has a faster response to the network changes while PS-PWM has fewer power losses regarding its lower switching frequency.

Chapter 4

Proposed voltage balancing control

4.1 Introduction

The Modular Multilevel Converter (MMC) has been one of the most attractive candidates in medium/high voltage applications for its greater flexibility and lower converter harmonics compared to traditional two-level or three-level thyristor-based multilevel converters [138] [139]. The MMC is also considered as one of the most efficient converters for long distance HVDC power transmission system, connecting networks with different fundamental frequencies, and distant subsea/offshore power transmission systems [140]-[143]. The MMC based transmission systems possess the ability to control the active power and reactive power flowing due to its Voltage Source Converter (VSC) structure [144]. However, in each arm of MMC, there are many submodules connected in series to step up the converter voltages. The high number of submodules not only increases the initial investment but also adds complexity to the control algorithm. Because at any given moment during the normal operation, there are a constant number of submodules being turned on whereas the rests are in bypassing mode. And the turned-on submodules are connected in series, therefore, monitoring and controlling of the DC voltage distribution among the capacitors is necessary to ensure the capacitor voltage is stable or the deviation is within the acceptable range. In [145], the primary control theories of controlling capacitor voltages are provided, the DC voltage distribution in the submodules are determined by the arm current directions and the capacitor voltages correspondingly. In [146], the voltage balancing was achieved by using an additional control loop for each submodule, forcing the capacitor voltage to follow the reference value. However, these voltage balancing approaches require voltage sensors and current sensors for the measurements of capacitor voltages and arm currents. When the voltage level of the converter increases, the number of sensors required is also increased. In the Trans Bay HVDC transmission system, 200KV, 400MW [147], there are more than 200 submodules in each arm, which are at least 1200 submodules in one substation. The investment saving by reducing the cost of sensors is significant. In [40], the capacitor voltages are balanced based on the high-frequency current components existing in the arm current when using Phase-Shifted Pulse Width Modulation (PS-PWM). However, the computation requirements are increased when the number of the submodules is increased. In [148], the Nearest Level Modulation (NLM) scheme is selected to cope with the problems caused by the high-level MMC. This is because the low

modulation frequency is preferred to avoid potential EMI effects and as well lower the switching losses. Dual sorting was also suggested in [148] to simplify the voltage balancing processes. In [149], the modified NLM was combined with the close-control-loop proposed in [146] to reduce the computation stresses. Furthermore, in [150], the capacitor voltage sorting stage is simplified to cooperate with the NLM for high-level MMC. The control topologies for the MMC not only require the control of the capacitor voltages but also involve the elimination of the circulating currents, Selective Harmonic Elimination (SHE) for low-level MMC, or fixing switching frequency [151]-[156], etc.

Both conventional and improved voltage balancing approaches are shown in Figure 29. For the conventional control approach, once the control is enabled, the voltage readings of both upper and lower arm capacitors are recorded and sorted order. At this moment, both current readings of the upper and lower arm are taken to determine the turn on/off states depending on the voltage readings recorded one step ahead. If the arm current is charging the capacitor, the submodule with the lowest capacitor voltage will be turned on with a higher priority. If the arm current is discharging the submodule, it will turn on the submodule with the lowest capacitor voltage before turning on other submodules. In this case, the communication between the voltage and current sensors is critical. The minor miscommunication will generate a small amount of voltage deviations. However, when the power rating of the converter is large, the UHVDC related applications, it will generate a significant amount of losses. Therefore, the proposed predictive voltage balancing control simplifies the measurement of the arm currents and the communication of the related sensors. The proposed voltage balancing control is generated based on the capacitor voltage samples. The computational requirements are significantly reduced when the converter voltage level is high. The reduced use of the current sensors not only reduces the cost for sensors but also simplifies the control approach. The comparisons between the proposed control approach and the conventional voltage balancing method indicated that the predictive control could reach the same system performances as the conventional method. Further study shows that the predictive control has higher immunity to the sampling frequency distortion than the standard voltage balancing control when the sensor sampling rate is high. Nevertheless, the cost of increasing the sampling rate and the sensor losses are presented in [157]-[159]. The cost increase, compare to the benefits, are negligible.

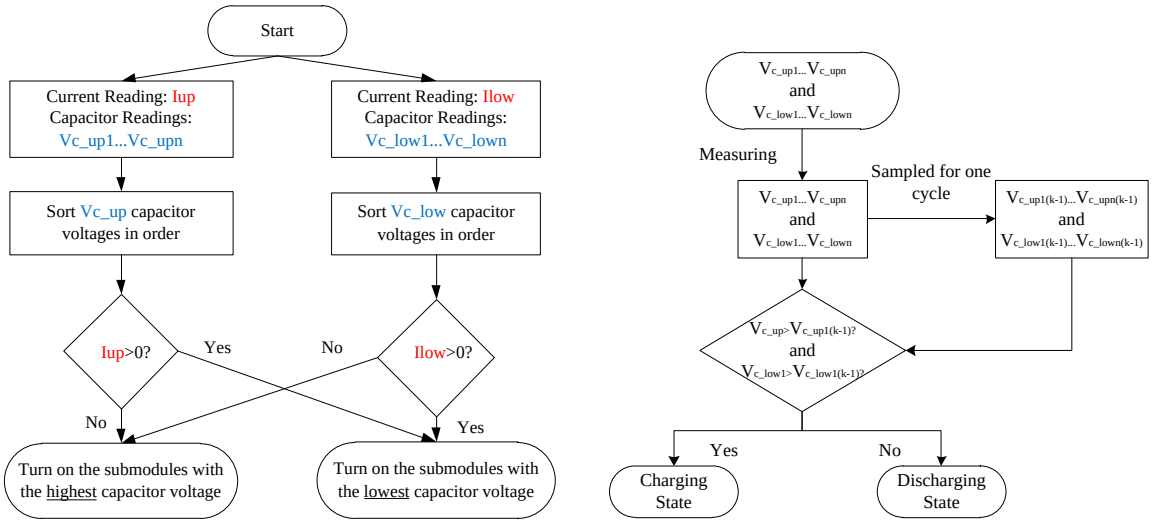


Figure 29: Flow chart of the (a) conventional voltage balancing (b) proposed voltage balancing controlling approach during normal operations.

4.2 Modelling

The structures of the MMC may vary based on the application requirements. Defined by the components inside one submodule, there are half-bridge MMC, full-bridge MMC, and hybrid MMC. The half-bridge MMC structure uses the least number of elements, and the investment saving is significant when the voltage level is high. Considering the simplicity and the economic benefit, the half-bridge MMC is preferred over other structures. Each submodule is connected to a voltage sensor in order to monitor the capacitor voltage. The $V_{c\_up1} \dots V_{c\_upn}$ are the capacitor voltage measurement for each submodule of the upper arm respectively, the $V_{c\_low1} \dots V_{c\_lown}$ are the capacitor voltage measurement for each submodule of the lower arm respectively. The series connection of the submodules can generate relatively small voltage steps when the number of the submodules is significant. Therefore, reducing the requirements of the filter at AC side or even considering the filter as unnecessary if the number of submodule is sufficient. The submodules are then connected with the line inductors L_s to limit the fault current. The DC side is supplied by the DC sources V_{dc} to provide the power from the DC side to AC side because the passive R and L load are connected beyond the point of common coupling. Besides the measurement of the capacitor voltages, the upper arm current I_{up} and the lower arm current I_{low} are also important indicators to perform the conventional voltage balancing control. However, the arm currents measurements are not necessary for the proposed predictive voltage balancing control, which is more flexible and adds simplicity to the future control system.

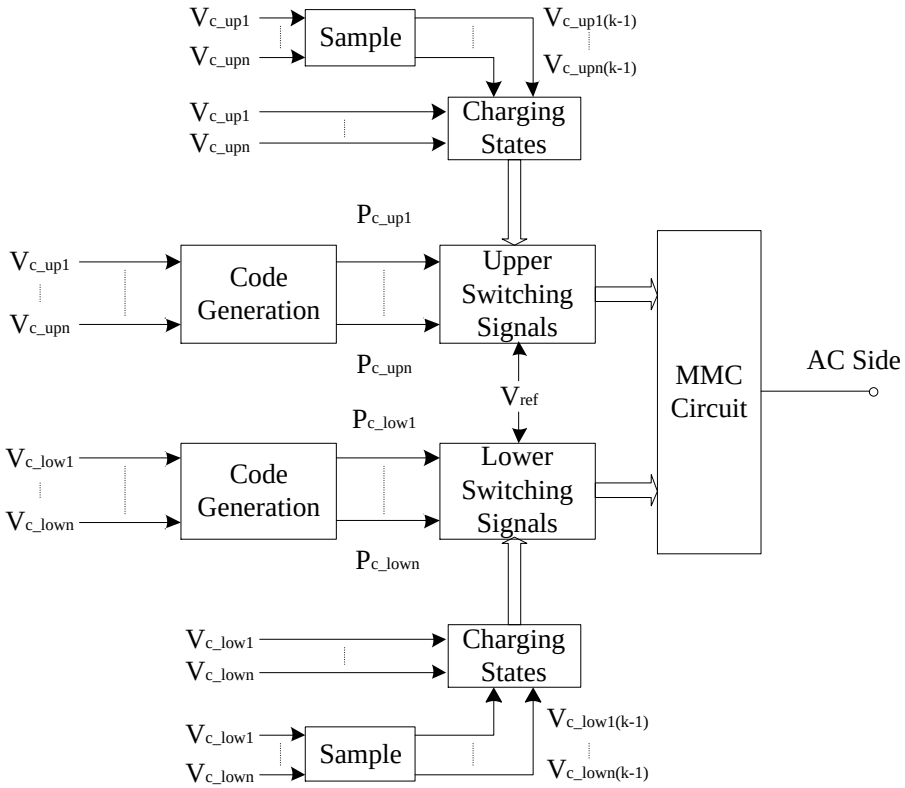
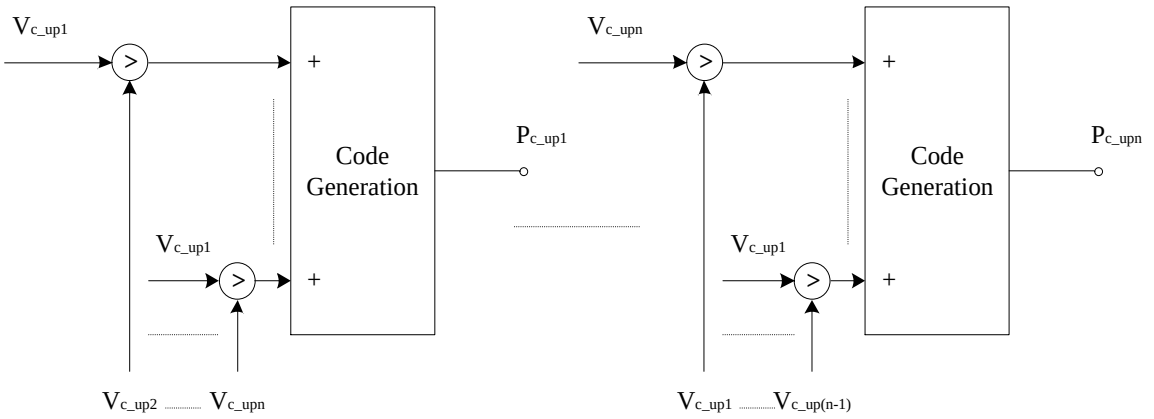


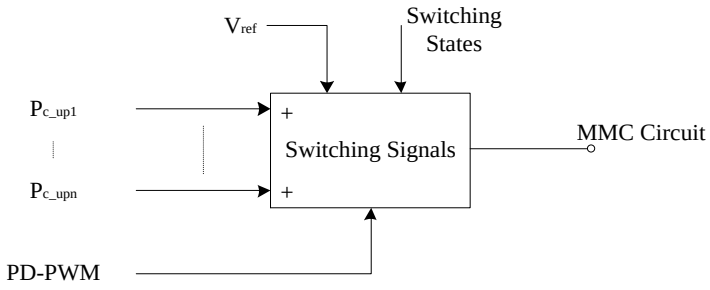
Figure 30: The proposed voltage balancing control scheme implemented in the simulation model.

The measurements recorded in Figure 29 (b) are then transmitted into the control unit as shown in Figure 30. Then the control unit generates corresponding gate signals depending on the priority code generated based on Figure 31. Then the control signals are transmitted to the MMC circuit to charge or discharge the capacitor. There are two power switches and one capacitor inside each submodule for the half-bridge structure MMCs. The current flowing into the capacitor can charge or discharge the capacitor depending on the current direction. The concept forms the fundamental theories of the voltage balancing control of the MMC:

- $V_{c\_out} = V_c$: The submodule is in ON mode when S_1 is on and S_2 is off, the capacitor inside the submodule is connected to the circuit directly.
- $V_{c\_out} = 0$: The submodule is in OFF mode when S_1 is off and S_2 is on, the capacitor inside the submodule is disconnected from the circuit and the current flowing is still able to pass through the submodule.



(a)



(b)

Figure 31: The generation of the (a) priority code (b) switching signal for the proposed voltage balancing control.

4.3 Mathematical representation of the MMC

Based on the assumption that the submodule uses ideal switches, the in-series connected submodules can be represented as the voltage sources in both upper arm and lower arm. The converter output voltage V_{out} can be expressed in (35):

$$V_{out} = \frac{V_{dc}}{2} - V_{c\_up} - V_{diff\_up} = \frac{-V_{dc}}{2} + V_{c\_low} + V_{diff\_low} \qquad (35)$$

Where V_{c_up} is the equivalent voltage source in the upper arm, V_{c_low} is the equivalent voltage source in the lower arm, V_{diff_up} and V_{diff_low} are the differential voltage of the upper arm inductor and the lower arm inductor respectively.

The arm current can be represented as shown in (36)-(38):

$$I_{up} = \frac{I_{out}}{2} + I_{diff} \qquad (36)$$

$$I_{low} = \frac{I_{out}}{2} - I_{diff} \quad (37)$$

$$V_{diff\_up} = V_{diff\_low} = Ls\frac{dI_{diff}}{dt} \quad (38)$$

In (36)-(38), where I_{diff} is the inner unbalanced current flowing in the arms. The existence of the inner unbalanced current causes the voltage differential at both upper arm and lower arm, therefore, giving rise to more differential currents flowing in the arms. On the other hand, the converter voltage steps are achieved by integrating the submodules as shown in (39) and (40):

$$V_{c\_up} = \sum_{k=1}^{n} N_{c\_upk} V_{c\_upk} \quad (39)$$

$$V_{c\_low} = \sum_{k=1}^{n} N_{c\_lowk} V_{c\_lowk} \quad (40)$$

Where N_{c_upk} and N_{c_lowk} are the switching states of the submodules at the upper arm and lower arm respectively. The switching states in the equations equal to one when it is in ON mode, and it equals to zero if it is in OFF mode. According to (35)-(40), the converter output voltage is determined by the switching signals for each submodule. Therefore, the fundamental concept of controlling the capacitor voltages is turning on the constant number of submodules to make sure the DC voltages are distributed evenly among them, so that the capacitor voltage can remain constant or drifting within the acceptable range.

The capacitor voltage deviations are shown in Figure 32 along with different sampling time. The capacitor deviation starts to drop significantly above 0.7ms when using the conventional voltage balancing method, whereas the proposed voltage balancing approach has a smoother capacitor deviation along the sampling period changes. Nevertheless, the proposed voltage balancing approach appears to have smaller capacitor voltage deviations than the conventional voltage balancing method with different sampling period. When the sampling period is at 1.1ms, the capacitor deviation difference between the proposed approach and the conventional approach can be as high as 14%. When the sampling period is smaller, such as 0.1ms to 0.5ms, the differences of the capacitor voltage deviation are still around 4%.

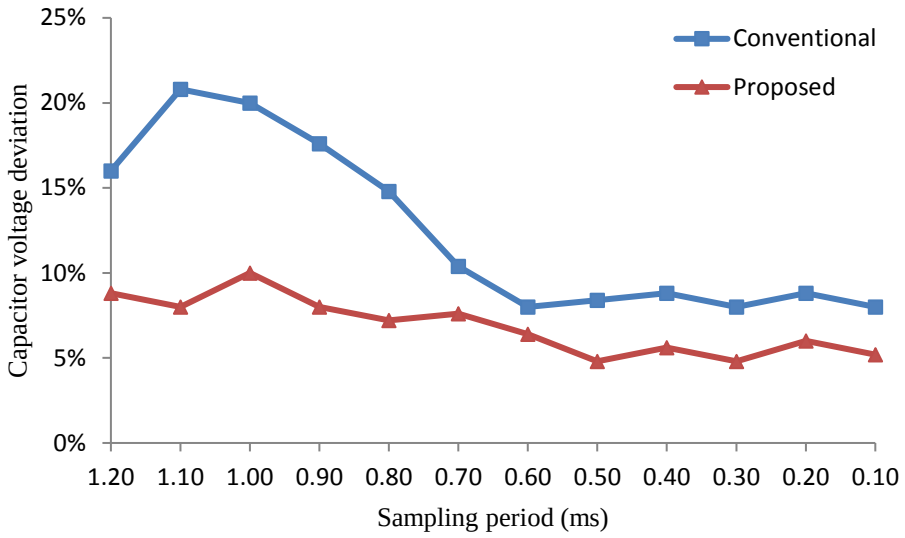


Figure 32: The capacitor voltage deviations with different sampling periods.

The sampling period of control could have a great impact on the performance of the converter even during normal operations. Tu has investigated the performance of the converter regarding different sampling frequency in [162]. He mentioned that there are lower limit f_1 and upper limit f_2 for the sampling frequency f_0 as shown in equation in (41) and (42). If the sampling frequency is much lower than the lower limit frequency f_1, it will generate a large amount of distortions at the output end. If the sampling frequency is higher than the upper sampling frequency f_2, it will be consuming more energy for less performance improvement.

$$f_1 = \pi \cdot f_0 \cdot \sqrt{2kN_{sm}} \quad (41)$$

$$f_2 = \pi \cdot f_0 \cdot k \cdot N_{sm} \quad (42)$$

Where k is the modulation index for the reference signal,· N_{sm} is the number of submodule in each arm.

With the guidance of the equation in (41) and (42), the range of the sampling frequency can be determined. In Table 12, the upper and lower limits of the sampling frequency are calculated. Based on the configurations of present MMC based transmission systems, in order to construct the 800kv UHV transmission line, there should be at least 800 submodules in each arm. Therefore, according to Table 12, the maximum sampling period could be 1.062ms when there are only 20 submodules or 0.009ms when there are 820 submodules in each arm.

Table 12: The range of the ideal sampling period with different number of submodules

Voltage levels (Nsm)	Lower frequency (Hz)	Upper frequency (Hz)	Lower Sampling period (ms)	Upper Sampling period (ms)
20	942	2826	1.062	0.354
120	2307	16956	0.433	0.059
220	3124	31086	0.320	0.032
320	3768	45216	0.265	0.022
420	4317	59346	0.232	0.017
520	4803	73476	0.208	0.014
620	5245	87606	0.191	0.011
720	5652	101736	0.177	0.010
820	6032	115866	0.166	0.009

However, the maximum sampling frequency is ideal and difficult to achieve due to the large number of submodules and the consequent large computation stress. One of the evidences of the increasing computation stress is the employing of the Nearest Level Modulation (NLM) when the number of submodule is increasing. It is believed that the NLM is more efficient than the PS-PWM or PD-PWM when the number of the submodule is large. However, the poor performance of the MMC using NLM is preventing NLM to be implemented in MMC with smaller number of submodules [163]. In this case, Li has provided a modified NLM approach to improve the performance of the NLM on MMC with low number of submodule [164]. That gives the general idea of how NLM is implemented in the MMC based system and further reveals the needs for NLM when the computation stress of the application is high.

Considering the ideal applications of MMC, the proposed approach can have a significant savings compared to the conventional voltage balancing control. In the UHV transmission lines, even 1% performance improvement could result in thousands or millions money savings. Furthermore, in order to reduce the initial investment of the substation/converter, the selection of the capacitor and inductor can be predicted to be as smaller as possible to reduce both the size and the cost. As a consequence, it will generate more current noises in each arm due to the circulating and resonant currents, which increases the possibility of the current sensor failure. In this case, the proposed voltage balancing approach avoids the situation by using the capacitor voltage samples to derive the charging/discharging states, which potentially lower the requirement for the passive components, hence the initial investment. On the other hand, it simplifies the control process which is critical when the computation cycle is another important factor to be considered when the number of voltage level is high.

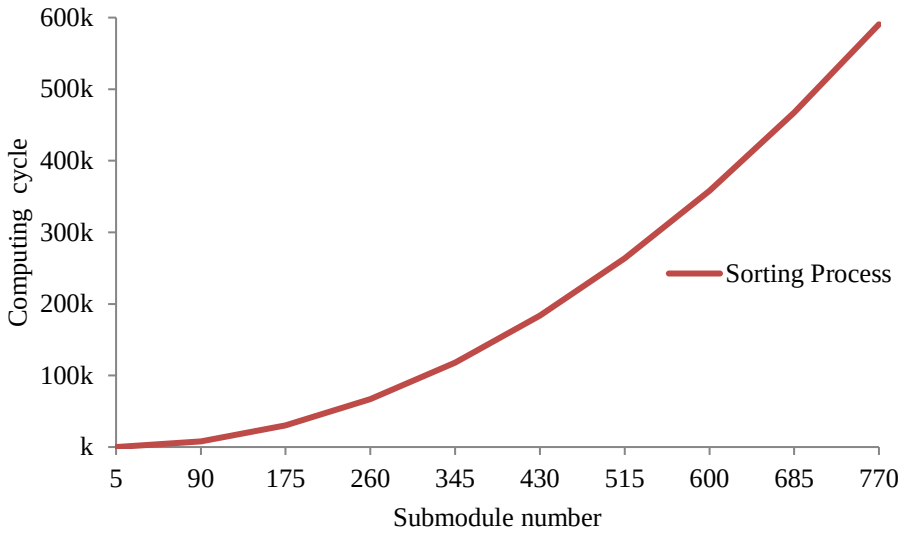


Figure 33: The computation cycle with different submodule numbers

It is shown in Figure 33 that with the increasing number of submodule, the computation stress is also increased exponentially. It can be up to 400k times of calculations during one operation cycle when the number of voltage level is at 685. Therefore, the computation stress can be foreseen when implementing the UHV applications.

4.4 Proposed control approach

The proposed control scheme is displayed in Figure 30, where all the capacitor voltages are monitored and transferred to the control unit for gate signal generation purposes. In this case, the priority codes are generated to simplify the voltage balancing processes, $P_{c\_up1} \ldots P_{c\_upn}$ are the priority codes for each submodule based on its capacitor voltage in the upper arm, P_{c_low1} and P_{c_low1} are the priority codes of each submodule based on its capacitor voltage in the lower arm. Figure 31 (a) shows the generation of the priority codes regarding the capacitor voltages. For example, the priority code of V_{c_up1} is to be determined. V_{c_up1} is compared with every other capacitor voltages to get the unique code for V_{c_up1} itself, etc. The priority codes are then sent to the switching generation controller as shown in Figure 31 (b).

$$\sum_{k=1}^{n} N_{c\_upk} \cdot C_{upk} \int_{t}^{t+Ts} \left(\frac{Sin(\omega_s t+\theta)}{2} + I_{diff}\right) dt < V_{c\_up} \cdot 10\% \qquad (43)$$

$$\sum_{k=1}^{n} N_{c\_lowk} \cdot C_{lowk} \int_{t}^{t+Ts} \left(\frac{Sin(\omega_s t+\theta)}{2} - I_{diff}\right) dt < V_{c\_up} \cdot 10\% \qquad (44)$$

In the conventional voltage balancing method, the arm currents are measured to determine the charging and discharging states of the submodule corresponding to directions of the arm

currents. However, the proposed predictive control takes advantage of the sampling actions of the control unit. Figure 31 (a) demonstrates the algorithm of the proposed control. The measured upper and lower arm capacitor voltages V_{c_up} and V_{c_low} are compared to the samples $V_{c\_up(k-1)}$ and $V_{c\_up(k-1)}$ taken by the control unit one operation cycle ahead.

However, based on (41) and (42), the maximum period of the operation cycle is determined by the capacitor voltage variations. The proposed voltage balancing should be able to limit the capacitor voltages within restraints. As demonstrated in (43) and (44), the lower margin of the sampling frequency which is aiming to reduce the capacitor variations can be determined. However, the computation requirements must also be considered to demonstrate the feasibility of the proposed voltage balancing control. Since the operation cycle is involved, the sampling frequency of voltage sensor becomes critical to the converter performance. According to [165], the sampling rate of the reference has a significant impact to the harmonics of the converter output. On the other hand, [166] has investigated the power losses related to the sensors in different sampling frequency conditions. The losses are small compared the overall power transmitted. Therefore, the proposed predictive voltage balancing control can easily fit into the current control system without any modifications.

4.5 Simulation validation

The simulation model was designed to evaluate the performance of the proposed voltage balancing approach regarding the changes of the modulation index, sampling frequency, and the disable/enable transience. The parameters for the simulation model is shown in Table 13.

Table 13: The parameter used in the simulation to verify the proposed voltage balancing approach.

Parameters	Values
MMC power rating, P (W)	100
DC-link voltage, V_{dc} (V)	+/-50
Load resistance, R(Ω)	12.5
Load inductance, L(H)	0.001
Phase inductance, L_s(H)	0.001
Capacitance, C(F)	0.002
Submodule reference voltage, V_{sub}(v)	25
No. of submodules in each arm, N	4
Carrier frequency, f (kHz)	1

In order to match the simulation model with the experiment in future, the power rating was selected at 100w, which is the same as the experimental test rig. The voltage source at the DC side is +/- 50 V. The load and in-series inductors were selected at 1mH since it is within the range as calculated in Chapter 2.3. The selection of the capacitor is as the same as calculated in Chapter 2.3. The number of the submodule was four, so that it will generate five voltage steps with the mid-point located at the zero voltage.

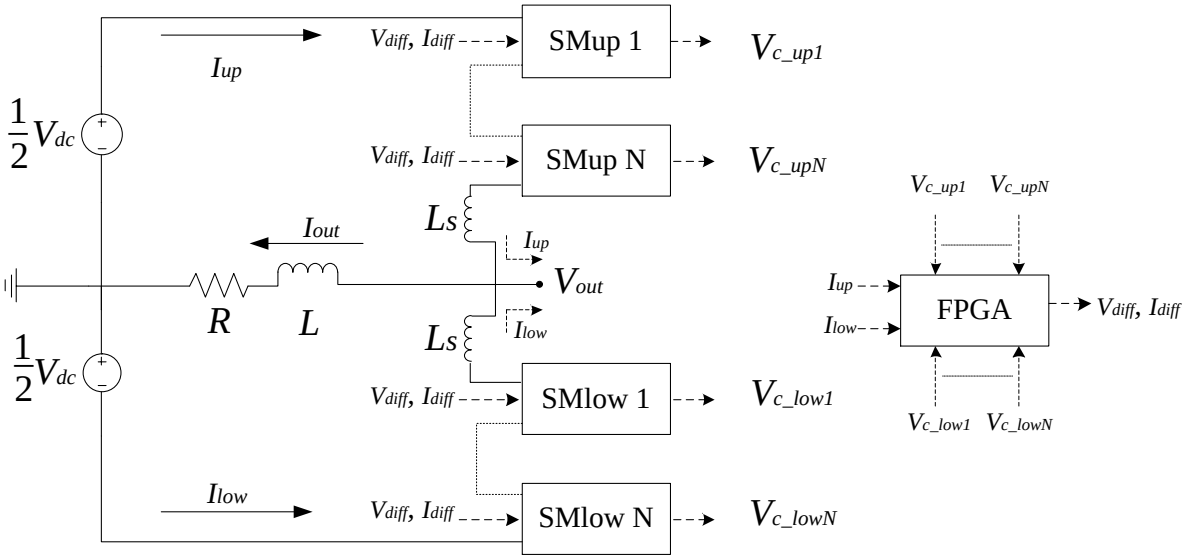


Figure 34: The simulation model of the single phase MMC.

The model was built based on the structure shown in Figure 34. In both upper and lower arms, there are four submodules. Since they are connected in series, the current flowing into the submodule is either zero or the same as the arm currents. The capacitor voltage for the upper arm are measured as $V_{c\_up1} \ldots V_{c\_upn}$, for the lower arm are measured as $V_{c\_low1} \ldots V_{c\_upn}$. The difference voltage generated by the imbalanced capacitor voltage for the upper and lower arms are V_{diff_up} and V_{diff_low} separately. The upper and lower arm current are I_{up} and I_{low}. The output voltage and current are I_{out} and V_{out} respectively. As shown in Figure 34, the measured signals, such as $V_{c\_up1} \ldots V_{c\_upn}$, $V_{c\_low1} \ldots V_{c\_upn}$ are transmitted in to the FPGA. Therefore, the primary control signals, such are generated to produce the gate signals. In the Simulink model, the FPGA is represented by several control blocks in order to perform the calculation.

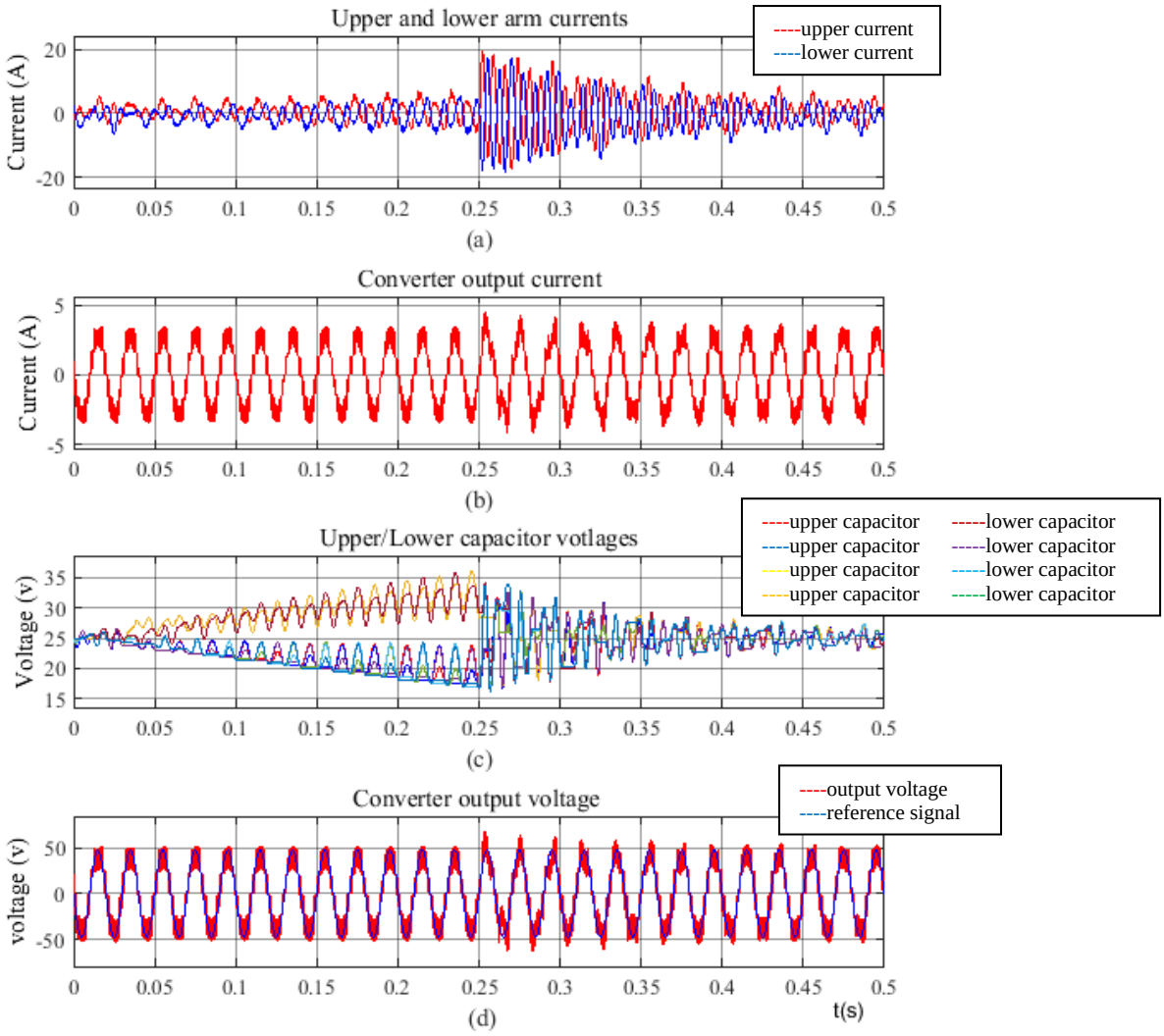


Figure 35: The converter (a) upper and lower arm currents (b) the current output (c) upper and lower arm capacitor voltages (d) voltage output when the sampling frequency is insufficient.

To test the feasibility and the dynamic performance of the proposed voltage balancing control, a single-phase MMC based inverter has been built in MATLAB. The model is running in the discrete mode with $1us$ time steps since the maximum frequency in the HVDC simulation model is 1 kHz, which has a minimum time step of $1ms$. Running in discrete mode with $1us$ time steps guarantees the accuracy of the system which is 1% of the minimum time steps and the simulation time required is also significantly reduced.

Described in Figure 35, in the same sampling frequency condition where the samples taken are insufficient, the proposed predictive voltage balancing control can still maintain the capacitor voltages at the nominated level with fewer variations than the original voltage balancing control. When the proposed voltage balancing control is activated at 0.25s, the upper and lower arm current shown in Figure 35 (a) contains a significant amount of circulating current

with the peak value increasing from 7.2A to 19.5A (170.8%). However, as expected, the circulating currents have limited effects on the converter output current as displayed in Figure 35 (b). The deviation of the upper and lower arm capacitor voltages are shown in Figure 35 (c) before 0.25s when the sampling frequency is low. As observed in Figure 35 (d), the converter output voltages can return to steady states when the proposed voltage balancing is activated after 0.25s.

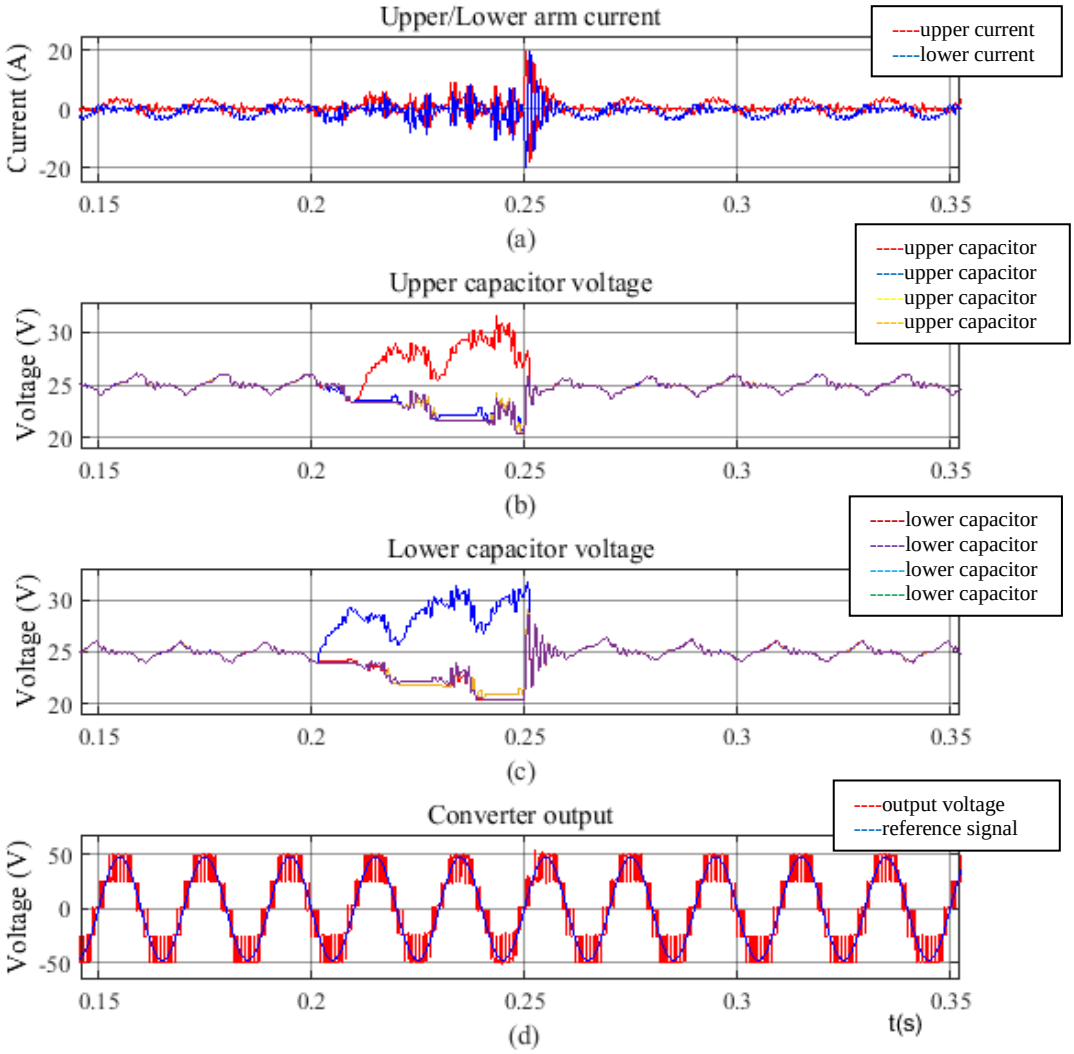


Figure 36: The voltage balancing is disabled at 0.2s and enabled again at 0.25s (a) upper and lower arm current (b) upper arm capacitor voltages (c) lower arm capacitor voltages (d) load voltage and reference signals

The voltage balancing control is disabled at 0.2s and enabled again at 0.25s as shown in Figure 36,When the voltage balancing is disabled, the capacitor voltage deviations are observed in both of the upper and lower arm as shown in Figure 36 (b) and Figure 36 (c)**.** The upper and lower arm currents are affected by the imbalanced upper and lower arm capacitor

voltage as well. As shown in Figure 36 (a), they generated 400% more ripple when the voltage balancing is disabled, although the upper and lower currents magnitudes have changed by nearly five times. The output waveform has not changed significantly as shown in Figure 36 (d), and only a small ripple is observed. In combination with (1)-(4), the I_p and I_n have not changed much, further indicating that the circulating current existing inside the converter is generated by the capacitor voltage imbalance and it has limited effect on the output waveform.

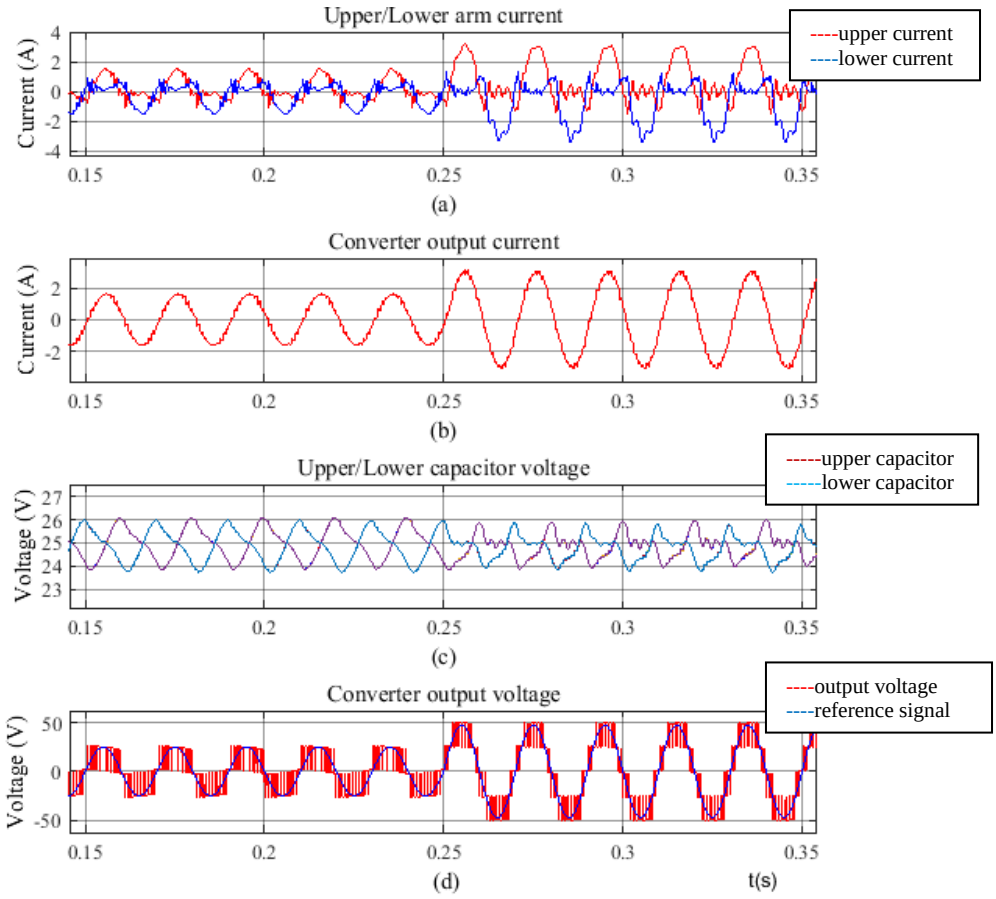


Figure 37: The simulation results (a) the upper and lower arm current (b) the load current (c) upper and the lower arm capacitor voltages (d) load voltage with reference signal when the modulation index changes from 0.5 to 0.95 at 0.25s

The modulation index was changed from 0.5 to 0.95 at 0.25s as demonstrated in Figure 37 to test the dynamic performance of the proposed control. It can be seen that in Figure 37 (a), the upper arm current and the lower arm current are acting as the positive and negative halves of a sinusoidal waveform, and which are forming the converter output current as shown in Figure 37 (b). However, the harmonics displayed in Figure 37 (a) are generated by the circu-

lating current existing at twice the fundamental frequency. The control of the circulating currents is not included. As shown in Figure 37 (c) the upper and lower arm capacitor voltages are balanced within a certain range from 25.7v to 24.7v whereas the nominal voltage is 25v, the voltage variation is 2.8% which is within the variation range agreed by the grid codes. However, the performance and the voltage variation ranges are different according to the voltage level of the application. The output voltage as shown in Figure 37 (d) has five voltage steps when the four submodules in each arm are fully activated. Before 0.2s, there are only three voltage levels as the modulation index is only 0.5 and only two submodules are turned on at the same time. By integrating a large number of the submodules, the voltage steps are relatively small. Furthermore, because of the characteristics of the MMC, it is easier to increase the number of converter voltage levels compared to the other types of conventional converters. Figure 37 demonstrates that the proposed predictive voltage balancing control has a fast system response regarding the modulation changes as it can reach the steady states within one operation cycle.

4.6 Experimental results

An experiment test rig has been built to verify the simulation results of the new voltage balancing method. The power rating of the experimental test rig has been scaled down as shown in Table 14. The test rig circuit has the same structure as the simulation model demonstrated in Figure 21.

Table 14: Parameters Used For Experimental Model

Symbol	Parameters	Values
$\boldsymbol{P}$	Rated Active Power	3.33W
$\boldsymbol{V_{ac}}$	AC Voltage RMS	7.07V
$\boldsymbol{R}$	Load Resistance	15Ω
$\boldsymbol{L}$	Load Inductance	1mH
$\boldsymbol{C_{sub}}$	Capacitance of SM	1mF
$\boldsymbol{V_c}$	Capacitor voltage	5V
$\boldsymbol{L_s}$	Arm inductance	1mH
$\boldsymbol{N}$	NO. of Submodules	4
$\boldsymbol{V_{dc}}$	DC voltage	20V

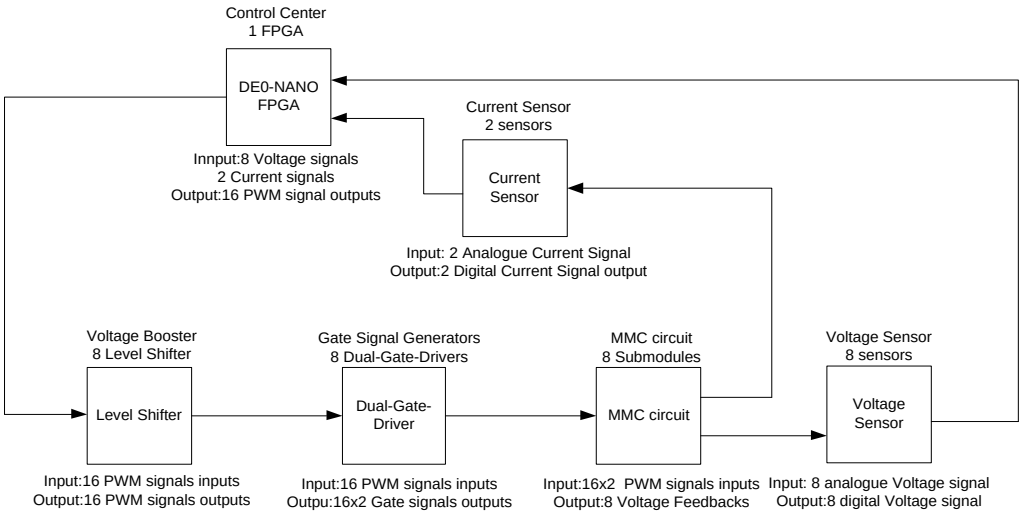


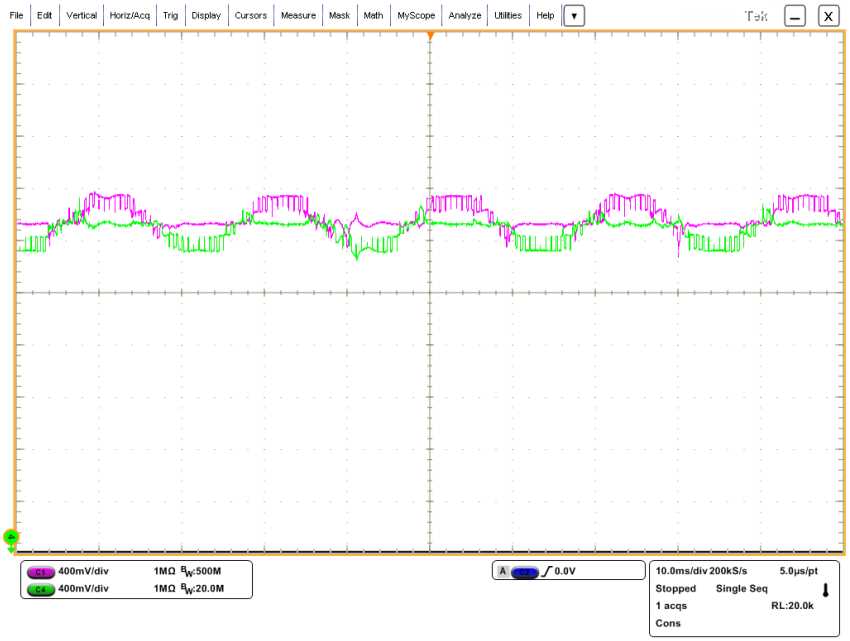
Figure 38: The flow diagram of the experiment model.

Because of the requirement for a large number of gate drive signals in the MMC circuit, it was decided to use a Field Programmable Gate Array (FPGA) rather than a micro controller to complete the test rig. Therefore, the DE0-NANO FPGA evaluation board from Altera is selected as the control unit in the test rig. Considering the number of I/O pins when there are four submodules in both upper and lower arms, each submodule needs four I/O pins for gate signals, and therefore 32 pins are required for switching signals. In addition to the gate signals, the control unit is receiving the capacitor voltage feedback signals for monitoring purposes. That results in a total pin number of 40 whereas there are 153 maximum FPGA I/O pins in aforementioned control unit. The clock speed is 50MHZ, which is sufficient for a four-level MMC control. The flow diagrams are shown in Figure 38. A total number of 16 PWM signals are sent into the level shifters for voltage compatibility with the dual-gate drivers. The dual-gate drivers can generate the corresponding gate turn on/off signals which are complementary two pairs of gate signals. There are N analogue voltage sensors, each connected in parallel with the capacitor inside each submodule to monitor the voltage changes during the normal operation. The capacitor voltage signals are sent back to DE0-NANO for use with the voltage balancing scheme.

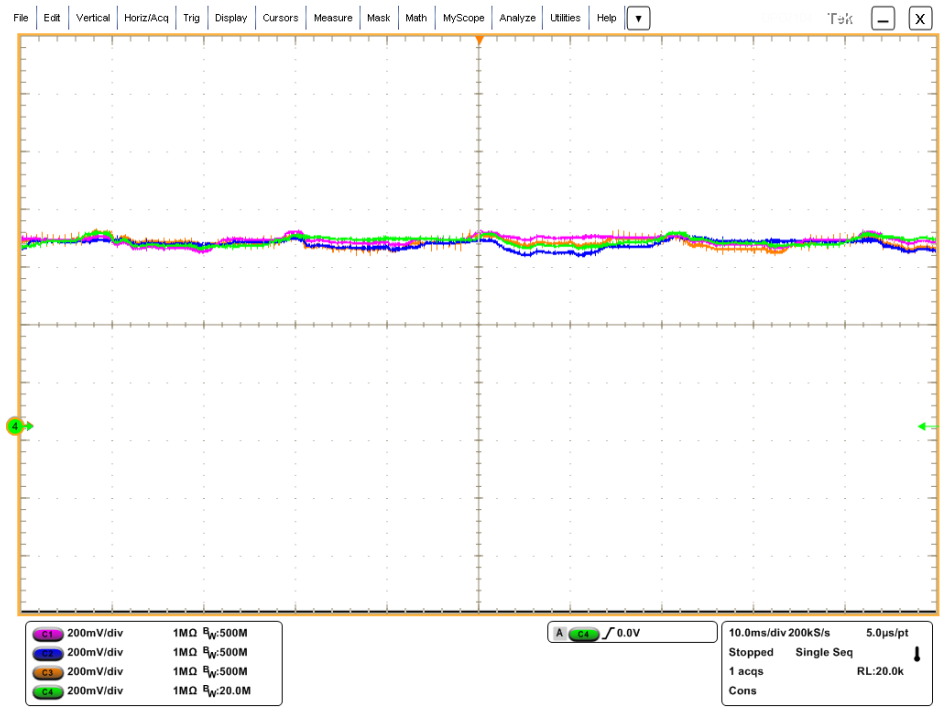
The experimental results during normal operations are shown in Figure 39, where the modulation index MI is 0.95 and fundamental frequency F is 50Hz. The voltage output V_{out} has 5-level voltage steps as the total number of the submodules N in both upper and lower arm is four. The upper arm current I_{up} forms the positive part of the output current while the lower arm current I_{low} is forming the negative part of the output current I_{out}. The upper and lower

arm current readings are provided by the current sensors connected in series with the DC voltage source. The upper and lower capacitor voltages are shown in Figure 39 (c) and Figure 39 (d) respectively. It has been demonstrated that, with the proposed predictive voltage balancing control, the capacitor voltage inside each submodule can be maintained with a minimum voltage ripple of < 4.3%. The parameters used in this converter follow the specifications given in Table 16.

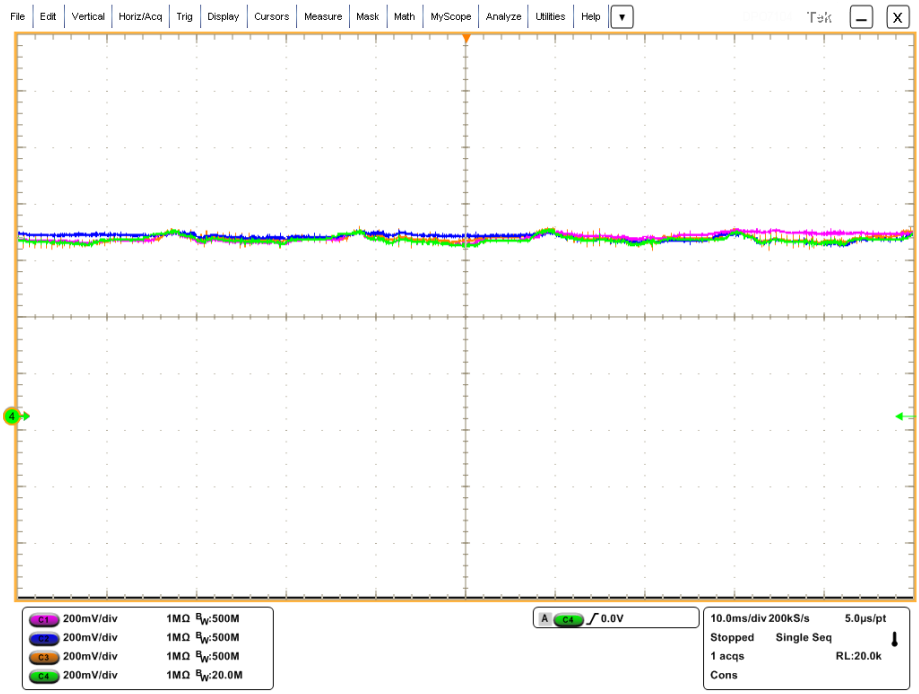
(a) output voltage (V_{out}) (5V/div)



(b) upper arm current (I_{up}) and lower arm current (I_{low}) sensor readings(400mv/div)



(c) upper arm capacitor voltage (V_{c_up1}, V_{c_up2}, V_{c_up3}, V_{c_up4}) (200mv/div)

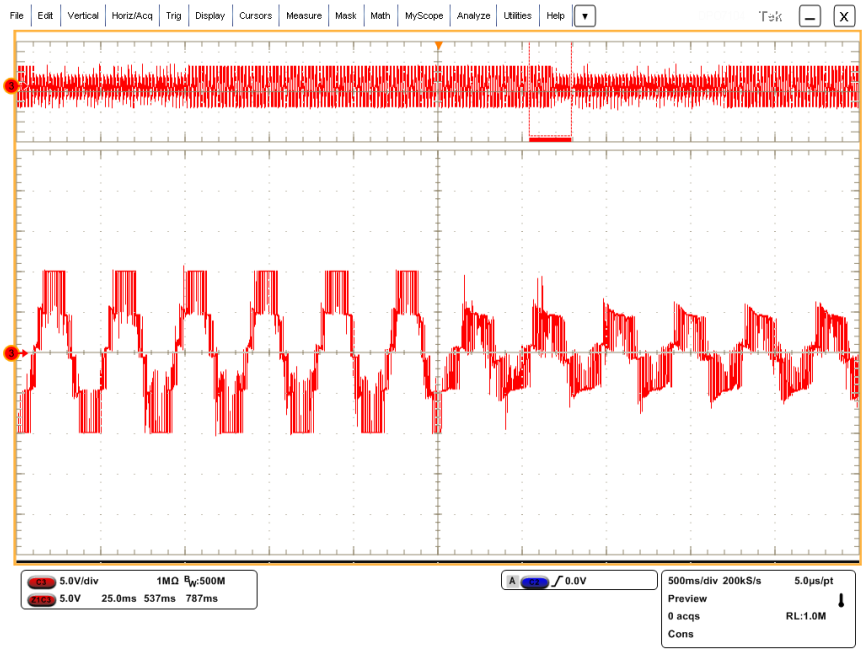


(d) lower arm capacitor voltages (V_{c_low1}, V_{c_low2}, V_{c_low3}, V_{c_low4}) (200mv/div).

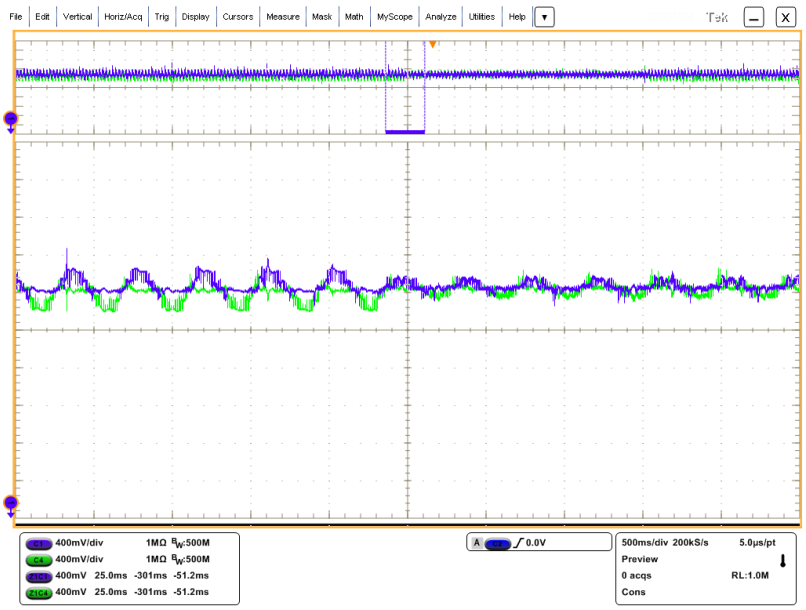
Figure 39: Experimental results during normal operation using new voltage balancing control where MI=0.95, F =50Hz.

The dynamic response of the proposed voltage balancing control is displayed in Figure 40. The modulation index MI was initially set at 0.95, and then changed to 0.5 at 0.25s. The converter voltage level was decreased from five to three as observed in Figure 40 (a). The upper

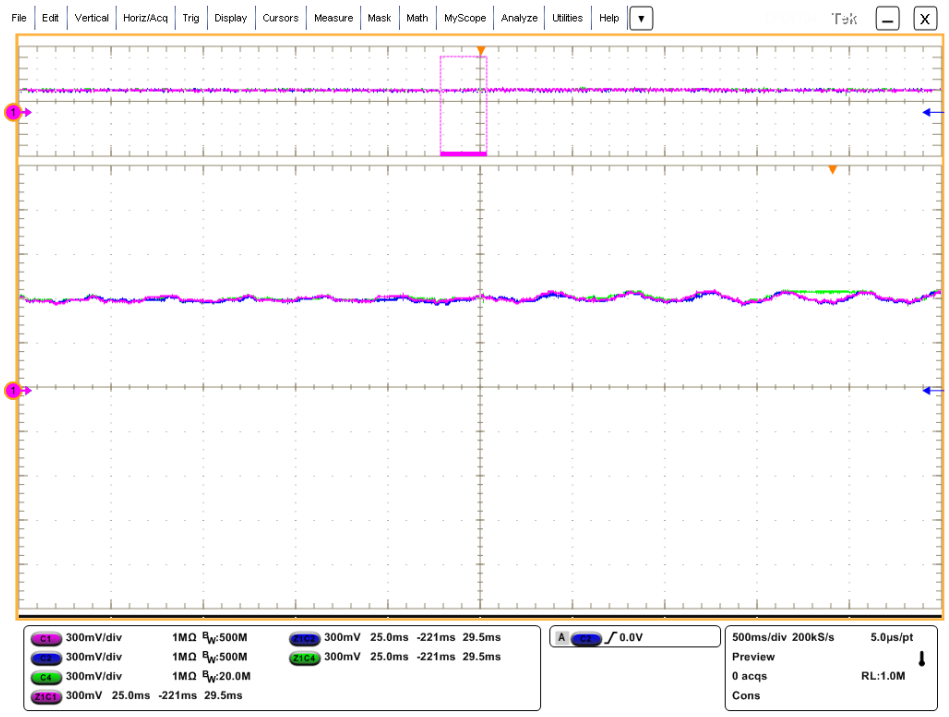
and lower arm capacitor voltages tend to have more ripple as demonstrated in Figure 40 (c) and (d), but the ripple level can still meet the grid code requirement (less than 6.1%) using the predictive voltage balancing control. The upper arm and lower arm currents are shown in Figure 40 (b). Because the converter is connected to a passive load, the lower converter voltage results in the converter output current drops. Figure 40 has shown that under different conditions, the proposed voltage balancing can maintain the required capacitor voltage levels. It also shows the scheme's ability to control the capacitor voltages when there is a sudden change at MI.



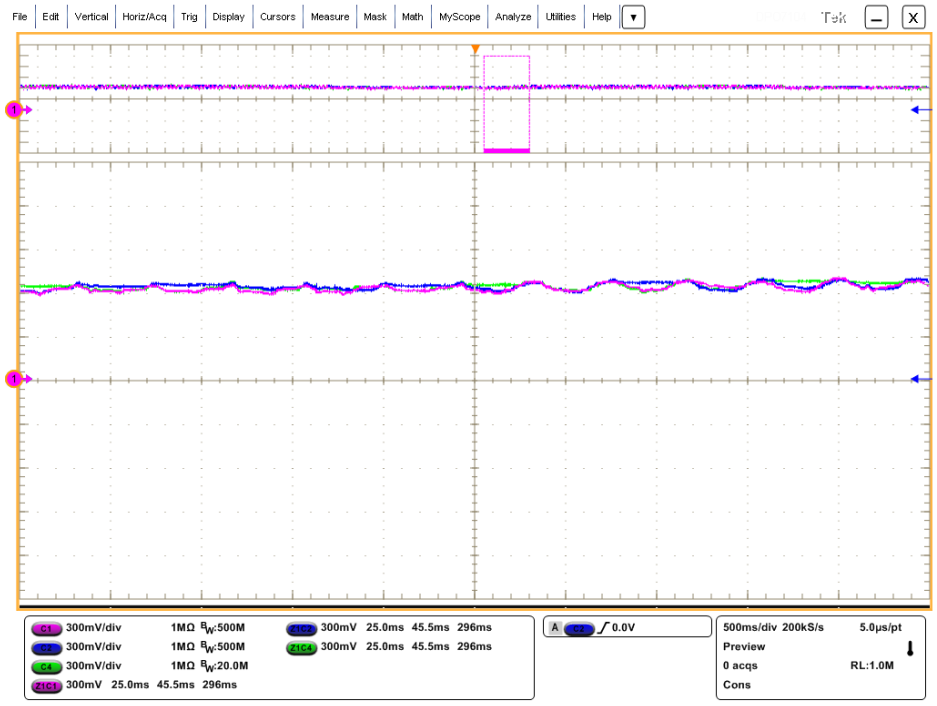
(a) output voltage (V_{out}) (5V/div)



(b) upper arm current(I_{up}) and lower arm current (I_{low}) sensor readings(400mv/div)



(c) Upper arm capacitor voltage (V_{c_up1}, V_{c_up2}, V_{c_up3}, V_{c_up4}) (200mv/div)

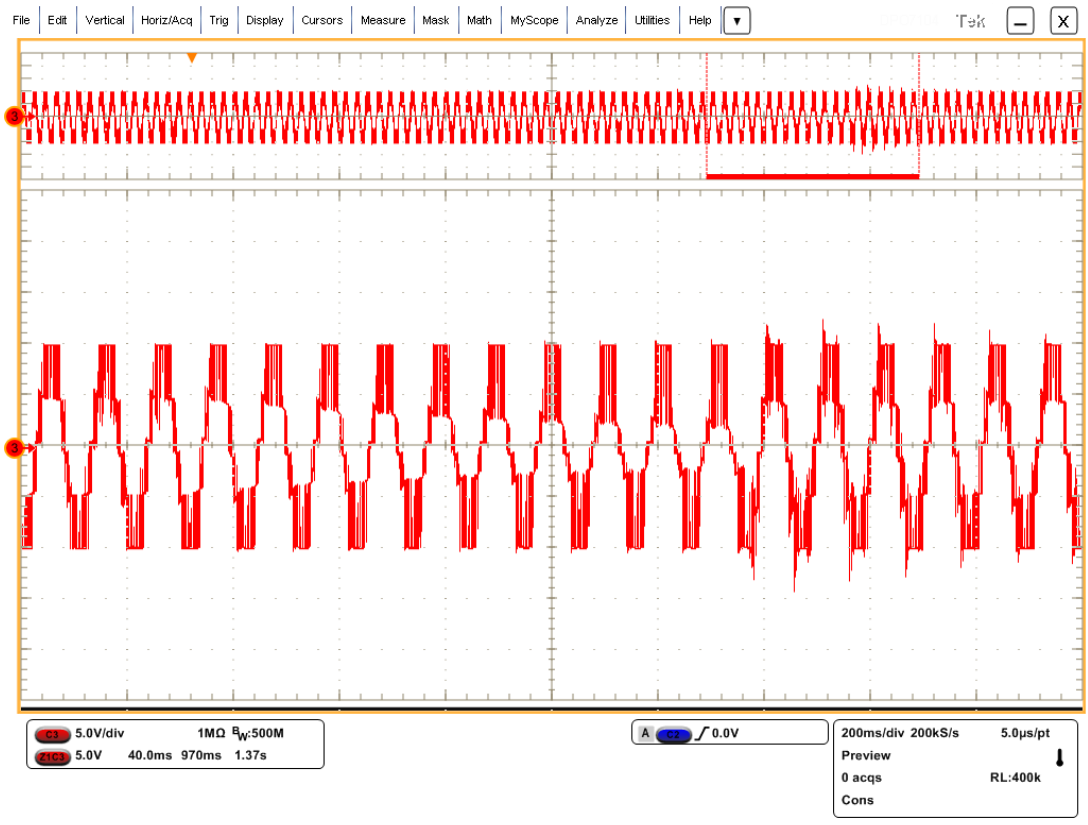


(d) lower arm capacitor voltages (V_{c_low1}, V_{c_low2}, V_{c_low3}, V_{c_low4}) (200mv/div).

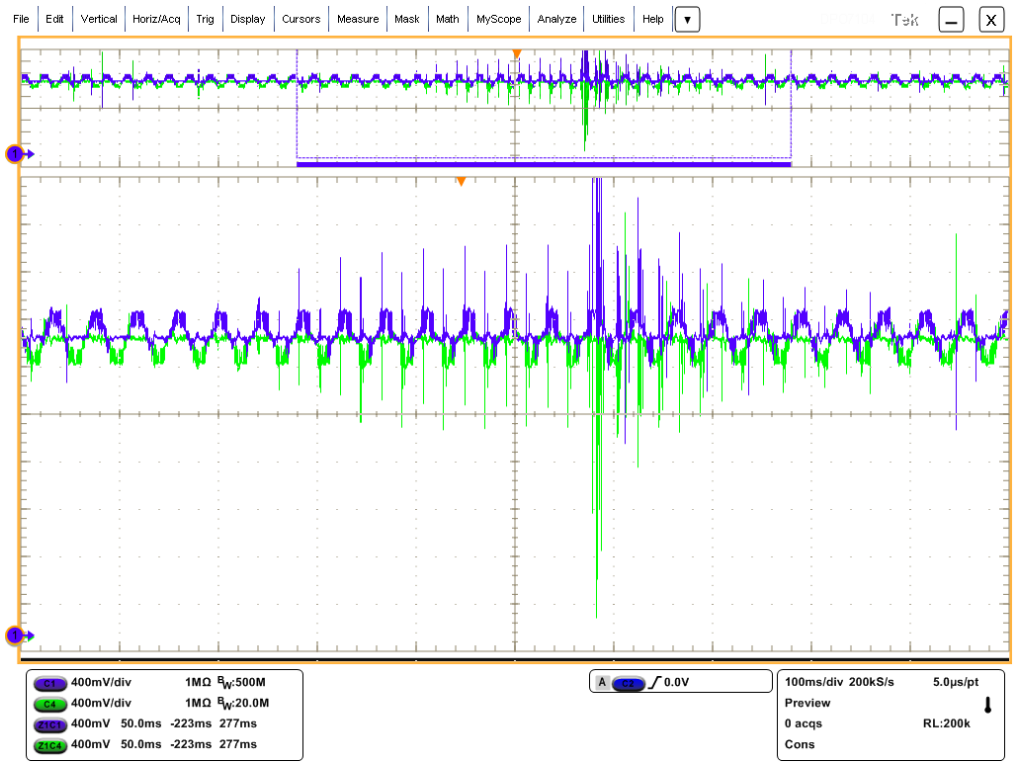
Figure 40: Experimental results for the new voltage balancing control where MI has changed from 0.95 to 0.5.

The proposed voltage balancing method is disabled for a short period as shown in Figure 41. The converter maximum and minimum output voltages remain at $\pm$10V, but there are slow deviations observed at the intermediate voltage steps since the DC voltage distribution among

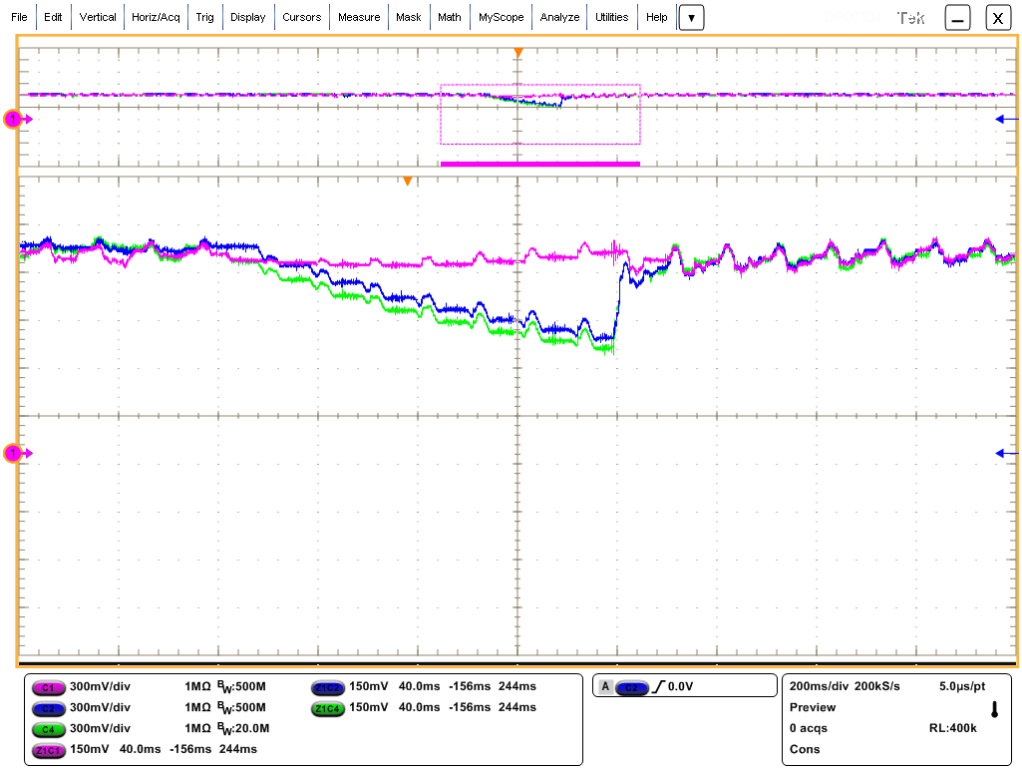
the submodules is not balanced. The converter output voltage can recover to the steady state when the voltage balancing control is enabled again as observed in Figure 41 (a). In Figure 41 (b) and (c), the upper and lower arm capacitor voltages start drifting due to lack of control. However, at the time when the voltage balancing control is enabled again, the capacitor voltages are controlled within the nominal range in less than a half cycle of operation. The increased voltage differences among the capacitors cause up to 285% of circulating current as shown in Figure 41 (b). This generates a large number of low-order harmonics in both upper arm and lower arm currents. Once the voltage balancing control is enabled again, both upper and lower arm capacitor voltages can recover to the appropriate steady state values. As a result, the circulating current components existing in the upper and lower arm current are also suppressed after re-enabling the voltage balancing control.



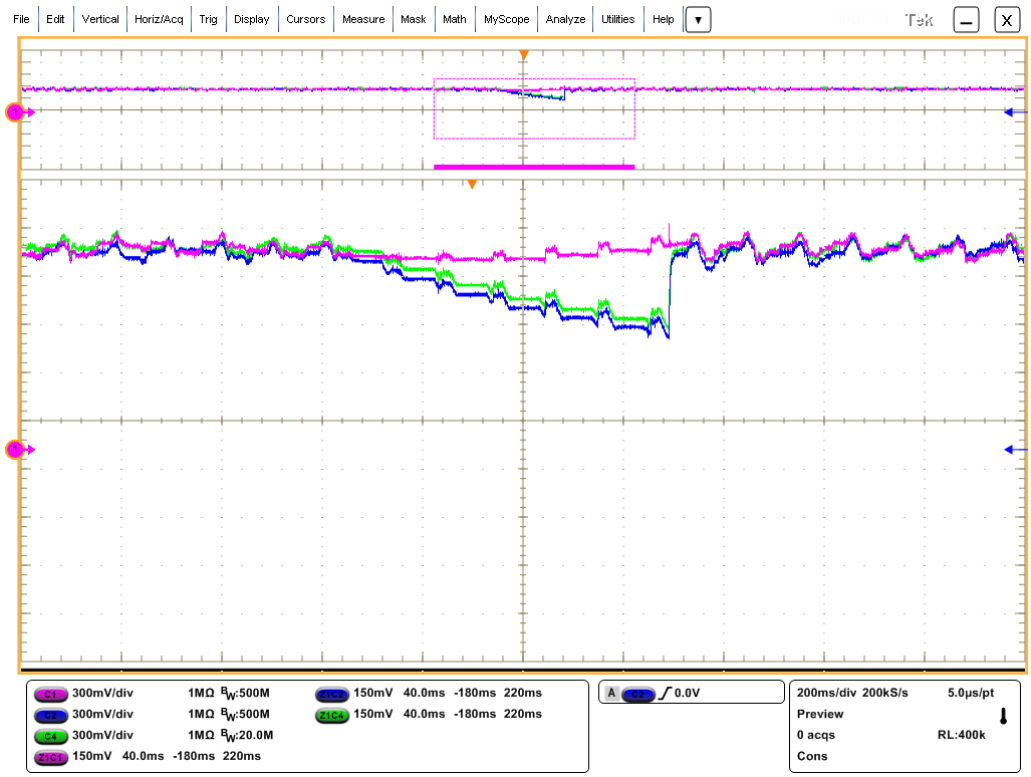
(a) output voltage (V_{out}) (5V/div)



(b) upper arm current (I_{up}) and lower arm current (I_{low}) sensor readings(400mv/div)



(c) Upper arm capacitor voltage (V_{c_up1}, V_{c_up2}, V_{c_up3}, V_{c_up4}) (300mv/div)



(d) lower arm capacitor voltages (V_{c_low1}, V_{c_low2}, V_{c_low3}, V_{c_low4}) (300mv/div).

Figure 41: Experimental results for the new voltage balancing control when disabled and enabled again after a short period.

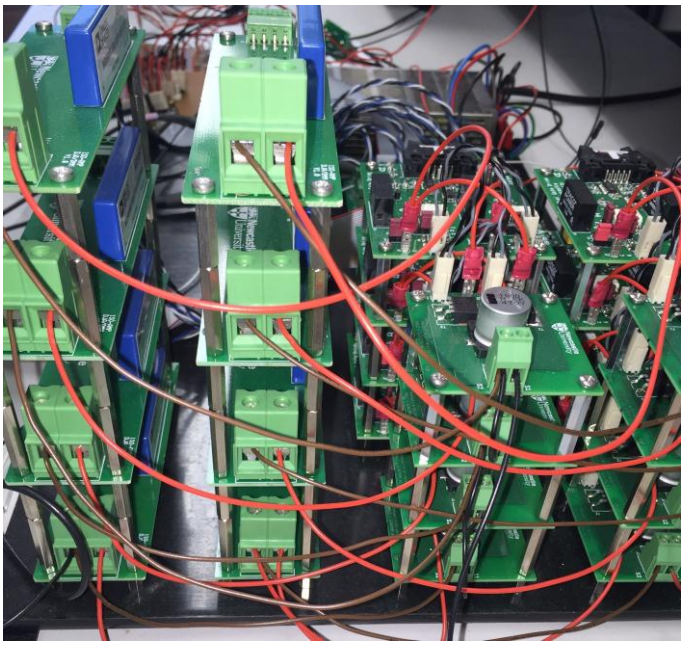


Figure 42. A photograph of the experimental test rig.

Figure 42 shows the experimental model of the one phase MMC scaled down at 50V. The control is depending on the FPGA evaluation board from TI, DE0-NANO.

4.7 Conclusion

This chapter presents the simulation and experimental results for the predictive voltage balancing control in the modular multilevel converter. The results have shown the successful control and reliability of the proposed approach compared to the conventional control. The new control approach provides dynamic voltage balancing control in different converter output conditions. Further experimental results have also shown the feasibility of the proposed approach by measuring the capacitor voltages. The key to the predictive voltage balancing control is to derive the charging and discharging state for next sampling period by taking into account the capacitor voltage differences between two samples. The new voltage balancing control does not require measurement of the arm currents but only the capacitor voltages compared to the conventional control, which means it does not require extra components beyond what is needed by the existing control systems. The scheme can be implemented using existing components within the MMC without any modification. Given the charging and discharging state by predicting the current direction, the new voltage balancing control can achieve the desired voltage distribution control similar to the conventional voltage balancing control.

Chapter 5

Circulating current control

5.1 Introduction

The modular multilevel converter has been one of the most attractive converters used in HVDC transmission systems for its simplicity in structure and the straightforward control topologies compared to other types of multilevel converters, such as diode-clamped multilevel converter and flying diode converter. Depending on the capacitor voltage in the converters, the voltage balancing control is required. For the latter two types of converters, the switching signals can have various patterns depending on the capacitor voltage, arm current, and the states of each power switches. For example, to turn on or turn off one particular submodule, there are several patterns of switching signals to achieve this. The selection of the control patterns are depending on the aforementioned converter parameters to achieve functions such as, increasing capacitor voltage, or reducing switching frequency. The complexity of selecting the particular control patterns can be significantly increased when the number of converter voltage levels is increased. However, the control approach of MMC can generate multiple voltage levels without increasing the control difficulty [167]. The fundamental control theories for the MMC include the balancing of the capacitor voltage distribution and the suppression of circulating current [146]-[172]. Because capacitors are used as power storage components and are connected in series, the current flowing through the submodules will cause the capacitor voltages to change. However, when increasing the number of the submodules in each phase, the voltage imbalance among submodules will become significant. This leads to problems such as increased component power ratings, circulating current flowing among each arm [170], and distortions on the output terminal voltage due to capacitor voltage variations [157]. Therefore, voltage balancing and circulating current suppressing controls are required during the normal operation for MMC. This keeps the voltage distribution among the submodules balanced and minimizes the circulating current.

The fundamental concept of different voltage balancing methods are similar, monitoring the capacitor voltages inside each submodule and turning on/off the corresponding submodule switches based on the arm currents passing through the submodules. Therefore, the capacitor voltages are controlled within a certain range to reach a balanced voltage distribution. There are other improved voltage balancing controls, such as reducing switching frequency [152],

predictive voltage balancing control [40] and voltage feedback loop control [146]. These controls can be adapted, cooperating with the circulating current control to further improve the system performance as they are independent of each other. The concept of the circulating current control is focusing on suppressing the AC circulating current, as stated in [170], the circulating current consists of two major parts, the double fundamental frequency alternating current and the DC current. In [169], the AC component of the circulating current was suppressed by decoupling the circulating current and forcing the AC components to be zero. This method requires an extra control loop to decouple the circulating current and generate the appropriate control signals. It was developed based on the assumption that the major AC component of the circulating current is the alternating current at twice the fundamental frequency. That assumption caused this control topology to be vulnerable to disturbances or faults which will generate additional circulating currents. In [173], the circulating current is suppressed when the DC component is used as a reference signal. The DC component is determined as shown in [154], and it is proven that the DC component is related to the power transmitted through the converter instead of the circulating current in the arms. In that case, this approach provides immunity to the disturbances or the faults caused additional circulating currents. In [172], the experimental results have demonstrated that the AC circulating current suppressing method can achieve the same system performance as the control used in [173], but it has a simpler control loop and suffers less from outside disturbances [174]. The modified circulating current suppressing control has advantages such as reliable AC circulating current components elimination without affecting the DC circulating current components. In addition the approach is feasible for implementation in a single-phase system without any modifications. A further simplified AC circulating current suppressing method is presented here, and the dynamic performances and output harmonics of this approach are investigated. A 1 MW two-end HVDC transmission system is used to verify the feasibility of this simplified CCSC method. The simulation and experimental results have shown that the proposed control can suppress most of the AC circulating currents, but the harmonics of the carrier frequency are observed as a consequence.

5.2 Modelling

A typical three-phase MMC is shown in Figure 43, which can be used in a two-ended transmission system which is described in the simulation results section. The submodule legs are connected in parallel with the DC power supply V_{dc} which produces a separate a dc volt-

age across the capacitor inside each submodule. In each arm, there are N submodules connected in series with a phase inductor which limits the circulating current as well as smoothing the rush current when the switching pattern on the upper and lower arms are changing. The selection of the arm inductors is based on the requirement of the maximum circulating current allowed and the maximum allowable rate of change of current when fault currents are flowing in the converter [175]. The inductance is required to be large enough to limit the circulating current existing in each phase as well as suppressing the fault currents whenever there is a failure to prevent the damage from overcurrent. On the other hand, a small inductance will give rise to a fast dynamic response and lower the losses on the converter. All of the submodules share this identical structure, which leads to ease of manufacture and controllability since the behaviors of each submodule are the same. The switches in each submodule have complementary gate signals. The output of the submodule is either V_c or zero, where V_c is the capacitor voltage inside the submodule. Because the voltage ripple across the submodule is related to the size of the capacitor, the selection of the capacitor can affect the system performance directly. In [176], it is demonstrated how the power capability and capacitor voltage ripple are affected by different capacitance values. Since the capacitors are used as energy storage components, like other types of multilevel converter, a voltage balancing method is required to control the voltage distribution. However, there are still voltage differences existing across each capacitor even with the voltage balancing control [177], which will cause circulating current flow from phase to phase or within one phase. Therefore to further refine the output waveform, circulating current control is also required.

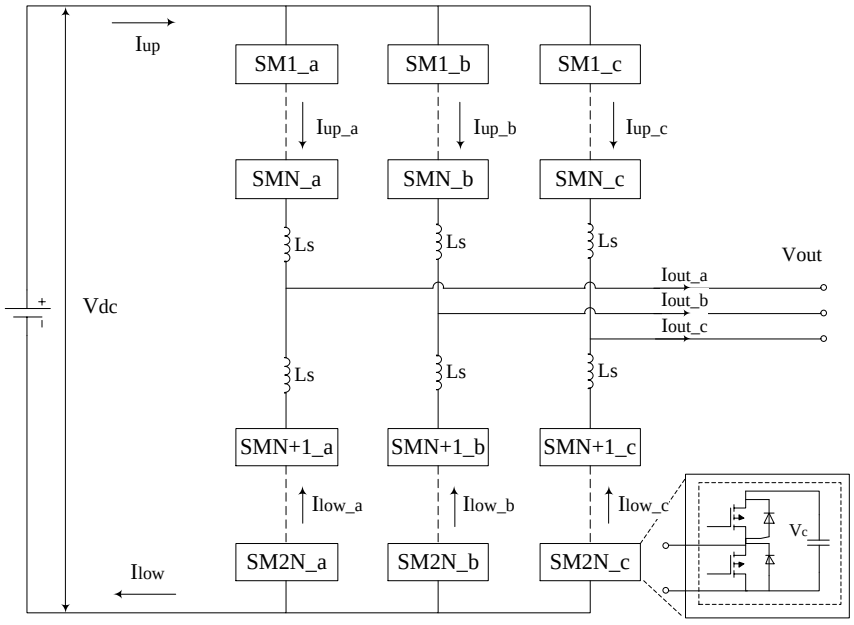


Figure 43: The three phase MMC model

5.2.1.Mathematical model

Because of the use of capacitors as power storage components, the series-connected sub-modules can be represented as inner voltage sources. The mathematical representations of the output voltage V_{out} are shown in (45) and (46).

$$V_{out} = \frac{1}{2}V_{dc} - V_{c\_up} - L_s \cdot \frac{dI_{up}}{dt} \quad (45)$$

$$V_{out} = -\frac{1}{2}V_{dc} + V_{c\_low} - L_s \cdot \frac{dI_{low}}{dt} \quad (46)$$

Combine (45) and (46),

$$V_{dc} = V_{c\_up} + V_{c\_low} - L_s \cdot \frac{d(I_{up} - I_{low})}{dt} \quad (47)$$

Based on the control theories of MMC, the desired upper inner voltage $V_{c\_up}^*$ and the lower inner voltage sources $V_{c\_low}^*$ can be expressed as (48) and (49):

$$V_{c\_up}^* = \frac{1}{2}V_{dc}(1 + MI\sin(\omega_0 t)) \quad (48)$$

$$V_{c\_low}^* = \frac{1}{2}V_{dc}(1 - MI\sin(\omega_0 t)) \quad (49)$$

Where MI is the modulation index, ω_0 is the angular velocity of the fundamental frequency. The upper and lower inner voltages are complementary regarding the DC voltage to reach minimum voltage differences as the DC voltage is distributed among a fixed number of the turned-on submodules. The upper and lower arm currents can be expressed in (50) and (51).On the other hand, because the DC bus current is flowing directly into the both upper and lower arms, DC current components must exist in the upper and lower arm current:

$$I_{up} = I_{dc} + \frac{1}{2}I_{out} \quad (50)$$

$$I_{low} = -I_{dc} + \frac{1}{2}I_{out} \quad (51)$$

According to (47) – (51), the equation can be rewritten as (52):

$$V_{dc} = V_{c\_up}^{*} + V_{c\_low}^{*} - L_s \cdot \frac{d(I_{diff})}{dt} + V_{diff} \quad (52)$$

Where V_{diff} is the voltage difference existing between the upper and lower arm voltage. The V_{diff} can be compensated by inserting the control signals into $V_{c\_up}^{*}$ and $V_{c\_low}^{*}$. Deduced from (7), V_{diff} is related to I_{diff} directly. It is feasible to obtain the control signal for V_{diff} by monitoring I_{diff}. According to the power balancing theory in [178], the instantaneous power of each arm of the MMC arm can be written as (53), (54):

$$P_{up} = V_{c\_up} I_{up} = \frac{1}{2} V_{dc} (1 + MI \sin(\omega_0 * t)) \left(I_{dc} + \frac{1}{2} I_{out} \right) \quad (53)$$

$$P_{low} = V_{c\_low} I_{low} = \frac{1}{2} V_{dc} (1 - MI \sin(\omega_0 * t)) \left(-I_{dc} + \frac{1}{2} I_{out} \right) \quad (54)$$

The energy is stored in the capacitor is proportional to the capacitor voltage and the energy stored in the capacitors can be expressed as (54). The capacitor voltage must have a DC voltage component and an AC voltage component at the fundamental frequency:

$$E = \int (P_{up} + P_{low}) d(t) = \int (\frac{1}{2} V_{dc} I_{out} + V_{dc} \cdot \mathrm{MI} \cdot I_{dc} \cdot \sin(\omega_0 t)) d(t) \quad (55)$$

Therefore, it is possible to regulate the circulating current by eliminating the ac components and keep the dc component. In [169]-[171], the circulating current control focuses on eliminating the double-fundamental frequency components. However, this control topology suffers from problems related to the AC side imbalance or grid fault because of the design of the control loop. In [172][173][179], the circulating current control is achieved by regulating the circulating current to its DC component, therefore suppressing the AC components. A moving average filter is adopted in [180] to eliminate the high-frequency distortions in the circulating current.

5.3 Proposed control for circulating current suppression

The fundamental concept is to remove the AC components in the circulating current. To achieve this, it is possible to regulate the circulating current to its DC components and suppress the AC component as much as possible according to (52). In [172], the repetitive control is

adopted to reduce the harmonics when suppressing the circulating current. In [173], several parallel PR controllers are used to reduce the AC components while regulating the DC components. [174] has proposed a simplified control topology to have a fast system response and low profile under unbalanced grid condition. The PR controller used in [172] can be replaced as shown in [173] considering the major component of the circulating current is a double-fundamental frequency current component, as expressed in (55). Above all, to finalize a stable system, the power flowing through both DC side and AC side must be equal to each other or with dynamic balance. According to [169]-[174], the alternating current components in both upper and lower arm are providing the AC side power output while the DC current components in both upper and lower arm are responsible for the DC side power flow. Based on the assumption that the system is in a steady state without any extra power stored in the converter, the DC component of the circulating current should be equal to the DC current in the transmission lines. The proposed controller is shown in Figure 44.

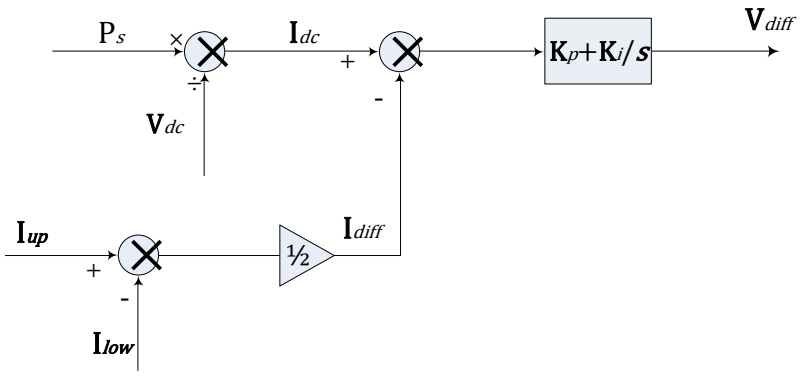


Figure 44: the feedforward controller for circulating current suppressing

Therefore, the desired inner upper and lower arm voltage can be written as (56), (57):

$$V_{c\_up}^{*} = \frac{1}{2}V_{dc}\left(1 + (MI\sin(\omega_0 t) + V_{diff}^{*})\right) = \frac{1}{2}V_{dc}\left(1 + MI\sin(\omega_0 t) + V_{diff}^{*}\right) \quad (56)$$

$$V_{c\_low}^{*} = \frac{1}{2}V_{dc}\left(1 - (MI\sin(\omega_0 t) + V_{diff}^{*})\right) = \frac{1}{2}V_{dc}\left(1 - MI\sin(\omega_0 t) - V_{diff}^{*}\right) \quad (57)$$

Where the V_{diff}^{*} is the voltage difference signal generated by the controller shown in Figure 44. The voltage differences among the capacitors inside the submodules can be suppressed by inserting the control signal as predicted in (52). The simulation results in the following section also indicate the successful circulating current control for this type of approach.

5.4 Simulation results

5.4.1.The simulation results for one-phase MMC scaled down model

The major control approaches are focusing on the voltage balancing and circulating current suppression control. Therefore, in most of the MMC based HVDC transmission systems, there are voltage balancing control and circulating current suppression control in operation at the same time. On one hand, the proposed voltage balancing control simplified the communication between the current sensor and the voltage sensor. On the other hand, the circulating current suppression control requires the both readings of the upper and lower arm currents. Therefore, the proposed voltage balancing method may or may not cause compatibility problems. In this case, the one phase model, as shown in Figure 45, was designed to illustrate the standard performance under simple operation conditions, then the two-end transmission model, shown in Figure 49, is designed to evaluate the performance of the selected control approaches when the active and reactive power control are involved.

The simulation section includes the following stages: 1. The single-phase MMC is designed and implemented with the proposed CCSC to verify the feasibility. 2. The proposed CCSC is implemented in the two-end HVDC transmissions system to evaluate the stability and dynamic performance during active/reactive power changes. The FFT analysis is given in both stages, showing that the major part of the circulating current has been suppressed.

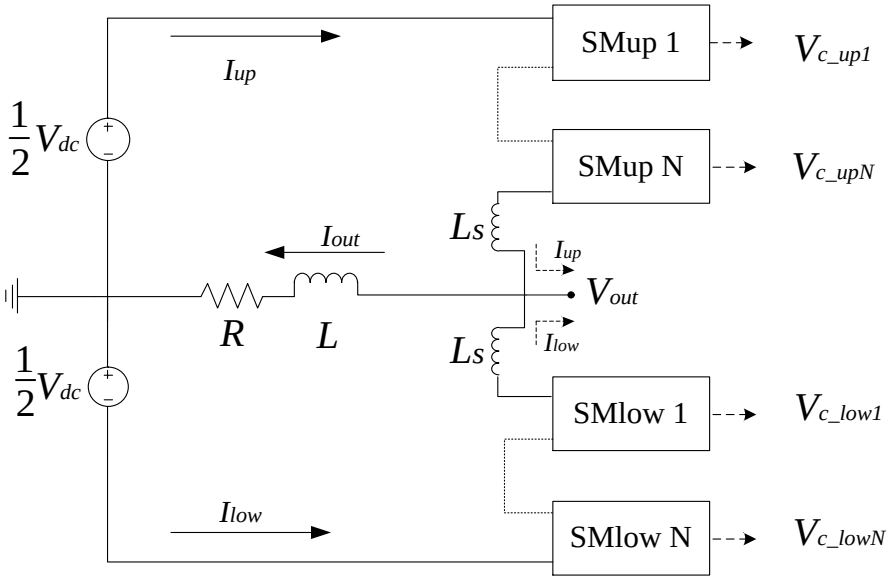


Figure 45: The single-phase scale-down model of the simulation for voltage balancing and circulating current suppressing.

Table 15: The parameters selected for the single-phase scaled down model.

Parameters	Values
MMC power rating, P (W)	100
DC-link voltage, V_{dc} (V)	+/-50
Load resistance, $R(\Omega)$	12.5
Load inductance, L(H)	0.001
Phase inductance, L_s(H)	0.001
Capacitance, C(F)	0.002
Submodule reference voltage, V_{sub}(v)	25
No. of submodules in each arm, N	4
Carrier frequency, f (kHz)	3

The single phase scale down model was designed based on the environment of the experiment test rig. Therefore, the dc voltage was scaled down to +/-50 V. The values of the inductor and capacitor were acquired in section 2.3.

The single-phase simulation results are shown in Figure 46. The CCSC is initially disabled and enabled again at 0.1s. The upper and lower arm currents in Figure 46 (a) have their peak values reduced from a maximum of 6A to 3.5A and from a minimum of -6A to -3.5A by 42%. The harmonics existing in upper and lower arm currents are also reduced significantly due to the circulating current suppressing effects of the CCSC after 0.1s. The smaller peak values of the arm currents can reduce the stresses on the devices as well as the power losses on the converter regarding the same power output. The output current shown in Figure 46 (b) has very little changes which verify that the AC components in the upper and lower arm currents are providing the power to AC side, and the DC component of the circulating current in the upper and lower arm currents are proving the DC side power. The capacitor voltages of the upper and lower arm have fewer harmonics after the CCSC is enabled, which reduces the isolation stress on the power switches since the voltage variations are slower than before. The output voltage is also shown in Figure 46 (d) along with the reference signal. Because the ripple component in the capacitor voltage has been reduced, the waveform is refined after applying the CCSC. Figure 46 (b) also shows the circulating current which indicates that, the peak value of the circulating current has reduced from 4A to 1A. Clearly most of the even order harmonic in the circulating current has been eliminated. The harmonics of the switching frequency is observed in Figure 47.

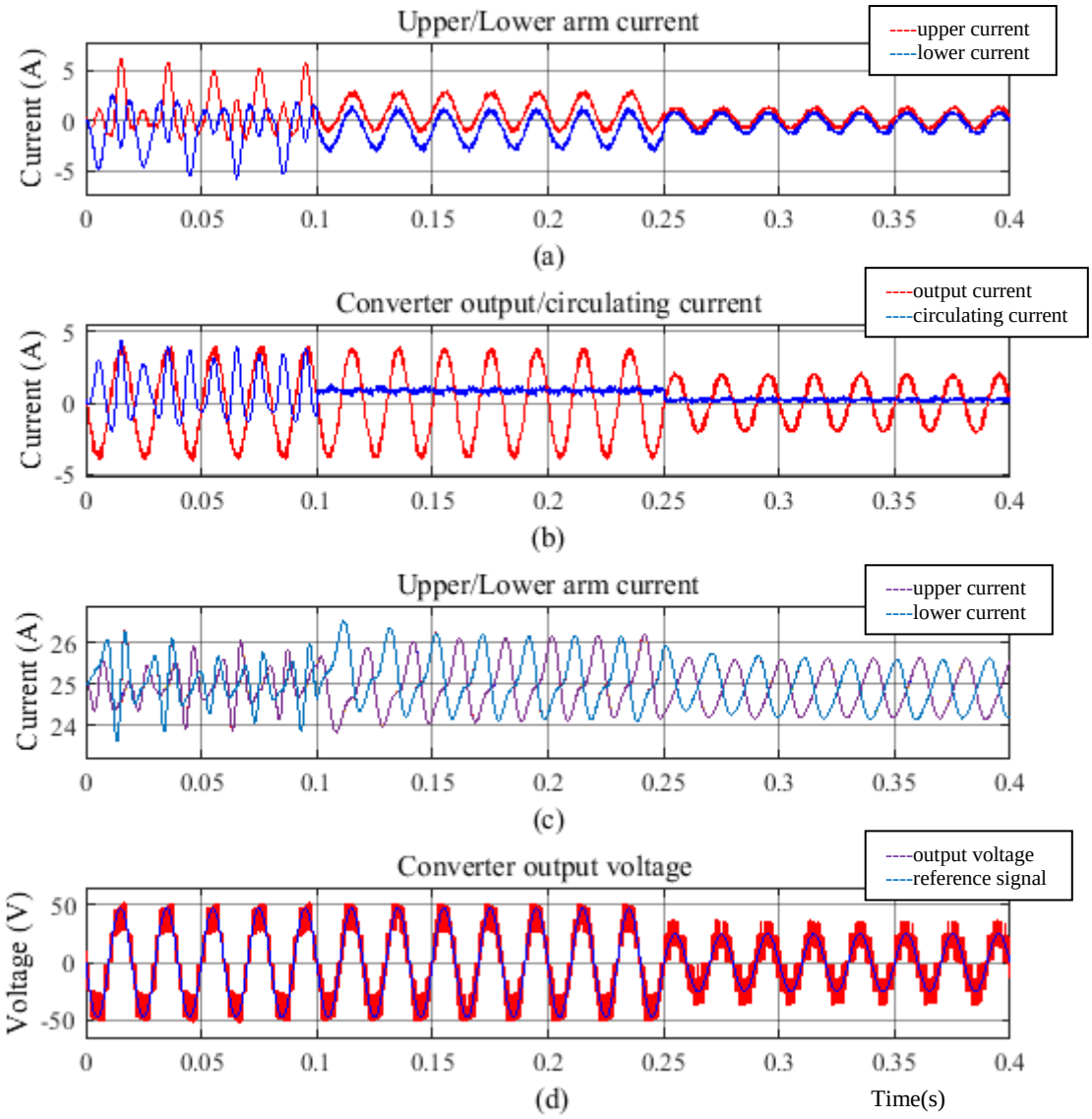


Figure 46 Simulation results for of the CCSC when it is activated at 0.1s and the modulation was changed from 0.95 to 0.5 at 0.25s, (a) the upper and lower arm currents, (b) converter output current and circulating current, (c) upper and lower arm current, (d) converter output voltage and reference signal.

The harmonic analysis is shown in Figure 47. Before the CCSC is enabled, the second order harmonic is observed as being as high as 250%, harmonics at the third and fourth order are also observed.

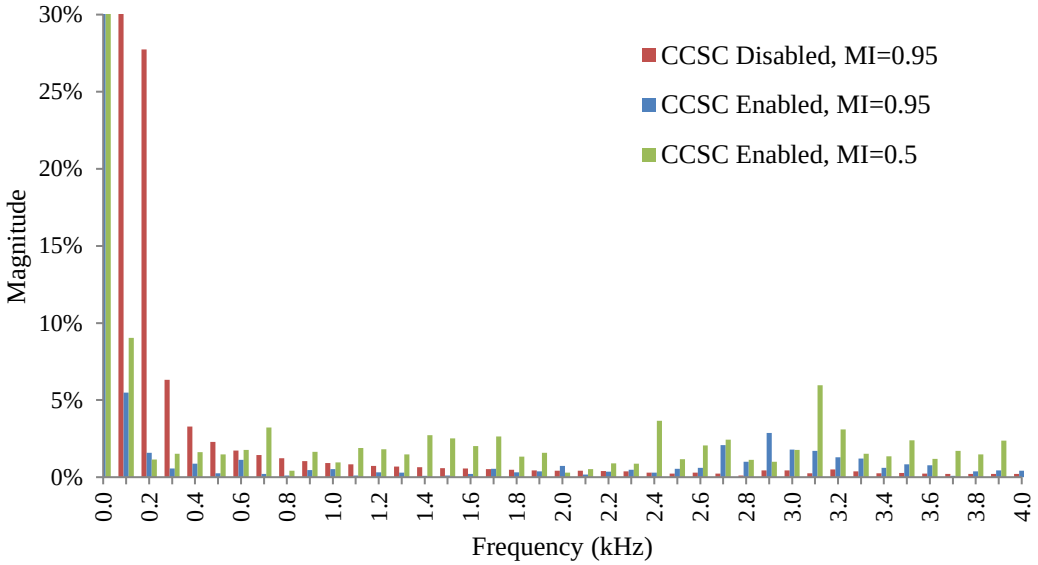


Figure 47 FFT analysis of the circulating current in 3 different stages (a) CCSC disabled, MI=0.95, (b) CCSC Enabled, MI=0.95, (c) CCSC Enabled, MI=0.5.

After enabling the CCSC, the harmonics at the second order have been suppressed and reduce to 10% when the MI=0.95, and increase as the MI is changed from 0.95 to 0.5. The change of MI results in the number of submodules being turned on and off. Thus the voltage differences among the capacitors are increased. Because the voltage differences are the primary reasons for the generation of circulating currents in each arm, the second order harmonics are increased as the MI changes. In both stages when CCSC is enabled, the existence of the harmonics around the carrier frequency is observed. It is also evident that the change of MI has effects on the harmonics at the carrier frequency.

It is believed that the circulating current will not affect the output current because it only flows between the arms of the MMC. However, due to the effects of the circulating current suppression, the current flowing into each submodule is also reduced as well. Therefore, the variation in the capacitor voltages is smaller compare to that seen without CCSC. The harmonics of the output voltages before and after applying the CCSC are shown in Figure 48. The most significant part of the harmonics appearing in the output voltage is around 3 kHz, which is the carrier frequency. The total harmonic distortion (THD) of the output voltage before applying the control is 28.11%, containing nearly 20% of the harmonics at the carrier frequency. The THD of the output voltage after applying the control is 24.90% which includes 17% of the harmonics at 1 kHz. The THD of the output voltage is reduced from 28.11% to 24.90% i.e. by 3.21%. However, it is still higher than the grid requirement in [181]. By in-

creasing the number of submodules in the MMC, the THD of the output voltage can be reduced to less than 2%.

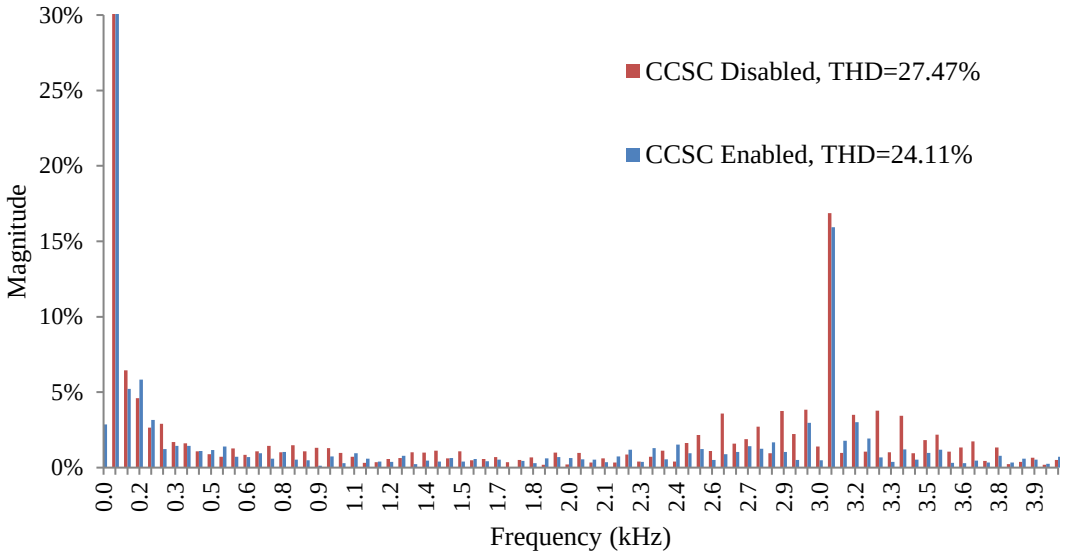


Figure 48 The output voltage analysis before/after the CCSC has been enabled.

5.4.2.The simulation results for two-end HVDC transmission system

A 1 MW transmission system is also designed and simulated to verify the implementation of the proposed CCSC performance in the three-phase system. Figure 49 shows the structure of the two-end transmission system. The rated power and the parameters used for the submodule capacitor and arm inductors in this transmission system are presented in Table 16. Further details of choosing suitable capacitors inside submodules and the arm inductors can be found in [175], [176] and [178].

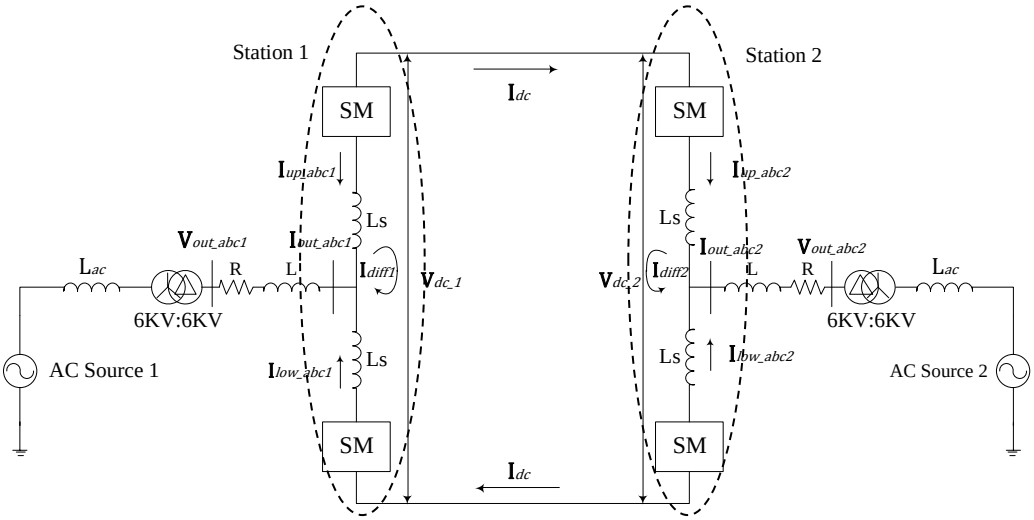
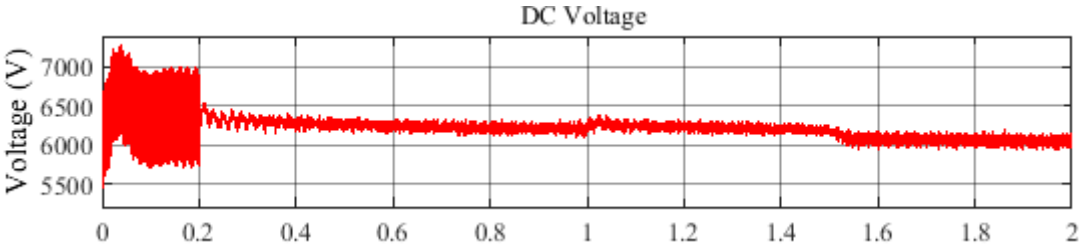


Figure 49. Two-terminal transmission system

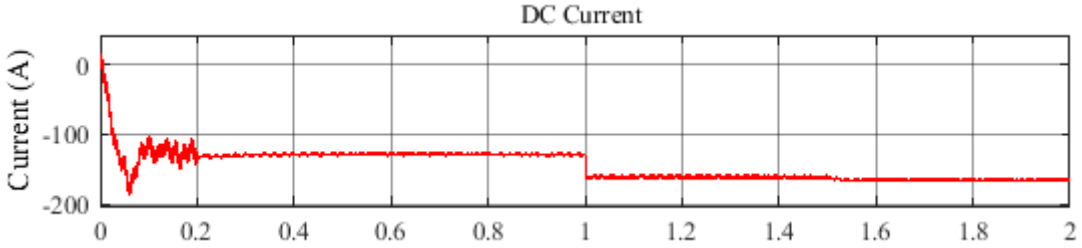
Table 16: Parameters Used For Experimental Model

Symbol	Parameters	Values
$\boldsymbol{P}$	Rated Active Power	3.33W
$\boldsymbol{V_{ac}}$	AC Voltage RMS	7.07V
$\boldsymbol{R}$	Load Resistance	15Ω
$\boldsymbol{L}$	Load Inductance	1mH
$\boldsymbol{C_{sub}}$	Capacitance of SM	1mF
$\boldsymbol{V_c}$	Capacitor voltage	5V
$\boldsymbol{L_s}$	Arm inductance	1mH
$\boldsymbol{N}$	NO. of Submodules	4
$\boldsymbol{V_{dc}}$	DC voltage	20V

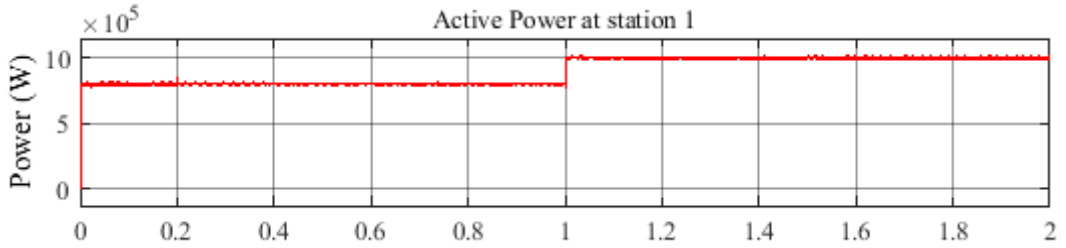
The simulation results are shown in Figure 50. The CCSC is initially disabled and reactivated at 0.2s. In Figure 50 (a), the DC side voltage is affected by the unsuppressed circulating current and the ripple voltage can be as high as 8.3% before 0.2s. The CCSC has successfully reduced the ripples from 8.3% down to 1.2% after 0.2s. In Figure 50 (b), the DC side current has fewer variations after applying the CCSC, the stable DC voltage and the DC current indicate that the power transmission is stable on the DC side of the converter. At 1s, the active power has increased from 0.8p.u to 1p.u (0.8MW to 1MW). The reactive power was changed from 0.2Mvar to 0.1Mvar at 1s. The increase in the active power leads to the increase in the DC voltage and DC current, and the decrease in the reactive power leads to the decrease in the DC voltage and DC current because of the power transmitted through the converter is balanced. In Figure 50 (e), the upper and lower arm capacitor voltages are maintained at the nominal voltage of 1kV with 2.5% ripple. The 2.5% ripple on the capacitor voltage will lead to maximum of 2.5% transmission voltage variations, while it is required to be less than 10% in [181]. The active power has changed from 0.8p.u to 1.0p.u at 1s. The capacitor voltage ripple has increased by 1% due to the increased active power flow. The significant changes of the circulating current can be observed in Figure 50 (f), where the circulating currents flowing in three phases are suppressed, and the major parts of the circulating current have been eliminated.


DC Voltage
Voltage (V)
7000
6500
6000
5500
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

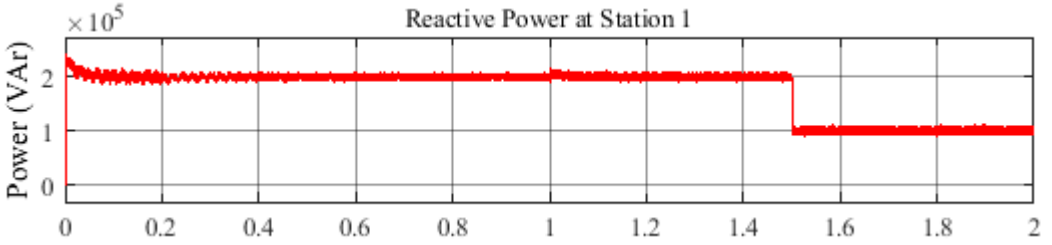
(a)


DC Current
Current (A)
0
-100
-200
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

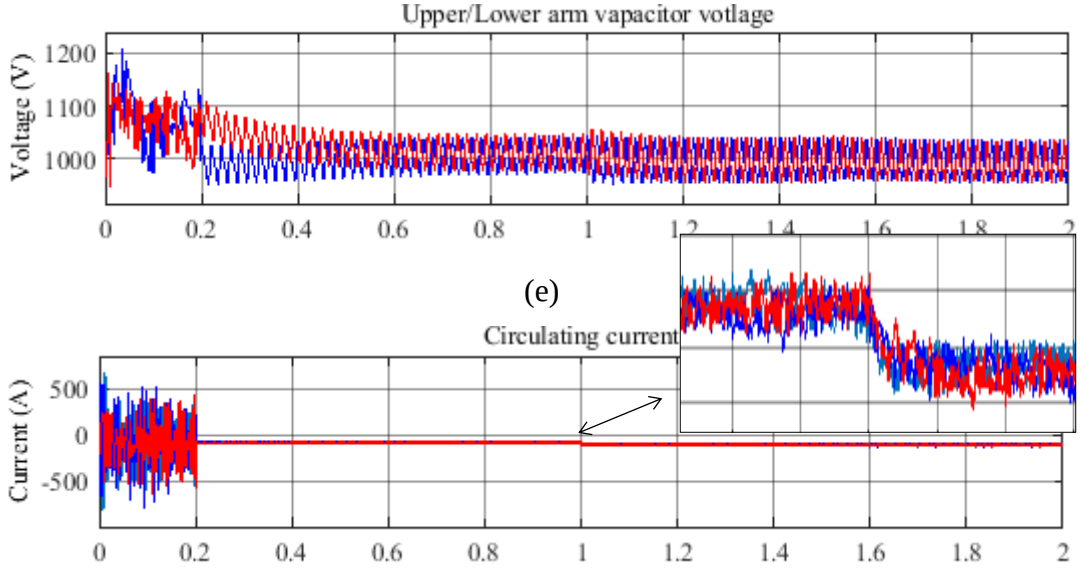
(b)


Active Power at station 1
×10^5
Power (W)
10
5
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

(c)

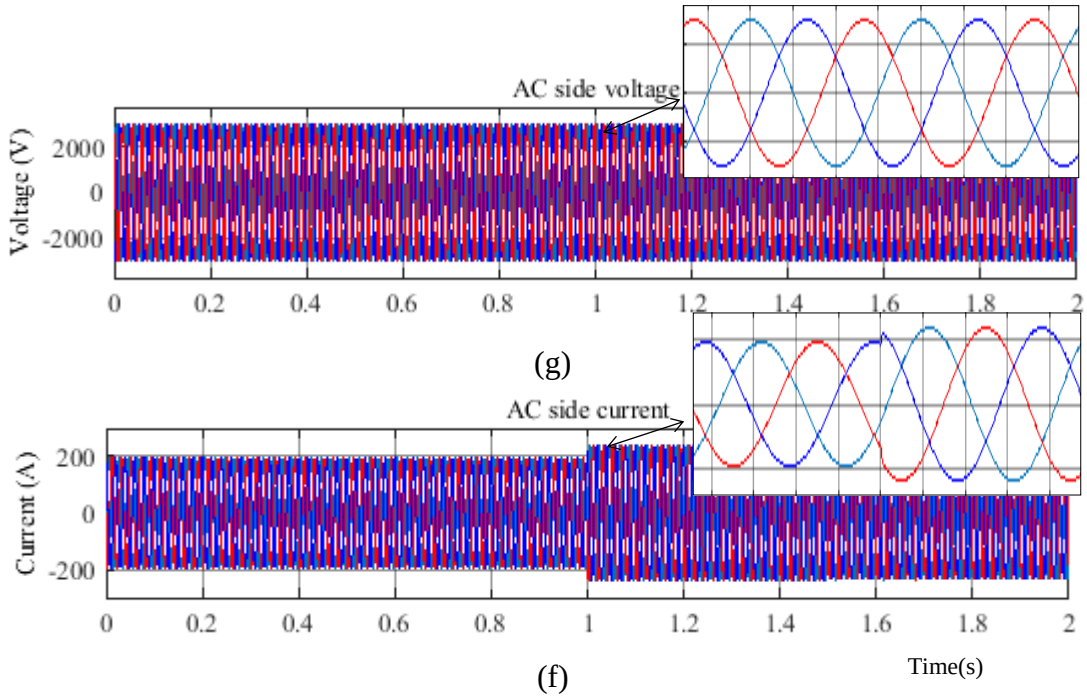

Reactive Power at Station 1
×10^5
Power (VAr)
2
1
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

(d)


Upper/Lower arm vapacitor votlage
Voltage (V)
1200
1100
1000
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Circulating current
Current (A)
500
0
-500
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

(e)

(f)



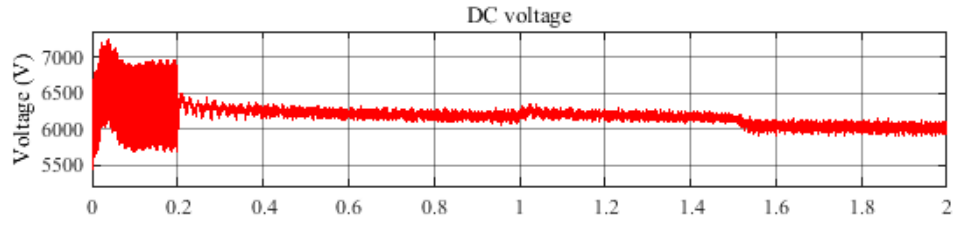
(g)

(f)

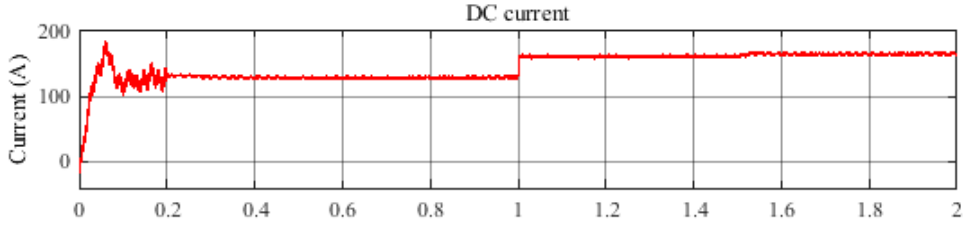
Figure 50 simulation results for station one (a) DC voltage (b) Direct current (c) active power (d) reactive power (e) upper/lower arm voltages (f) circulating current (g) AC side voltage (h) AC side current.

The simulation results for station two are shown in Figure 51. The DC voltage appears to be the same as the DC voltage of station one based on the assumption that the power losses in the transmission lines are small. The changes of the DC voltage and DC current occurred when the active power and the reactive power were changed at 1s and 1.5s.

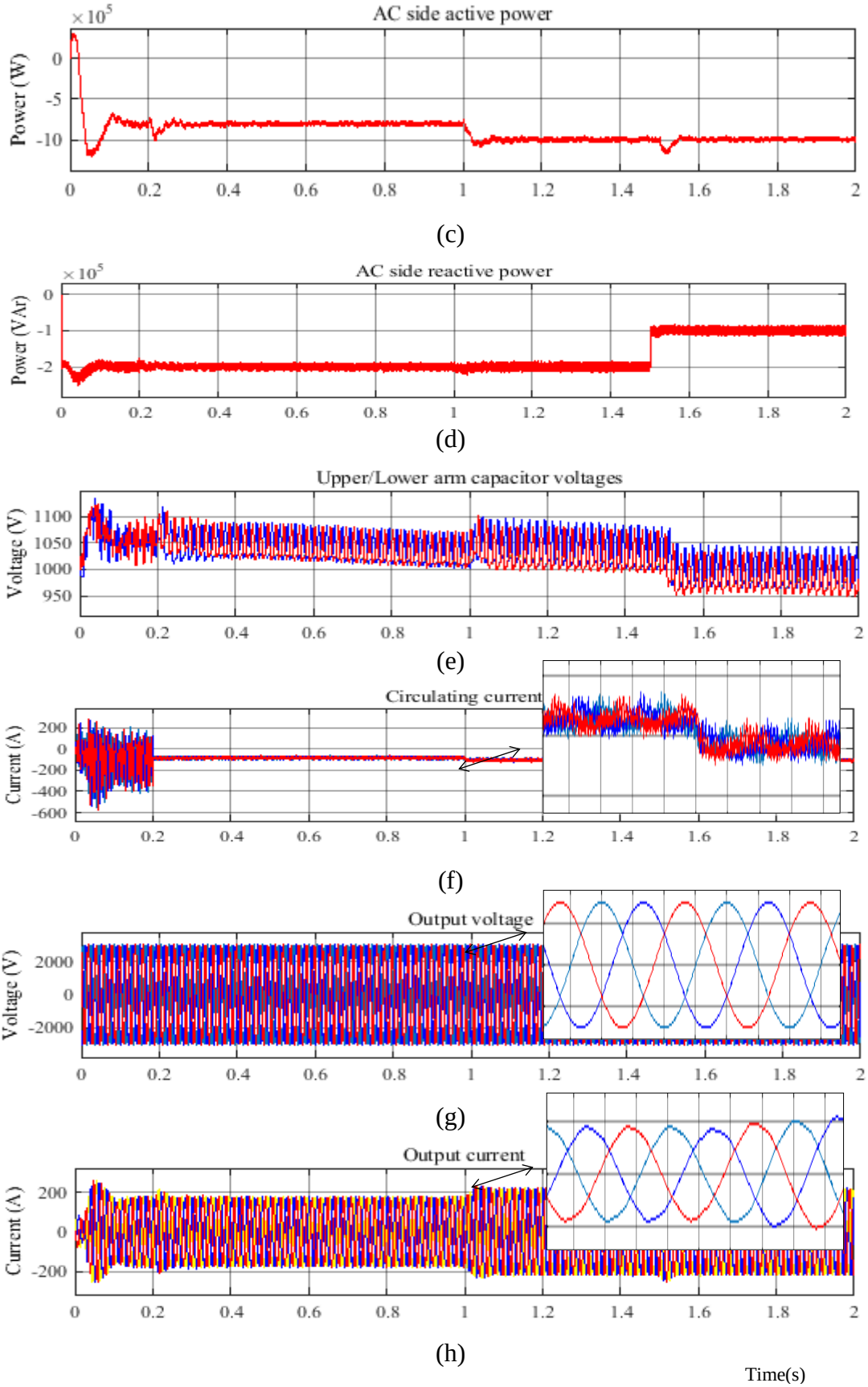
In Figure 51 (c), the active power is following the preset value provided in station one. It takes maximum 0.06s (3 operation cycles) to reach the steady state. The upper and lower arm capacitor voltages of station two are shown in Figure 51 (e), with the proposed voltage balancing control, the voltage ripples are controlled within +/-2.5%. The second order harmonics of the circulating current shown in Figure 51 (f) are controlled and the harmonics of the twice fundamental frequency have being reduced from 250% to 5% as illustrated in Figure 53.



(a)



(b)



(c)

(d)

(e)

(f)

(g)

(h)

Figure 51 Simulation results for station two (a) DC voltage (b) DC current (c) active power (d) reactive power (e) upper/lower arm voltages (f) circulating current (g) AC side voltage (h) AC side current.

In Figure 52, the harmonics profile before/after the control show that after applying the CCSC, the double-frequency components have been suppressed. The second order harmonic is observed, which can go as high as 260% of the fundamental DC voltage. After the control is applied, most of the second harmonics are eliminated and only a few of second order harmonics are observed in Figure 52. In addition to the elimination of the second order harmonics, harmonics around the switching frequency are also shown in the results, which indicate the CCSC can generate a small amount of harmonic at the switching frequency.

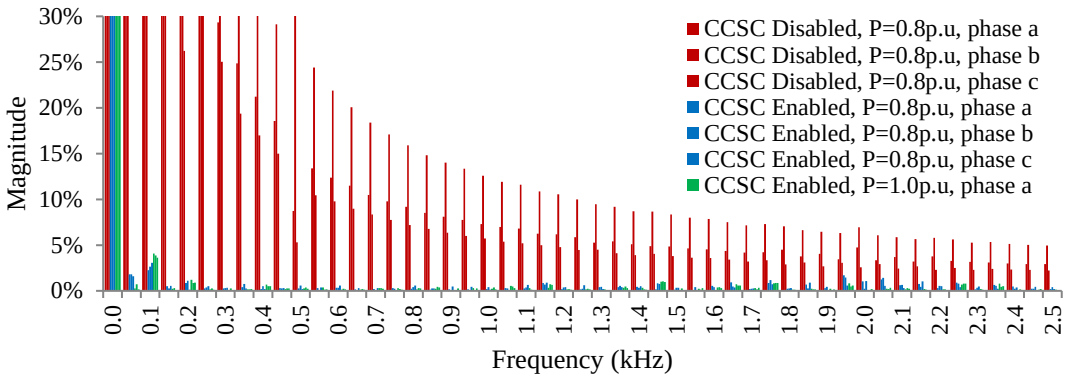


Figure 52 FFT analysis of the circulating current in station one (a) before applying the CCSC (b) after applying the CCSC with P=0.8MW (c) after applying CCSC with P=1MW.

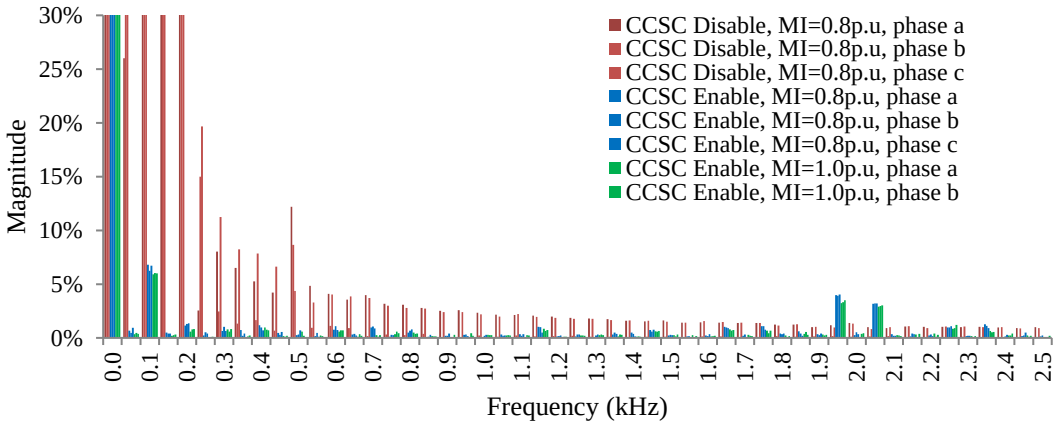


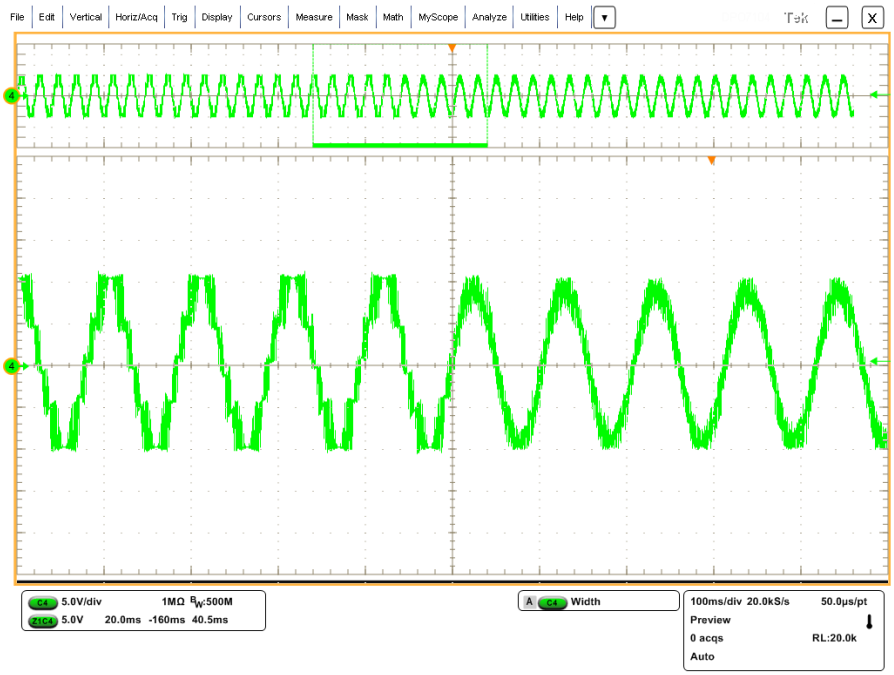
Figure 53 FFT analysis for the circulating current in station two (a) before applying the CCSC (b) after applying the CCSC with P=0.8MW (c) after applying CCSC with P=1MW.

The harmonic analysis presented in Figure 53 further indicate that the proposed CCSC can suppress the harmonics at twice the fundamental frequency, but it also generates around 4% harmonic at the carrier frequency. Overall, the simulation results have shown the strong con-

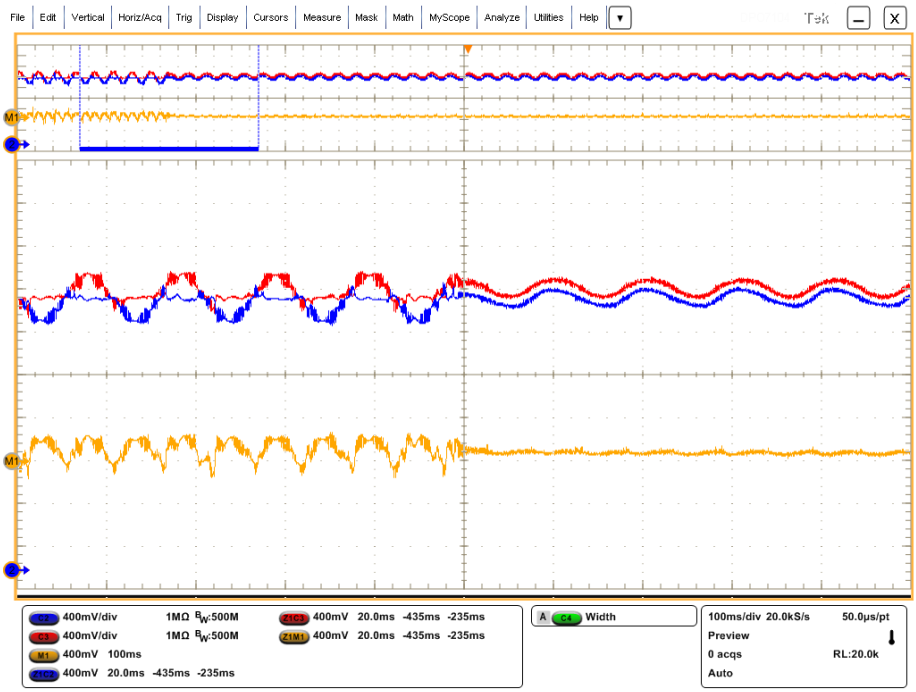
trol of the two-terminal transmission system and the impact of the CCSC to the overall system. The suppressed circulating currents not only reduce the stress on the switching units but also improve the controllability and the observability by reducing the unnecessary harmonics in the phase currents, therefore, improving the dynamic performance of the system.

5.5 Experiment results

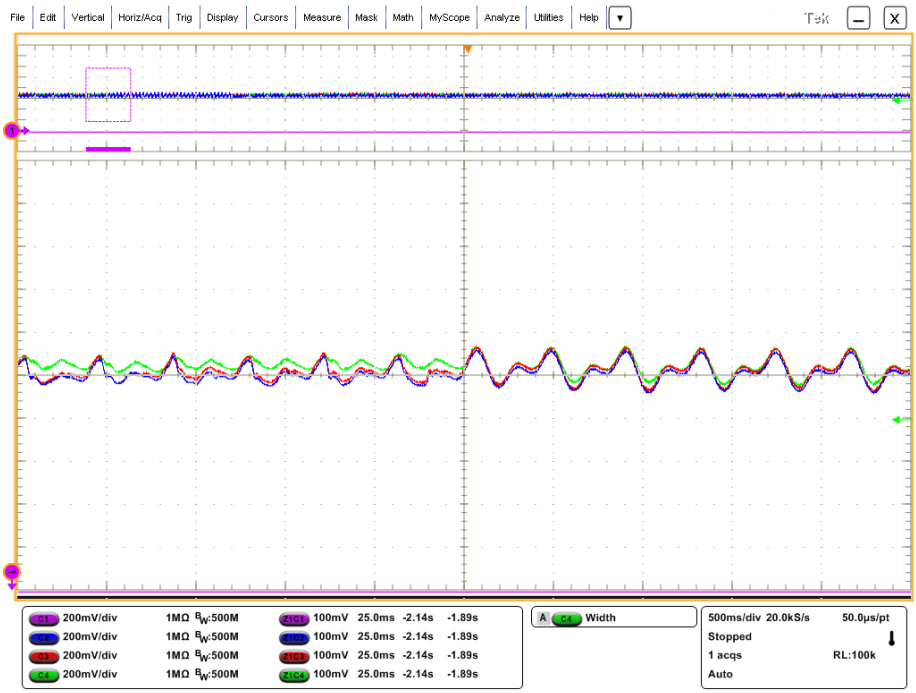
The proposed CCSC has been tested experimentally by implementing a scaled-down model. The experimental results also show the effects of the suppression control of the circulating current in a single-phase model. Figure 38 shows the system setups of the experiment design. The central control unit is the DE0-NANO FPGA using EE4CE22F17C6N chip from Altera. It reads the sensor signals from AD215AY isolation amplifier which are connected in parallel with the MMC to monitor the capacitor voltages. The gate signals are generated inside the FPGA and propagated to the MMC via gate drive circuits. The upper and lower arm currents and the circulating currents before and after applying the CCSC are shown in Figure 54. The AC components in the circulating current are suppressed after the control is enabled. The major part of the AC circulating current is eliminated by the control, the DC component in the circulating current remains. The FFT analysis in Figure 57 also shows that the harmonics present in the circulating current at twice the fundamental frequency has been suppressed. The upper and lower arm currents are shown in Figure 54 (b). Before applying the CCSC, the upper arm current consists of the positive half of the output current while the lower arm current forms the negative half of the output current as in (6) and (7).



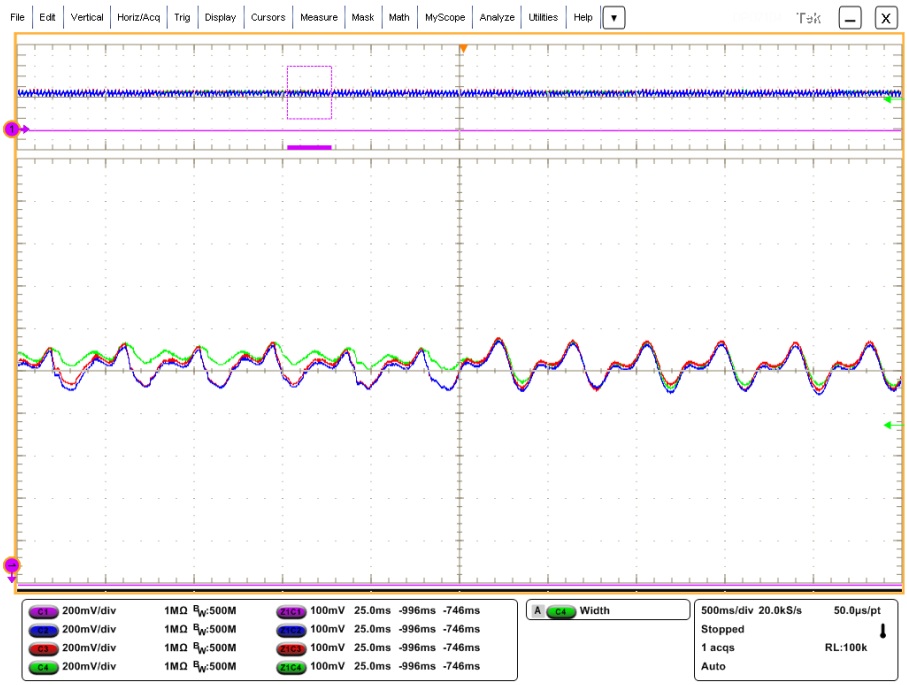
(a) output voltage



(b) upper/lower arm currents and the circulating current



(c) upper arm capacitor voltages



(d) lower arm capacitor voltages

Figure 54 The experiment results of the single phase MMC model, the CCSC is initially disabled and enabled again later.

After applying CCSC, both upper and lower arm currents have been changed from two halves into two complete sinusoidal waveforms. The peak values of both upper and lower arm currents are lower compared to the peak values before applying the CCSC because of the eliminations of the AC components in the circulating current, and the variations of the upper and lower arm currents are also slower, therefore, reducing the stresses of the switching components and lowering the harmonics generated in the converter output voltage.

The harmonic analysis of the output voltage is shown in Figure 55. The major parts of the THD exist at the carrier frequency, which is at 3 kHz. The THD of the output voltage before applying the CCSC is 27.47%, and it is reduced down to 24.11% i.e. 3.36% when the circulating current is suppressed. Compared with the simulation results shown in Figure 48, they both reduce the THD of the output voltage due to the suppressed circulating current. By eliminating the AC components in the circulating currents, the unnecessary currents flowing into the capacitor inside each submodule is reduced as well. Therefore, the voltage patterns are smoother as shown in Figure 46, Figure 50, Figure 51, Figure 54 and Figure 56, leading to the THD reduction of the output voltage.

The upper arm capacitor voltages are also shown in Figure 54 (c), the voltage differences among those capacitors can be observed before applying the CCSC. One of the reasons caus-

ing circulating current is the voltage differences among each arm. By the time the AC components of the circulating current have been eliminated, the voltage differences among the capacitors are actively reduced. The increment of the peak values is observed as well in the simulation results in Figure 47. According to (53) and (54), the V_{diff}^{*} term inserted into the reference signals is causing the changes of the inner voltages of the upper and lower arms. By increasing the proportional gain of the feedback controller shown in Figure 46, the upper and lower arm capacitor voltages gains are observed.

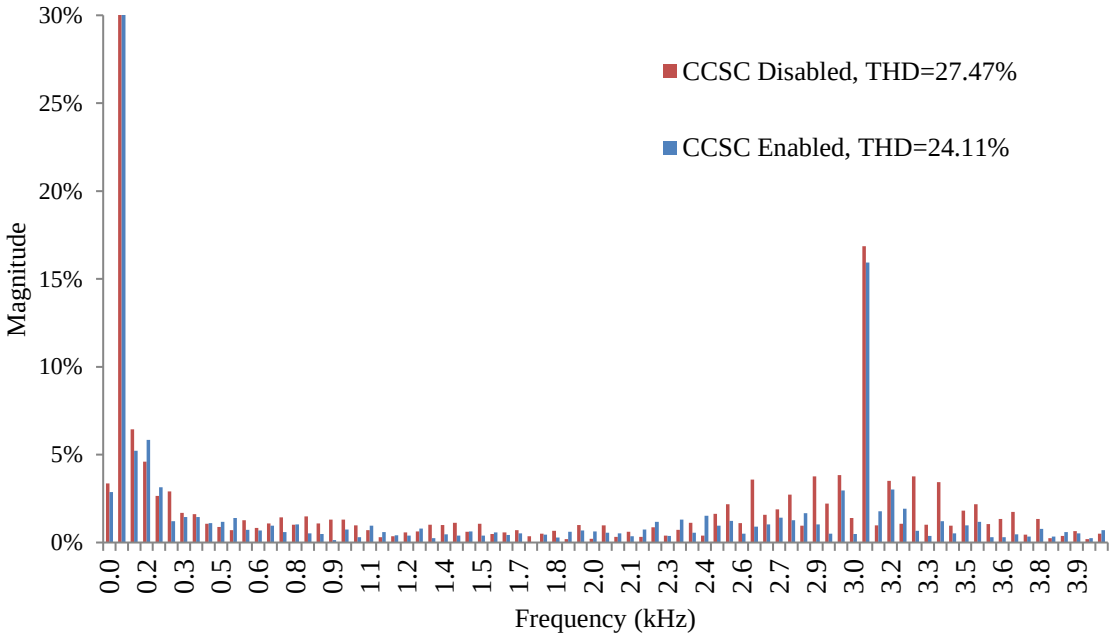
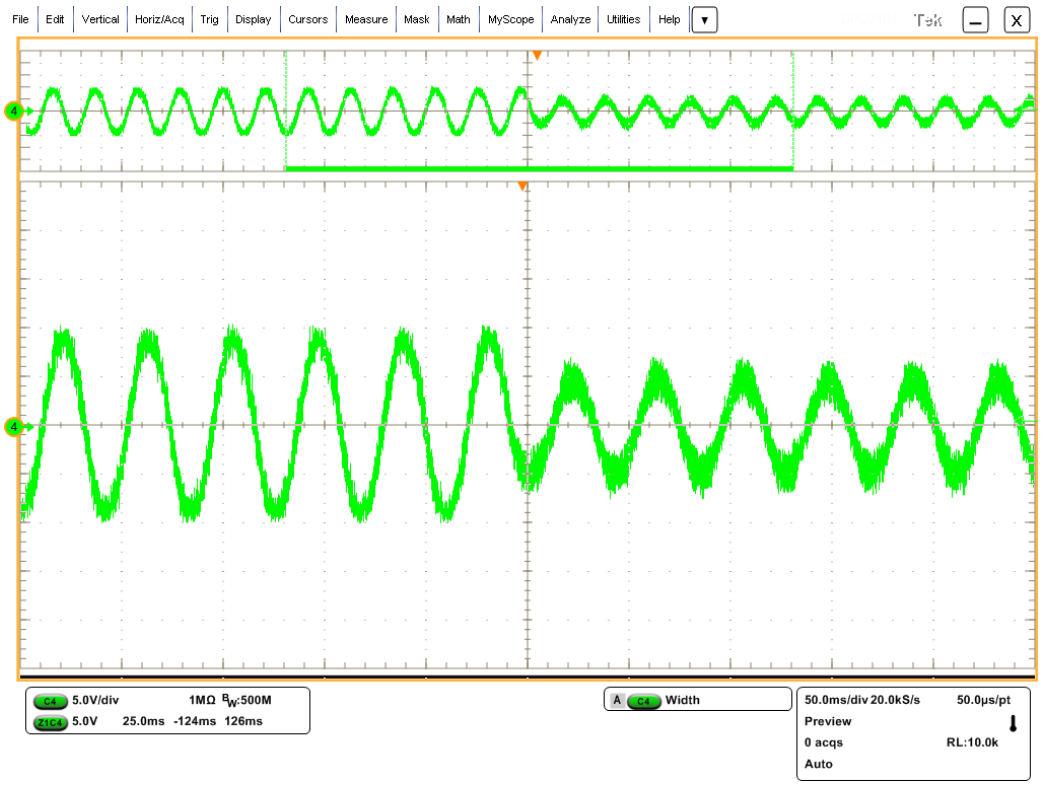


Figure 55 The FFT analysis of the output voltage before/after the CCSC has been enabled.

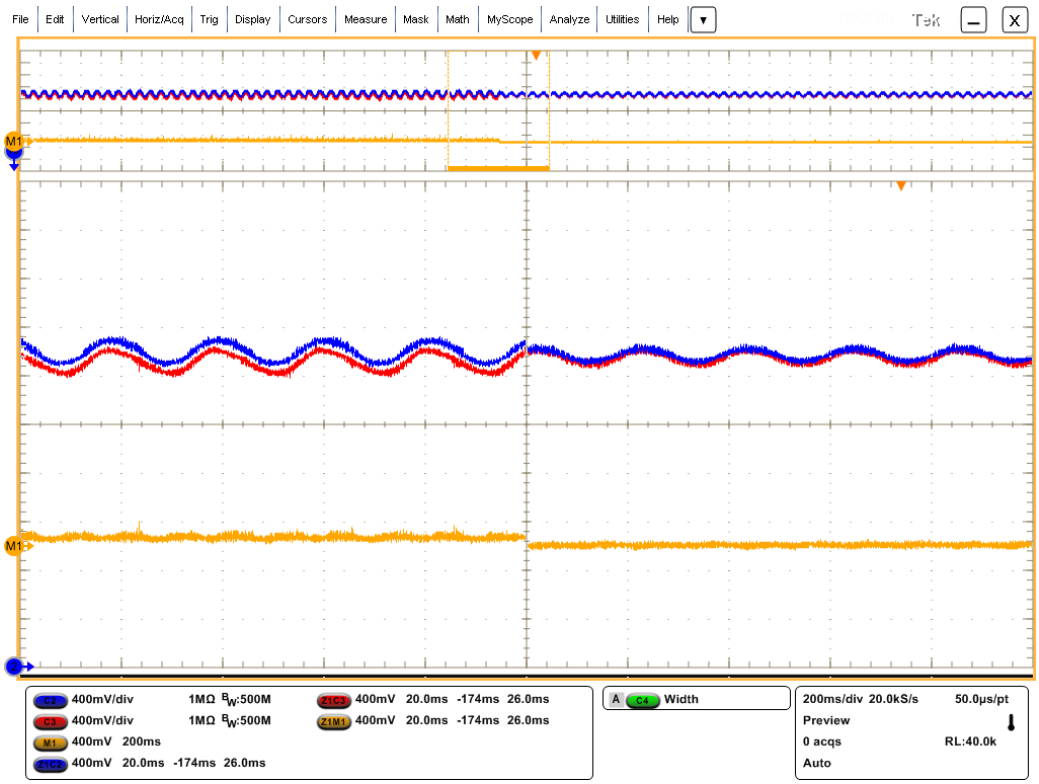
The modulation index was changed from 0.95 to 0.5 in Figure 56. The changes of the modulation index leads to the decrease of the output voltage, which results in the output power decreasing when connected to passive loads. According to (55) the power transmitted is balanced between the AC side and the DC side, the power dropping on the AC side leads to the current decreasing on the DC side, and when the DC voltage remains the same. As a result, the amplitudes of the upper and lower arm currents are also lower when the modulation index was reduced. Additionally the circulating current is lower as the transmitted power is reduced.

The output voltage, shown in Figure 56 (a) has reduced peak values since the modulation index has changed from 0.95 to 0.5. The voltage differences among the upper/lower arm capacitors shown in Figure 56 (c) and (d) are similar when modulation index changes. The peak values of the upper and lower arm capacitor voltages are lower, which is indicating the reduced power output. The variations of the capacitor voltage are also reduced because of the

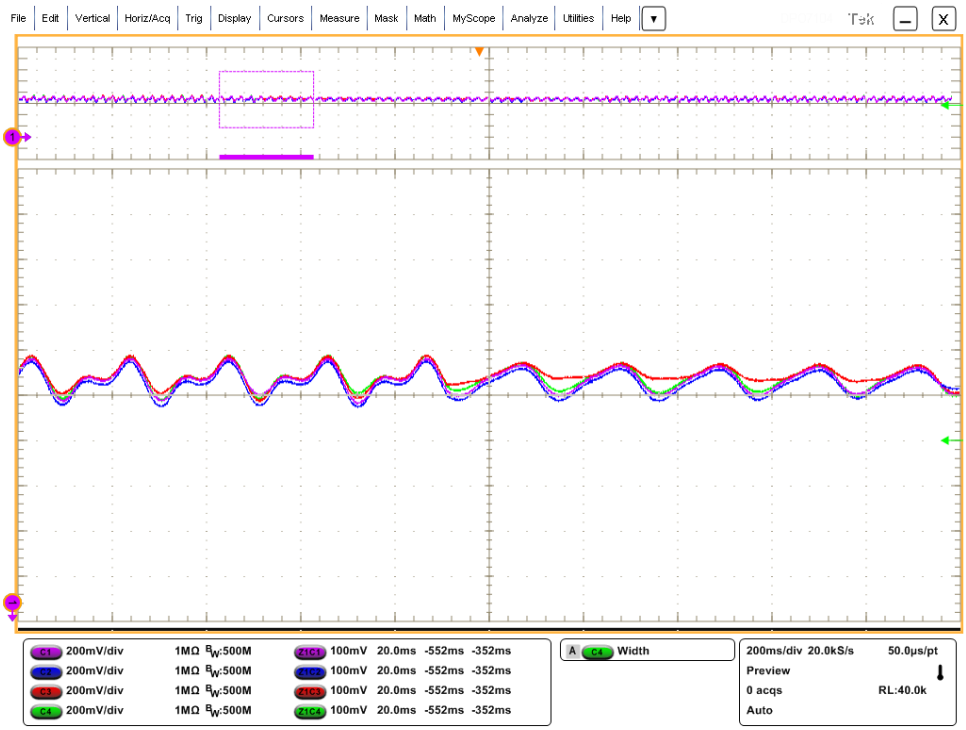
smaller currents flowing into each submodule, which also results in the smoothing of the capacitor voltages. The upper and lower arm currents are also lower when the modulation index changed. As stated in (53) and (54), the energy stored in the submodules is provided by the DC component of the circulating current. The lower reference signal leads to the reduced power output. Therefore, the suppressed circulating current shown in Figure 56 (b) has a lower value after the change. As expected, the harmonic analysis shown in Figure 57 indicates that the proposed CCSC can eliminate the second order harmonics, but will generate a small harmonic component around the carrier frequency. It is observed that, when the modulation index is at 0.5, the harmonics at the 3.3 kHz carrier frequency, is as high as 6.5%. However, the second order harmonics have been suppressed when the CCSC is activated in the experiment. The initial value of the second order harmonics was as high as 96%. After the control has been activated, it fell to 13.1% and 7.8% in regard to 0.95 MI and 0.5 MI respectively.



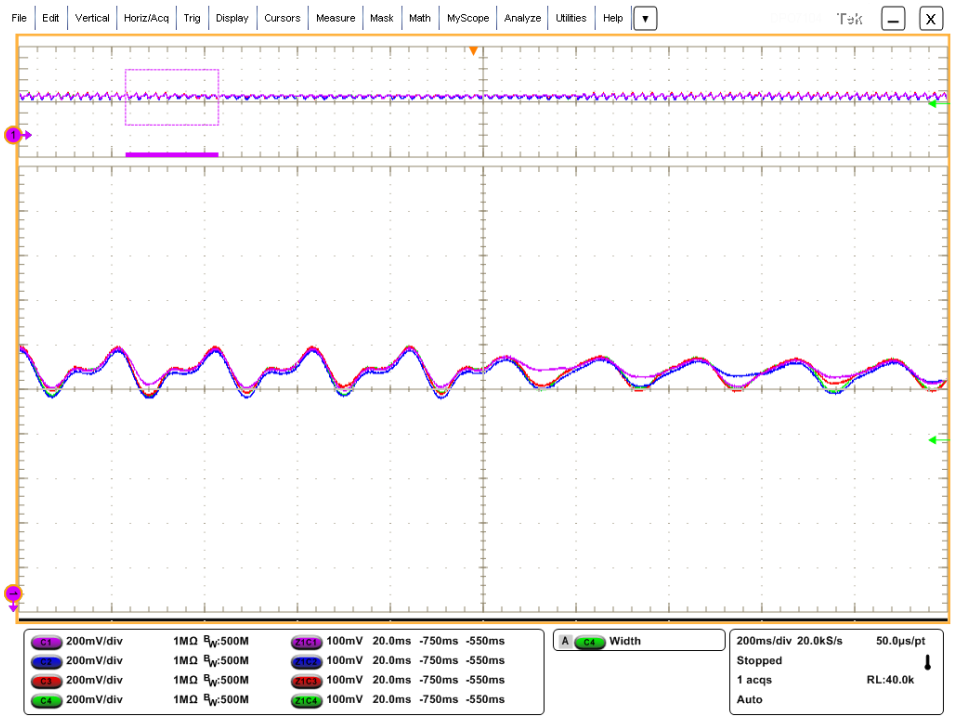
(a) output voltage



(b) upper/lower arm currents and the circulating current



(c) upper arm capacitor voltages



(d) lower arm capacitor voltages

Figure 56 The experiment results of the single-phase MMC model where the MI is initially set at 0.95 and later was changed to 0.5.

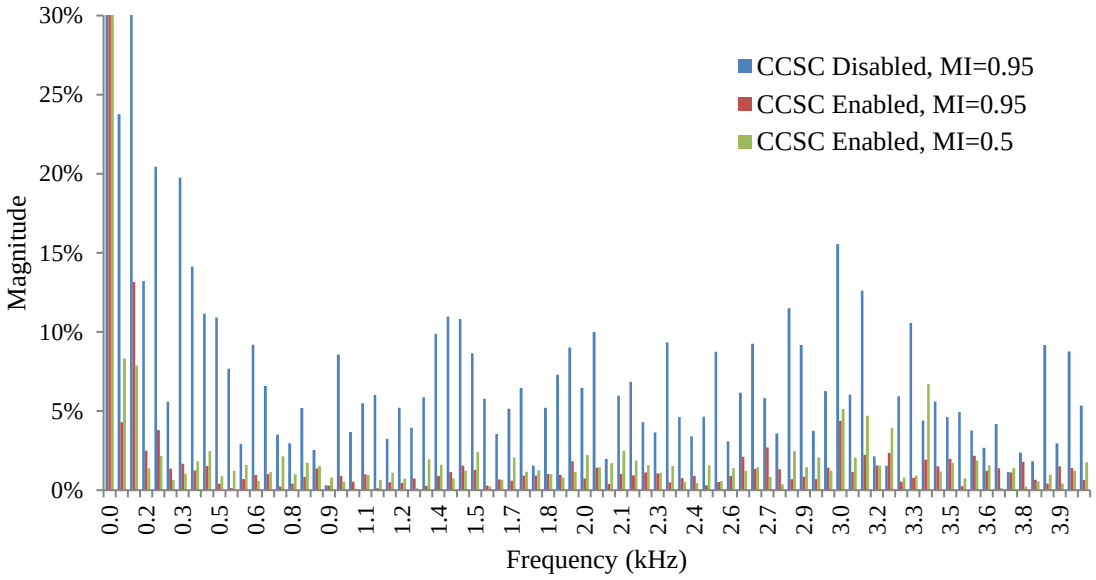


Figure 57 the FFT analysis of the circulating current (a) before the CCSC has applied (b) after the CCSC has applied and MI= 1 (c) after the CCSC has applied and MI=0.5

5.6 Conclusion

The simplified CCSC method has been proposed and experimentally tested. The simulation

and experimental results have shown the feasibility and the controllability of this approach. This CCSC is based on power balancing through the DC and AC sides of the converter. The scheme removes the need for the PR controller tuning at a higher frequency than the fundamental frequency to get a fast system response. The reference signals for circulating current control were deduced from the power transmitted through the converter. Therefore, it would easily adapt to the existing control system without adding more components. The FFT analysis indicates that the proposed CCSC can suppress the second-order harmonics of the circulating current. The AC components at twice the fundamental frequency have been eliminated, but the harmonics of the carrier frequency are observed due to the control effects. Further improved CCSC control or the use of a feedback loop can be designed to reduce the second order harmonics without generating the carrier frequency harmonics.

Chapter 6

The experiment test rig design

6.1 Introduction

The experiment test rig was designed and built to verify the proposed voltage balancing control and the circulating current suppression control. The experimental results presented in the previous chapters have demonstrated a good agreement with the simulation results and the capabilities of the proposed approaches. However, the selection of the control unit and the relevant components can affect the performance of the overall system in every aspect.

6.2 System units

Based on the simulation results, there are two basic control approaches are considered when designed the system. The voltage balancing control and the circulating current suppressing control. The voltage balancing control requires the voltage measurement of each capacitor, hence generating the corresponding gate signals. Therefore, the voltage monitoring is required. Regarding the circulating current suppressing control, both upper and lower arm currents are recoded to generate the control signals to suppress the circulating current. Therefore, the monitoring of both upper and lower arm currents is necessary. Furthermore, because the voltage ratings of the gate drive and the MMC circuit are different, hence the voltage regulation circuit is essential. The level-shifter is designed to boost the voltages of the control signals. The system was designed as shown in Figure 58. The whole circuit consists of six parts: 1. The FPGA board which is used to receive the voltage and current signals in order to generate the control signals for each submodule. 2. The level shifter which is used to boosted the voltage of the signals since the voltage of the FPGA is limited to its supply voltage which is lower than the switching on voltage requirement of the gate-drive. 3. The dual-gate drive board which is used to transform the gate signals into the switching signals according to the voltage level of the submodules. 4. The main MMC circuit which consists of eight submodules connected in series.5. The voltage sensor circuit which are connected in parallel with the MMC circuit in order to monitor the changes of the capacitor voltages. 6. The current sensors which are connected in series with the MMC circuit in order to take readings of both upper and lower arm current, then transmitting them to the FPGA control unit. All circuits are connected to the on-board power supply, which are 5V and 15V respectively.

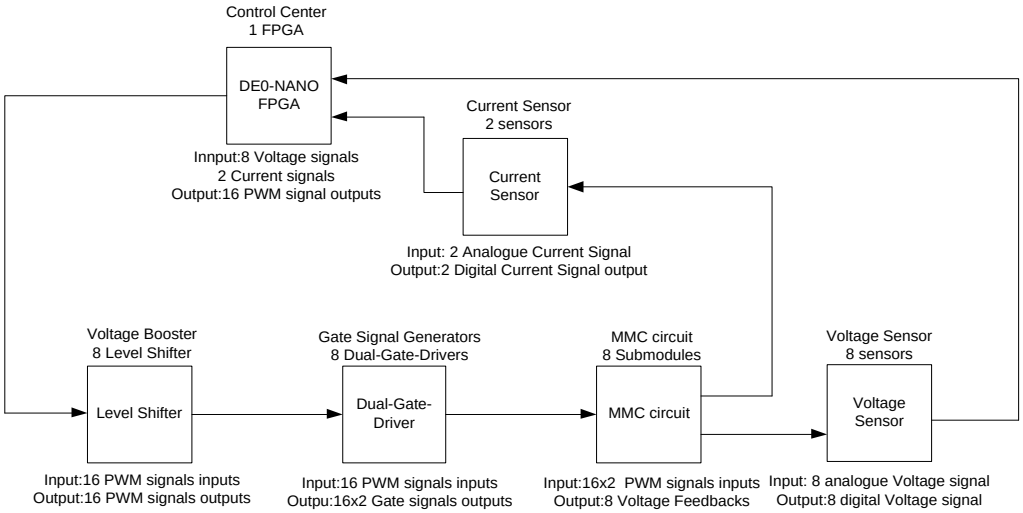


Figure 58: Block diagram of the experiment test rig.

6.2.1.Control unit

(a)*FPGA vs DSP*

The control unit is one of the core components for controlling the power circuit. Depending on the application, the control unit has two branches as demonstrated in [183]. In general, the FPGA is more capable of the processing of the data when there are time constraints due to its number of logic gates. The DSP is more capable of performing a lot of functions based on variances of data. As shown in , if the control of the circuit is highly depended on data and many services are required, then the DSP is preferred over the FPGA.

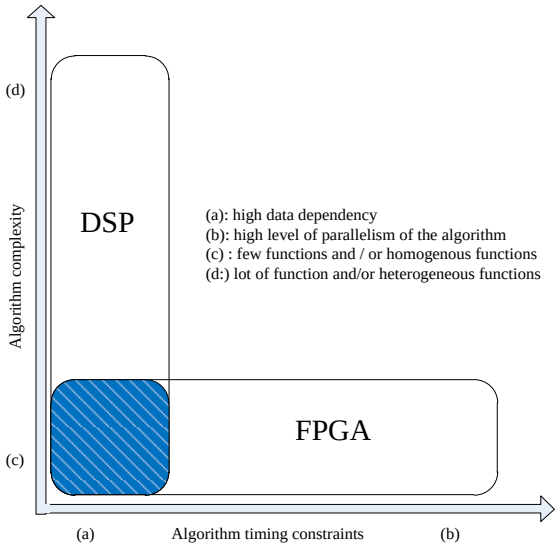


Figure 59: the use of the DSP and FPGA regarding the time constraints and the complexity.

Otherwise, if the circuit algorithm and the data process are highly homogenous, then the FPGA is preferred for its faster speed. In this case, especially for MMC, the number of the series-connected submodules can be large due to the system specifications. Furthermore, the data processing for the MMC focuses on the capacitor voltage balancing and the circulating current control. In regard to the capacitor voltage balancing, the algorithm of the voltage feedback loops determines the high level of parallelism in the data processing. Therefore, the FPGA is selected over the DSP in this case.

(b)Clock speed

Other important factors of selecting the FPGA are the clock speed, the number of the I/O pins, and the program language. However, the higher clock speed is always preferred but it can have a higher price. Fortunately, the average clock speed of FPGA technology has increased in the past a few decades. Therefore a regular commercially available control unit can fit the requirements of this test rig. For example, the highest frequency exists in the PWM control signals for the circuit. In the experiment test rig, the PWM carrier frequency is set at 3 kHz. Furthermore, due to the digital implementation of the PWM signal in the control unit, the samples per cycle are selected as 512 in co-operating with the reference signal, which means, to generate the 3 kHz carrier frequency, the control unit should generate $3\ KHz\ x\ 512$ step up and step down signals respectively. In this case, the minimum clock speed is depending on the carrier frequency of the MMC model. For the aforementioned model, the period of one operation cycle is calculated as $1\ /\ (\ 3\ KHz\ x\ 512\ )\ =\ 651ns$. Therefore the minimum clock speed is $1/651ns\ =\ 1.54MHz$. A quick desktop research reveals that the regular PIC33 series chips have around 40MHz clock speed which is capable of generating the 1 kHz carrier regarding the MMC model. However, the samples per cycle can be increased to reduce the converter output distortion generated by the change of the sampling frequency as stated in [182].

(c)Number of pins

For the MMC under consideration, one-phase contains eight submodules in total. This results in eight capacitor voltage feedback signals. Depending on the number of voltage sensors, the minimum pins required for the capacitor voltage readings are eight. Furthermore, the gate signals generated by the control unit are also transmitted to one-phase of the converter through its I/O pins. Because of the voltage level of the gate driver unit, the lever shifter is required to boost the voltage from 5v to 15v. Therefore, the number of pins required could be different since there is a level shifter in between the FPGA and the gate drive unit. The circuit of both the level shifters and the dual gate drive are detailed in Appendix C. Because the gate

signals for the dual gate drivers are complementary to each other, the gate signals can be reduced to several couples of gates signals instead. For each submodule, there is a couple of gate singles since the switch signals for these two switches are complementary. Because there are 8 submodules in total in the MMC circuit, the gate singles required for the dual gate drivers are $8 * 2 = 16$ PWM signals. However, the input voltage level of the dual gate drivers is at 15v, and the nominal voltage output of the FPGA control unit is between 3.3v and 5.0v. The level shifter is required to boost the voltage of the gate signals. Because the gate signals are boosted separately, the number of the gate signals remains the same

(d)Program language

The programming language is also an important consideration when choosing the control unit because advanced programming languages are faster and can perform the complex functions efficiently. In this case, the programming language for FPGA is based on the VHDL and Verilog. There are differences in the detail of these two languages, but they are similar to each other regarding the program structures. As with microcontrollers, a compiler is required to program the FPGA. .

Therefore, according to the aforementioned requirements, the DE0-NANO FPGA board from Altera was selected as the core controller for the experiment test rig. The board has two 40 pins headers to provide 72 I/O pins along with two 5v power pins, two 3.3v power pins, and four ground pins. The embedded ADC128S022 which has eight channels and a 12-bit A/D converter is used for the capacitor voltage measurements. The compiler used in this project is Quartus 11. Further details can be found in [184].

6.2.2.The level shifter and the dual gate drive controller

Because the voltage output of the DE0-NANO board is not high enough to drive inputs of the dual gate drive circuit, a level shifter is designed to boost the logic voltage levels. The SN75372 dual MOSFET driver is connected to the PWM outputs of the FPGA control unit. Details of the SN75372 can be found in [185]. The SN75372 level shifter is required to raise the FPGA voltage levels to a level compatible with the dual gate drive which is 15v. As stated in [4], the maximum output voltage of the SN75372 is 24V, which is high enough to drive the dual gate drive boards. On the other hand, the response time for this device is in *ns* scale. So it is fast enough to handle the PWM signals since the experimental test rig does not require a particular high-frequency PWM. The supply voltage V_{cc2} of the SN75372 is connected to 15v voltage source to generate the corresponding 15v PWM voltage output to enable the dual gate driver.

When the MOSFET is turned on, the capacitor inside the controlled submodule is charged or discharged by the arm current. Otherwise, the arm current is bypassing the submodule. The detailed structure is shown in Appendix C. Because of the in series connection of the submodules, the electrical potential of the submodules are different according to the position of submodule in the circuit. Therefore, the dual gate drivers are used to make sure the turning on and turning off voltages are suitable to the electrical potential of that particular submodule. Because the PWM signals for the submodules are in pairs, one dual gate driver can control a pair of MOSFETs in one submodule. Therefore, the number of the dual gate driver is the same as the number of the submodules.

6.2.3.Submodules and MMC circuit

The structure of the submodules in the experimental test rig is based on the half-bridge MMC. The submodule consists of two switches and one capacitor. The selection of the switch is based on the range of the nominal working voltages. The rated power of the experimental test rig is 100W and the DC source voltage is + /- 10v. The MOSFETs are related to withstand the full impact supply of 20v. The details of the FS3004 MOSFET used can be found in [186]. The rated maximum voltage of this device is 40v which guarantees the safety of the switches when subject to the worst-case voltage. On the other hand, the turning-on and turning-off delays are in *ns* scale which is more than adequate for this low-frequency PWM application.

The capacitor in the submodule is selected to withstand the voltage as the MOSFET switches. Again, the capacitor voltage rating must consider the worst case of full supply voltage of 20v. A capacitor with a 25v rating was chosen [187].

6.2.4.Voltage sensors and current sensors

Because the capacitor voltages are balanced with the use of voltage feedback, voltage sensors are necessary in the test rig. Because the voltage sensor is used to monitor the voltage variations of the capacitor voltage inside the submodule. Therefore, sensitive and fast response sensors are desirable. The selected voltage sensor has a $6\ V/\mu s$ slew rate, considering the capacitor voltage variations are within +/-10% of the rated voltage, the voltage sensor can monitor the capacitor voltage changes. The power supply of this sensor is +/-15V, +/-10mA, which can be provided directly by the on-board power supply. Further details of the selected voltage sensor can be found in [188]. The bandwidth of the AD215 is 120 kHz, which provides a high tracking performance to the voltage changes necessary for the proposed precise voltage balancing control. The voltage sensor readings are transmitted to the embedded

ADC128S002 A/D converter within DE0-NANO board. The minimum voltage difference that can be detected by the 12 bit A/D converter is 1mV, which enables predictive control based on the capacitor voltage variations.

The supply voltage of the selected current sensor ranges from 4.75V to 5.25V which can be supplied by the on-board power supply. The voltage and current rating of this current sensor is 5V and 6A respectively. This current has a fast response time which is less than 0.3ms. Because both upper and lower arm currents of the scale-down model are lower than 5A according to the power rating. Therefore, the selected current sensor can monitor the current changes in time. The details of the selected current sensors can be found in [189].The measured arm currents are transmitted into the ADC1061CIN A/D converter, the details of which can be found in [190].

6.3 Experimental setup

The system setup is detailed in Figure 60. The size of the control unit is much smaller compared to the PWM enabling circuits and the voltage sensors. Because of the parallel connection of the MMC circuit, the system can be easily modified by adding more submodules. The power sources consist of one 30V 2A dual DC power supply and one 30v 2A power supply. If necessary, the voltage level of the DC voltage sources can be increased to examine the electro-magnetic interference effects on the designed circuit in high voltage condition.

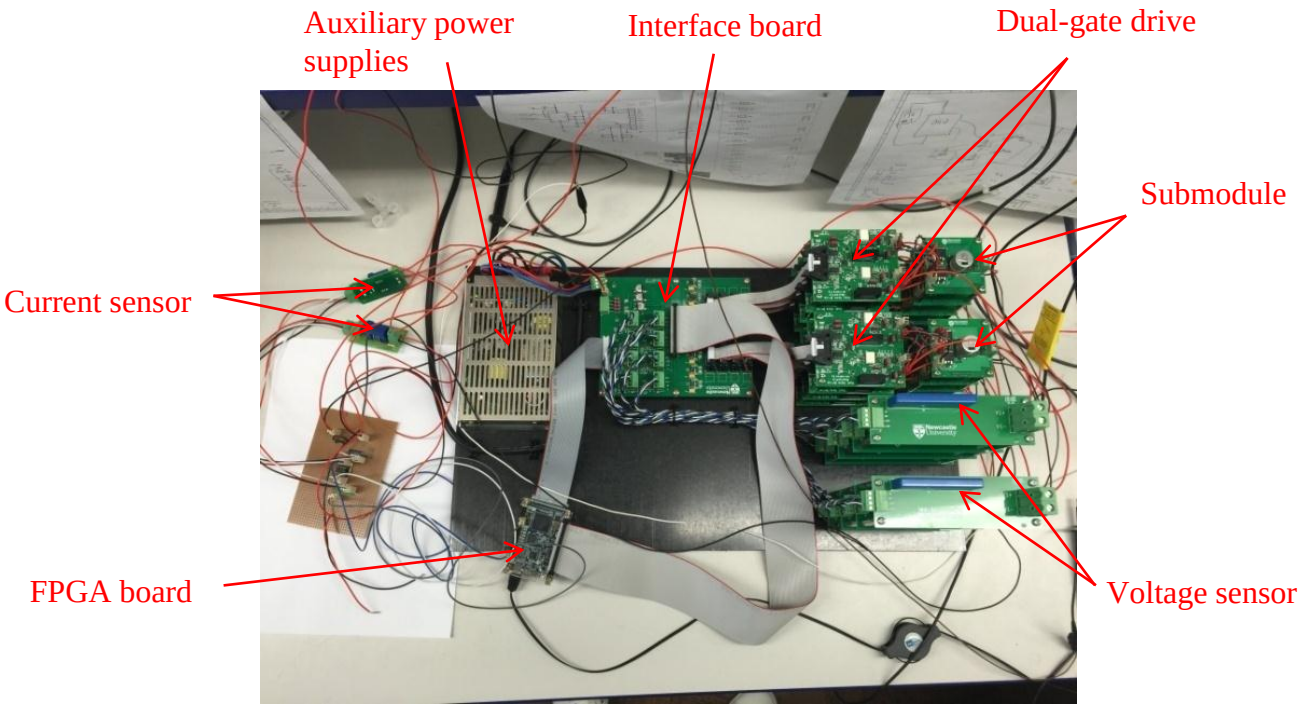


Figure 60: The experiment model of the hall-bridge based MMC.

The block diagram of the test rig is shown in Figure 58. The DE0-NANO FPGA board is collecting the voltage signals read from the MMC circuit and generates the corresponding PWM gate signals. There are eight feedback signals since there are eight submodules in total connected to both upper and lower arms. The 16 PWM gate pulse signals are transmitted into the level shifter for voltage boosting purposes. The gate pulse signals are increased from 5v to 15v to enable the dual gate driver. As demonstrated in Figure 58, to generate a 5-level converter voltage output, there are eight level shifters, eight dual gate drivers, and eight voltage sensors are required. When the converter voltage levels are increased, the components cost will increase significantly. However, one of the advantages of the MMC based transmission system is that the size of the AC side filter is much smaller than the conventional two-level or three-level VSC based transmission systems. Therefore, the realization of the MMC based system is focusing on the comparisons between the components cost, and the cost saved in regard to the AC side filter.

6.3.1.The measurement of the capacitor voltage

One of the difficulties of building the experimental test rig is the conversion between the digital signal and the analogue signal. Because in the simulation model, most of the signals are generated based on the build-in functions and they are required to be generated by the FPGA board in the experimental test rig. The capacitor voltage feedback signals are required to report the status of each submodule to the control unit. The communications between the voltage sensors and the control unit are presented as Appendix D.Because there are eight voltage sensors in total, channel selection is required to take readings from the first to eighth voltage sensor. As shown in Table 17, the channel number corresponds to the bit value of the CHL_Select.

Table 17: The channel selection code diagram

CHL_Select[4]	CHL_Select[5]	CHL_Select[6]	Channel Selected*
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

*: There are eight submodules in total in the MMC circuit. Therefore, the number of channel is eight.

The timing diagram of the ADC128S002 is shown in Figure 61. The $\overline{CS}$ is the chip select signal which is used to start a conversion at the falling edge of $\overline{CS}$, the conversion continues when $\overline{CS}$ stays low. *SCLK* is the digital clock input which controls the conversion process directly. *DIN* (represented as *Data* in code) is the digital date input which is used to indicate which channel the chip is reading in the same cycle. *DOUT* is the digital date output which is the digital representation of the analogue input, i.e. the capacitor voltage reading of the test rig.

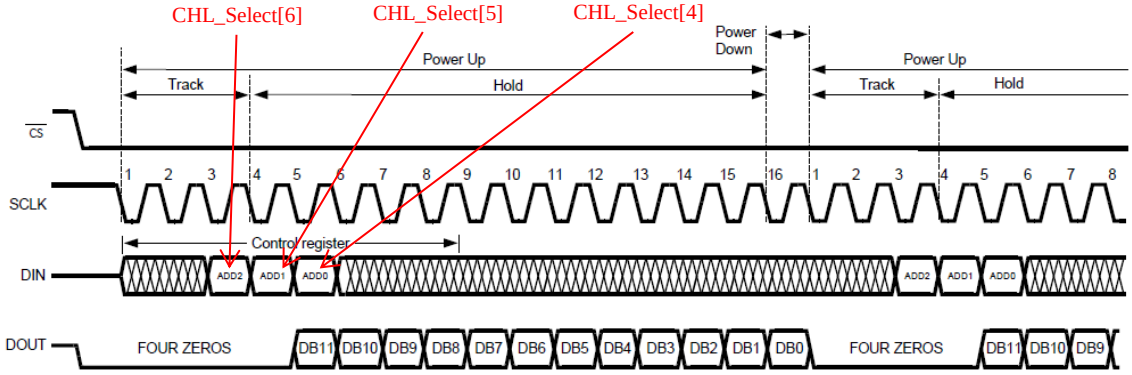


Figure 61: The timing diagram of the ADC128S002

The *DIN* is used to inform the control unit which bit of the voltage sensor feedbacks it is reading. The first three bits are "don't care" bits which are left blank during regular operation. However, the *DIN* is transferred in a reversed order. The fourth bit of the voltage sensor feedback is the most significant bit of the voltage feedback. The voltage feedback signals are stored in the *Vc_up1… Vc_up4* are the measurement of the capacitor voltages for the upper arm submodules, *Vc_low1… Vc_low4* are the measurement of the capacitor voltages for the lower arm submodules. The proposed voltage balancing control approach requires the measurement of the capacitor voltages in the previous operation cycle. To achieve this, the voltage feedback data are stored in *Vc_up1Reg* for one operation cycle and get refreshed every time the new operation cycle comes. This is the natural advantage of the test rig controller compared to the simulation. The FPGA registers are accessible during the normal operation. Therefore, the continuous measurement of the capacitor voltage can be done during the normal operation.

6.3.2.The measurement of the arm current

The proposed voltage balancing control approach does not require the measurement of the arm current. However, the measurement of the arm current is required in the circulating current suppressing control. Therefore, it is necessary to include the code for the arm current measurement. The code for taking the arm current readings from the current sensors is shown

in Appendix E. The model of the current sensor is Current transducer CAS 6. However, because the output of the current sensor is analogue, it is required another A/D converter to convert the analogue signal to the digital signal. In this case, the 10-bit parallel A/D converter ADC1061CIN is selected.

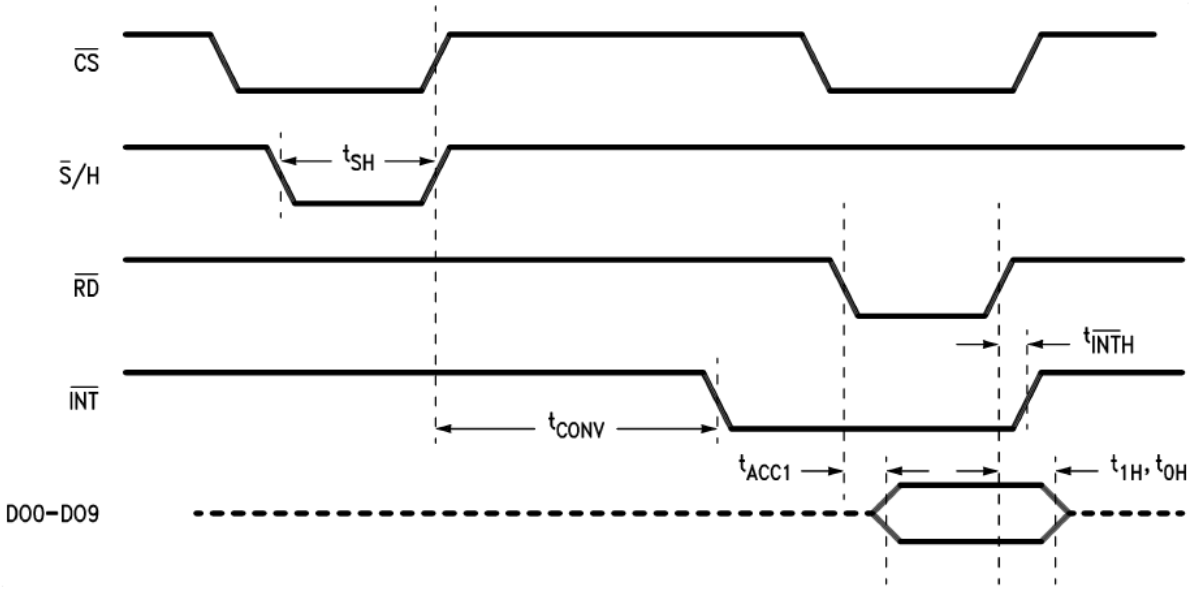


Figure 62: The timing diagram of the ADC1061CIN

The timing diagram of the ADC1061CIN is shown in Figure 62. Because it has 10-bit parallel output, it does not the clock signals as required in the ADC128S002. $\overline{CS}$ is the chip select bit. $\bar{S}/H$ is the sample and hold control input. When the pin is forced low, it causes the analogue input signal to be sampled and initiates a new conversion. $\overline{INT}$ is the active low interrupt bit, it goes to low at every end of the conversion. $\overline{RD}$ is the active low Read control input. When it is low, any data in the converter's register will be placed to the bus. As shown in Appendix E. GPIOTestEN1 and GPIOTestEN2 are the control input $\overline{INT}$ and $\overline{RD}$ separately. They are used to enable the A/D converter for the current readings. Because the conversion is forced to start when the control inputs are low, the I/O pins are set to zero to enable the readings of the A/D converter. GPIOTest1_1…GPIOTest_9 are the D00-D09 outputs as shown in Figure 62. They are used to store the parallel data read from the converter. GPIOTest1_1 is the least significant bit and GPIOTest1_9 is the most significant bit. As aforementioned, the A/D converter is working in the scale of *ns*, and the conversion speed is set according to the time register Time[5] and Time[6] which are the fifth and sixth bit of the time register. The time register is increasing by one each clock cycle which is at 50MHz. Therefore, the arm current reading is taken within $\frac{1}{50MHz} \times 2^5 = 640ns$. The readings are transferred to I_{up} and I_{low} which are representing the arm current readings of the upper and lower arm separately.

6.3.3.PWM generation

According to the analysis in previous chapter, the capacitor voltage ripple can be manipulated by changing the sampling time of the voltage readings. The sampling time Ts (operation cycle period) in (58) and (59) can have a great impact on the capacitor voltage ripple. Therefore, the generation of the PWM can be another aspect of determining the performance of the experimental test rig.

$$\sum_{k=1}^{n} N_{c\_upk} \cdot C_{upk} \int_{t}^{t+Ts} \left(\frac{Sin(\omega_s t)}{2} + I_{diff}\right) dt < V_{c\_up} \cdot 10\% \quad (58)$$

$$\sum_{k=1}^{n} N_{c\_lowk} \cdot C_{lowk} \int_{t}^{t+Ts} \left(\frac{Sin(\omega_s t)}{2} - I_{diff}\right) dt < V_{c\_up} \cdot 10\% \quad (59)$$

The generation of the PWM signal involves two parts: 1. The generation of the PWM carrier signals. 2. The generation of the gate pulse signal. The PD-PWM carrier signals are generated as shown in Figure 63. Because the frequency of the PWM carrier can affect the capacitor voltage ripples as aforementioned. Therefore, the impact of different PWM carrier frequency is investigated and the code is explained in Appendix F.

In order to generate the corresponding PWM signals, there were two registers used for this purpose. The "Time" register and the "bPWM" register. Because the FPGA is using the predefined clock speed which is 50MHz, and the PWM used in the circuit is 3.3 kHz, hence the transformation between the clock speed and the PWM signals is required. The "Time" register is used as a counter to store every clock step, Time register added by one whenever there is a clock pulse. Therefore, when the sixth bit of the Time register (Time [6]) is set at high, it means there are $2^6 = 64$ clock pulses have been stored. At that moment, the "bPWM" register will add one to represent the step up of the PWM signals. In this case, the values of the PWM signals can be stored in bPWM0…bPWM3 which are used to represent the four carriers in different magnitude. By setting the number of the bits it has in each bPWM register, the frequency of the PWM can be manipulated. In the experiment model, there are eight bits in the bPWM0 register (bPWM[8]), so there are $2^8 = 256$ operations cycles for the register to complete a full PWM cycle. For example, the PWM frequency f_s can be calculated as $f_s = \frac{50MHz}{2^6 * 2^8} = 3051Hz$ as shown in Table 18. Hence, the gate pulse signals can be generated inside the FPGA board according to the reference signal. The generation of the reference signal

depends on the capacitor voltage measurement (voltage balancing) and the arm current measurement (CCSC). And the measurement for both capacitor voltage and arm current can be obtained by the aforementioned codes. Therefore, proposed control approach can be compiled in the FPGA. The detailed code of generating the PWM signals is shown in Appendix F.

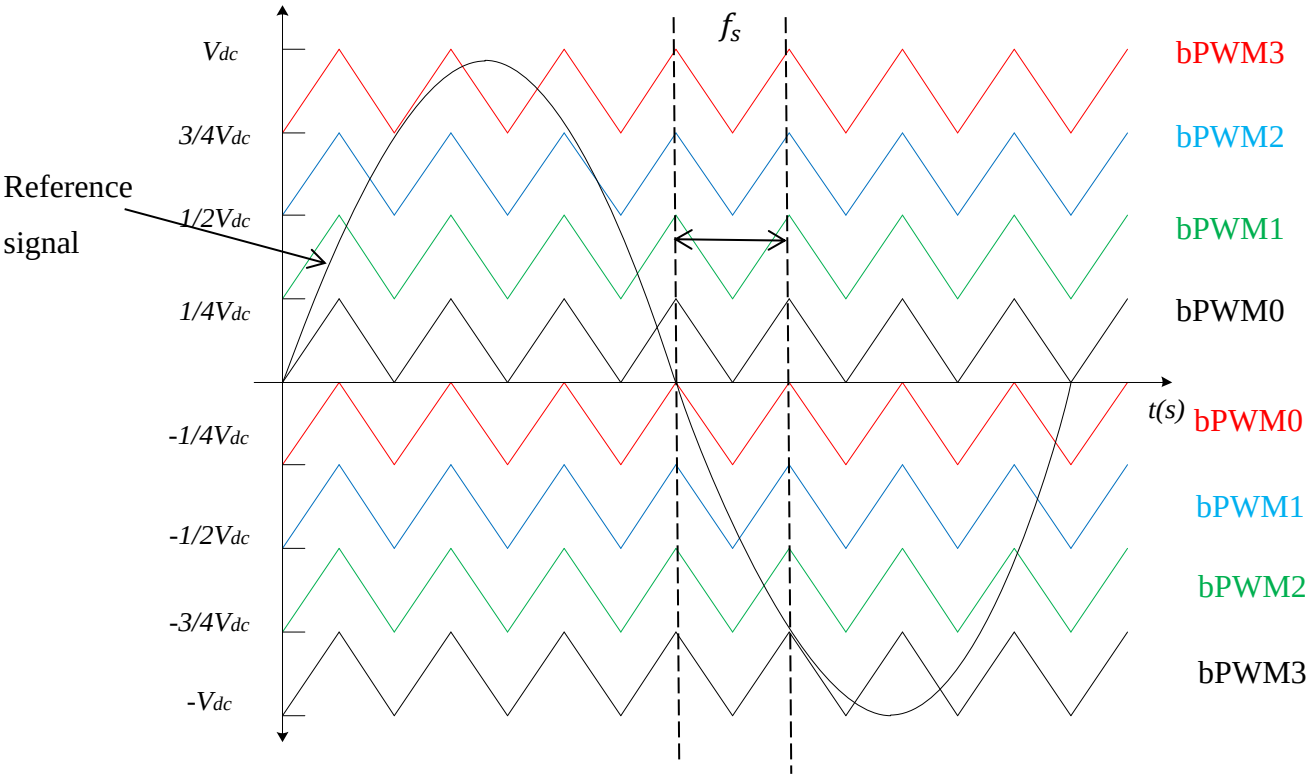


Figure 63: The PWM carrier signal and the reference signal.

Table 18: The PWM frequency list regarding the time register and the PWM register

Frequency (Hz) / Bit	Time[5]	Time[6]	Time[7]	Time[8]	Time[9]
bPWM0[5]	48828.00	24414.00	12207.00	6103.50	3051.75
bPWM0[6]	24414.00	12207.00	6103.50	3051.75	1525.88
bPWM0[7]	12207.00	6103.50	3051.75	1525.88	762.94
bPWM0[8]	6103.50	3051.75	1525.88	762.94	386.47
bPWM0[9]	3051.75	1525.88	762.94	386.47	193.24

6.3.4.Priority code generation

Since the voltage balancing and the circulating current suppression control are related to the control of the PWM pulse signals, it is necessary to combine the data readings and the PWM signals to balance the capacitor voltages or suppress the circulating current. Appendix G demonstrated the implementation of the priority code generation. The priority code is used to label the submodules from the highest capacitor voltage to the lowest capacitor voltage. The use of the priority code removes the need for the sorting processes which is required in conventional voltage balancing control. Therefore, it simplifies the control process. First, the capacitor voltage readings for all the submodules are taken and stored in the registers. The registers of adc-dataReg0…adc_dataReg7 are representing the capacitor voltages corresponding to a total eight submodules in both upper and lower arm. Then they are compared to each other to obtain the priority code which is assigned to the each submodule. The assignment of the priority codes is illustrated in Figure 64. Every submodule is selected to compare with to each other to generate the priority codes. The P0…P7 are the priority codes for the eight submodules respectively. The values of the priority codes P0…P7 are constant during one operation cycle.

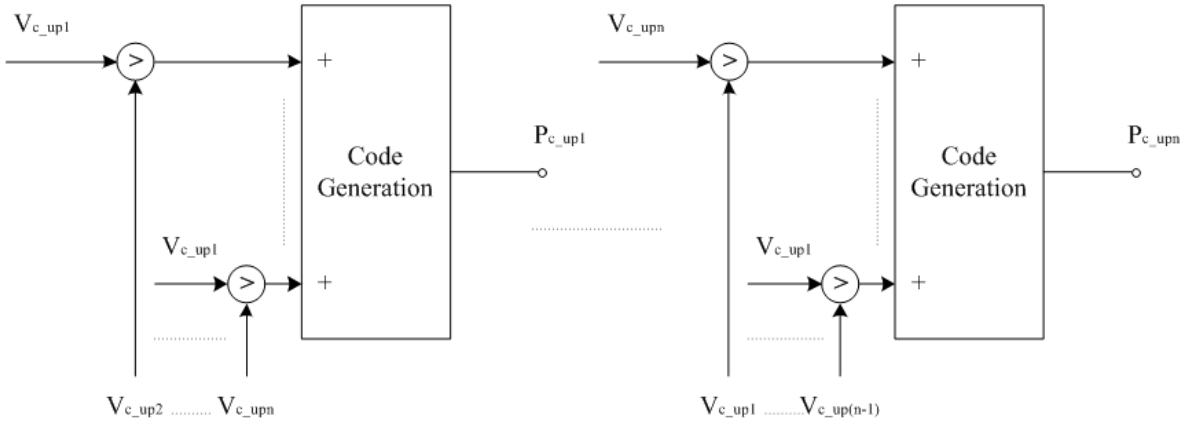


Figure 64: The assign of the priority codes

The priority codes are used to select the corresponding PWM pulses for the submodules. However, the voltage balancing control requires that the turn-on and turn-off processes for the submodules are different depending on the direction of the arm current, as shown in Figure 65. Based on the capacitor voltage variations, the PWM pulses are generated as Appendix H. However, there are four different conditions need to be considered.

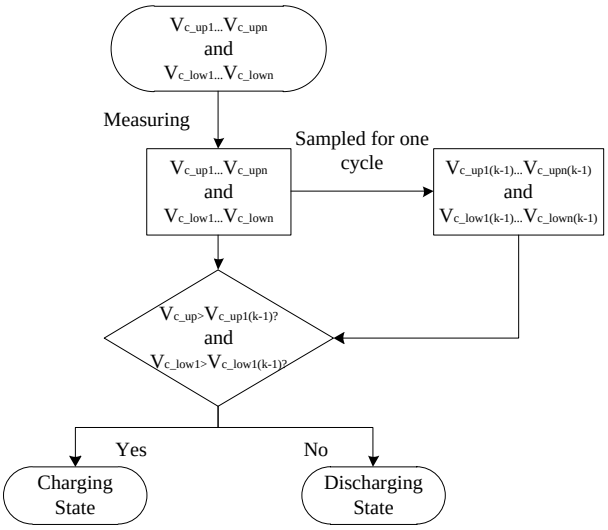


Figure 65: The states selection approach according to the capacitor voltage.

The sum of the capacitor voltages is compared to the sum of the capacitor voltages in the previous sampling cycle. If the result of the comparison indicates that the arm current is charging the capacitor, the submodule with the lowest capacitor voltage will be turned-on prior to others, otherwise the submodule with the highest capacitor voltage will be turned-on. Because the chance of the capacitor having the same voltages is highly unlikely, the priority codes for different submodules are distributed from zero to four as demonstrated in the program code. In this case, each of the four submodules can have a unique priority code. This avoids problems such as the discrete turning on and off actions and the imbalanced distribution of the DC voltages among the submodules. However, the PWM pulse signals for each submodule can be different depending on the capacitor voltage variations. There are four situations to consider during the normal operation. They are the 1). The upper arm current is charging the upper submodules. 2). The upper arm current is discharging the upper submodules. 3). The lower arm current is charging the lower submodules. 4). The lower arm current is discharging the lower submodules as demonstrated in Appendix I.

6.3.5.The implementation of the proposed control approaches

The simulation result in previous chapter has demonstrated the effectiveness of the proposed voltage balancing control and the circulating current suppression control. Therefore, it is necessary to verify the feasibility of the proposed control approaches in the experimental test rig. Because the proposed voltage balancing control approach does not require the measurement of the arm current, the readings of the current sensors are not required in the code. In addition, the CCSC does not require the measurement of the capacitor voltage. Only the arm

current readings are necessary in the CCSC. Therefore, the control approaches for the proposed voltage balancing and the CCSC are independent of each other, which avoids the potential conflicts and shortens the processing time. In Appendix I, the registers adc_dataReg0, adc_dataReg2, adc_dataReg5, and adc_dataReg7 contain the capacitor voltage readings of the upper arm submodules respectively, and registers adc_dataReg1, adc_dataReg4, adc_dataReg3, and adc_dataReg6 contain the capacitor voltage readings for the lower arm submodules respectively. The comparisons between the capacitor voltages determine the arm current directions in present operation cycle. Therefore the code implements the proposed voltage balancing control as shown in Figure 65.

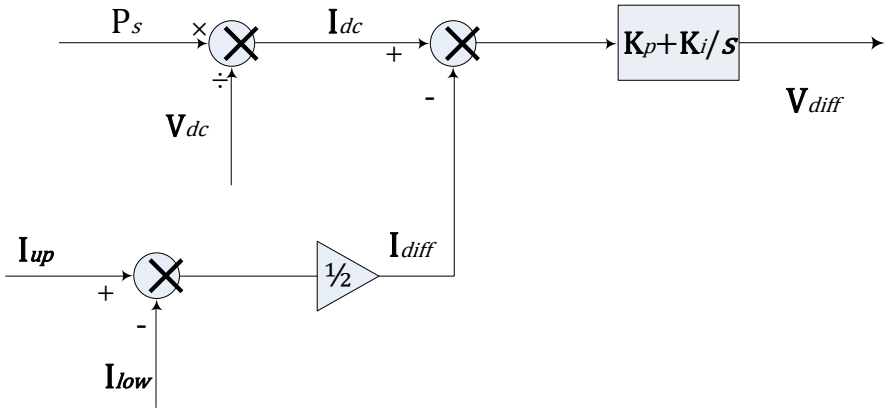


Figure 66: The control block diagram of the CCSC with measuring of both upper and lower arm currents.

As shown in Figure 66, the measurements required for the CCSC are the upper and lower arm currents, the converter transmitted power, and the DC voltage. The measurements of the capacitor voltages are not required. Because the arm currents are required in suppressing the circulating current, therefore the measurement of the arm current through two 10-bit A/D converters is included in the code. However, a key factor in the suppression the circulating currents is the differential current between the upper and lower arm. Therefore, the readings of both upper and lower arm currents are required to be taken in the same operation cycle. And to suppress the AC components of the circulating current, the differential currents are transmitted through the PID controller to generate the differential voltage. Therefore, in Appendix J, the $Constant$ is representing the proportional gain in the PID controller. $Vdiff\_control1$ and $Vdiff\_control2$ are the differential voltages obtained for the upper arm and lower arm separately. By adjusting the proportional gain of the $Vdiff\_control1$ and $Vdiff\_control2$, the suppression of the circulating current can be optimized. Because the passive loads are

used in the single-phase test rig, the reference signals are pure sinusoidal waveforms for simplicity. Therefore, the sampled reference signals are generated using step up and step down functions as shown in Appendix K. The Time register (Time[])set the minimum step period for the reference signal. The $RefSignal$ indicates how many steps in one cycle of the reference signal. In this case, the frequency of the reference signal is calculated as: $f_r = \frac{50MHz}{2^{13}*128} = 47.68Hz$. The frequency can be adjusted according to the system requirements.

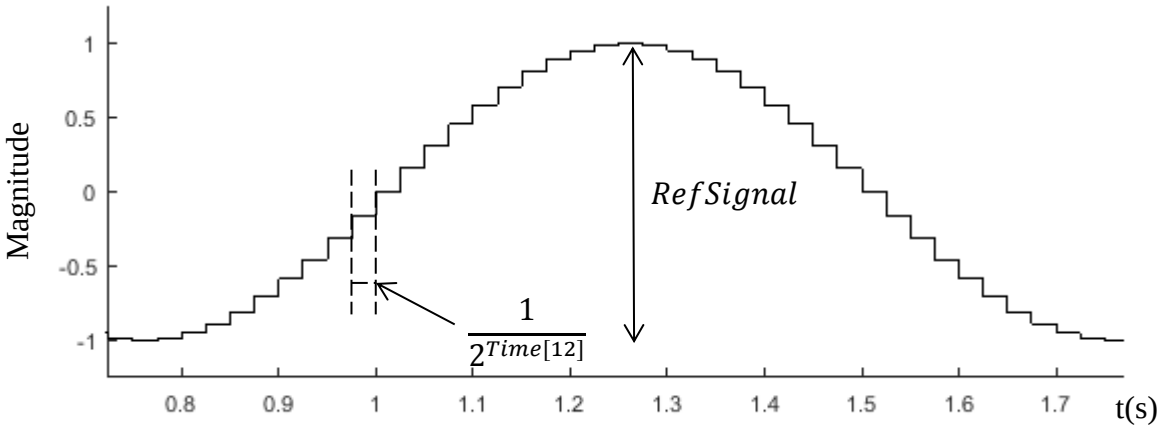


Figure 67: The step-up step-down generation of the reference signal

Chapter 7

Conclusion and future work

7.1 Introduction

The desire for greater interconnection of power system networks has stimulated the development of the distance transmission systems. As one of the most promising applications, the MMC-based HVDC transmission system is receiving more attention due to its low transmission losses over long distances. The related areas range from the renewable energy, such as wind farm, photovoltaic connections, to variable speed drives and other FACT applications. Because the MMC based HVDC transmission systems are always preferred in medium or high voltage application which normally has a very high power rating. Even a 10% saving would be significant considering the large power rating of the applications. The potential for this specific technology is overwhelming. This has benefits in particular for subsea cables, and its unique ability to interconnect two grids with different fundamental frequencies. In order to reveal the potential opportunity in improving the efficiency and reliability of the MMC based system. The proposed control approach is established based on publications produced in recent period. The key element of this technology is to suppress the unnecessary circulating current existing inside the power electronics, which lower the stresses son each components and reduce the output harmonics. The initial simulation and test have demonstrated clear benefits of harmonic reduction, which in turn will reduce the investment of hardware and increase the reliability of the equipment. The characteristics of the MMC converters are investigated using a mathematical model, to examine external and internal control loops, voltage balancing, and circulating current suppression.

7.2 Findings with regard to the modelling and experimental test rig of the MMC

7.2.1.The mathematical model

The modelling of the MMC involves the build of the mathematical model. Several modelling approaches are investigated and they suggested that the characteristics of the MMC are similar to the conventional VSC. Therefore, the conventional control approaches used for the VSC can be applied to the MMC with a little or no modifications. This provides a convenient way of designing the control approach for a particular MMC-based HVDC transmission system. However, the difference between the MMC-based HVDC transmission systems and the conventional VSC-based HVDC transmission systems is the number of the voltage level. There

are a lot more voltage level of the MMC-based HVDC transmission system than the conventional VSC-based HVDC transmission system. Therefore, the modelling of the MMC can be difficult as there are a large number of submodules in each arm of the converter. However, based on the aforementioned assumptions, the arm submodules can be replaced by the controllable voltage sources which have the same arm voltage as the submodules. This approximation significantly reduces the modelling requirement for the MMC-based system and can also provide accurate simulation results when the voltage level is high. And the investigation of the voltage difference between the upper arm and lower arm voltages indicates that the inner voltage is an essential parameter to control the MMC. Besides that, the differential voltage is also suggested by the mathematical model to suppress the AC components in the circulating current. The investigation regarding the upper arm current and the lower arm current suggests the AC component in the circulating current is related to the differential voltage. And a major part of the AC component in the circulating current is at double-fundamental frequency. Therefore, the two different CCSC can be implemented. One is focusing on eliminating the double-fundamental frequency AC currents in the circulating current. The other is based on the differential voltage which is focusing on regulating the upper and lower arm voltages.

7.2.2.Selection and comparison of the PWM scheme

Depending on the voltage level of the MMC, the modulation of the reference signals can be either PWM or NLM. However, the requirement boundary between these two modulation methods is not distinct. When the converter voltage level is low (the number of submodules is low), the PWM method can be conventional PD-PWM and PS-PWM with or without interleaving technology. The interleaving technology is considered to have the ability to increase the number of the converter output voltage levels without adding more submodules. That leads to more frequent turn-on and turn-off actions to generate the higher voltage levels, hence the switching losses and the circulating current. When the converter voltage level is high (the number of submodules is high), the NLM is preferred because of its lower switching losses thus higher efficiency. However, as aforementioned, the selection of the PWM or NLM is depending on the system requirements, such as the maximum switching frequency, converter output harmonic levels, etc. It is not determined by the number of the submodules solely. In the simulation model and the experimental test rig, the low voltage level of the converter determines that the PWM methods are preferred. Therefore, the investigation of the differences between the PD-PWM and the PS-PWM is necessary. The selections of the PWM method depend on the control difficulty and the performance of the converter. The PS-PWM

scheme has a better converter output voltage than the PD-PWM scheme based on the simulation results. However, the implementation of the PS-PWM is more difficult than the PD-PWM, because it is controlled by changing the phase angle of each carrier instead of changing the magnitude.

7.2.3.The proposed voltage balancing control

The voltage balancing control is one of the two major controls in the MMC-based applications. Because of there are capacitors inside each submodule, the currents flowing into the submodule will charge or discharge the capacitor, causing the capacitor voltage deviations. Without appropriate control, the capacitor voltage will tend to increase or drop uncontrollably. This generates a large amount of harmonics at the converter output voltage and the circulating current flowing from arms to arms. Therefore, the voltage balancing control is necessary in the controls for capacitor-based multilevel converters. However, depending on the control approach, the voltage balancing controls are divided into two parts. One requires the measurement of the arm current. The other does not require the measurement of the arm current. The commonly used voltage balancing approach requires the monitoring of the arm current in order to determine the charge and discharge states of each submodule. The other control approach, which does not require the measurement of the arm current, is using more control loops than the commonly used one. The cost increase is one of the major problems preventing the implementation of the voltage balancing control while not measuring the arm current. Therefore, the proposed voltage balancing control approach reduces the use of the extra loop in order to lower the number of extra components required. The proposed voltage balancing control approach does not require the measurement of the arm current. The simulation results have shown the successful control of the MMC. The dynamic responses of this approach are also investigated. The settle time is within half of the cycle. Further experimental results have also shown the fast dynamic response of this control approach against the changes of modulation index or the circulating current control. In addition, the simulation results using Matlab have demonstrated the high immunity to the sampling frequency disturbance compared to the commonly used control approach. When the sampling frequency is low, the capacitor voltage deviation is as high as 40% for the conventional voltage balancing control, whereas the proposed voltage balancing control can maintain it below 15%. Therefore, it can provide a larger margin when selecting the appropriate sampling frequency or PWM carrier frequency for the MMC-based applications.

7.2.4.AC current suppression control

The CCSC is the other necessary control required in the MMC-based applications. Because of the voltage difference existing between the upper arm and lower arm, the circulating current can flow from arm to arm. The magnitude of the circulating current is depending on the differential voltage as deduced in the mathematical model. Therefore, it can be suppressed by reducing the differential voltage between the upper and lower arm. Some of the CCSC involves the decoupling of the arm current in order to eliminate the double-fundamental frequency component in the circulating current. These control approach requires the decoupling control loop which is focusing on eliminating the double-fundamental frequency component. This increases the computational requirement of the system which potentially increase the cost. Therefore, the proposed CCSC is developed based on the previous papers and further simplified. The proposed CCSC does not require the PR controllers which are tuned at higher order harmonics to get rid of the AC components in the circulating current. It is based on the balancing of the power transmitted through the converter. Because the decoupling process and the PR controllers are not required in this approach, the dynamic performance of the system is promising in both simulation and experimental results. Most of the doubly-fundamental harmonics in the circulating current have been suppressed from up to 250% down to nearly 8% of the fundamental frequency. However, a small amount of harmonics around 4% at the PWM carrier frequency is observed. As a result of the reduced capacitor voltage deviation, the harmonics at the converter output voltage is reduced by 3.3%, indicating the successful control of the MMC.

7.2.5.The experimental test rig setup

The setup and the programming of the experimental test rig are the major reasons that affecting the performance of the converter. The selection of the hardware component is emphasized to demonstrate the criteria which are important to the required system performance. The clock speed of the control unit can affect the maximum sampling speed, PWM frequency, and the maximum converter output frequency. In this case, the clock speed of the FPGA board is selected as 50MHz which is 15k times faster than the carrier frequency which is at 3.3 kHz. This guarantees the PWM cycle can be completed within 1% of the FPGA board capability. The number of the I/O pins sets the threshold of the minimum number of pins required. Depending on the circuit connections and the design of the header, some of the pins can be used as power supplies or grounds. Therefore, an investigation of the arrangements of the I/O pins

is necessary before selecting particular FPGA. The nominal voltage for each component is another important factor in determining the design of the circuit. The sensors are the last to select because they are selected based on the voltage ratings of the affected components, i.e. capacitors in the submodules of the experiment model. The coding is depending on the development software used by the FPGA board. According to the investigations of the control signal generations, the generations of the control signals are different from the simulation codes. However, the realization of the simulation model can be done in different ways based on the different control unit selected. The FPGA-based DE0-NANO board was selected to control the MMC test rig for its highly competitive data processing speed and the parallel data transferring ability. Further optimization of the program codes could potentially improve the accuracy and speed of the overall control system.

7.3 General conclusions

The general conclusion can be categorized into conclusions about the mathematical model of the MMC, the selection and comparison of the PWM schemes, the proposed voltage balancing control, and the AC current suppression in the circulating current. Although they are presented in this section as solitary units, they are to be interpreted properly and understood in combination with information provided in the chapters presented in this thesis.

- The simplified mathematical model of the MMC is produced and used to show that the control approach used for the conventional VSC-based system could be applied to the MMC-based system with moderate modifications. It also reveals that the inner voltage can be used as a control variable to balance the energy distribution among the submodules.
- The comparison between the PS-PWM and PD-PWM schemes has been included. The philosophies of each modulation methods were investigated, and the simulation results showed the simplicity and accuracy of the PD-PWM compared to the PS-PWM when the converter has multiple voltage levels. The 40-level MMC was designed and tested in MATLAB to illustrate the minimum number of the submodules in each arm to minimize the converter output harmonic. The THD of the 40-level MMC is lower than the planned in grid codes requirements.
- The energy distribution among the submodules is achieved by assigning the proper gate signals to the corresponding submodules in accordance with the capacitor voltage variations. The proposed voltage balancing method derived the current directions from

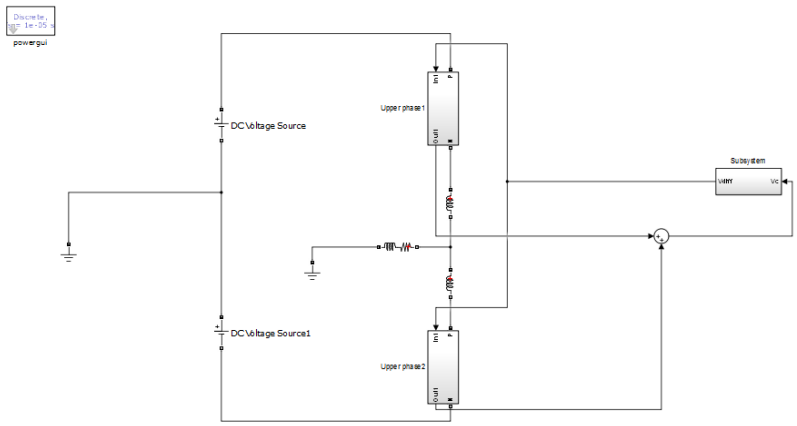
the arm voltage changes. Therefore the usage of the current sensors was reduced to simplify the communication between the sensors and the control unit. In addition, it also lowers the impact of component failure during regular operations.

- The control system of the MMC is completed by inserting the differential voltage into the reference signals to suppress the circulating current. The two-terminal MMC-based system employing the proposed control system was designed, and the performance was evaluated. Both simulation and experimental results have proven the promising AC current suppression in the circulating current.

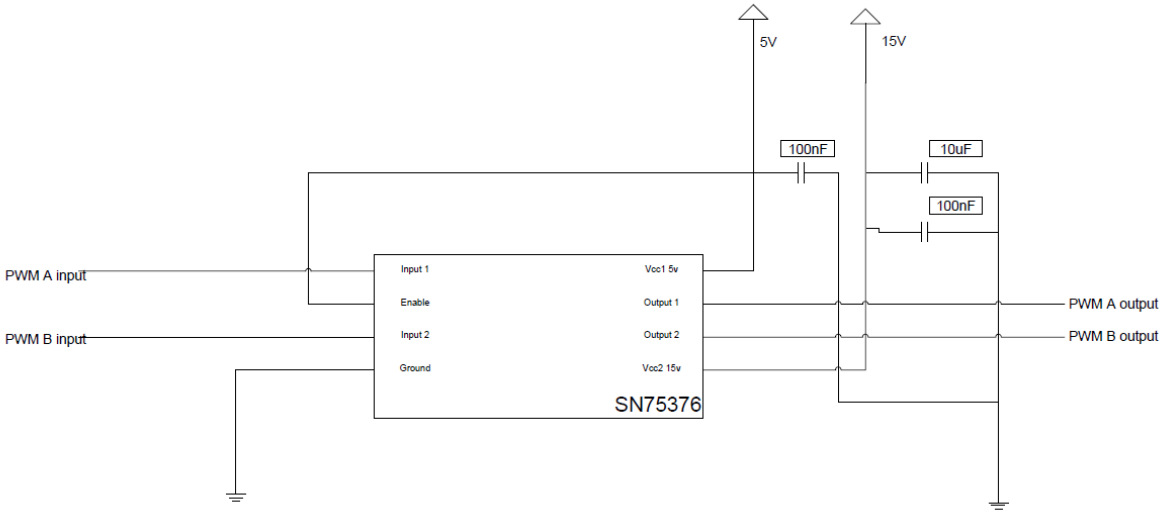
7.4 Future work

One of the primary barriers of commercializing the MMC-based HVDC system is the higher initial investment of the substation when compared to the conventional two-level or three-level HVDC system. Therefore, the control approach can be improved to reduce the necessary components such as the voltage sensors. Because of the unfavourable working conditions for the DC circuit breaker, most of the research regarding the MMC-based systems was focusing on the regular operations. Limited practical work has been done regarding the fault conditions on the DC side or imbalanced grid conditions. On the other hand, the transmission voltage of the MMC-based HVDC system can be ultrahigh which will have a great impact on the requirements of the transmission line, i.e. the cables. Above all, the future of the MMC-based application is promising yet challenging.

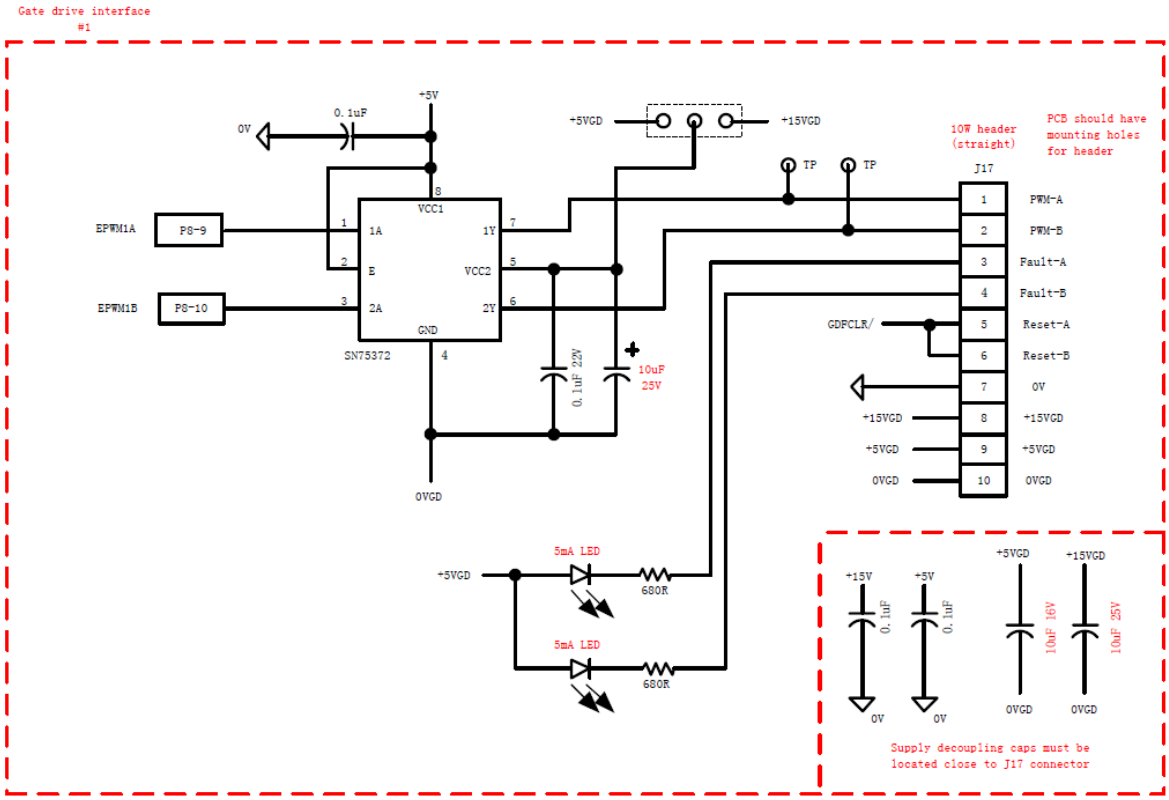
Appendix A The Simulink model for 41 level MMC



Appendix B: Level shifter



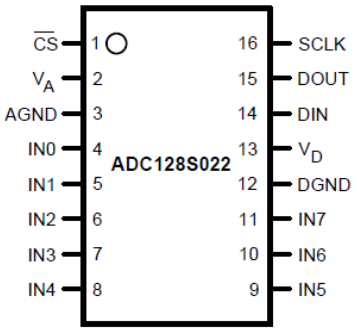
Appendix C: Dual gate driver



Appendix D: Channel selection

Symbol	Description
CHL_select	Channel selection bit, the fourth, fifth and sixth bit are used to define the channel number.
Data	Digital input bit, determine the channel selection bit for next cycle
m_cont	Continuous input bit, record the current bit number for reference.
Vc_up1	Storage register, store the capacitor voltage reading for channel 0.
adc_dataReg0	Storage register, store the capacitor voltage reading for channel 0 in previous cycle.

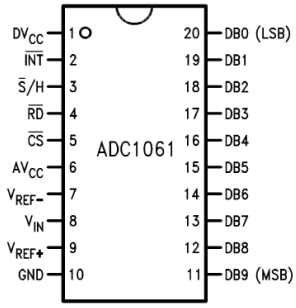
```
if( ( CHL_select [4] = = 0 ) && ( CHL_select [5] = = 0 ) && ( CHL_select [6] = = 0 ) )
begin
case ( m_cont )
1:Data = 0 ;
2:Data = 0 ;
3:Data = 1 ;
4:Vc_up1 [11] = iDOUT ;
5:Vc_up1 [10] = iDOUT ;
6:Vc_up1 [9] = iDOUT ;
7:Vc_up1 [8] = iDOUT ;
8:Vc_up1 [7] = iDOUT ;
9:Vc_up1 [6] = iDOUT ;
10:Vc_up1 [5] = iDOUT ;
11:Vc_up1 [4] = iDOUT ;
12:Vc_up1 [3] = iDOUT ;
13:Vc_up1 [2] = iDOUT ;
14:Vc_up1 [1] = iDOUT ;
15:Vc_up1 [0] = iDOUT ;
endcase
CHL_select = CHL_select + 1 ;
```



```
m_cont = m_cont + 1 ;
adc_dataReg0_1 = adc_dataReg0 ;
if ( m_cont = = 15 )
adc_dataReg0 = Vc_up1 ;
```

Appendix E: Current sensor readings

Symbol	Description
Time	Time register, set the conversion speed
GPIOTestEN	Enable bit, active the chip
GPIOTest	Output bit, the digital output of the analogue input
C_Reading	Storage register, store the output bits.




```
if ( Time [5] = = 1 || Time [6] = = 1 )
begin
GPIOTestEN1 = 0 ;
GPIOTestEN2 = 0 ;
C_Reading1 = GPIOTest1_2*1 + GPIOTest1_3*2 + GPIOTest1_4*4 + GPIOTest1_5*8 + GPIOTest1_6*16 + GPIOTest1_7*32 + GPIOTest1_8*64 + GPIOTest1_9*128 ;
C_Reading2 = GPIOTest2_2*1 + GPIOTest2_3*2 + GPIOTest2_4*4 + GPIOTest2_5*8 + GPIOTest2_6*16 + GPIOTest2_7*32 + GPIOTest2_8*64 + GPIOTest2_9*128 ;
```

Appendix F: PWM generation

```
always @ (  posedge Time [6]  )
begin
 if (  ~cs_n  )
begin
bPWM1  =  0  ;
bPWM2  =  0  ;
bPWM3  =  0  ;
if (  PWM_adder  =  =  0  )
begin
bPWM0  =  bPWM0  +  1  ;
PWM_adder  =  bPWM0 [7]  ;
end
else bPWM0  =  bPWM0 – 1  ;
if (  bPWM0  =  =  0  )
PWM_adder  =  0  ;

bPWM1  =  bPWM0  +  128  ;
bPWM2  =  bPWM0  +  256  ;
bPWM3  =  bPWM0  +  384  ;

end
end
```

Appendix G: Priority code generation

```
always @ (  posedge Time [4]  )
begin
 if (  ~ cs_n  )
begin
if  (  ~CCSC_en  )
begin
p0 = 0 ;
p1 = 0 ;
p2 = 0 ;
p3 = 0 ;

p4 = 0 ;
p5 = 0 ;
p6 = 0 ;
p7 = 0 ;

if ( adc_dataReg1 > adc_dataReg4 )
p0 = p0 + 1 ;
if ( adc_dataReg1 > adc_dataReg3 )
p0 = p0 + 1 ;
if ( adc_dataReg1 > adc_dataReg6 )
p0 = p0 + 1 ;

if ( adc_dataReg4 > adc_dataReg1 )
p1 = p1 + 1 ;
if ( adc_dataReg4 > adc_dataReg3 )
p1 = p1 + 1 ;
if ( adc_dataReg4 > adc_dataReg6 )
p1 = p1 + 1 ;

if ( adc_dataReg3 > adc_dataReg1 )
p2 = p2 + 1 ;
if ( adc_dataReg3 > adc_dataReg6 )
p2 = p2 + 1 ;
if ( adc_dataReg3 > adc_dataReg4 )
p2 = p2 + 1 ;

if ( adc_dataReg6 > adc_dataReg1 )
p3 = p3 + 1 ;
if ( adc_dataReg6 > adc_dataReg3 )
p3 = p3 + 1 ;
if ( adc_dataReg6 > adc_dataReg4 )
p3 = p3 + 1 ;

if ( adc_dataReg0 > adc_dataReg2 )
p4 = p4 + 1 ;
if ( adc_dataReg0 > adc_dataReg5 )
p4 = p4 + 1 ;
if ( adc_dataReg0 > adc_dataReg7 )
p4 = p4 + 1 ;

if ( adc_dataReg2 > adc_dataReg0 )
p5 = p5 + 1 ;
if ( adc_dataReg2 > adc_dataReg5 )
p5 = p5 + 1 ;
if ( adc_dataReg2 > adc_dataReg7 )
p5 = p5 + 1 ;

if ( adc_dataReg7 > adc_dataReg2 )
p6 = p6 + 1 ;
if ( adc_dataReg7 > adc_dataReg0 )
p6 = p6 + 1 ;
if ( adc_dataReg7 > adc_dataReg5 )
p6 = p6 + 1 ;
```

```
if ( adc_dataReg5 > adc_dataReg7 )
p7 = p7 + 1 ;
if ( adc_dataReg5 > adc_dataReg0 )
p7 = p7 + 1 ;
if ( adc_dataReg5 > adc_dataReg2 )
p7 = p7 + 1 ;

end
```

Appendix H: PWM selection 2

Condition

```
    if ( adc_dataReg0_1 + adc_dataReg2_1 + adc_dataReg5_1 + adc_dataReg7_1 <  = adc_da-
taReg0 + adc_dataReg2 + adc_dataReg5 + adc_dataReg7 )
    begin
    case ( p0 )
    0:PWM_selected0 = bPWM0 ;
    1:PWM_selected0 = bPWM1 ;
    2:PWM_selected0 = bPWM2 ;
    3:PWM_selected0 = bPWM3 ;
    endcase
```

Appendix I: Proposed voltage balancing control

```
if ( adc_dataReg0_1 + adc_dataReg2_1 + adc_dataReg5_1 + adc_dataReg7_1 <  = adc_dataReg0 + adc_dataReg2 + adc_dataReg5 + adc_dataReg7 )
if ( adc_dataReg0_1 + adc_dataReg2_1 + adc_dataReg5_1 + adc_dataReg7_1 > adc_dataReg0 + adc_dataReg2 + adc_dataReg5 + adc_dataReg7 )
if( adc_dataReg1_1 + adc_dataReg4_1 + adc_dataReg3_1 + adc_dataReg6_1 < adc_dataReg1 + adc_dataReg4 + adc_dataReg3 + adc_dataReg6 )
if( adc_dataReg1_1 + adc_dataReg4_1 + adc_dataReg3_1 + adc_dataReg6_1 >  = adc_dataReg1 + adc_dataReg4 + adc_dataReg3 + adc_dataReg6 )
```

Appendix J: Differential voltage control signal generation

```
always @ ( posedge Clock  )
begin
Constant = 4 ;
if  ( CCSC_en  )
begin
if  ( Constant >  = C_Reading_Reg1  )
begin
Vdiff_control1 =  (  ( Constant-C_Reading_Reg1 + C_Reading_Reg2  ) *50  )  ;
Vdiff_control2 = 0 ;
end
else
begin
Vdiff_control1 = 0 ;
Vdiff_control2 =  (  ( C_Reading_Reg1-Constant + C_Reading_Reg2  ) *50  )  ;
end
```

Appendix K: Reference signal generation

```
always @  ( posedge Time [12]  )
begin
 if  ( ~cs_n  )
begin

if ( 1  )
begin
RefSignal = RefSignal + 1 ;
case ( RefSignal  ) //RefSignal
0:RefValue = 256 ;
1:RefValue = 269 ;
2:RefValue = 281 ;
…
```

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