SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

μSystems Research Group

Power Efficient, Event Driven Data Acquisition and Processing using Asynchronous Techniques

by

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ABSTRACT

Doctor of Philosophy

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Data acquisition systems used in remote environmental monitoring equipment and biological sensor nodes rely on limited energy supply soured from either energy harvesters or battery to perform their functions. Among the building blocks of these systems are power hungry Analogue to Digital Converters and Digital Signal Processors which acquire and process samples at predetermined rates regardless of the monitored signal's behavior. In this work we investigate power efficient event driven data acquisition and processing techniques by implementing an asynchronous ADC and an event driven power gated Finite Impulse Response (FIR) filter.

We present an event driven single slope ADC capable of generating asynchronous digital samples based on the input signal's rate of change. It utilizes a rate of change detection circuit known as the slope detector to determine at what point the input signal is to be sampled. After a sample has been obtained it's absolute voltage value is time encoded and passed on to a Time to Digital Converter (TDC) as part of a pulse stream. The resulting digital samples generated by the TDC are produced at a rate that exhibits the same rate of change profile as that of the input signal. The ADC is realized in 0.35μm CMOS process, covers a silicon area of 340μm by 218μm and consumes power based on the input signal's frequency.

The samples from the ADC are asynchronous in nature and exhibit random time periods between adjacent samples. In order to process such asynchronous samples we present a FIR filter that is able to successfully operate on the samples and produce the desired result. The filter also poses the ability to turn itself off in-between samples that have longer sample periods in effect saving power in the process.

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Acknowledgements

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I am deeply indebted to my parents who have stood by and supported me throughout my life. It is because of their inspiration and encouragement that I am able to be where I am today.

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Chapter 1

Introduction

1.1 Motivation

With the increased innovation in the area of low power electronics devices, there has been a growing interest in the biomedical field to build low power implantable devices for monitoring various biological signals such as Local Field Potential neural signals [1]. These applications usually use sensor arrays consisting of a large number of signal conditioning amplifiers and there subsequent Analogue to Digital converters (ADC) [2], forming separate channels which output streams of digital bits. These resulting digital bits are thereafter passed on to a local digital signal processor as done in [3], [4] and [5] or transmitted (wired or wirelessly) as done in [6], [7] and [8] to an external processor for digital processing. A typical sensor node consists of a signal conditioning Analogue Front End (AFE) and an ADC. The AFE amplifies the sensed signal and filters it to obtain its desired baseband frequency components before being passed to the ADC. As the sensor channels increase, the power consumption and die area also increases substantially. In order to mitigate the problem of increased die area, a single ADC can be multiplexed [7] to operate on a group of AFE channels as shown in figure 1.1. This will in turn necessitate operating the ADC at a relatively high sampling rate resulting in large power consumption. As a result of the high sampling rate, the output data rate also increases requiring even more power for the data to be transmitted to the next processing stage. This becomes a big problem for implanted sensor nodes as they are typically required to operate at a low power budget, with the

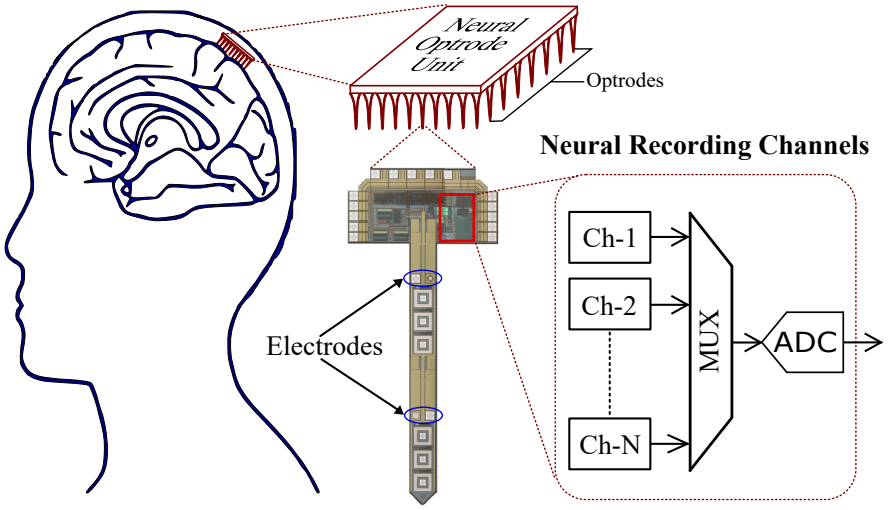


Figure 1.1: An implantable multi-sensor optical-electro neural interface chip [10]. Each sensing channel may have its local ADC or share a single ADC with multiple channels via multiplexers.

energy being sourced from either batteries or from energy harvesters. The increased sampling and data rates can be directly attributed to the use of conventional synchronous Nyquist rate [9] ADCs that sample signals at a rate which is at least twice the frequency of the highest expected spectral component of the signal. These ADCs output digital data at a constant rate independent of the signal characteristics; continuously giving uniformly spaced samples even when the sensed signal is non-changing or reduces in frequency. This results in the generation of unnecessary samples leading to unnecessary power consumption in the ADC as well as in the subsequent digital processing stages. Instead of continuously sampling these kinds of signals at a relatively high constant sampling rate dictated by the highest expected frequency, it would be desirable to have an ADC that samples the signal at a rate dictated by the signal itself. This would allow the ADC to adapt its sampling rate to the input signal's changes in frequency and generate no samples when the signal is not changing.

1.2 Asynchronous Signal Sampling

Conventional ADCs operate by sampling signals synchronously under the control of a clock resulting in a fairly constant power consumption profile. In applications such as implantable neural recording devices and "always on" speech recording devices, the recorded signals are usually sparse, bursty and of low frequencies (1Hz-20Khz in audio applications and 1Hz-100Hz in neural recording applications). Sampling these signals synchronously results in constant power consumption in the ADC regardless of the signals activity. In order to address the constant power consumption in the ADCs the conventional nyquist rate ADCs are beginning to be replaced with asynchronous level crossing ADCs [11], [12], [13]. The main principle used in these types of ADCs is to sample the signals only when they cross given quantized thresholds and remain idle when the signal exhibits no activity. Figure 1.2a shows a signal being sampled at a constant rate, at or above the nyquist rate of period T_s. This gives a constant number of sampled values for

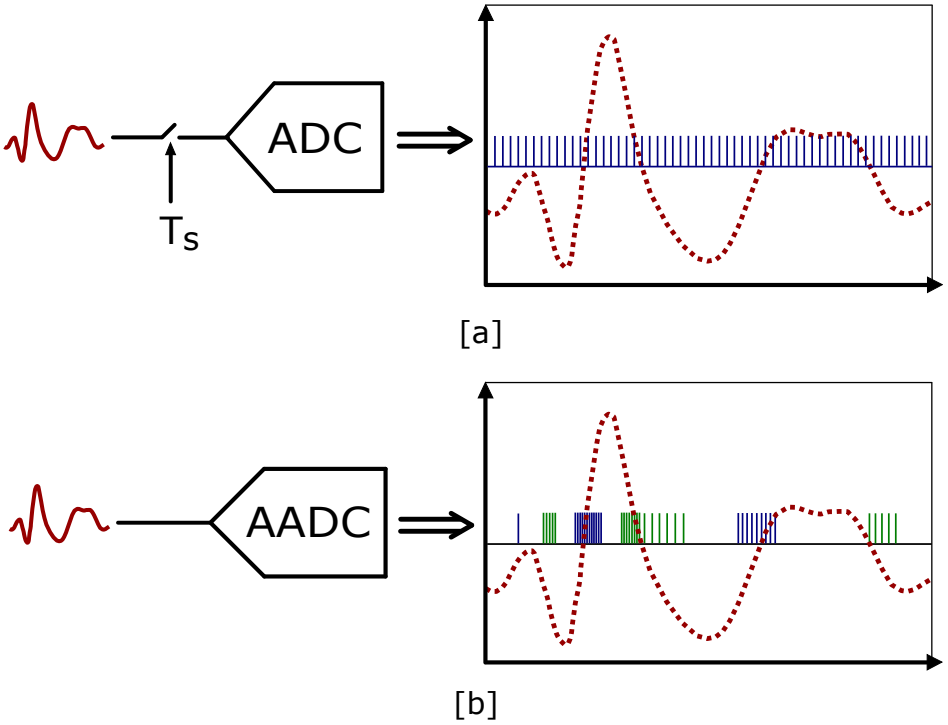


Figure 1.2: Synchronous Vs Asynchronous Sampling schemes a) Uniform sampling in synchronous ADCs at regular intervals of T_s b) Non-uniform sampling at irregular intervals in Asynchronous ADCs

a given time period. For level crossing sampling given in figure 1.2b, samples are only taken when the signal crosses some predefined quantization levels. It can be seen that when the signal remains between two quantization levels, no sample is taken. This results in a fewer number of samples as compared to the nyquist rate sampling, thereby leading to a lower data rate. The level crossing ADC only converts the analogue signal to digital when there are considerable amount of activity on the signal and therefore can be said to be 'event driven'. They tend to have a power consumption profile that resembles the signals activity as opposed to their nyquist rate counterparts that consume relatively constant power throughout. During periods of inactivity, asynchronous ADCs remain idle and do not push any sample into the digital signal processing stage thereby eliminating dynamic power consumption in the digital signal processor (operated in asynchronous mode). In addition, the signal processing stage can be power gated within these idle periods to further minimize power consumption as a results of current leakage. Figure 1.3 shows a conceptual structure of how the power gated digital signal processor can be turned ON/OFF under the control of the incoming asynchronous samples from an asynchronous ADC.

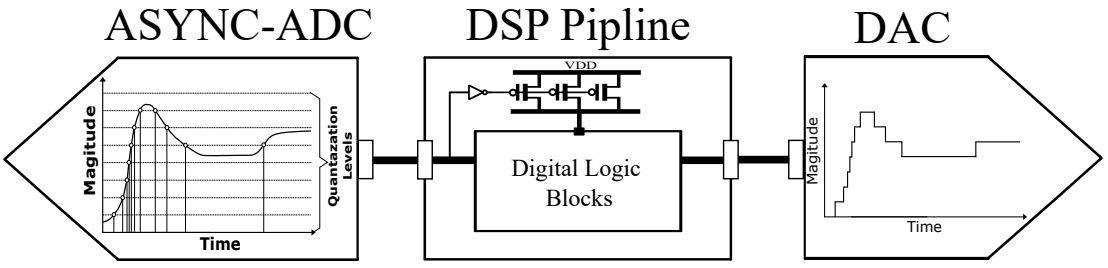


Figure 1.3: Asynchronous signal acquisition and processing pipline. The generation of samples is driven by the number of quantization level crossings made by the input signal and the operation of the DSP pipline is driven by the generated samples.

1.3 Thesis Contribution

The aim of this thesis is to present a power efficient event driven data acquisition and processing system that is capable of adapting its power consumption to the activity profile of the input signal applied. The following contributions were made as a result of this research work:

- An Asynchronous Single Slope Level Crossing ADC architecture was proposed. This new architecture is presented as an alternative to already existing asynchronous ADCs that generate more samples than necessary and introduce some distortion to the resulting signal. This is due to the fact that these ADCs use the crossing of a set voltage level as the actual quantization of the signal. The proposed design addresses this issue by separating the level crossing detection process from the quantization process.

- A burst mode power gated Asynchronous FIR filter capable of processing asynchronous samples obtained from an asynchronous ADC was proposed. The filter was chosen as a case study of a DSP circuit and therefore the technique it utilizes can be adopted for other DSP circuits. This technique for processing these asynchronous samples was put forward as an alternative method to the continuous time digital signal processing that require large delays in each stage of the FIR filter in order to keep track of the timing information between samples. The proposed techniques enables the filter to turn itself off during periods when there is no samples or when the period between two samples is large.

- A test chip consisting of the Single Slope Level Crossing ADC architecture and the Burst mode Power Gated Asynchronous FIR filter was fabricated and used in experimental tests to validate the desired operation of the system.

1.4 Organisation of the thesis

Chapter 2 - Background

This chapter provides an overview of widely used synchronous and asynchronous ADCs, Asynchronous Digital Circuits, Time to Digital Converters and power gating techniques applied on asynchronous circuits. Throughout the chapter, the operations of the mentioned circuits are discussed with their advantages and disadvantages highlighted.

Chapter 3 - Asynchronous Single Slope Level Crossing ADC

This chapter presents a event driven single slope asynchronous ADC that exhibits a power consumption profile resembling the shape of the input signal. This ADC is presented to address

the shortcomings of the currently available asynchronous ADCs that are highlighted in 2.3. The architecture of the proposed ADC is first put forward together with its expected mode of operation. From this, the specifications of the circuit building block are determined and are thereafter used to implement the ADC in a 0.35μm CMOS technology. Finally, the simulated results of the ADC circuit with an audio signal applied at the input is presented to show the ADC's power consumption profile.

Chapter 4 - Event driven burst mode digital signal processing

This chapter presents a brief overview of the difference between discrete time and continuous time digital processing techniques, after which an event driven burst mode signal processing technique is presented. Various implementations of the continuous time signal processing are reviewed and their limitations highlighted. The operation of the burst mode signal processing technique is discussed in details using a digital FIR filter as the subject. The required behaviour of the filter is modelled using timing diagrams which are later on used to implement a control circuit for the filter. The chapter also presents a power gating scheme that is implemented on the event driven burst mode FIR filter to minimize power consumption due to leakage current when there is no sample at the input. The power gating cell design procedure will be presented and the methods of the cell insertion discussed. Finally the chapter will conclude with the description of the physical design procedure undertaken in the implementation of a mixed signal system consisting of the single slope asynchronous ADC and the burst mode FIR filter.

Chapter 5 - Results

In this chapter the measured results of the mixed signal system is presented. A test bench with the ability to measure the dynamic characteristics and power consumption of the system is set up in order to validate the operation of the asynchronous ADC and FIR filter. The measured results are compared to the simulated ones and the differences highlighted. Lastly a summary of the measured results of the ADC will be presented in a table and compared to other asynchronous ones.

Chapter 6 - Conclusion and Future Work

This chapter presents a summary of the contributions made by this work. The benefits of the single slope asynchronous ADC as compared to other asynchronous ADCs is highlighted. In addition to this the power gated event driven burst mode FIR filter is compared to other continuous time asynchronous ADCs and its benefits presented. Finally various ways of improving the design will be presented as part of possible future research work.

Chapter 2

Background

Over the past years device power consumption has been on the rise and is predicted to continue rising as transistor sizes shrink and the frequency of operation increases as given in the 2011 International Technology Roadmap for Semiconductors report [14] and summarised in Figure 2.1. In order to counter the increase in power consumption, various low power design techniques have been put forward and adopted in the design of battery powered portable electronic devices. Techniques such as clock gating and dynamic voltage and frequency scaling have been used to tackle dynamic power consumption while multithreshold design, body biasing and power gating have been used to minimize static power consumption. In recent years, there has been a growing interest in designing mixed signal circuits that adopt their power consumption based on the input signal's activity, i.e the higher the input signals rate of change the higher the power consumption. This behaviour has been made possible by the development of new activity dependent asynchronous analogue to digital conversion and digital signal processing techniques. The purpose of this chapter is therefore to provide a review of power consumption in CMOS circuits, operation of synchronous and asynchronous Analogue to Digital converters as well as static power reduction techniques in asynchronous circuits, with the aim of identifying research opportunities in the design of power efficient activity dependent mixed signal systems.

In the first section of this Chapter, power consumption in CMOS circuits and methods of minimizing it will be presented. In Section 2.2 an overview of the operation of current commercially

available synchronous ADC will be presented with their merits and demerits discussed. Asynchronous ADC will thereafter be presented in section 2.3. This section will begin by a short introduction detailing the difference between synchronous and asynchronous ADC, after which various asynchronous ADC architectures, present in literature, will be reviewed. In Section 2.4 the principle of time to digital conversion will be explored and various time to digital converter architectures suitable for high resolution conversion discussed. The final section of this chapter, section 2.4, will introduce the principles of asynchronous logic design with emphasis on their suitably in implementation of low power designs. In addition to this, the section will also explore the advantages of adopting power gating in asynchronous circuits.

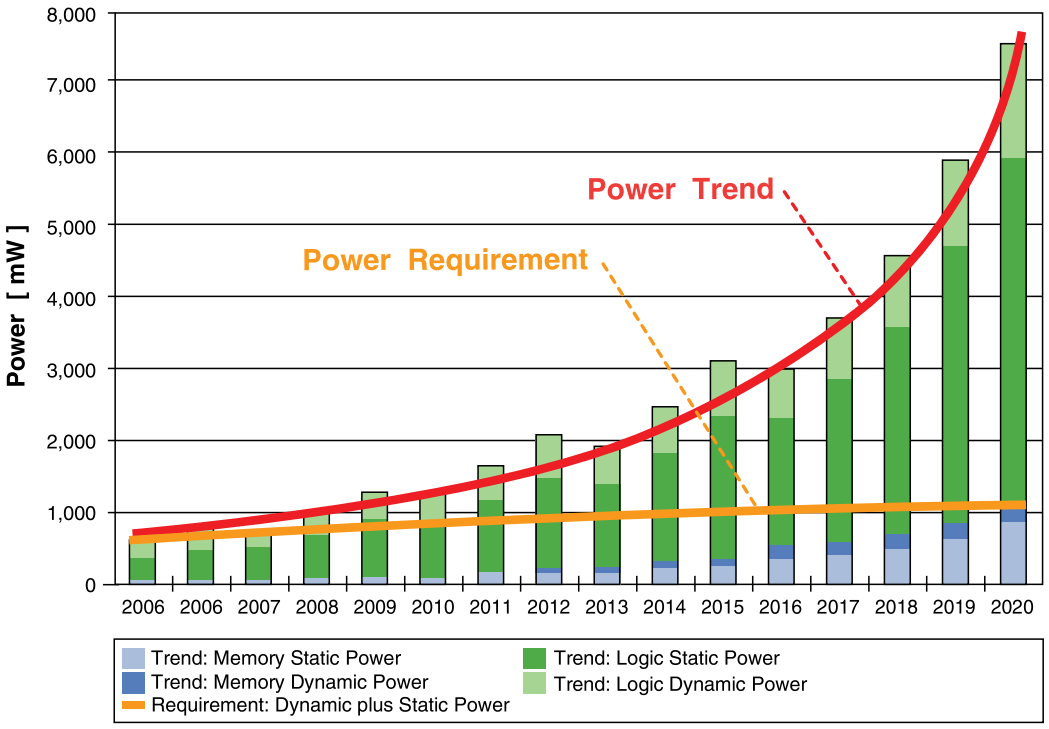


Figure 2.1: IRTS Power Consumption Trend. The Power Trend curve shows the exponential increase in power consumption over the years. The Power Requirement Curve shows the desired power consumption.

2.1 Power Consumption in CMOS circuits

CMOS electronic circuits devices rely on power they obtain from sources such as batteries, solar panels and mains electricity in order to perform their functions. These devices use the electric current obtained from the power supplies in charging and discharging of the inherent capacitance that occur on conduction wires and on the gate of transistors, within the circuits. This form of power consumption is known as dynamic power consumption. Part of the dynamic power consumption, known as short circuit power, is consumed during the short period when a digital logic gate switches from one state to another. In addition to this some of the current obtained from the supply usually flows directly to ground due to the physical properties of the CMOS devices and is referred to us leakage current power consumption. The total power consumed by a device can therefore be summarized by equation 2.1.

$$Total\ Power = P_{switching} + P_{short-circuit} + P_{Leakage}$$

$$Total\ Power = P_{Dynamic} + P_{Leakage} \tag{2.1}$$

2.1.1 Dynamic Power

As mentioned previously, dynamic power is only consumed when there exists switching activity within a circuit. Figures 2.2a to 2.2c illustrates this using the CMOS inverter. When the input of the inverter is connected to ground any positive charge present at the gates of the PMOS and NMOS transistor will be removed. The NMOS transistor will be turned OFF while the PMOS turned ON resulting in the flow of charge from the supply to the load capacitor as shown in figure 2.2a (the capacitor represent the capacitance introduced by the wiring and the gates of the next CMOS circuits). On the other hand, if the input of the inverter is connected to the supply then the gates of the transistors will acquire a positive charge, resulting in the PMOS being turned OFF and the NMOS ON. The charge that was previously transferred to the capacitor will be drawn to ground as shown in figure 2.2b. During the switch over period there exists a short

time where both transistors are on at the same time. This will result in some charge being drawn directly to ground as shown in figure 2.2c.

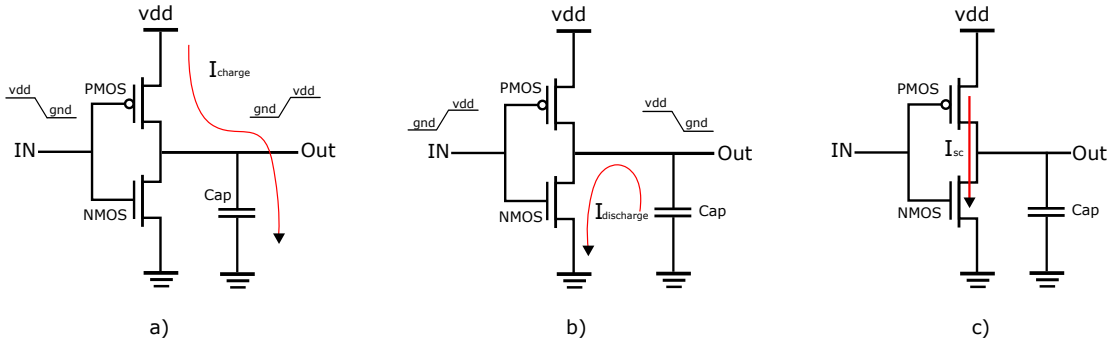


Figure 2.2: Power Consumption in CMOS devices. a) When the inverter's input is low (ground), I_{charge} current charges the capacitor to V_{dd} via PMOS, b) when the input is high (V_{dd}), the capacitor discharges to ground via NMOS, c) when the input is midpoint between V_{dd} and ground, the supply V_{dd} is shorted to ground causing a current of I_{sc} to ground.

Equation 2.2 gives the energy that is drawn from the supply. V_{dd} is the supply voltage, C_L is the load capacitance and V_{out} the capacitor voltage. Half of this energy is dissipated as heat by the PMOS while the other half (equation 2.3) is stored in the capacitor.

$$E_{total} = \int_0^{V_{dd}} V_{dd}\, C_L\, dV_{out} = C_L\, V_{dd}^2 \tag{2.2}$$

$$E_{cap} = \int_0^{V_{dd}} V_{out}\, C_L\, dV_{out} = \frac{1}{2} C_L\, V_{dd}^2 \tag{2.3}$$

For a given number of ON/OFF transitions, N_T, within a single clock cycle, the total switching power consumed is given by equation 2.4; where N_T is the switching activity and f_{clk} is the clock frequency of the circuit. On the other hand, the short circuit power can be given by equation 2.5, where I_{sc} is the short circuit current and t_{sc} is the period the circuit stays in the ON/OFF transition phase. The total dynamic power can therefor be given as the sum of the short circuit power and the switching power as shown in equation 2.6.

$$P_{switching} = N_T V_{dd}^2 C_L f_{clk} \tag{2.4}$$

$$P_{short-circuit} = V_{dd} I_{sc} t_{sc} f_{clk} \tag{2.5}$$

$$P_{dynamic} = N_T V_{dd}^2 C_L f_{clk} + V_{dd} I_{sc} t_{sc} f_{clk} \tag{2.6}$$

2.1.2 Leakage Power

As was shown in figure 2.1 , leakage power has surpassed dynamic power in deep sub-micron technologies. Leakage power is consumed constantly as long as the CMOS circuit is powered on. It occurs as a result of the flow of current to ground due to inherent physical properties of the silicon semiconductor. It is the summation of sub-threshold current leakage, gate oxide leakage, and the diode reverse bias current leakage as shown in equation 2.7.

$$P_{leakage} = V_{dd} \left(I_{sub} + I_{diode} + I_{gate-oxide}\right) \tag{2.7}$$

Where I_{diode} is the diode reverse bias leakage current and $I_{gate-oxide}$ is the gate leakage current and I_{sub} is the subthreshold leakage current.

Gate leakage is the current that flows from the transistor gate through the oxide into the substrate, in the case of NMOS , or from the N-Well through the oxide into the gate in case of the PMOS as shown in figure 2.3. The gate leakage current can be attributed to the direct tunneling of charge carriers through the oxide [15].

The diode reverse bias leakage occurs in the parasitic PN junction diodes formed within the CMOS structure as shown in figure 2.3. The leakage current results due to the high electric field across the reverse biased PN junction that causes tunneling of electrons from the valence band of the p region to the conduction band of the n region (Band to band tunneling) and is a function

of the junction area and doing concentration [16]. Heavier doping results in an increased reverse bias current [16].

Sub-threshold leakage, which dominates the leakage power in CMOS, occurs when a conducting channel made up of minority charge carriers is formed when the NMOS or the PMOS transistor is OFF. It can be calculated by equation 2.8 [17].

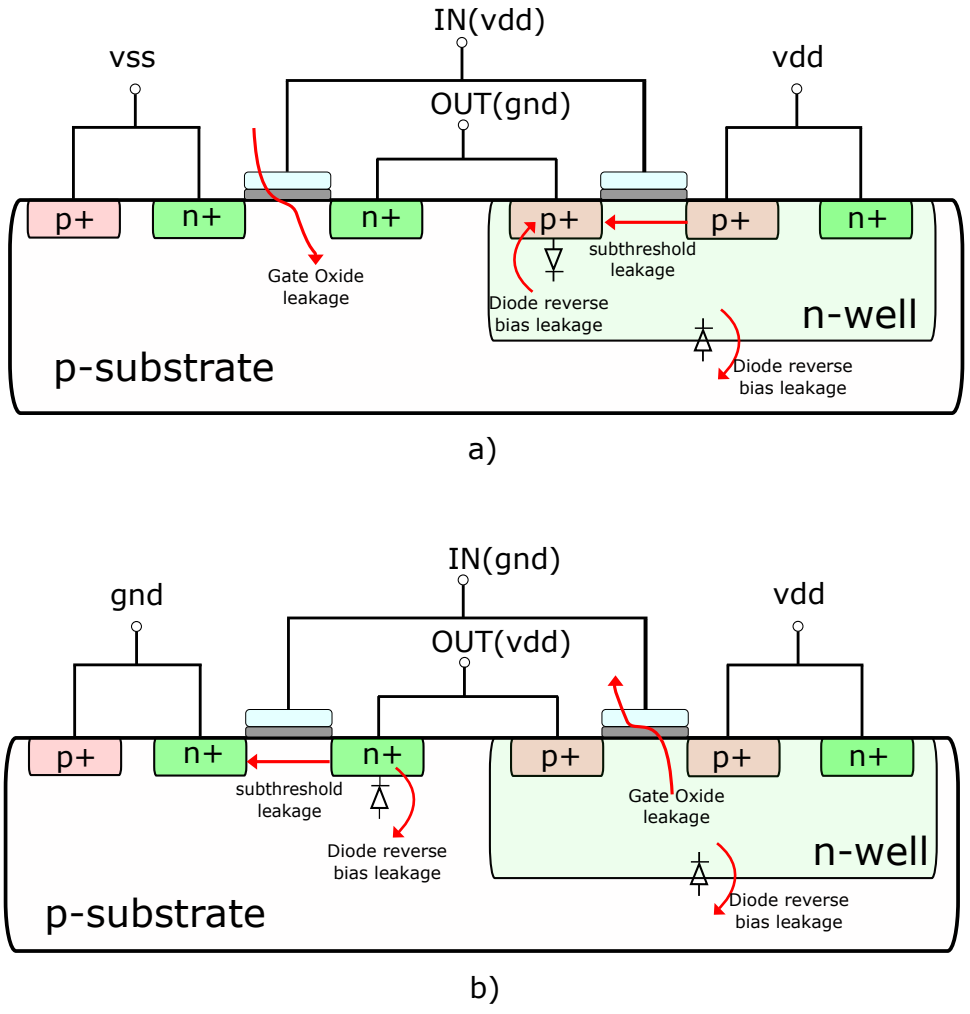


Figure 2.3: CMOS leakage power consumtion **a)** When the input to the inverter is high (Vdd), NMOS is on and PMOS is off resulting in gate leakage in the NMOS transistor. **b)** When input is low, NMOS is off and NMOS is on resulting in gate leakage in PMOS

$$I_{sub} = \mu C_{ox} V_t^2 \frac{W}{L} e^{1.8} e^{\frac{Vgs-Vth}{nVt}} (1 - e^{-\frac{Vds}{Vt}}) \tag{2.8}$$

Where μ is the carrier mobility, C_{ox} is the oxide capacitance, V_t is the thermal voltage, W is the transistor width, L is the transistor length, V_{gs} is the gate to source voltage, V_{ds} is the drain to source voltage, V_{th} is the threshold voltage, n is a function of the fabrication process.

2.2 Synchronous ADC Architecture

Synchronous analogue to digital data conversion is the standard conventional way of data acquisition for analogue signals. The operation of synchronous ADCs involves the sampling of a continuous analogue signal, resulting in an equally spaced sampled discrete time signal which is later on digitized using a quantizer. These ADCs can be divided into two broad categories based on their sampling rates i.e Nyquist Rate ADCs and Oversampling ADCs. The Nyquist rate converters sample the input analogue signal at the Nyquist rate which is two times the frequency of the highest spectral component of the signal. This criteria is based on the Nyquist sampling theorem [9] which states that a bandlimited analogue signal can successfully be reconstructed from its sampled equivalent if it was previously sampled at the Nyquist rate. The input analogue signal is usually passed through a lowpass filter to ensure that any signal that appears above the required baseband bandwidth is removed such that they cannot be aliased back into the baseband frequencies. Oversampling ADCs on the other hand sample the input at a rate much higher than the Nyquist rate. The high sampling rate will in effect spread the quantization noise over a large frequency range thereby lowering the quantization noise power per frequency [18]. The high sampling rate also reduces the steep roll off requirement for the antialiasing filter [19]. Within the broad category of the Nyquist rate and oversampling ADCs, different types of architectural implementations, that will be discussed in this section, can be classified according to their resolution and operating speed as shown in Figure 2.4.

2.2.1 Flash/parallel ADC

The flash ADC, also referred to as the parallel ADC, performs the conversion of an analogue signal by comparing the signal to set voltage references using comparators. The multiple references are usually generated from a single reference voltage through the use of resistors as

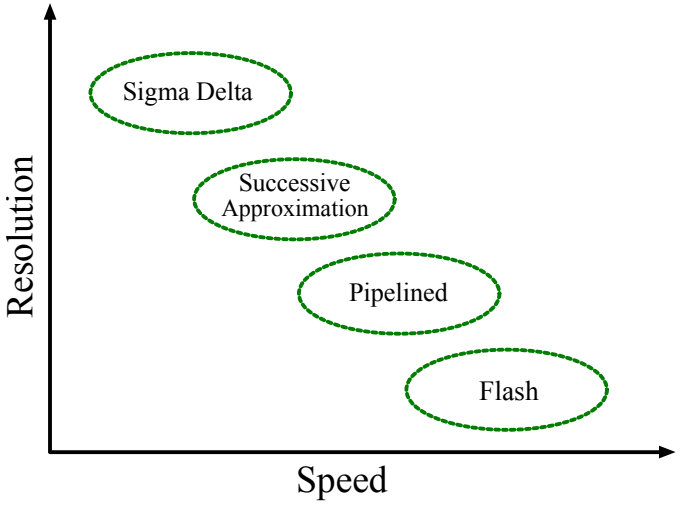


Figure 2.4: ADC classification based on resolution and conversion speed [19].

voltage dividers. In order to achieve an N-bit converter 2^N-1 comparators and 2^N resistors are needed. A 3 bit flash ADC configuration would therefore be configured as shown in Figure 2.5. The reference voltage V_{ref} is divided into 7 reference voltages that are fed to the comparators, with the difference between two adjacent voltage references being equal to the Least Significant Bit (LSB).

Each time the input signal's voltage goes above the voltage at the positive input of a comparator, the comparator outputs a logic '1'. As the input voltage rises the comparators output '1s' in succession and at any given voltage all the comparators with their reference voltages below this value will output '1s' while the ones with reference voltages greater that input voltage will output '0s'. These '0s' and '1s' produce a thermometer code that is fed to a priority encoder for conversion into an N-bit binary number. The comparators can be clocked or a sample and hold circuit placed at the input in order to give timed digital samples for every clock cycle. The flash ADC speed is limited by the sum of the comparator delay and the encoder's delay, which are usually relatively small. This makes the flash ADC the fastest performing ADC. However as the number of bits increases, the number of comparators and resistors increase considerably thereby incurring area and power penalties. This therefore renders the ADC only useful for low resolution applications, below 10 bits [20].

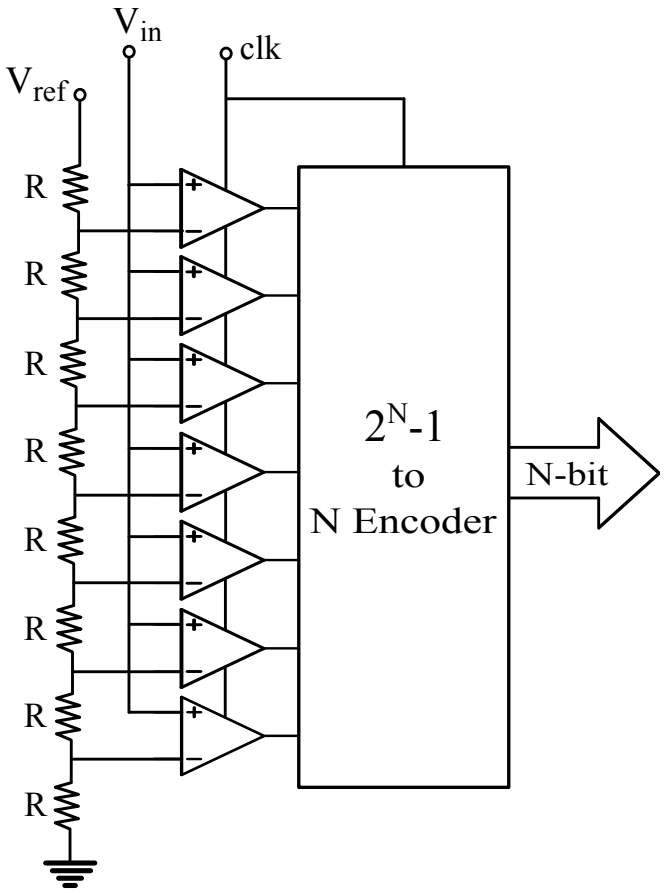


Figure 2.5: A 3 bit Flash ADC. It requires 2^3-1 comparators to compare the input voltage to 2^3-1 voltage references.

2.2.2 Pipeline/subranging ADC

The pipeline ADC architecture utilizes multiple low resolution flash ADCs concatenated together to form successive stages with each giving binary outputs that are later on combined to form the N bit binary output. Figure 2.6 shows a 3 bit implementation of the pipeline ADC based on a single bit flash ADC with each stage consisting of a sample and hold (S/H) circuit, Comparator, 1 bit DAC and an Amplifier. Each stage's operation involves the conversion of the value from the S/H circuit, giving a single bit D_i and a residue obtained from the summation of the S/H value and the one bit DAC. The residue value is amplified by a factor of 2 before being passed on to the succeeding stage.

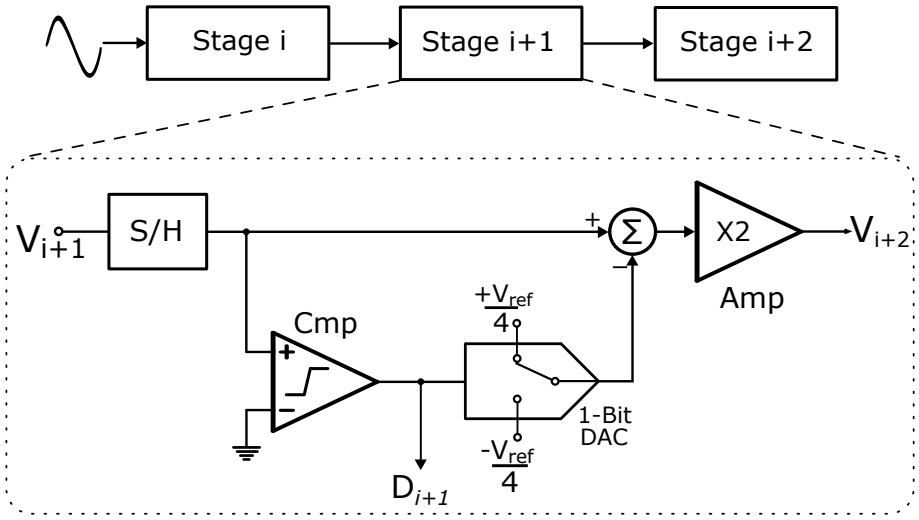


Figure 2.6: A 3bit Pipeline ADC implementaion with a 1bit flash ADC in each pipeline stage.

The implementation given in Figure 2.6 assumes that the input voltage swing is between -V_{ref}/2 and V_{ref}/2. When the input voltage is applied to the first stage, the polarity of the value at the output of the S/H circuit will be detected by the comparator resulting in a 1 given at D_1 if it is positive or 0 if negative. This resulting binary output is fed into the DAC to generate a voltage of -V_{ref}/4 or +V_{ref}/4 at its output. The DAC's output voltage is thereafter added to the S/H value in order to generate a residual value. Since the input voltage swing in the first stage is between -V_{ref}/4 and +$V_{ref}V_{ref}$/4, it is desired that the next stage also receives an input voltage with the same swing. The residual voltage V_{i+1} $\pm Vref/4$ is therefore multiplied by a factor of two such that the maximum and minimum values of the residual voltage fall within -V_{ref}/2 and +V_{ref}/2 as shown in equation 2.9.

$$\frac{-V_{ref}}{2} \leq 2\left(V_i \pm \frac{V_{ref}}{4}\right) \leq \frac{V_{ref}}{2} \tag{2.9}$$

The first conversion output of the pipeline ADC is obtained after N clock cycles after which results will be obtained after every clock cycle. Figure 2.7 shows the residual values at the output of stage i+1 and stage i+2 for a ramp input V_i. It can be seen that the resulting binary output is obtained by finding the polarity of the input voltage and residual voltages at each clock

cycle. The accuracy of the conversion depends on the linearity of the gain amplifier and the digital to analogue converter in each stage.

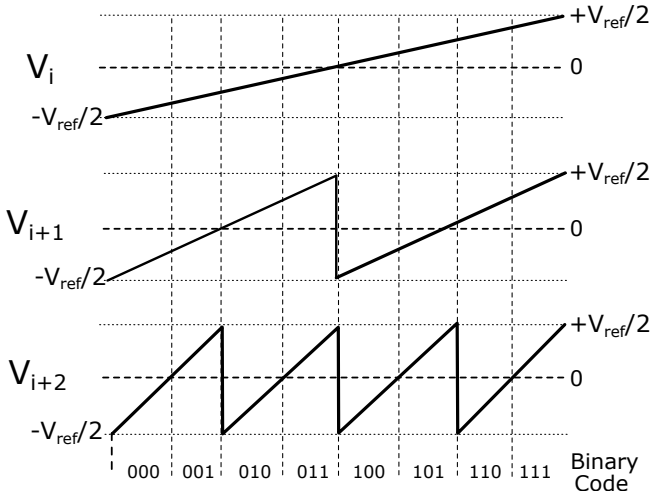


Figure 2.7: Pipeline ADC waveform showing the output of each pipeline stage. Each stage generates a binary 1 when its input voltage is positive and a binary 0 when its voltage is negative.

2.2.3 Successive Approximation Register ADC

The successive approximation ADC is a medium speed ADC that performs the A/D conversion in N amount of clock cycles, where N is the ADC's number of bits. It comprises of a comparator, a digital to analogue converter (DAC) and a Successive Approximation Register (SAR) as shown in Figure 2.8.

At the beginning of each conversion cycle, the analogue input voltage sample obtained from a sample and hold circuit is compared to the previously converted sample (obtained from the DAC) and the results passed on to the SAR logic block. Initially the SAR sets the MSB of the output word to logic '1' and the other bits to logic '0'. The N output bits are passed on to the DAC which generates $0.5V_{ref}$ volts at its output. The voltage is thereafter compared to the analogue input sample. If the input voltage is greater than $0.5V_{ref}$ then the result of the comparison will be logic '1' and the SAR confirms that the MSB is logic '1'. It thereafter moves on to the next lower bit and continue to search for the input voltage value at values greater than

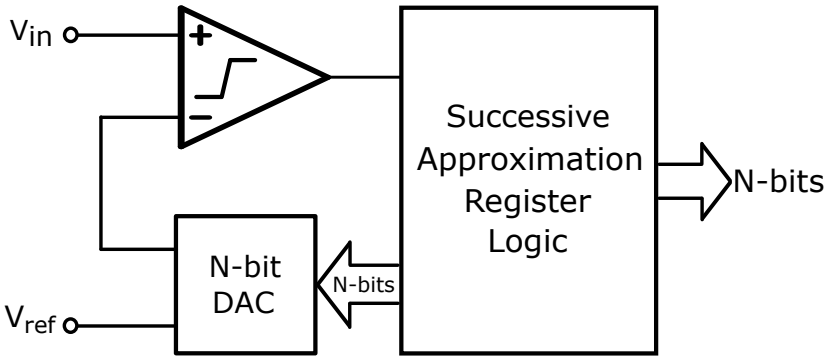


Figure 2.8: SAR ADC. The Successive Approximation Register performs a binary search algorithm while controling the DAC to output the voltage closest to V_{in}.

$0.5V_{ref}$. However if the input voltage is less than $0.5V_{ref}$ then the result of the comparison is a logic '0'. The SAR will confirm that the MSB is not logic '1' and therefore changes it to logic '0'. It will thereafter move on to the next lower bit and continue the search at values less than $0.5V_{ref}$. Assuming a given input sample was above $0.5V_{ref}$ and that the MSB has already been set, the SAR will set the MSB-1 bit to logic '1'. This will update the DAC's output to $0.75V_{ref}$. If the input value is greater than $0.75V_{ref}$ then the comparator's output remains at logic '1' and the SAR confirms that the MSB-1 bit is logic '1'. If it's less than $0.75V_{ref}$ MSB-1 will be set to logic '0'. This process of continuous approximation of the bit values is continued until all the N-bits values are confirmed as shown in Figure 2.9, thereby giving the digital word which represents the analogue input.

Since the SAR ADC utilizes a multi bit DAC, its accuracy and resolution will be limited to how well the capacitors (for a charge redistribution DAC) or resistors (for a R2R resistor ladder DAC) are matched. The maximum resolution possible without error correction circuitry is 10bit as reported in [21].

2.2.4 Single Slope ADC

The single slope ADC also known as the integrating ADC performs the analogue to digital conversion by comparing a ramping voltage to the input signal. The ramp voltage generation begins when a reference voltage is applied to the integrator's input. As the ramp rises at the

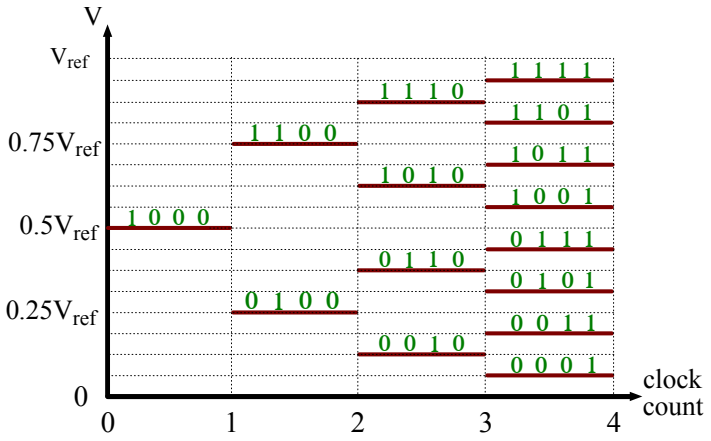


Figure 2.9: Successive Approximation Register binary search algorithm for a 4 bit SAR ADC. The MSB is resolved in the 1^{st} clock cycle while the LSB in the 4^{th} cycle.

integrator's output, the time taken for its voltage to equal the input signal's voltage is encoded into a pulse width modulated signal by the comparator. The time encoded pulse is thereafter passed to the counter as an enable signal which allows it to count to a digital value representing the time information. The operation of the ADC is controlled by a digital logic block, as shown in figure 2.10, that resets the integrator after a set amount of clock cycles elapse. This time, which represents the ADC's conversion time, should be enough to ensure that the counter can count up to the highest possible value that represents the full scale analogue input. For a clock period of T_s, the conversion time for an N bit single slope ADC is given by the product of the clock period T and the value of the full scale count 2^N.

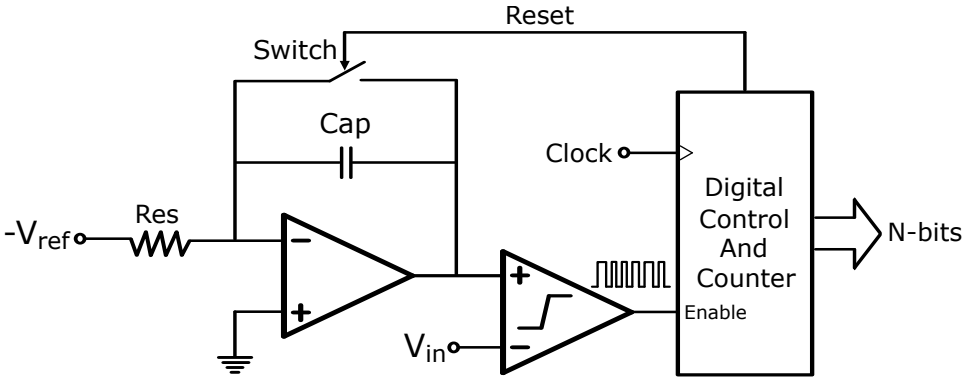


Figure 2.10: Single Slope ADC. A ramping voltage is compared to the input signal V_{in} and the time it takes for the 2 voltages to equal each other is recorded.

The major drawback of this architecture is that the accuracy of its conversion depends on the accuracy of the ramp generator. Since the ramp generator depends on the accuracy of the resistor and capacitor values, a small change in them will result in a significant shift in the ramp voltage gradient.

2.2.5 Dual Slope ADCs

The Dual Slope ADC was put forward as an improvement to the single slope ADC. It is designed to alleviate the dependence of the single slope ADC's accuracy to the changes in the resistor and capacitor values. Instead of having one ramp slope as the single slope one, it has two. This is achieved by integrating the analogue input signal in one polarity direction then integrating a reference voltage in the opposite polarity direction. Figure 2.11 shows the dual slope architecture configuration. Initially switches S_1, S_2 and S_3 are open. The digital controller will give a pulse to reset the integrator's output V_{int} = 0V by closing switch S_3.

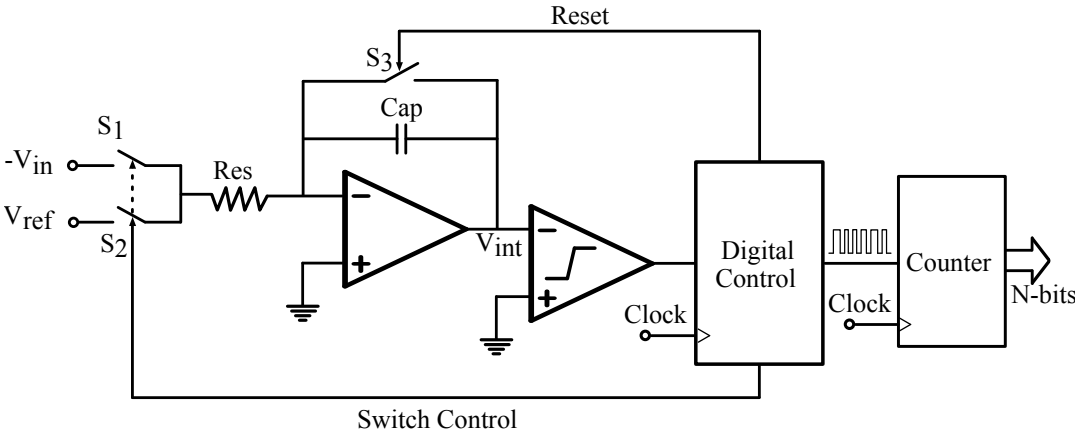


Figure 2.11: Dual Slope ADC. V_{in} is used to charge a capacitor via the integrator for a fixed period T_1 and $Vref$ is used to fully discharge the capacitor for the period T_2. The ratio of Vin/Vref will be equal to the ratio T_2/T_2.

The conversion is performed in two phases. In the first phase switch S_1 is closed and V_{int} begins to ramp up in the positive direction with a slope determined by V_{in}/RC. The ramp is in the positive direction since the analogue input voltage V_{in} (from a sample and hold circuit) is given as a negative value. Switch S_1 is kept closed for a time period T_1 which is the time taken to

count the number of clock cycles elapsed until the highest possible digital output value of the ADC (2^N for an N-bit converter) is reached. At the end of this period, a final voltage V_{peak} = -$V_{in}T_1$/RC is held at V_{int} as shown in figure 2.12. In the second phase, S_1 is opened and S_2 closed. The voltage V_{int} begins to ramp down from V_{peak} with a constant slope given by V_{ref}/RC. At the same time the counter is initialized and begins to count the number of clock cycles. When the V_{int} reaches 0V after a time period of T_2, the comparator gives a logic high output to the controller which indicates the end of conversion. At this point the counter is disabled and the results made available. For the ramp up phase, V_{peak} can be obtained as given in equation 2.10 and for the ramp down phase, equation 2.11.

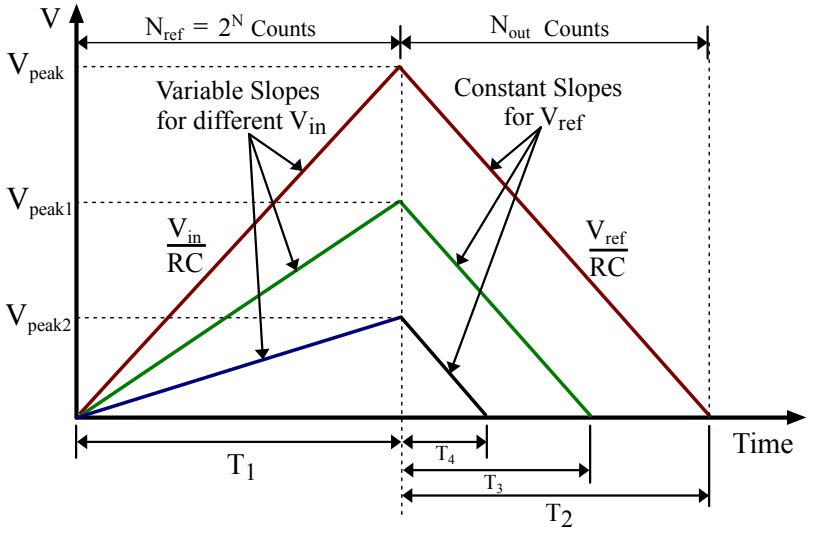


Figure 2.12: Dual Slope ADC timing diagram. The capacitor's voltage rises from 0 to Vpeak with the gradient Vin/RC for the period T_1 and falls from Vpeak to zero

$$V_{peak} = V_{int(T_1)} = \frac{1}{RC}\int_0^{T_1} -V_{in}\mathrm{d}x + V_{int(0)} = \frac{-V_{in}T_1}{RC} \tag{2.10}$$

$$V_{peak} = \frac{-V_{in}T_1}{RC}$$

$$V_{int(T_1+T_2)} = \frac{1}{RC}\int_{T_1}^{T_1+T_2} V_{ref}\mathrm{d}t + V_{peak} = \frac{V_{ref}T_2}{RC} + V_{peak} = 0 \tag{2.11}$$

$$V_{peak} = \frac{-V_{ref}T_2}{RC}$$

$$\therefore \frac{-V_{in}T_1}{RC} = \frac{-V_{ref}T_2}{RC} \Rightarrow \frac{V_{in}}{V_{ref}} = \frac{T_2}{T_1} \tag{2.12}$$

$$\frac{V_{in}N_{ref}}{V_{ref}} = N_{out} \tag{2.13}$$

Combining the two equations as shown in equation 2.12 gives us the relationship between V_{in}, V_{ref}, T_1 and T_2. The ratio of a constant Vin sample to V_{ref} is equal to the ratio of the ramp down time to the ramp up time. Since the full scale count N_{ref} during the period T_1 is performed using the same clock as the one used for count N_{out} during the period T_2, equation 2.12 can be rewritten as given in equation 2.13. From the resulting relationship it can be seen that the output N_{out} of the dual slope ADC is independent of the slopes of the ramp and therefore is not affected by small variations in the values of the capacitor and resistor. The main disadvantage with the dual slope ADC is that it requires a conversion time which is two times the period of the full scale count i.e $2(2^N\ T_{clk})$, where T_{clk} is the clock period and N the ADC number of bits.

2.2.6 Charge Rundown ADC

The charge rundown ADC shares some similarity to the single slope ADC as it relies on a single slope negative gradient ramp obtained by discharging a capacitor through a constant current source to perform the A/D conversion. It consists of a capacitor, comparator, counter and a digital logic controller as shown in figure 2.13.

The first phase of the conversion process begins when sampling the analogue input voltage onto the capacitor by closing switch S_1 while leaving S_2 open. On the second phase S_2 is now closed while S_1 is opened. The counter is enabled during the second phase of conversion and it counts the time it takes to discharge the capacitor through the constant current source I_{dch}. The end of

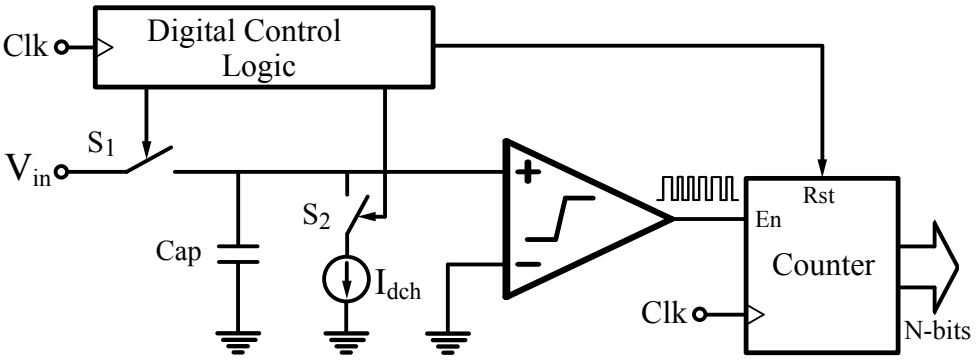


Figure 2.13: Charge Rundown ADC. Capacitor Cap is discharged through I_{dch} and the time it takes it to fully discharge is recorded

conversion is reached once the capacitor is fully discharged and the results made available at the outputs of the counter. Since the accuracy of the charge rundown ADC depends on the accuracy of the constant current source and the value of the capacitor, any deviation from there design values due to process and voltage variations will affect the ADC's accuracy.

2.2.7 Sigma Delta ADC

The previously discussed ADCs operate by directly quantizing the analogue signal's amplitude at a Nyquist rate i.e at a rate that is at least two times the frequency of the highest expected spectral component of the signal. They are usually relatively fast in their conversion speed but are unable to achieve high resolution. This is because as voltage is continuously being scaled down in submicron technologies, the LSB becomes very small and therefore the ability of circuits to resolve it is highly impacted by mismatches in analogue circuit building blocks as well as process and voltage variations [19]. The sigma delta ADC on the other hand is an oversampling type of ADC that operates at a sampling rate much higher than the Nyquist rate. Its sampling rate is usually an integer multiple of the Nyquist rate and the ratio of the oversampling rate to the nyquist rate is known as the oversampling ratio. The high sampling rate of oversampling ADCs allow for the relaxation of the antialiasing filter requirements. The antialiasing filter is usually designed such that the frequency at the beginning of its stopband lies around half the Nyquist sampling rate frequency ($0.5f_S$) as shown in figure 2.14.

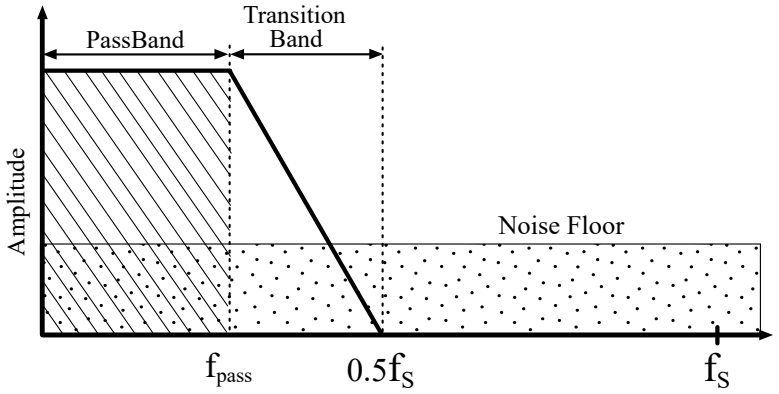


Figure 2.14: Frequency response of antialiasing filter showing the desired begining location of the stop band, which is half the value of the sampling frequency $0.5f_S$.

This ensures that all the unwanted signals between $0.5f_S$ and f_S are removed so that they cannot be aliased back into the passband frequencies. It is therefore evident that in order to place the stopband frequency at $0.5f_S$, a filter with a steep roll off is required unless the sampling frequency is increased as in oversampling ADCs. Figure 2.15 shows the frequency of an anti aliasing filter for an oversampling ADC. It can be seen that now the beginning of the stop band occurs at $0.5Kf_S$, where K is the oversampling ratio. This will allow for the use of a low order antialiasing filter.

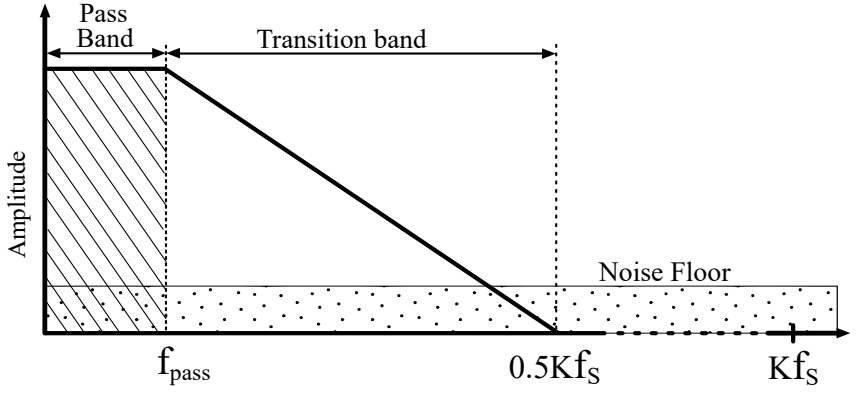


Figure 2.15: Frequency response for an antialiasing filter of an oversampled ADC. A low order filter can be used to realize the filter since the begining of the stopband is now moved to $0.5Kf_S$

A first order sigma delta ADC architecture consists of an analogue frontend referred to as the sigma delta modulator and a digital signal processor backend as shown in figure 2.16. The

analogue frontend is implemented as a feedback loop consisting of an integrator, comparator and a single bit DAC.

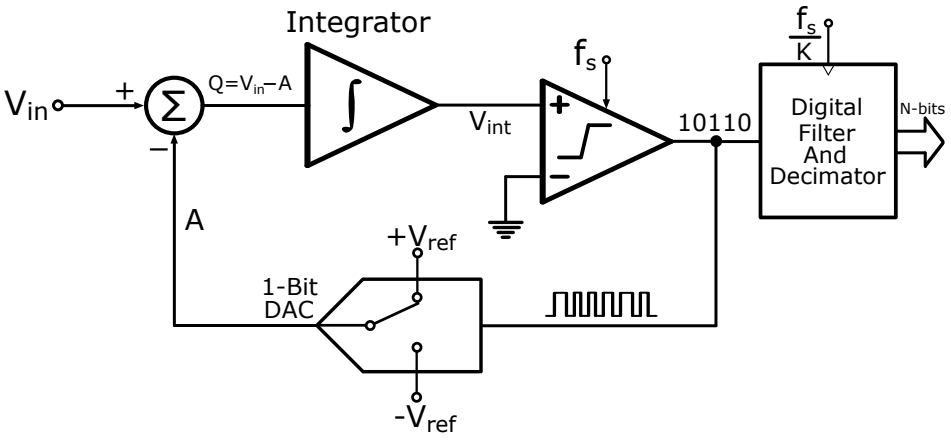


Figure 2.16: First Order Sigma Delta ADC Architecture

When the voltage at the output of the integrator V_{int} increases in the positive direction the output of the comparator will go high when the clock is applied. This will in turn cause the DAC to produce a positive reference voltage $+V_{ref}$ at its output (point A). This reference voltage is thereafter subtracted from the input voltage V_{in} and the results at point Q passed on to the integrator. Since the $+V_{ref}$ is chosen to be equal to the maximum positive peak of V_{in}, the results at point Q (quantization error) will be positive. This will result in the integrator pulling V_{int} in the negative direction. The feedback loop will continuously add and accumulate the quantization error every clock period further pulling down V_{int} until it goes below 0V. The comparator will pull its output low resulting in point A being pulled down to $-V_{ref}$. The quantization error at Q will become positive and continuously be accumulated by the integrator until V_{int} rises above 0V. Figure 2.17 shows a switched capacitor implementation of the modulator. The integrator is implemented using an operational transconductance amplifier, capacitors and switches. During the clock phase ϕ_1, C_1 is charged to V_{in}. In the next clock phase ϕ_2, the DAC output is connected to C_1 resulting in the summation of V_{in} (sampled during ϕ_1) and the voltage at the DAC output, which is integrated into C_2 via the OTA.

This action of accumulating the error in the positive and negative directions will continue as the sigma delta modulator tries to minimize the quantization error by making the local average

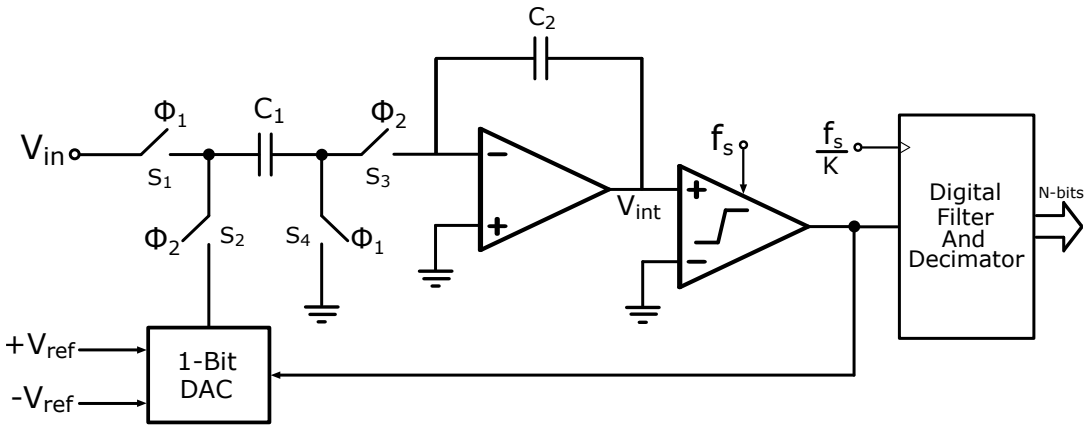


Figure 2.17: 1^{st} Order Sigma Delta Modulator switched capacitor implementation

voltage at point A equal to the local voltage of V_{in}. The resulting bit stream is passed on to the digital filter that averages out a given number of bits per sample. Figure 2.18 shows the resulting bit stream at the comparators output when the input voltage V_{in} is positive. Assuming the averaging digital filter is of order 8, the resulting average value will be the sum of the 8 bits divided by 8 i.e 6/8. This means that the LSB is given by 1/8 and the resolution of the ADC is 3bits. As the filter order is increased, more bits are averaged resulting in a higher dynamic range.

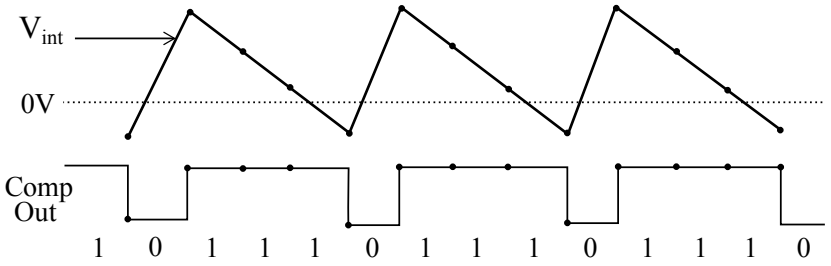


Figure 2.18: Integrator and comparator output of the sigma delta modulator.

This property of the Sigma Delta ADC enables it to rely on digital signal processing to obtain high levels of resolution rather than relying on accurate quantization of the analogue signal's amplitude in the analogue circuitry. In addition to this, the sigma delta ADC has the ability to shift the quantization noise from the lower frequencies of interest to higher frequencies in a

process referred to as noise shaping. Figure 2.19 shows a linearised model of the sigma delta modulator that shows how the quantization noise is shaped.

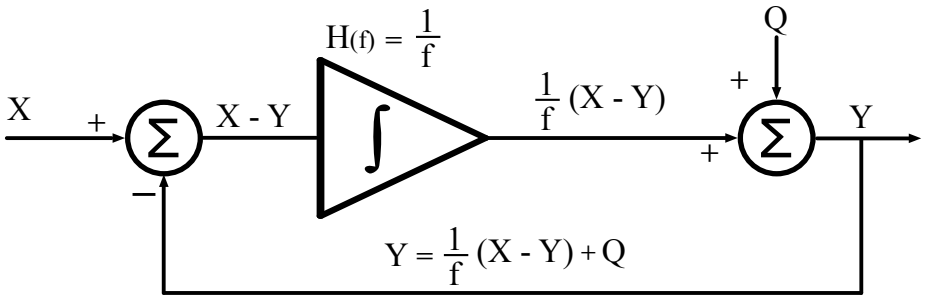


Figure 2.19: A linearised model of the Sigma Delta modulator

$$Y = \frac{1}{f}(X - Y) + Q \tag{2.14}$$

$$Y = \frac{X}{f+1} + \frac{Qf}{f+1} \tag{2.15}$$

The integrator with the transfer function of $H_{(f)}$=1/f operates on the value X-Y and gives a resulting value of 1/f(X-Y) at its output. The quantization noise Q is added to the results yielding equation 2.14 that is further rearranged as shown in equation 2.15. It can be seen that as the frequency reduces towards zero the noise term Q.f/(f+1) is minimized and the signal term X/(f+1) dominates. On the other hand, as frequency increases the signal term becomes small and the noise term dominates. This results in lowering of the noise floor in the passband as illustrated in figure 2.20. The quantization noise that has been shifted to higher frequencies can now be easily removed using a digital low pass filter.

2.3 Asynchronous ADCs Architectures

As is evident in the discussions in the previous chapter, a constant sampling rate is exhibited by all synchronous A-D converters currently available. With the constant sampling rate, they produce the resulting digital bits at a constant data rate and they generally exhibit a fairly constant

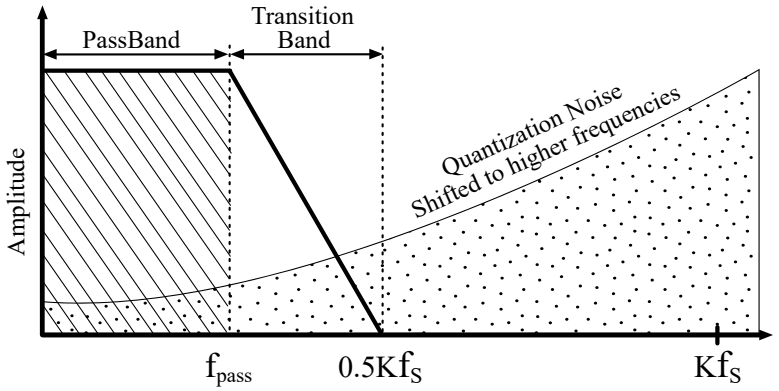


Figure 2.20: Frequency response of the sigma delta modulator showing the attenuation of the quantization noise in the passband.

power consumption profile regardless of the input signal. These properties render synchronous A-D converters less suitable for conversion of sparse, bursty and intermittent signals such us Electrocardiogram (ECG) and Electroencephalogram (EEG) signals [1] [3].

Asynchronous A-D converters on the other hand do not exhibit a constant sampling rate but rather sample the input signal intermittently and at irregular periods as was discussed in section 1.2. These A-D converters rely on the level-crossing sampling scheme whereby a signal is only sampled when its voltage goes above a predetermined reference voltage level. The main advantage of the level crossing asynchronous ADC over synchronous A-D converters is that, due to the fact that they obtain samples only when the input signal increases or decreases across a given threshold, they will exhibit a sampling profile similar to the signal profile, i.e signals with low frequency and low amplitude are sampled less densely in time compared to high frequency and high amplitude signal [22]. This will in effect result in overall lower power consumption as compared to if sampling is done constantly.

The Level crossing A-D converters can be classified under two main categories i.e Floating Window Level Crossing ADC (the reference voltage level is updated each time the signal changes) and Fixed Window Level Crossing ADC (the reference voltage level is remains constant even if the signal changes). In this section these two types of asynchronous level crossing A-D converters available in literature will be presented and their advantages and disadvantages discussed.

2.3.1 Floating Window Level Crossing ADC

The Level Crossing ADC performs its analogue to digital conversion asynchronously in continuous time, i.e instead of generating samples at equal time intervals, it only generates samples once a set threshold voltage is crossed and hence the name "level crossing". It can generally be implemented either as a parallel converter or serial converter. Its parallel implementation presented in [23], [24] and [25] is similar to that of the flash ADC but with the use of continuous time comparators rather than clocked comparators. It suffers the same problem of increased area and power consumption as the flash ADC when a higher number of bits is required. In the serial implementation [26], only two comparators are used as shown in figure 2.21. Together with the two DACs the comparators form a voltage window which is equal to the LSB of the ADC.

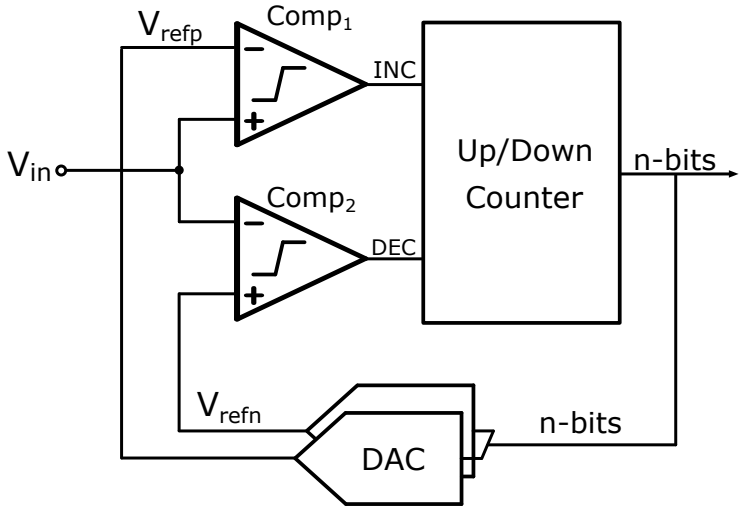


Figure 2.21: Tracking Window Level Crossing ADC. V_{in} is compared to a voltage boundary set by V_{refn} and V_{refp}.

The voltage window upper and lower boundaries are set by the reference voltages V_{refp} and V_{refn} respectively. When the analogue voltage V_{in} is applied, the comparators determine whether the input signal level is within the voltage window by comparing it to V_{refp} and V_{refn}. If the voltage is greater than V_{refp}, the increment signal INC is generated and if it is below V_{refn} the decrement signal DEC is generated. These signals will in turn increment or decrement the counter accordingly by a value of one LSB. The digital output from the counter are thereafter fed back to the DAC to generate new values of V_{refp} and V_{refn} resulting in a new voltage window

which is now either 1 LSB above or below the previous one. However if the input voltage remains constant within the voltage window then no samples will be generated as shown in figure 2.22.

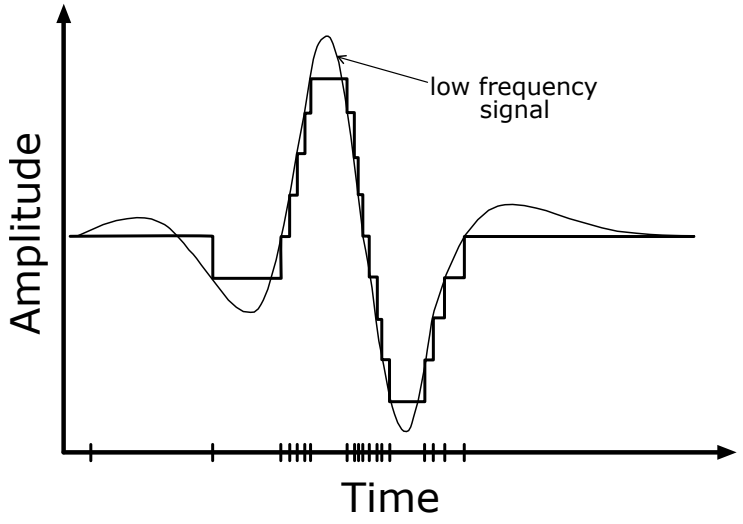


Figure 2.22: Tracking Window Level Crossing A-D conversion of a low frequency signal.

The rate at which the level crossing ADC generates samples per unit time is determined by the slope of the input signal, the value of the voltage window (LSB voltage) and the time it takes to evaluate a single sample (loop delay). Fast rising signals results in generation of more sample than slow rising signals. On the other hand the smaller the voltage window the higher the number of samples. It is therefore evident that for a small voltage window and high frequency signals the ADC will produce a lot of unnecessary samples. For a particular signal the generation of lots of samples during periods of fast signal change might consume more power than the amount of power saved during periods of inactivity. This is contrary to the desired operation of the level crossing ADC, which is to minimize power consumption by minimizing the number of generated samples. In addition to this, if the signals frequency is high such that the time it takes for the signal to move from one voltage window to the next is less than the loop delay then the quantization process will not be able to keep up with the signal rate of change. This will result in a "slew rate limited" like behaviour known as slope overload [27] that introduces distortion in the converted signal as shown in figure 2.23. The ADC should therefore be designed to ensure

that the magnitude of the rate of change of V_{in} is always less than the conversion rate of the ADC as shown in equation 2.16.

$$\frac{dV_{in}}{dt} < \frac{V_{LSB}}{loopdelay} \tag{2.16}$$

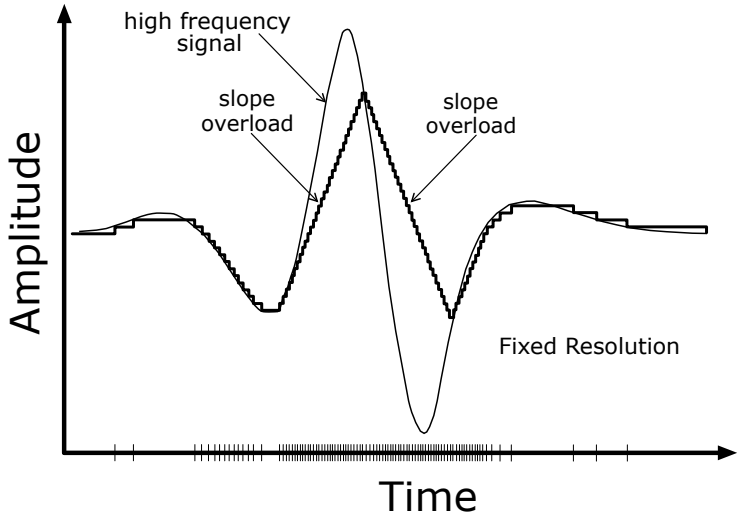


Figure 2.23: Tracking Window Level Crossing A-D conversion of a high frequency signal. The ADC suffers from slope overload since it's conversion speed cannot keep up with the high rate of change of the signal.

Since the Level crossing ADC generates lots of samples for fast changing signals, a trade-off between the ADC's bandwidth and its resolution should be considered during design i.e if a wide bandwidth is required then the resolution should be lowered and if a high resolution is required then the bandwidth should be narrowed. In order to avoid making the trade-off between bandwidth and resolution, improvements to the level crossing ADC have been made as described in [27], [11], [28] to allow it to be able to vary its resolution. For high frequency fast changing signals, the resolution is reduced by increasing the LSB voltage while for low frequency signals the resolution is increased. This has a net effect of maintaining the number of samples produced for both high frequency and low frequency signals. It also ensures that the overload distortion does not arise since an increase in dV_{in}/dt is countered by an increase in V_{LSB} , therefore maintaining the validity of equation 2.16. This improvement, shown in figure 2.24, referred to as adaptive

resolution control is implemented by using algorithms that detect the slope of the signal and adjust the voltage window as required.

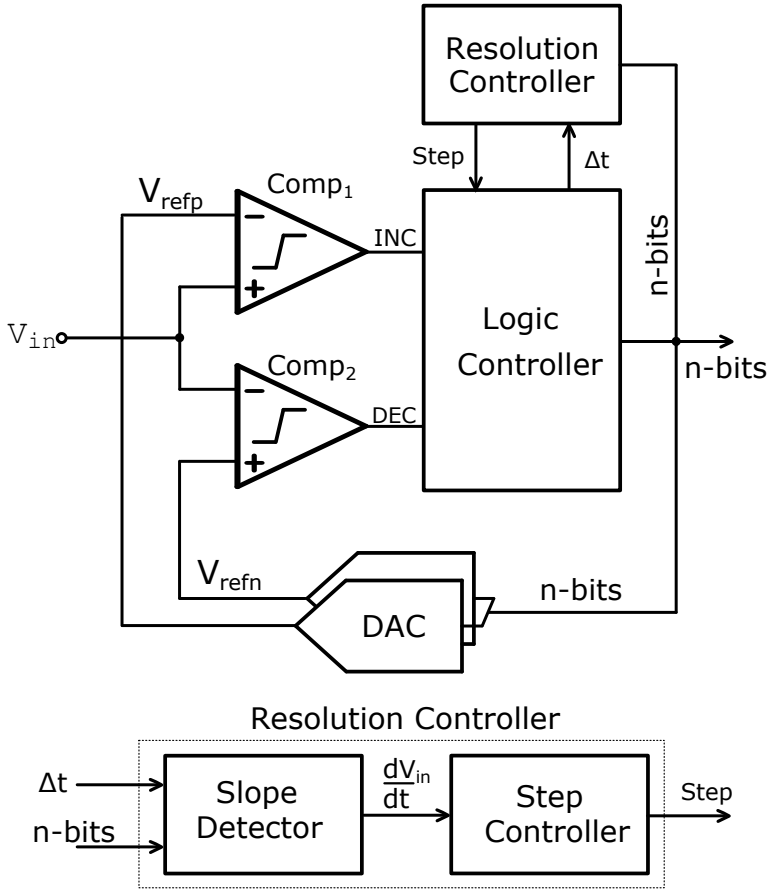


Figure 2.24: Tracking Window Level Crossing ADC with adaptive resolution control. The voltage window is continously being increased or decreased based on the rate of change of V_{IN}.

Initially a given lower value of the voltage window is set and a timer initialized to measure the time difference between two adjacent samples. If the resulting time is greater than a pre-set timing boundary then the voltage window is maintained. When the input signal's slope increases then the time between the new samples will be reduced. If this time goes below the set timing boundary then the voltage window will be increased by a predetermined value thereby reducing the resolution. A reduction in the signal slope will result in increased time between samples and thereby the resolution will be increased. The result of adaptive resolution can be seen in figure 2.25, showing the sampled waveform with no slope overload.

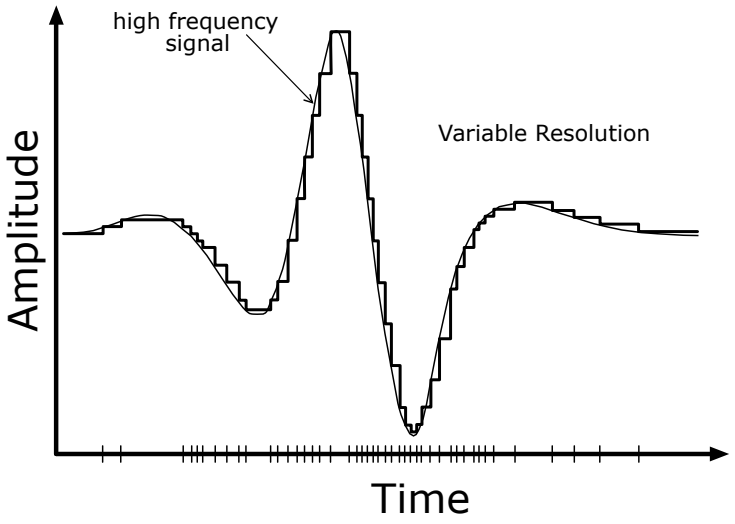


Figure 2.25: Tracking Window Level Crossing A-D conversion with adaptive resolution control. The ADC changes its resolution from high to low at steep sections of the signal and from low to high at less steep sections.

It is worth noting that the quantization noise of the adaptive resolution ADC will vary dynamically with the increase and decrease of the LSB voltage. When the resolution is decreased the quantization noise power increases. This might pose a problem to small amplitude fast changing signals that might be present within the baseband frequencies. It is therefore necessary to utilize an algorithm, as presented in [11], [28], that dynamically changes the voltage window as both a function of the input signal's rate of change as well as its amplitude. In addition to this problem the ADC implementation as presented in [27], [11], [28] and [29] require the use of at least two DACs that are able to vary the voltage window position throughout the desired full scale range. These DACs are usually implemented as current steering DACs as opposed to charge scaling DACs and therefore incurs additional area and power penalties. The charge scaling DACs is not used because in cases where the input signal is not changing over long periods of time, the leakage current through the capacitors in the charge scaling DAC will result in drifting of the output value over time thereby changing the position of the voltage window.

2.3.2 Fixed window Level Crossing ADC

The fixed window Level crossing ADC architecture was put across in order to eliminate the use of the DACs present in the tracking window level crossing ADC. Instead of dynamically updating the voltage window across the whole full scale range, a fixed voltage window is used throughout the full scale range. It operates by generating samples when the value of dV_{in}/dt surpasses set threshold voltages as opposed to the tracking window architecture where the samples are generated when the amplitude of signal goes above a voltage window. Since the voltage window is fixed, the value of dV_{in}/dt has to be reset to its original value after a sample is acquired. The resulting samples are presented as pulses that are counted to give the digital value. Figure 2.26 shows an implementation of the fixed window level crossing ADC as presented in [30].

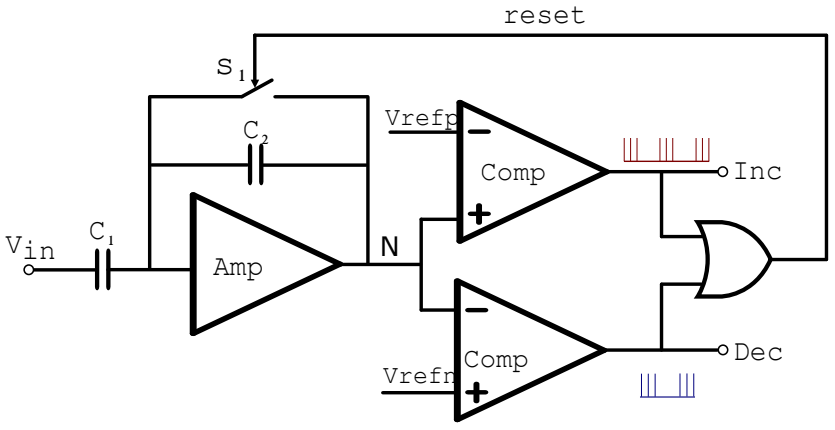


Figure 2.26: Fixed Window Level Crossing ADC. The change in V_{in} is compared to a fixed voltage bondary set by V_{refn} and V_{refp}.

The amplifier together with capacitors C_1 and C_2 perform a derivative function on V_{in} giving dV_{in}/dt at node N. The comparators compare the result to the voltage window boundary references V_{refp} and V_{refn}. If the analogue signal is rising and the voltage at node N rises above V_{refp}, then the increment signal INC is raised high. If the analogue signal is falling and node N (initially at midpoint between V_{refp} and V_{refn}) falls below V_{refn} then the decrement signal DEC is raised high. The generation of either the INC or DEC signal will inturn increment or decrement the counter as well as reset the amplifier circuit via switch S1. There exists a slight delay from the time the comparators are triggered to the time the reset process begins. During

this period the signal rise at node N cannot be detected and will not form part of the count value. In addition to this there is a delay during the period when the amplifier's output at node N is reset to the mid point value and also the delay in pulling down of the INC/DEC signal. During this period the amplifier cannot track the analogue signal change and therefore the signal change will not be part of the count value. Over time the accumulation of the signal loss due to the sum of these delays (loop delay), during successive reset periods, will significantly distort the signal resulting in gain error as shown in figure 2.27.

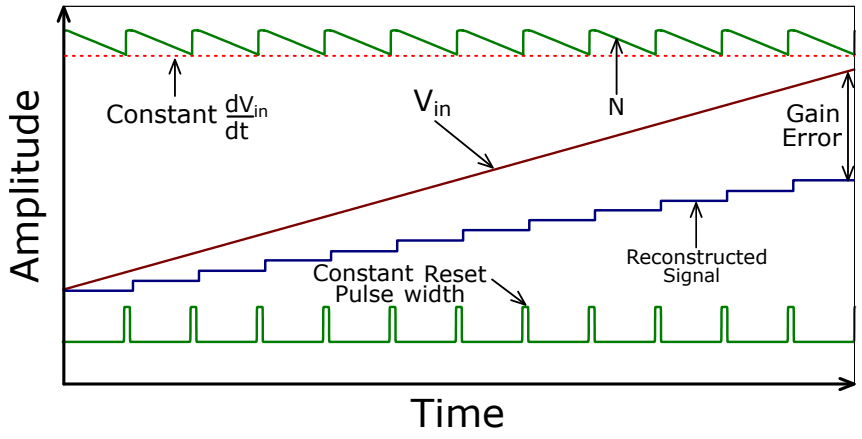


Figure 2.27: Fixed Window Level Crossing ADC gain error when a linear rising input is applied.

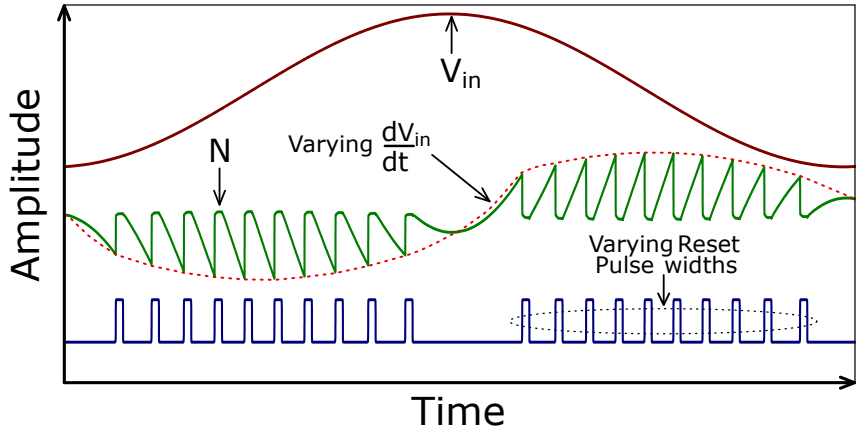


Figure 2.28: Fixed Window Level Crossing ADC output waveform with sinusoidal input

For a constant slope signal the value of dV_{in}/dt at node N remains constant for each tracking

cycle. This results in a constant gain error that can easily be removed during digital post processing. However if a signal with varying slopes such as a sine wave is applied as in figure 2.28 , the value at node N will also vary as shown in figure. This is because a fast rising signal will transfer more charge onto capacitor C_2 than a slow rising signal. The delay time for each reset cycle will therefore also vary since the amplifier response time varies with the voltage at node N. Due to this effect, the resulting gain error will be a function of the signal's slope. This will make the process of removing the gain error complicated as it has to be estimated after each sample and thereafter using the estimate to extrapolate the succeeding sample as presented in [30]. The distortion due to the constantly changing gain error will severely limit the ADC's dynamic range.

2.3.3 Fixed window Level Crossing ADC with DAC feedback

The operation of this type of asynchronous ADC, presented in [13], closely resembles that of the one discussed in section 2.3.2 as they both rely on a fixed voltage window to determine how much the input signal has changed. The major difference between the two types is that this implementation has memory of the previous sample and uses it to evaluates the next sample as opposed to the one in section 2.3.2 that does not rely on the value of the previous sample to generate the next sample. Another important difference is that in this variant the detection of a level crossing is determined by one comparator as opposed to two as was done in 2.3.2. This is achieved by swapping the inputs to the window comparison comparator depending on whether a signal is rising or falling. Figure 2.29 shows an input signal that rises/falls consecutively passed various voltage levels. When the signal increases/decreases monotonically, the level crossing mode is referred to as Consecutive level crossings (CLC). On the other hand if the signal changes non-monotonically within the voltage window then the level crossing mode is referred to as Repeated Level Crossing (RLC). The change in the signal during the RLC period cannot be later on reconstructed since the sampling at this point violates the Nyquist theorem. However this does not create a significant distortion in the reconstructed signal since the changes in this period are restricted to less than 1 LSB above and below the sampling point. Each time the signal crosses a voltage window threshold, it's direction is recorded as a either a 'rise' or a

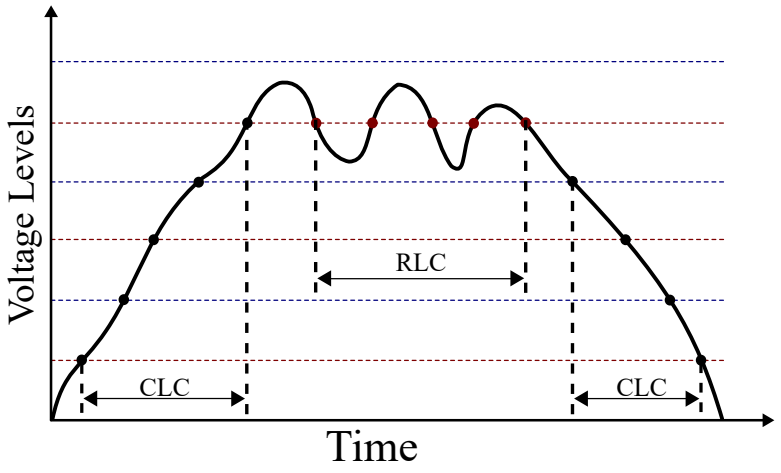


Figure 2.29: Consecutive voltage Level Crosing (CLC) and Repeated voltage Level Crossing (RLC) of a signal.

'fall'. This direction of travel is used to instruct a counter to either count up or down when each time a voltage window threshold is crossed.

Figure 2.30 shows the system block level of the ADC. It consists of a one bit DAC that adds/-subtracts the voltage value equivalent of 1 LSB from the input signal V_{ON}, a comparator *Comp1* for detecting the signal direction, a comparator *Comp2* for detecting a level crossing and a multiplexer *MUX* for changing the voltage inputs to comparator *Comp2*. It also contains additional blocks; Consecutive Level Crossing (CLC) and Repeated Level Crossing (RLC) logic used for generating a single pulse each time a voltage level is crossed and each time the signal direction changes respectively. The voltage window is defined by the voltage references V_H, V_L as V_H - V_L = 2 LSB and V_M voltage is the mid point between V_H and V_L.

Figure 2.32 shows a waveform depicting the operation of the ADC. Initially when there is no input to the ADC, V_{ON} is held at V_M and the inputs to the positive and negative terminals of comp1 are held at V_H and V_{ON} respectively via the RLC logic and multiplexer shown in figure 2.31. When a rising input signal V_{in} is applied, V_{ON} will begin to rise until it crosses V_H. At this point in time the output of Comp1 will be raised high which in turn causes the CLC logic to generate the Consecutive Crossing pulse (Cc). This resulting pulse is fed into the DAC causing it to produce a V_{ON} of V_{in}-(V_H - V_L)/2, thereby causing Comp1 output to be pulled back low. During this time the output of Comp2 is held high to indicated that the signal is rising

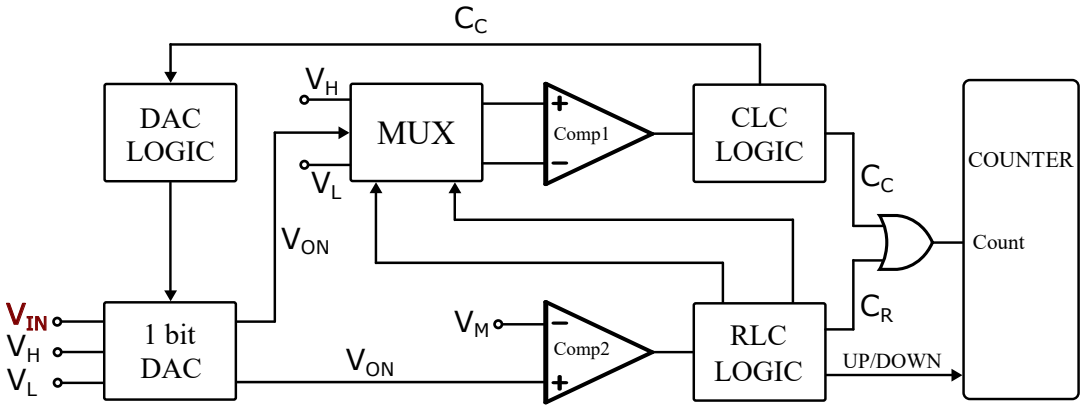


Figure 2.30: Fixed Window Level Crossing ADC with DAC feedback. Comparator 1 detects consecutive level crossings while comparator 2 detects repeated level crossings that were shown in figure 2.29.

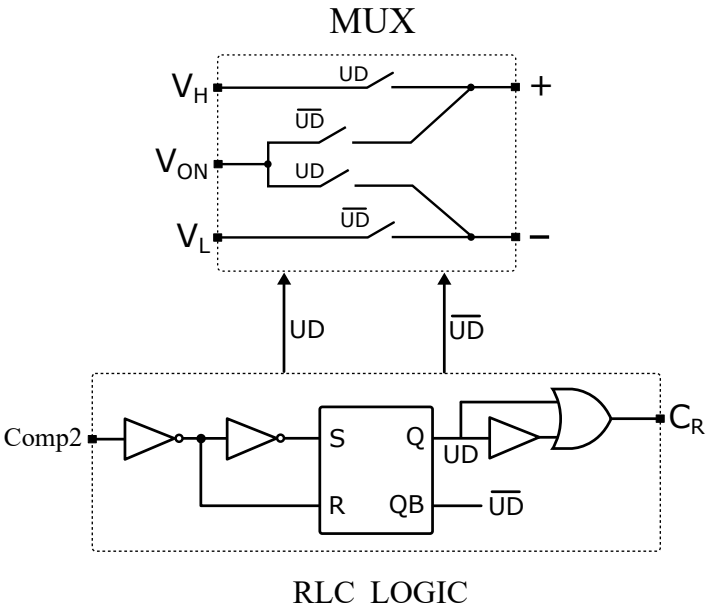


Figure 2.31: The Multiplexer and RLC logic circuit diagrams. The values UD and its inverted version are used to configure the multiplexer to connect V_H, V_{ON} and V_L to comp1.

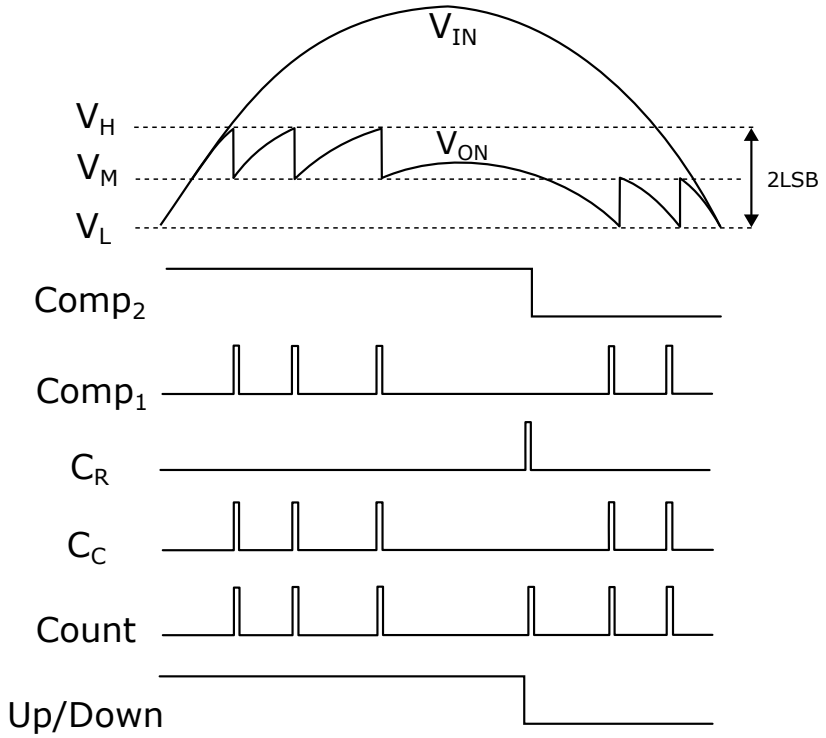


Figure 2.32: Timing diagram showing the operation of the ADC 2.30. Comp2 signal indicates whether V_{IN} is falling or rissing while comp2 indicates whether the voltage window has been crossed. A combination of the C_R and C_C pulses combine to form the cout pulse which are counted to give the converted value.

since V_{ON} is greater than V_M. This will in effect cause the RLC logic to produce UP/DOWN signal that instructs the counter to increment when it receives Cc via the OR gate. This cycle continues so long as the signal keeps on rising within the limits of the dynamic range; set by the maximum count of the counter. When the signal begins to fall, V_{ON} will go below V_M casing comp2 output to be pulled low and the multiplexer configured to switch the values at the input of the comparator i.e the positive and negative terminals of Comp1 are held at V_L and V_{ON} respectively. The UP/DOWN signal will be pulled low in effect configuring the counter to increment each time the Cc signal is received. As V_{in} continues to fall, V_{ON} also falls until it crosses V_L causing the output of Comp1 to be raised high, the counter decremented and the V_{ON} increased by (V_H - V_L)/2 until the output of Comp1 is pulled back low. This process repeats itself as the signal continues to fall. It can therefore be noted that the ADC continuously counts up/down whenever V_{ON} is above or below the voltage window and the 1 bit DAC used to generate a value of V_{in}-(V_H - V_L)/2 that pulls V_{ON} up/down in an attempt to keep it between

the voltage window.

2.4 Time to Digital Converters (TDCs)

Time to digital converters (TDC) are circuits designed to provide a relatively accurate measurement of the time interval it takes between the beginning and the end of an event. The resulting output of The TDC is a binary digital representation of the measured time. In the past TDCs have found applications in the nuclear particle physics experiments where they have been used to measure the mean lifetime and time of light of radioactive particles [31] as well as in positron emission tomography medical imaging technology [32]. Recently, they have been widely used in the implementation of high resolution sigma delta ADCs [33], digital phase locked loops (PLL) [34] and digital delay locked loops (DLL) [35]. Time to digital converters operated on the basic principle that time can be divided into measurable intervals that can be quantized into a digital code. Figure 2.33 shows a timing diagram that summarizes the operation of a typical TDC. It can be seen that the time period T_a, represented by the difference between T_{start} and T_{stop} is compared to a timing reference that is divided into fixed time periods of T_{ref} which can be derived from a clock or a delay element. T_a can therefore be estimated by counting the amount of T_{ref} that elapse between the start and stop of an event. It should be noted that if the result of dividing T_a by T_{ref} is not an integer, then a residual error T_{err} will be introduced in the results as given in equation 2.17.

$$\begin{aligned} T_{stop} - T_{start} &= (Cnt * T_{ref}) + T_{err} \\ \frac{T_{stop} - T_{start} - T_{err}}{T_{ref}} &= Cnt \end{aligned} \tag{2.17}$$

In order to reduce or totally eliminate this error, a high resolution timing reference is desired. The simplest form of a TDC is a counter which uses its clock as the timing reference. If a high resolution is desired, the counter must be designed to operate at a high frequency which in turn will result in high energy consumption. In order to alleviate the problem, various approaches such as the ones presented in [36], [37], [38] use the propagation delay of a buffer to derive the

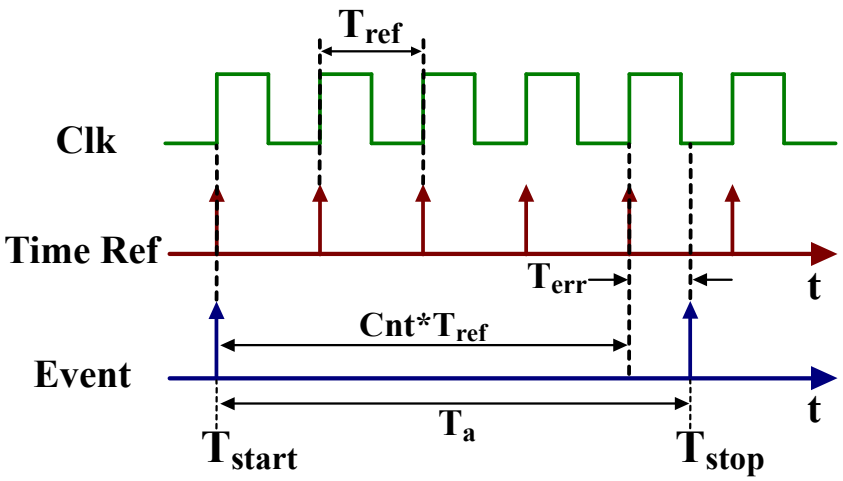


Figure 2.33: Timing representation of the operation of a TDC. Time T_a between T_{start} and T_{stop} is divided into mesurable intervals of T_{ref}

timing reference T_{ref}. These approaches rely on the advances made in modern digital CMOS technology that have been able to reduce the supply voltage as well as reduce the gate delays. This has enabled the implementation of TDCs that are both energy efficient and can achieve high resolution. In the next section various types of time to digital converters will be reviewed with their related performances discussed and compared.

2.4.1 Delay line based TDC

The delay based TDC architecture utilizes a single delay cell for its unit time measurement. It consists of several delay unit cells connected together as shown in figure 2.34 with each unit cell's output connected to the input of a register. The idea behind its operation is that the input signal propagation delay time through the delay line can be captured between the time a signal event occurs and when it stops. When the beginning of the event is detected, the start signal is raised high while the stop signal is low. The start signal is held high and begins to propagate through the delay line with the propagation delay though a single unit delay given as T_d. When the end of the event is detected, the stop signal is raised high resulting in the output of each delay cell being latched into the registers as shown in the timing diagram 2.35.

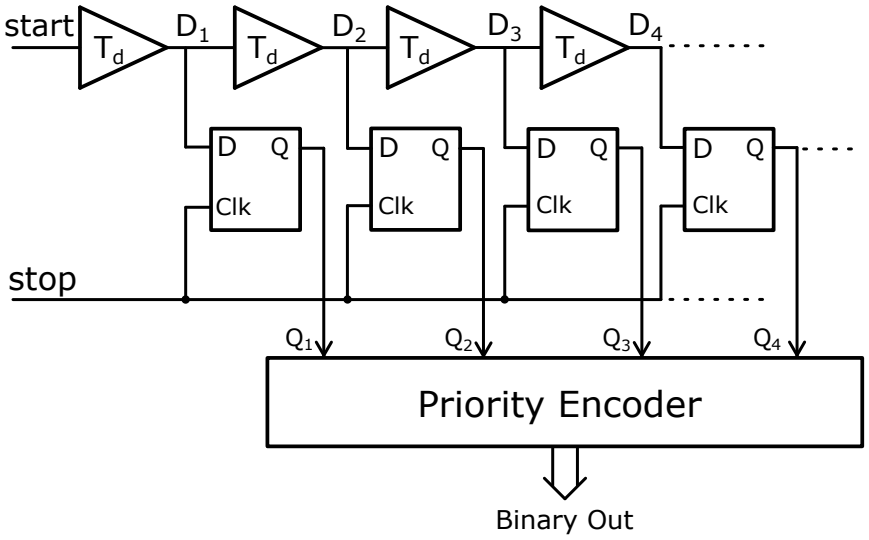


Figure 2.34: Delay based Time to Digital Converter. The time between the start and stop event is mesured using the unit delay cells and the registers

The captured register values represents the time elapsed between the start and stop events and is presented in the form of the thermometer code. The thermometer code is thereafter passed onto a priority encoder that converts it into binary value. The priority encoder gives the binary equivalent of the number of last register to capture the propagating start signal i.e if the start signal is captured by registers 1 and 2 (figure 2.34) only then the priority encoder gives the binary equivalent of 2 The delay line based TDC's resolution depends on the propagation delay T_d of each unit cell which is usually implemented with the smallest possible delay buffer. This therefore limits its maximum achievable resolution for a particular given technology. Since each unit delay cell represent an LSB transition, their number has to be increased if a higher dynamic range is required. The increased number of delay cells on other hand makes matching there propagation delays difficult and therefore making them susceptible to process and temperature variations.

2.4.2 Vernier TDC

The Vernier TDC is designed to improve resolution of the delay based TDC beyond the resolution that is achievable by the unit delay cell. Its architecture is realized by adding a delay line to

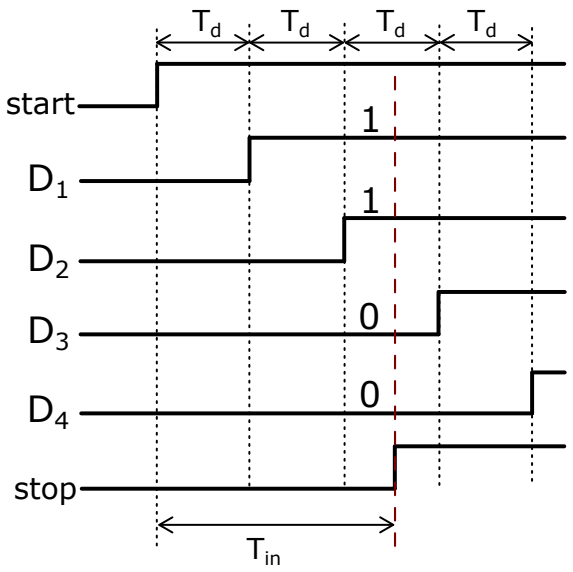


Figure 2.35: Delay based Time to Digital Converter timing diagram. The start signal is propagated through the delay cells and the stop signal used to clock each delay cell's output.

the stop signal path of the delay based TDC as shown in figure 2.36. The delay line consists of unit delay cells that have a smaller propagation delay time T_{d2} as compared to the ones in the start signal's delay line with delay time of T_{d1}.

Once the start signal has been allowed to fully propagate through its delay and the stop signal applied, the values from the start signals delay line will be captured by the registers sequentially as the stop signal propagates through its delay line. This means that the start signal will still continue to propagate until the stop signal catches up with it. Since the stop signal moves slightly faster than the start signal and the registers are edge triggered, the registers will not capture any change in the start signal's delay line once the stop signal surpasses the start signal. From this operation it can be seen that the TDC will have a base time measurement at the point when the stop signal is applied and the time measurement afterwards which depends on how long the start and stop signals align. This measurement after the stop signal is applied determines the resolution of the TDC and can be obtain as the difference of the unit delays of the start signal line and the stop signal line i.e T_{d2}-T_{d1} .

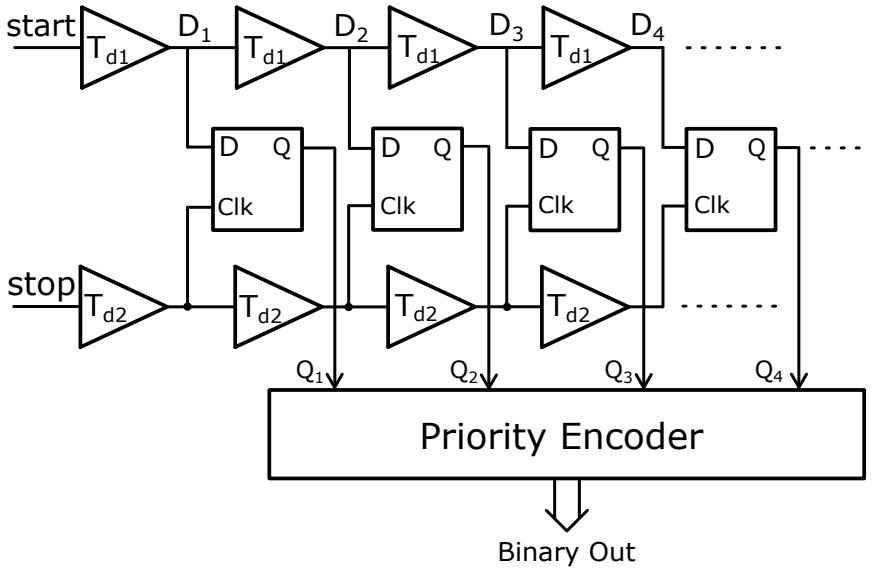


Figure 2.36: Vernier Time to Digital Converter. A delay line is added to the the stop signal path of the delay based TDC allowing for the resolution of time smaller than the unit cell delay

2.4.3 Dual step TDC

The dual step architecture consist of two TDC's, one for coarse time measurements and one for fine time measurements as shown in figure 2.37. As discussed in the delay line based TDC and vernier TDC, an increase in the unit delay cells make matching their propagation delay difficult resulting in differential non-linearity (DNL) and integral non-linearity (INL) errors. The dual slope TDC architecture is therefore designed to minimize the number of unit delay cells without reducing the dynamic range.

The coarse time measurement is done by a counter which uses the clock period as the coarse time delay (much greater than the unit delay cell). When a signal event is detected the counter is enabled by the synchronizer and begins counting the number of clock cycles elapsed. This continues until the synchronizer and the fine time TDC receive the stop signal. The fine time TDC will immediately initiate time measurement of the stop signal. On the other hand, since the stop signal can be received at any point in time within the clock period, the synchronizer has to wait for the rising edge of the clock before it can pull down the enable signal. The counter will therefore register an extra count before it stops counting after the period t_c as shown in the timing

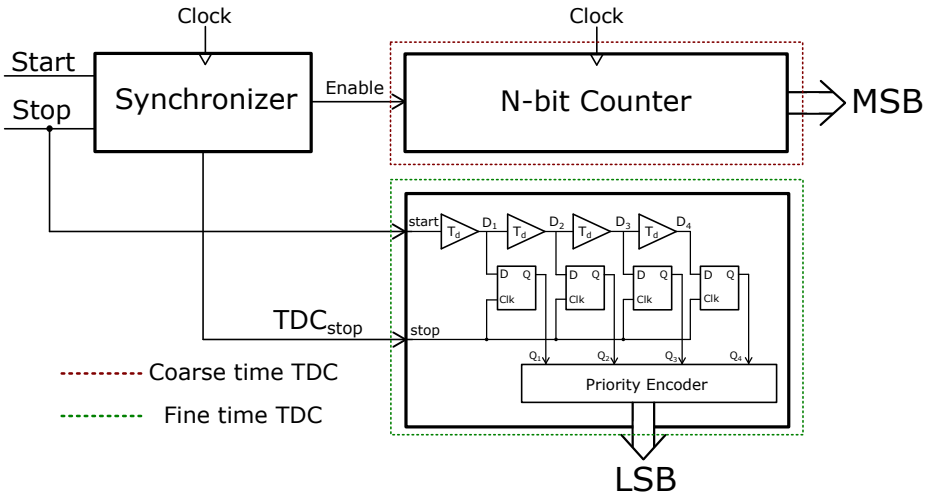


Figure 2.37: Two Step Time to Digital Converter. A coarse time TDC (counter) is combined with a fine time TDC

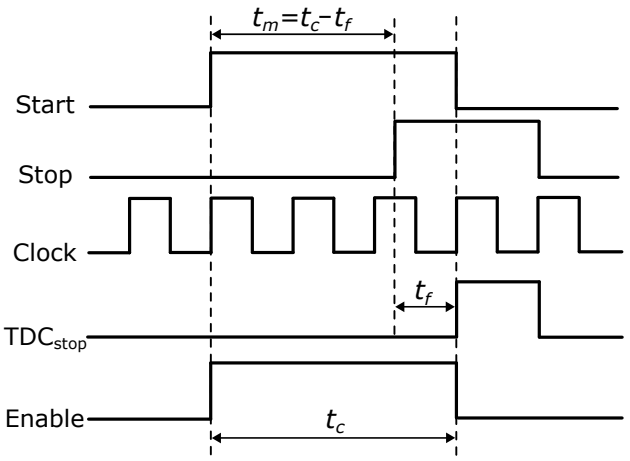


Figure 2.38: Two Step Time to Digital Converter timing diagram. The counter resolves the time t_m and the delay TDC resolves the residual time t_f that is less than the clock's period.

diagram 2.38. The TDC_{stop} signal, which is also synchronized to the clock, is pulled high when enable is pulled low thereby ending the time t_f measurement by the fine time TDC. In order to obtain the desired time measurement t_m between the start and stop events, the time measured by the fine time TDC is subtracted from the one measured by the counter i.e. t_m=t_c-t_f. To obtain the binary equivalent, the value from the fine time TDC (representing the least significant bits) is subtracted from the counter value (representing the most significant bits).

2.5 Asynchronous Digital Circuits

Most conventional digital circuit designs are usually implemented with a global clock that synchronizes the movement of data between consecutive memory blocks. The clock period has to be chosen such that it is greater than the worst case propagation delay period of data through the combinational block between adjacent registers. Since the clock in synchronous designs is global, it has to be distributed throughout the design ensuring that all registers receive the rising edge of the clock at the same time. As the designs become larger in terms of chip area, the clock distribution network has to be designed to ensure that the timing requirements are met. This necessitates the use of high drive strength buffers within the clock network to counter the delays that arise from the increased interconnect wire length. The combination of the switching in the clock buffer cells and the charging and discharging of the capacitance associated with the interconnect wire accounts for a large percentage,up to 40%, of the overall power consumption of the design as reported in [39], [40] and [41]. Asynchronous circuits on the other hand do not rely on a global clock but instead use local handshake signals to indicate the successful transfer of data from a sending block to a receiving block. This ensures that there is localized switching of the handshake signals only in the sections of the design that are involved in the sending and receiving of data. This is contrary to the switching in the global clock networks of synchronous designs where clock switching is propagated throughout the design even if movement of data is localized. The event driven nature of asynchronous circuits also ensures that the switching is only done with the availability of data. Even though modern synchronous designs can rely on clock gating to disable switching in branches of the clock network where movement of data is not required, the added circuitry required to achieve this further complicates the clock network design [40]. There are various ways that the handshaking scheme or communication channel can be implemented, depending on the trade-off between power consumption and performance as will be discussed in the next section.

2.5.1 Asynchronous Datapath encoding schemes

At the highest hierarchical level, an asynchronous design datapath consists of a sending and receiving block with a communication channel between them. The communication channel relies on an encoding scheme, consisting of a bunch of data and signalling wires, to synchronize the data transfer between blocks. There exists various types of asynchronous datapath encoding scheme with the commonly used ones being the bundled data and the dual rail encoding schemes [42], [43], [44]. The bundled data encoding scheme consists of two handshaking lines, the request and acknowledge lines, as well as a unidirectional data bus as shown in figure 2.39.

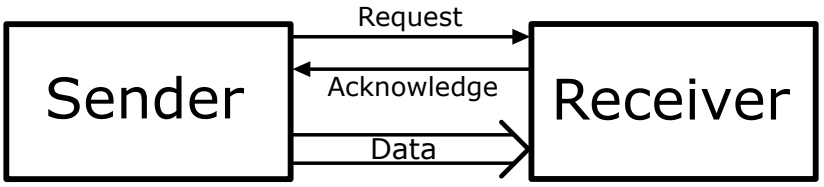


Figure 2.39: Asynchronous bundled data encoding scheme. The request and acknowledge handshake signals are used to control the movement of the data.

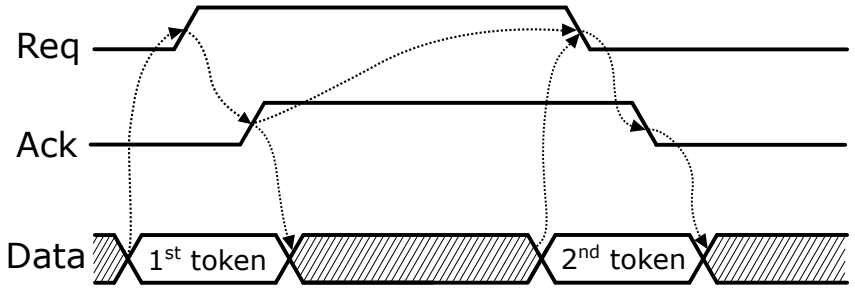


Figure 2.40: Two phase handshaking data transfer protocol. The Req and Ack signals use both thier rising and falling edges to send and receive the data respectively.

Transfer of data in this scheme can either be done using a two phase or four phase handshake protocol. The two phase protocol utilizes a single transition on the request line to indicate the availability of data and a single transition on the acknowledgement line to indicate the reception of the data. Figure 2.40 shows the timing diagram of the two phase handshaking process.

When the 1st token is ready to be sent, the sender places it on the data lines and raises the request line high. The receiver on the other hand waits until it detects the transition on the request line

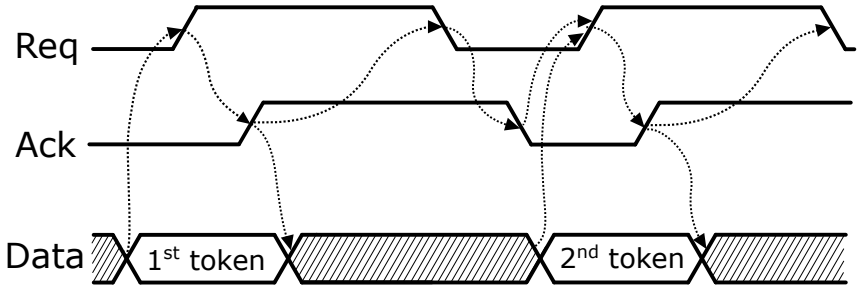


Figure 2.41: Four phase handshaking data transfer protocol. Both handshake signals must return to zero before the next data bundle can be sent.

before it can accept the data. Once the data is accepted, the acknowledgement line is pulled high thereby indicating the end of data transfer. At this point in time the sender is free to place the 2nd token on the data line. The next handshake protocol will now rely on detecting the transitions from high to low for both the request and acknowledgement lines. It can be seen that for a single token transmission only single transitions on the handshake lines are performed. On the other hand the four phase protocol shown in figure 2.41 requires that the handshake signals return to zero after a token has been transferred before the next token can be sent. It should be noted that in this handshaking protocol the data and the handshake signals path delays must be matched to ensure that they arrive at the receiver at the same time. This scheme is therefore susceptible to process, voltage and temperature (PVT) variations i.e if any of these conditions change then the propagation delay in the datapath and the handshake signal path will change and might result in the mismatch of these delays (datapath delay greater than the handshake signal delay). In order to counter this the handshake signal path delay should be made to be much larger than that of the datapath. This in turn has the undesired effect of increasing the silicon area.

The dual rail encoding scheme, shown in figure 2.42, does not rely on a request signal to indicate the validity of the data on the data lines. Instead it encodes each data bit using two bit lines i.e the Data false and data true lines resulting in a "01" for logic "1" and "10" for logic "0" as shown in table 2.1. The handshake is initiated when one of the data lines is raised high in this case data false as shown in figure 2.43.

The receiver detects this and generates the acknowledgement signal that instructs the sender to pull down its data false line. At the point when the data false is pulled down, the encoding

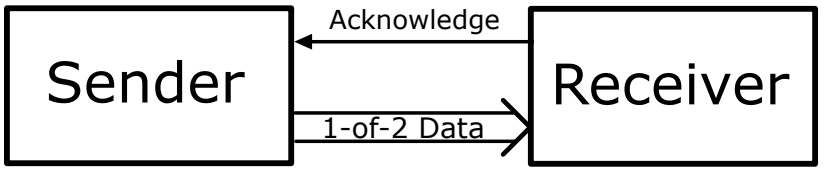


Figure 2.42: Dual rail encoding scheme uses 2 data encoding lines and an ACK signal.

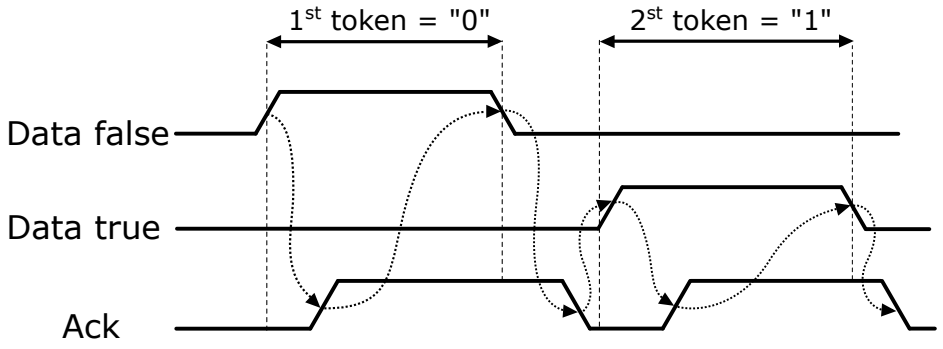


Figure 2.43: Dual rail data transfer protocol. Each data bit is encoded using a data fales and data true line. A mutualy exclusive change in these lines indicates a transfer of either a 0 or 1 after which the ACK signal is raised high.

Table 2.1: Dual rail encoding scheme

State	Data False	Data True
Spacer	0	0
Logic "1"	0	1
Logic "0"	1	0
Not used	1	1

will be "00" (spacer) indicating the end of data transfer and the next token can now be sent. It can be seen that although the request line has been removed thereby reducing the handshaking signal by one, the number of data lines increases considerably as each bit is represented by two data lines. This will in turn result in greater power consumption as compared to the bundled data scheme. However, the dual rail approach does not depend on the delay matching of the handshaking signals with the data lines. This is so because the data and its validity are encoded together on the same line thereby making this protocol delay insensitive and less susceptible to

PVT variations.

2.5.2 Power gating in asynchronous circuits

Power consumption in CMOS circuits consists of the dynamic power dissipated during circuit switching and leakage power dissipated through the flow of leakage current. In older technologies the dynamic power used to be the dominant source of power consumption. This was due to the fact that in older technologies both the gate areas as well as the supply voltages were quite large. In modern technologies the gate geometry and supply voltages have been scaled down resulting in more power being consumed through leakage current as compared to circuit switching. In order to minimize leakage power consumption, various technology solutions such as FinFets [45] and Fully Depleted Silicon On Insulator (FDSOI) [46], [47] as well as architectural solutions such as power gating [48], [49], [50], [51], [52] and reverse body biasing [53], [54] have been put forward. In conventional synchronous designs power gating/shutoff is usually initiated by a control circuit during the periods when a circuit subsystem is considered to be idle (not performing any computation). Since leakage power consumption is always constant whether the circuit is active or idle, the mentioned method of power gating does not minimize current leakage during the active period. A technique known as Sub-clock power gating has been proposed in [55] that is able to shut down the circuit during both active and idle circuit periods. This technique utilizes the fact that a given circuit might exhibit some idle time within the clock period and therefore can be turned off. Figure 2.44 shows the timing diagram for the sub-clock power gating procedure.

The power gated combinational block CB is shut off a short period after the rising edge of the clock to ensure that the hold time T_{hold} condition for the clocked registers is met. The CB will remain off for the period T_{off} until the falling edge of the clock arrives after which it will be switched on for the period T_{on}. This period, which occurs within one half of the clock period, has to be long enough to allow for the evaluation time T_{eval} of the CB results and provide the required setup time T_{stup} before the results can be clocked into the registers. If the sum of the propagation delay through the combinational block (T_{eval}), the setup and hold times is larger than one half of the clock period then the clock period has to be increased. This therefore makes

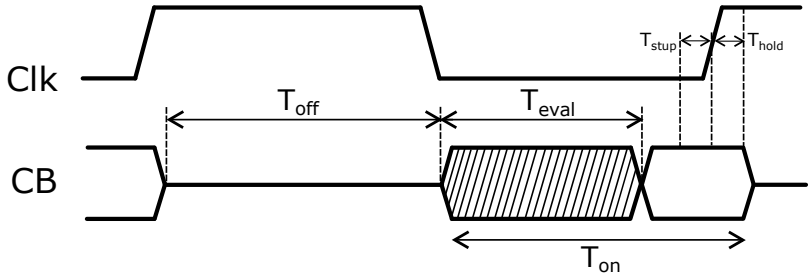


Figure 2.44: Sub clock active mode power gating timing. The combinational logic is turned OFF and back ON within a clock cycle while ensuring that the logic function is computed within T_{eval} before the next clock cycle.

this technique only suitable for low frequency clocked circuits. It should also be noted that the chosen clock period still has to take into account the worst case propagation delay path. This results in a non-optimal form of power gating since the paths with shorter propagation delays do not benefit from extra shutoff time.

In asynchronous designs power gating can be done in a more efficient manner, compared to synchronous designs as demonstrated in [56], [57], [58] and [59]. This is due to the fact that since asynchronous designs rely on local handshake signals, power gating can be applied in a more fine grained manner by turning off idle combinational blocks as soon as they compute their results. The shutoff periods of different subsections now do not depend on the worst case computation time as in the synchronous sub-clock power gating. This can be seen in figure 2.46 which is the 4 phase bundled data timing diagram for the asynchronous power gating implementation in figure 2.45.

Initially the design is shutoff until the sender raises the request signal high when it is ready. The generated request signal will immediately turn ON the combinational block which in turn begins evaluating the input data for the period T_{eval}. During this period the request signal is passed through a delay line which has a propagation delay much greater than the sum of T_{eval} and T_{stup} in order create positive slack that will counter the worst case delay on the data path. Once the request signal reaches the receiver, the results of the combinational block is latched into the receiver's registers and the acknowledgment signal generated. Upon receiving the acknowledgement signal, the sender will pull down the request signal thereby powering down the

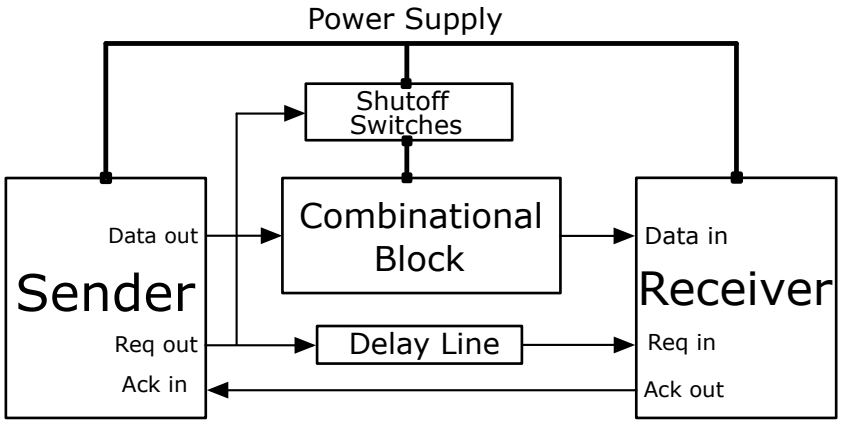


Figure 2.45: Power gating implementation in an asynchronous circuit

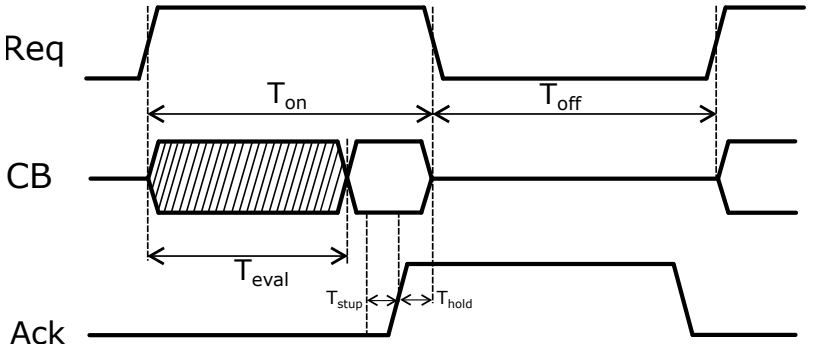


Figure 2.46: Power gating timing in a 4 phase bundled data asynchronous circuit.

combinational block and allowing the receiver to pull down the acknowledgement signal. The combinational block will remain powered off for the time T_{off} until a new token is ready to be sent. It should be noted that there is some extra power consumed through the charge-up and discharge of the power distribution network during subsequent turn ON-turn OFF cycles. Therefore in order to make some meaningful power savings gain, the leakage power saved during the T_{off} period should be greater than the power consumed during turn ON-turn OFF as explored in [60]. Power gating in asynchronous circuits can be very useful in circuits that process sparsely occurring signals such as neural and speech signals since the circuits will spend more time in the T_{off} period than the T_{on} period.

Chapter 3

Asynchronous Single Slope Level Crossing ADC

As described in Chapters 1 and 2, it would be desirable to have an ADC that only samples when the signal at its input is changing. Asynchronous ADCs exhibit this kind of operation as opposed to their synchronous counterparts. However the asynchronous ADCs described in Chapter 2 pose some undesirable effects that limit their practical usability. The floating window types [61] and [29] suffer from slope overload issues described in 2.3.1 and require complex circuits that dynamical adjust the LSB step size to avoid this problem. The fixed window type 2.3.2 suffers from linearity issues and requires extrapolation algorithms to accurately estimate the LSB step size for every sample. These problems can be attributed to the fact that the quantization process is dependent on the signals rate of change i.e quantization is performed by simply incrementing or decrementing the number of counts each time the signal crosses a voltage window above or below the previous one. This chapter introduces and describes a new asynchronous ADC architecture that intends to minimize the undesired effects of the previously described asynchronous ADC architectures by making the absolute digital amplitude obtained by quantization independent of the rate of change of the signal. The top level block design is introduced and its desired operation and waveforms discussed. Thereafter each building block requirements is described and the block's physical implementations presented. Finally simulation results of the proposed design are presented.

3.1 ADC Architecture

Figure 3.1 shows the block diagram of the proposed ADC architecture. It consists of a slope detector, voltage to time converter (comparator and ramp generator), time to digital converter and an asynchronous control logic block. The slope detector continuously monitors the input signal and triggers the voltage to time converter (VTC) to begin conversion when the input signal crosses a set voltage window. The TDC receives the pulse width modulated signals from the VTC and converts them to digital bits. The novelty in this architecture is in the fact that the ADC circuit configuration alows for the actual quantized signal amplitude to be independent of the signal's rate of change and will therefore not suffer from the overload distortion and linearity issues present in [27] [29]. The signals rate of change is only used to trigger the sampling point.

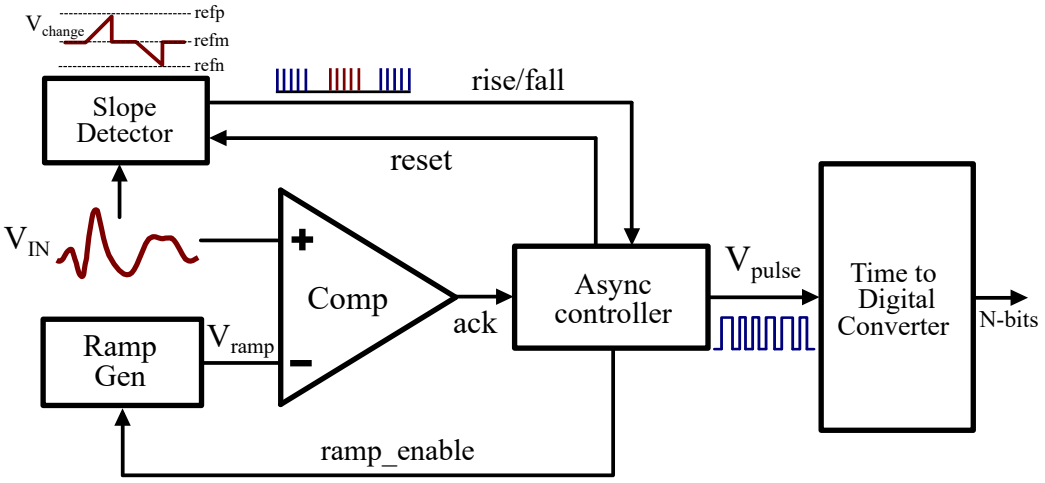


Figure 3.1: Single Slope Asynchronous Level Crossing ADC Architecture

Figure 3.2 shows the waveform from given points of the proposed ADC detailing its desired operation. The slope detector monitors the input signal V_{in} to determine if it crosses the voltage window set by the fixed voltages refp and refn. Initially when the input signal is non changing, the slope detector's internal signal V_{change} is held at a voltage refm midpoint of refp and refn. The voltage of the signal V_{change} is proportional to the rate of change of the input signal V_{in} i.e an increase in the V_{in} will result in an increase in V_{change} while a decrease in V_{in} results in a decrease of V_{change}. The corresponding change in V_{change} signal is compared to the fixed voltage window upper limit (refp) and lower limit (refn) resulting in the generation of the rise

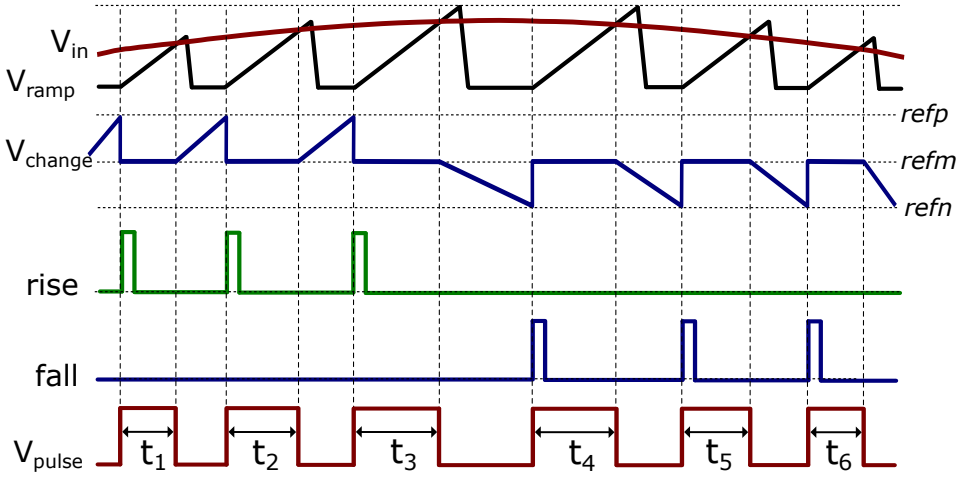


Figure 3.2: The slope detector performs a time derivative function on V_{in} to generates V_{change}. An intersection between V_{change} and refp/refn initiates the A-D conversion

or fall pulses respectively when the thresholds are crossed. Once the asynchronous control logic block detects either a rise or fall pulse, it will immediately reset the slope detector by raising the reset signal high and at the same time enable the ramp generator to begin producing V_{ramp}. The V_{pulse} signal which is passed on to the TDC is pulled high at the same time V_{ramp} is enabled. When V_{ramp} intersects V_{in}, the comparator output ack is pulled low resulting in the signals V_{pulse} and $ramp_{enable}$ also being pulled low by the asynchronous controller thereby marking the end of the voltage to time conversion. The TDC will thereafter convert V_{pulse} into its equivalent digital binary code. Since the quantization process in this architecture only depends on the ramp generator and TDC rather than the signals rate of change (as in previous asynchronous ADC architectures), the converted signal will be independent of the signals rate of change. The slope detector, which is the only block sensitive to the signal's rate of change, is only used to determine at which point in time a sample is to be taken. The operation of the ADC given by the timing diagram in 3.2 can further be summarized into the flow chart given in figure 3.3.

On the other hand since the sampling is done asynchronously when the threshold window is crossed, the sampling rate is not fixed and will vary with the rate of signal change. As shown in figure 3.4, the sampling periods $T_{sample1}$ and $T_{sample2}$ between the two consecutive pulses P_1 and P_2 are different. They are determined by the amount of time T_{quant} it takes for the TDC

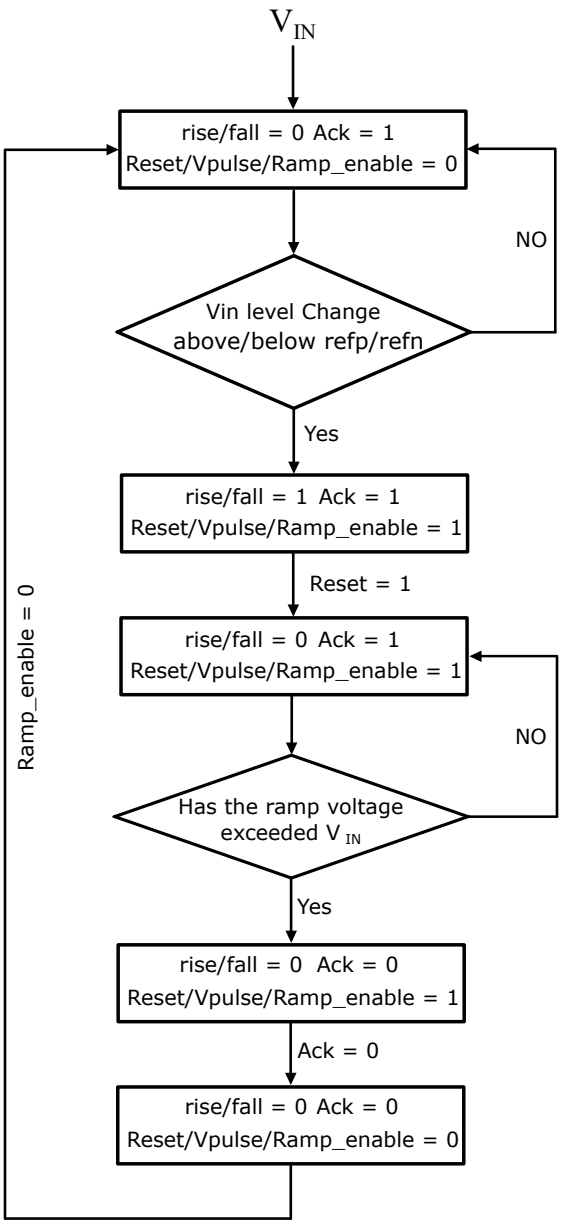


Figure 3.3: The operation of the ADC slope detector performs a time derivative function on V_{in} to generates V_{change}. An intersection between V_{change} and refp/refn initiates the A-D conversion

to quantize each sample, the delay during the reset period T_{reset} and the time T_{track} it takes the slope detector to track and detect the voltage window crossing. The reset delay period, which is the time it takes to transition between T_{quant} and T_{track}, is constant and is determined by the propagation delay of the asynchronous control logic and the inherent delay in the slope detector circuitry. Both the quantization time T_{quant} and the tracking period T_{track} are not constant.

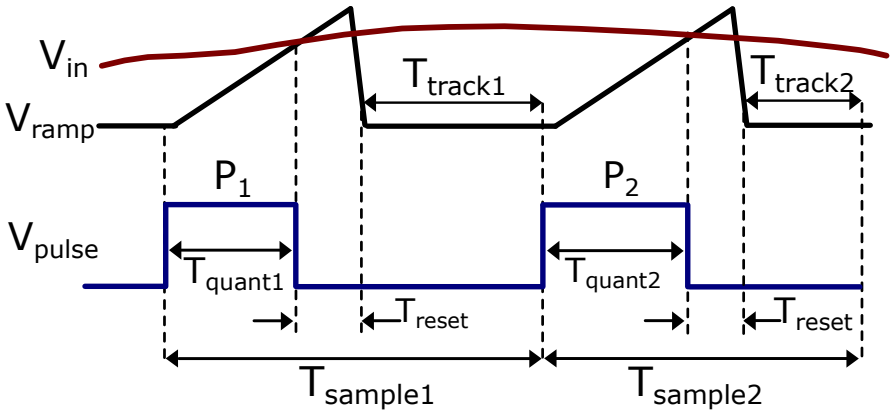


Figure 3.4: Timing diagram of the single slope Level crossing ADC showing the individual time periods T_{quant}, T_{reset} and t_{track} that add up to form the sampling period T_{sample}

The quantization time is directly proportional to the signal's amplitude while T_{track} is inversely proportional to the signal's rate of change. The sampling period between two adjacent samples can therefore be obtained as given in equation 3.1. Figure 3.5 shows the simulated results obtained from the ADC's model based on the operation given in figure 3.2 . It can be seen that the sampling period T_{sample} is smaller when the rate of change of the sine wave is high and is larger when rate of change is low. During the period when the change in V_{in} does not cross the fixed voltage window, no samples are produced.

$$\begin{aligned} T_{sample} &= T_{quant} + T_{reset} + T_{track} \\ T_{quant} &\propto V_{in} \\ T_{reset} &= Constant \\ T_{track} &\propto \frac{1}{dV_{in}/dt} \end{aligned} \tag{3.1}$$

3.2 Slope detector

As described in the previous section, the slope detector should be able to perform a derivative function on V_{in} and compare its result to a fixed voltage window. Figure 3.6 shows the realization of the desired operation by using a switched capacitor differentiator that performs the

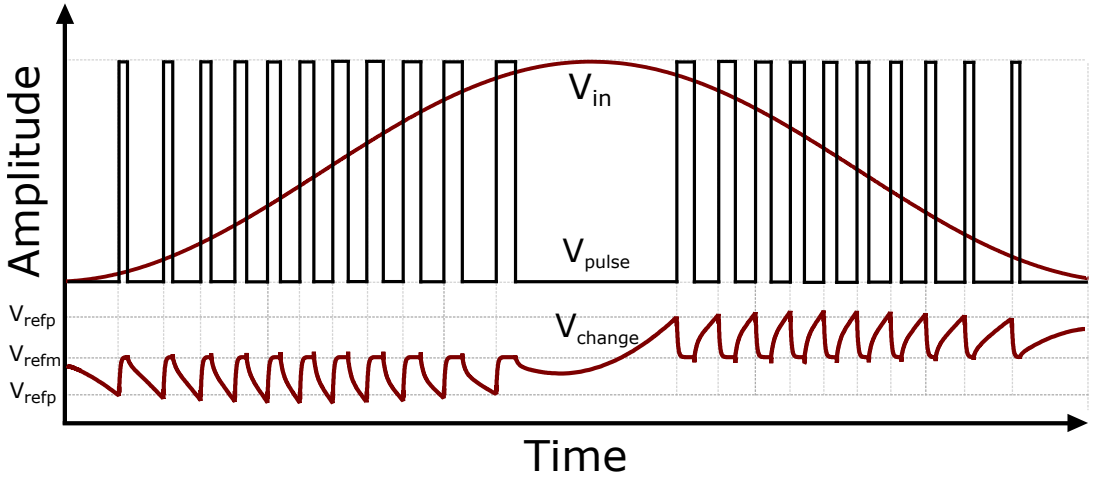


Figure 3.5: Simulated results showing V_{in}, its time derivative V_{change} and the resulting pulse width modulated signal V_{pulse}

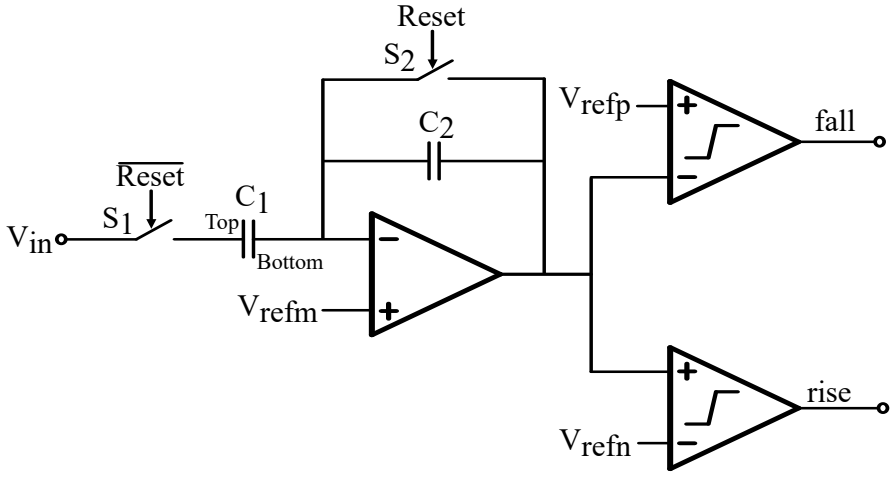


Figure 3.6: The slope detector realizes the time derivative of V_{in} through the switched capacitor differentiator formed by the OTA and the capacitors. The resulting V_{change} is compared to V_{refn} and V_{refp}.

derivative function and two comparators that are used for setting the fixed voltage window. The slope detectors has two phases of operation, i.e track phase and, the reset and hold phase. The switched capacitor implementation was chosen over a continuous time one due to the fact that it is able to detect any change in V_{in} that occurs during the reset and hold phase as will be explained later.

During the reset and hold phase, switch S_2 is closed while S_1 is opened making the differentiator

operate as a voltage follower as shown in figure 3.7. The voltages at both the inputs and the output of the transconductance amplifier (OTA) will therefore be the sum of the offset voltage and the midpoint reference voltage V_{refm}. The voltage V_{refm} is applied to the positive input

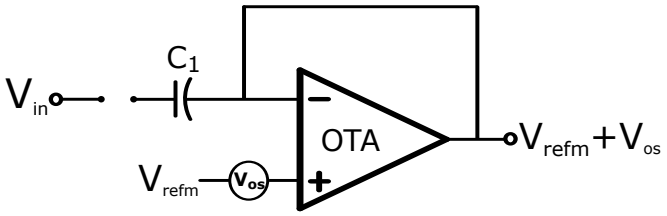


Figure 3.7: The differentiator is configured as a voltage follower during the quantization period T_{quant} that is shown in figure 3.4

terminal of the OTA so as to pull the OTA's output to the midpoints of V_{refn} and V_{refp}. Initially, in the previous track phase V_{in} was connected to capacitor C_1 resulting in its top plate acquiring a positive charge equivalent to V_{in}. Since the top plate of C_1 is now disconnected from V_{in}, any change in V_{in} during this phase will not result in the generation of additional positive charge and therefore C_1 will still retain the charge it acquired in the track phase. The bottom plate of C_1 on the other hand will acquire charge equivalent of V_{refm}+V_{os} due to the fact that the differentiator is connected in a voltage follower (unity gain amplifier) configuration. The output of the OTA will be held at V_{refm}+V_{os} throughout this phase. During the track phase, switch S_2 is opened

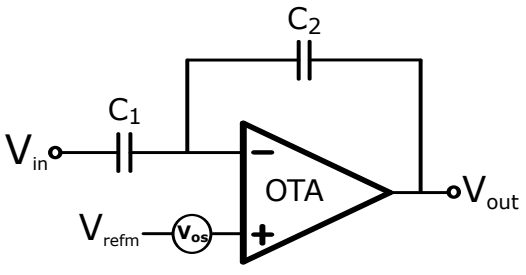


Figure 3.8: The differentiator is configured as a charge amplifier during the quantization period T_{track} that is shown in figure 3.4

and S_1 closed thereby configuring the differentiator to operate as a charge amplifier as shown in figure 3.8. Assuming that the OTA has a significantly large open loop gain, the charge transfer from C_1 to C_2 is given by equation 3.2 and the transfer function of the charge amplifier given

by equation 3.3. The change in the input signal, ΔV_{in} , is given by the difference between the present value of V_{in} and its previous value immediately after the reset and hold phase. It should be noted that although the slope detector does not track the input voltage change during the reset and hold phase, any signal change during this period will still be detected in the next track phase. This is because there will exist a voltage difference between the voltage at the top plate of C_1 and V_{in} at the beginning of the track phase. This difference will be part of the accumulated change in V_{in} during this phase.

$$C_2 V_{out} = -\Big[C_1(\Delta V_{in}) + C_1(V_{refm} + V_{os-ota})\Big] \tag{3.2}$$

$$V_{out} = -\left[\frac{C_1}{C_2}[\Delta V_{in} + (V_{refm} + V_{os-ota})]\right] \tag{3.3}$$

The resulting OTA voltage output V_{out} in the track phase is continuously compared to the voltages V_{refp} and V_{refn} via the comparators. These reference voltages are chosen such that the voltage difference between each of them and V_{out} of the OTA, during the reset and hold phase, should be the same. This should be done in order to ensure that the tracking period for a given voltage slope is constant for both a rise and a fall in V_{out}. The offset voltage of the OTA, which is present in V_{out} (equation 3.2), together with the offset voltages at the input of the comparators (as shown in figure 3.9) will however make it difficult to pick the right fixed values of V_{refn} and V_{refp}.

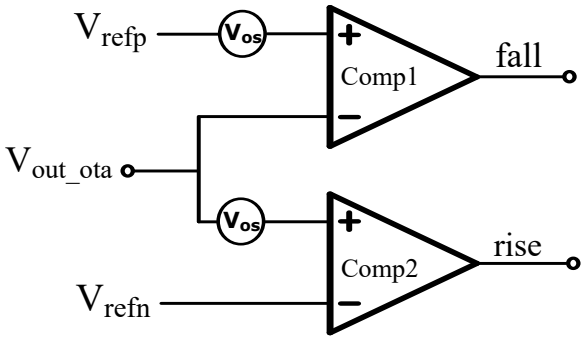


Figure 3.9: The uncorrelated comparator offsets at the inputs of the comparators will affect the period T_{track} for a rising and a falling V_{in}

This might result in a difference in the number of samples generated between when a sine wave signal of a particular amplitude and frequency is rising and when it is falling. It is therefore desirable to make these reference voltages tuneable after fabrication to counter the changes due to the offsets. It should be noted that since the slope detector is not part of the quantization circuitry, a slight difference in these voltages will not affect the quantized signal's amplitude but would rather affect the sampling periods. There will therefore be a variation in the Track variable in equation 3.1 resulting in two equations, one for when the signal is rising and the other for when the signal is falling. In addition to this, since the slope detector operation does not modulate the quantized signal's amplitude it follows that the LSB of the ADC is also independent of the value of the voltage window as opposed to the fixed widow level crossing asynchronous ADCs discussed in chapter 2.3 . This therefore allows for some degree of flexibility in choosing the voltage window size. If the capacitors C_1 and C_2 are chosen to be equal, then there will be no amplification of the input voltage change. This will require that the voltages V_{refp} and V_{refn} be chosen to give a smaller voltage window so that a small change in the input signal can be detected. The lower limit of the voltage window will however be limited by the offset voltages of the comparators. In order to counter this, a larger voltage window can be chosen and capacitors C_1 and C_2 selected so that the ratio C_1/C_2 is greater than 1 resulting in the amplification of the value of ΔV_{in} and $V_{refm}+V_{os-ota}$ as given in equation 3.2. This will therefore allow for the detection of signals that are smaller than the two comparators offset voltages.

3.2.1 Operational Transconductance Amplifier

As was discussed in the previous section, the slope detector relies on the OTA and the capacitors C_1, C_2 to determine the rate of change of the input signal. It is therefore necessary to design an OTA that would satisfy the requirements of the slope detector. The target applications for the ADC, such as implantable neural recording devices and "always on" speech recording devices, described in Chapter 1, requires that the slope detector be able to track signals within the range of $1Hz$ to about $20KHz$, and therefore its bandwidth during the track phase should be above $20KHz$. Since in the track phase the slope detector is operating in closed loop as a charge amplifier, the OTA has to be designed to have a high open loop gain bandwidth in order to

satisfy the bandwidth requirements of the slope detector. The transfer function of the charge amplifier can be calculated from equation 3.4 where A_V is the open loop gain, F is the feedback factor and LG the loop gain.

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}\left[\frac{\frac{A_V C_2}{C_1+C_2}}{1+\frac{A_V C_2}{C_1+C_2}}\right] = -\frac{C_1}{C_2}\left[\frac{A_V F}{1+A_V F}\right] = -\frac{C_1}{C_2}\left[\frac{|LG|}{1+|LG|}\right] \tag{3.4}$$

$$For \quad A_V = \infty, \quad \frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}$$

For an ideal OTA the open loop gain is taken to be infinite and therefore the transfer function is evaluated to be the ratio of C_2 to C_1. For a practical OTA the open loop gain is finite and therefore its transfer function will be a scaled value, by a factor of $(|\mathbf{LG}|/(\mathbf{1}+|\mathbf{LG}|)$, of the infinite OTA's open loop gain i.e. $-\mathbf{C_1}/\mathbf{C_2}(|\mathbf{LG}|/(\mathbf{1}+|\mathbf{LG}|)$. If C_1 and C_2 are chosen to be equal then the feedback factor will be 0.5 thereby halving the open LG. This will in effect result in the new unity gain bandwidth of the charge amplifier, which is in a closed loop configuration, being divided by 2.

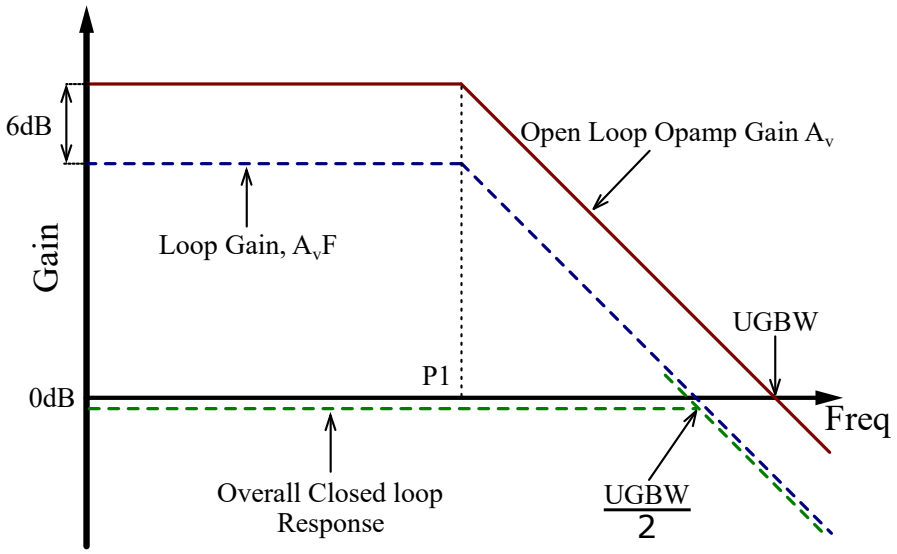


Figure 3.10: OTA frequency response plot showing the loop gain, open loop gain and the overall closed loop gain when the OTA is configured as shown in figure with C1 equal to C_2

This can be illustrated in figure 3.10 showing the bode plot of the open loop gain A_V, loop gain $A_V F$ and overall closed loop response. It can be seen that the overall closed loop response has a bandwidth which is equal to half the Unity Gain Bandwidth (UGBW) of the OTA in open loop.

In order for the slope detector to be able to operate up to a frequency of 100 *kHz*, the OTA should have a Unity Gain Bandwidth that is above 200 *kHz*. In addition to this the OTA should also be designed such that it is not slew rate limiting at 100 *kHz*. With the peak to peak voltage of the input signal Vin_{pp}, the operating frequency F and the load capacitance known, the required slew rate and slew current I_{SR} of the OTA can be calculated as shown in equation 3.5 . In this particular design the maximum Vin_{pp} is expected to be 2V and the load capacitance, which is the value of C_2, is taken as 250 *fF*. The slew rate is therefore evaluated to be 1.2V/μs and the slew current to be 0.31μA (increased to 0.5μA for the design).

$$\begin{aligned} SR &= 2.\pi.F.Vin_{pp} \\ I_{SR} &= SR.C_L \end{aligned} \tag{3.5}$$

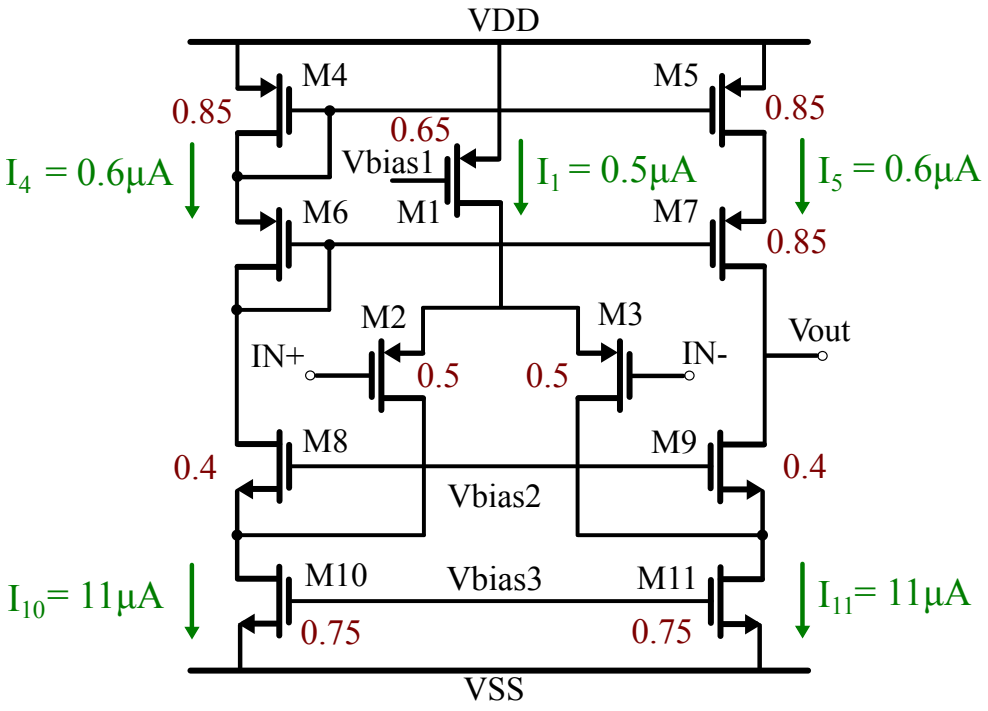


Figure 3.11: Folded cascode OTA schematic

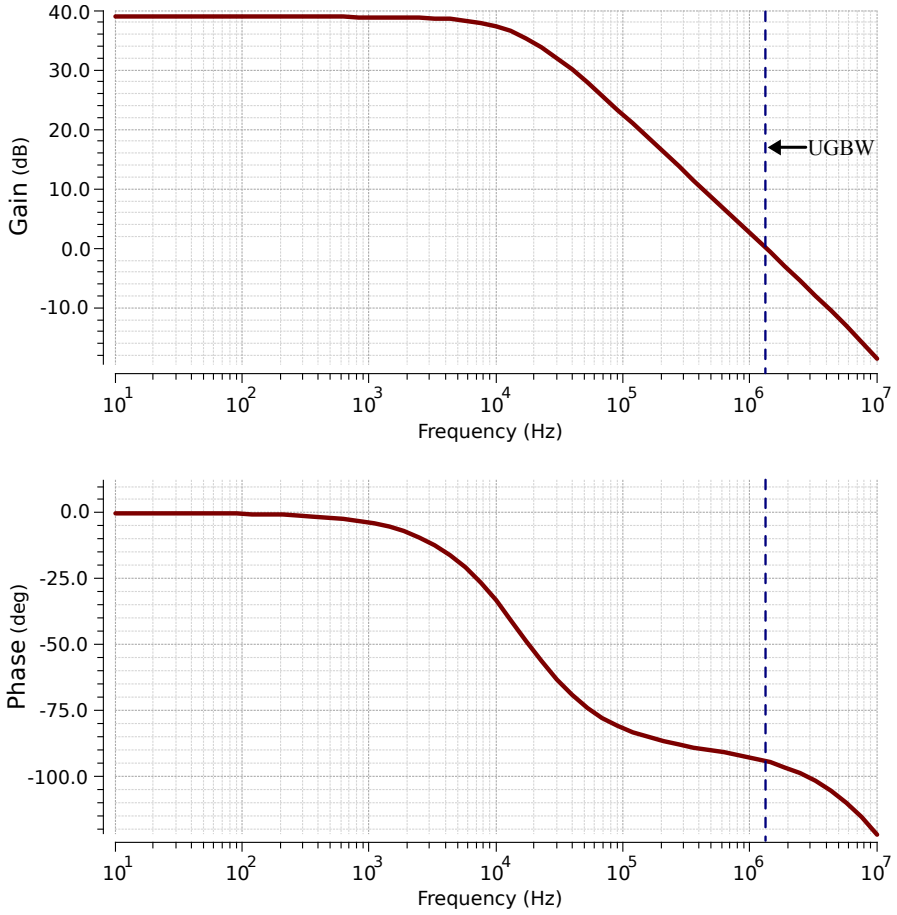


Figure 3.12: OTA frequency response. The unity gain bandwidth is 1.766MHz and the phase margin 89.2 degrees

The folded cascade topology was chosen for the OTA implementation because of its ability to achieve high gain with a single stage in addition to the fact that a good phase margin can be achieved without requiring a compensation capacitor. The topology also provides a good Power Supply Rejection Ratio as compared to the two stage compensated OTA [62]. Figure 3.11 shows the OTA circuit implemented in a 0.35μm technology.

The transistor sizes were calculated based on a voltage supply of 2.6V and a chosen effective overdrive voltage of 200mV. The supply voltage is slightly lower than that recommended 3.3V of the CMOS technology being used i.e AMS 0.35μm technology. This was done in order to minimize the power consumption of the OTA. The biasing current I_1 for transistor M_1 was obtained from the slew rate requirements as 0.5μA while I_4 and I_5 were chosen to be 0.6μA.

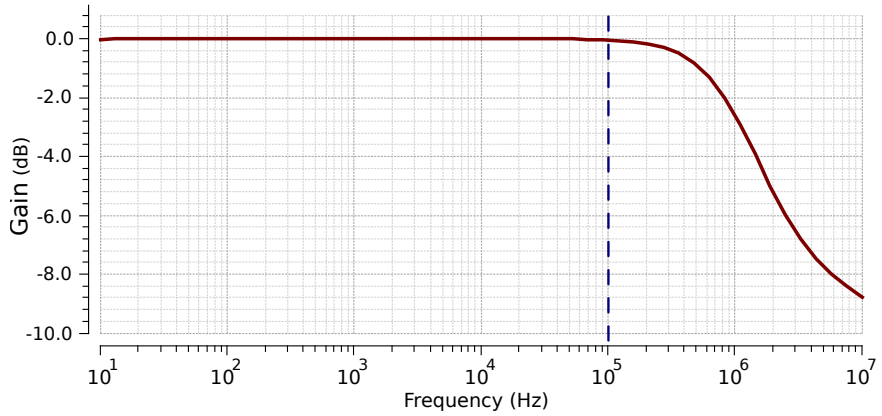


Figure 3.13: Frequency response of the slope detector operating in the track phase. The unity gain bandwidth of the circuit is 100kHz, which is way bellow that of the OTA

All transistor lengths were chosen to be 1μm. The magnitude and phase response of the OTA with respect to frequency are shown in figure 3.12 while the magnitude response of the slope detector operating in the track phase is shown in figure 3.13. It can be seen the bandwidth of the slope detector is much lower than that of the OTA as was discussed at the beginning of this section.

Figure 3.14 shows the monte-carlo simulations results of the OTA's UGBW for 300 random sampling points obtained as a result of process variations and mismatch in transistor dimensions.It can be seen that the UBGW varies from $500KHz$ to $2.3MHz$ about a mean value of 1.34MHz. Since the OTA was designed to function with inputs of up to 100KHz when its operating as part of the slope detector circuit, the minimum UGBW due to process variations and device sizes will not negatively impact the desired operation of the slope detector. Figure 3.15 shows the group of OTA gain curves obtained from the simulations.

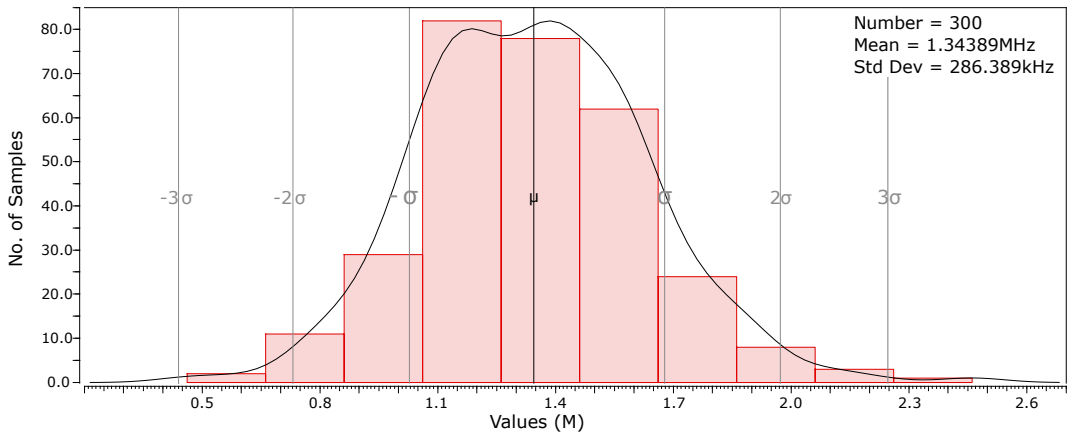


Figure 3.14: Monte-carlo simulations results of the OTA's UGBW for 300 random sampling points obtained as a result of process variations and mismatch in transistor dimensions

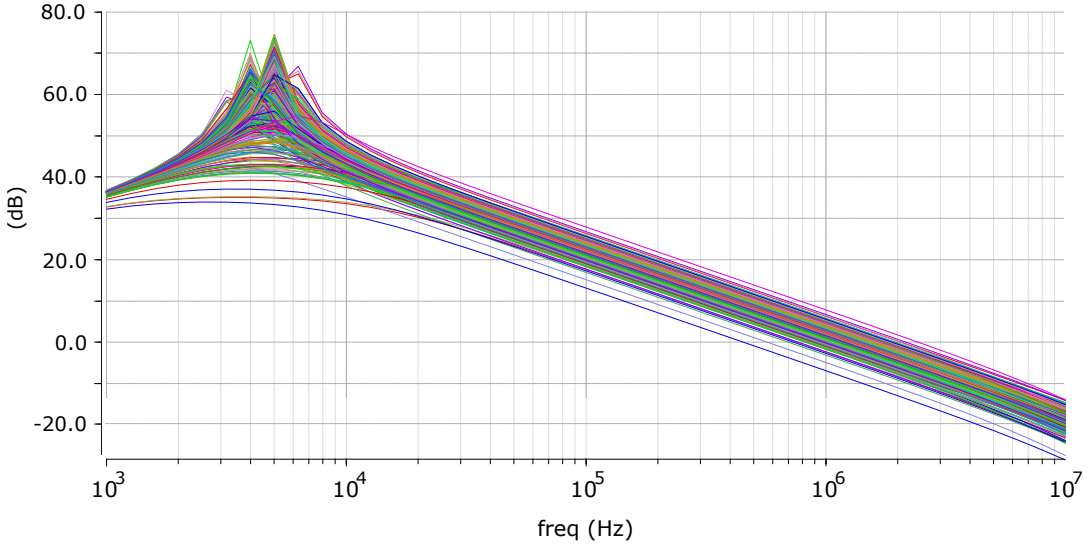


Figure 3.15: OTA gain curves obtained from the monte carlo simulations.

Figure 3.16 shows the squared output referred noise plot of the OTA. The total output referred of the OTA, found by integrating the noise from 1Hz to 1.76MHz, is $1.24E^{-5}\ V^2$ which can be referred to the input by dividing it by the gain to give $3.15E^{-8}\ V^2$. The noise contribution of the OTA to the input signal is dominated by the flicker noise generated by transistors M10 and M11 providing a total output referred noise of $7.333.15E^{-5}\ V^2$ (58.9% of total noise). Initially

this number was higher and therefore the area of the two transistors were increased in order to minimize it. The noise was integrated from $1Hz$ to $1.76MHz$ (UGBW) since above the UGBW the OTA attenuates any present thermal noise.

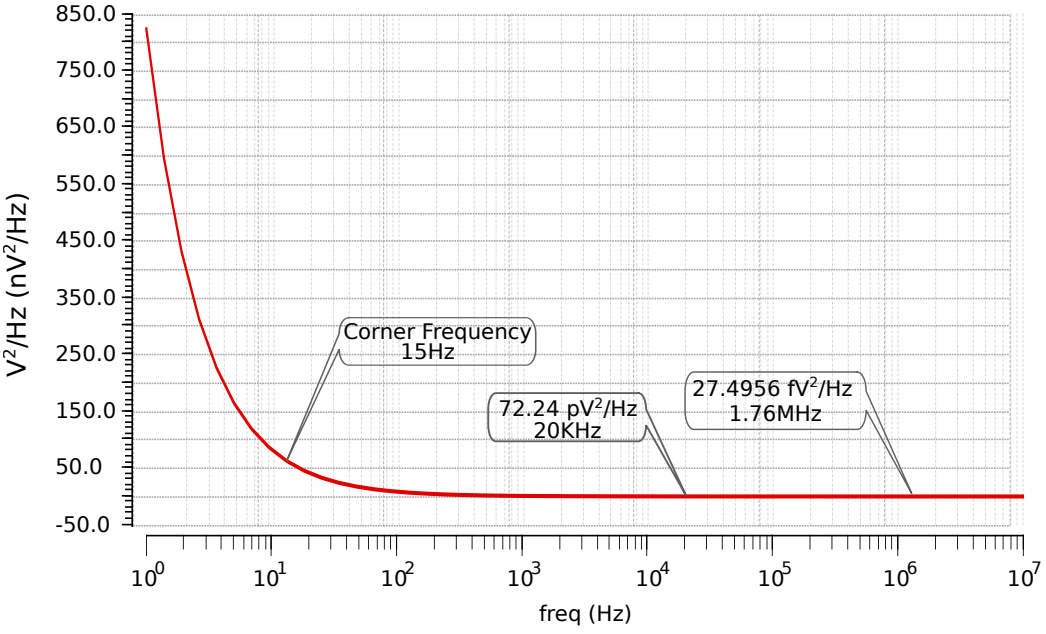


Figure 3.16: OTA squared output referred noise. The corner frequency occurs at about 15Hz.

3.2.2 Comparator

The proposed ADC utilizes two comparators in the slope detector and one comparator used for comparing the input signal and ramp generator. As was discussed in section 3.2, any voltage offset at the input of the comparators might affect the minimum possible voltage window that can be set on the slope detector. This is so if the slope detector is set to operate with a gain of unity during its tracking phase. If on the other hand it is configured to have a gain greater than unity then the voltage window can be chosen to be large, thereby avoiding the offset problem, without really affecting the minimum level of signal change detectable. In addition to this it should be noted that due to the amplification of the signal change, the level of voltage that the comparator is able to resolve can be relaxed. The comparator that performs the comparison between the input signal and the ramp signal on the other hand has to have a high resolution and

should be designed to minimize the input offset voltages. Instead of designing two comparators with different specifications, a comparator that satisfies the resolution requirements of the ramp and input signal's magnitude was chosen.

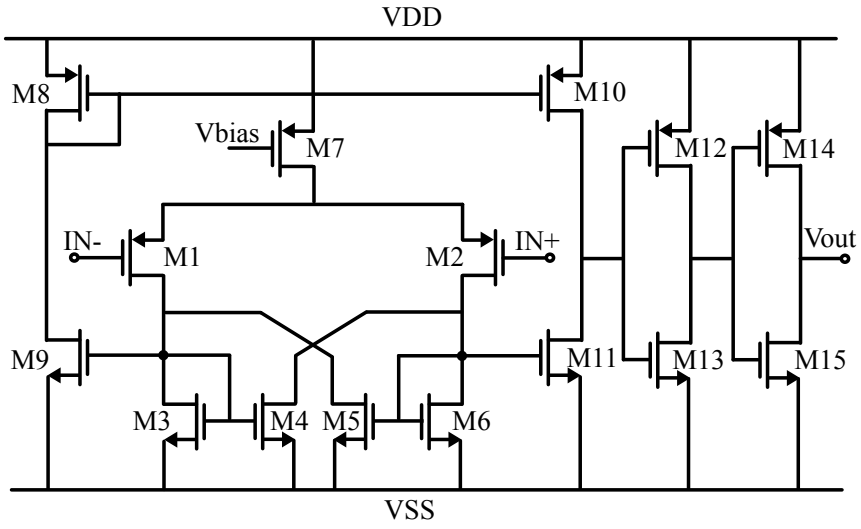


Figure 3.17: Schematic of the comparators used in the slope detector and the voltage to time converter.

Figure 3.17 shows the circuit diagram of the comparator. It is a continuous time open loop comparator with positive feedback introduced by transistors M_4 and M_5 to provide hysteresis [63] and two push pull inverters at its output. In order to evaluate the resolution of the comparator using equation 3.6 as presented in [63], we need to know the upper voltage V_{OH} and lower voltage V_{OL} limits at the outputs as well as the comparator's gain Av.

$$V_{res} = \frac{(V_{OH} - V_{OL})}{A_V} \tag{3.6}$$

These values must meet the required upper and lower input limits of the following digital circuits. For CMOS digital circuits these values should be at least 70% (upper limit) and 30% (lower limit) of the rail to rail supply voltage. In our case, with a supply voltage of 2.6V for the analogue blocks (including the asynchronous controller) and a comparator gain of 54dB, the comparator's resolution is evaluated to be about 2mV. However when a 300 random point Monte

Carlo simulations were performed on the comparator to evaluate the variance in its 2mV resolution, it was found that only a yield of 46% is possible. By adjusting the resolution to 10mV it was found that a yield of over 93% is possible. This therefore placed a limit on the minimum difference between the upper and lower reference voltages to the midpoint voltage of the slope detector to 10mV.

3.3 Ramp Generator

As has been mentioned in section 3.1, the analogue input signal is converted from its amplitude's voltage representation to a time representation by comparing it to a ramping voltage signal. The ADC's resolution is therefore dependent on the ramp generator together with the time to digital converter. Figure 3.18 shows the ramp signal being compared to the input signal.

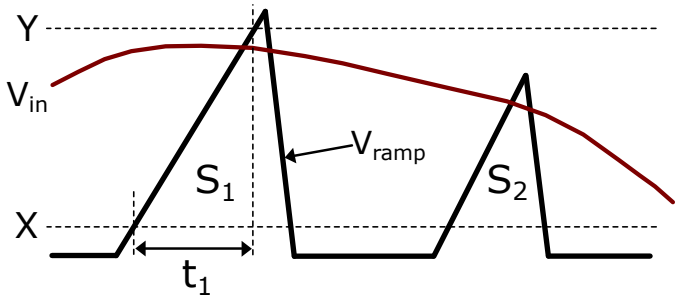


Figure 3.18: The ramping voltage should be designed to be linear between point X and the full scale input signal's amplitude represented by Y.

The ramp signal starts from its lowest value X and rises to its highest value Y. It's voltage rise during this period determines the ADC's dynamic range. The ramping signal's slope is therefore desired to be linear up to point Y and the input signal must be limited within this range as shown in figure 3.18. In order to determine the number of bits that can be obtained, the time resolution of the TDC must be known first. The number of bits can thereafter be obtained as given in equation 3.7. The value t_1 represents the time it takes the slope to rise from point X to Y as shown in figure 3.18, while t_2 represent the minimum possible time resolution (LSB) of the TDC.

$$N_{bits} = Log_2\left(\frac{t_1}{t_2}\right) \tag{3.7}$$

Since the proposed ADC samples its input signal asynchronously with non-uniformly spaced samples, the sample rate will continuously vary depending on the input signal. We will therefore pick a desired minimum sampling rate based on the expected maximum input signal frequency, which is $20KHz$ in our case, and the signal's maximum amplitude. The rationale for picking these operating points to obtain the minimum allowable sampling rate can be deduced from figure 3.18. It can be seen that it takes a longer time for the ramp signal to intersect the input signal at high amplitudes (S_1) as opposed to the shorter time it takes in the case of a smaller amplitude (S_2). This differences in time will in turn affect the sampling rate. The input signal's frequency on the other hand will affect the time that the ADC's slope detector takes during the track phase as was discussed in section 3.1 and summarized in equation 3.1. As required by the Nyquist theorem, we must chose a sampling rate that is at least twice the frequency of the highest frequency signal in order to guarantee the proper capture of the input signal. In our case the sampling period can be calculated using equation 3.1. The value of T_{quant} can be obtained from the time it takes the TDC to convert a full range input, T_{track} can be approximated as the slew rate of the input signal of the highest expected frequency of $20KHz$ and T_{reset} obtained from simulations. The resulting sampling period has to be lower than that dictated by the nyquist theorem.

Figure 3.19 shows the circuit implementation of the ramp generator. It consists of a cascade current mirror that charges up a capacitor via a transmission gate switch S_2, and an NMOS transistor switch S_1 that discharges the capacitor. When an input signal rises above or falls below a set voltage window, the slope detector will send a signal to the asynchronous digital controller which in turn enables the ramp generator to begin charging C_r via S_1. Once the capacitor voltage equals the input signal's voltage, the asynchronous digital controller will open switch S_1 and close S_2 thereby discharging C_r. Transistors M_2 and M_4 are sized to provide a constant current of $192nA$ that charges C_r ($1pf$) during the T_{quant} period upto the higher voltage limit Y (as shown in figure 3.18), in our case 1.35V. This voltage is chosen such that M_2 and M_4 remain in saturation during the ramp up period to ensure a good degree of linearity. Process

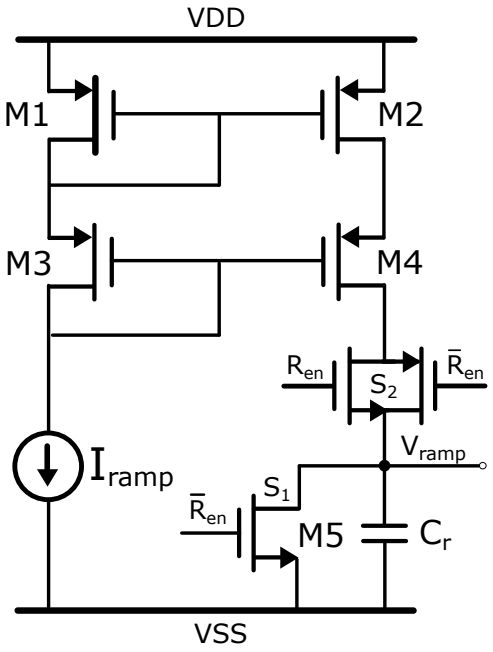


Figure 3.19: Schematic of the ramp generator.

variations and device mismatch will however change the value of the charge current. This is taken into account and will be dealt with by adjusting the ring oscillator frequency (increasing or decreasing its supply voltage) in the time to digital converter.

3.4 Time to Digital Converter

Since the analogue to digital conversion of the single slope asynchronous ADC starts by the conversion of an input voltage to a corresponding pulse width modulated signal, a time to digital converter is required to quantize the signal. In our design a dual-step time to digital conversion approach, discussed in section 2.4.3 was chosen. It consists of a 6-bit counter, clocked by a ring oscillator that makes the coarse time measurements and a 4-bit delay based TDC that measures the fine time intervals within a clock cycle. Figure 3.20 shows the circuit implementation of the two step TDC. Since the incoming V_{pulse} signal pulse widths are not necessarily a time multiple of the ring oscillator clock, there will exist a time portion of V_{pulse} that cannot be quantized by the counter. The residual portion of V_{pulse}, which is present within the oscillator can be measured by capturing, into registers, the values at the output of each unit buffer stage as shown

in figure 3.20 at the end of each pulse. The delay of the unit buffer represents the LSB of the TDC. These values present themselves as a thermometer code and have to be passed through a binary encode. The results from the coarse time TDC (MSBs) and the fine time TDC (LSBs) are combined together to form the digital representation of the analogue signal. The V_{pulse} signal is passed through a delay block (matched with the binary encoder delay) to generate the ready signal (active low), marking the end of conversion.

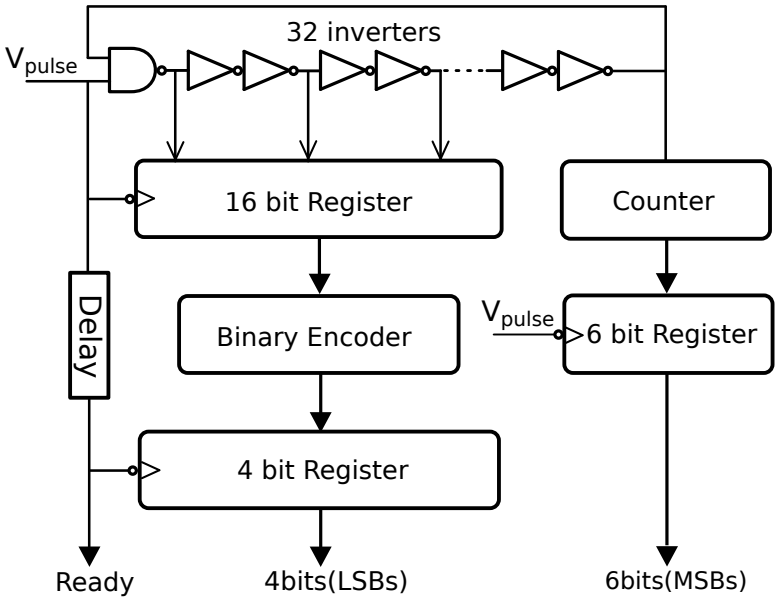


Figure 3.20: Two step time to digital converter. The counter mesures the coarse time while the fine time information is obtained from taps at the output of each unit delay cell.

In order to obtain a 4-bit value from the fine time TDC, the oscillator must have 2^4 unit buffers and a single inverter. In this design, the ring oscillator consists of 32 inverters together with a NAND gate as shown in figure 3.20 . The ring oscillator generates a clock signal which should be able to provide a full range count of 2^6 within the linear operating region of the ramp generator. For the 0.35μm technology used, at a voltage of 1V (voltage just above the threshold voltage of the transistors to minimize power), the ring oscillator provides a clock of period $109ns$. This will ensure that the full range count takes the same time as the time the ramp rises to its maximum value, to complete its count. It should be noted that in our design, the oscillator has a tuneable

voltage supply that can be varied to counter the changes in the clock frequency as a result of process and temperature variations after chip fabrication.

3.5 Asynchronous Digital Control

The desired operation of the ADC shown by the waveform diagram in figure 3.21 can be used to deduce a signal flow diagram that represents the functional control steps required for operation.

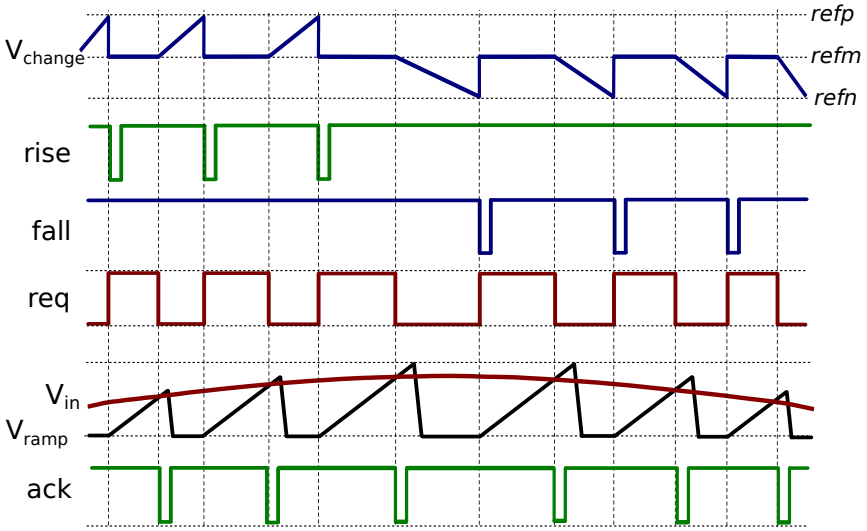


Figure 3.21: The desired operation of the ADC

It can be seen that there are two mutually exclusive events (rise and fall) that trigger the beginning of A-D conversion. It can also be seen that once a conversion has been triggered by either a rise or fall event, the ADC conversion process remains similar for either of the events. We therefore require a controller that can capture the two events and generate the necessary signals that control the slope detector, ramp generator and the time to digital converter. Since the mode of conversion involves the use of a comparator to detect when the ramp signal rises above the input signal, its output signifies the end of conversion. The controller can use this output to enable the slope detector and disable the ramp generator by resetting to and holding it at zero. This sequence of events can be modelled by a Signal Transition Graph (STG) [43] as shown in figure 3.22.

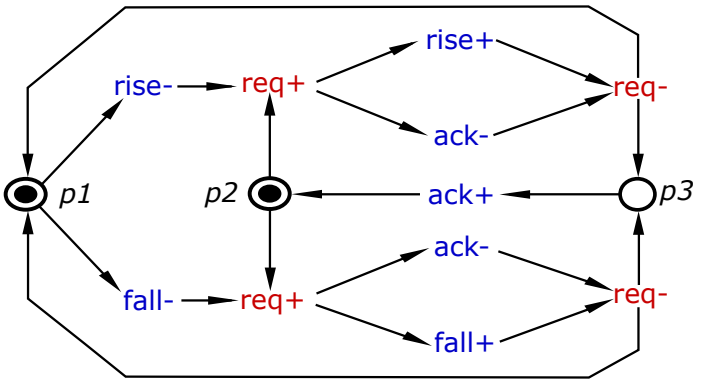


Figure 3.22: Signal Transition Graph deduced from the ADC operation described by figure 3.21. All signals execpt **req** are inputs.

When the input signal change goes beyond the threshold window, the slope detector generates either the rise or fall signals (active low). These signals are captured by the controller and used to fire a token from its initial position *p1* in effect causing the request signal req to be raised high. At this point the controller has to check if the acknowledgment signal ack from the comparator is high and if so then the token at *p2* will be fired resulting in the signal rise/fall to be pulled back high. Once the ramp voltage surpasses the input signals voltage, the comparator will pull the ack signal low. At this point the controller will fire tokens to pull req low, as a result of rise/fall being pulled high and ack low. Immediately this is done, ack will be pulled back high thereby marking the end of the A-D conversion. This STG model was used to synthesize the combinational circuit of the controller in figure 3.23 using Workcraft EDA tool [64], and simulated using a SPICE simulator to verify its operation. From the circuit it can be seen that the req signal is the same signal that controls the ramp generator, slope detector and is the time encoded value representing the analogue signal that is passed on to the time to digital converter.

3.6 Complete Design and simulation Results

The ADC was designed and implemented on a 0.35μm CMOS AMS technology, using Cadence IC tool set. Figure 3.24 shows the complete circuit diagram of the ADC. The slope detector capacitors were chosen to be C_1=C_2=250fF providing unity gain when the slope detector operates in the tracking phase. This will in turn require a small voltage window in order to detect a

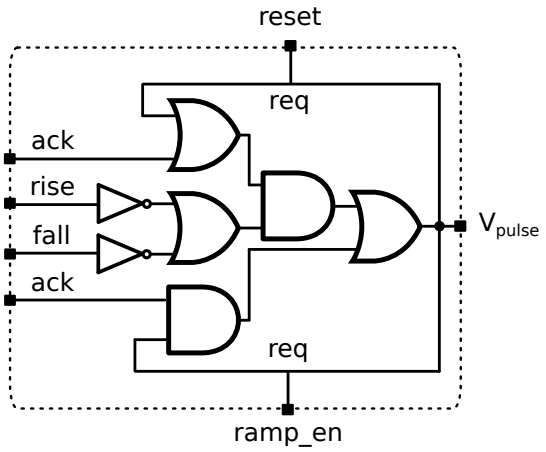


Figure 3.23: Asynchronous Controller generated from the STG in figure 3.22

small voltage change (A window of 40mV, 20mV above and 20mV below the midpoint). With a chosen midpoint, refm of 1V, refp and refn become 1.02V and 0.98V respectively.

The analogue circuits (including the asynchronous controller) were powered at a supply voltage of 2.6V while the time to digital converter was powered at 1V. To ascertain the operation of the ADC, simulations were performed to observe the ADC's power consumption and its dynamic characteristics. For a pure tone to 2 kHz sinusoidal input signal of amplitude $1V_{pp}$, the ADC's total power consumption was 30μW. The analogue circuits consumed 26μW while the time to digital converter consumed 4μW. The non-uniformly spaced samples from the time to digital converter were recorded together with their time stamps and later on applied to a reconstruction zero order hold DAC. The resulting continuous time signal was resampled at a uniform fixed sampling rate for the purpose of deriving the signal's power spectrum. A 1024 point FFT was computed from the resulting samples in Matlab giving the power spectrum shown in figure 3.25. It should be noted that the FFT was computed directly on the reconstructed signal from the DAC without post processing.

The analogue input signal was varied from 2 kHz to 20 kHz in steps of 2 kHz and the resulting ADC outputs reconstructed. The Signal to Noise and Distortion Ratio (SNDR) was calculated for each step frequency and plotted as shown in figure 3.26 with the peak SNDR recorded as 39.56dB. It can be seen that the SNDR reduces as the signal's input frequency is increased. This is due to the fact that an increase in frequency will result in fewer samples being obtained for

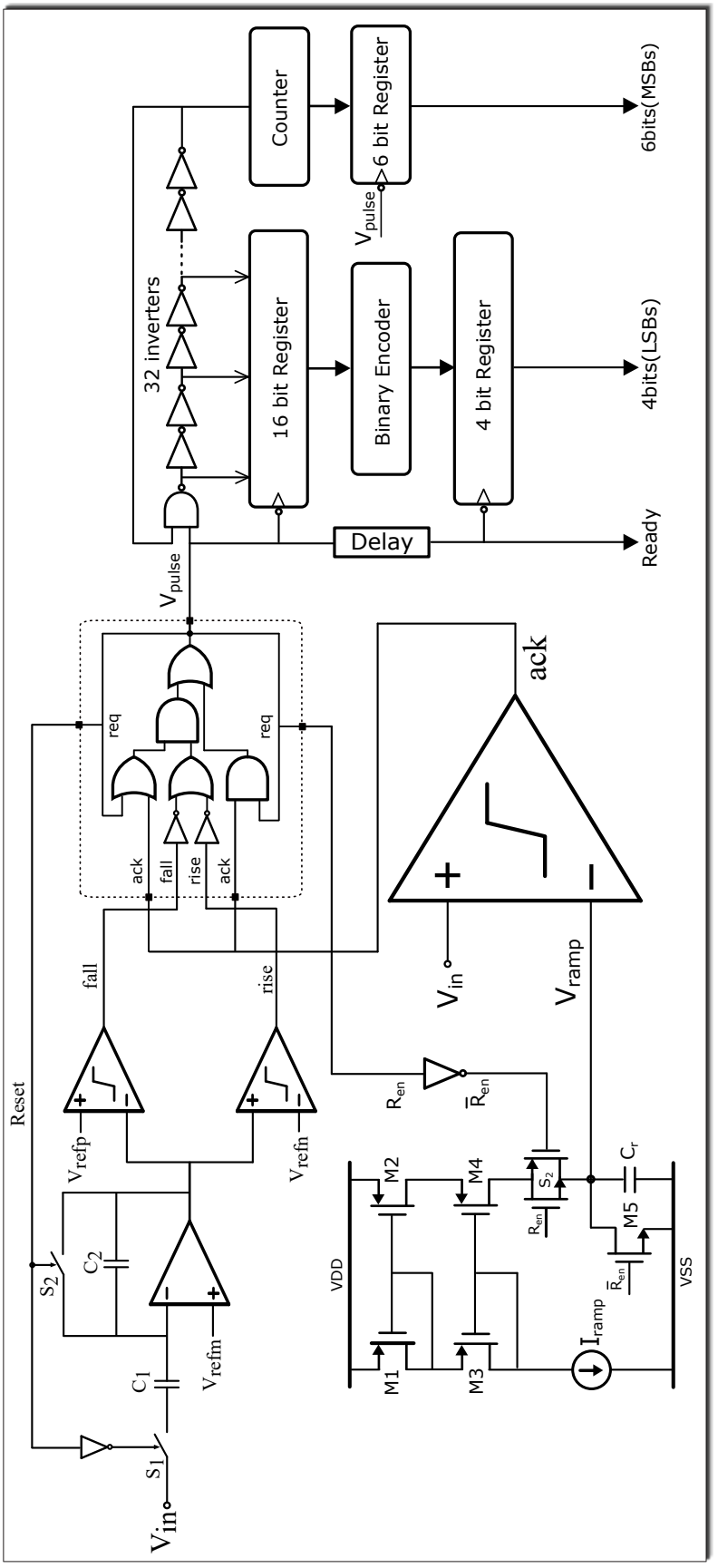


Figure 3.24: Complete schematic of the Single Slope Level Crossing Asynchronous ADC

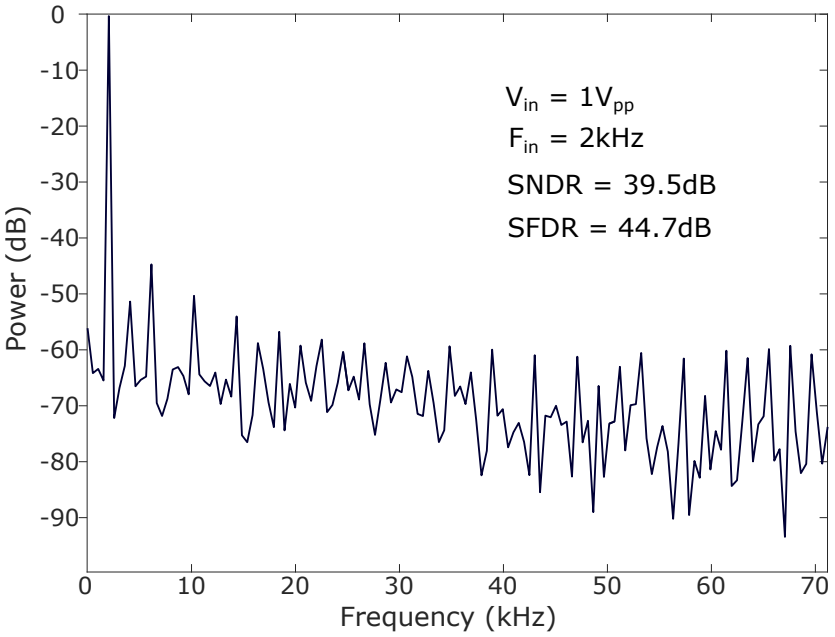


Figure 3.25: Power spectrum of the ADC's output for a pure tone sine wave signal input.

each signal cycle. The figure of merit of the ADC was calculated using equation 3.8 and found to be 2.4pJ per conversion.

$$FOM = \frac{Power}{2^{ENOB} \times 2 \times BW} \tag{3.8}$$

The power consumption results from the simulations were obtained with the assumption that an input signal is of a fixed frequency over time. For a signal with multiple frequency components the power consumption will continuously vary over time. This is due to the fact that the ADC will only consume dynamic power when it evaluates a samples asynchronously. When the signal is not changing past the set voltage window then the ADC only consumes static power as a result of the analogue circuitry. Its instantaneous power consumption will therefore have a profile similar to the signal rate of change profile. This power consumption characteristic of the ADC can be seen in figure 3.27 where a speech signal was passed as its input. Different signals will have different power consumption profiles.

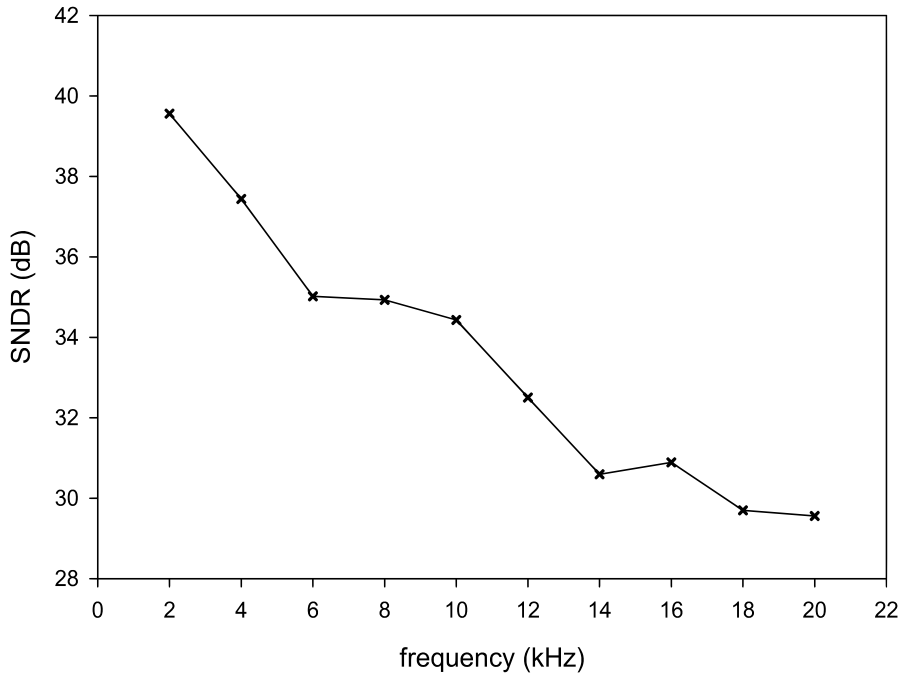


Figure 3.26: Signal to Noise and Distortion Ratio .

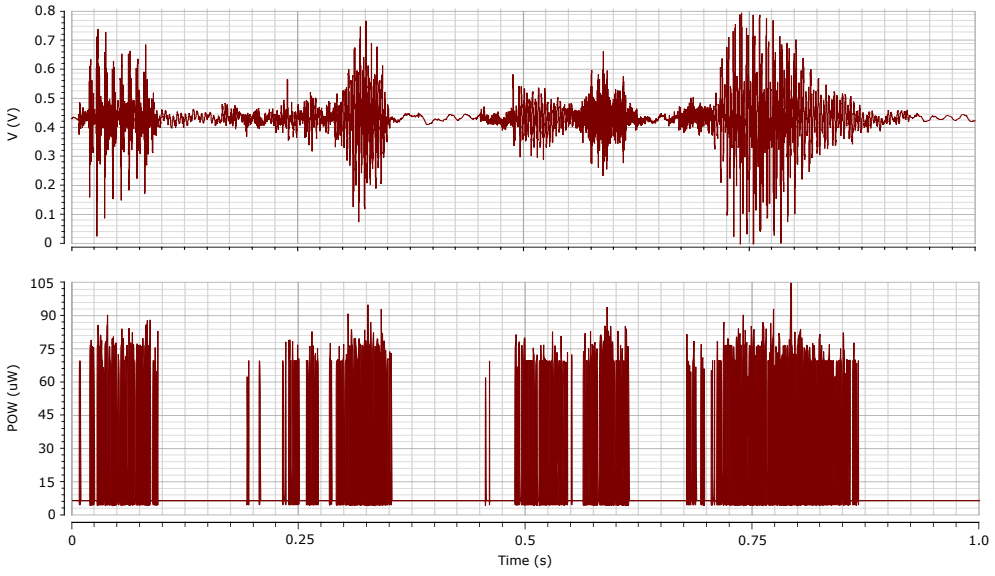


Figure 3.27: Power consumption profile of the AADC for a speech signal input.

Chapter 4

Event driven burst mode digital signal processing

4.1 Asynchronous Signal Processing

In the chapter 3, a new type of asynchronous A-D converter was presented and was shown (as can be seen in figure 3.27) to consume power only when the signal is changing above or bellow set voltage threshold levels. It obtained asynchronously sampled analogue samples and converted them into their digital representation using the Time to Digital Converter. The resulting samples are presented without any timing information i.e the distance in time between two adjacent samples is not provided. Since most digital signal processing algorithms operate in discrete time i.e on synchronously sampled signals which exhibit a constant time period between two adjacent samples, they cannot be directly applied to asynchronously sampled signals. In order to process the irregularly spaced samples obtained from the asynchronous A-D converter, other algorithms operating in continuous time should be used.

In this chapter an overview of Uniformly spaced Discrete time Digital Signal Processing and Continuous time Digital Signal Processing (available in literature) will be presented with their similarities and differences discussed. Section 4.1.3 will present a digital signal processing technique that is event driven and operates in short bursts when a sample is made available to it.

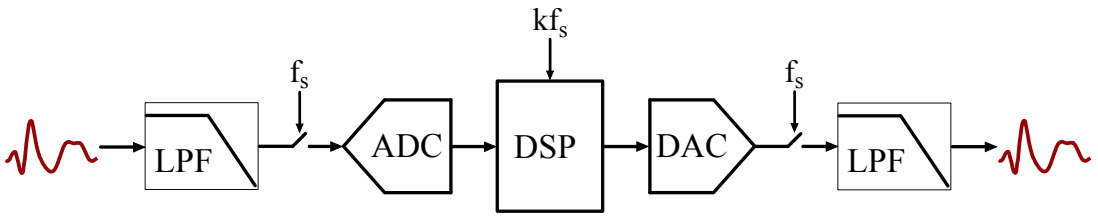


Figure 4.1: Synchronous Sampled data System. A clock of period fs is used for sampling at the input of the ADC and output of the DAC while a scaled version kfs is used to drive signal processing in the DSP

The advantage of this technique to minimize dynamic power consumption during idle periods of time when there is no sample available will be explored in sections 4.1.2 and 4.1.3. In section 4.2 a burst mode power gated asynchronous FIR filter that is able to switch itself off when it has no new samples to process will be presented. The method of preforming the power shutdown and the design procedure of the power shutoff cells will be discussed. The chapter will be concluded by presenting the description of the physical implementation methodology employed in realizing a mixed signal system consisting of the asynchronous A-D converter and the burst mode power gated asynchronous FIR filter.

4.1.1 Uniformly spaced Discrete time Digital Signal Processing

Uniformly spaced discrete time signal processing is the most common and conventional method of executing digital signal processing algorithms on uniformly spaced discrete amplitude sampled. Figure 4.1 shows a typical uniformly spaced discrete time digital processing pipeline that consists of a digital signal processor core (such as a digital filter), ADC and a DAC. It can be seen that all of these block require a constantly running clock of the same frequency or integer multiple of a base frequency in order to ensure that all the signal that pass through them are operated on correctly.

In this type of digital signal processing the DSP sub-blocks are always continuously triggered at a set time interval i.e the ADC is always sampling and the sampled signals are always being processed regardless of the signal's rate of change. Due to this constant sampling and processing rate, slower signals will result in an unnecessarily large number of calculations in the DSP than

is required. This inability of the system to adapt itself to the signals rate of change will result in unnecessary power consumption for signals that exhibit periods of inactivity intermittently.

4.1.2 Continuous time Digital Signal Processing

Continuous time digital signal processing, first proposed in [65] [66] , is a relatively new technique of processing sampled digital signals. It involves the processing of discrete in amplitude, but continuous in time signals without requiring a constant frequency clock. This will enable the system to perform operations on the signal at any given point in time and will therefore make it possible for the processing of asynchronous samples. If these samples are obtained from a Level Crossing ADC as discussed in section 3.1, then it follows that the digital signal processing block will also exhibit a signal dependent power consumption profile.

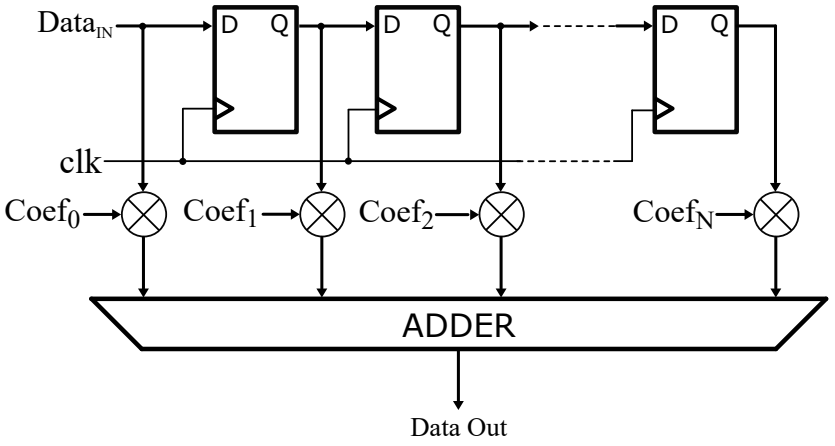


Figure 4.2: Synchronous FIR filter. Multiplication of the data and coeficients are performed during each clock cycle regardles of the signals rate of change. Its operation is sumarised by the convolution equation 4.1

$$\sum_{k=0}^{N-1} Coef(k)Data(n-k), \tag{4.1}$$

where $Coef(k)$ *are the filter coefficient and* $Data(n-k)$ *the sampled input data*

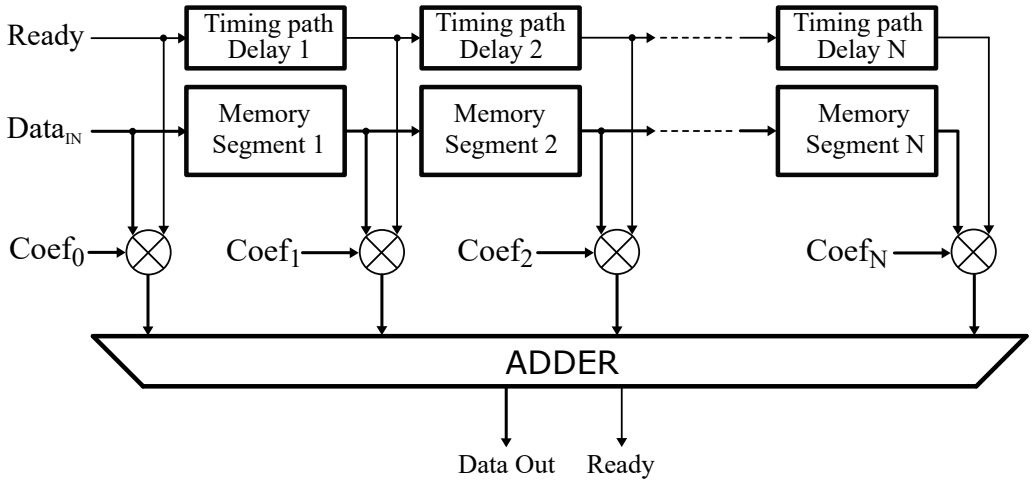


Figure 4.3: Continous time asynchronous FIR filter presented in [67], [29], [61]. The clock is replaced by a segemnted timing path consisting of propagation delay blocks. The ready signal pulse triggers calculations each time it reaches the end of a delay segment.

The architectural structure of a continuous time FIR filter closely resembles that of a discrete time FIR filter as illustrated in figure 4.2 and figure 4.3 . It can be seen that for the continuous time FIR filter implementation, shown in figure 4.3 , the D flip flops of the discrete time FIR filter have been replaced by continuous time delay blocks. These delay blocks consists of a memory element for storing the input samples and a delay line for passing the timing information. Since there is no clock to control the movement of data through the delay elements, the timing information represented by a short pulse of the ready signal through the delay line, will be used to trigger the propagation of a sample through the memory elements when a signal change is detected. In order to obtain correct results that would be obtained by a discrete time filter (satisfying the convolution equation 4.1), the delay encountered by the pulse on the delay line of each stage should be identical. The timing pulse is also used to trigger the calculations in the multipliers and adders as it passes each filter tap. When the input signal is not changing and no new samples are generated, the previous samples that were present in the memory elements will continue to propagate together with the timing pulse until the last sample that was obtained reaches the end of the delay block. At this point no more operations will occur and henceforth no logic switching. The system will remain in this state until a change in the sampled signal is observed. In addition to this it should also be noted that a signal with low rate of activity will

results in lower power consumption due to its lower sample rate as compared to a high activity signal.

The continuous time FIR filter representation given in figure 4.3 shows a generic way of implementing the delay blocks for the timing and data paths. In [29] and [61], the memory element and the delay lines are implemented in the same way, as a propagation delay buffer. This implies that the timing pulse together with the input data should propagated through the delay buffer with the input data arriving at each filter tap slightly earlier than the timing pulse. Controlling these delay buffers to achieve the required timing conditions for proper operation of the system is quite difficult due to process, voltage and temperature variations. In addition to this problem, there is a huge area and power overhead associated with the huge delay buffers. For the implementations in [61] the delay buffer block constituted more than two times the size of all the digital and analogue blocks combined, while in [29] it constituted about the same size as the total size of all the other circuits within the design. It is also worth noting that these implementations used a 1 bit data input. This makes these approaches non scalable in multi bit design cases. In [67] the propagation delay blocks of the data path were replaced by multiple static random access memory (SRAM) blocks ,one block for each tap, that hold the samples when the signal processing calculations are being performed. This was done in order to reduce the large area that was previously required for the implementation of the propagation delay buffers of the data path. The SRAM blocks were designed to support concurrent read and write operations for the sample entering, and leaving an FIR filter tap stage. Since the samples coming into and leaving the SRAM block are non-uniformly spaced, the control signals related to the read and write operations have to be properly designed. If this is not done timing violations, with respect to the timing pulse obtained from the timing path, will result. It should be noted that the timing path still requires a propagation delay line to ensure that the data is read from the data memory blocks at the right time. Although in this approach there is no requirement for matching the delay of the data path to that of the timing path, there is still the requirement of ensuring that the delay on the timing path of each FIR filter stage should be identical. This necessitates the need to build multiple tuning circuits that should be able to detect delay variations (after fabrication) in the timing path delay of each stage and adjust the delays independently until they match as was done in [67]. These tuning circuitry adds unnecessary complexities to the FIR filter as well

as increasing its overall area. In the continuous time digital signal processing FIR filter implementations discussed in this section, the filter taps are taken at the end of each delay line before being multiplied and added together. Since the delay blocks on the timing paths are designed to have the same delay, if equally spaced samples were given as the input, then the FIR filter's operation would be similar to that of a conventional synchronous FIR filter provided that the samples spacing is equal to the propagation delay of the delay block. The structure should be able to achieve the convolution function with the constant sampling period of the synchronous FIR filter replaced with the time delay of the delay block as shown in equation 4.2. It should be noted that in order to satisfy the nyquist criteria the delay time T_d should be equal to, or less than the inverse of two times the highest frequency component of the input signal.

$$\begin{aligned} 2F_s &\geq 2F_0, \\ \frac{1}{F_s} &\leq \frac{1}{2F_0}, \\ T_d &\leq \frac{1}{2F_0}, \end{aligned} \tag{4.2}$$

Assuming a single sample was fed to the filter, then it would travel through the filter stages with its request pulse triggering the multiplication and addition operations as it passes each filter tap point. This means that the results from the filter will be obtained after every time delay T_d of a delay line. On the other hand if multiple samples are fed to the filter, then each time a request pulse (corresponding to a sample) is detected at any of the filter taps the multiplication and addition operations have to be performed.

4.1.3 Event Driven burst mode Digital Signal Processing

The main pitfall of the discussed methods of non uniformly spaced samples signal processing is that in order to maintain the validity of equation 4.2 a lot of large delay structures (covering upto 70% of the design area as reported in [61]) and complex control circuitry are required in cases where the delay in the data path are implemented using SRAM blocks. These added circuitry will pose a detrimental effect in terms of increased power consumption through both circuit switching and circuit current leakage as was reported in [29] where the delay blocks

consume 83% of the total digital power at 1*Khz* signal input and 19% at 22*Khz* signal input. It should also be noted that as these approaches reduce dynamic power consumption, they do not address the leakage power consumption during the idle period when there are no samples to process. Since the input samples obtained from an asynchronous ADC might be sparse in nature as a result of input signal inactivity, the system might spend a lot of time in the idle mode. As was discussed in section 4.1.2, the operation of the continuous time FIR filter was shown to resemble that of a conventional synchronous FIR filter that satisfies equation 4.1. The sampling time period in the synchronous FIR filter is replaced by the propagation delay time of the delay lines in its continuous time implementation. With this in mind we can observe that in order to gain the benefits of minimized circuit switching as a result of processing non-uniformly spaced samples, additional circuitry is added onto the synchronous FIR filter in order to transform it into a continuous time one. As was discussed in chapters 1 and 3, the target signals for these signal processing techniques occur in bursts i.e interchangeable periods of rapid signal activity and inactivity. We can therefore conclude that the basic principled desired for these system is for them to also operate in a burst mode manner with a switching activity profile similar to that of the signal. Instead of removing the clock from the synchronous FIR filter and adding additional circuitry to deal with timing, the synchronous FIR filter can be designed to operate in burst mode manner. In this configuration the FIR filter is enabled by the incoming bundled samples and is disabled once the sample has been operated on and there are no more incoming samples available. This would allow it to achieve the power consumption reduction due to minimized switching as the continuous time FIR filter. Since the clock will still be used there will be no need for the use of the large delay lines which require a large silicon area and unnecessarily consume energy due to leakage current while the circuit is in its idle mode. In the next section we will discuss a proposed design methodology, using an FIR filter as a test case, that has the potential of operating in a burst mode manner and henceforth minimizing its energy consumption.

4.2 Burst mode, power gated Asynchronous FIR filter design

Figure 4.4 shows a mixed signal design approach for an event driven system consisting of an asynchronous ADC and a power gated FIR filter. The ADC generates non uniformly spaced

samples together with a ready signal that provides the timing information of the samples. The ready signal is passed to an asynchronous control unit while the samples are fed directly to the FIR filter block. When a new sample is available from the ADC, the controller switches on the FIR filter power supply by closing the power shutoff switches and thereafter sending a request signal to the FIR filter. This will enable the FIR to perform its calculations after which it will generate an *ack* signal. The period between when the *req* and when the *ack* signals are generated should be equal to or less than half the time period of the input signal in order to satisfy the nyquist criterion. It should be noted that the FIR filter calculation must be completed within this period. This time period can either be generated by passing the *req* signal through a delay line or by using a clock generated by the receiver. If the delay line approach is chosen then the transfer of the results from the filter to the receiver must be synchronized. Once all samples have been operated on, the controller will power down the FIR filter as well as the delay line thereby minimizing power consumption due to current leakage.

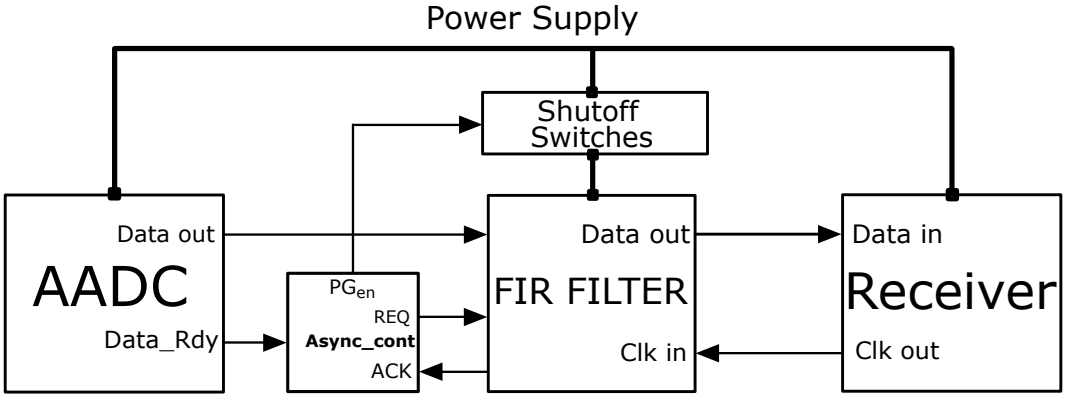


Figure 4.4: Non uniformly sampled mixed signal system consisting of an asynchronous ADC (AADC) and a power gated FIR filter.

4.2.1 Circuit Design

Figure 4.5 shows the eight tap circuit implementation of the FIR filter. It can be seen that the internal structure of the burst mode asynchronous FIR filter resembles that of its synchronous counterpart discussed in section 4.1.2. The main addition to this design is a power gating circuitry, a single delay line, two c-elements logic blocks used for handshaking and

an asynchronous controller. The asynchronous controller ensures that incoming samples are asynchronously processed on a global scope while the calculations local to the FIR filter are performed synchronously.

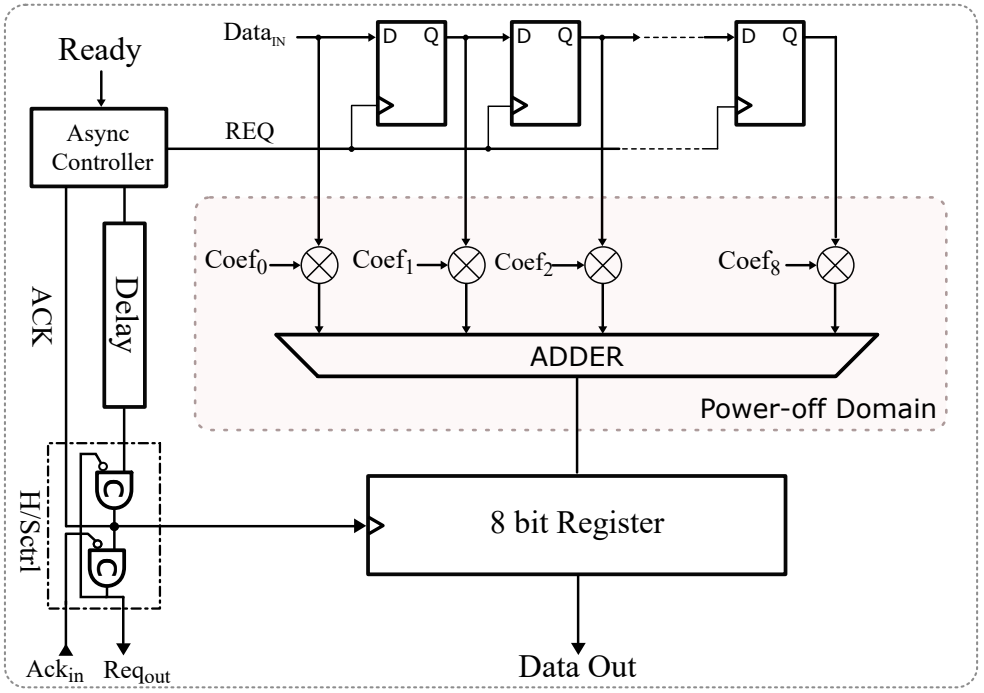


Figure 4.5: Burst mode, power gated Asynchronous FIR filter. The asynchronous controller ensures that incoming samples are asynchronously processed on a global scope while synchronous convolution calculations are made local to the FIR

In order to maintain the integrity of the results of an asynchronous FIR filter the convolution equation 4.1, which is based on discrete synchronous time calculations, must still be satisfied. Assuming a single sample together with a ready signal are made available at the input of the filter, a *req* signal will be generated by the controller and passed on to the registers which will in turn sample what values are available at their inputs. During this period the *req* signal is allowed to propagate through the delay line till it reaches the handshake controller *H/Sctrl*. If the receiver is ready to accept the output of the filter then an *ack* is sent back to the controller which will pull down the *req* signal thereby completing a 4 phase handshake protocol as described in 2.5.1. At this point in time after a single handshake cycle, if the filter is stopped then the FIR filter results based on equation 4.1 will be invalid. The controller must therefore continue performing more

handshake cycles until the number of handshake cycles equals the FIR filter number of taps as shown by the *req* in figure 4.6 a, for a 4 tap filter.

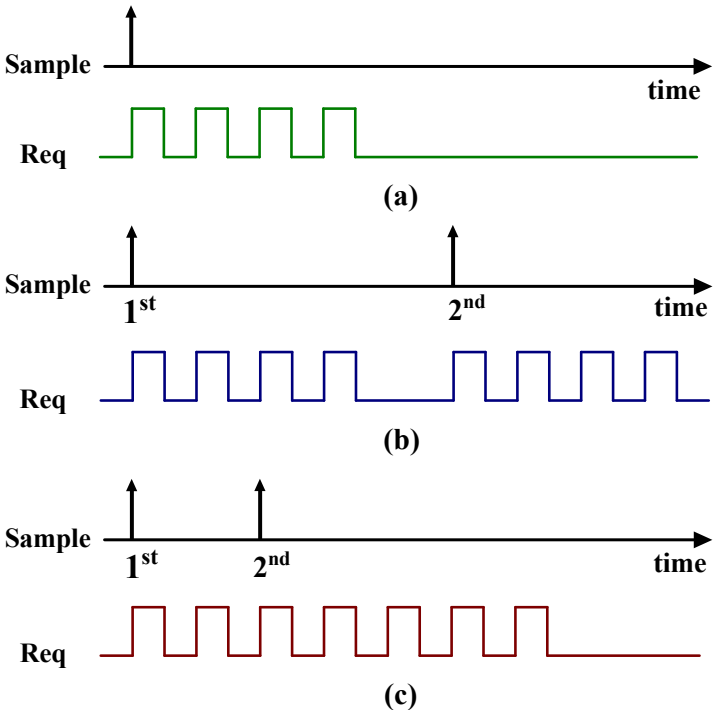


Figure 4.6: Asynchronous FIR filter controller operation for a 4 tap filter. **a)** For a single sample 4 handshake cycles are performed, **b)** For two samples with time period between them greater than 4 times of a handshake cycle, **c)** For two samples with time period between them lesser than 4 times of a handshake cycle.

This is to ensure that the single sample that was provided at the input propagates through each register. When the sample reaches the last register then all registers will have the same value. At this point in time the final value available at the results register will be held constant even if more handshakes are made. The filter can therefore be disabled and switched off in order to save power without affecting the validity of the results. It should be noted that the last sample must always be available at the input until when a new one is available. When multiple samples with time period spacing between two successive samples greater than 4 times the propagation delay of the delay line are applied at the input, the filter will operate in a similar manner as when a single sample is applied as shown in figure 4.6 b. However if the samples time period spacing is less than 4 times the propagation delay of the delay line then the controller has to reset and begin a new count down (from 4) of the number of handshake cycles each time a new sample is

received. This can be seen in figure 4.6 c where the controller performs 3 handshake cycles for the first sample, resets the count when a new sample is received and begins the generation of 4 new handshake cycles. Figure 4.7 shows the implementation of the controller. It consists of a counter used for keeping count of the handshake cycles, a condition test circuit (used to detect when the required count has been reached) and the handshake control circuitry. The counter has a single pulse generator circuit connected to its active low reset input. The generated pulse ensures that the counter is reset and begins a new count every time a falling edge of the ready signal RDY is detected as shown in figure 4.8.

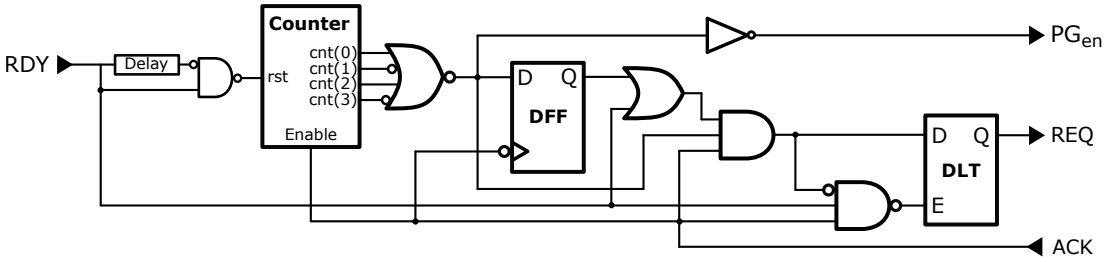


Figure 4.7: Asynchronous controller for the 8 tap FIR filter circuit shown in figure. The counter keeps track of the number of handshake cycles and is reset each time the falling edge of RDY is detected. 4.5

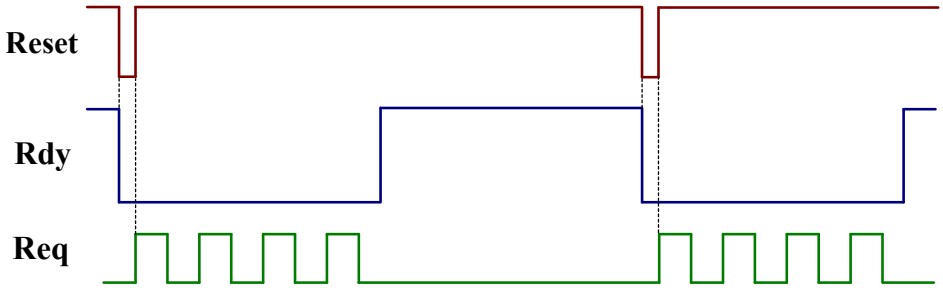


Figure 4.8: Asynchronous FIR filter controller operation showing the generated reset pulse and the handshake signal req.

In addition to the generation of the request signal that is fed to the registers and the delay line within the filter, the power gating shutoff signal PGen is also generated by the controller. This signal is fed to the power gating circuitry consisting of an array of power gating cells. Each individual cell consists of 2 PMOS transistor that acts as the power switch and a logic buffer, made up of two inverter, that is used to buffer the PGen signal though the cell shown in figure

4.9. The input signal to the PMOS transistor is given as the inverted version of PGen*in* and is obtained from the output of the first inverter. It is later on reverted back to its original state by the second inverter and thereafter passed on as the output signal PGen*out*. This output signal is connected to the PGen*in* of the next cell in the array forming a control chain that propagates through all power shutoff cells until it emerges at the output of the last cell in the chain.

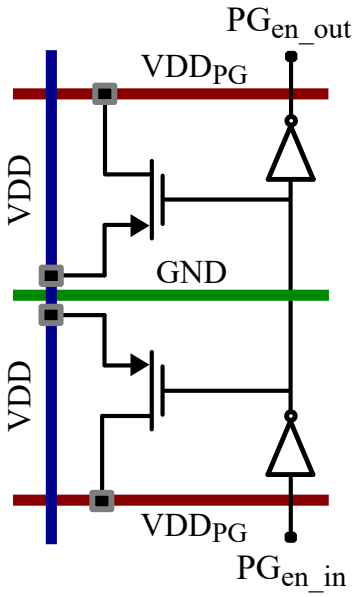


Figure 4.9: Power Shutoff Cell implementation using PMOS transistors. VDD is the always on power rail while VDD$_{PG}$ is the switched off power rail. PG$_{en-in}$ is the enable signal input port of the cell.

The power gating cell is designed for use in a grid style power cell insertion technique as shown in figure 4.10. This was chosen over the the ring implementation mainly due to the fact that the grid implementation requires fewer shutoff cells than the ring implementation to achieve the same IR drop target [48]. The power shutoff cell is twice the height of the digital standard cell height in the target technology and is implemented to have its control signal PGen connect back to back to form a control channel throughout the power gating cell array. It can also be seen in figure 4.10 that the power rail VDD is implemented such that a vertical power stripe will be created when the power cells are abutted together.

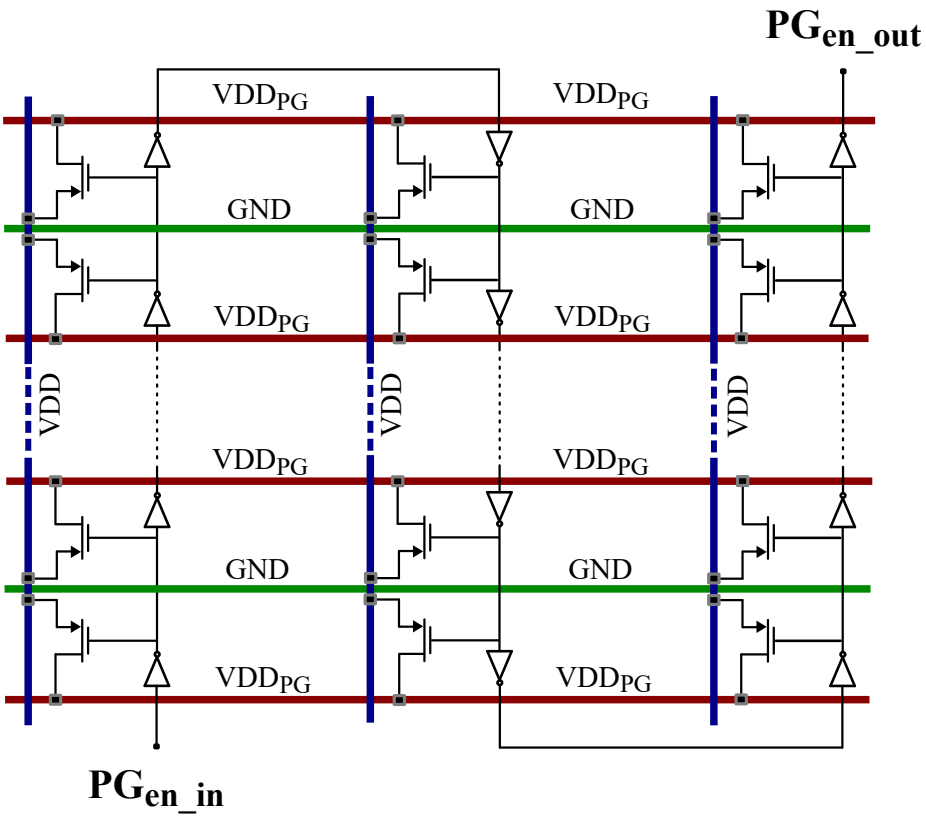


Figure 4.10: Grid style power gating cell insertion. Multiple power cells of the type shown in figure 4.9 are placed back to back allowing for the VDD, VDD$_{PG}$, PG$_{en-in}$ and PG$_{en-out}$ to connect by abutment.

Power Off transistor Design

The power shutoff transistors used in power gating cells can either be of the footer or header type i.e implemented using NMOS transistor to cut off the VSS supply or PMOS transistor to cut off VDD respectively. When choosing the desired power shutoff transistor type, the performance of the NMOS and PMOS must be considered in terms of their switch efficiencies, area efficiency and IR drop [48], [68].

The switch efficiency of a power gating transistor is defined as the ratio of the current it can supply during its ON period *Ion* to the current that leaks through it during its OFF period *Ioff*. The higher the ratio the more power efficient the transistor is. Since *Ion* current is the drain current of the power off transistor, any variation in the transistor length, width, substrate bias, temperature and other technology process parameters will result in different efficiency figures.

Of these variables, the length , width and substrate bias are the once that can be optimized during design to achieve an efficient power shutoff transistor. In order to determine which transistor type to choose and their respective optimal lengths and widths, a simulation was set up for measuring the ON and OFF currents for both NMOS and PMOS transistors. The PMOS source and gate terminals were connected to the power supply and its drain connected to ground. The length of the transistor was swept, while recording the drain current, from 0.35μm to 30μm with the width held constant at 0.35μm. The gate of the PMOS was thereafter connected to ground and the length swept again to obtain the drain current as a result of leakage when the transistor is off. The simulations were repeated with an NMOS transistor and the resulting currents used to compute the switching efficiency for varying gate lengths of the transistors. From the resulting plot shown in figure 4.11 it can be seen that the switching efficiency *Ion/Ioff* for the PMOS reduces as the gate length is increased. This is basically due to the fact that the

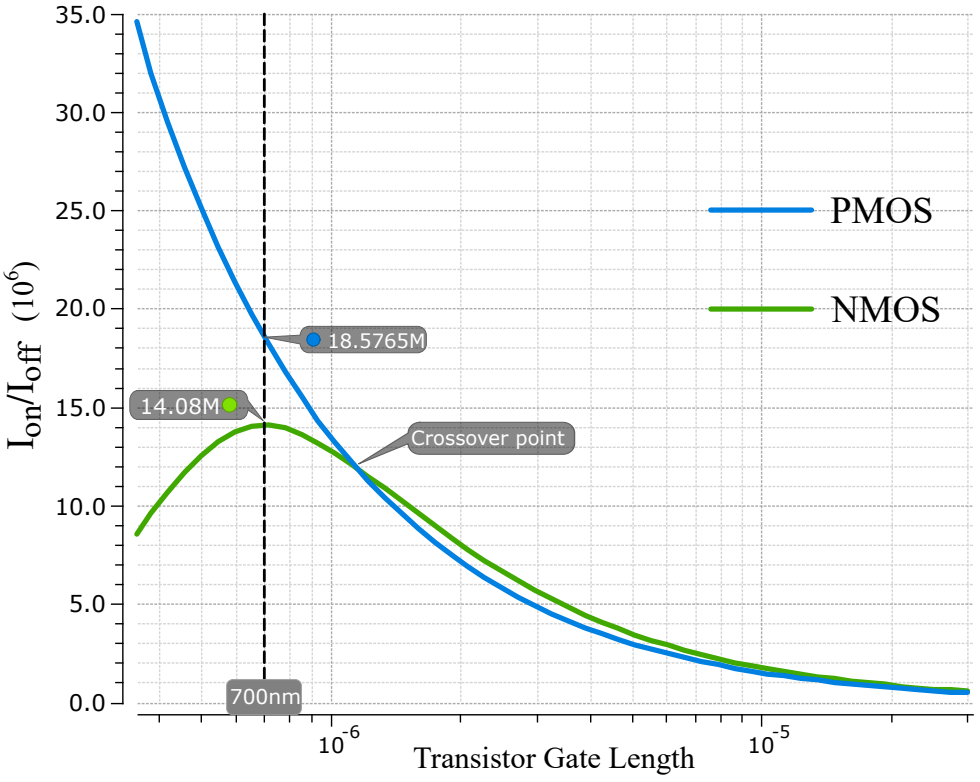


Figure 4.11: Sleep transistor power efficiency profile with increase in channel length. At gate lengths below 700*nm* the PMOS transistor is more power efficient than the NMOS transistor. Above 1μm, efficiency for both transistor become relatively similar and decrease almost at the same rate.

channel resistance increases with the increase in transistor length, leading to the reduction of *Ion* at a rate greater than the reduction of *Ioff*. The switching efficiency for the NMOS is much lower compared to that of the PMOS at shorter lengths. It starts by increasing as the length of the transistor is increased form 0.35μm and levels off at 14.08x10^6, at a length of 0.7μm. Increasing the length above this point results in the reduction of the switching efficiency up to a crossover point where it goes above that of the PMOS as shown in figure 4.11.

The described simulations were repeated for varying widths (0.35μm to 30μm) and a fixed length of 0.35μm. The *Ion* and *Ioff* were thereafter used to plot figure 4.12. It can be seen that the switching efficiency of the PMOS transistor is fairly constant as its width is increased. The switching efficiency of the NMOS on the other hand increases up to 9.18x10^6 at a width of 1.24μm as a result of the fringing effect of narrow gate width [69] that changes the threshold voltage of the transistor. After this point it begins to reduce until it levels off at about a width of 10μm.

From the results obtained from the simulations, it can be seen that the PMOS transistor offers better switching efficiency as compared to the NMOS. The optimal length for better switching efficiency is found to be 0.35μm when the PMOS transistor is picked. As for the width, it can be seen that the switching efficiency for the PMOS transistor is much greater than that of the NMOS i.e it is about 34.63x10^6 at 1.24μm where the NMOS switching efficiency is at its highest value of 9.18x10^6. With these results in mind, the PMOS transistor was picked for our design and sized to have a length of 0.35μm and a width of 15μm. As was described in 4.2.1 each power shutoff cell contains two PMOS transistor connected in parallel resulting in a combined width of 30μm. The resulting layout of the sleep transistor is shown in figure 4.13.

4.2.2 Physical Implementation

The complete mixed signal system consisting of, the Asynchronous Single slope Level Crossing ADC discussed in chapter 3 and the burst mode power gated Asynchronous FIR filter discussed in section 4.2, was implemented in the 350μm AMS technology. Figure 4.14 shows a block diagram of the integration of the two blocks. The asynchronous ADC, which had its implementation already given in chapter 3, receives the analogue signal through its input V_{in} and

produces the RDY signal together with the digital sample. These two output signals provide the only interface to the FIR filter. The physical layout of the Asynchronous ADC and its physical verifications (Layout verse schematic (LVS) and Design Rule Check (DRC)) were performed using Cadence Virtuoso set of tools. The resulting layout of the ADC was as shown in figure 4.15, covering an area of 340μm by 218μm. As was discussed in chapter 3 the ADC requires two power supplies i.e one for the analogue blocks (VDDA) and one for the digital blocks in the time to digital converters (VDD). This necessitated the creation of three power tracks (VDD, VDDA, VSS) going round the ADC to provide for good power distribution throughout the design as can be seen in figure 4.15. In this design a Digital On Top design methodology was chosen for system integration and therefore a Layout Exchange File (LEF) for the ADC was generated. The LEF file contains only the necessary pin connections that will be required for interfacing the ADC to the FIR filter. It also contains information that will inform the automatic

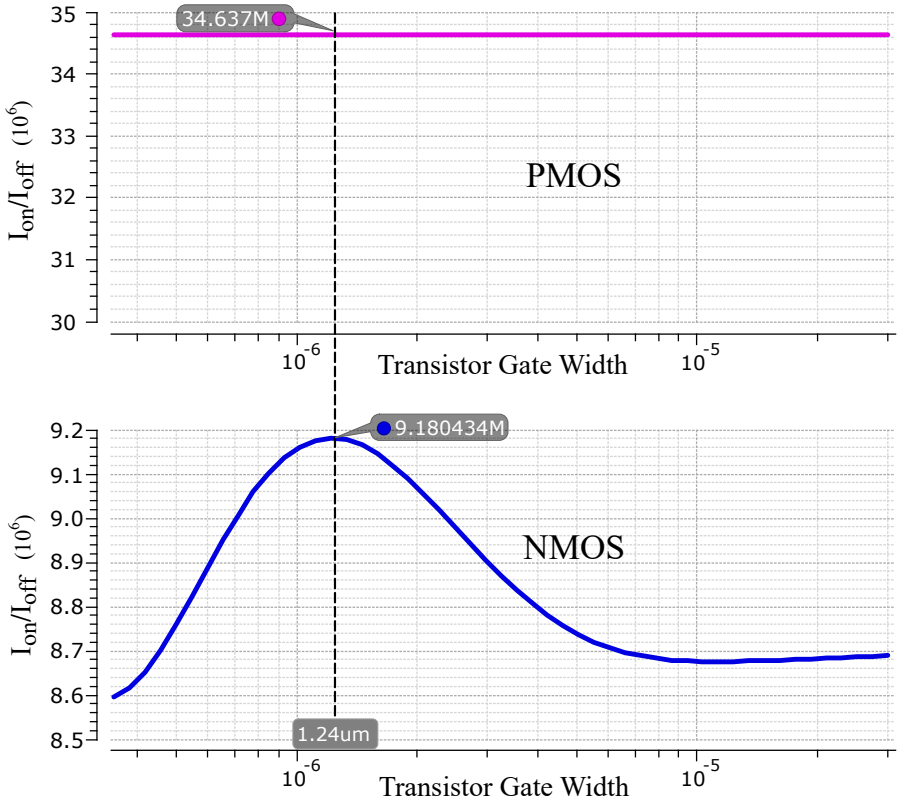


Figure 4.12: Sleep transistor power efficiency profile with increase in channel width. The power efficiency of the PMOS transistor is far much greater than that of the NMOS transistor for all widths.

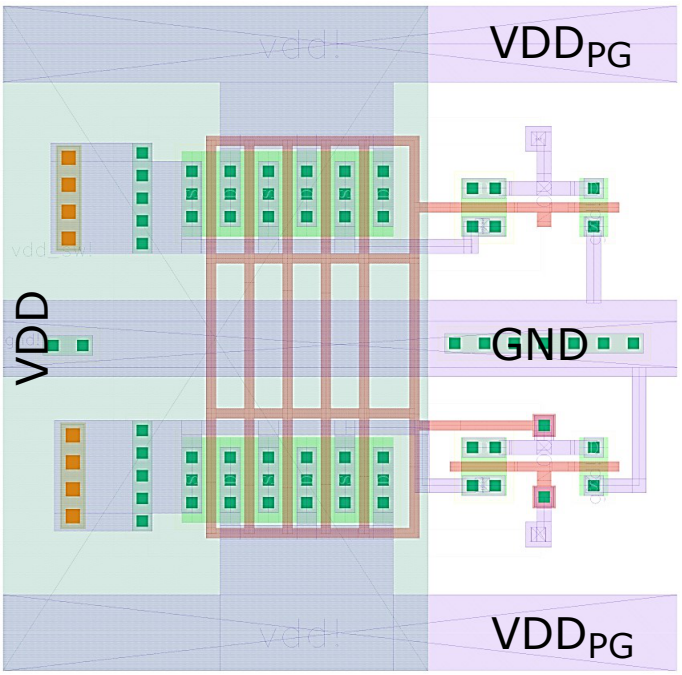


Figure 4.13: Power Shutoff Cell. The total width of the 2 PMOS transistors is 30μm and the whole cell covers an area of 23.8μm by 23.5μm

place and route tool on areas over the ADC layout where routing is prohibited.

The burst mode power gated Asynchronous FIR filter design was captured in VHDL at the RTL abstraction level. The resulting code was thereafter converted/synthesised into digital standard cells by using Synopsis Design Complier digital synthesis tool. Since the design has multiple power domain, a Common Power Format (CPF) file was created to describe the power domain connections and the power shut off cells voltage domain. A verilog top level netlist representing the circuit in figure 4.14, consisting of the synthesized FIR filter netlist and the single slope asynchronous ADC was created. The top level netlist, the ADC LEF, the digital standard cell LEF, the power shutoof cell LEF and the CPF file were passed as the main input files to the automatic place and route tool, Encounter Digital Implementation. Due to the presence of two power domains in the digital block i.e always ON VDD and switch-able VDD_{PG}, the asynchronous control and all registers were grouped together under the always ON supply VDD while the Multiplier and Adder were placed under the the VDD_{PG}. This grouping is described in the CPF file. During the floor and power planing steps in the place and route flow, three

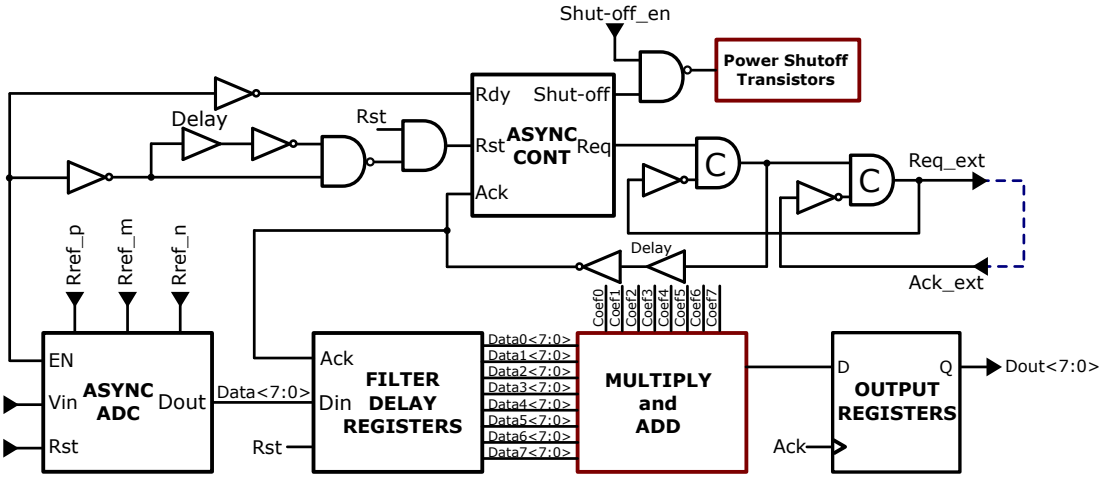


Figure 4.14: Event Driven Mixed Signal Data Acuisition and Processing System. The asynchronous single slope level crossing ADC provides the input data to the burst mode, power gated Asynchronous FIR filter. Only the Multiply and Add blocks belong to the power shutoof domain.

power rings (VDD, VSS, VDD_{PG}) were created around the digital blocks as can be seen in the resulting layout shown in figure 4.16. The power shutoff cells were inserted using the grid methodology discussed in section 4.2.1, forming four continuous vertical power strap which are further extended at both ends of each column and connected to the VDD ring. The power shutoof cells have their horizontal switch-able power supply rails connected to VDD_{PG} power ring as shown in figure 4.16. Once the FIR filter digital standard cells and the ADC macro block were placed in their respective partitions on the floorplan, the whole design was routed and the resulting metal routing tracks checked for connectivity. The final step in the design flow was the performing of the LVS and DRC physical verifications.

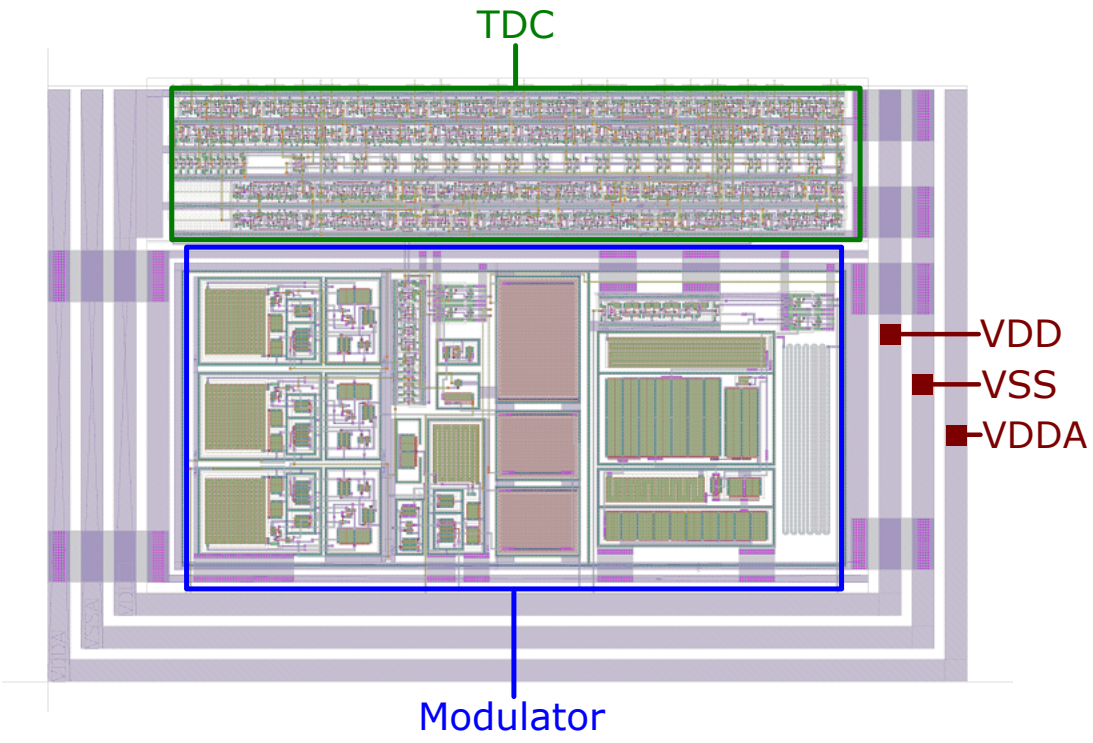


Figure 4.15: Single Slope Level Crossing Asynchronous ADC Layout. The design is implemented in a 350*nm* process and covers an area of 340μm by 218μm. The modulator consists of the slope detector, ramp generator, comparator and reference voltage generators.

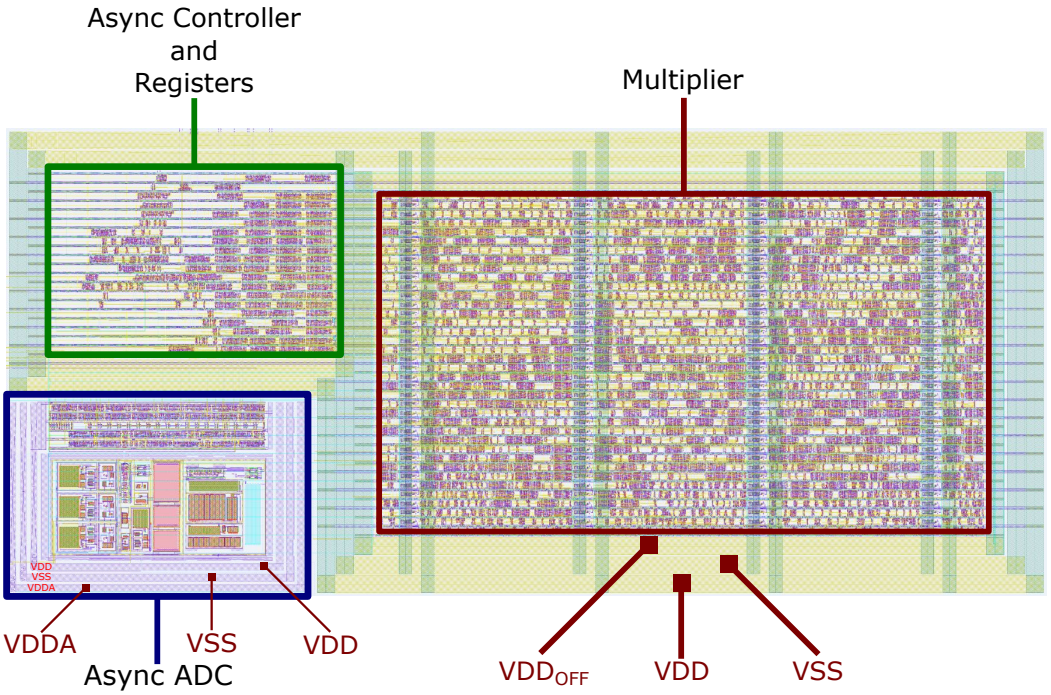


Figure 4.16: Mixed signal system layout consisting of the Asynchronous Single slope Level Crossing ADC 3.1 and the burst mode power gated Asynchronous FIR filter 4.5. The asynchronous control and all registers in the design are grouped together under the always ON supply VDD while the Multiplier and Adder are under the the switchable power VDD_{PG}

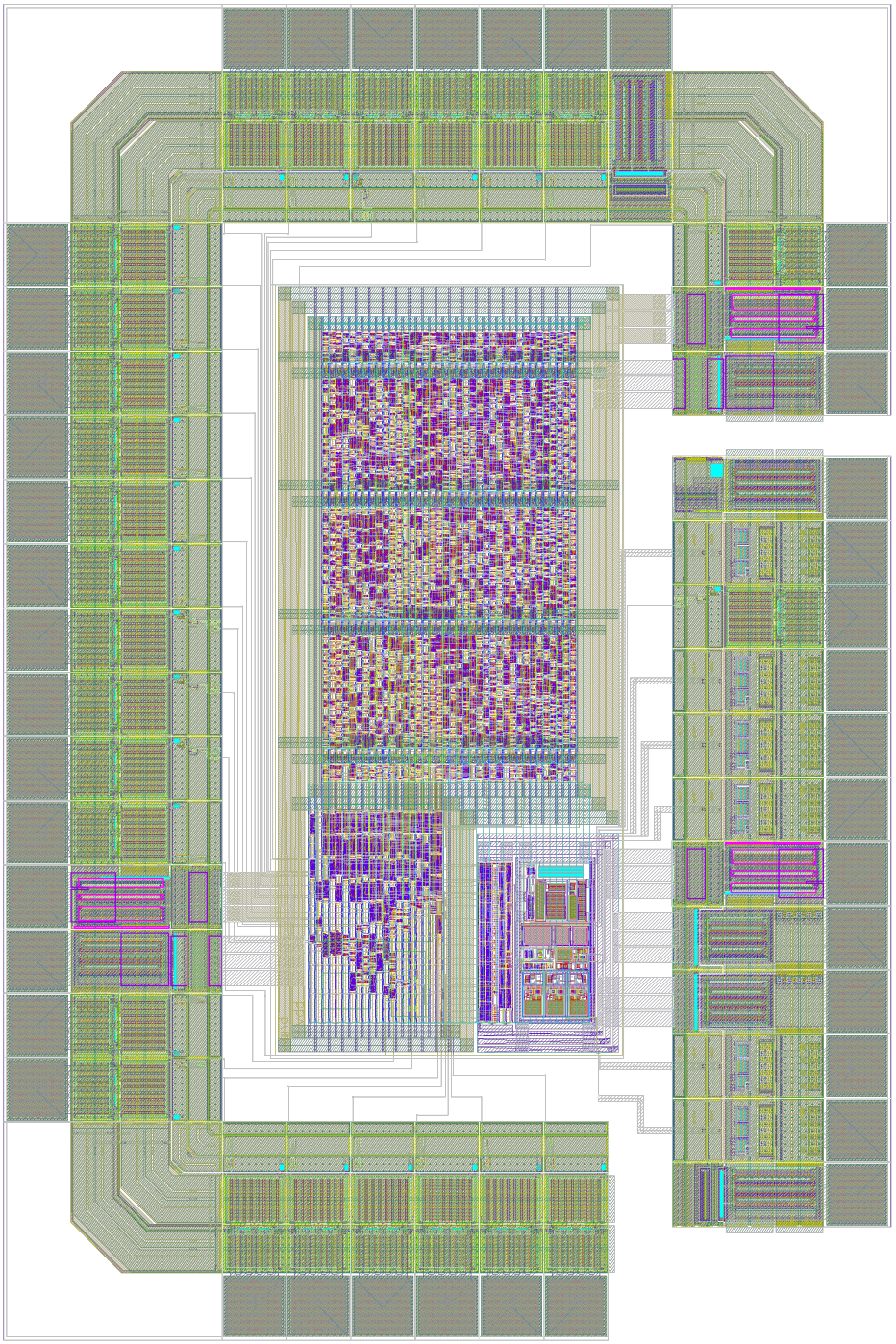


Figure 4.17: Complete design layout of the Asynchronous ADC, burst mode FIR filter, Input/Output cells and bonding pads.

Chapter 5

Experimental Results

The mixed signal system for asynchronous data acquisition and processing discussed in chapter 4 was fabricated in the AMS 0.35μm CMOS process technology. In this chapter the resulting test chip obtained is put under experimental tests to validate its operation and record data obtained from its operation. Section 5.1.1 of this chapter will begin by first presenting the micrograph of the fabricated test chip and denoting its active silicon area. The design of the PCB used for holding the chip during the testing will be briefly discussed after which the test bench setup will be presented. In section 5.2 the dynamic testing of the asynchronous ADC will be presented and the chapter concluded by performing power consumption tests in section 5.3.

5.1 Test Setup

5.1.1 Fabricated Chip

The die micrograph of the test chip can be seen in figures 5.1. It covers an total area of 2.4mm^2, 0.56mm^2 of which is covered by the FIR filter, 0.07mm^2 by the asynchronous ADC (shown in figure 5.2) and 1.77mm^2 by the input/output cells together with the bonding pads. The chip was packaged in a 68-pin J lead Plastic Leaded Chip Carriers (JLCC68).

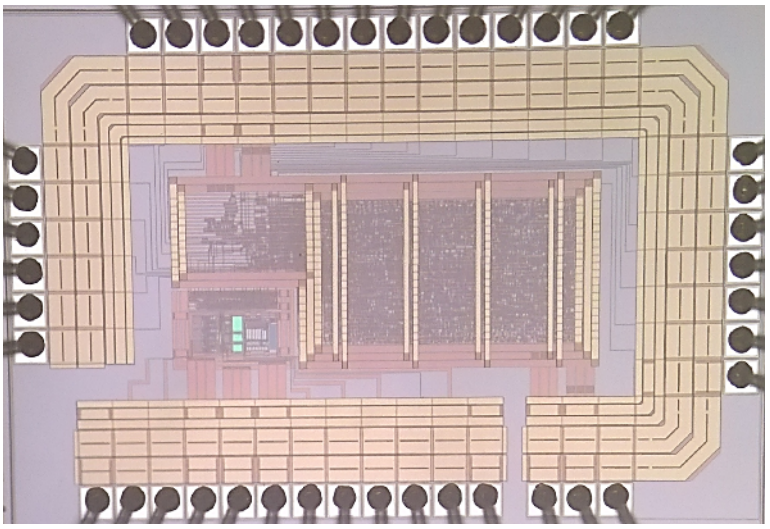


Figure 5.1: Test Chip Micrograph.

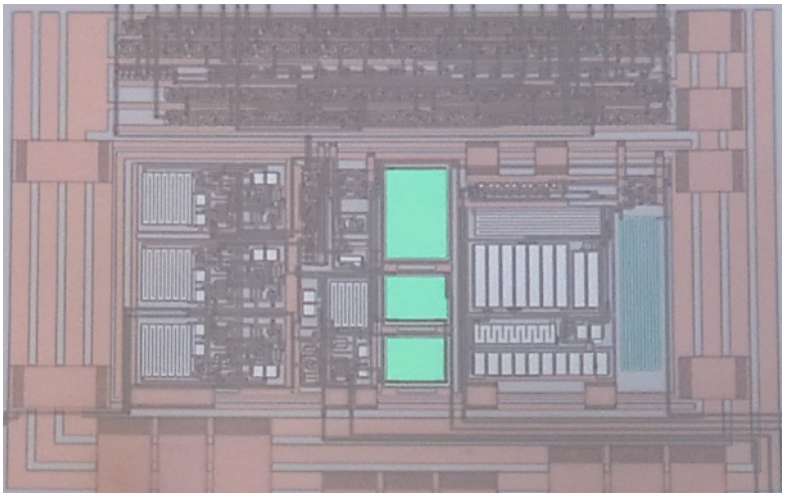


Figure 5.2: Event driven single slope level crossing asynchronous ADC micrograph.

5.1.2 Printed Circuit Board

A custom two layer printed circuit board (PCB), measuring 168.28*mm* by 125.60*mm* was designed and fabricated for use in the testing of the chip. The PCB was designed such that all the inputs and outputs together with the power supply ports of the test chip have corresponding connection points on the board. Both the data outputs of the ADC and the FIR filter were made available separately on the PCB. All the digital outputs from the test chip are passed through

buffer ICs that are used as level shifters. An array of switches were also made available on the board and were used to configure the design via internal multiplexers to use either internally or externally generated references as well as enable/disable power gating on the FIR filter. Figures 5.3 and 5.4 show the PCB layout and its corresponding photograph after fabrication.

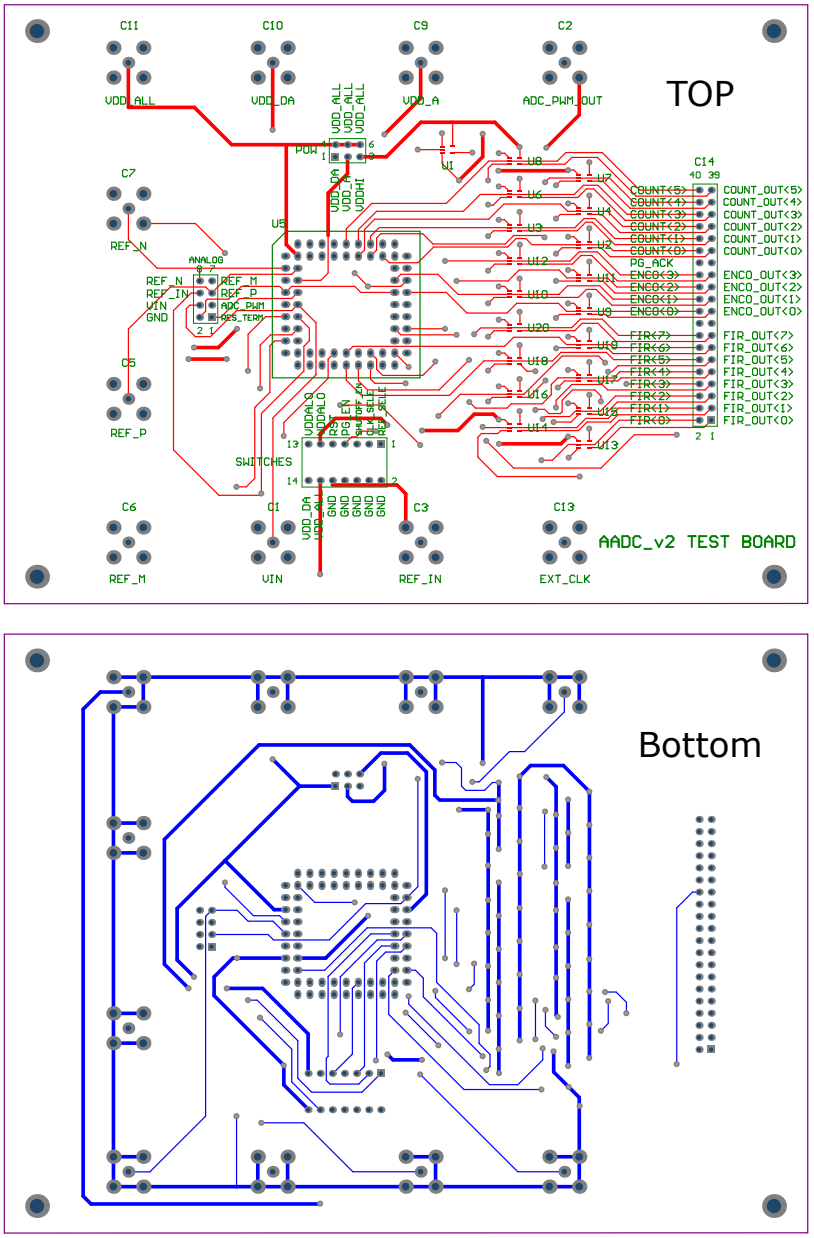


Figure 5.3: Test PCB layout

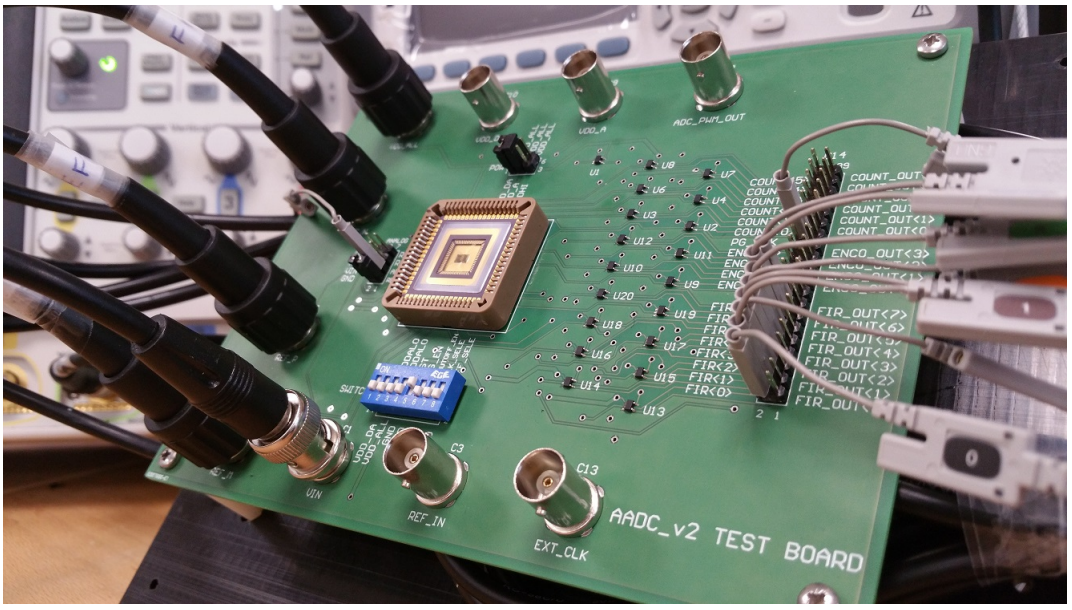


Figure 5.4: PCB board with the testchip mounted.

5.1.3 Equipment

Figure 5.5 shows the test setup configuration used in the experimental testing of the chip. The PCB is connected to a power supply source (Agilent Technologies N6705B), waveform generator (Keysight 33500B) and a logic analyser available on the Agilent Technologies MSO-X-4034A Mixed Signal Oscilloscope. The Agilent Technologies N6705B power supply provides both the digital voltage VDD (1.5V) and the analogue one VDDA (2.6V). It also provides the voltage references *refn*, *refm*, and *refp* required by the slope detector in the ADC. These reference voltages were set such that the level crossing voltage window obtained was $30mV$.

The Keysight 33500B waveform generator is used to generate the required waveforms used in the testing i.e a sine wave and ECG waveform. Both waveforms are generated to span 1V peak to peak which is the range accommodated by the ADC.

The Agilent MSO-X-4034A Mixed Signal Oscilloscope contains a logic analyzer that is used in recording the digital information generated by the test chip. The resulting digital waveforms captured are thereafter imported onto a computer for analysis.

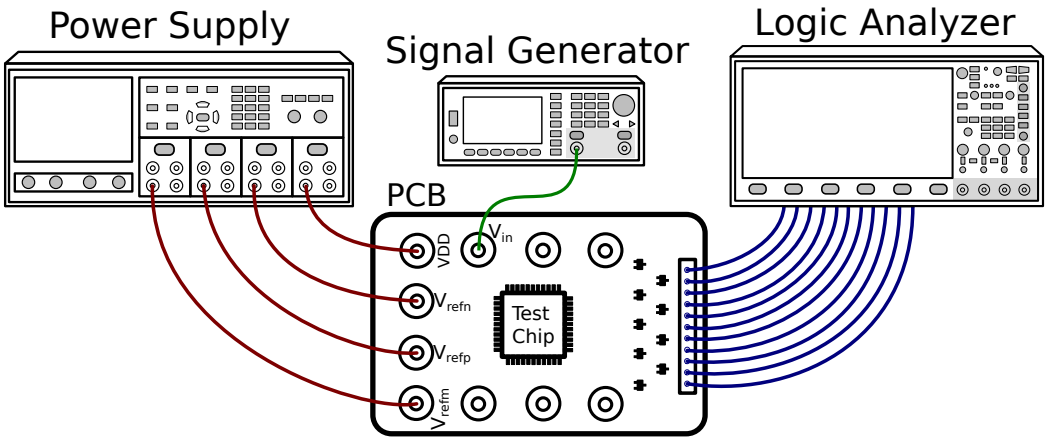


Figure 5.5: Test Setup. The PCB is connected to a power supply (Agilent N6705B) that provides the power and voltage references required by the test chip, a waveform generator (Keysight 33500B) and a logic analyser(Agilent MSO-X-4034A).

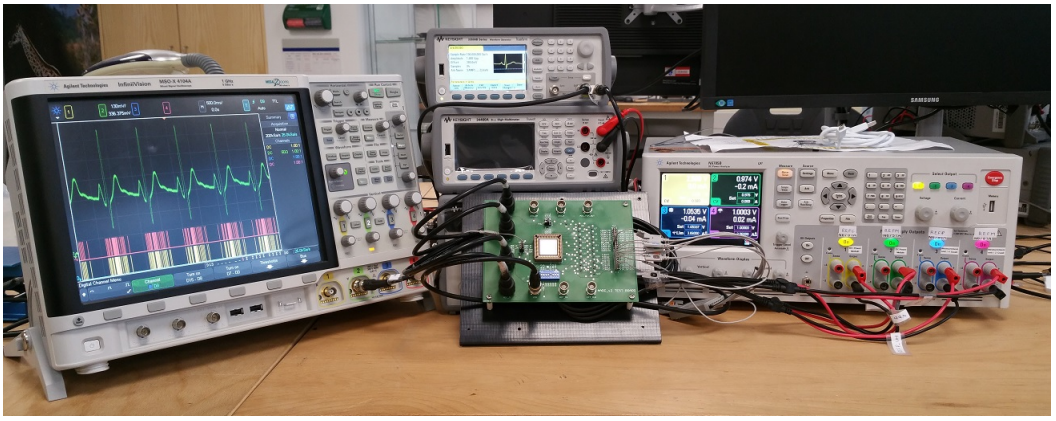


Figure 5.6: Picture of the test setup.

5.2 Dynamic Testing

The waveform generator was configured to output a sine wave of 1V peak to peak at 16kHz. The resulting digital signal generated by the test chip was captured by the logic analyzer an imported onto a computer. In order to perform frequency analysis on the signal using conventional methods, zero order hold interpolation was performed to aid in the reconstruction of the signal. A 1024 point Fast Fourier Transform (FFT) was performed on the reconstructed signal

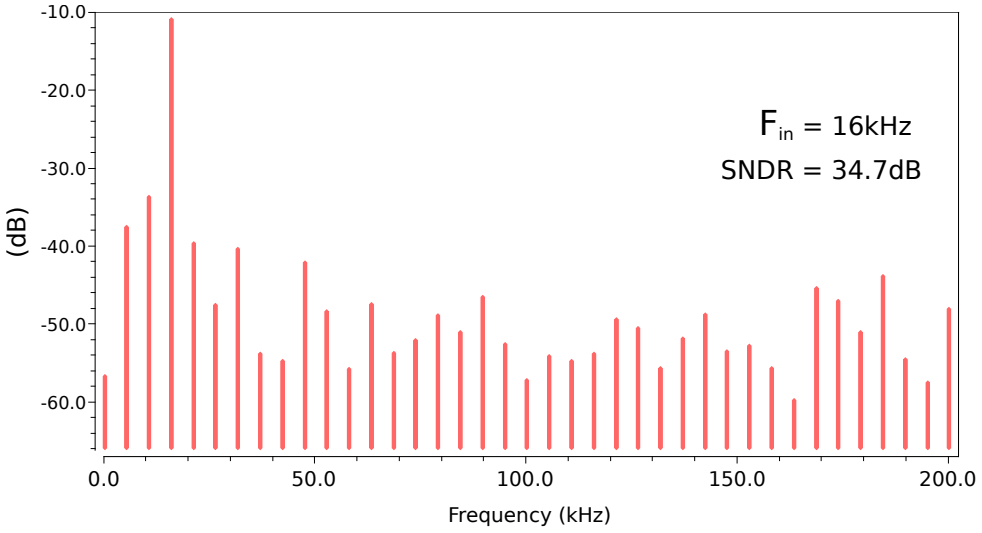


Figure 5.7: Frequency spectrum of the system's output waveform for a 16kHz sine wave input.

resulting in the frequency spectrum shown in figure 5.7. The SNDR of the signal was calculated to be 34.7dB. This is lower than that obtained from the simulated value (39.5dB) of the SNDR presented in chapter 3. This reduction in the SNDR could be attributed to the distortion introduced to the input signal by the electrostatic discharge (ESD) protection circuits found on the Input/Output cells. The second reason for the reduction could be due to the switching noise injected into the silicon substrate by the digital circuits since the digital and analogue circuitry share the same ground on the substrate (this was due to the fact that the CMOS process was a twin well process). The third reason could be due to the limited measurement resolution of the logic analyser used i.e since the ADC digital outputs are asynchronous they can change at any moment in time e.g in between the logic analyser's sampling period thereby resulting in a loss in time measurement.

The same sine wave input was increased from 1kHz to 20kHz in steps of 1kHz and the SNDR calculated at each step resulting in the plot shown in figure 5.8. From the plot it can be seen that the SNDR varies about a 30dB as the frequency of the input sine wave increases. This is slightly different to the trend observed in the simulation results in chapter 3 where the SNDR reduces with increase in frequency.

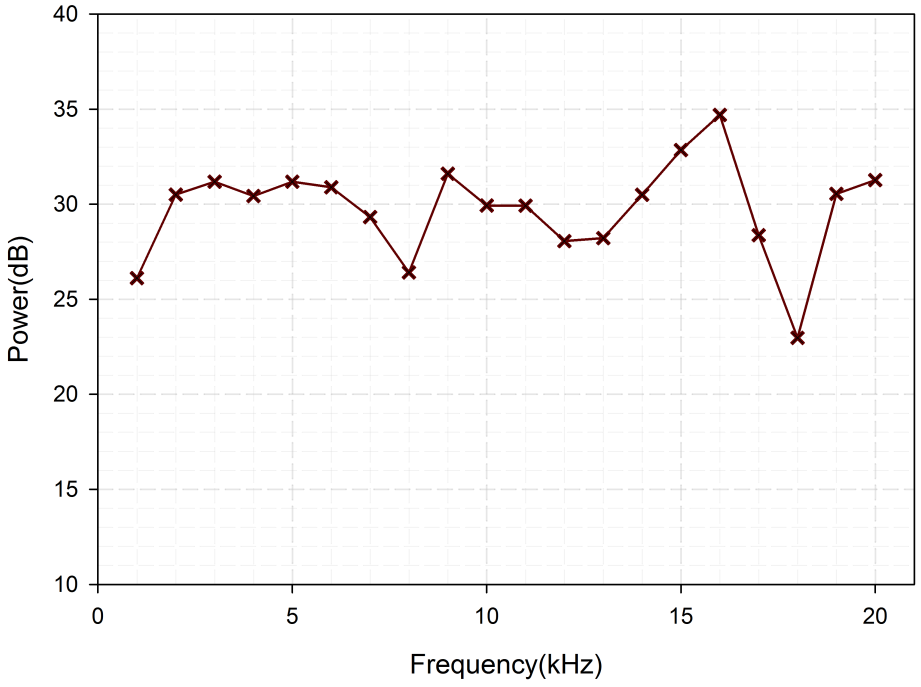


Figure 5.8: SNDR observed on the output as the sine wave signal frequency increases.

5.3 Power Consumption

Since the design under test operates in an event driven manner, generating and operation on samples only when the input signal is significantly changing, the average power consumption of the test chip will vary depending on the input signal. This therefore necessitated the power consumption experiment to be performed with two significantly different input signals i.e sine wave and ECG, in order to get a true depiction of the system's power consumption. Initial before any signal was provided at the input of the test chip, the static power consumption of the ADC was measured to be 9.7μW while that of the FIR filter was 0.4μW when power gating is enabled and 2.4μW when power gating is disabled. For a pure 2kHz sine wave input, the power consumption of the ADC was measured to be 30.4μW while that of the FIR filter was 89μW with power gating disabled and 87.8μW with power gating enabled. It can be seen that the measured ADC power is about 4μW more than that of the simulated value presented in section 3.6. Figure 5.9 shows the graph of power vs input signal frequency of the ADC and FIR.

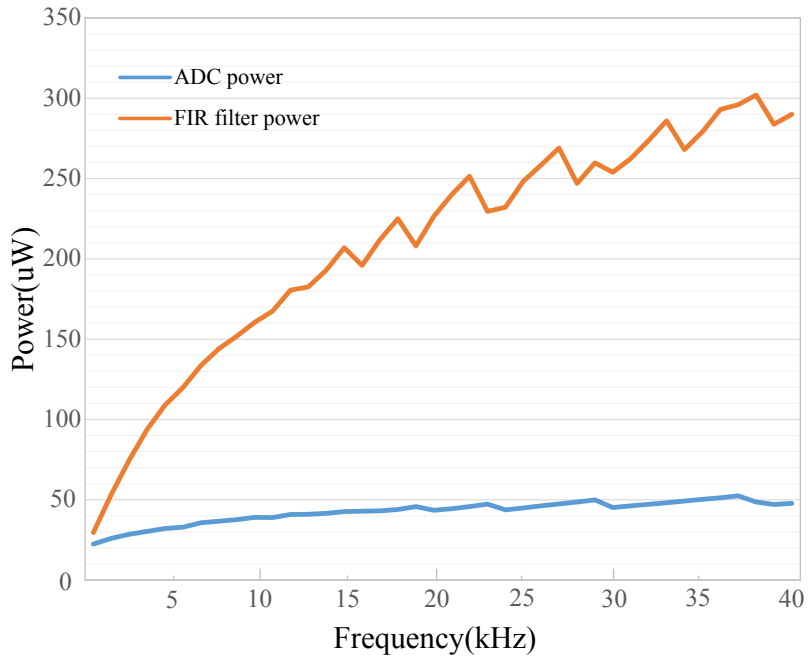


Figure 5.9: ADC and FIR power consumption as signal frequency increases.

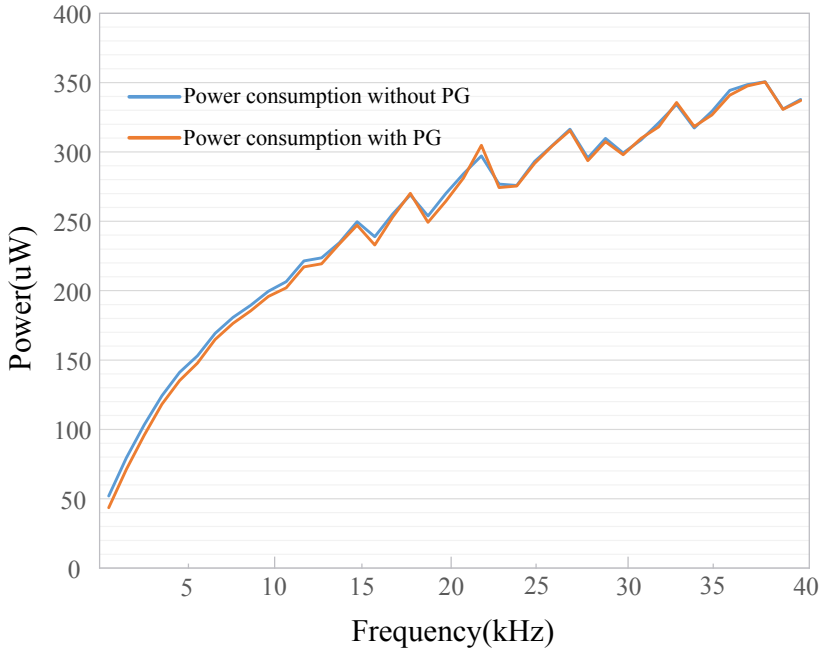


Figure 5.10: Test Chip power consumption when power gating is enabled and when it is disabled as signal frequency increases

As the frequency is increased the power consumption of both the ADC and FIR increases. This can be attributed to the fact that as the frequency increases there will be more "level crossings" resulting in more samples per unit time being generated by the ADC and processed by the FIR filter. Figure 5.10 shows the total power consumption profile for the test chip when power gating is enabled and disabled. It can be seen that initially, at low frequencies the power consumption of the test chip when power gating is enable is lower than that when power gating is disabled. As the frequency is increased the power consumption, with power gating enable, increases until it becomes almost similar to the power consumed when it is disabled. This can be attributed to the fact that as the sample rate increases with increase in frequency, the power consumed by the power gating cells and power grid during the power ON/OFF cycles is greater than the actual leakage power saved due to power gating. At 0.35μm leakage current is quite small hence the minimal savings seen in this experiment. At lower geometry technology however, the savings might account for a significant amount of total power savings as was explored in [55] and [60].

To further illustrate the increase in sample rate with increase in signal frequency figures 5.11a, 5.11b and 5.11c obtained from the Agilent MSO-X-4034A Mixed Signal Oscilloscope, that show the input sine wave and the active low RDY signal generated by the ADC can be considered. The approximate number of samples generated per second was calculate to be 68*kS/s* for a 2*kHz* input, 160*kS/s* for a 10*kHz* input and 200*kS/s* for a 20*kHz* input.

For an ECG waveform input applied at a frequency of 2*kHz* , the power consumption of the ADC was measured to be 23μW (this is not the real frequency of the ECG pattern and is only used for giving higher dynamic power dissipation usd for comparison purposes). It should be noted that one single section of the ECG shown in figure 5.12a was taken as a single cycle and repeated at the 2*kHz* frequency to generate a continuous waveform as shown in figure 5.12b. This consumed power value is 7.4μW less than that of a pure sine wave. This can be attributed to the fact that the ECG signal has a relatively flat sections that stay longer within the level crossing voltage window where no switching occurs and power gating is enabled to mitigate leakage power. As was observed for the sine wave, an decrease in frequency reduces the power consumption, therefore for a real ECG signal of about 50 beats per minute the power consumed would be much lower than 23μW. The FIR filter on the other hand consumes 58.4μW when power gating

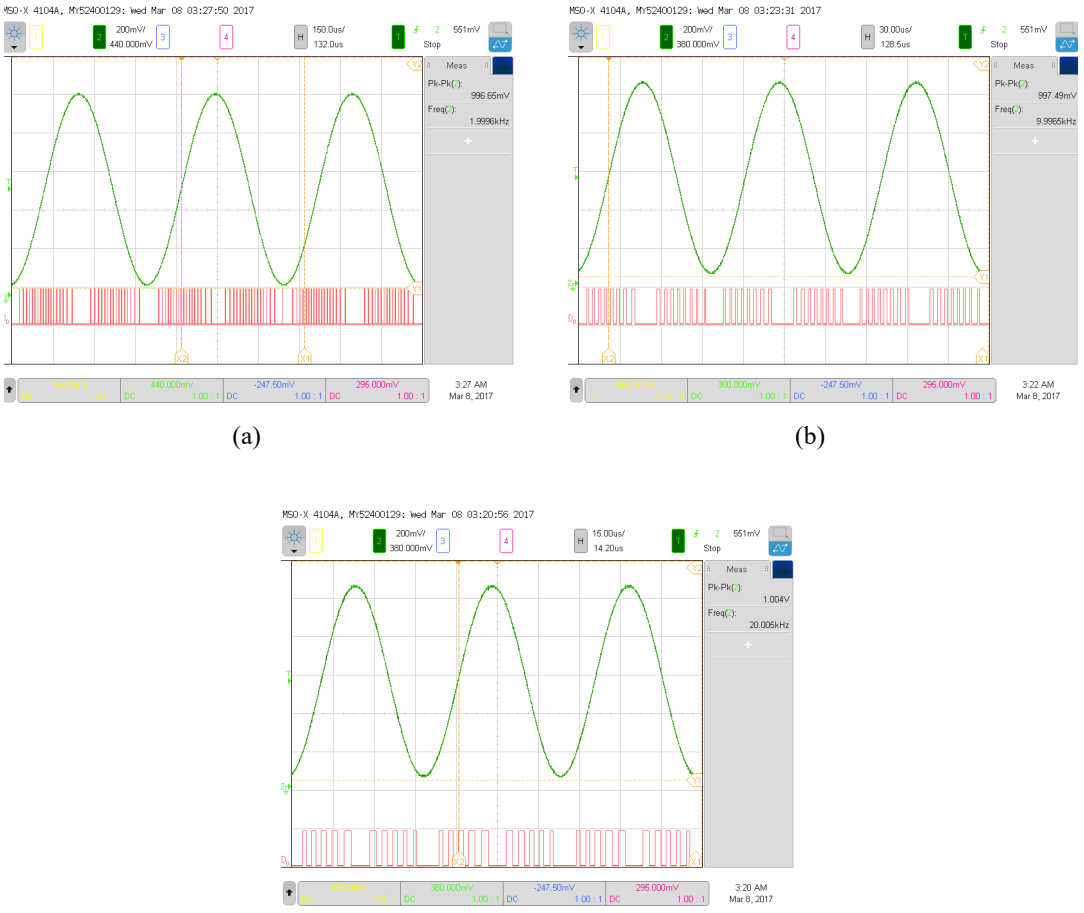
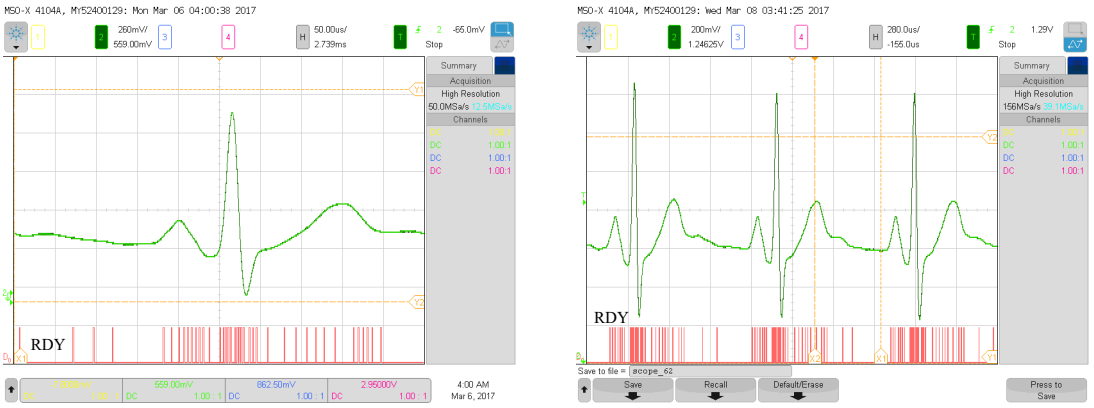


Figure 5.11: Sine wave signal input to the ADC and the resulting active low RDY signal (representing presence of a sample). **a)** At *2kHz* the RDY signal is generated at an average rate of 68 *kS/s*, at **b)** *10kHz* the rate is 170 *kS/s* and at **b)** *20kHz* the rate is 200 *kS/s*

is enabled and 61μW when it is disabled. The difference between the two values, represents the power consumed constantly due to leakage current when power gating is disabled. However when power gating is enabled leakage current will be reduced during periods when the filter is idle i.e the period in between adjacent samples that is observed once the filter has completed its operations on a single sample.



(a) (b)

Figure 5.12: ECG signal applied at the input and the resulting RDY signal generated by the ADC. The generation of the RDY signal is done when there is significant change on the ECG signal above the set voltage window.

5.4 Summary

The experimental results obtained for the test chip are summarised in Table 5.1. From the results it has been proven that the mixed signal data acquisition and processing system's power consumption depends on the rate of change signal and would therefore be suitable for use in applications with sparsely occurring signals. It has also been shown that the power gating applied on the FIR filter is only beneficial below a given average sample rate after which the power gating network consumes more power than the power it saves by minimizing leakage current.

From the ADC's power consumption, effective number of bits (ENOB) and the SNDR, the figure of merit (the ADC's energy efficiency per conversion) is calculated using equation 3.8 and found to be 2.58pJ/conv to 5.5pJ/conv between the frequencies of 0.5kHz to 20kHz. Since the figure of merit is directly proportional to the power consumption it flows that an increase in signal frequency results in an increase in the figure of merit value.

Figure 5.2 shows a table of comparison for the performance of 2 fixed window level crossing ADC, a single floating window level crossing ADC and our proposed ADC.

Table 5.1: Summary of Measured System Characteristics

Process Technology	AMS 0.35μm CMOS
ADC area	0.07mm^2
FIR filter Area	0.56mm^2
Analogue Supply Voltage	2.6V
Digital Supply Voltage	1.5V
ADC Power (0.5kHz to 20kHz)	22.4μW to 47.8μW
FIR Filter Power (0.5kHz to 20kHz)	43.5μW to 337μW
Sampling Rate (2kHz to 20kHz)	68kS/s to 200kS/s
Peak SNDR (at 16kHz)	34.7dB
ENOB	7.757 bits
FOM	2.58-5.5pJ/conv

Table 5.2: Performance comparison of asynchronous Level Crossing ADCs recently reported in literature

Parameter	[61]	[13]	[30]	This Work
AADC type	Floating Window	Fixed window	Fixed window	Fixed window
Process Technology	90*nm* CMOS	0.18μm CMOS	0.5μm CMOS	0.35μm CMOS
ADC Area	0.06mm^2	0.04mm^2	0.06mm^2	0.07mm^2
Supply Voltage	1*V*	0.8*V*	3.3*V*	1.5*V*(D), 2.6*V*(A)
Frequency range	0.2*kHz* to 3.4*kHz*	5*Hz* to 5*kHz*	0.2*kHz* to 5*kHz*	0.5*kHz* to 20*kHz*
ADC Power	40μW	313-282*nW*	106μW	22.4-47.8μW
Peak SNDR	62*dB*	49*dB*	31*dB*	34.7*dB*
FOM	4.9 - 27.3*pJ*/conv	219-565*fJ*/conv	1.6*nJ*/conv	2.58-5.5*pJ*/conv

Chapter 6

Conclusion

6.1 Thesis Contributions

In this thesis an asynchronous single slope level crossing ADC and an event driven burst mode FIR filter were proposed. It was shown that both designs consume power in a manner proportional to the rate of change of the input signal. The ADC was proposed as an alternative to other asynchronous ADC's that either generated a lot of samples per unit time as was in the case of the floating window type [29], [61] discussed in chapter 2.3.1 or cause signal distortion as was shown in chapter 2.3.2 for the ADC presented in [30].

In our proposed ADC design the process of detecting a level crossing, and the process of the actual conversion of the absolute value of the sampled signal are separated i.e the level crossing event only triggers at what point in time a sample is taken and doesn't form part of the signal quantization process. This is opposed to the other types of level crossing ADCs that use the level crossing event as the actual quantization step. As a result these ADC require the LSB (Level Crossing Window) to be very small in order to guarantee high dynamic range resulting in large number of samples. In addition to this the fixed window level crossing ADC [30], [70] and [13] require that there upper and lower boundary reference voltages of the voltage window be equidistant from the mid point reference voltage. In a case were these values are different, due to offsets observed at the comparator inputs or process and temperature variations, the LSB during

rising and during falling of the the signal will be different resulting in signal distortion. In our design, since the level crossing event does not form part of the quantization process, the voltage window does not determine the LSB and therefore a variation in the reference voltages will not distort the signal. In addition to this the voltage window can be increased or decreased in order to decrease or increase the sampling rate since it affects the T_{track} component of equation 3.1.

The event driven burst mode FIR filter presented in this thesis was shown to be able to handle asynchronous samples at its input. This filter was presented as an alternative to the ones presented in [67], [29] and [61] that rely on large delay structures in each stage of the filter in order to maintain the time information in-between samples for it operate properly. It has the capability to power itself up when it detects a sample at its input and power itself down once the evaluation of the sample is completed. By doing this it is able to minimize leakage power consumption in between time periods when there are no samples or when two adjacent samples are far apart in time. It was shown that the power consumption of the filter is dependent on the sample rate of the input signal i.e it increases with and increase in sample rate. It is worth noting that this FIR filter was presented as case study of how a DSP system can benefit in-terms of minimizing its power consumption if it's presented with asynchronous samples.

A test chip was fabricated in a 0.35μm CMOS process and consists of both the asynchronous single slope level crossing ADC and the power gated burst mode asynchronous FIR filter. The experimental results showed that the ADC achieves a maximum SNDR of $34.71dB$ over a bandwidth of $20kHz$. The power consumption of the ADC was measured to be between 22.47μW and 47.8μW when the input signal frequency was increased from $0.5kHz$ to $20kHz$. The FIR filter on the other hand consumes between 43.5μW and 337μW for the same input frequency range.

6.2 Future Research

The design of the comparator that compares the ramp voltage to that of the input signal suffers from offset issues and also introduces 1/f noise to the resulting converted signal. In future designs, it would be desirable to have offset cancellation circuitry that would be able to sample

onto a capacitor the offset present at the input of the comparator. This could be done as an initialization process each time a level crossing is detected. A short pulse can be generated and used to shortly reconfigure the comparator (via a switch) as a voltage follower before configuring it back as a comparator.

Due to the fact that the system was implemented on a 0.35μm CMOS process that has minimal leakage power consumption, it was not very obvious to what extent power gating the FIR filter in between asynchronous samples would reduce power consumption. We were able to show a savings of about 2μW at lower input signal frequencies in our experiment. An implementation of the design in a lower geometry process where leakage current is an issue would give a good measure of how beneficial the technique is.

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