In-situ Health Monitoring Applied to High-Voltage IGBT Power Modules

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Abstract

This thesis addresses an important issue of identifying insulated gate bi-polar transistor (IGBT) chip failures in multichip IGBT power modules. IGBT power modules are the dominant semiconductor devices of choice in high-voltage (HV) high-power converter applications which include domestic, commercial, automotive, railway, marine, aerospace and industrial applications. Commonly available HV IGBT power modules in the market are rated at 3.3 kV, 4.5 kV and 6.5 kV. These HV IGBT modules comprise several IGBT chips connected in parallel to achieve high-current capability; hence they are also known as multichip IGBT power modules.

IGBT power modules are not flawless. The increased complexity of IGBT power module construction and inhomogeneous semiconductor chips make HV power modules less reliable. IGBT chips and electrical and mechanical interface material within the modules wear out and fail due to thermal cycling, operating environment or mishandling. IGBT failures while in application have repercussions on safety and failure costs. Thus the reliability of IGBTs while in their application is crucial especially in HV applications which comprise critical and large loads. To improve the reliability, an in-situ (online) health monitoring interface for HV IGBT power modules is proposed in this thesis. Two distinct advantages of in-situ IGBT health monitoring are that it allows IGBT module replacement prior to complete failure thus reducing safety and reliability risks. The second advantage is that the interval time for IGBT maintenance work can be tailored towards the real degradation rather an obligatory fixed time interval thus reducing maintenance costs.

In large power modules, it is common to have IGBT chips as well as anti-parallel diode chips within the power module. This research focusses only on the health monitoring of the IGBT chips and not the diode chips. The main reason is that IGBT chips experience higher thermal stresses compared to diodes hence IGBT chips are more susceptible to failures compared to diode chips. In practice, IGBT chip failures are accompanied by a change in junction temperature. Thus this thesis proposes the use of temperature-

sensitive electrical parameters (TSEPs) for in-situ health monitoring of IGBT power modules.

Following a comparison of twelve traditional online TSEPs from literature and five new TSEPs proposed in this thesis, this thesis employs a novel TSEP, gate-emitter pre-threshold voltage ($V_{GE(pre-th)}$) as a health-sensitive parameter (HSP) for chip failure detection in multichip HV IGBT power modules. A $V_{GE(pre-th)}$ online chip loss monitoring circuit has been successfully implemented on a commercially available IGBT gate driver. $V_{GE(pre-th)}$ is measured at a fixed pre-determined instant of the gate-emitter voltage (V_{GE}) between the V_{GE} zero-crossing ($V_{GE(0)}$) and threshold voltage ($V_{GE(th)}$) during IGBT turn-on. $V_{GE(pre-th)}$ requires low hardware with only a voltage sensor and a counter. Since it is based on the low-voltage (LV) gate side rather than the HV collector side of IGBT, $V_{GE(pre-th)}$ does not require HV isolation or HV insulation.

Simulation and experimentation of 16-chip 3.3kV 800A DIM800NSM33-F IGBT power modules from Dynex Semiconductor Limited (Ltd) have shown that $V_{GE(pre-th)}$ has a good accuracy and repeatability; a linear sensitivity of 500 mV/chip loss with IGBT chip failures; a linear virtual junction temperature (T_{vj}) sensitivity of -2.2 mV/°C and tracks the highest chip temperature. It has thus been concluded that $V_{GE(pre-th)}$ can be used for both T_{vj} and IGBT chip failure monitoring in HV IGBT power modules. $V_{GE(pre-th)}$ can be tested during normal IGBT turn-on operation or during the off-state of the IGBT. In both cases the same information about temperature and loss of chip number can be detected which makes $V_{GE(pre-th)}$ more versatile than any other TSEP or HSP.

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List of Abbreviations

3D	Three-Dimensional
A	Amperes
ac	Alternating Current
ADC	Analogue-to-Digital Converter
B	Base
BJT	Bi-polar Junction Transistor
BNC	British Naval Connector / Bayonet Neill–Concelman
C	Collector
CTE	Coefficient of Thermal Expansion
CVR	Current Viewing Resistor
dc	Direct Current
DCB	Direct Copper Bonding
DPO	Digital Phoshor Oscilloscope
DUT	Device Under Test
E	Emitter
EMI	Electro-Magnetic Interference
EOS	Electrical Overstress
F	Frequency
FWD	Free Wheel Diode

G	Gate
GTO	Gate Turn-Off
H	Henry
HSP	Health-Sensitive Parameter
HV	High-Voltage
HVDC	High-Voltage Direct Current
Hz	Hertz
IGBT	Insulated Gate Bi-polar Transistor
IGCT	Insulated Gate-Commutated Transistor
kA	Kilo amperes
kV	Kilo volts
LCD	Liquid Crystal Display
Ltd	Limited
LUT	Look-Up Table
LV	Low-Voltage
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide Silicon Field-Effect Transistor
MSO	Mixed Signal Oscilloscope
MHz	Megahertz
NPT	Non-Punch-Through
PIC	Programmable Interrupt Controller
PoF	Physics of Failure

ppm	Parts Per Million
PSU	Power Supply Unit
PT	Punch-Through
PWM	Pulse Width Modulation
TCR	Temperature Coefficient of Resistance
TDDB	Time-Dependant Dielectric Breakdown
s	Seconds
ms	Milli seconds
μs	Micro seconds
ns	Nano seconds
SOA	Safe Operating Area
SSTDR	Spread Spectrum Time Domain Reflectometry
TSEP	Temperature-Sensitive Electrical Parameter
V	Volts
W	Watts
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

List of Symbols

α_{pnp}	Bi-polar transistor gain
Ω	Ohm
%	Percent
ϕ_F	Fermi energy
A_L	Cross-sectional area of layer
A_C	Cross-sectional area of channel
A_{GC}	Gate-collector overlap area
β_{pnp}	Current gain of the bi-polar transistor in IGBT
°C	Degrees Celsius
c	Specific heat capacity
C	Capacitance
C_{th}	Thermal capacitance
C_0	Charge extraction capacitance
C_{ce}	Collector-emitter capacitance
C_{DS}	Drain-source capacitance
C_{gc}	Gate-collector capacitance
C_{GD}	Gate-drain capacitance
C_{ge}	Gate-emitter capacitance
C_{GS}	Gate-source capacitance

C_{ies}	Input capacitance
$C_{ies,total}$	Total input capacitance
C_{res}	Reverse transfer capacitance
C_{ox}	Gate oxide capacitance
d	Density
dI_C/dt	Collector current slope
dV_{CE}/dt	Collector-emitter voltage slope
D_a	Ambipolar diffusion coefficient
D_{nE}	Diffusion coefficient for minority carriers
e^-	Electron
E_a	Activation energy
ε_{ox}	Dielectric constant of oxide
ε_{Si}	Dielectric constant of silicon
GaN	Gallium nitride
G_M	Trans-conductance
h^+	Hole
$I_{C(latch)}$	Collector latching current
$I_{C(leak)}$	Collector leakage current
$I_{C(tail)}$	Collector current tail
$I_{C(sat)}$	Collector saturation current
I_G	Gate current
I_{GES}	Gate leakage current

I_{GG}	Gate supply current
$I_{G(miller)}$	Gate current Miller plateau level
$t_{IG(miller\ width)}$	Gate current Miller plateau width
$I_{G(peak)}$	Gate peak current
J_c	Collector current density
J_{ch}	Channel current density
k	Thermal conductivity
k_B	Boltzmann's constant
l	Length
l_a	Ambipolar diffusion length
l_{ch}	Channel length
l_{nE}	Diffusion length for minority carriers
l_t	Layer thickness
L	Inductance
L_C	Collector inductance
L_G	Gate inductance
L_E	Emitter inductance
L_M	IGBT module inductance
Q_g	Gate charge
n	Negative doped material
N_{AE}	Minority carrier doping concentration
N_B	Base doping concentration

N_f	Number of cycles to failure
n_i	Intrinsic concentration
p	Positive doped material
p_D	Density of layer material
p_0	Hole concentration
P_D	Power loss dissipation
P(t)	Instantaneous power dissipation
q	Elementary charge
R	Resistance
R_B	Base resistance
R_C	Collector resistance
R_{DS}	Drain-source resistance
R_E	Emitter resistance
R_G	Gate resistance
$R_{G(int)}$	Internal gate resistance
$R_{G(int),total}$	Total internal gate resistance
$R_{G(ext)}$	External gate resistance
$R_{G(ext),on}$	Turn-on external gate resistance
$R_{G(ext),off}$	Turn-off external gate resistance
R_{th}	Thermal resistance
SiC	Silicon carbide
SiO_2	Silicon dioxide

τ_{HL}	High-level lifetime decay of carriers
τ_n	Space charge region lifetime
t	Time
T	Temperature
ΔT	Temperature variation
T_a	Thermal ambient
T_C	Case temperature
$t_{d(off)}$	Turn-off delay
$t_{d(on)}$	Turn-on delay
T_j	Junction temperature
T_m	Mean temperature
$t_{VGE(miller\ width)}$	Gate-emitter voltage Miller plateau duration
T_{vj}	Virtual junction temperature
μ	Mobility of charge carriers
μ_{ni}	Inversion layer mobility
μ_{ns}	Surface mobility of electrons in the channel
V	Volts
V_{CE}	Collector-emitter voltage
$V_{CE(sat)}$	Collector-emitter saturation voltage
$V_{CE(tail)}$	Collector-emitter voltage tail
$V_{dc\text{-}link}$	DC-link voltage
$V_{EE'}$	Main emitter-auxiliary emitter voltage drop

V_{FB}	Flat-band voltage
$V_{GD(cs)}$	Gate driver voltage control signal
V_{GE}	Gate-emitter voltage
$V_{GE(miller)}$	Gate-emitter voltage Miller plateau level
$V_{GE(pic)}$	Gate-emitter voltage at PIC input pin
$V_{GE(pre-th)}$	Gate-emitter pre-threshold voltage
$V_{GE(th)}$	Gate-emitter threshold voltage
V_{GG}	Gate supply voltage
$V_{GG(on)}$	On-state gate supply voltage
$V_{GG(off)}$	Off-state gate supply voltage
W	Width
W_{ch}	Channel width
W_N	Drift region width
x_d	Diffuse length
Z_{th}	Thermal impedance
$Z_{th(jc)}$	Junction-case thermal impedance

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Chapter 1. Introduction

Insulated gate bi-polar transistor (IGBT) power modules continue to dominate the market in medium and high-voltage applications. This is due to their attractive electrical characteristics and superior overall performance [1]. Although IGBT manufacturers continue improving the robustness of IGBT power modules, the reliability and useful lifetime of IGBT power modules in their applications cannot be guaranteed; they are bound to deteriorate and fail during their lifetime. Thermal stress is a common cause of failures in IGBT due to mismatch of the coefficient of thermal expansion (CTE) of the different materials in the IGBT's structure. This thesis identifies reliability concerns in high-voltage (HV) multichip IGBT power modules as they are more susceptible to failures due to their complex construction, inhomogeneous chips and high power operating environments.

In large power modules, it is common to have IGBT chips as well as anti-parallel diode chips within the power module. This thesis focusses only on the health monitoring of the IGBT chips and not the diode chips. The main reason is that IGBT chips experience higher thermal stresses compared to diodes which IGBT chips less reliable compared to diode chips. In practice, IGBT chip failures are accompanied by a change in junction temperature [2]. The junction region of an IGBT cell is reported to be hottest point where the most heat is generated hence the term junction temperature (T_j) is commonly used when referring to an IGBT chip's temperature [3]. In multichip power modules, the terminology virtual junction temperature (T_{vj}) is often used because the measured temperature is an aggregate of the T_j's of the parallel-connected IGBT chips within the power module [4, 5]. This thesis proposes the use of a novel temperature-sensitive electrical parameter (TSEP), gate-emitter pre-threshold voltage ($V_{GE(pre-th)}$), both to determine T_{vj} as well as to detect the loss of IGBT chips in multichip IGBT power modules. This chapter discusses the research background, challenges and methodology.

1.1 IGBT Applications and Reliability

1.1.1 IGBT Applications

The prominence of IGBTs in the market pave the way for their application in this research. Before the invention of IGBTs in the early-1980s, metal-oxide silicon field-effect transistors (MOSFETs) and bi-polar junction transistors (BJTs) dominated the power semiconductor industry. This is because MOSFETs are renowned for their fast switching speeds, and BJTs for their low on-state voltage drops hence lower conduction losses. The deficiencies of MOSFETs (high on-state voltage drop especially at high voltages) and BJTs (slow switching speed) motivated the invention of the IGBT which integrates the functions of MOSFETs and BJTs, for improved performance [6]. While MOSFETs are still favourable in low-power applications, IGBTs dominate the medium and high-power devices market [7, 8] as portrayed in Figure 1.1. Figure 1.1 also shows that IGBT power modules are still gaining more shares in the market over wide-bandgap power modules - silicon carbide (SiC) and gallium nitride (GaN), which have been recently introduced in the market.

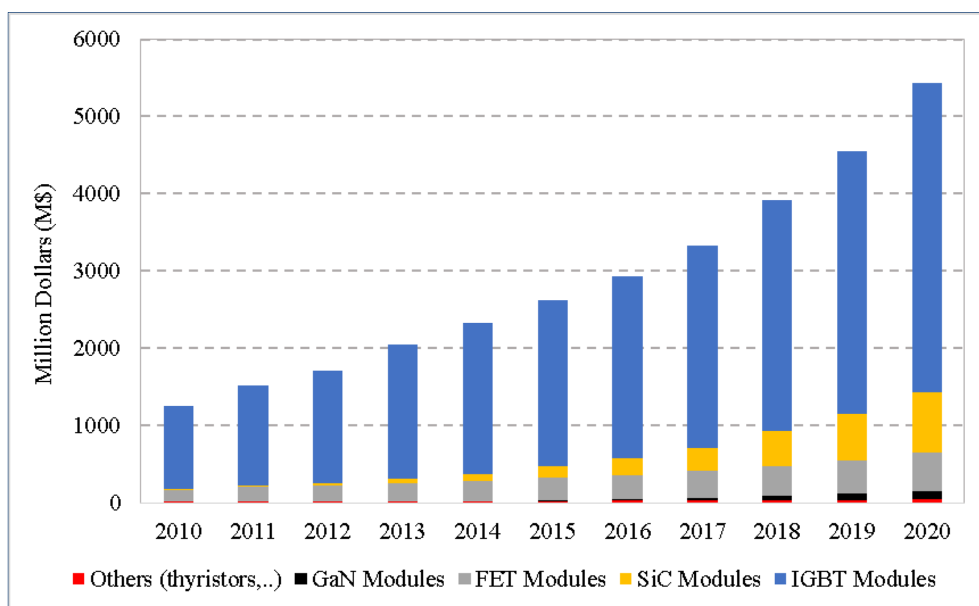


Figure 1.1: 2010 - 2020 Market Size for Power Modules [7].

Common IGBT applications include automotive [2], railway [9], marine and aerospace [10] traction systems; industrial motor drives; energy storage systems; renewable energy sources where power converters enable their connection to electrical power grids; and high-voltage direct current (HVDC) transmission with power converters facilitating the transfer of power between active alternating current (ac) and dc networks [11].

1.1.2 IGBT Reliability

Literature often ranks power semiconductor switching devices as having the lowest reliability in power converters [12-15]. To improve IGBT reliability, IGBT manufacturers are always enhancing their robustness through advances in technology, and feedback from failed devices [16]. To safeguard IGBTs from operational stresses, IGBT gate drivers are often equipped with IGBT protection features such as short circuit protection and active clamping [17]. Despite these efforts, IGBTs still endure stressful operating environments which lead to their failure [14, 16]. Moreover, mishandling of IGBTs during manufacturing, transportation and storage may also induce defects which contribute to their failures [16]. Consequently, the reliability and useful lifetime of IGBTs cannot be guaranteed as depicted in Figure 1.2.

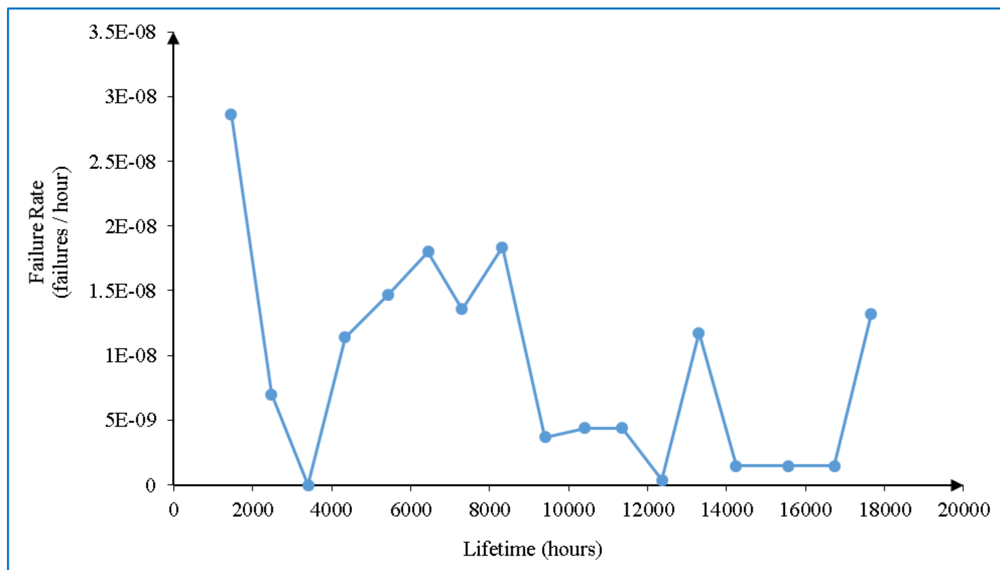


Figure 1.2: Typical Roller-coaster Curve of Failure Rate for Generic Transistor-based Devices [16].

Figure 1.2 curve describes the relative failure rate for a given population of generic transistor-based devices over their useful lifetime. It is referred to as ‘the roller coaster curve’ due to the random nature of component failures against their expected lifetime. The curve shows an initial high failure rate which is attributed to stresses or damage induced in the devices during manufacturing, transportation, storage or installation. Following the initial peak failure rate is a sharp decline of the failure rate. The failure rate then is randomly fluctuating high and low throughout transistor lifetime on account of wear and tear or environment and operational stress/damage. This is a closer representation of failure rate unlike the traditional bathtub curve which would assume a flat trend/constantly low failure rate after 4000 hours. Consequently, the reliability of IGBTs while in their application is uncertain. To overcome this, in-situ/online health monitoring of IGBTs has been proposed.

1.2 IGBT In-situ Health Monitoring

In critical applications, IGBT failures have repercussions on safety and failure costs. In the long term, the reputation of IGBT manufacturers, as well as the end users, may be ruined [18]. To overcome this, in-situ health monitoring has been proposed. This allows IGBT module replacement prior to complete failure; thus reducing safety and reliability risks [13, 19, 20]. In addition IGBT maintenance work can be tailored towards the real degradation rather than obligatory fixed time interval thus reducing maintenance costs.

A number of IGBT health monitoring methods exist which are presented in Table 1.1. The IGBT failures presented in Table 1.1 are described in Chapter 3. Table 1.1 shows that the IGBT health monitoring methods all employ TSEPs. Unfortunately the methods do not always perform well with different IGBT types being available in the market. The pros and cons of the existing IGBT health monitoring methods are discussed in Chapters 3 and 5, and reflect that the demand for new IGBT health monitoring techniques is high. For this reason, five new TSEPs applicable for online IGBT health monitoring are proposed in Chapter 6.

Table 1.1: Existing IGBT Online Health Monitoring Methods.

IGBT Component Monitored	Method	IGBT Tested
Junction temperature (T_j)[1]	On-state voltage drop ($V_{CE(sat)}$) [21-24]	1.7 kV, 1 kA 600 V, 70 A
	Threshold voltage ($V_{GE(th)}$) [25, 26]	1.7 kV, 1.2 kA
	Collector current slope (dI_C/dt) [27, 28]	3.3 kV, 1.2 kA
	Trans-conductance (G_M) [27]	
	Gate resistance (R_G) [29-31]	6.5 kV, 600 A
	Turn-off delay ($t_{d(off)}$) [32]	1.2 kV, 40 A
	Turn-on delay ($t_{d(on)}$) [28]	-
	Saturation current ($I_{C(sat)}$) [33]	1.2 kV, 75 A
	Voltage drop between main emitter and auxiliary emitter ($V_{EE'}$) [34]	1.2 kV, 300 A 1.7 kV, 650 A
	Power loss dissipation (P_D) [35]	600 V, 400 A
	Thermal modelling [36, 37]	600 V, 400 A
Bond wire lift-off	$V_{CE(sat)}$ [2, 21, 38, 39]	600 V, 800 A 600 V, 70 A
Chip defects	Gate peak current ($I_{G(peak)}$) [40]	1.7 kV, 200 A
Solder-joint degradation	$V_{CE(sat)}$ [38]	600 V, 800 A
Die-attach degradation	$V_{CE(sat)}$ [41]	600 V, 16 A
	Turn-off time [42]	
Latch-up	$V_{CE(sat)}$ [41]	600 V, 16 A
	Turn-off time [42]	
Gate oxide degradation	$V_{GE(th)}$ [41]	600 V, 16 A
	Gate capacitance voltage [41]	
Metallization	$V_{CE(sat)}$ [39]	600 V, 200 A

1.3 Research Gap - HV IGBT In-situ Health Monitoring

Table 1.1 does not show many existing health monitoring methods for HV IGBT power modules. Hence the investigation of new methods for HV IGBT online health monitoring has been identified as a research gap in this thesis. Figure 1.3 results from a recent industry-based survey portrays the need for health monitoring in high-power applications where HV IGBT power modules are utilized.

[1] T_j is an IGBT ageing indicator, with symptoms including solder fatigue and bond wire wear out

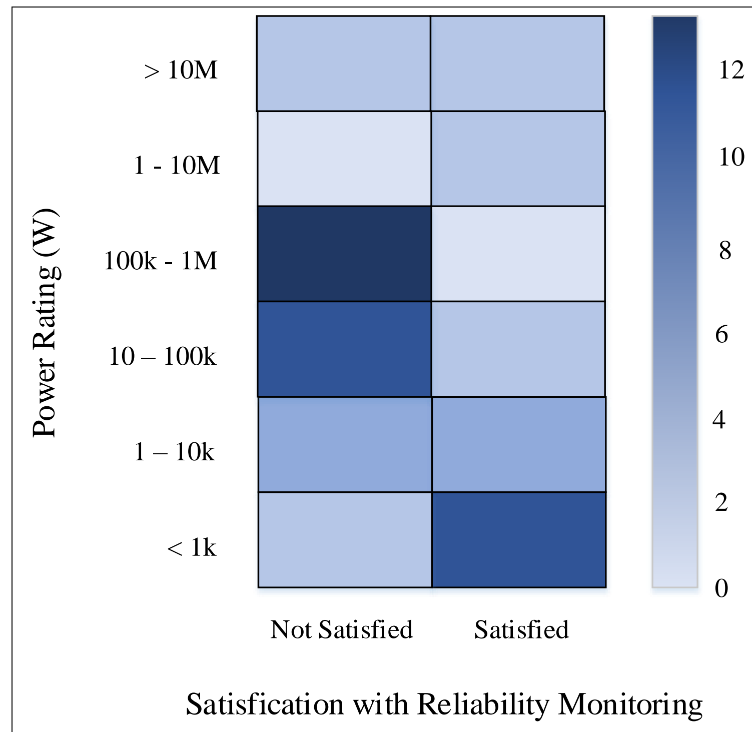


Figure 1.3: Correlation Between Power Rating and Reliability Concerns [43]

Figure 1.3 shows increased reliability concerns in IGBT modules for high-power applications. These applications are often considered critical due to the large scale and sensitive nature of load [43-45]. Most of high-power applications, such as modular multi-level converters (MMCs) [46], utilize the technique of 'redundancy' where components in excess of the design requirements are off-duty and on standby, and are switched online in the event of any on-duty device failing, taken out for maintenance testing or just rotational duty. Redundancy thus is utilized to improve the operational reliability of the converters. However, it is uneconomical to have redundant components in excess of the design requirements as they take up physical space and result in complexity. Moreover, the technique of redundancy may still disturb the application's normal operation during the switch-over process. The proposed IGBT in-situ health monitoring can improve the operational reliability of IGBT power modules and eliminates the need for redundancy in high-power IGBT applications. Unlike time based scheduled maintenance work on a redundancy-based system or routine shutdown, a health oriented IGBT maintenance based on in-situ health monitoring allows low-cost

as the interval time can be tailored towards the real degradation rather than obligatory fixed time interval.

Dynex Semiconductor Ltd have shown their interest in this research and donated some IGBT power modules utilized in the experiments. This also indicates that the proposed research gap is apparent in industry.

Standard 3.3 kV IGBT power modules with plastic casing are among the most commonly used devices in high-power applications such as railway traction [9]. 3.3 kV, 800 A single switch IGBT power modules DIM800NSM33-F from Dynex Semiconductor Limited (Ltd) have been chosen as reference modules and used in simulation and experimentation. Standard HV IGBT power modules generally have similar packaging structures and failure mechanisms. Thus the outcomes of this research are applicable to all standard HV IGBT power modules such as 4.5 kV and 6.5 kV IGBT power modules.

1.4 Research Methodology

The research's main objective is the development of a novel online health monitoring technique for high-power IGBT modules. In large power modules, it is common to have IGBT chips as well as anti-parallel diode chips within the power module. This research focusses only on the health monitoring of the IGBT chips and not the diode chips. The main reason is that IGBT chips experience higher turn-on and turn-off losses compared to diodes and therefore higher thermal stresses compared to diodes hence IGBT chips are more susceptible to failures compared to diode chips. In addition, IGBT chips have a more complex semiconductor structure and due to the gate a more complex chip surface structure which makes IGBT chip less reliable compared to diodes [47].

Figure 1.4 indicates three main categories of the research work.

Figure 1.4: Research Framework.

As depicted in Figure 1.4 the research required an in-depth literature survey of the IGBT structure, operation and failure mechanisms. To enhance understanding of the IGBT theory and performance, a DIM800NSM33-F simulation model derived from datasheets was created in SaberRD. Simulation techniques have been devised to emulate IGBT chip failures and temperature changes.

Figure 1.5 shows samples of the DIM800NSM33-F single switch IGBT power module. The DIM800NSM33-F IGBT power module has a high component count: 16 IGBT chips, 8 anti-parallel diode chips and 4 internal gate resistors. In large power modules, it is common to have more IGBT chips than diode chips due to the different current density for each device type.

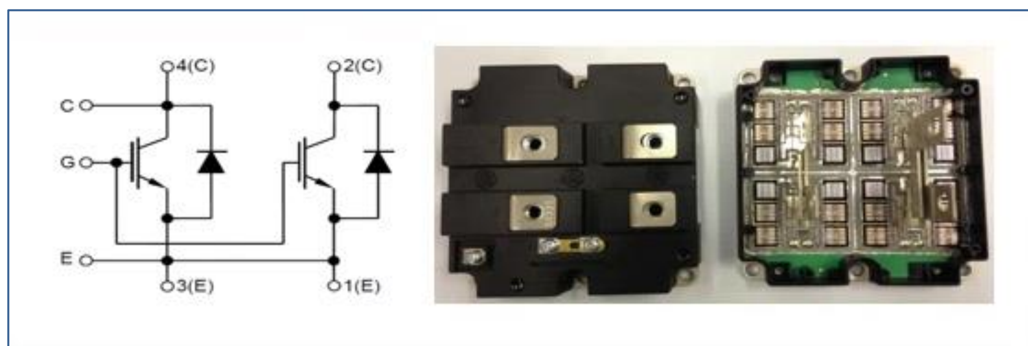


Figure 1.5: DIM800NSM33-F IGBT Power Module: Electrical Configuration, External and Interior View.

Layers of different material are employed between the IGBT chips and the baseplate in order to achieve both thermal conduction and electrical insulation. Each of the IGBT chips has 8 emitter bond wires and 1 gate bond wire; there are more bond wires connecting the diode chips and emitter pads within the module. Overall, a total of 280 bond wires and four busbars provide the necessary electrical connections of the components within the module.

The final process in assembling the module is the hermetic sealing in a plastic package and filling with silicone gel and epoxy resin. Silicone gel provides electrical isolation in the physical space between the components, while epoxy resin prevents ingress of moisture and gases. Once it solidifies, epoxy resin is highly rigid and this is welcome for mechanical protection and allows the final bending of the busbars. Once an IGBT module is sealed, internal components are inaccessible for direct measurements or visual inspections. For this reason, when in application, IGBT power module internal component failures are not noticed until the IGBT module ceases to function. For this reason in-situ health monitoring has been proposed.

1.4.1 Recommendation of TSEPs for IGBT Health Monitoring

IGBTs generate heat due to power dissipation owing to the concurrency of voltage and current in the IGBT switching and conduction states [48]. Traditionally, in an IGBT cell, the junction region has often been reported as the hottest region thus the term junction temperature (T_j) has commonly been used when referring to an IGBT device/chip temperature.

IGBT TSEPs have defined temperature dependences and are directly measured either from the gate-emitter circuit or collector-emitter circuit in order to determine IGBT T_j. Changes in the health status of an IGBT device changes the TSEP/T_j relation. Consequently TSEPs are promising for IGBT health monitoring, as discussed in Chapters 3 and 7.

In HV IGBT power modules, unlike discrete single chip IGBTs, the measured temperature is an aggregate of the IGBT chip temperatures, that is, the T_j profiles from each of the parallel-connected IGBT chips. In practice, the hottest point of an IGBT chip depends on load conditions and semiconductor technology used [49]. On this basis,

rather than junction temperature (T_j), this thesis refers to multichip IGBT power module temperature as virtual junction temperature (T_{vj}) as defined by [4] and Infineon in their IGBT application note [5]. Thus the challenge in this research is that the T_j profile of each IGBT chip in the DIM800NSM33-F is difficult to obtain. As they comprise numerous IGBT chips and associated interface components, another challenge for multichip IGBT modules is that high sensitivity requirement to detect individual components such as bond wire lift-off. In practice, the parallel-connected internal components (chips and bond wires) allow the IGBT module to continue operation upon initial failure of the internal components. Hence the research proposes IGBT chip failure as a precursor rather than chip interfaces like bond wires.

Twelve online TSEPs from literature have been investigated and described in this thesis including their pros and cons. Novel TSEPs were found on the gate-emitter voltage (V_{GE}), gate current (I_G) and collector-emitter voltage (V_{CE}) waveforms and are proposed in Chapter 6. In context of hardware implementation, one of the new TSEPs on V_{GE}- $V_{GE(pre-th)}$ - was recommended for HV IGBT power module in-situ health monitoring. $V_{GE(pre-th)}$ can indicate IGBT T_{vj} and IGBT chip failures. It is measured between the V_{GE} zero-crossing ($V_{GE(0)}$) and threshold voltage ($V_{GE(th)}$) during IGBT turn-on. Experimental tests of the DIM800NSM33-F have shown successful implementation of $V_{GE(pre-th)}$ with a linear temperature-sensitivity of -2.2 mV/°C and IGBT chip failure linear sensitivity of 500 mV/chip failure as discussed in Chapter 7. It has thus been concluded that $V_{GE(pre-th)}$ can be used both as TSEP and as health-sensitive parameter (HSP).

$V_{GE(pre-th)}$ has the advantage that it does not require HV isolation or HV insulation as it is based on the gate side rather than the HV collector side. Another distinct advantage of $V_{GE(pre-th)}$ is that it is measured before the conduction of the IGBT collector current (I_C) hence does not suffer from changes in load/I_C conditions or electro-magnetic interference (EMI)/noise of the I_C and HV V_{CE} switching modes. Furthermore, since $V_{GE(pre-th)}$ is measured before the collector current has started to flow through the power module, $V_{GE(pre-th)}$ is not influenced by self-heating. Self-heating causes measurement errors [50]. All TSEPs in Table 1.1 suffer from self-heating except R_G, $V_{EE'}$ and $I_{G(peak)}$. Self-heated TSEPs require additional sensors to determine if the same operational conditions are met; which $V_{GE(pre-th)}$ does not suffer from.

Theoretical analysis and experimental results in this thesis show that $V_{GE(pre-th)}$ has good immunity to the dc-link voltage ($V_{dc-link}$) and collector current (I_C) or load changes. However, $V_{GE(pre-th)}$ is highly dependent on gate supply voltage (V_{GG}) and external gate resistors ($R_{G(ext)}$). The results for the impact of V_{GG} show that $V_{GE(pre-th)}$ performs well with a stringent 2% maximum fluctuation of V_{GG} and it is recommended that for gate drivers operating with larger error, a voltage sensor should be added to determine if the same V_{GG} conditions are met when measuring $V_{GE(pre-th)}$. The study of the impact of $R_{G(ext)}$ shows when the same $R_{G(ext)}$ is utilized, the impact of temperature changes on $R_{G(ext)}$ can be ignored. Whereas when $R_{G(ext)}$ is physically changed, different $R_{G(ext)}$ values will lead to different results, but the fundamental $V_{GE(pre-th)}$ principal remains. Hence it is recommended that any physical change of $R_{G(ext)}$ of more than 1% require re-calibration of $V_{GE(pre-th)}$.

1.5 Contribution to Knowledge

The main outcome of this research is the successful hardware implementation of a new TSEP, $V_{GE(pre-th)}$, on IGBT power module in-situ health monitoring. Consequently, this research has made the following contributions:

- New online TSEPs for IGBT power modules.
- New IGBT in-situ health monitoring circuit based on $V_{GE(pre-th)}$.
- New simulation and experimentation techniques for HV multichip IGBT power modules.

1.6 Publications

This research has resulted in the following two journal publications on IEEE Transactions on Power Electronics:

Mandeya, R., Chen, C., Pickert, V. and Naayagi, R.T., "Pre-threshold Voltage as a Low-Component Count Temperature-Sensitive Electrical Parameter without Self-Heating", *IEEE Transactions on Power Electronics*, September 2017 [48].

Mandeya, R., Chen, C., Pickert, V., Naayagi, R.T. and Ji, B., "Gate-emitter Pre-threshold Voltage as a Health-Sensitive Parameter for IGBT Chip Failure Monitoring in High-Voltage Multichip IGBT Power Modules", *IEEE Transactions on Power Electronics*, November 2018 [47].

1.7 Thesis Structure

Chapter 2, is an overview of IGBT power modules which includes IGBT structure, operation, modelling and simulation. Chapter 3 discusses background of IGBT health monitoring and proposes a methodology for implementing health monitoring. Chapter 4 is an overview of TSEPs while Chapter 5 presents TSEP screening methodology. New TSEPs are proposed in Chapter 6 followed by hardware implementation of new TSEP, $V_{GE(pre\text{-}th)}$, for IGBT in-situ health monitoring in Chapter 7. Finally, Chapter 8 is the thesis conclusion.

1.8 Summary

The introduction has outlined the research objectives, background and methodology. The importance of IGBT power modules in the market has been highlighted. This considerably justified the viability of the proposed IGBT online health monitoring studies. Limitations of the existing IGBT health monitoring methods have been pinpointed and TSEPs have been identified as an alternative solution. Although various TSEPs have been proposed in literature, most of the work published focuses on discrete IGBT devices with single IGBT chips or power modules with low IGBT chip count. This provides an opportunity for new TSEPs which are proposed in this thesis. One of the proposed TSEPs, $V_{GE(pre\text{-}th)}$, is recommended for in-situ health monitoring of HV IGBT power modules. $V_{GE(pre\text{-}th)}$ is capable of measuring T_{vj} of the IGBT module as well as indicating IGBT chip failures. $V_{GE(pre\text{-}th)}$ operation and implementation is discussed in Chapter 7.

Chapter 2. IGBT Power Modules – Principle and Modelling

It is important to consider the IGBT structure and operation while implementing IGBT health monitoring circuit. This chapter contains an overview of the IGBT structure and operation. This includes analysis of the parasitic components in the IGBT internal structure, packaging as well as external circuitry, which are influential in IGBT performance. Finally the IGBT electro-thermal modelling and simulations are presented.

2.1 IGBT Structure

Owing to continual advances in IGBT generations (now in 6th generation) since their introduction in the early-1980s, different variations of the IGBT cell geometry have been developed. However, two common types of IGBT cell structures are punch-through (PT) and non-punch-through (NPT). The PT and NPT IGBT cell structures have four main alternating positive doped (p) and negative doped (n) layers. The n-channel cell layers are arranged with a p^+ substrate on the collector, n^+ buffer layer (PT IGBTs only), n^- drift region, p^- body region and n^+ emitter as shown in Figure 2.1. The difference between PT and NPT as shown in Figure 2.1 is the additional n^+ buffer layer to increase the blocking voltage capabilities in the PT cell structure.

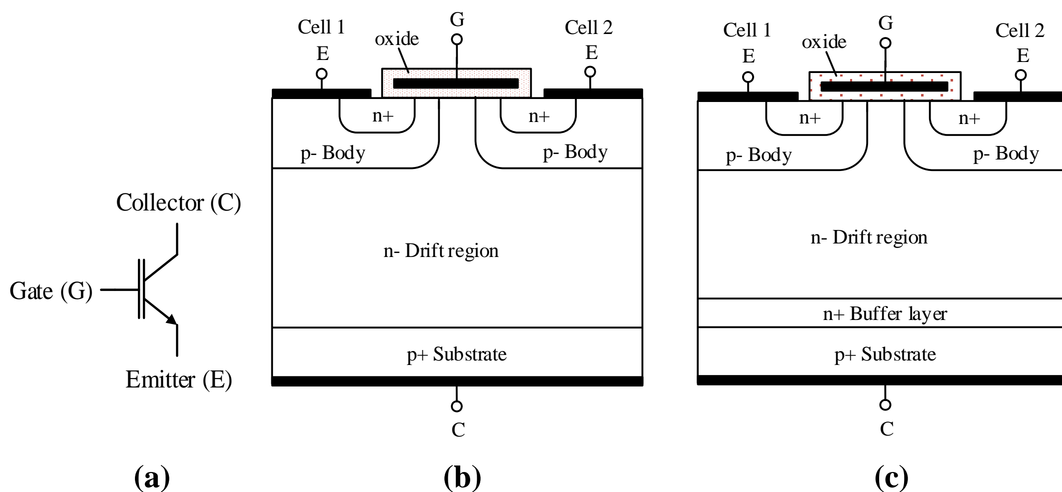


Figure 2.1: (a) IGBT Symbol; (b) Planar Gate NPT and (c) Planar Gate PT Basic Cell Structures [51, 52].

While Figure 2.1 shows PT and NPT structures with planar gate; PT and NPT structures can also be designed with a trench gate as shown in Figure 2.2. Although planar gate appeals more for easy fabrication, trench gate allows narrower cell pitches hence larger channel aspect ratio compared to planar gate [53, 54]. The number of IGBT cells in an IGBT chip determines the current capability of the IGBT device. Consequently trench gate is the mostly used technology over planar gate because cells can be densely packed for greater current capability.

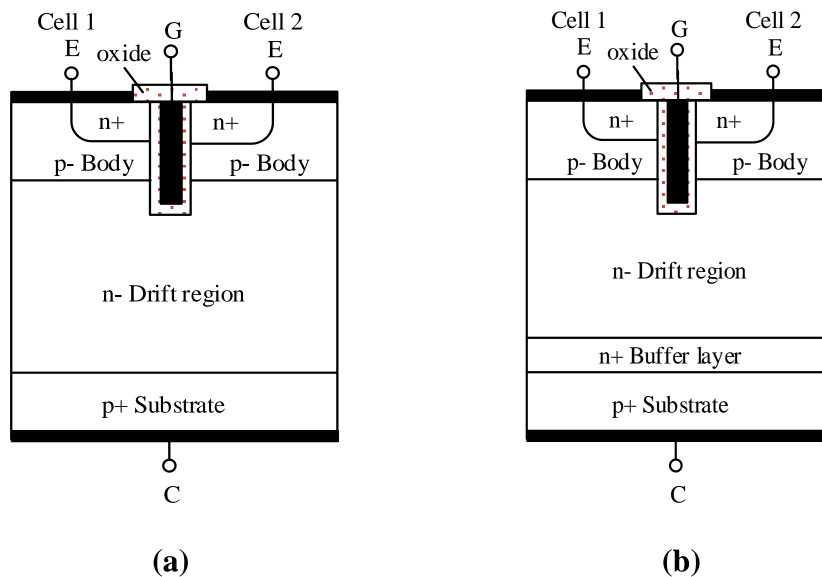


Figure 2.2: IGBT Trench Gate Cell Structures: (a) NPT, (b) PT [52-54].

2.2 IGBT Operation

2.2.1 IGBT Turn-on

The p-n layers of an IGBT are arranged that when the IGBT is forward biased with a positive supply on p^+ collector and the negative on n^+ emitter and gate, V_{CE} is blocked by the lack of a continuous electron path (n-channel) between the J1 in Figure 2.3 and the n^+ emitter. The n-channel absence also results in reverse-bias on J1 hence V_{CE} is blocked. In this way, the IGBT switching relies on the status of the IGBT gate supply.

A close look at the IGBT gate reveals a MOS structure which exhibits inherent capacitances. A positive polarity on the gate induces an n-channel on the p- body beneath the oxide. The n-channel only forms when the gate voltage surpasses the

threshold voltage, $V_{GE(th)}$, at which the parasitic gate input capacitances become charged. Once the n-channel is established, J1 and n^+ emitter are bridged allowing electrons (e^-) to flow from the emitter through to the collector and holes (h^+) in the opposite direction. This constitutes the IGBT's switch-on as shown in Figure 2.3(b).

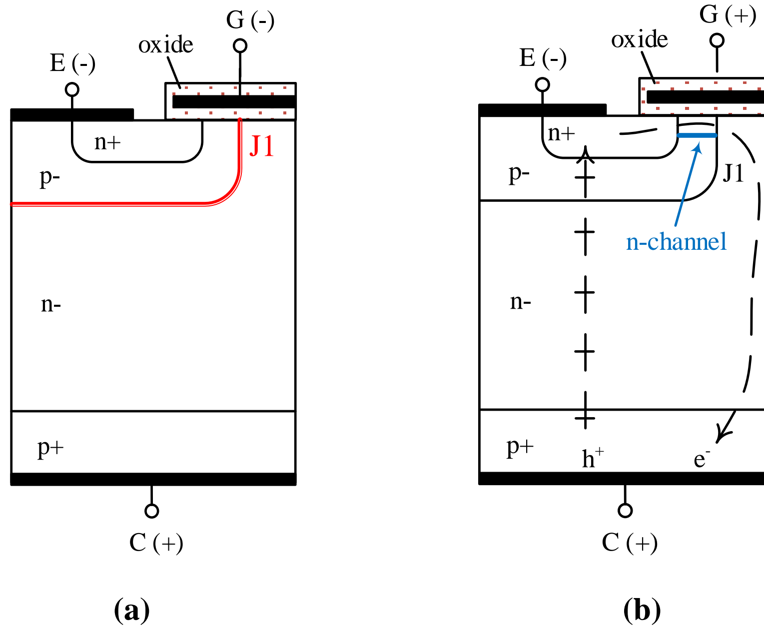


Figure 2.3: IGBT Operating States: (a) IGBT-off (Blocking State), (b) IGBT-on (Conducting State).

Analogous to MOSFETs, the MOS gating in IGBTs allows very high input impedance, fast switching speed and relatively small gate voltage to drive the IGBTs [6, 55, 56]. In practice, IGBTs are rated for a maximum turn-on gate voltage of 20 V [57]. However, typical threshold gate voltages for IGBTs to switch-on are in the region of 8V and only 15 V is required to maintain V_{CE} at absolute low on-state value, $V_{CE(sat)}$. Hence a gate voltage of +20 V would turn-on IGBT 'too hard'. This causes a high electric field hence stress in the dielectric region, and can reduce the lifetime of the device. On the other hand, if the IGBT is not driven hard enough, this increases switching losses. In addition, the on-state voltage drop will not go down to its absolute low value as required to minimise on-state losses. Consequently, +15 V is the optimal gate supply voltage that is commonly used in order to prevent driving the gate too hard but hard enough to achieve low on-state voltage drop, $V_{CE(sat)}$ [58].

To ensure safe operation, IGBT gate drivers are employed to regulate the gate supply. In addition IGBT gate drivers offer protection such as IGBT turn-on short circuits and prevention of spurious turn-on by dV_{CE}/dt [17].

2.2.2 IGBT Turn-off

IGBT switch-off is achieved when the gate voltage is below $V_{GE(th)}$ at which the n-channel that is formed in the turn-on process is depleted. Once the n- channel is depleted, the IGBT enters the off-state. In the turn–off process IGBTs may inadvertently switch back-on through dV_{CE}/dt spuriously re-charging the gate and driving IGBT back on. Immunity against this is attained by using a negative gate voltage turn-off. Typical maximum negative gate voltage rating for IGBTs is -20 V. As explained above for IGBT turn-on, rather than -20 V, typically -10 V is employed to ensure optimal IGBT operation. Most IGBT gate drivers provide gate supply voltage regulation as well as control of the IGBT turn-off process.

Another technique to prevent spurious IGBT switch-on through dV_{CE}/dt during the turn-off process, is by using a high external gate resistance $R_{G(ext)}$ in the gate turn-off circuit. For example the DIM800NSM33-F datasheet shows that tests were conducted with 3.9 Ω turn-on external gate resistor, $R_{G(ext),on}$, while a higher resistance value of 6.2 Ω was utilized for the turn-off external gate resistor, $R_{G(ext),off}$ [57].

2.3 IGBT Module Packaging

Mechanical and electrical interfaces facilitate connection of IGBT chip to the application. The interfaces constitute IGBT packaging and are carefully structured for optimal IGBT performance. Two common IGBT packaging types are 1) press-pack and 2) plastic case. Unlike plastic case, press-packs offer double cooling and exclude bond wires for improved reliability. This research focuses on the plastic packaged IGBT power modules as they are popular due to low manufacturing costs and easy to install. Figure 2.4 shows the main components of a standard plastic packaged IGBT power module.

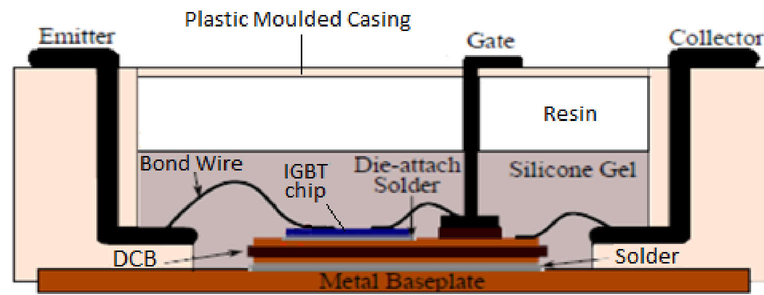


Figure 2.4: Cross-section of IGBT Module Packaging [59].

In order to maintain safe operating temperatures, the heat generated by IGBT chips during operation needs to be efficiently conducted away from the chips. The mechanical interfaces in Figure 2.4 facilitate thermal conduction while at the same time ensuring electrical insulation between the IGBT chips and baseplate. To fulfil both electrical isolation and thermal conduction between an IGBT chip and baseplate, layers of different materials are applied. The materials include copper substrate, direct copper bonding (DCB) substrate, solder and aluminium or copper baseplate, as shown in Figure 2.4. The main considerations in choosing these materials include thermal conductivity, operating temperature range, dielectric strength, volume resistivity, stability, long-term reliability, nontoxicity and shelf life [52].

In Figure 2.4, bond wires and busbars facilitate electrical connections from the IGBT chip to the external electrical terminals. For good bonded joints, wires of small diameter (typically 0.3mm) are utilized for bond wires. For each IGBT chip emitter connection, multiple bond wires are parallel-connected over the chip's emitter surface. This helps in spreading current over the entire IGBT chip emitter surface to avoid current crowding. Due to their thin size, bond wires are not able to conduct heat away thus the main heat path is to the baseplate as described above. In addition to thermal resistance, the thin bond wires introduce significant parasitic inductance that contribute to large peak V_{CE} voltages (overshoot) during switching transients. For this reason, bond wire design has been continuously improved over the years. For example [60] describes the use of ribbons rather than aluminium wire to achieve low parasitic inductance, and improved IGBT switching performance and reliability. However, V_{CE} overshoot risk moving the IGBT device out of the safe operating area (SOA) if the IGBT voltage rating is exceeded hence IGBT power modules often include co pack diode/anti-parallel diode/free wheel diode (FWD) chips for reverse recovery.

In order to complement the low inductance advantage of press-packs, parasitic inductances are further reduced in plastic packs by using high magnetic permeability material around the emitter contact metal. This prevents oscillations and current circulation around IGBT chips [52].

IGBT power modules include a filling silicone gel and epoxy resin as shown in Figure 2.4. Silicone gel provides electrical isolation in the physical space between the components, while epoxy resin prevents ingress of moisture and gases, and provides mechanical protection.

As the minimisation of stray inductance is crucial for IGBT performance, the external circuit layout of the application needs careful design so as to minimise these. One way to achieve this is by using copper busbars instead of cables (or minimising the cable length) for the dc-link. In addition, the gate connection cables (positive and negative) should also be minimised are made short and twisted together to cancel-out noise.

2.4 IGBT Static and Dynamic Performance

Figure 2.5 is an IGBT pulse tester showing an IGBT device under test (DUT) and measuring locations for IGBT electrical signals - V_{GE}, I_G, V_{CE} and I_C for IGBT dynamic performance study. An inductive load is utilized to emulate typical IGBT loading conditions.

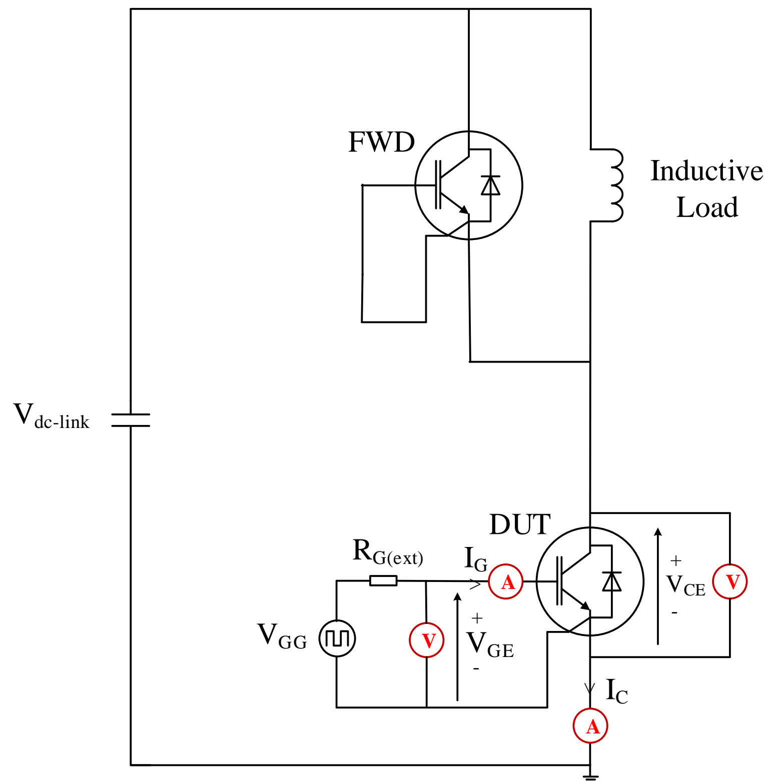


Figure 2.5: IGBT Switching Test Circuit.

2.4.1 Turn-on Process

Figure 2.6 shows combined IGBT waveforms at turn-on.

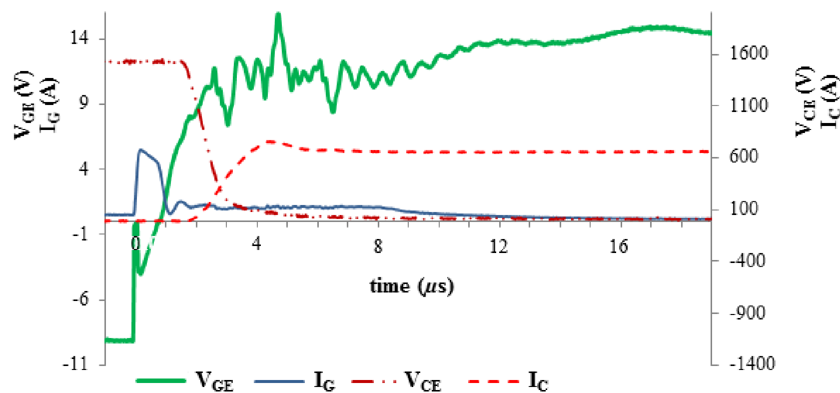


Figure 2.6: IGBT Turn-on Waveforms.

Following IGBT turn-on command, V_{GE} rises and I_G falls exponentially due to the charging of the gate input capacitance, Cies.

$$C_{ies} = C_{ge} + C_{gc} \tag{2.1}$$

where C_{ge} and C_{gc} are the gate-emitter and gate-collector capacitances of the IGBT. The gate-emitter circuit is represented as shown in Figure 2.7.

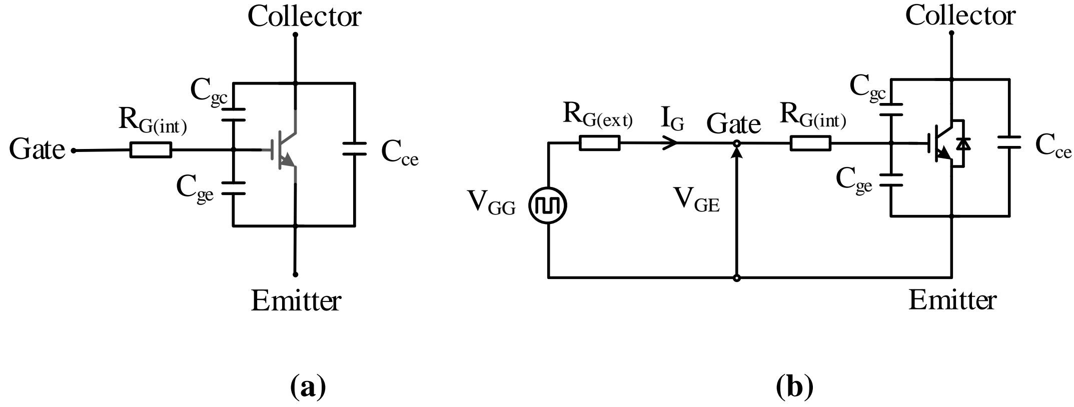


Figure 2.7: (a) Representation of IGBT Inherent Capacitances, (b) Equivalent IGBT Gate-Emitter Circuit.

The gradual rising of V_{GE} and corresponding falling of I_G are described by equations (2.2) and (2.3) [61]

$$V_{GE} = V_{GG}\left(1 - e^{-\left[\frac{t}{R_G C_{ies}}\right]}\right) \tag{2.2}$$

$$I_G = C_{ies}\left(\frac{dV_{GE}}{dt}\right) \tag{2.3}$$

where V_{GG} is the gate supply voltage, t is time and R_G is the total gate resistance which includes IGBT internal gate resistance, $R_{G(int)}$, and external gate resistance, $R_{G(ext)}$.

When V_{GE} reaches the threshold voltage, I_C begins to rise coupled with the transition of V_{CE} from the blocking state as described in (2.4) [28] and (2.5) [62].

$$\frac{dI_C}{dt} = \left[\frac{1}{1 - \alpha_{pnp}}\right]\left[\mu C_{ox}\frac{W}{l}\left(V_{GE} - V_{GE(th)}\right)\right]\left[\frac{dV_{GE}}{dt}\right] \tag{2.4}$$

$$\frac{dV_{CE}}{dt} = \frac{1}{R_G C_{gc}} \left(\frac{V_{GG(on)} - V_{GG(off)}}{1 + \left(\frac{C_0}{G_M R_G C_{gc}} \right)} \right) \quad (2.5)$$

In (2.4) and (2.5) α_{pnp} is the gain of the inherent bi-polar transistor, μ is mobility, W/l is the ratio between width and length of the MOS channel, $V_{GG(off)}$ is the off-state gate voltage supply, $V_{GG(on)}$ is the on-state gate voltage supply, G_M is the trans-conductance, C_0 is charge extraction capacitance and C_{ox} the gate oxide capacitance.

I_C peaks with an overshoot due to stray inductances from the IGBT power circuit and anti-parallel diode reverse recovery charge. Once I_C reaches its peak value, V_{GE} and I_G enter into a Miller plateau and remain constant. During the Miller period, I_C drops from the overshoot to its load value while V_{CE} continues falling and reaches its steady value of $V_{CE(sat)}$ at the end of the Miller plateau.

The Miller effect occurs when the IGBT is in active region thus in (2.1), C_{ge} is no longer active; only C_{gc} is active [61]. Therefore in the Miller period, all the gate input current I_G flows into C_{gc}, discharging it. The reason for V_{GE} and I_G remaining approximately constant during the Miller plateau is because the C_{gc} is getting discharged and at the same time C_{gc} is increasing at a rate which is dependent on the falling V_{CE}. On this account, C_{gc} is known as the Miller capacitance or reverse transfer capacitance, C_{res} [63]. The increase in C_{gc} as V_{CE} falls is portrayed in (2.6) and accounts for the slowdown/tailing-off of V_{CE} in the Miller plateau period.

$$C_{gc} = \frac{A_{GC}\varepsilon_{Si}}{\sqrt{2\varepsilon_{Si}\left(V_{CE} - V_{GE(th)}\right)/qN_B}} \quad (2.6)$$

where A_{GC} is the gate-collector overlap area, ε_{Si} the dielectric constant of silicon, q is the elementary charge and N_B the base doping concentration [64].

On account of the Miller effect described above, the Miller plateau duration, $t_{VGE(miller\ width)}$, is determined by [61]:

$$t_{VGE(miller\,width)} = R_G C_{gc} \left[\frac{V_{CE} - V_{CE(sat)}}{\frac{I_C}{G_M} + V_{GE(th)}} \right] \quad (2.7)$$

Finally after the end of the Miller plateau, the IGBT is completely ON and in its linear region. V_{GE} then continues rising above the Miller voltage towards its maximum value (typically +15 V). Likewise I_G continues to fall below the Miller current to its minimum value.

2.4.2 Turn-off Process

Figure 2.8 shows combined IGBT waveforms at turn-off.

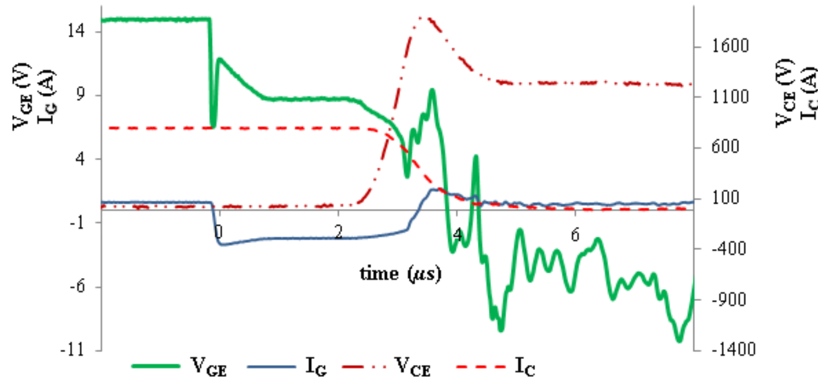


Figure 2.8: IGBT Turn-off Waveforms.

The turn-off process follows a corresponding analysis described for turn-on. Initially, V_{GE} abruptly drops to the Miller voltage and so does I_G. At Miller level, V_{GE} is still above $V_{GE(th)}$ hence V_{CE} and I_C remain in their steady-state values for IGBT on-state. The duration of the Miller plateau is obtained using (2.7). After the Miller level, V_{GE} decreases exponentially as described in (2.8) due to the discharging of the gate input capacitance, C_{ies}. When V_{GE} drops below $V_{GE(th)}$ the IGBT begins to switch-off, with I_C falling and V_{CE} rising linearly towards the blocking voltage (with an overshoot due to stray inductance). I_C follows the exponential change in V_{GE} as expressed in (2.9) [61].

$$V_{GE} = \left(\frac{I_C}{G_M} + V_{GE(th)} \right) e^{-\left[\frac{t}{R_G C_{ies}} \right]} \quad (2.8)$$

$$I_C(t) = \left(I_C + G_M V_{GE(th)}\right) e^{-\left[\frac{t}{R_G C_{ies}}\right]} - G_M V_{GE(th)} \quad (2.9)$$

In theory, the final portion of I_C fall is slower due to the decay of excess carriers by recombination in the n^- drift region of the IGBT. This portion of I_C is called collector current tail ($I_{C(tail)}$) and impedes the turn-off speed of IGBTs. $I_{C(tail)}$ is given by [65] as,

$$I_{C(tail)} = \frac{q D_{nE} p_0^2(t)}{A_E l_{nE} N_{AE}} e^{\frac{-2t}{\tau_{HL}}} \quad (2.10)$$

where p_0 is the hole concentration, q is charge, N_{AE} is the minority carrier doping concentration, l_{nE} is the diffusion length for electrons in the p^+ collector substrate, D_{nE} is the diffusion coefficient for minority carriers in the p^- body region, τ_{HL} is the high-level lifetime decay of carriers.

2.4.3 Power Losses

As described above, the IGBT switching phases are characterized with the V_{CE} either going from the blocking state to the conduction state for turn-on or vice versa for turn-off. This allows I_C to switch on or off as required. Ideally IGBTs should switch in such a way that V_{CE} and I_C do not cross-over during the switching phase. In reality, the switching of IGBTs is non-ideal; V_{CE} and I_C tend to cross-over during the switching transient and a small voltage drop, $V_{CE(sat)}$ occurs in the conduction phase. This results in unsolicited power dissipation during the IGBT switching and conduction phases as depicted in (2.11) and Figure 2.8.

$$P_{D(total)} = P_{D(turn\text{-}on)} + P_{D(turn\text{-}off)} + P_{D(conduction)} \quad (2.11)$$

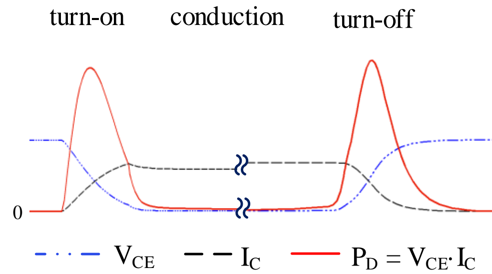


Figure 2.9: Illustration of Total Power Dissipation from IGBT Switching and Conduction Phases.

To reduce high losses associated with the switching transitions portrayed in Figure 2.9, some IGBT gate drivers utilize soft switching techniques such as zero voltage switching (ZVS) and zero current switching (ZCS). ZVS is where a resonant condition is created to force V_{CE} to fall to the saturation level, $V_{CE(sat)}$, before I_C starts rising. Likewise in ZCS, I_C is forced to fall to zero before V_{CE} starts rising to the blocking state. Another means to minimize switching losses is by tuning $R_{G(ext)}$ to control IGBT turn-off and turn-on.

2.5 IGBT Modelling and Simulation

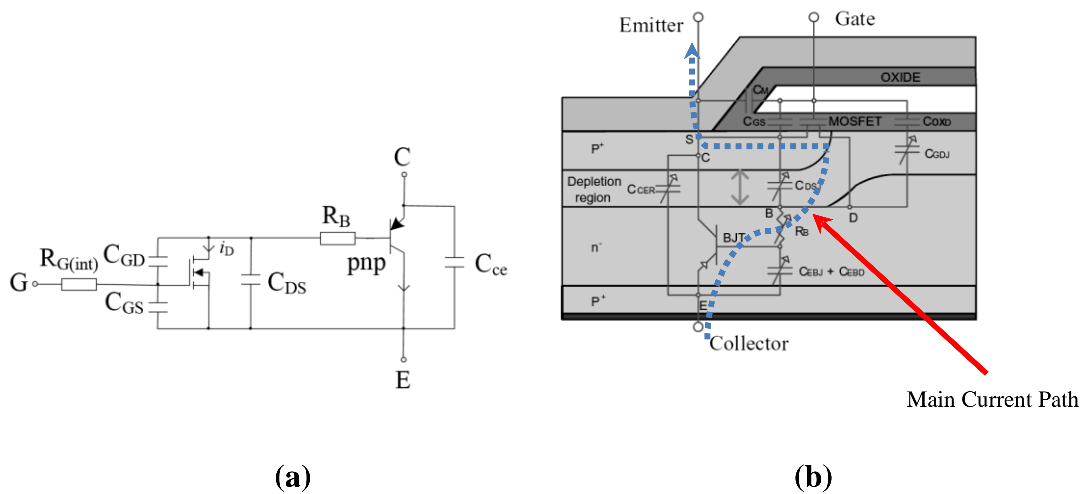
2.5.1 IGBT Equivalent Electrical Circuit

i. Internal Structure

An IGBT model needs to include all of the physical effects that describe IGBT static and dynamic operation. The main influence of IGBT static and dynamic behaviour are the discrete components which make-up the IGBT as well as the parasitic components which are integrated in the IGBT structure as shown in Figure 2.10.

Figure 2.10(a) shows the MOSFET and the parasitic gate input capacitances that are integrated on the IGBT gate. These components control the IGBT turn-on as discussed in section 2.4. Figure 2.10(b) shows the main current path across a series of resistance from the IGBT layers and p-n junctions. These effects can be modelled and simulated by representing the IGBT internal structure as a construction of basic discrete components as depicted in Figure 2.10(b). Consequently, IGBT simulation models are

able to produce IGBT electrical signals and parameters such as voltage drop which represents the IGBT's on-state voltage drop ($V_{CE(sat)}$).



(a) **(b)**

Figure 2.10: The IGBT Equivalent Circuit Superimposed on IGBT Internal Structure [6, 28, 51, 56].

In Figure 2.10(b) the IGBT main current path also encounters capacitive elements lumped up in the collector-emitter capacitance (C_{ce}). The effects of the capacitive elements are mainly observable in the gradual switching transient of the IGBT electrical signals, and impact on IGBT switching losses. Subsequently modelling of all the known IGBT parasitic elements enhances accuracy of the simulation of IGBT electrical parameters which occur in the IGBT conduction and switching phases such as power losses.

While most of the parasitic components within an IGBT cell generally contribute to the losses dissipated by IGBT during switching and conduction, the integrated BJT shown in Figure 2.10 allows the IGBT to have lower conduction losses. This is because the p^+ layer on the collector facilitates conductivity modulation at base depleted region of the integrated BJT resulting in lower on-state voltages. This is why IGBTs are capable of high current ratings even in high temperature operation [6, 56]. On the other hand, the modulated charge carriers in the bi-polar part need time to recombine again when the IGBT is switched-off. This determines the IGBT turn-off speed and has a significant impact on turn-off losses [6]. All these effects are simply modelled by including a BJT in the IGBT equivalent circuit as shown in Figure 2.10.

ii. Packaging

Electrical connections of IGBT chips within the IGBT power module include bond wires, tracks and busbars. These contribute stray elements which are mainly resistive and inductive [40]. Figure 2.11(a) shows the bond wires, tracks and busbars connecting the IGBT chips to the external terminals of the IGBT power module. The resistance (R) and inductance (L) of the bond wires, tracks and busbars are estimated from their dimensions. Figure 2.11(b) illustrates representation of the effective total R and L from the IGBT chip to the gate, collector and emitter external terminals. As the emitter has several parallel-connected bond wires as shown in Figure 2.11(a), for simplicity the R and L contribution from each bond wire is lumped-up and included in the effective total R and L of the chip connections as depicted in Figure 2.11(b).

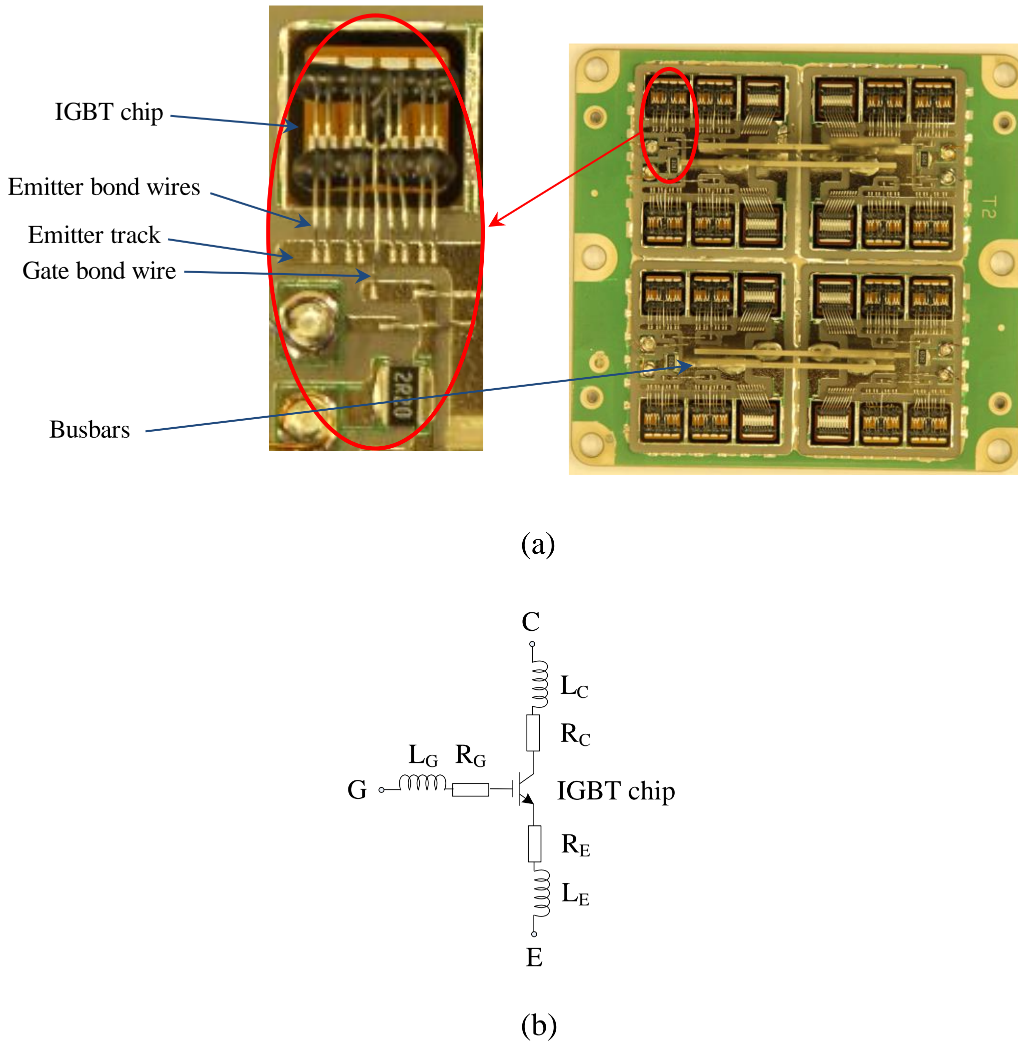


Figure 2.11: (a) IGBT Module Interior and IGBT Chip Close-up. (b) Electrical Configuration of the Resistive and Inductive Elements Associated with IGBT Chip Connections within IGBT Power Module.

While Figure 2.10 portrays on-chip IGBT parasitic resistive and capacitive elements, Figure 2.11 reveals off-chip parasitic resistive and inductive elements. A completed model of an IGBT power module should therefore include both on-chip and off-chip IGBT parasitic elements. The external circuitry which allows connection of IGBT power module to the application also contributes stray elements. Also, these should be taken into account in IGBT simulation. Consequently, the dynamic performance of a complete IGBT simulation model can yield a similar impression to practical results in terms of the characteristic oscillations (ripples), overshoots and gradual switching transient of the IGBT V_{GE}, I_G, V_{CE} and I_C waveforms.

2.5.2 IGBT Equivalent Thermal Network

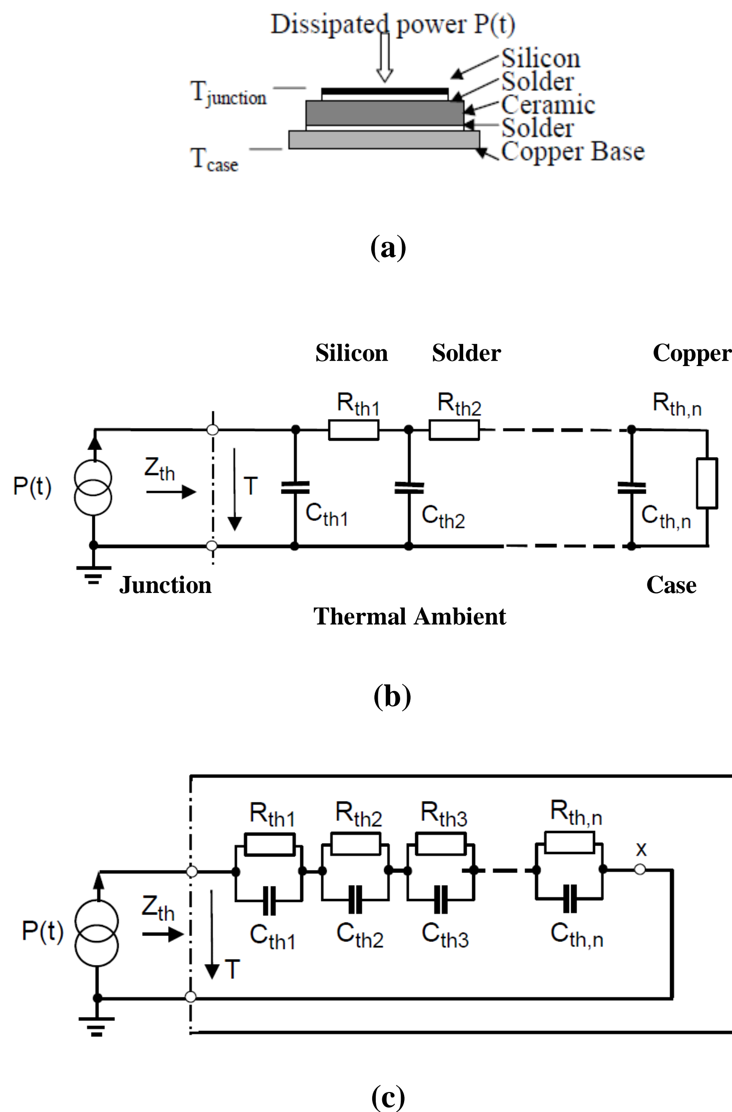


Figure 2.12: IGBT Equivalent RC Thermal Network: (a) IGBT Structure, (b) Cauer Model [37, 66] and (c) Foster Model [66, 67].

Modelling of the IGBT main heat path, IGBT chip to baseplate, facilitates thermo-electric simulation studies such as IGBT power losses, junction temperature, heat flow and temperature performance. Analogous to resistive (R) and capacitive (C) elements which are described in section 2.5.1, IGBT thermal modelling comprises thermally resistive (R_{th}) and capacitive (C_{th}) elements which are produced by the layers of material between an IGBT chip and baseplate shown in Figure 2.12(a). Figure 2.12(b) and (c) show two common methods of thermal representation of the IGBT structure materials between the IGBT chip (junction) and baseplate (case) which are the Cauer model (Figure 2.12(b)) and the Foster model (Figure 2.12(c)).

In Figure 2.12(b) and (c) both models employ the theory of RC circuit time constant to describe the rate of heat propagation away from the IGBT chip. In both models, P(t) is the instantaneous IGBT power dissipation. The main difference between the models is that the Cauer model RC layers are arranged in order of their physical location on the IGBT device. On the hand the Foster model is a simplified mathematical description of the layers as a whole hence the RC nodes have no relation with the physical arrangement of the IGBT layers. For this reason the RC network in Figure 2.12(c) are enclosed in a border signifying a 'black box'. This implies that node 'x' in Figure 2.12(c) does not represent the case interface as in Figure 2.12(b). Therefore the Foster model has the disadvantage that if an additional layer needs to be added, heat sink for example, the system would have to be re-measured and re-calculated as a whole. For a Cauer model, the heat sink can be added to extend an existing RC thermal network as shown in Figure 2.13.

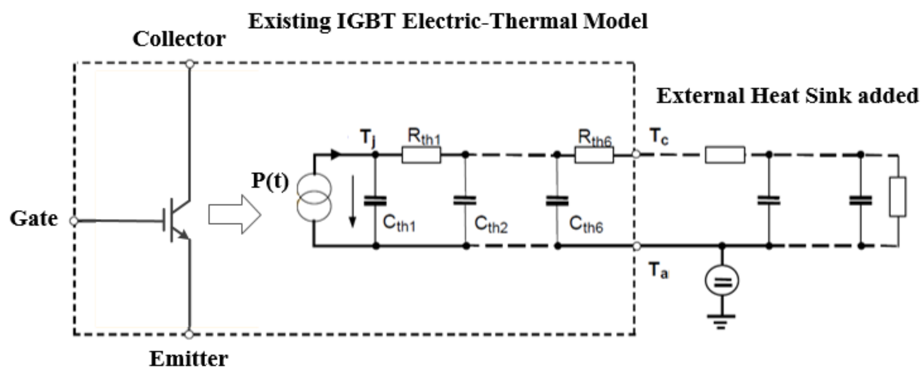


Figure 2.13: Coupling of Additional Thermal Component (Heat Sink) to an Existing Cauer-based IGBT Model [66].

In the Cauer model, the relation between T_j and T_C is described in (2.12).

$$T_j = T_c + P_D \bullet Z_{th(jc)} \quad (2.12)$$

In (2.12) P_D is the IGBT power loss dissipation and $Z_{th(jc)}$ the thermal impedance between the IGBT junction and case. Thermal resistance (R_{th}) and capacitance (C_{th}) of the IGBT structure layers are estimated from their dimensions using (2.13) and (2.14). These can be validated experimentally from a thermal impedance curve [68].

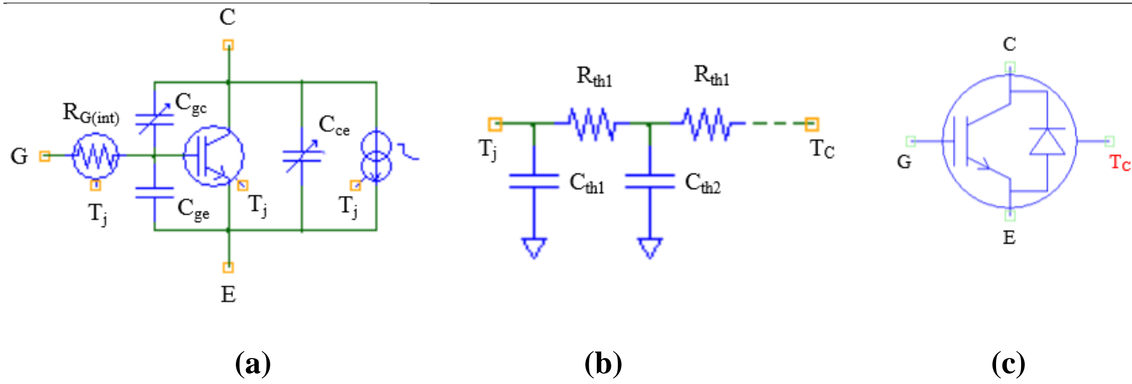
$$R_{th} = \frac{l_t}{k \bullet A_L} \quad (2.13)$$

$$C_{th} = c \bullet d \bullet l_t \bullet A_L \quad (2.14)$$

In (2.13) and (2.14), A_L is the cross-sectional area of a layer, l_t is the thickness of material along heat flow path across the layer, k is thermal conductivity, c is the specific heat capacity and d is the density of the layer material [68].

2.5.3 IGBT Modelling and Simulation Based on SaberRD

The extensive range of IGBT applications accounts for the variation in IGBT types available in the market. This constrains any simulation package from containing, in its parts libraries, every kind of IGBT a user may need to study. In particular, 3.3 kV, 800 A IGBT power module DIM800NSM33-F chosen as the reference module in simulation and experimentation of this research has no simulation model readily available in the market. A DIM800NSM33-F simulation model derived from the datasheet was created in SaberRD. The developed IGBT simulation model is shown in Figure 2.14.



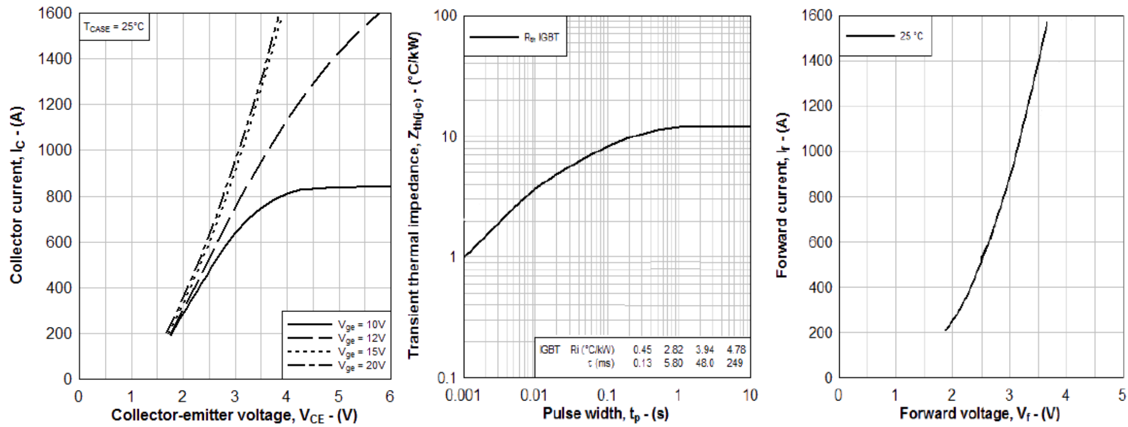
(a) (b) (c)

Figure 2.14: Dynamic Thermal IGBT Module Characterized in SaberRD: (a) Equivalent Electrical Circuit, (b) Thermal Resistance and Capacitance (RC) Network, and (c) Symbol with a Thermal Case Terminal (T_C).

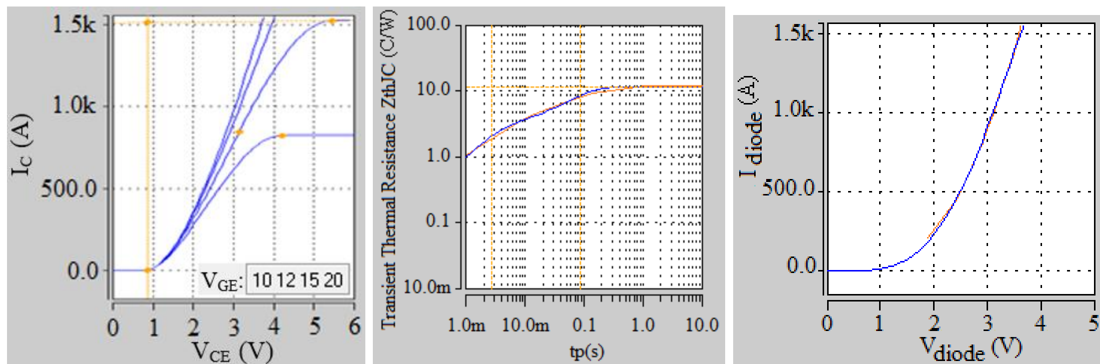
In Figure 2.14, the thermal RC network is a Cauer model representing the thermal elements which lie in the layers of the IGBT structure material between the IGBT chip and case (baseplate). In Figure 2.14(c), the IGBT electro-thermal model has 3 electrical terminals - C, G and E - connected to the component model of the electrical network and a thermal terminal - T_C - connected to the thermal network component model. The electrical model is a temperature-dependent model and computes the device electrical parameters (V_{GE}, I_G, V_{CE} and I_C) in terms of IGBT chip surface temperature at that instant (that is, it is based upon the temperature dependence of the IGBT model parameters and variation of silicon properties with temperature). On the other hand, the thermal model determines the evolution of temperature distribution in the thermal network thereby calculates the instantaneous silicon surface temperature values which are supplied to the electrical model. In this manner, the dynamics of the IGBT electro-thermal interactions are accounted for.

Figure 2.15 illustrates typical IGBT datasheet characteristics that have been input in the IGBT simulation model in SaberRD. Other datasheet characteristics are shown in Appendix A. These include gate charge (Q_g), C_{ies}, C_{res}, $V_{GE(th)}$, module inductance (L_M), $R_{G(int)}$, switching times, energy losses and FWD reverse recovery and output characteristics. In the DIM800NSM33-F IGBT model developed, the RC elements have been characterized to match the junction-to-case transient thermal impedance, $Z_{th(jc)}$, characteristics provided in the datasheet. The $Z_{th(jc)}$ curve from the datasheet is shown in Figure 2.15(a). The curve data was input into the IGBT simulation model using a scanning facility on the SaberRD IGBT modelling tool. The resulting $Z_{th(jc)}$ curve of the

model is shown in Figure 2.15(b). A command file of the characterized model is then produced in the form of a MAST source code shown in Appendix A. The MAST code can be added to the user's parts library. The output from the developed DIM800NSM33-F simulation model matches characteristics provided in datasheet as portrayed in Figure 2.15. A further validation of the developed simulation model is the matching simulation and experimentation results in Chapter 7.



(a)



(b)

Figure 2.15: Characterization of the DIM800NSM33-F Characteristic Curves: I_C-V_{CE} Output Characteristics, Transient Thermal Impedance and Anti-parallel Diode I-V Forward Characteristics: (a) Datasheet [57], (b) Simulation.

It should be noted that section 2.4 specifies that the modelling of IGBT modules must consider all parasitic components within IGBT power module such as IGBT chips, anti-parallel diode chips and bond wires. The effects of these components are included in IGBT datasheet parameters and characteristics since the IGBTs are measured from the

external terminals. Since simulation model is based on the IGBT datasheets, the model includes the on-chip and off-chip R, L and C parasitic elements which have been discussed in this chapter.

2.6 Summary

IGBT structure and operation have been discussed. Parasitic components integral in the IGBT structure and packaging which are influential in IGBT static and dynamic performance have been revealed. Stray elements which are contributed by IGBT external connections to the application have been described. This chapter has concluded with IGBT electro-thermal modelling and simulation which considers the IGBT structure and packaging as well as external circuitry components.

The next chapter contains an overview of online IGBT health monitoring.

Chapter 3. In-situ Health Monitoring Techniques

Health monitoring is a technique where the on-going health of a component is determined by directly measuring one or more parameters that have characteristics related to the fitness/health of the component. This chapter presents a health monitoring methodology as guidance for practical implementation. The techniques are applied to IGBTs such that the IGBT does not require removal from the application for testing. Therefore IGBT health monitoring is often referred to as in-situ or online health monitoring. The chapter includes comparison of in-situ health monitoring with other health monitoring methods like the fuses and canaries. It is clearly shown that in-situ health monitoring is the preferred technique that provides a better insight of IGBT health status while in field thus improving the reliability of IGBTs.

3.1 Background of Health Monitoring

Health monitoring is a successful technique employed in different fields of engineering to improve or predict reliability of components. Table 1.1 has highlighted various techniques applying health monitoring to IGBTs. Other health monitoring applications include induction motor stator fault online diagnosis [69] and aerospace engine monitoring to identify engine shutdown problems before they threaten airplane operation and safety [70].

Unlike fuses and canaries where an expendable device is embedded into a host component so that its failure provides advance warning of time to failure of the host component [71], in-situ health monitoring is based directly on the component thus provides better insight of the component's health status. Figure 3.1 illustrates the main functions of a health monitoring system.

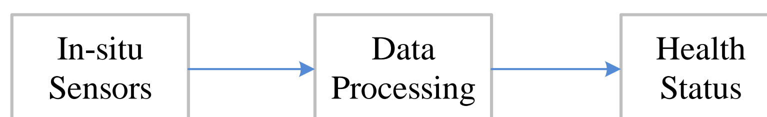


Figure 3.1: Block Diagram of a Health Monitoring System.

In Figure 3.1, the three main parts for a health monitoring system - in-situ sensors, data processing and health status output - are discussed next.

3.1.1 In-situ Sensors

In Figure 3.1 in-situ sensors are required in order to measure a failure precursor – a parameter of the component which can indicate its health status. In order to identify a suitable failure precursor, a failure mechanism of the component being monitored must be identified and characterized.

The main challenge for in-situ sensors is that when measurements are taking place, the normal operation of the component should not be disturbed. In addition, the complexity of the measurement system or modifications of the component should be avoided to reduce the impact on implementation costs and reliability of the application. However today these issues are often overcome with the help of advances in technology.

Additional sensors may be added that measure environmental conditions in order to determine if the same operational or environmental conditions for health monitoring are met. In implementing health monitoring, it is difficult and expensive to consider sensors for all the environmental and operation conditions/loading. To overcome this challenge, only the loads that may dominate stress in the system may be considered and the rest neglected. For instance, in aerospace applications, the effects of radiation may be ignored because radiation levels are low enough during flight [71]. An alternative is by using information on lifecycle conditions to eliminate failure mechanisms that may not occur under given application conditions [71]. For example, where steady-state temperature results are sufficient to assess failure conditions, a temperature cycle experiment to determine a particular failure mechanisms can be adequately defined by determining the highest and lowest steady-state temperature conditions.

3.1.2 Data Processing

In Figure 3.1 once measurements are sampled by in-situ sensors, the measured data is processed and the health status is output. Three common approaches in data processing are: Data-driven, Physics of Failure (PoF) and Hybrid.

i. Data-driven

The Data-driven approach uses available and historical information to statistically and probabilistically derive decisions, estimates and predictions about the health and reliability of the system or component [71]. As it is based on statistics and probability, this method does not require a thorough understanding of the failure mechanisms of a given process, and hence only works well if loads and the response behaviour of the component or system into the future are similar to those observed in the past. The Data-driven approach is therefore not sensitive enough for effective monitoring until the ultimate failure occurs.

ii. Physics of Failure (PoF)

Unlike data-driven, a PoF based system considers actual operational and external environmental loading conditions, and requires an understanding of the dependence of damage or failure on the operational and external environmental loading conditions. For example if a connector responds differently to small and large operational loads, a PoF model will be needed to describe changes in the bent flange for the different loading levels [72]. PoF is therefore ideal for predicting reliability throughout lifecycle including manufacture, storage and usage.

iii. Hybrid

Hybrid is a combination of Data-driven and PoF hence a more effective approach.

3.1.3 Health Status Output

As indicated in Figure 3.1, the ultimatum for health monitoring is outputting the health status of the component. With the help of lifetime models like Coffin Manson’s law, information such as the remaining lifetime of component can be determined based on pre-determined wear out mechanism. Coffin-Manson law is expressed as follows [37]

$$N_f = Af^{-a} \Delta T^{-b} e^{\frac{E_a}{k_B T_m}} \tag{3.1}$$

where N_f is the number of cycles to failure which represents remaining useful life; A, a and b are coefficients; f is the frequency of the switching cycle or input frequency [73],

(the output frequency - load cycle frequency, can also be utilized [74]); ΔT is the temperature variation and T_m the mean temperature of the application profile; E_a is the activation energy, which is a constant related to the chemical property of the material and k_B is the Boltzmann's constant [37]. ΔT and T_m of the mission profile are obtained using counting and sorting algorithms like the real-time rainflow algorithm [75].

As described in equation 3.1, temperature swing, ongoing temperature profile and switching frequency or load cycle frequency have an impact on wear and tear which can be utilized in lifetime prediction of the component. Although switching frequency is usually higher than load cycle frequency and would have a higher impact on temperature and lifetime prediction according to (3.1), either or both the switching frequency and load cycle frequency can be incorporated and their effect depends on the converter topology and location of the component under test on the circuit [73].

3.2 IGBT Failure Mechanisms

The application of health monitoring to IGBTs requires investigation of common IGBT failure sites. IGBTs fail in two ways: wear-out failure and sudden failure. Wear-out failure occurs when accumulated environmental or operational stress of the device exceed the endurance limitation of a device. On the other hand, sudden failure is caused by mechanical shock such as vibrations or electrical shock from exposure to influences like cosmic radiation, voltage collapse or electrical discharge. Sudden failures are usually activated by the extreme end of wear-out failures when the component finally gives in. Table 3.1 highlights common IGBT failure types which are discussed next.

Table 3.1: Common IGBT Failure Mechanisms and Sites [71].

Failure mechanism	Failure site
Corrosion	Metallization
Electro-migration [76]	Metallization
Conductive filament formation	Between metallization
Stress-driven diffusion voiding	Metal traces
Latching [42]	Parasitic thyristor
Time-dependant dielectric breakdown [52, 76]	Dielectric layers
Fatigue	Die attach, bond wires, bond pads, solder leads, traces, interfaces

3.2.1 IGBT Wear-out Failures

i. Corrosion

It was highlighted in Chapter 2 that silicone gel and epoxy resin protect the ingress of moisture and gases into the power module. Imperfections or failure of the silicone gel or epoxy resin allows oxygen to escape into the power module resulting in corrosion of the copper layers on both sides of the DCB substrate. This leads to short circuits or current leakage between the gate and emitter.

ii. Electro-migration

High current density on the IGBT chip results in atomic migration which causes the silicone gel surrounding emitter bond wires to solidify due to thermal effect. Eventually the bond wire temperatures heat up until they melt and lift-off.

iii. Time Dependent Dielectric Breakdown (TDDB)

High temperature generated by the IGBT chip and strong electric field increases the kinetic energy of charge carriers so much that the thin gate oxide (SiO_2) suffers from fatigue and break down. Consequently excessive leakage current occurs and the IGBT response time is affected.

iv. Fatigue

Fatigue is a common failure mechanism in IGBT chips caused by mismatch of the coefficient of thermal expansion (CTE) of different materials in the IGBT structure. Thus the repetitive temperature swings due to pulsed operation of IGBTs causes fatigue of the layer joints through bimetallic effect resulting in failures like solder cracking and bond wire lift-off. When a bond wire lifts-off/fails, the load current is reallocated to the remaining bond wires and overloading them. The overloaded bond wires suffer from electrical overstress (EOS) and a series of the bond wires begin to fail and eventually the IGBT chip fails outright [77].

The most critical interface of solder fatigue failure is represented by the solder between the ceramic substrate and the copper base plate which has the worst mismatch of CTE [16]. Consequently maximum temperature swing is experienced here. When the ceramic cracks and copper layer of the DCB lifts-off, this creates voids which have high thermal resistance leading to uneven heat flow across the IGBT chips and inhomogeneous current sharing of the chips.

Other consequences of fatigue include void and holes on the thin aluminium metallization which also leads to uneven heat on the surface of the metallization and current density becoming uneven due to variances in the metal sheet resistance.

3.2.2 IGBT Sudden Failures

i. Latch-up

Latch-up occurs when too large values of dV_{CE}/dt during turn-off trigger the parasitic thyristor in IGBTs [78]. This is noticeable with a sudden collapse of V_{CE} as the gate can no longer control the switching since the collector, emitter and base become short-circuited.

ii. External radiation

External radiation and cosmic rays cause ionisation and displacement damage in the device. A single event of expose to radiation can induce catastrophic burn-out of the device [79].

iii. Partial Discharge

Partial discharge mainly occurs as a result of cracks in the DCB which are caused by fatigue. The cracks in the DCB ceramic causes the DCB substrate to become uneven thus reducing the distance between the two copper layers. When high-voltage occurs over the metallization edges and the interface in silicone gel is big enough to exceed the breakdown voltage limitation, a sudden flash-over discharges between the two copper layers [56].

3.3 IGBT In-situ/Online Health Monitoring Techniques

The offline methods are based in the laboratory or measurements take place when the IGBT is physically removed from the converter; with online health monitoring, the measurement circuit is physically embedded in the power converter and measurements are carried out during in-field operation. Many IGBT online health monitoring techniques have been proposed, for example, ringing characterization. In ringing characterization, high-order oscillatory responses (ringing) present in V_{CE} and I_C of the system reflect on ageing of the device [80].

In section 3.2, it has been pointed out that the main cause of IGBT failures are thermo-mechanical effects due to thermal cycling/temperature swings [81]. Therefore any changes in the health status of the IGBT as a result of common failures in power modules like bond wire lift-off and solder fatigue are reflected in IGBT temperature/T_j change. For this reason, a majority of IGBT online health monitoring methods employ TSEPs to monitor T_j and evaluate the state of health of a particular IGBT failure site [21, 43, 44, 82, 83]. The safe operating range for T_j is limited. Depending on the IGBT chip material, semiconductor manufacturers state a maximum temperature of 125 °C to 175 °C [84, 85]. Therefore T_j monitoring is also necessary to ensure T_j stays within safe operation limits.

However, due to packaging, T_j is inaccessible for direct contact temperature measurements. Various indirect T_j measurement techniques have been reported, for example, spread spectrum time domain reflectometry (SSTDR) [86, 87]. In [86, 87] SSTDR determines the drain source resistance (R_{DS}) of a MOSFET by injecting ac signals into the gate. R_{DS} is temperature dependent and by computing the reflections of

the injected ac signal, T_j can be determined. SSTDR is a new trend in indirect T_j measurement and requires many components making this approach expensive.

The mainstream approaches for measuring T_j are thermal-electric modelling and TSEPs.

3.3.1 Thermal-Electric Modelling

Thermal-electric models are commonly employed in power electronic converters estimating T_j using equation (2.12) in Chapter 2. As per equation (2.12), thermal-electric models use case temperature, T_C, from a temperature sensor adhered to the base plate/heatsink, and power loss calculation [88]. It is well known that thermal-electric modelling has inaccuracies and therefore models must include a safety factor resulting in higher estimated T_j levels which reduces the amount of power that can be delivered [89].

Various thermal-electric models have been published trying to increase accuracy, estimation speed or reduce model complexity [36, 37, 90]. Thermal-electric models, however, have two distinct disadvantages. The first disadvantage is that the technique requires knowledge of the IGBT chip power losses during switching events and conduction periods. Thus instantaneous voltage and current measurements are required which are difficult to implement practically. The second disadvantage is the fact that thermal-electric models do not represent every IGBT power module from the same manufacturing batch due to manufacturing tolerances.

3.3.2 TSEPs

TSEPs is a technique where T_j is measured indirectly by measuring one or two electrical parameters that have defined temperature (T_j) dependencies [15]. Measuring these electric parameters provide consequently knowledge of T_j. Thus unlike thermal-electric models, TSEP is a measurement of T_j and not an estimation of T_j.

The TSEP technique involves characterization of IGBTs where a look-up table (LUT) with defined TSEP/T_j relationship is characterized. When the TSEP is measured in application, T_j is computed using the LUT. This thesis proposes the use of a TSEP as an HSP for IGBT chip failure detection for multichip IGBT power modules. The use of a LUT as described above facilitates the chip failure detection as the baseline TSEP/HSP

value will change with every chip loss and detected based on the decision statements stored in the LUT. On this account, many online TSEPs have been published which are presented in Chapter 4 and five new online TSEPs are proposed in Chapter 6.

3.4 Summary

The chapter has presented a background of health monitoring. A guidance has been provided for applying in-situ health monitoring to IGBTs. Common IGBT failure sites have been revealed and failure mechanisms described. Thermal cycling has been highlighted as a common cause of IGBT failures due to layers of different materials on the IGBT structure having mis-matching CTEs. Consequently the use of online TSEPs for IGBT in-situ health monitoring has been proposed. The next chapter is an overview of common IGBT TSEPs.

Chapter 4. Temperature-Sensitive Electrical Parameters

Chapter 3 has shown that T_j monitoring is crucial for IGBT safe operation and health monitoring. In addition, it has been highlighted that TSEPs are the mainstream choice for T_j estimation/monitoring compared to thermal-electric models. This chapter describes the operation and practical implementation of twelve online/in-situ TSEPs which can be applied to multichip HV IGBT power modules. In addition, the analytical electric-thermal equations behind each TSEP are shown. Such in depth study across the twelve in-situ TSEPs on multichip HV IGBT power modules has not been presented before. Hence the presented comprehensive work and investigation in this chapter is unique.

4.1 TSEP Classification

Literature review of various publications over the past three decades has revealed eighteen IGBT TSEPs. Figure 4.1 SaberRD simulations illustrate some of the TSEPs on IGBT waveforms.

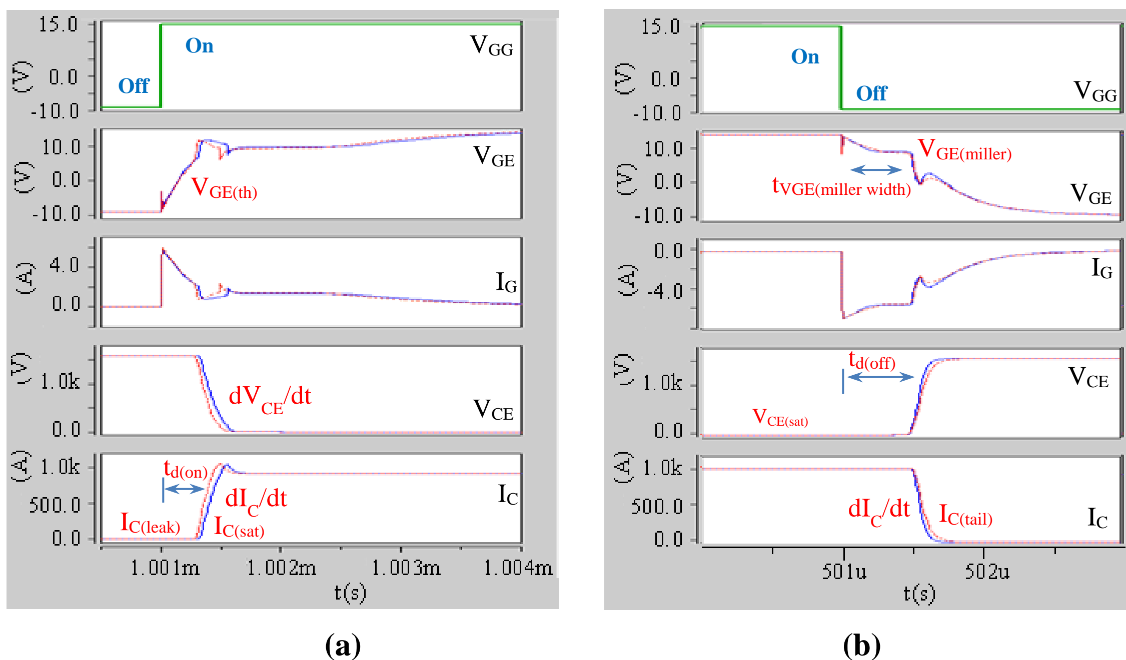


Figure 4.1: TSEPs on IGBT Waveforms (Temperature 1 - Blue solid line; Temperature 2 - Red dashed line) – (a) IGBT Blocking and Turn-on Phases (b) IGBT Conduction and Turn-off Phases.

TSEPs can be classified into online and offline TSEPs. Online TSEPs include a measurement system that is practically embedded in the power converter and measurements are carried out during in-field operation. Online TSEPs can therefore also be described as in-situ T_j measurements. In this regard, offline TSEPs are those measurements where the IGBT power module is physically to be removed from the application and tested in the laboratory.

The main objective in this research is online TSEP with a key focus on practical implementation in real applications. In principle any online TSEP technique can be used for offline TSEP measurement, but a few offline TSEP techniques cannot be applied for online TSEP measurement. For example [3, 33, 91] propose the measurement of the breakdown voltage and [56] describes the measurement of the latching current as TSEP but both techniques work close to the destruction of the device, causing the risk of a catastrophic failure and are therefore unsuitable to be considered for online TSEP. The differential voltage between the main emitter and auxiliary emitter of IGBT power modules ($V_{EE'}$) during IGBT switching has also been proposed as an online TSEP in reference [34]. However, this TSEP is limited to modules that have an auxiliary emitter terminal hence cannot be applied to discrete IGBT devices.

Online TSEPs can be categorized as "one-step" or "two-steps". Two-steps TSEPs determine the T_j from at least two temperature-dependent electric parameters that are measured and then processed as one value. Examples for two-steps TSEPs are internal gate resistance ($R_{G(int)}$) [29-31], Trans-conductance (G_M) [27, 56, 76] and power loss dissipation (P_D) [35, 36]. For instance, P_D measures the on-state voltage and conduction current that are then processed into power losses P_D. As both the on-state voltage ($V_{CE(sat)}$) and the conduction current (I_C) are temperature dependent so is their product P_D and thus P_D can be classified as a two-steps TSEP. Due to their nature in measuring at least two different parameters (mostly voltage and current) two-steps TSEPs require two different types of sensors increasing cost, packaging and measurement errors. The error in the calculation of T_j increases further due to numerical calculation errors. In addition processing the data adds coding requirements that can be challenging for low-cost applications where ultra-low-cost microprocessors are used that have very limited data memory. TSEPs that correlate T_j directly to one measured electric parameter of the IGBT power module are called one-step direct TSEPs. The associated number of

sensors and data processing complexity rule out two-steps TSEPs in favour of one-step TSEPs. Consequently, screening and categorising of the TSEPs resulted in 12 online TSEPs listed in Table 4.1. that can be applied to IGBTs which are all one-step TSEPs.

Table 4.1 shows that online TSEPs can be classified into 'Gate-emitter' or 'Collector-emitter'. These categories describe the access points for the electric parameter measurement at the IGBT power module. IGBT power modules have three terminals: gate, emitter and collector. Thus TSEPs are either measured from a gate-emitter circuit or from a collector-emitter circuit. The fundamental difference in this category is that voltage measurement between gate-emitter does not require isolation whereas voltage measurement between collector-emitter does require isolation.

Table 4.1: Online TSEP Classification.

	TSEP	Gate-emitter / Collector-emitter
1	Gate-emitter Miller plateau voltage level ($V_{GE(miller)}$), at IGBT turn-off [92]	Gate-emitter
2	Gate-emitter voltage Miller plateau width ($t_{VGE(miller\ width)}$), at IGBT turn-off [62, 77]	
3	Gate-emitter threshold voltage ($V_{GE(th)}$) [25, 26, 76, 91-97]	
4	Collector-emitter voltage slope (dV_{CE}/dt), at IGBT turn-off [62, 98]	Collector-emitter
5	Collector current slope (dI_C/dt), at IGBT turn-on [27, 28, 92]	
6	Collector current slope (dI_C/dt), at IGBT turn-off [92]	
7	Collector current tail ($I_{C(tail)}$) [92]	
8	Collector saturation current ($I_{C(sat)}$) [33, 93, 97, 99]	
9	Turn-on delay ($t_{d(on)}$) [28, 92]	both
10	Turn-off delay ($t_{d(off)}$) [28, 42, 56, 92, 94]	
11	Collector-emitter saturation voltage ($V_{CE(sat)}$) [2, 21-24, 37, 38, 56, 76, 91, 94, 96, 97, 100-102]	Collector-emitter
12	Collector leakage current ($I_{C(leak)}$) [56, 94]	

4.2 Online TSEPs Overview

The 12 online TSEPs in Table 4.1 are analysed further in this section. In order to illustrate the TSEP trends and performance on multichip HV IGBT power modules, simulations were conducted for each of the 12 TSEPs. The simulations used here are for illustration only to demonstrate the change of the waveform at different temperatures within the typical IGBT operating temperature range and consequently to demonstrate

the change of the online TSEP parameter. The results obtained help to compare the different TSEPs.

The IGBT power module DIM800NSM33-F (3.3 kV, 800 A) from Dynex Semiconductor Ltd was chosen as a reference module and utilized in the simulations. The DIM800NSM33-F IGBT is a trench gate soft punch through IGBT of the sixth generation [57]. Details of the IGBT devices, the generation and the packaging are important as TSEPs vary with manufacturing technologies, generation status and packaging. For example the on-state voltage drop and turn-off losses of PT and NPT IGBTs have different temperature sensitivities [52]. Likewise with every new IGBT chip generation, TSEPs are changing. For instance, Infineon's IGBT saturation voltage $V_{CE(sat)}$ has dropped with every new launch of a new IGBT generation [103]. Finally, power module manufacturers have different packaging and IGBT chip connection technologies which impacts on the measurement accuracy of TSEPs.

Table 4.2 shows some of the temperature-sensitive data provided in datasheet for the DIM800NSM33-F.

Table 4.2: Electrical Characteristics of the DIM800NSM33-F (at V_{CE} = 1800 V, I_C = 800 A, V_{GE} = +/-15 V, Stray Inductance (L_S) = 100 nH [57]).

Parameter	T_C = 25 °C	T_C = 125 °C
$V_{GE(th)}$	6.5 V	Not provided
$V_{CE(sat)}$	2.8 V	3.6 V
Turn-on delay, $t_{d(on)}$	1.3 μs	1.2 μs
Turn-off delay, $t_{d(off)}$	3.02 μs	3.1 μs
Rise time	275 ns	315 ns
Fall time	270 ns	280 ns
Turn-on energy loss	1.25 J	1.75 J
Turn-off energy loss	1.05 J	1.2 J

4.2.1 Simulation Set up

A DIM800NSM33-F simulation model derived from the datasheet was realized in SaberRD. Electro-thermal simulations were employed using Figure 4.2 IGBT pulse tester to investigate online TSEPs.

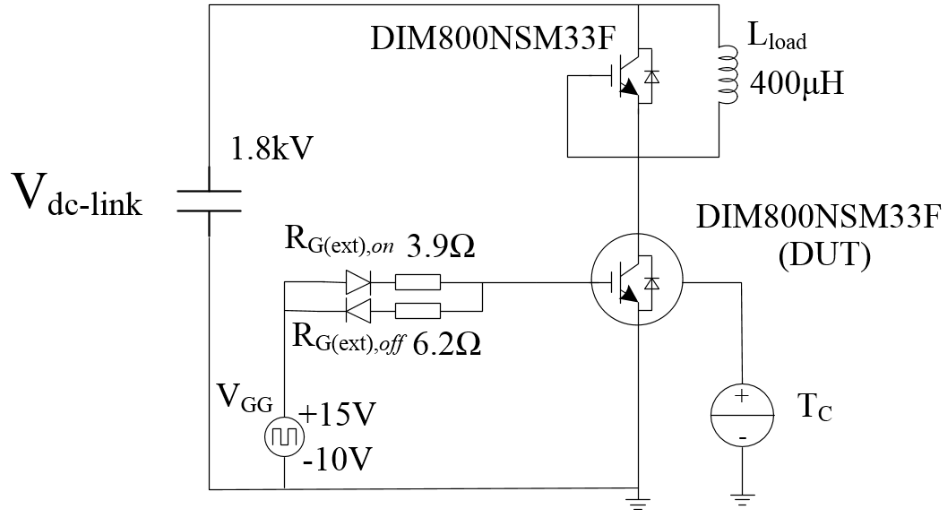


Figure 4.2: IGBT TSEP Characterization Circuit Implemented in SaberRD.

In Figure 4.2, the IGBT DUT is a dynamic electro-thermal model with three electrical IGBT pins and one thermal pin defining the IGBT case interface. As such, the temperature source connected to the IGBT thermal pin is utilized to vary the IGBT case temperature (T_C). This alters the IGBT T_j according to equation (2.12) in Chapter 2 and enables examination of TSEP performances at different IGBT T_j's.

The supply was set to 1800V dc, 800 A dc and a 400 μH inductive load produce the required dc-link current levels for the IGBT pulse tests. This size of inductance is typically used in HV IGBT pulse tests [27]. The gate-emitter of the top IGBT is short circuited thus the top IGBT is off at all times. The top IGBT was employed for its anti-parallel diode which can generate reverse recovery effects. The IGBT under test was pulsed from an ideal pulsed voltage supply operating from -10 V to +15 V at a frequency of 1 kHz which is typical for high-power applications [9, 73]. External gate resistors of 3.9 Ω for turn-on and 6.2 Ω for turn-off were utilized between the ideal pulsed voltage generator and the gate of the IGBT.

4.2.2 Simulation Results for 12 Online TSEPs

i. TSEPs at IGBT turn-on phase

Figure 4.3 shows temperature-dependencies of four TSEPs at the IGBT turn-on phase: $V_{GE(th)}$, $I_{C(sat)}$, dI_C/dt and $t_{d(on)}$. The TSEPs were measured from 20 ºC (blue solid bold

line) to 120 ºC (red dashed bold line), every 20 ºC. On IGBT waveforms, some of the TSEPs have temperature changes which are more visible and dominant than others. The reason is the scaling of the y and x axis but is not a reflection on the resolution. Thus the simulation results in Figure 4.3 include the IGBT waveforms to show change of the TSEPs at different T_{vj}, as well as graphs of TSEP versus T_{vj} in order to show the sensitivity of the TSEPs.

In Figure 4.3, three of the TSEPs have approximately a linear behaviour with the temperature while $I_{C(sat)}$ is approximately exponential. All TSEPs show falling values with increasing temperatures except dI_C/dt and $I_{C(sat)}$ where values are rising with increasing temperatures.

The sensitivity of $V_{GE(th)}$ over the temperature range is -10 mV/ºC. Thus $V_{GE(th)}$ is easy to detect. However, $V_{GE(th)}$ requires two sensors: one to measure the voltage and another one to measure the emitter current that triggers the voltage measurement. That is because $V_{GE(th)}$ is defined as the voltage when the IGBT starts conducting. The required current sensor is placed at the bottom of the emitter increasing cost and packaging constrains. It is possible to avoid adding a current sensor by making use of the parasitic inductance (L_M) of the IGBT power module. Instead of measuring the current directly voltage $V_{EE'}$ is measured across the emitter Kelvin connector of the power module and the main emitter terminal. The relationship between $V_{EE'}$ and the temperature T_j is [34].

$$V_{EE'}(\mathbf{Tj}) = L_M \cdot \frac{dI_C}{dt}(\mathbf{Tj}) \tag{4.1}$$

In principal this method can be used for all successive collector current measurements discussed in section 4.2.3. $V_{GE(th)}$ can be analytically expressed as follows [61, 94]

$$V_{GE(th)}(\mathbf{Tj}) = V_{FB} + 2\left(\frac{k_B T}{q}\ln\frac{N_A}{n_i(\mathbf{Tj})}\right) + \frac{\sqrt{2\varepsilon_{ox}\varepsilon_{si} q N_A 2\left(\frac{k_B T}{q}\ln\frac{N_A}{n_i(\mathbf{Tj})}\right)}}{C_{ox}} \tag{4.2}$$

where in (4.2) V_{FB} is flat-band voltage, ε_{ox} ε_{si} are the dielectric constants of oxide and silicon respectively, q is the elementary charge, k_B is the Boltzmann's constant, N_A is surface concentration of the channel region, and C_{ox} is gate oxide capacitance, T is the channel temperature and n_i is the intrinsic concentration.

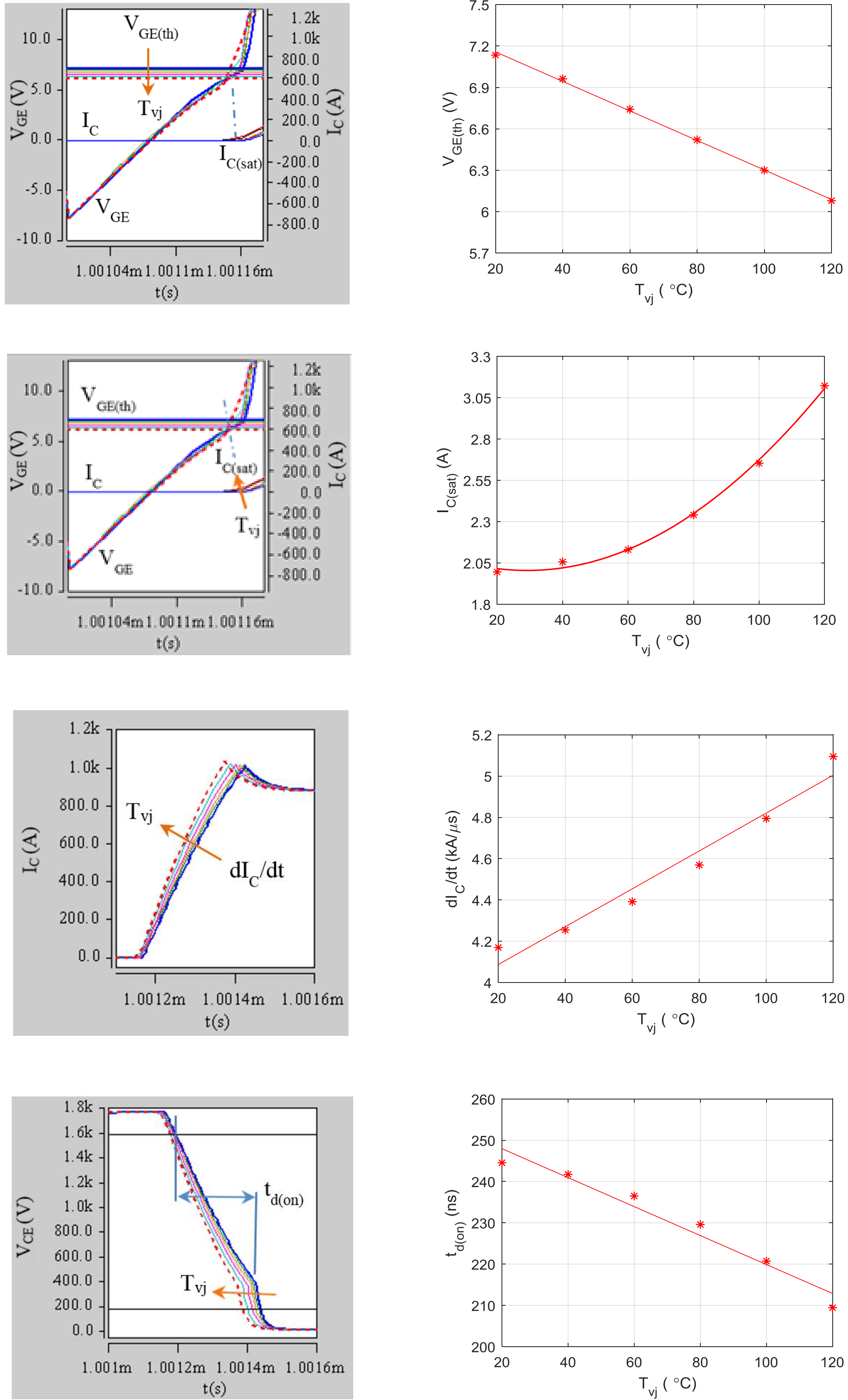


Figure 4.3: Temperature Variation of TSEPs at IGBT Turn-on.

$I_{C(sat)}$ is the collector current that flows at the gate threshold voltage, $V_{GE(th)}$, where the IGBT is on the verge of turning on from the off-state. Under this condition, the channel in the MOS portion of the IGBT cell is pinched-off and its current is saturated hence the term $I_{C(sat)}$ [65]. The main disadvantage of $I_{C(sat)}$ it is dependent on $V_{GE(th)}$. To avoid an additional sensor to measure $V_{GE(th)}$, $I_{C(sat)}$ is measurable with a current sensor connected to the emitter of the IGBT and switching the IGBT with a constant gate-emitter voltage only some hundreds of millivolts above the IGBT threshold voltage [99]. However this kind of testing would require the IGBT to be off duty to prevent interference with the application's normal operation. The temperature dependence of $I_{C(sat)}$ is evident in (4.3) [33].

$$I_{C(sat)}(\mathbf{Tj}) = \left(1 + \beta_{pnp} \frac{\mu_{ns}(\mathbf{Tj}) C_{ox} W_{ch}}{2 l_{ch}}\right) \left(V_{GG} - V_{GE(th)}(\mathbf{Tj})\right)^2 \quad (4.3)$$

In (4.3), β_{pnp} is the current gain of the bi-polar transistor in IGBT, μ_{ns}, the surface mobility of electrons in the channel, W_{ch}, the channel width, l_{ch}, the channel length. The quadratic term in (4.3) indicates that $I_{C(sat)}$ is exponential, becoming higher with rising temperature as depicted in Figure 4.3. The exponential nature of $I_{C(sat)}$ in Figure 4.3 implies a poor sensitivity at low temperatures that would affect measurement accuracy at low temperatures. At temperatures in excess of 50 °C, sensitivity is in the tens of milliamps per degrees Celsius which can be detected.

The dependence of dI_C/dt with temperature is evident during IGBT turn-on when dI_C/dt is rising [35]. Figure 4.3 depicts a positive linear temperature relation of dI_C/dt [27].

$$\frac{dI_C}{dt}(\mathbf{Tj}) = \left[\frac{1}{1 - \alpha_{pnp(\mathbf{Tj})}}\right] \left[\mu(\mathbf{Tj}) C_{ox} \frac{W}{l} \left(V_{GG} - V_{GE(th)}(\mathbf{Tj})\right)\right] \left[\frac{dV_{GE}}{dt}\right] \quad (4.4)$$

In (4.4) α_{pnp} is the gain of the inherent bi-polar transistor, μ is the mobility of charge carriers, W/l is the ratio between the width and the length of the MOS channel, and C_{ox} is the oxide capacitance.

Fast sampling current measurements are required for dI_C/dt. Once the converter control board commands the turn-on of the IGBT, current (I_C) sampling is triggered and an algorithm calculates the change of the dI_C/dt gradient. According to Figure 4.3, dI_C/dt requires sensitivity in the region of 9 A/μs·°C, of which existing technology may not

cope. Hence the IGBT switching transient may entail slowing down, for instance increasing the value of gate resistor in order to take the samples [104, 105]. dI_C/dt gradient values are first zero (off-state), then turn high (turning-on) and finally turn back to zero (on-state). A technique that avoids the use of fast data processing is by connecting a current sensor to the emitter of the IGBT power module and including a Schmitt trigger that detects a lower current band which triggers a fast counter and an upper current band that stops the counter. The defined upper and lower current bands in combination with the time from the counter results in dI_C/dt.

The final TSEP of the four is $t_{d(on)}$ which describes the time between the gate signal from the controller board (or V_{GE} rising edge) and the time the collector current starts rising. This TSEP does not require fast current sampling but a current sensor attached to the emitter of the module. This current sensor detects the start of the IGBT current (I_C) rise and the time difference between the current rise and the control signal which is known as $t_{d(on)}$. Alternatively $t_{d(on)}$ is described as the time taken for V_{CE} to decrease from 90% to 10% [42]; in this way, a second sensor to measure V_{GE} is not necessary. $t_{d(on)}$ equation is shown in (4.5) [28, 52, 92]:

$$t_{d(on)}(\mathbf{Tj}) = R_G(\mathbf{Tj})\left(C_{gc} + C_{ge}\right)\ln\left(1 - \frac{V_{GE(th)}(\mathbf{Tj})}{V_{GE}}\right) \quad (4.5)$$

ii. TSEPs at IGBT On-state and Off-state Phase

Between the turn-on phase and the turn-off phase the IGBT is either ‘on’ or ‘off’ allowing two TSEPs to be detected: $V_{CE(sat)}$ when the device is ‘on’ and $I_{C(leak)}$ when the device is ‘off’. $V_{CE(sat)}$ is the collector-emitter voltage drop that results during the IGBT conduction state [94]. $V_{CE(sat)}$ has a linear relation with temperature depicted in (4.6) [65] and Figure 4.4 with a tail off at higher temperatures.

$$V_{CE(sat)}(\mathbf{Tj}) = \frac{2k_BT}{q}\ln\left[\frac{J_CW_N}{4qD_an_iF(W_N/2l_a)}\right](\mathbf{Tj}) + \left[\frac{pl_{ch}J_{ch}}{\mu_{ni}C_{ox}\left(V_{GG} - V_{GE(th)}\right)}\right](\mathbf{Tj}) \quad (4.6)$$

In (4.6) D_a is the ambipolar diffusion coefficient, $F(W_N/2l_a)$ is function of N-drift region width over twice ambipolar diffusion length, p is the hole concentration, J_{ch} is the current density, J_c collector current density and μ_{ni} the inversion layer mobility [65].

Under a small collector current, $V_{CE(sat)}$ has a negative temperature coefficient. This is because at small current, the p-n junction voltage for the inner transistor of IGBT is in effect. This is associated with the first bracket in (4.6) which has the physical parameters of the internal resistance that decreases with temperature. Under high collector current, $V_{CE(sat)}$ has a positive temperature coefficient reflected in the second bracket of (4.6) which comes into effect with the long N-base (MOS channel) resistance increasing with temperature due to the negative temperature dependence of μ [38, 94].

$I_{C(leak)}$ is the current that flows in the IGBT blocking state. Figure 4.4 portrays an exponentially rise of $I_{C(leak)}$ with temperature. This is because as temperature increases, the generation and movement of charge carriers becomes acute [94]. Therefore diffusion current increases, resulting in the exponential rising of $I_{C(leak)}$ depicted in (4.7) [94]:

$$I_{C(leak)}(\mathbf{Tj}) = qA_L \frac{n_i^2(\mathbf{Tj})}{N_B}\sqrt{\frac{D_n}{\tau_n(\mathbf{Tj})}} + \frac{qA_L n_i(\mathbf{Tj}) x_d}{\tau_n(\mathbf{Tj})} \tag{4.7}$$

where A_L is channel area, n_i is intrinsic carrier doping concentration, τ_n is lifetime of space charge region, D_n is diffusion coefficient of electron, x_d is diffuse length at high temperature, q is the elementary charge and N_B is surface concentration.

Figure 4.4 shows that the sensitivities of $V_{CE(sat)}$ and $I_{C(leak)}$ are in the order of tens of millivolts and tens of milliamps per degrees Celsius respectively. Detecting voltages and currents at these low levels are achievable so long only one IGBT power module is in use in a power converter (for example single-phase step-up dc/dc converter). If more than one IGBT power module is in use (for instance three phase inverter) voltage and current detection can be challenging due to the associated EMI noise caused by the other switches.

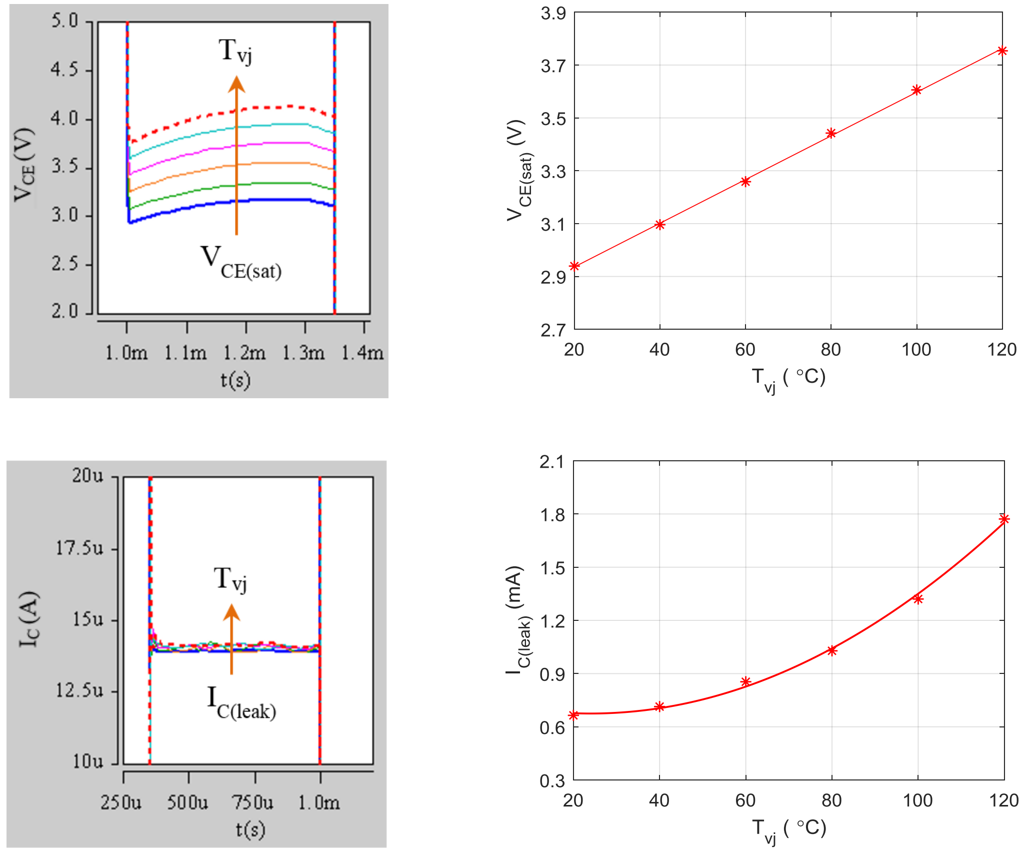
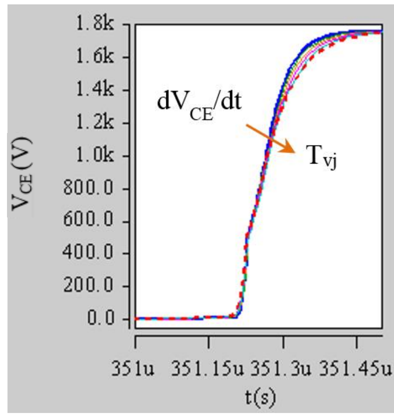
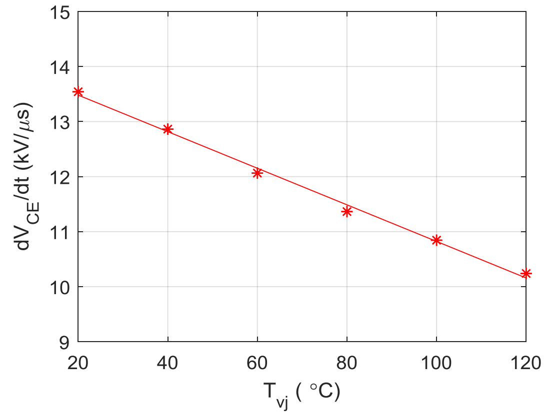


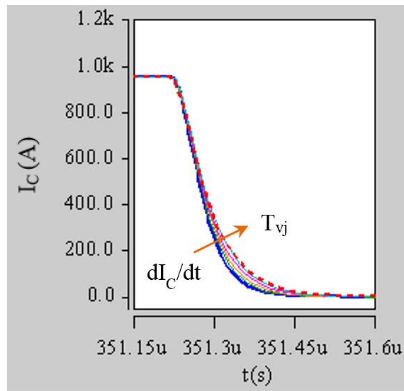
Figure 4.4: Temperature Variation of $V_{CE(sat)}$ and $I_{C(leak)}$.

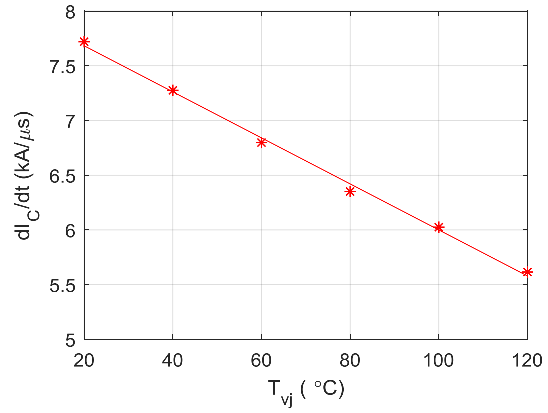
iii. TSEPs at IGBT turn-off phase

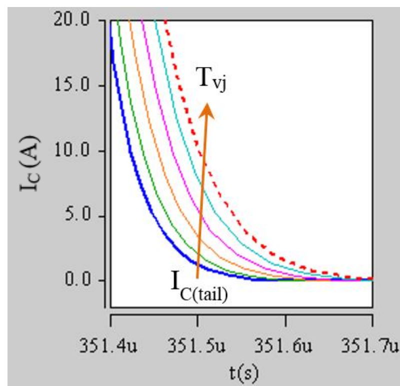
Six TSEPs have been reported for the turn-off phase: dV_{CE}/dt, dI_C/dt, $I_{C(tail)}$, $t_{d(off)}$, $t_{VGE(miller\ width)}$ and $V_{GE(miller)}$. Figure 4.5 shows the temperature dependencies of all six TSEPs.

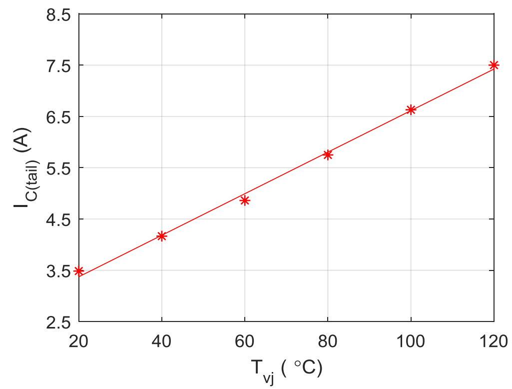

dV_CE/dt
T_vj
V_CE (V)
t(s)

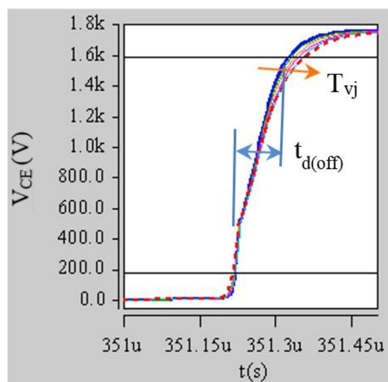

dV_CE/dt (kV/μs)
T_vj (°C)

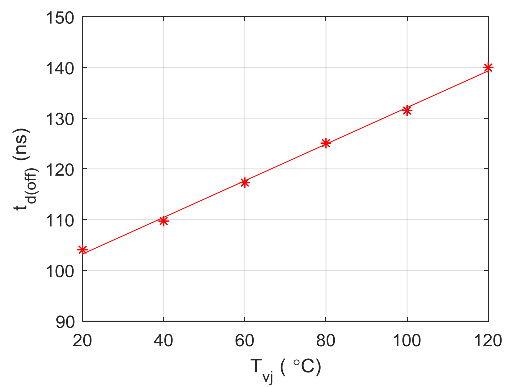

T_vj
dI_C/dt
I_C (A)
t(s)


dI_C/dt (kA/μs)
T_vj (°C)


T_vj
I_C(tail)
I_C (A)
t(s)


I_C(tail) (A)
T_vj (°C)


T_vj
t_d(off)
V_CE (V)
t(s)


t_d(off) (ns)
T_vj (°C)

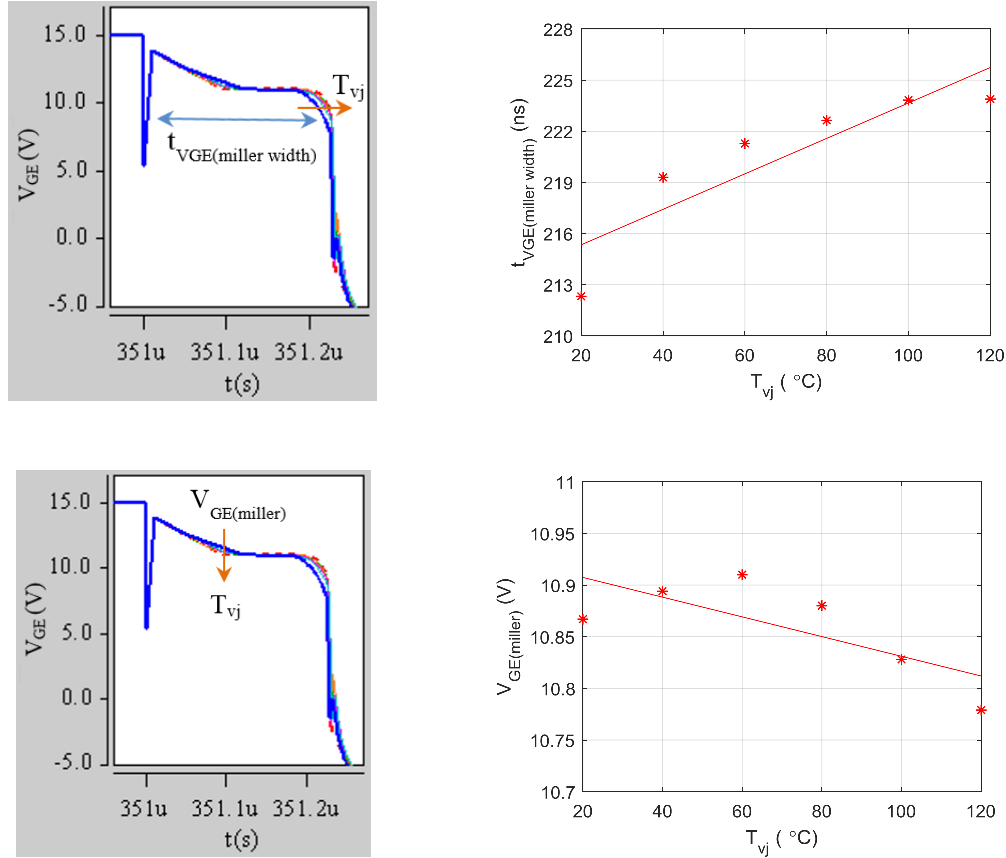


Figure 4.5: Temperature Variation of TSEPs at IGBT Turn-off.

The collector-emitter voltage rise time dV_{CE}/dt has also been proposed as a TSEP. The IGBT V_{CE} slope, dV_{CE}/dt, during IGBT turn-off has a negative linear temperature relationship [62, 98] depicted in Figure 4.5. Equation (4.10) [98] below shows the temperature dependent parameters that account for the negative linear temperature co-efficiency of dV_{CE}/dt.

$$\frac{dV_{CE}}{dt}(\mathbf{Tj}) = \frac{1}{R_G(\mathbf{Tj})C_{gc}}\left(\frac{V_{GG(on)} - V_{GG(off)}}{1 + \left(\frac{C_O}{G_M(\mathbf{Tj})R_G(\mathbf{Tj})C_{gc}}\right)}\right) \tag{4.8}$$

dV_{CE}/dt measurement follows the same principle described for dI_C/dt in the previous section but using a voltage sensor across the collector and emitter of the IGBT power module.

dI_C/dt at IGBT turn-off has a negative temperature coefficient as opposed to dI_C/dt when the IGBT is turned-on. However, they follow the same principal equation (4.4). The

only difference is that the slope of dI_C/dt at the turn-on phase is steeper than dI_C/dt at the turn-off phase.

$I_{C(tail)}$ is the tailing or slow fall of the collector current waveform in the final portion during turn-off [65]. $I_{C(tail)}$ increases with temperature and its magnitude is dependent on the applied maximum voltage across the IGBT power module. The temperature-dependency of $I_{C(tail)}$ is described in (4.9) [65].

$$I_{C(tail)}(\mathbf{Tj}) = \frac{qD_{nE}p_0^2(t)(\mathbf{Tj})}{A_E l_{nE} N_{AE}} e^{\frac{-2t}{\tau_{HL}}} \tag{4.9}$$

In (4.9) p_0 is the hole concentration, q is charge, N_{AE} is the minority carrier doping concentration, l_{nE} is the diffusion length for electrons in the p^+ collector region, D_{nE} is the diffusion coefficient for minority carriers in the in the p-region, τ_{HL} is the high-level lifetime decay of carriers.

$t_{d(off)}$ is the time between the gate signal from the controller board (or V_{GE} falling edge) and the time the collector-emitter voltage reaches 90% of the final value [28]. Since the turn-off time is dominated by the tail in the collector current waveform, $t_{d(off)}$ is also defined as the time taken for the collector current to decay to 10% of its original value after termination of the gate pulse [56]. Thus $t_{d(off)}$ is alternatively described as the time taken for I_C to decrease from 90% to 10% [56] or V_{CE} to increase from 10% to 90% [42]; in this way a second sensor to measure V_{GE} is not necessary. Unlike $t_{d(on)}$, $t_{d(off)}$ has a positive temperature coefficient and is temperature-dependent through the following equation [92]:

$$t_{d(off)}(\mathbf{Tj}) = R_G(\mathbf{Tj})C_{ies} \ln\left(\frac{I_C}{G_M(\mathbf{Tj})V_{GE(th)}(\mathbf{Tj})} + 1\right) \tag{4.10}$$

where C_{ies} is the input capacitance which comprises C_{gc} and C_{ge}.

dI_C/dt and $t_{d(off)}$ require the same measurement method and sensors as outlined in the previous section for dI_C/dt and $t_{d(on)}$ at IGBT turn-on and are not listed again.

Like dV_{CE}/dt and dI_C/dt, $V_{GE(miller)}$ demands a fast sampling voltage measurement. Gate turn-off waveforms are in the order of hundreds of nanoseconds so sampling rates above 1 MHz are essential. Once the converter control board commands the turn-off of the IGBT, voltage sampling is triggered and an algorithm calculates the change of the dV_{GE}/dt gradient. Theoretically at Miller plateau the gradient is zero so if the algorithm detects a dramatic change in the dV_{GE}/dt slope, $V_{GE(miller)}$ is detected. $t_{VGE(miller\ width)}$ also requires sampling rates above 1 MHz but more recorded data is required compared to the data for $V_{GE(miller)}$. This is because $t_{VGE(miller\ width)}$ must record the event when V_{GE} goes into the Miller plateau and when it comes out of the Miller plateau. It is possible for $t_{VGE(miller\ width)}$ to avoid fast sampling measurement by using a Schmitt trigger device that sets an upper and a lower limit of the Miller plateau. Once the gate-emitter voltage hits the lower threshold band a counter starts and when the voltage hits the upper limit bans the counter stops resulting in the Miller plateau width time. $V_{GE(miller)}$ and $t_{VGE(miller\ width)}$ can be analytically expressed as follows (equation (4.11) [92, 106, 107] and (4.12) [62, 77]).

$$V_{GE(miller)}(\mathbf{Tj}) = V_{GE(th)}(\mathbf{Tj}) + \frac{I_C}{G_{M(sat)}(\mathbf{Tj})} \tag{4.11}$$

$$t_{V_{GE(miller\ width)}}(\mathbf{Tj}) = \frac{R_G(\mathbf{Tj})C_{gc}\left(V_{dc-link} - V_{CE(sat)}(\mathbf{Tj})\right)}{\left(\frac{I_C}{G_M}(\mathbf{Tj}) + V_{GE(th)}(\mathbf{Tj})\right)} \tag{4.12}$$

In (4.11), $G_{M(sat)}$ is the trans-conductance at pinch-off. In (4.12), $V_{dc\text{-}link}$ is the dc-link voltage.

4.3 Summary

This chapter has described a wide variety of existing IGBT TSEPs. Screening and categorising of the TSEPs resulted in 12 one-step online TSEPs that are preferred for IGBT online applications. The operation and practical implementation of the 12 TSEPs have been described. In addition, the analytical electric-thermal equations behind each of the 12 online TSEPs have been shown.

The TSEPs outlined in this chapter provide a wide variety of TSEP alternatives for online applications. However, as the TSEPs are numerous, TSEP selection can be

challenging. The next chapter provides a guidance for screening TSEPs for online implementation and compares the online TSEPs using comparable TSEP properties.

Chapter 5. Comparison of Temperature-Sensitive Electrical Parameters

TSEPs are not always reliable. TSEP performance depends on various parameters such as TSEP measurement method, IGBT application type, converter topology and IGBT structure type. Therefore a feasibility assessment is necessary before engaging a TSEP for practical application. This chapter provides a guidance for screening TSEPs and describes comparative TSEP properties that influence hardware implementation which include temperature-sensitivity, repeatability, cost and self-heating. The online TSEPs discussed in Chapter 4 are highlighted in these categories.

5.1 TSEP Screening Methodology

The flowchart in Figure 5.1 illustrates a thought process for screening TSEPs. The TSEP screening parameters shown in Figure 5.1 are discussed in the next section.

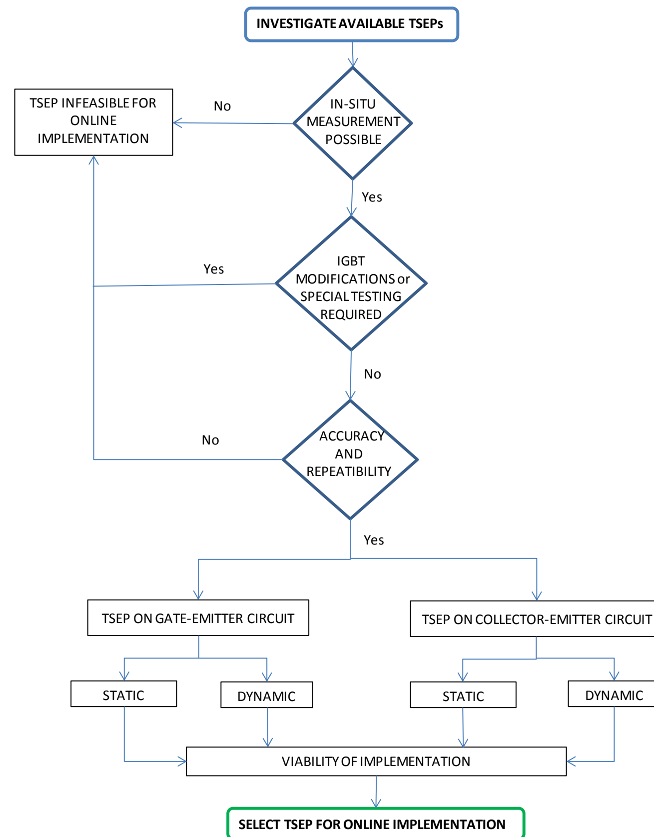


Figure 5.1: Flowchart Guidance of TSEP Screening for Online Implementation.

In Figure 5.1, the initial step is to ensure in-situ measurement of the TSEP is practical. Next, the measurement technique should avoid IGBT modifications to prevent IGBT manufacturing costs. Then feasibility assessments using comparative TSEP properties such as sensitivity, accuracy, self-heating, isolation, complexity and other parameters which reflect on hardware requirements. The TSEP properties are defined in Appendix B. The next section applies the TSEP properties and compares the hardware requirements for online TSEPs.

5.2 Comparison of Online TSEPs

Table 5.1 compares twelve online TSEPs using measurements from the DIM800NSM33-F (3.3 kV, 800 A) IGBT power module simulation results in the temperature range 20 – 120 °C which are discussed in Chapter 4 and compare well with the references provides in Table 5.1.

Table 5.1: Comparison of Traditional Online TSEPs

TSEP	Gate-emitter / Collector -emitter	Static / Dynamic	Voltage/ Current sensor	Sensitivity	Relative Sensitivity	Linearity	Self-heating	Accuracy	Repeat ability
$V_{GE(miller)}$ [92]	Gate-emitter	Dynamic	Voltage	-1 mV/°C	0.01 %/°C	Linear	Yes	10 °C	low
$t_{VGE(miller\ width)}$ [77]			Voltage[2]	0.11 ns/°C	0.05 %/°C	Linear	Yes	8 °C	low
$V_{GE(th)}$ [93]			both	-10 mV/°C	0.15 %/°C	Linear	small	2 °C	low
dV_{CE}/dt [98]	Collector -emitter	Dynamic	Voltage	-34 V/µs°C	0.24 %/°C	Linear	Yes	3 °C	low
dI_C/dt –on [27]			Current	9 A/µs°C	0.18 %/°C	Linear	Yes	5 °C	low
dI_C/dt –off [92]			Current	-22 A/µs°C	0.27 %/°C	Linear	Yes	3 °C	low
$I_{C(tail)}$ [92]			Current	40 mA/°C	0.54 %/°C	Linear	Yes	3 °C	low
$I_{C(sat)}$ [97]			Current	14 mA/°C	0.36 %/°C	Exponential	small	3 °C	low
$t_{d(on)}$ [92]	both	Dynamic	both[2]	-0.36 ns/°C	0.14 %/°C	Linear	Yes	5 °C	low
$t_{d(off)}$ [92]				0.38 ns/°C	0.26 %/°C	Linear	Yes	4 °C	low
$V_{CE(sat)}$ [97]	Collector -emitter	Static	Voltage	8 mV/°C	0.22 %/°C	Linear	Yes	2 °C	low
$I_{C(leak)}$ [94]			Current	10 mA/°C	0.62 %/°C	Exponential	No	1 °C	low

5.2.1 Measurement Point

In Table 5.1, the first TSEP category describes whether the TSEP is measured from the gate-emitter circuit or from the collector-emitter circuit. The fundamental difference in this category is that voltage measurement between gate-emitter does not require isolation or HV insulation whereas voltage measurement between collector-emitter does require isolation.

5.2.2 Static or Dynamic

Table 5.1 also classifies TSEPs into 'static' mode, where IGBTs are either in the conduction or in the blocking mode, and 'dynamic' mode, where IGBTs are in switching transients. As they are measured in the IGBT switching mode, dynamic TSEPs are more sensitive to operating conditions such as switching noise, parasitic components and fluctuations in gate driver performance compared to static TSEPs [15]. IGBT switching transients are in the order of hundreds of nanoseconds hence dynamic TSEPs require high sampling rates above 1 MHz and precise measurement triggering. High sampling voltage sensors are expensive. As several samples are required, data storage becomes an issue.

[2] All sensors are used to read a measured TSEP value except [2] which are used to trigger an event

On the other hand, static TSEPs require a single point measurement only and the measurement of voltage or current do not require high bandwidth sensors.

5.2.3 Sensor Type

In Table 5.1 the third column indicates the type of required sensor. In general voltage sensors are simpler and lightweight compared to current sensors hence voltage-based TSEPs are preferred from a practical perspective [48]. Some TSEPs like $V_{GE(th)}$ require at least two different parameters to be measured (voltage and current). Such TSEPs requiring more than one sensor lead to increased cost, complexity and measurement errors.

5.2.4 Sensitivity

The fourth column in Table 5.1 shows the temperature-sensitivity for each TSEP. Temperature-sensitivity provides an indication of the resolution requirements for the voltage/current sensor. TSEPs with small variations with temperature are highly sensitive. For example, dI_C/dt and dV_{CE}/dt have sensitivities of 9 A/μs·°C and -34 mV/μs·°C respectively which require fast sampling. High sampling voltage/current sensors are expensive.

The sensitivity of $V_{GE(th)}$ and $V_{GE(miller)}$ differ by a factor of 10 as $V_{GE(th)}$ varies in 10 mV over the temperature range and $V_{GE(miller)}$ varies in 1 mV. Thus $V_{GE(th)}$ is easier to measure.

$t_{d(on)}$ and $t_{d(off)}$ are commonly short. They are not favourable as their sensitivity is merely in the region of 0.4 ns/°C.

5.2.5 Relative Sensitivity

The TSEPs presented in Table 5.1 are measured in different units - $V_{GE(miller)}$, $V_{GE(th)}$ and $V_{CE(sat)}$ are measured in V; dV_{CE}/dt in V/s; $I_{C(tail)}$, $I_{C(sat)}$ and $I_{C(leak)}$ in A; dI_C/dt in A/s, and $t_{d(on)}$, $t_{d(off)}$ and $t_{VGE(miller\ width)}$ are measured in s. Thus a direct comparison of their sensitivity to temperature changes is challenging. As such the sensitivity of each TSEP must be normalised for comparison. In Table 5.1 the relative sensitivity of the TSEPs is

a normalised parameter for the temperature sensitivity which is determined as shown in equation (5.1) [108]

$$\text{Relative Sensitivity} = \frac{|\text{Sensitivity}|}{|\text{Highest Value}|} \times 100 \qquad (5.1)$$

In equation (5.1), '|Sensitivity|' is the absolute value of the sensitivity and '|Highest Value|' is the absolute value of the highest reading of the TSEP over the given temperature range. In general, the higher the relative sensitivity the lower the bandwidth requirement and in general the easier for hardware implementation.

In Table 5.1, $I_{C(leak)}$ and $I_{C(tail)}$ have the best temperature sensitivity as they both have the highest relative sensitivities of 0.62 %/°C and 0.54 %/°C respectively. $V_{GE(miller)}$ has the least relative sensitivity of 0.01 %/°C which is difficult to measure and is unfavourable from a hardware perspective.

5.2.6 Linearity

Generally a linear TSEP requires less measurement points [108]. Due to their exponential shape depicted in Figure 4.3 and Figure 4.4, $I_{C(sat)}$ and $I_{C(leak)}$ have poor temperature-sensitivity especially at temperatures below 50 °C. Figure 4.3 and Figure 4.4 show that $I_{C(sat)}$ and $I_{C(leak)}$ have better linearity with temperature at temperatures above 50 °C thus these TSEPs are only applicable to limited applications which operate at temperatures above 50 °C [94].

5.2.7 Self-heating

Another TSEP category in Table 5.1 groups the TSEPs into self-heating and non-self-heating. Self-heating occurs in the IGBT switching and on-state phases when the main current, I_C, flows through the device raising T_j away from the known T_j that is set through the heat plate temperature during TSEP characterization. Non-self-heating TSEPs give a better T_j indication as measurements take place before conduction of I_C [48]. All TSEPs in Table 5.1 suffer from self–heating except $I_{C(leak)}$. Marginal self-heating is considered for $I_{C(sat)}$ and $V_{GE(th)}$ as measurements take place shortly after I_C starts conducting.

In addition to causing measurement errors, another disadvantage of self-heated TSEPs is that they require additional sensors which are used to determine if the same operational conditions are met. However, existing converter sensors like phase current sensors or dc-link voltage sensors can be used [48].

5.2.8 Accuracy

Accuracy is the absolute error in the TSEP T_j measurement referenced to the validated T_j measurement [109]. Self-heating is the main cause of TSEP measurement errors as discussed in section 5.2.7 above [50]. In Table 5.1, all the TSEPs that are affected by self-heating have a poor accuracy which is 2% or above. For this reason, as opposed to [23] where high current (I_C) injection of 150 A is utilized to measure $V_{CE(sat)}$ resulting in 5 °C measurement error, [2] uses low current injection of 100 mA in order to minimise self-heating thus reduced measurement errors to 2 °C.

Type of TSEP sensor also contributes to measurement errors as discussed in section 5.2.3 above. Thus although $I_{C(leak)}$ does not suffer from self-heating, its accuracy is also affected because of its low temperature sensitivity of -14 mA/°C. In addition detecting the typically low levels (few milli-amps) of $I_{C(leak)}$ values can be challenging. However, it is possible to improve accuracy by using high performance sensors/components and achieve accuracy better than those depicted in Table 5.1.

In Table 5.1, time-based TSEPS have require high sensitivity and have poor accuracy. The sensitivities of $t_{d(on)}$ and $t_{d(off)}$ are very small to detect in ns. Furthermore these TSEPs require accurate triggering when the IGBT is commanded to turn-on or off for the timing to start and when the IGBT actually switches on or off for the timing counter to stop which results in them suffering measurement errors. $t_{VGE(miller\ width)}$ also requires accurate trigger for the timer to start when the Miller plateau starts and to stop at the end of the plateau, the sensitivity is also in the ns and difficulty to detect. $V_{GE(miller)}$ is among the TSEPs which have poor accuracy. The Miller plateau level where $V_{GE(miller)}$ is measured is characterized with oscillations and hence the behaviour of V_{GE} at a single instant is not consistent at different temperatures, many samples are required to average them and determine $V_{GE(miller)}$ and accuracy cannot be guaranteed. Other TSEPs with low accuracy include dV_{CE}/dt and dI_C/dt which require two sensors (one for measuring

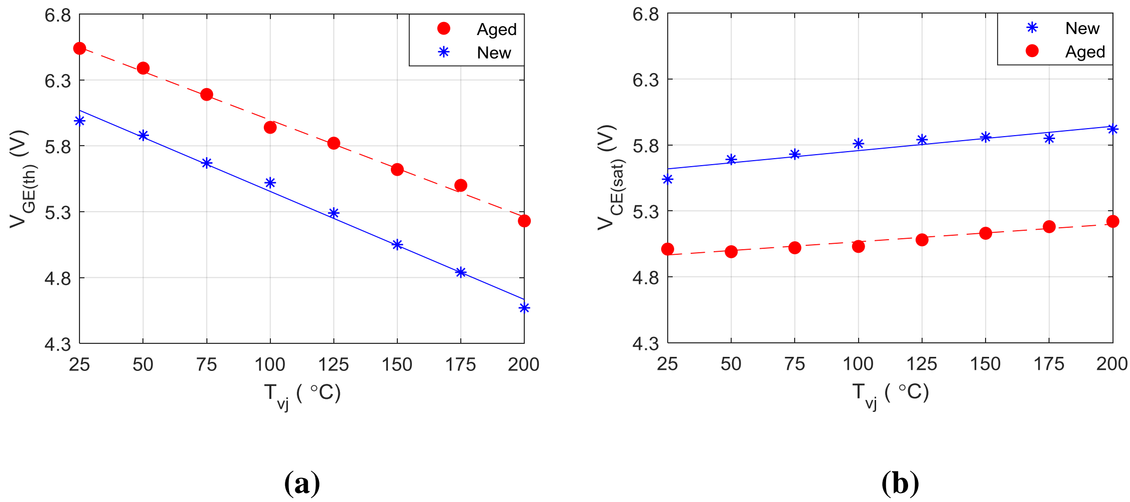
the time and another for trigerring the measurement). Such TSEPs which require more than one sensor are prone to computational errors thus measurement errors .

EMI is also a common cause of inaccuracies. For example in converter configurations with more than one IGBT power module in use (for instance three phase inverter) EMI noise caused by the other IGBT switches may have an impact on the accuracy of some TSEPs especially dynamic TSEPs.

5.2.9 Repeatability and Drift

It is vital for a TSEP to provide consistent and reliable/accurate measurements. Repeatability is a good indication of TSEP accuracy. TSEPs affected by self-heating as well as those with low sensitivity have low repeatability. TSEPs such as $I_{C(tail)}$ and $V_{GE(miller)}$ are also deemed as having low repeatability in Table 5.1. This is mainly because they fall in the IGBT switching phase where the I_C and V_{GE} waveforms have oscillations/ripples. Thus it is difficult to determine a single measurement point to measure from as the measurement point transverses due to oscillations. For this reason, these TSEPs are measured by collecting a few samples and then averaging. This presents a further problem that several samples are required hence large data memory is required.

Drift also accounts for some TSEPs failing in the repeatability category. TSEP drift is caused by variation of circuit parameters such as V_{GG}, $V_{dc\text{-}link}$ and load/I_C conditions. The ageing of IGBTs [76] and internal IGBT failures can also cause TSEP drifting with IGBT lifetime. Reference [76] reveals that $V_{GE(th)}$ and $V_{CE(sat)}$ are examples of TSEPs that are not immune to device ageing as illustrated in Figure 5.2 results from [76].



(a) **(b)**

Figure 5.2: (a) $V_{GE(th)}$ and (b) $V_{CE(sat)}$ Performance with IGBT Ageing [76].

In Figure 5.2(a) $V_{GE(th)}$ was measured from a new 600 V 15 A IRG4BC30KD IGBT device from International Rectifier. In general $V_{GE(th)}$ decreases with temperature as expected based on discussion in Chapter 4. The same device was aged using thermal cycling. $V_{GE(th)}$ tests on the aged device show about 10.1% increase in $V_{GE(th)}$ values across all temperatures as portrayed in Figure 5.2(a). A similar analysis in Figure 5.2(b) shows reduced $V_{CE(sat)}$ with device ageing with about 11.4% drift which is worse off compared to $V_{GE(th)}$.

5.3 High-Voltage Multichip IGBT Power Modules

In addition to the TSEP screening properties discussed above, TSEPs applied to multichip IGBT power modules require the following considerations:

Maximum/Minimum/Average Chip Aggregate Temperature: Multichip devices comprise many IGBT chips connected in parallel in a single package. This parameter determines whether the measured T_{vj} value is a maximum, minimum or average value of the parallel-connected IGBT chips.

Tolerance: In multichip power modules tolerance it is a measure of the difference between the TSEP temperature measurement and the actual hottest IGBT chip temperature.

Local/Global Chip Temperature: This parameter tests whether the TSEP provides individual IGBT chip temperatures (local chip temperatures), or global temperature (aggregate of the parallel-connected IGBT chip temperatures in the power module).

Table 5.2 highlights TSEPs that have been investigated on multichip IGBTs. Table 5.2 does not show many TSEPs as TSEPs applied to multichip devices is still a grey area hence the main focus of this research.

Table 5.2: TSEP Screening Properties for Multichip IGBT Power Modules.

TSEP	Max/Min/Ave temperature	Tolerance	Local / Global temperature
$V_{GE(th)}$ [91]	Close to maximum	+/-8 ℃	Local
$t_{VGE(miller\ width)}$ [62]	Average	+/- 7.5 ℃	Global
$V_{CE(sat)}$ [91, 100]	Close to maximum	+/- 3 ℃	Local
dV_{CE}/dt [62]	Maximum	+/- 3 ℃	Global

Isolation: Table 5.1 has grouped the TSEPs into gate-emitter circuit and collector-emitter circuit. In high-voltage applications, typical V_{GE} is 15 V where as V_{CE} is in the kilovolt range. TSEPs such as $V_{CE(sat)}$ and dV_{CE}/dt which are measured from the collector-emitter circuit suffer from EMI, switching noise and require HV isolation. In addition, the TSEP sensor must deal with large voltage swings between the kilovolt blocking voltage and a few volts of $V_{CE(sat)}$ [48]. Consequently additional hardware is required to isolate and protect the sensor from HV as described in [110], this increases hardware complexity and costs [48].

Sampling Rate: HV applications have typical operating frequency in the region of 500 – 1000 Hz [9]. For this reason static TSEPs have enough time (up to 1ms) for the measurement to take place. On the other hand dynamic TSEPs still require fast sampling above 1 MHz. In [105] a large $R_{G(ext)}$ is inserted to reduce the device switching speed during measurements. This method leads to increased switching losses and risks damaging the device especially in high-voltage applications. Secondly it requires the device to be isolated/switched-over from the normal $R_{G(ext)}$ of the application. This may interfere with the normal operation of the application, and may not be suitable in critical online applications.

5.4 Summary

This chapter has presented a methodology for screening TSEPs based on comparative TSEP properties like temperature-sensitivity and hardware requirements. As a guidance the existing online TSEPs have been compared. The pros and cons of each of the online TSEPs have been highlighted. It is shown that in HV multichip IGBT power module applications, gate voltage-based TSEPs are preferred from a practical perspective. This is because they require no HV isolation and employ voltage sensors which are of lower price compared to current sensors.

In this chapter the in depth study comparing twelve in-situ TSEPs on HV multichip IGBT power modules is unique and have not been presented before. The study has revealed that there is no outstanding TSEP for HV multichip IGBT power modules based on the comparison. Thus new TSEPs are on demand. Chapter 6 proposes five new IGBT TSEPs.

Chapter 6. New Temperature-Sensitive Electrical Parameters

The existing TSEPs which have been published to date are highly valuable and informative as discussed in Chapters 4 and 5. Figure 6.1 shows that since the launch of IGBTs in the 1980-s, there has always been a quest for new TSEPs. Static TSEPs - $V_{CE(sat)}$ and $I_{C(leak)}$, launched in 1985 [56], were among the first TSEPs as they do not need high sampling and were easier to implement at the time compared to dynamic TSEPs. Over the years technology has advanced substantially, becoming easily accessible and cheap. This resulted in the introduction of more dynamic TSEPs like dI_C/dt, dV_{CE}/dt and $V_{GE(miller)}$ from early 2000-s onwards [27, 77, 98]. The recent rapid growth[3] in new online TSEPs from 2009 onwards is due to the increased use of power electronic devices coupled with new legislation pushing for a low carbon future worldwide through campaigns such as greener energy sources and electric vehicles [7].

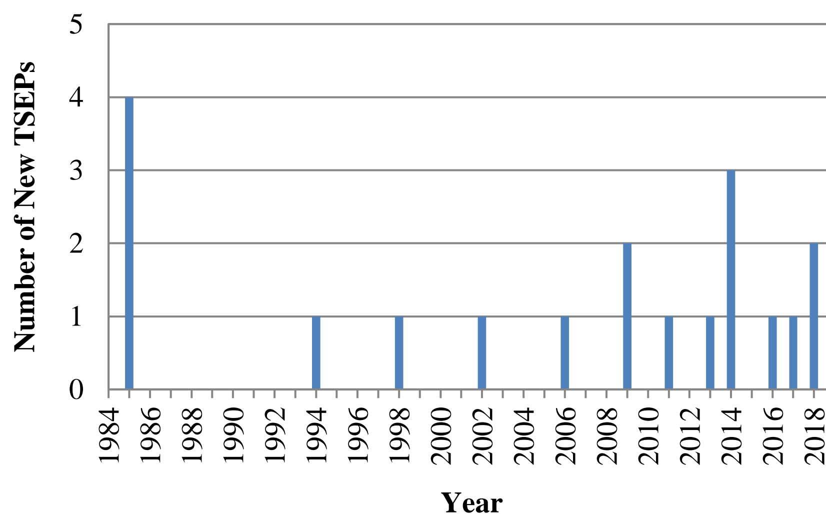


Figure 6.1: Number of New Online TSEPs for Each Year.

As the existing TSEPs are unsuccessful in satisfying all categories of TSEPs attributes as discussed in Chapter 5, today the research gap for new TSEPs is apparent. As a

[3] Figure 6.1 peaks in 2009, 2014 and 2018. Also from 1985 to 2006 rate of new TSEPs is 1 every 3 years where as between 2009 and 2018 it is 1 every year

result, Dynex Semiconductor Ltd have shown interest in this research and donated some IGBT power modules samples utilized in the experiments.

6.1 Investigation of New IGBT TSEPs

The introduction of IGBTs and their semiconductor physics in Chapter 2 shows that the equations (equations (2.2), (2.3), (2.5) and (2.7)) describing the exponential rising of V_{GE} and corresponding falling of I_G as well as V_{CE} at IGBT turn-on have temperature-dependence as depicted below where temperature-dependent parameters are tagged with (T_j).

$$V_{GE}(\mathbf{Tj}) = V_{GG}\left(1 - e^{-\left[\frac{t}{R_G(\mathbf{Tj})C_{ies}}\right]}\right) \tag{6.1}$$

$$I_G(\mathbf{Tj}) = C_{ies}\left(\frac{dV_{GE}}{dt}\right)(\mathbf{Tj}) \tag{6.2}$$

$$\frac{dV_{CE}}{dt}(\mathbf{Tj}) = \frac{1}{R_G(\mathbf{Tj})C_{gc}}\left(\frac{V_{GE(on)} - V_{GE(off)}}{1 + \left(\frac{C_0}{G_M R_G(\mathbf{Tj})C_{gc}}\right)}\right) \tag{6.3}$$

$$t_{VGE(miller\ width)}(\mathbf{Tj}) = R_G(\mathbf{Tj})C_{gc}\left[\frac{V_{CE} - V_{CE(sat)}}{\frac{I_C}{G_M} + V_{GE(th)}(\mathbf{Tj})}\right] \tag{6.4}$$

The temperature dependence of V_{GE}, I_G and V_{CE} revealed above are mainly due to TSEPs $R_{G(int)}$ and $V_{GE(th)}$ which are in the equations. This analysis has not been presented in literature before especially for HV IGBT power modules. Hence experimental tests were conducted to investigate new TSEPs on V_{GE}, I_G and V_{CE} at IGBT turn-on.

6.2 Experimental Set-up

A high-voltage high-current IGBT test rig was set up based on Figure 6.2 pulse test schematic in order to investigate new TSEPs using the DIM800NSM33-F.

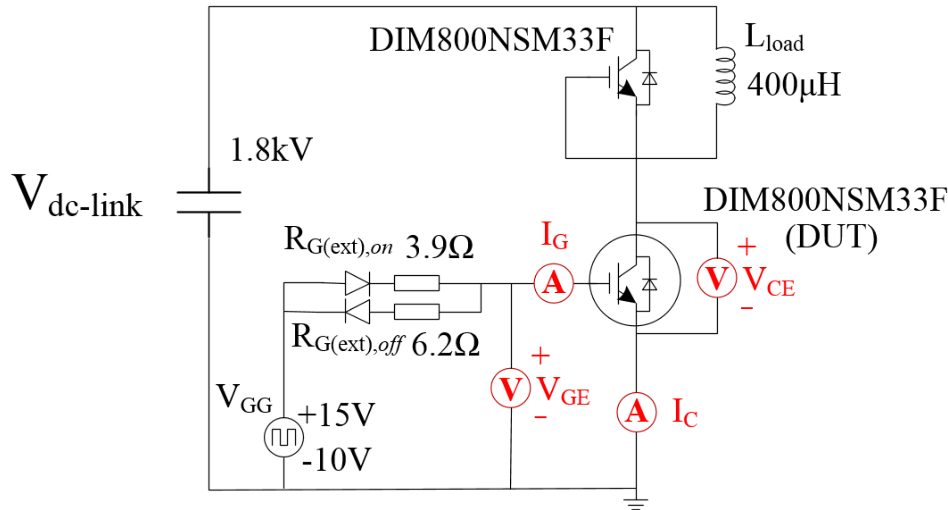


Figure 6.2: IGBT Test Rig Schematic showing Measurement Points for V_{GE}, I_G, V_{CE} and I_C.

As shown in Figure 6.2, the supply voltage was set to 1800V dc. A 400 μH inductive load was used in order to set 800 A dc-link current levels for the IGBT pulse tests. The 400 μH inductive load is the typical size utilized in HV IGBT tests [27] and was in the form of air core inductor coils with a dc resistance of 80 mΩ [111]. The IGBT under test was pulsed from an ideal pulsed voltage supply operating from -10 V to +15 V at a frequency of 1 kHz which is typical in high power applications [9]. The gate driver used is the 2SC0535T2A1-33 from CONCEPT [112]. The external gate resistors used ($R_{G(ext),on}$: 3.9 Ω and $R_{G(ext),off}$: 6.2 Ω) are thick-film surface-mount resistors 1206 with a low resistance tolerance of 1% and temperature coefficient of resistance (TCR) of 100 ppm/K [113]. Film surface-mount resistors are widely used in gate driver circuits and are recommended in the 2SC0535T2A1-33 gate driver application note and manual [17, 112, 114]. Unlike wire wound resistors which are highly inductive and may alter the IGBT switching performance, film surface-mount resistors have high-power proofing to minimize gate-loop inductances [114].

A high-contact liquid temperature controlled heatsink was used to alter the IGBT power module's T_C. The IGBT baseplate temperature was measured with thermocouples. The thermocouples used are Type K stainless steel washer probes with a tolerance of +/-1.5 °C [115]. In order to average out thermocouple errors, six thermocouples were placed around the IGBT module mounting holes on the baseplate. The IGBT electrical waveforms (V_{GE}, I_G, V_{CE} and I_C) were measured by oscilloscope to determine the

TSEPs. The measuring points for the IGBT waveforms are shown in Figure 6.2. The test meters used include 6 kV HV differential probes for V_{CE}, 30 V LV differential probes for V_{GE}, shunt resistor (current viewing resistor (CVR)) for I_C and a miniaturized Rogowski coil for I_G. A photograph of the experimental set-up is shown in Figure 6.3. A complete description of the purpose built IGBT pulse tester is given in Appendix C.

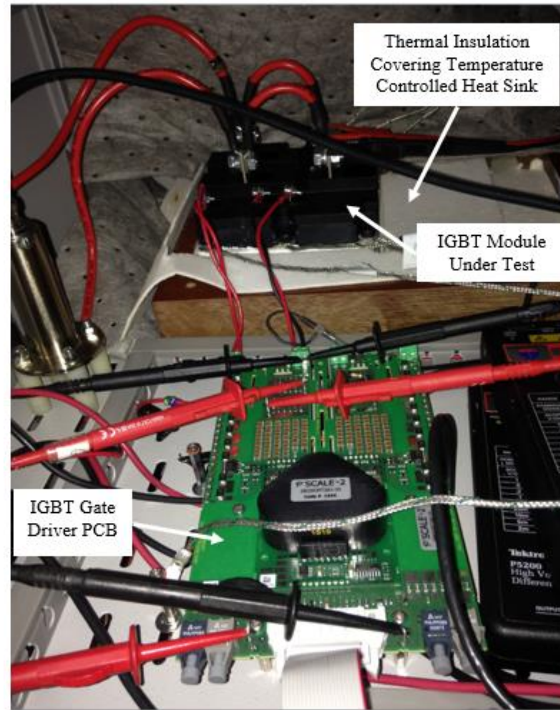


Figure 6.3: Photograph of the Experimental Set-up.

6.3 Practical Results of Five New IGBT Online TSEPs

Practical tests on DIM800NSM33-F IGBT power modules revealed five new TSEPs on the IGBT turn-on transient. The new TSEPs are: gate-emitter pre-threshold voltage ($V_{GE(pre\text{-}th)}$), pre-threshold gate current ($I_{G(pre\text{-}th)}$), gate current Miller plateau width ($t_{IG(miller\ width)}$), gate current Miller plateau level ($I_{G(miller)}$) and collector-emitter voltage tail ($V_{CE(tail)}$). The TSEPs have been classified into two categories: 'TSEPs in IGBT turn-on before IGBT switch-on' in which TSEPs are measured when the IGBT power module is in the turn-on transient but has not switched-on for I_C to flow; and 'TSEPs in IGBT turn-on after IGBT switch-on' for TSPEs measured after the IGBT has switched-on and I_C is conducting. To prevent damaging the IGBT power modules, the TSEP tests were conducted in the temperature range between 20 °C and 80 °C. To show the trend

above 80 °C, the results presented in the next section are extrapolated and indicated as dashed lines for values above 80 °C.

6.3.1 TSEPs in IGBT Turn-on Phase before IGBT Switches-on: $V_{GE(pre-th)}$ and $I_{G(pre-th)}$

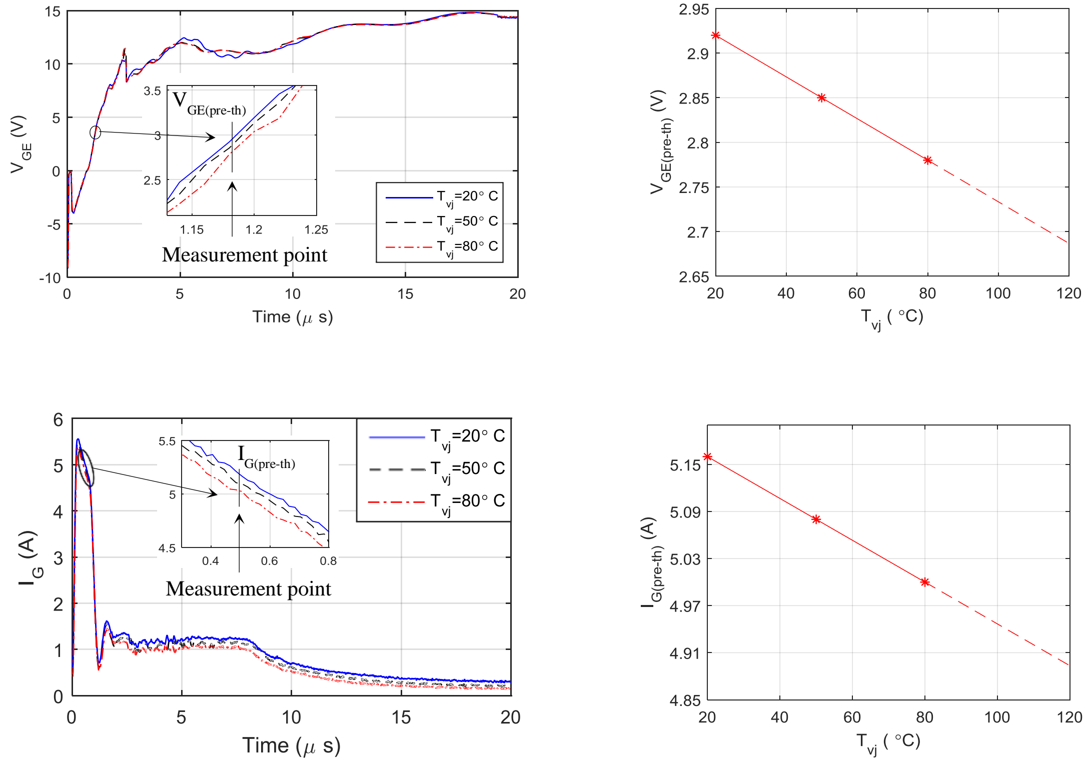


Figure 6.4: Practical Results of New TSEPs in IGBT Turn-on Phase before IGBT Switches-on.

$V_{GE(pre-th)}$ and $I_{G(pre-th)}$ have good temperature-dependencies which are linear throughout the operating temperature range. The sensitivities are -2.2 mV/°C and -2.7 mA/°C for $V_{GE(pre-th)}$ and $I_{G(pre-th)}$ respectively which are practical for hardware implementation. $V_{GE(pre-th)}$ and $I_{G(pre-th)}$ are both measured before the IGBT has switched-on hence do not suffer from self-heating. Once the IGBT has been commanded to turn-on, both V_{GE} and I_G start always from fixed voltage ($-V_{GE}$) and peak gate current level respectively. R_G and C_{ies} which form an RC circuit with V_{GG} account for the exponential rising of V_{GE} and corresponding falling of I_G at IGBT turn-on as described by equations (2.2) and (2.3) in Chapter 2 section 2.3. The relation of $V_{GE(pre-th)}$ and $I_{G(pre-th)}$ with temperature are depicted in (6.5) and (6.6)

$$V_{GE(pre-th)}(t)(\mathbf{Tj}) = (V_{GG(on)} + V_{GG(off)})\left(1 - e^{-\left[\frac{t}{R_G(\mathbf{Tj})C_{ies}}\right]}\right) - V_{GG(off)} \qquad (6.5)$$

$$I_{G(pre-th)}(t)(\mathbf{Tj}) = I_{GG}\left(e^{-\left[\frac{t}{R_G(\mathbf{Tj})C_{ies}}\right]}\right) \qquad (6.6)$$

In (6.5) and (6.6), t is time and I_{GG} is the gate supply current. Figure 6.4 shows V_{GE} starting from a negative value due to the negative turn-off gate voltage (-10 V) utilized. Therefore equation (6.5) includes $V_{GG(off)}$ to account for the negative turn-off gate voltage.

As depicted in (6.5) and (6.6), the gradients of V_{GE} and I_G waveforms change with temperature due to the IGBT internal gate resistance which has a positive linear temperature relation. Consequently, $V_{GE(pre-th)}$ and $I_{G(pre-th)}$ have negative linear temperature-dependencies as depicted in Figure 6.4.

Similar to $V_{GE(pre-th)}$, only one sample is required in measuring $I_{G(pre-th)}$. Both TSEPs are measured at a fixed time delay from the moment V_{GE} begins to rise and I_G begins to fall during IGBT turn-on. Hence both TSEPs allow the use of a simple counter that determines the point of measurement rather than using a current/voltage sensor to determine when to measure. The transient of V_{GE} and I_G in the pre-threshold region last about 1 μs hence fast sampling (in excess of 1 MHz) is required. However the I_G slope is less steep at the beginning and this is where the measurement point is proposed in Figure 6.4 since the required sampling rate for hardware is lower in this region. Besides low hardware requirement, the determination of $V_{GE(pre-th)}$ and $I_{G(pre-th)}$ before the IGBT has switched-on has the advantage that the TSEPs are not influenced by self-heating since at this point the collector current has not started to flow through the device. All existing online TSEPs in Chapter 4 Table 4.1 suffer from self–heating except $I_{C(leak)}$.

6.3.2 TSEPs in IGBT Turn-on Phase after IGBT Switches-on: $t_{IG(miller\ width)}$, $I_{G(miller)}$ and $V_{CE(tail)}$

Figure 6.5 shows $t_{IG(miller\ width)}$, $I_{G(miller)}$ and $V_{CE(tail)}$ which all occur in the Miller period which has been described in Chapter 2 section 2.4. The expression for $t_{IG(miller\ width)}$ is presented in Chapter 2 equation (2.7). $I_{G(miller)}$ is described in (6.7) [61].

$$I_{G(miller)}(\mathbf{Tj}) = \frac{V_{GE(th)}\,(\mathbf{Tj}) + \left(\frac{I_C}{G_m}\right)(\mathbf{Tj})}{R_G(\mathbf{Tj})} \tag{6.7}$$

$V_{CE(tail)}$ is given by [61]:

$$V_{CE(tail)}(t)(\mathbf{Tj}) = V_{CE} - \left[\frac{V_{GG} - \left(V_{GE(th)}\,(\mathbf{Tj}) + \left(\frac{I_C}{G_m}\right)(\mathbf{Tj})\right)}{R_G(\mathbf{Tj})C_{gc}}\right]t \tag{6.8}$$

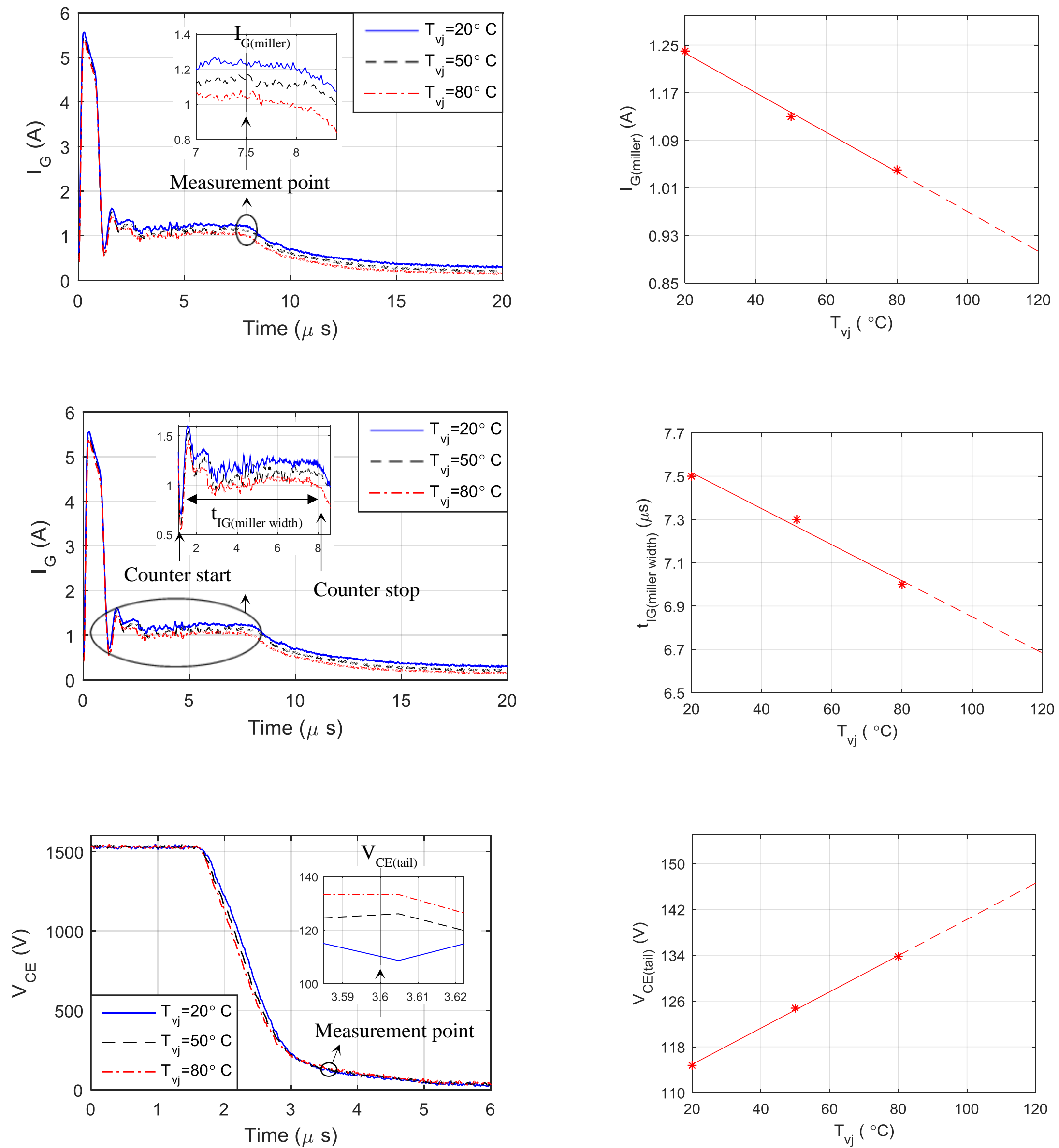


Figure 6.5: Practical Results of New TSEPs in IGBT Turn-on Phase after IGBT Switches-on.

In Figure 6.5, the temperature-dependencies of $I_{G(miller)}$, $t_{IG(miller\ width)}$ and $V_{CE(tail)}$ as described in (2.7), (6.7) and (6.8) are mainly influenced by the TSEPs $R_{G(int)}$ and $V_{GE(th)}$ in the equations. Compared to the TSEPs in Figure 6.4 which are measured before IGBT turn-on hence immune to self-heating scattered and whose measured values are in line with the linear interpolation; the measurements in Figure 6.5 are slightly scattered out of the linear interpolation as the TSEPs are prone to self-heating and switching noise.

$I_{G(miller)}$ and $V_{CE(tail)}$ measurements both follow the same principle described for $V_{GE(pre\text{-}th)}$ and $I_{G(pre\text{-}th)}$ and utilize a voltage sensor and a current sensor respectively.

The duration of the Miller width is about 1 μs hence $t_{IG(miller\ width)}$ requires fast sampling similar to $t_{VGE(miller\ width)}$ in Chapter 4. An alternative method is current sampling measurements by using a Schmitt trigger that sets an upper and lower limit of the I_G Miller plateau. Once I_G hits the upper threshold band a counter starts, and when I_G hits the lower limit band the counter stops resulting in the I_G Miller plateau width time.

6.4 Comparison of New TSEPs

Table 6.1: Comparison of New TSEPs

TSEP	Gate-emitter / Collector-emitter	Static / Dynamic	Voltage/ Current sensor	Sensitivity	Relative Sensitivity	Linearity	Self-heating	Accuracy	Repeat ability
$V_{GE(pre\text{-}th)}$	Gate-emitter	Dynamic	Voltage	-2.2 mV/°C	0.08 %/°C	Yes	No	1 °C	High
$I_{G(pre\text{-}th)}$			Current	-2.7 mA/°C	0.05 %/°C	Yes	No	1 °C	Medium
$t_{IG(miller\ width)}$			Current[4]	-8.3 ns/°C	0.11 %/°C	Yes	Yes	3 °C	Low
$I_{G(miller)}$			Current	-3.3 mA/°C	0.27 %/°C	Yes	Yes	2 °C	Low
$V_{CE(tail)}$	Collector-emitter	Dynamic	Voltage	317 mV/°C	0.24 %/°C	Yes	Yes	3 °C	Medium

Relative sensitivity in Table 6.1 and Table 5.1 is a normalized sensitivity which allows comparison of the new online TSEPs with the existing online TSEPs as they are measured in different units. The relative sensitivity of the new online TSEPs in Table 6.1 compare well with those of the traditional online TSEPs Table 5.1. In Table 6.1

[4] All sensors are used to read a measured TSEP value except [4] which is used to trigger an event

$V_{CE(tail)}$ and $I_{G(miller)}$ have the highest relative sensitivities of 0.27 %/°C and 0.24 %/°C respectively which compare well dI_C/dt and dV_{CE}/dt which have relative sensitivities of 0.25 %/°C and 0.24 %/°C respectively. The remaining TSEPs in Table 6.1 - $V_{GE(pre\text{-}th)}$, $I_{G(pre\text{-}th)}$ and $t_{IG(miller\ width)}$ all have relative sensitivity of about 0.1 %/°C which is similar to that of the traditional TSEPs - $V_{GE(th)}$ and $t_{VGE(miller\ width)}$ which both also have a relative sensitivity of about 0.1 %/°C. Hence with similar relative sensitivities to the well-established traditional TSEPs, the proposed TSEPs are also suitable for practical online implementation and permit accurate temperature measurement just like the traditional TSEPs.

Despite their comparable relative sensitivities, the new TSEPs like $t_{IG(miller\ width)}$, $I_{G(miller)}$ and $V_{CE(tail)}$ are not so much better than the existing 12 online TSEPs in terms of other influential parameters like self-heating which they suffer from, but they offer additional options for online TSEP applications. The main advantage of the proposed new TSEPs is that they are simple to implement, requiring only a single sample after a fixed time delay with the use of a counter and voltage sensor for V_{GE} and V_{CE} or current sensor for those I_G-based. In Table 6.1, $V_{GE(pre\text{-}th)}$ is the only TSEP that achieves the best of all TSEP screening categories. $V_{GE(pre\text{-}th)}$ is not current-based and is not influenced by self-heating. $V_{GE(pre\text{-}th)}$ is especially preferable in HV applications as it does require HV isolation and can be easily integrated on the IGBT gate driver. Consequently $V_{GE(pre\text{-}th)}$ is employed for HV IGBT in-situ health monitoring in the next chapter, Chapter 7.

6.5 Summary

This chapter has highlighted the rising demand in new online TSEPs. In this regard, five new TSEPs on the IGBT turn-on phase have been proposed. The analytical relationship between the TSEPs and T_j have been presented. The temperature sensitivities of the new TSEPs ($V_{GE(pre\text{-}th)}$: -2.2 mV/°C, $I_{G(pre\text{-}th)}$: -2.7 mA/°C, $t_{IG(miller\ width)}$: -8.3 ns/°C, $I_{G(miller)}$: -3.3 mA/°C and $V_{CE(tail)}$: 317 mV/°C) are comparable with traditional TSEPs hence the proposed TSEPs are suitable for online applications. Practical implementation of each of the proposed TSEPs has been described in this chapter. The main advantage of the new TSEPs over most of the traditional TSEPs is that they can be easily implemented and require only a single sample using a counter and voltage sensor for V_{GE} and V_{CE} or current sensor for those I_G-based. Comparison of the new TSEPs shows the superiority

of $V_{GE(pre-th)}$ especially because it is not affected by self-heating and can be easily integrated on the IGBT gate driver.

Chapter 7 recommends $V_{GE(pre-th)}$ for HV IGBT in-situ health monitoring and includes hardware implementation of $V_{GE(pre-th)}$ which measures T_{vj} and detects IGBT chip failures.

Chapter 7. In-situ Health Monitoring Circuit

This Chapter presents a novel in-situ health monitoring circuit that identifies IGBT chip failures in multichip IGBT power modules. Most IGBT TSEPs described in Chapter 5 do not fulfil all categories in screening TSEPs for online application; the TSEPs are unfavourable for implementation as they require convoluted hardware and data processing, which are associated with increased complexity and cost [48]. One of the new TSEPs proposed in Chapter 6, $V_{GE(pre-th)}$, achieves all categories when employed to HV IGBT in-situ health monitoring. It is not current-based hence simple hardware and is preferable especially in HV applications as it does require HV isolation or HV insulation. Since $V_{GE(pre-th)}$ is measured before I_C turn-on, it does not suffer from self-heating or changes in load conditions.

$V_{GE(pre-th)}$ can be used both as TSEP for T_{vj} measurement and as HSP for IGBT chip failure detection in multichip IGBT power modules. This chapter presents hardware implementation of $V_{GE(pre-th)}$ for in-situ health monitoring in HV IGBT power modules. The developed in-situ health monitoring circuit is embedded on the gate driver of the DIM800NSM33-F. Simulation and experimentation results in this chapter show successful implementation of $V_{GE(pre-th)}$, with a linear temperature-sensitivity of -2.2 mV/°C and IGBT chip failure sensitivity of 500 mV/chip failure. The temperature variation of $V_{GE(pre-th)}$ is a about 0.2 V over the typical IGBT operating temperatures such as from 20 °C to 120 °C. As the change of $V_{GE(pre-th)}$ at one chip loss is about 0.5 V that is more than 0.2 V, this means that the temperature variation will not affect the chip failure detection hence $V_{GE(pre-th)}$ can be used as both TSEP and HSP. For this reason, the proposed in-situ health monitoring circuit only utilizes one TSEP, $V_{GE(pre-th)}$, and no other sensor is required since $V_{GE(pre-th)}$ can be used to determine the health status of the IGBT monitored and to determine that the same T_{vj} conditions prevail during health monitoring test. This chapter also includes study of the influence of factors such as changes in temperature, V_{GG} and $R_{G(ext)}$ on $V_{GE(pre-th)}$.

7.1 Simulation

7.1.1 Simulation Set-up

Figure 7.1 shows the schematic circuit of the 16-chip DIM800NSM33-F IGBT power module in the simulator of SaberRD, which is prepared for IGBT pulse tests to investigate the proposed $V_{GE(pre\text{-}th)}$ method for failure detection. In Figure 7.1, 16 IGBT chips constitute a single switch for the DIM800NSM33-F IGBT power module under test which is individually modelled with an integrated electro-thermal model. The electro-thermal model facilitates the investigation of the impact that temperature has on the proposed new HSP, $V_{GE(pre\text{-}th)}$. The thermal pins in the model are the case interfaces for the IGBT chips. In this way, the temperature sources connected to the IGBT chip thermal pins are utilized to vary the individual IGBT chip case temperatures (T_C's). This alters the individual IGBT chip T_j's according to equation (2.12) in Chapter 2. Although the thermal network is simplified by neglecting the thermal coupling and three-dimensional (3D) thermal conduction, the model meets the need to evaluate the $V_{GE(pre\text{-}th)}$ method of emulating the temperature variation across the IGBT chips at different chip temperatures that is typically encountered in real applications.

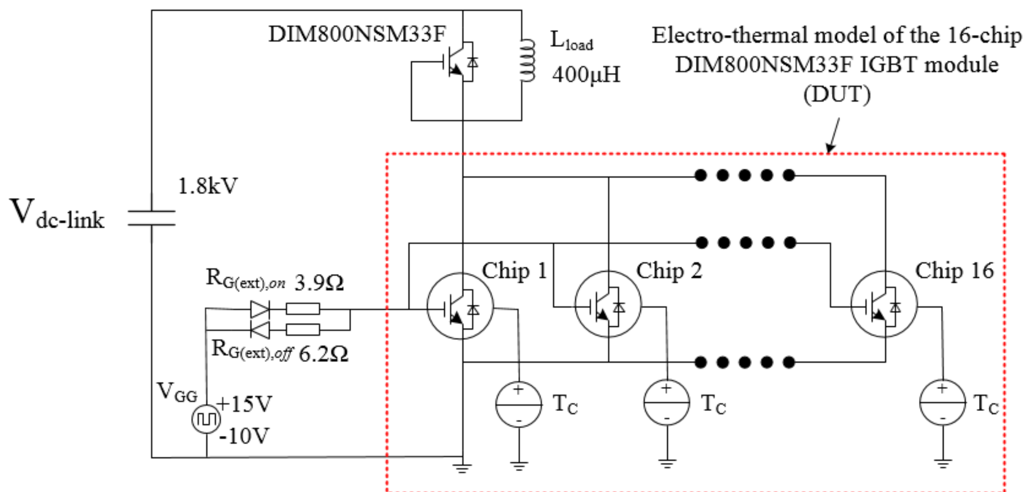


Figure 7.1: Simulation of the 16-chip DIM800NSM33-F IGBT Module in SaberRD.

A close inspection of open IGBT modules from Dynex Semiconductor Ltd which are shown in Appendix C (the 2-chip 3.3 kV, 100 A DIM100PHM33-F, 8-chip 3.3 kV, 400 A DIM400NSM33-F and 16-chip 3.3 kV, 800 A DIM800NSM33-F), and examination

of their datasheets shows that IGBT chips are scaled in order to attain different current ratings in IGBT power modules for a particular chip family. For example, the 2-chip DIM100PHM33-F and 16-chip DIM800NSM33-F datasheets have matching $V_{GE(th)}$, $V_{CE(sat)}$ and gate leakage current (I_{GES}) [57, 116, 117]. The IGBT junction-to-case thermal resistance ($R_{th(jc)}$) per arm, input capacitance and gate charge of the DIM800NSM33-F are a multiple of DIM100PHM33-F with a factor similar to that of their current ratings. On this basis, the IGBT chips in the DIM800NSM33-F simulation model in Figure 7.1 are derived from the DIM100PHM33-F datasheet. Each chip has characteristics such as C_{ies} and $R_{G(int)}$, switching and output characteristics which are taken from the datasheet and input into the chip model in SaberRD.

In Figure 7.1 the dc-link supply voltage was set to 1800 V dc, 800 A dc and a 400 μH inductive load was utilized. The IGBT at the top is off at all times and is employed as an anti-parallel diode. The 16-chip IGBT module under test was pulsed from a voltage supply operating from -10 V to +15 V. External gate resistors of 3.9 Ω for turn-on and 6.2 Ω for turn-off were utilized between the ideal pulsed voltage generator and the gate of the IGBT.

7.1.2 Simulation of IGBT Chip Failures in Multichip IGBT Modules

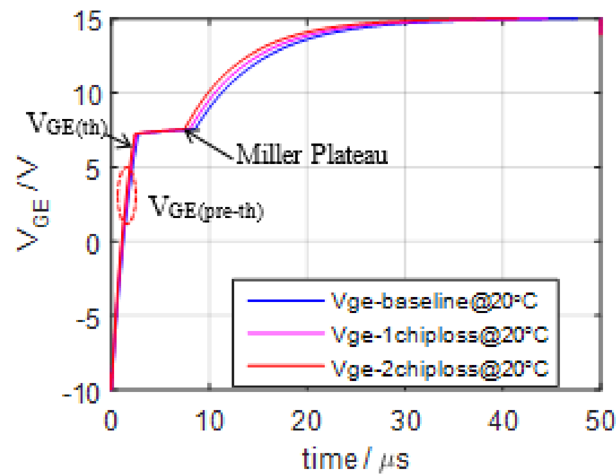
IGBT chip failures and IGBT T_{vj} have been proposed as effective health indicators for HV IGBT power modules. Parallel connection of IGBT chips and bond wires allows IGBT power modules to continue operating with a single IGBT chip failure or bond wire lift-off [2, 40]. Hence rather than having many sensors monitoring every failure site of the IGBT power modules, which is not practical, IGBT chip failure monitoring is proposed. It has been revealed in Chapter 3 that T_{vj} provides a good indication of wear-out damages in the IGBT power module. Hence T_{vj} monitoring is also proposed to detect wear out damages emerging before outright IGBT chip failure.

The DIM800NSM33-F IGBT power module has 16 chips and each chip has 8 bond wires resulting in 128 bond wires in total. Consequently the loss of 8 bond wires connected to one chip will result in an outright chip failure and the loss of 16 bond wires connected to the two chips will result in the loss of two IGBT chips. Therefore in Figure 7.1 IGBT chip failure tests are simulated by disconnecting one and two IGBT chips from the model. T_{vj} changes or wear out damages such as bond wires failures

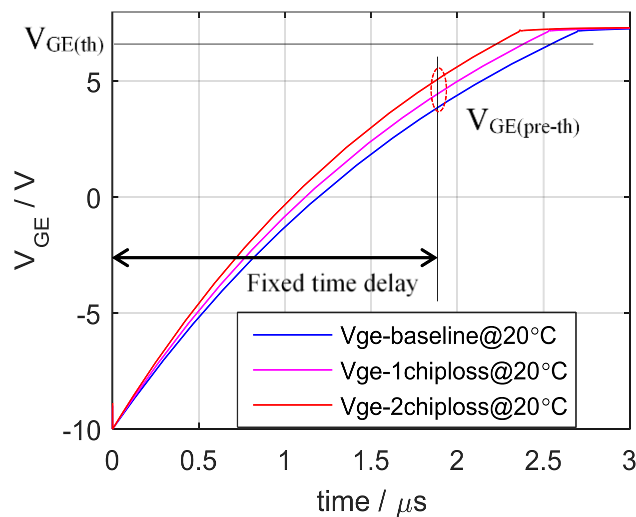
which cause T_{vj} changes before outright IGBT chip failure are emulated and simulated by altering T_j/T_C of the IGBT chips via the temperature sources shown in Figure 7.1.

7.1.3 Simulation Results

The simulation results are shown in Figure 7.2(a) and the point of measurement of $V_{GE(pre\text{-}th)}$ is illustrated in Figure 7.2(b). Figure 7.2(b) shows that two IGBT chip failures of the sixteen-chip DIM800NSM33-F simulated in succession revealed a consistent trend on $V_{GE(pre\text{-}th)}$ in that the voltage level $V_{GE(pre\text{-}th)}$ rises with every IGBT chip loss.



(a)



(b)

Figure 7.2: a) Changes on $V_{GE(pre\text{-}th)}$ with IGBT Chip Failures, b) Use of Fixed Time Delay to Trigger $V_{GE(pre\text{-}th)}$ Measurement.

Chapter 2 equation (2.2) described the exponential rising of V_{GE} at turn-on which is shown in Figure 7.2 baseline results with the IGBT power module healthy. In multichip IGBT power modules, the inherent gate input capacitances on each of the parallel-connected IGBT chips are networked in parallel as portrayed in Figure 7.3. Thus, when all IGBT chips are healthy, an IGBT power module exhibits an overall gate input capacitance, $C_{ies,total}$ ($C_{ies,total} = (C_{ge} + C_{gc}) \times n$) with $C_{ies,total}$ being the total capacitance accounting for each parallel-connected IGBT chip n [47]. DIM800NSM33-F IGBT modules have a typical $C_{ies,total}$ of 144 nF [57]. Consequently, IGBT chip failure in a multichip IGBT power module alters the effective interchip connection resulting in a corresponding decline in $C_{ies,total}$ with every reduction in the number of available/healthy IGBT chips. This in turn changes the $V_{GE(pre\text{-}th)}$ baseline value increasing it as shown in Figure 7.2 according to equation (2.2). Hence $V_{GE(pre\text{-}th)}$ is an effective HSP for chip failure monitoring in multichip IGBT power modules. According to the simulation results, the resolution is about 500 mV per IGBT chip loss.

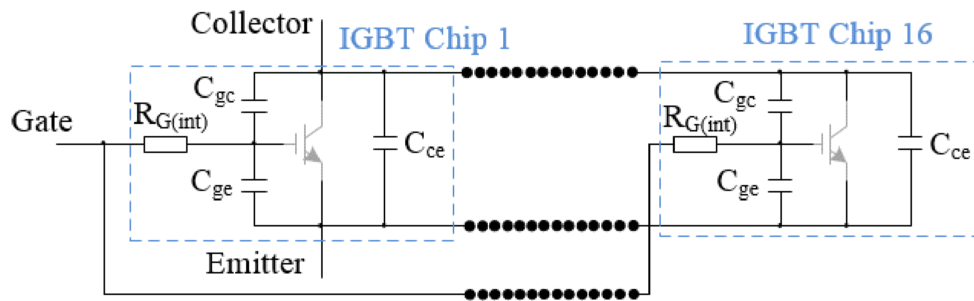


Figure 7.3: Representation of IGBT Capacitances and Internal Resistances in the IGBT Power Module [47].

In general, HSPs are temperature dependent which means temperature variation will lead to change in HSP. Therefore T_{vj} changes were also simulated to verify that the temperature dependency of $V_{GE(pre\text{-}th)}$ will not influence the IGBT chip failure detection. For this investigation, the IGBT chips were set to low chip temperatures of 20 °C and then to higher chip temperatures of 100 °C, before and after the IGBT chip losses in SaberRD simulation. Figure 7.4 shows the simulation results of T_{vj} changes and IGBT chip failures; T_{vj} being the average temperature across all the IGBT chips in the IGBT power module.

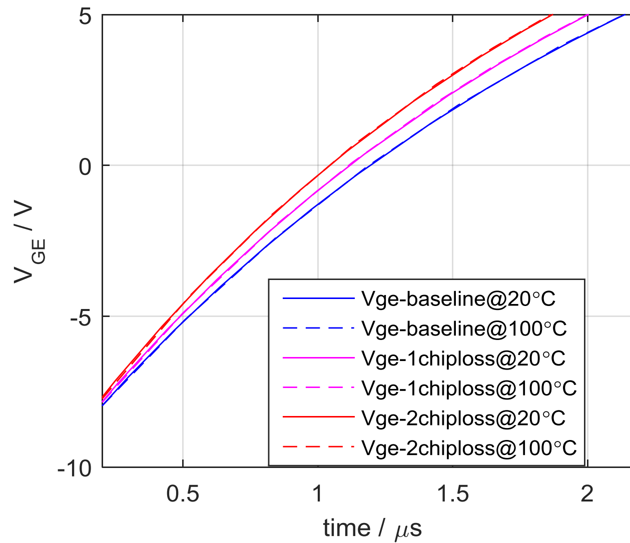


Figure 7.4: $V_{GE(pre\text{-}th)}$ Discrimination of T_{vj} Changes and IGBT Chip Failures.

The results in Figure 7.4 show that for the healthy power module the voltage level of $V_{GE(pre\text{-}th)}$ at T_{vj} = 100 °C is not persistently higher or lower compared to $V_{GE(pre\text{-}th)}$ at T_{vj} = 20 °C over the range of t=0.5 μs and t=2.4 μs. The gate-emitter voltage waveforms are very close. The same observation is made when the power module lost one IGBT chip or two IGBT chips. However, Figure 7.4 shows clearly that once the first IGBT chip has failed, there is a jump in the $V_{GE(pre\text{-}th)}$ level compared to the healthy module. Another jump in $V_{GE(pre\text{-}th)}$ is detected when the second IGBT chip becomes disconnected with the bond wires. The jumps with chip losses are a result of the decline in $C_{ies,total}$ as discussed above.

The behaviour with temperature before the jumps or every subsequent chip loss is a result of changes in $R_{G(int)}$ with temperature which has been as discussed in Chapter 6 where $V_{GE(pre\text{-}th)}$ is introduced as a TSEP. In multichip IGBT power modules, the inherent internal gate resistances on each of the parallel-connected IGBT chips are networked in parallel as shown in Figure 7.3. Thus, when all IGBT chips are healthy, an IGBT power module exhibits an overall $R_{G(int),total}$ ($R_{G(int),total} = R_{G(int)} \div n$) with $R_{G(int),total}$ being the total internal gate resistance accounting for each parallel-connected IGBT chip n. DIM800NSM33-F IGBT modules have a typical $R_{G(int),total}$ of 135 $\mu\Omega$ [57]. Consequently, IGBT chip failure in a multichip IGBT power module alters the effective interchip connection resulting in a corresponding rise in $R_{G(int),total}$ with every reduction

in the number of available/healthy IGBT chips. This in turn causes the $V_{GE(pre-th)}$ baseline, 1 chip loss and 2 chip loss values to decrease at a rate of about -2.2 mV/°C according to equation (2.2) and as shown in Figure 7.4.

Consequently, it can be concluded that $V_{GE(pre-th)}$ is not significantly affected by T_{vj} changes. This is because the resolution of 500 mV per IGBT chip loss for chip failures is far greater than that of -2.2 mV/°C for T_{vj}.

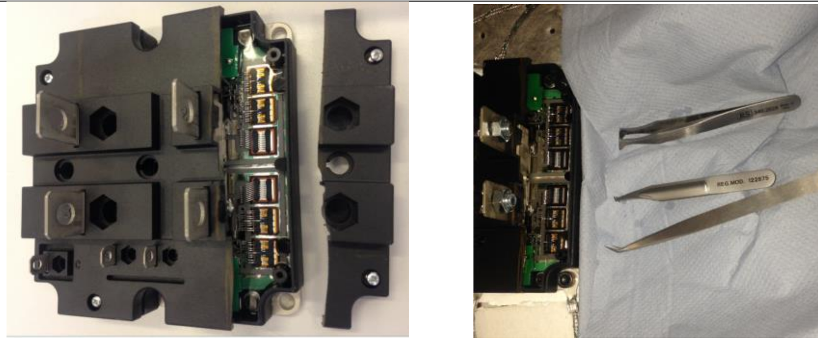
The next section presents experimental results and discusses the influence of temperature, V_{GG} and $R_{G(ext)}$ on $V_{GE(pre-th)}$. This is followed by practical implementation of the $V_{GE(pre-th)}$ IGBT chip loss monitoring circuit on the IGBT gate driver.

7.2 Experimentation

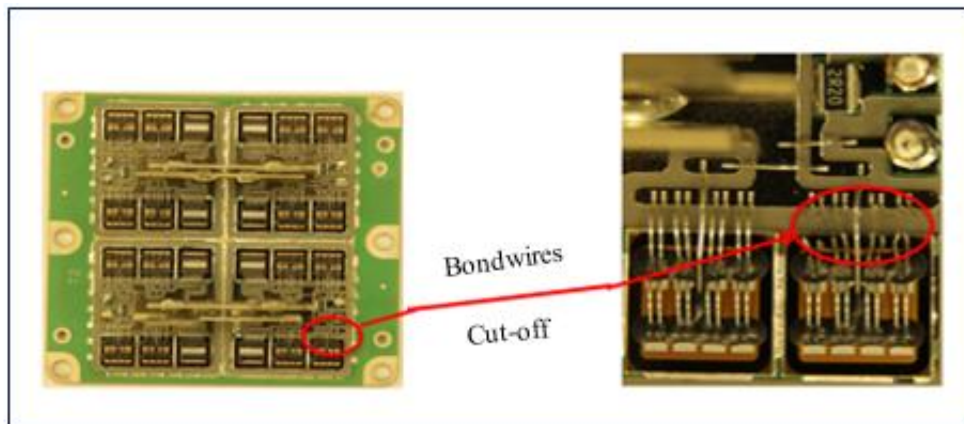
According to equation (6.5), $V_{GE(pre-th)}$ is dependent on T_{vj}, V_{GG} and $R_{G(ext)}$. This section presents experimental results to show the performance of $V_{GE(pre-th)}$ with changes in temperature, V_{GG} and $R_{G(ext)}$.

7.2.1 Experimental Set-up

The IGBT test rig was set up with the dc-link supply voltage set to 1800 V dc, 800 A dc and a 400 μH inductive load utilized as described in Chapter 6. The V_{GE} waveform was measured by oscilloscope to determine the best measurement point for $V_{GE(pre-th)}$. A special order for open IGBT power modules with no resin was acquired from Dynex Semiconductor Ltd. Hence the module cover can be opened to access the IGBT chips as shown in Figure 7.5(a). IGBT chip failures were emulated by cutting off all 8 emitter bond wires of the IGBT chip as shown in Figure 7.5(b). In practise, bond wire failures occur on the emitter bond wires rather than the gate bond wire [2]. The reason is that emitter bond wires are on the IGBT power circuit and experience higher thermal stresses compared to the gate bond wire on the low power control circuit. Therefore Figure 7.5(b) shows the gate bond wire still connected while the emitter bond wires are cut off.



(a)



(b)

Figure 7.5: Cutting off Bond wires to Impose IGBT Chip Failures: (a) Access Hatch, (b) Close-up of cut Bond wires.

T_{vj} changes were imposed by altering the IGBT baseplate temperature through the controlled heatsinks shown in Figure 7.6. A description of the purpose built mechanical rig interfacing the heat plate, chiller and water heater pipework is given in Appendix C.

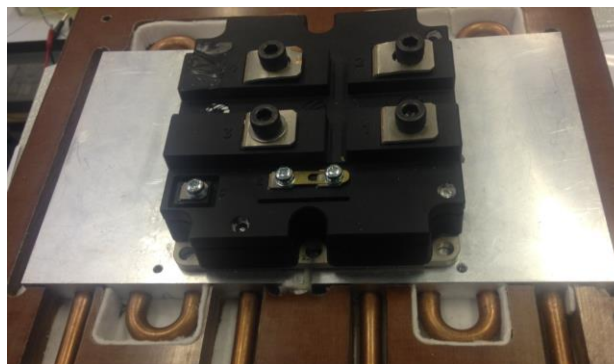


Figure 7.6: IGBT Baseplate across Two Temperature-controlled Heatsinks Mounted on Thermal Insulation Block.

7.2.2 Experimental Results

i. $V_{GE(pre-th)}$ as TSEP

The simulation results above have shown $V_{GE(pre-th)}$ to have a temperature-sensitivity similar to that of -2.2 mV/°C presented in Chapter 6 practical results.

Repeatability

T_{vj} measurement was conducted on two different DIM800NSM33-F IGBT power modules from the same manufacturing batch to show repeatability of $V_{GE(pre-th)}$. Results are portrayed in Figure 7.7 where, for the same fixed time delay (1.2 μs), the recorded errors are: 1.1% at 20 °C, 0.5% at 50 °C and 2.9% at 80 °C. The small errors show that $V_{GE(pre-th)}$ is repeatable. However if high accuracy is required, each IGBT power module must be characterized individually [48].

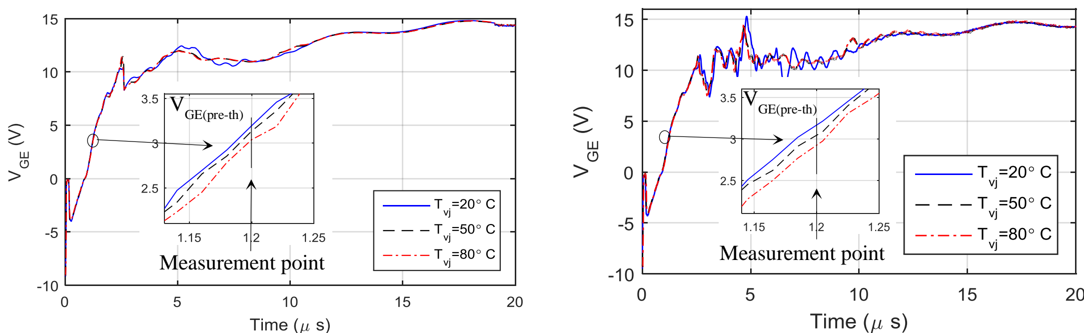
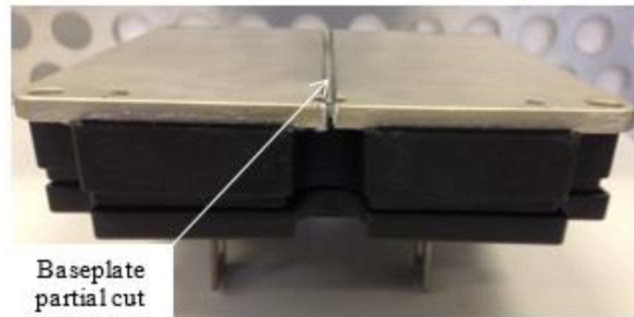


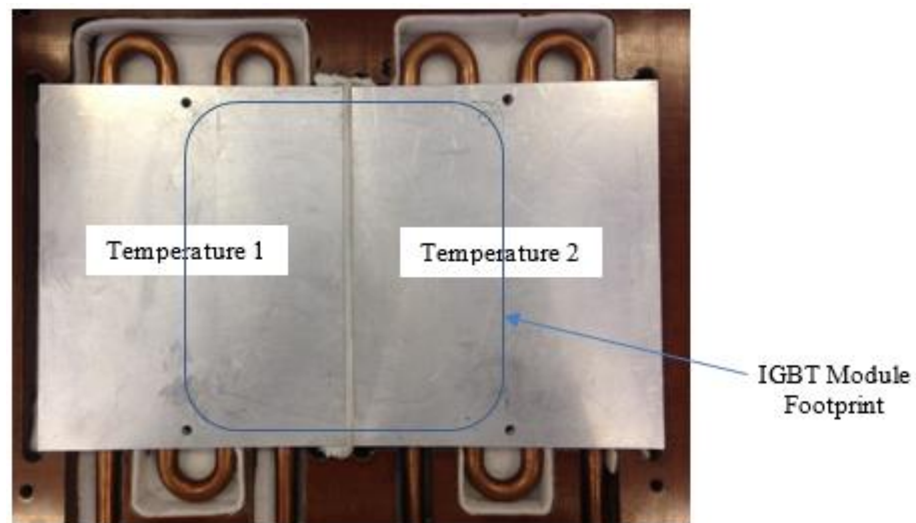
Figure 7.7: Experimental Results of $V_{GE(pre-th)}$ T_{vj} on Two Different DIM800NSM33-F Power Modules [48].

$V_{GE(pre-th)}$ Tracking Maximum IGBT Chip Temperature

Tests have been conducted to determine whether $V_{GE(pre-th)}$ provides maximum, minimum or average aggregate of the IGBT chips within the DIM800NSM33-F IGBT module. The tests were conducted for the worst case scenario with half of the module at a cold temperature (20 °C) and the other half hot temperature (100 °C). The tests were repeated with half of the module at a cold temperature (20 °C) and the other half hot temperature (80 °C). To ensure accurate characterisation, the set temperatures on each half are maintained by partially cutting the IGBT baseplate as shown in Figure 7.8.



(a)



(b)

Figure 7.8: (a) DIM800NSM33-F Prepared for Half Baseplate Hot Temperature/Half Baseplate Cold Temperature Tests (b) Set-up of Temperature-controlled Heatsinks for IGBT Hot-Cold Tests.

Figure 7.9 shows two cases marked with blue star '*' (100 °C /20 °C and 80 °C/20 °C) where $V_{GE(pre-th)}$ is tracking the higher IGBT chip temperature. Thus it has been concluded that $V_{GE(pre-th)}$ tracks the IGBT semiconductor chips with the highest temperature.

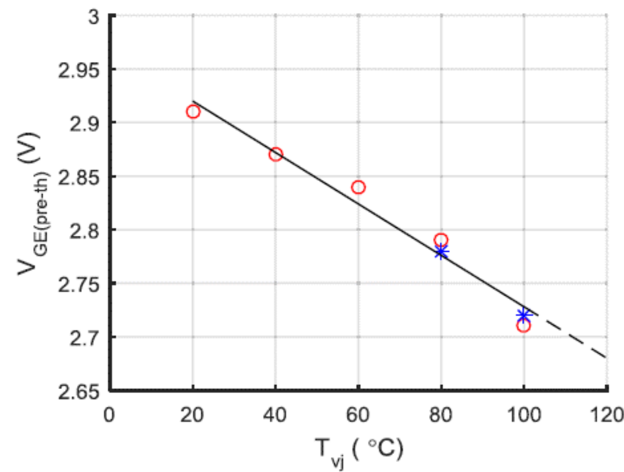


Figure 7.9: Results of $V_{GE(pre\text{-}th)}$ Tracking Higher IGBT Chip Temperatures [48].

ii. $V_{GE(pre\text{-}th)}$ as HSP

It has been highlighted in Chapter 3 that any change in the IGBT failure sites like bond wire lift-off is reflected in IGBT T_j change and IGBT chip temperature rises. Consequently most TSEPs alone cannot easily detect if a measured change in the TSEP is generated by component failure or higher operational temperature. Hence in practice two TSEPs and sensors are required for IGBT health monitoring, one to determine the same T_{vj} conditions prevail during health monitoring test and another to determine the health status of the component monitored. This is not the case with $V_{GE(pre\text{-}th)}$ – the experimental results in Figure 7.10 show that $V_{GE(pre\text{-}th)}$ is immune to T_{vj} changes.

Similar to the simulation results discussed above, the practical results in Figure 7.10 depict that before the initial IGBT chip failure $V_{GE(pre\text{-}th)}$ is able to provide T_{vj} based on all IGBT chips being healthy. Once an IGBT chip has failed, suddenly there is a jump of $V_{GE(pre\text{-}th)}$ to another set of consistent T_{vj} based on the remaining healthy IGBT chips. The worst case changes in temperature (20 °C to 100 °C) produced a total $V_{GE(pre\text{-}th)}$ shift of 220 mV which is below a threshold of 500 mV per IGBT chip failure.

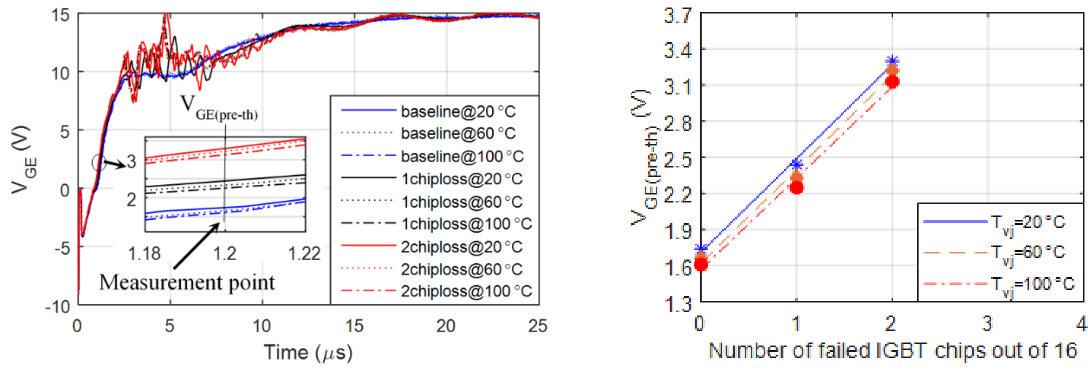


Figure 7.10: Variation of $V_{GE(pre-th)}$ with Initial Two IGBT Chip Failures at Different T_{vj}'s [47].

In Table 1.1 of from Chapter 1, $I_{G(peak)}$ is the only HSP for IGBT chip failure detection which can be compared with $V_{GE(pre-th)}$. Using equation (5.1), the relative sensitivity of $V_{GE(pre-th)}$ is 0.08%/°C for T_{vj} and 28.7%/chip loss for chip failures. This compares well with $I_{G(peak)}$ which has a strong immunity to T_{vj} with a T_{vj} relative sensitivity of 0.05%/°C and the chip failure sensitivity of 36%/chip loss [47]. However, $V_{GE(pre-th)}$ has been applied to multichip IGBT power modules (16-chip) whereas $I_{G(peak)}$ was only applied to 2-chip IGBTs. The main advantage of $V_{GE(pre-th)}$ over $I_{G(peak)}$ is that $V_{GE(pre-th)}$ employs a voltage sensor while $I_{G(peak)}$ utilizes a current sensor. In general, voltage sensors are cheaper, simpler and lightweight compared to current sensors hence voltage-based HSPs are preferred from a practical perspective [48].

iii. $V_{GE(pre-th)}$ Immunity to Noise

$V_{GE(pre-th)}$ has a good noise immunity because it is measured to the LV gate-emitter circuit of the gate driver rather than the HV collector-emitter circuit. In addition, $V_{GE(pre-th)}$ is measured before I_C begins to flow and V_{CE} begins to switch hence it is not affected by the noise from the V_{CE} and I_C switching transients or changes in load size. Figure 7.11 results show noise developing on V_{GE} when the device begins to turn-on. The waveforms are at different IGBT chip failures and show a consistent relation before I_C begins to flow and V_{CE} begins to turn-off. The trend between the waveforms is then distorted from the onset of I_C flow and V_{CE} switching transient. Hence it is clear that $V_{GE(pre-th)}$ measurements are immune to switching noise as they are collected before the falling of V_{CE} and rising of I_C. This is particularly essential for high-voltage applications where switching noises are common and pronounced.

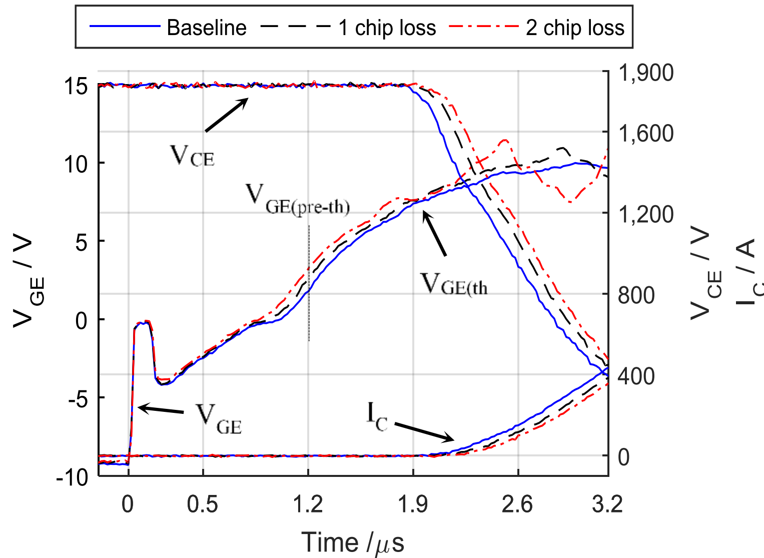


Figure 7.11: Clearance of $V_{GE(pre\text{-}th)}$ from I_C and V_{CE} Switching Noise at Different IGBT Health States at T_{vj}=20 °C [47].

iv. Impact of V_{GG} Changes on $V_{GE(pre\text{-}th)}$

The impact of the changes in V_{GG} on $V_{GE(pre\text{-}th)}$ is investigated due to their relation in equation (6.5). The 2SC0535T2A1-33 gate driver used has voltage regulation on $V_{GG(on)}$ but not $V_{GG(off)}$ [114]. Moreover, the 2SC0535T2A1-33 gate driver has a 2% temperature compensation [112]. Therefore to cater for component tolerances and the temperature dependency of the gate driver components, tests were conducted to investigate the impact of 2% on $V_{GG(off)}$. The $V_{GG(off)}$ used is -10 V hence was varied from -10 V to -9.8 V (2% error). Figure 7.12 shows repeatability of $V_{GE(pre\text{-}th)}$ in the context that the correct information about the loss of IGBT chips is still achieved despite the changes in $V_{GG(off)}$. Figure 7.12 results also depict that there is enough margin in $V_{GE(pre\text{-}th)}$ to allow the IGBT chip loss detection. Hence the resulting $V_{GE(pre\text{-}th)}$ shift due to 2% on $V_{GG(off)}$ can be ignored. However, for gate drivers without voltage regulation where a higher error may be expected on $V_{GG(off)}$, a voltage sensor may be added to determine if the same $V_{GG(off)}$ conditions for the IGBT health monitoring tests are met [47].

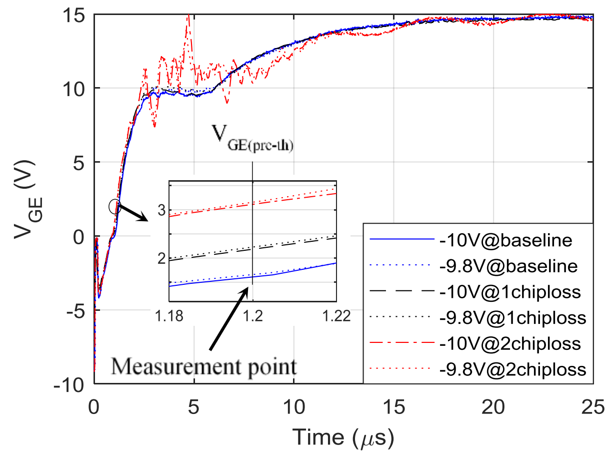
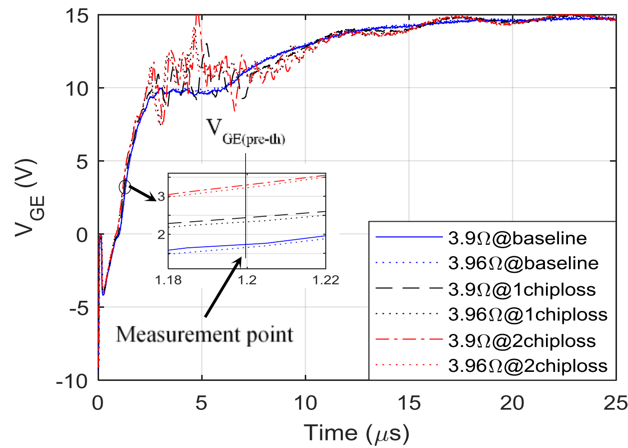


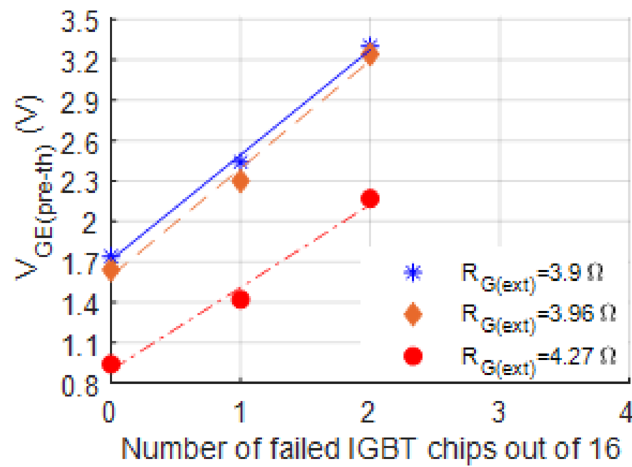
Figure 7.12: V_{GE} as a Function of Change in V_{GG} at T_{vj}=20 °C [47].

v. Impact of Changes on $R_{G(ext)}$

An investigation was conducted to test the impact of temperature changes in the application environment. $R_{G(ext)}$ is one of the external circuitry components that is temperature-sensitive and is on the gate-emitter circuit through which $V_{GE(pre-th)}$ is measured. Thus the impact of temperature change in $R_{G(ext)}$ has been examined. The resistor employed for $R_{G(ext)}$ has a TCR of 100 ppm/K thus the overall resistance changes to 3.93 Ω [113]. To examine this effect, the nearest resistor size of 3.96 Ω was utilized [47]. The results in Figure 7.13 show a 4.5% maximum error in the 3.9 Ω and 3.96 Ω $R_{G(ext)}$ conditions hence the change on $V_{GE(pre-th)}$ is small and can be neglected. However, if $R_{G(ext)}$ is physically changed by more than 1%, this will lead to different results as depicted in Figure 7.13(b) results for $R_{G(ext)}$=4.27 Ω. However the fundamental $V_{GE(pre-th)}$ principle remains hence $V_{GE(pre-th)}$ will require a re-calibration [47].



(a)



(b)

Figure 7.13: V_{GE} as a Function of Change in $R_{G(ext)}$ caused by Temperature [47].

7.3 $V_{GE(pre-th)}$ Measurement Circuit

Measurement of $V_{GE(pre-th)}$ requires only one sample to be taken at a fixed time instant during the V_{GE} turn-on process. Alternatively a fixed $V_{GE(pre-th)}$ magnitude can be chosen and the time taken to reach that $V_{GE(pre-th)}$ is monitored for different IGBT health conditions. The earlier method of fixing the time and measuring $V_{GE(pre-th)}$ is employed in this thesis. IGBT gate turn-on waveforms are in the order of hundreds of nano seconds thus precise measurement triggering and high bandwidth are required.

The proposed $V_{GE(pre-th)}$ measurement circuit can sample $V_{GE(pre-th)}$ in normal IGBT switching operation. Figure 7.14 schematic shows hardware implementation of the

$V_{GE(pre-th)}$ circuit that was embedded on the 2SC0535T2A1-33 gate driver of the DIM800NSM33-F IGBT power module.

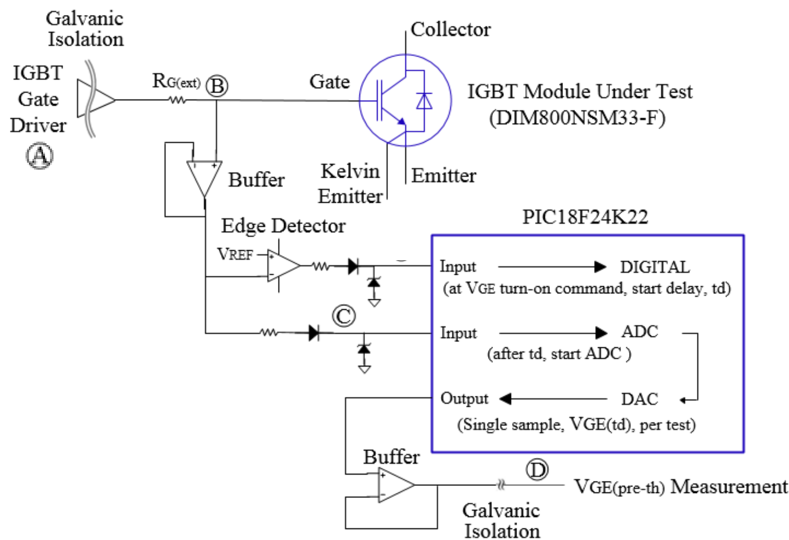


Figure 7.14: Schematic of $V_{GE(pre-th)}$ Measurement Circuit Interfaced on the IGBT Gate Driver for IGBT T_{vj} and IGBT Chip Failure Monitoring [47].

Figure 7.14 shows the measurements points labelled A, B, C and D for $V_{GD(cs)}$ (gate driver voltage control signal), V_{GE}, $V_{GE(pic)}$ (V_{GE} analogue input to a programmable interrupt controller (PIC) for $V_{GE(pre-th)}$ measurement) and $V_{GE(pre-th)}$ signals respectively. Figure 7.14 also includes galvanic isolation of the gate driver input as well as the $V_{GE(pre-th)}$ output. These isolation barriers are necessary to protect users as well as associated low-voltage components and equipment from the high-voltage environment on the IGBT power module's collector-emitter circuit. $V_{GE(pre-th)}$ is more pronounced on the V_{GE} region between the zero-crossing and 5 V which are within the voltage rating of the PIC pins. Thus a diode and Zener diode combination has been utilized to allow only V_{GE} portion between zero and 5 V to progress through to the PIC. This protects the PIC from over voltage and negative voltage [47].

In Figure 7.14, a programmable interrupt controller (PIC) PIC18F24K22 is utilized for measuring and processing $V_{GE(pre-th)}$. PIC18F24K22 has high clock speed of 64 MHz [118] hence enough bandwidth to capture $V_{GE(pre-th)}$ in the normal V_{GE} transient of 1 MHz. Figure 7.14 also shows a buffer as the first stage in collecting $V_{GE(pre-th)}$. The buffer prevents the $V_{GE(pre-th)}$ measurement circuit from loading the gate driver. In this

way, gate's normal operation is not affected thus the proposed $V_{GE(pre-th)}$ monitoring interface is suitable for online applications.

An edge detector is also shown in Figure 7.14. The gate driver uses -10 V to drive the IGBT off. Following IGBT turn-on command, V_{GE} starts rises from -10 V and the edge detector senses the initial V_{GE} rising edge. When V_{GE} reaches -8 V, the edge detector sets off a delay counter in the PIC via a digital input on the PIC. A delay of 1.2 μs has been utilized. After a 1.2 μs delay, an analogue-to-digital converter (ADC) in the PIC measures $V_{GE(pre-th)}$. To allow precise timing in sampling the $V_{GE(pre-th)}$ measurement, the code in the PIC enables the ADC module at the same time instant when the delay counter is started by the edge detector [47]. In this way the ADC is ready to execute timely measurement of $V_{GE(pre-th)}$ once the 1.2 μs time delay is reached. Figure 7.15 and Figure 7.16 below both show successful $V_{GE(pre-th)}$ measurement of 1.8 V on a healthy DIM800NSM33-F IGBT power module at T_{vj}=20 °C. Each health monitoring test requires only a single $V_{GE(pre-th)}$ sample hence collection of multiple samples of V_{GE} and averaging to determine $V_{GE(pre-th)}$ is not necessary and the rising V_{GE} does not need to be tracked. If assurance is required the proposed single measurement process can be repeated [47].

7.3.1 $V_{GE(pre-th)}$ Measuring Techniques

Since $V_{GE(pre-th)}$ occurs before IGBT turn-on, $V_{GE(pre-th)}$ can be applied to two modes: Mode 1 is when the IGBT is in its off-state and Mode 2 is when the IGBT turns-on. In both cases the same information about IGBT T_{vj} and loss of IGBT chip can be detected which makes $V_{GE(pre-th)}$ more versatile than any other TSEP or HSP.

i. Mode 1: IGBT Off-state

As the proposed V_{GE} measurement is before the threshold, $V_{GE(th)}$, tests can be conducted without allowing the IGBT to turn-on. This is achieved by driving the IGBT with a duty cycle that allows only enough V_{GE} to produce the required V_{GE} transient at which $V_{GE(pre-th)}$ is measured, then driving the gate drive signal back to the negative off-state gate voltage supply. In this way, the status of V_{CE} and I_C is not affected: V_{CE} remains in the blocking state and no collector current is flowing. Hence this technique can be applied during the off-state period of IGBTs since V_{CE} and I_C are not perturbed.

Figure 7.15 shows pre-mature V_{GE} pulse for testing $V_{GE(pre\text{-}th)}$ when IGBT is off. A $V_{GE(pre\text{-}th)}$ of 1.8 V is measured successfully on a healthy DIM800NSM33-F IGBT power module at T_{vj}=20 °C. An oscilloscope screenshot from this technique is shown in Appendix D. The pulse last only about 2 μs hence the converter controller can only activate the measurement knowing that the off-state is longer than the pulse measurement period [47].

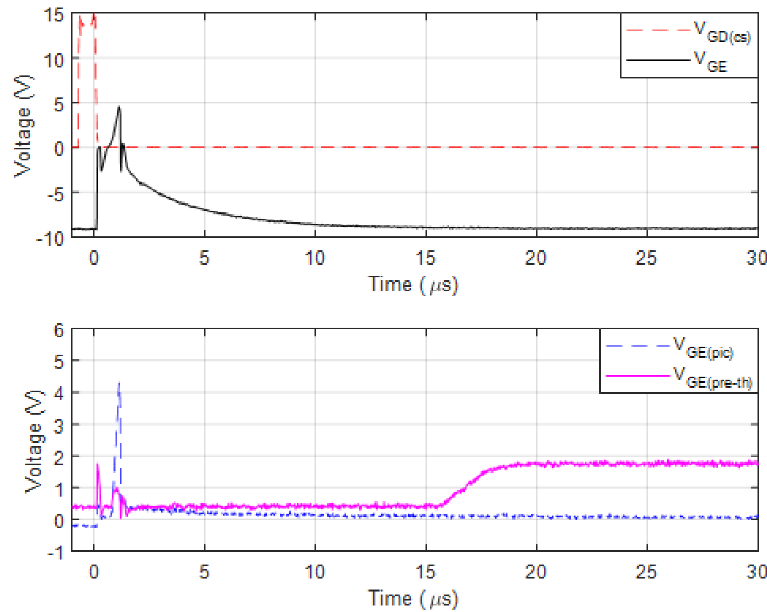


Figure 7.15: $V_{GE(pre\text{-}th)}$ Applied During the IGBT Off-state (Duty Cycle: 0.07%) [47].

ii. Mode 2: IGBT Turn-on State

This is where $V_{GE(pre\text{-}th)}$ measurements are collected online during the normal IGBT switching operation. The IGBT is driven as normal and V_{GE} continues to its full on-state gate voltage of 15 V of the normal duty cycle as depicted in Figure 7.16.

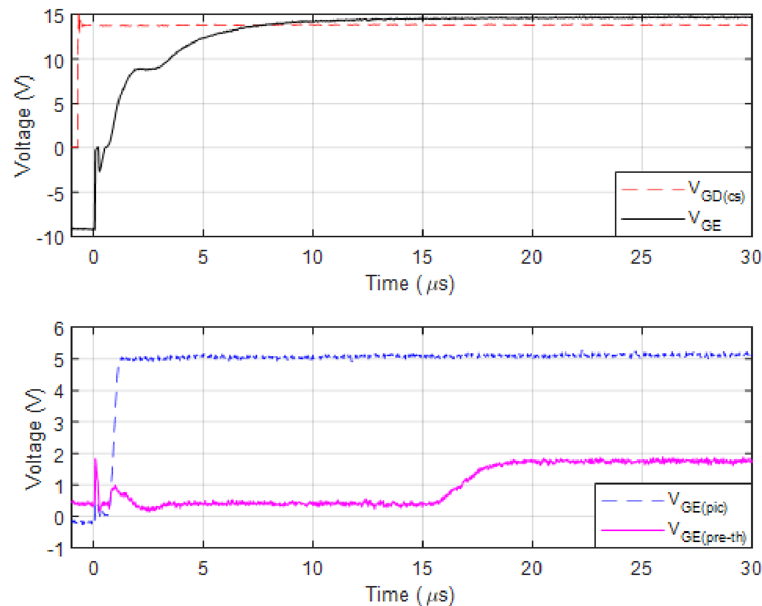


Figure 7.16: $V_{GE(pre\text{-}th)}$ Applied During the IGBT On-state (Duty Cycle: 35%) [47].

Similar to mode 1, Figure 7.16 also shows measurement of $V_{GE(pre\text{-}th)}$=1.8 V for mode 2. In Figure 7.16, $V_{GE(pre\text{-}th)}$ is successfully measured online in a typical PWM of 1 kHz for a healthy IGBT power module at T_{vj}=20 °C. An oscilloscope screenshot from this technique is shown in Appendix D. It can be seen in Figure 7.16 that the measured $V_{GE(pre\text{-}th)}$ is available approximateley10 μs later after the measuring event. This is caused by the processing time of the PIC ADC employed. A faster ADC may be utilized but this is not necessary because in health monitoring, wear out failures are gradual and slow compared to switching frequencies thus time can be afforded for processing and transferring data to a host computer or other means of display and processing such as the use of a liquid crystal display (LCD) as shown in Figure 7.17. The developed C programme codes for $V_{GE(pre\text{-}th)}$ measurement with PIC and for the LCD are given in Appendix D.

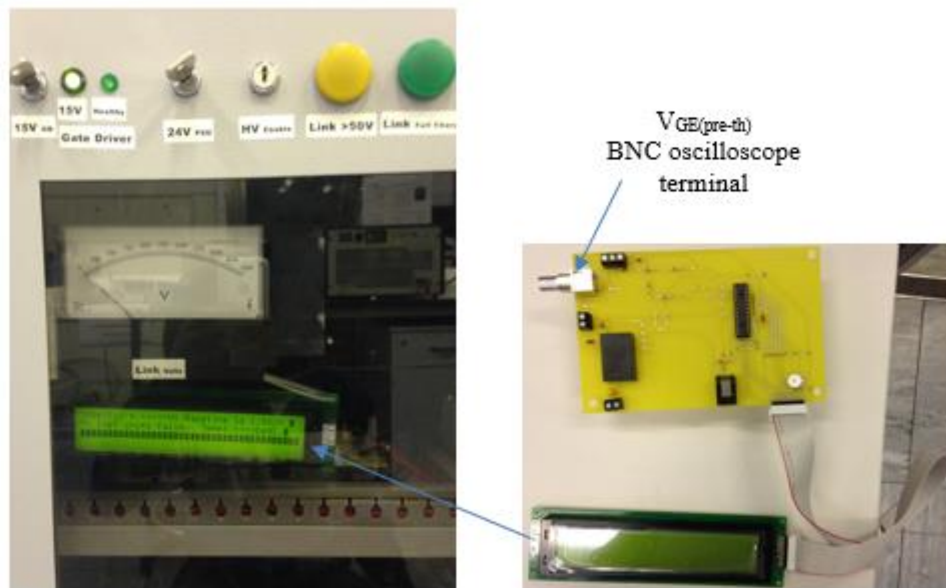


Figure 7.17: LCD on IGBT Test Rig Displays IGBT T_{vj} (°C) and IGBT Chip Loss Count, both Computed from $V_{GE(pre-th)}$.

Figure 7.18 shows photograph of the experimental set-up of the developed in-situ IGBT health monitoring interfaced with the DIM800NSM33-F IGBT power module gate driver.

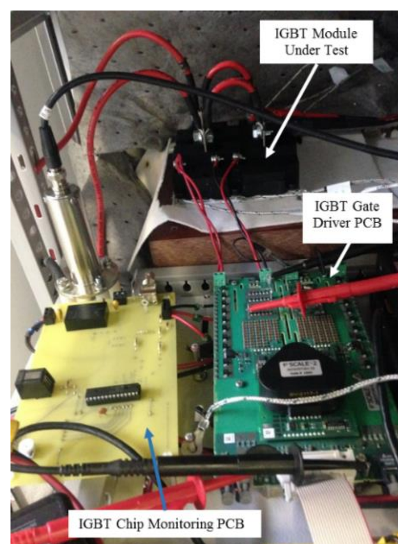


Figure 7.18: $V_{GE(pre-th)}$ Practical Implementation and Testing.

7.3.2 $V_{GE(pre-th)}$ Circuit Results

i. IGBT Chip Failure Detection

A look-up table (LUT) was derived from the characterization of $V_{GE(pre-th)}$ in Figure 7.10. The LUT holds the following information: $V_{GE(pre-th)} < 2.0$ V - power module is healthy (baseline); 2.0 V < $V_{GE(pre-th)} < 2.8$ V - one IGBT chip has failed; $V_{GE(pre-th)} > 2.8$ V - two IGBT chips have failed. The results in Table 7.1 show successful implementation and repeatability with the $V_{GE(pre-th)}$ measured on DIM800NSM33-F IGBT power modules from the same manufacturing batch as the IGBT power modules for the LUT characterization. This is because regardless of temperature changes, the correct information about the IGBT chip failure count is obtained according to the LUT [47].

Table 7.1: IGBT Chip Failure Detection with $V_{GE(pre-th)}$ Circuit [47].

Lookup table (V)		$V_{GE(pre-th)}$ circuit		
		$V_{GE(pre-th)}$ (V)		Prediction
		20 °C	100 °C	IGBT chip failure count
Baseline	$V_{GE(pre-th)} < 2.0$	1.86	1.71	0
1 Chip failure	$2.0 < V_{GE(pre-th)} < 2.8$	2.25	2.12	1
2 Chip failures	$2.8 < V_{GE(pre-th)}$	3.03	2.88	2

ii. IGBT T_{vj} Measurement

T_{vj} was estimated using a LUT based on results from the characterization of $V_{GE(pre-th)}$ and T_{vj} in Figure 7.9. Table 7.2 shows that the monitoring circuit has an error of 3°C. The error is due to the linear interpolation in Figure 7.9, thermocouple error (+/-1.5°C [115]) and the 10-bit ADC used. The errors can be minimized by using thermocouples with a smaller error and an ADC with a higher resolution.

Table 7.2: IGBT Temperature Measurements with $V_{GE(pre-th)}$ [48].

Thermocouple (°C)	$V_{GE(pre-th)}$ Circuit (°C)	Error (°C)
20	23	+3
50	48	-2
80	77	-3

7.4 Summary

A new method for in-situ monitoring IGBT T_{vj} and IGBT chip failures in HV IGBT modules has been proposed. The method employs one novel TSEP, $V_{GE(pre\text{-}th)}$. $V_{GE(pre\text{-}th)}$ is measured at a defined instant between V_{GE} zero-crossing and threshold voltage. Simulation and experimentation have shown that $V_{GE(pre\text{-}th)}$ has a good accuracy and repeatability, and has a linear T_{vj} sensitivity of 2.2 mV/°C and IGBT chip failure sensitivity of 500 mV per chip loss.

A $V_{GE(pre\text{-}th)}$ online chip loss monitoring circuit has been successfully implemented on a commercially available IGBT gate driver. $V_{GE(pre\text{-}th)}$ is based on the LV gate side rather than the HV collector side hence no HV insulation or HV isolation is required. Since $V_{GE(pre\text{-}th)}$ is measured before the start of the conduction of I_C, it does not suffer from self-heating, changes in load conditions or EMI/noise from I_C and HV V_{CE} switching modes. Furthermore, it has been shown that $V_{GE(pre\text{-}th)}$ can be tested during normal IGBT turn-on operation or during the off-state of the IGBT.

The impact of other operational and environmental conditions such as temperature, V_{GG} and $R_{G(ext)}$ changes were investigated. The chip failure signature of $V_{GE(pre\text{-}th)}$ is not affected by T_{vj} changes. However, $V_{GE(pre\text{-}th)}$ performs well with a 1% fluctuation in $R_{G(ext)}$ and 2% fluctuation in V_{GG}. If higher errors in V_{GG} and $R_{G(ext)}$ are expected, additional sensors can be added to determine the V_{GG} and $R_{G(ext)}$ conditions during tests.

Although, $V_{GE(pre\text{-}th)}$ has been successfully tested on standard 3.3 kV, 800 A IGBT power modules, it is applicable to other standard multichip IGBT power modules such as 3.3 kV, 4.5 kV and 6.5 kV IGBT modules.

The next chapter is the thesis conclusion.

Chapter 8. Conclusion

This thesis has identified research gaps in the application of in-situ health monitoring to multichip high-voltage (HV) insulated gate bi-polar transistor (IGBT) power modules. Consequently, a new technique for identifying IGBT chip failures in multichip IGBT power modules has been proposed in this thesis. Multichip IGBT power modules comprise large number of IGBT chips typically 4 to 24 IGBT chips within the power module. The increased complexity of multichip IGBT power module construction, inhomogeneous semiconductor chips and high power operating conditions affect the reliability of multichip HV power modules.

3.3 kV 800 A DIM800NSM33-F IGBT power modules from Dynex Semiconductor Limited (Ltd) were used for simulation and experimentation in this thesis. A DIM800NSM33-F comprises 16 IGBT chips and 8 anti-parallel diode chips. In large power modules, it is common to have IGBT chips as well as anti-parallel diode chips within the power module. This thesis has focussed only on the health monitoring of the IGBT chips and not the diode chips. The main reason is that IGBT chips experience higher thermal stresses compared to diodes hence IGBT chips are more susceptible to failures compared to diode chips.

This thesis has recommended the application of temperature-sensitive electrical parameters (TSEPs) to in-situ IGBT health monitoring. Consequently twelve traditional online/in-situ TSEPs from literature have been investigated and described in this thesis including their pros and cons. The comprehensive work and in depth study across the twelve in-situ TSEPs on HV multichip IGBT power modules have not been presented before hence unique. Furthermore, five new online TSEPs which are comparable to existing/traditional online TSEPs have been proposed in Chapter 6.

The new online TSEPs proposed in thesis are: gate-emitter pre-threshold voltage ($V_{GE(pre\text{-}th)}$), pre-threshold gate current ($I_{G(pre\text{-}th)}$), gate current Miller plateau width ($t_{IG(miller\ width)}$), gate current Miller plateau level ($I_{G(miller)}$) and collector-emitter voltage tail ($V_{CE(tail)}$). The temperature sensitivities of the new TSEPs are - $V_{GE(pre\text{-}th)}$: - 2.2

mV/°C, $I_{G(pre\text{-}th)}$: -2.7 mA/°C, $t_{IG(miller\ width)}$: -8.3 ns/°C, $I_{G(miller)}$: -3.3 mA/°C and $V_{CE(tail)}$: 317 mV/°C which compare well with the traditional TSEPs. This indicates that the proposed TSEPs are suitable for practical implementation from a hardware perspective. The new online TSEPs and the traditional online TSEPs have been screened and $V_{GE(pre\text{-}th)}$ has been employed as a TSEP for virtual junction temperature (T_{vj}) measurement and as a health-sensitive parameter (HSP) for chip failure detection in multichip HV IGBT power modules.

$V_{GE(pre\text{-}th)}$ is measured on the gate-emitter voltage (V_{GE}) at a pre-determined fixed instant between the V_{GE} zero-crossing and threshold voltage, during IGBT turn-on. Since $V_{GE(pre\text{-}th)}$ is measured before the conduction of the IGBT collector current (I_C), it does not suffer from self-heating, changes in load/I_C conditions or noise from I_C and HV V_{CE} switching transients. Furthermore, $V_{GE(pre\text{-}th)}$ does not require high-voltage isolation or HV insulation since it is based on the low-voltage (LV) gate side rather than the HV collector side. One of the primary failure mechanisms of IGBT power modules is bond wire failure. $V_{GE(pre\text{-}th)}$ has a limitation that singular bond wires cannot be detected. The chip failure is detected once all of the bond wires connected to one chip have been lost. However for multichip IGBT power modules the detection of the first few bond wires lift-off is not practical and is not critical or necessary as the module could still operate due to several parallel-connected bond wires employed for the chip connection. For that reason, chip failure is an attractive failure precursor compared to a single bond wire lift-off for IGBT power modules with a very large number of chips.

A $V_{GE(pre\text{-}th)}$ measurement circuit that was developed and integrated on a commercially available gate driver of the DIM800NSM33-F IGBT power modules has been described. Experimental tests have shown that $V_{GE(pre\text{-}th)}$ has a good accuracy and repeatability with a linear temperature-sensitivity of -2.2 mV/°C and IGBT chip failure sensitivity of 500 mV/chip loss. The operation of $V_{GE(pre\text{-}th)}$ has been described in this thesis which shows that it can be used as both TSEP and HSP in multichip HV IGBT power modules. Moreover $V_{GE(pre\text{-}th)}$ can be tested during normal IGBT turn-on operation or during the off-state of the IGBT. In both cases the same information about IGBT T_{vj} and loss of IGBT chip can be detected which makes $V_{GE(pre\text{-}th)}$ more versatile than any other TSEP or HSP. Since the DIM800NSM33-F power modules tested comprise 16 IGBT chips, two cases were considered with half the IGBT chips at high

temperature and the other half at low temperature, revealing that $V_{GE(pre-th)}$ tracks the IGBT semiconductor chips with the highest temperature.

In general, HSPs are temperature dependent which means temperature variation in the IGBT module due to normal operational conditions will lead to change in HSP. For this reason, most HSPs alone cannot easily detect if a measured change in the HSP is generated by component failure or higher operational temperature. Hence in practice two TSEPs and sensors are required for IGBT health monitoring, one to determine the same T_{vj} conditions prevail during health monitoring test and another to determine the health status of the component monitored. As the change of $V_{GE(pre-th)}$ of about 0.5 V at one chip loss is more than 0.2 V for the typical T_{vj} operating range such as from 20 °C to 120 °C or 0.36 V for temperature variation over the DIM800NSM33-F's safe T_{vj} operating range of -40 °C to 125 °C, this means that the temperature variation in the IGBT module will not affect the chip failure detection. Therefore an additional sensor or determination of the T_{vj} conditions for the health monitoring test is not required.

The dependency of $V_{GE(pre-th)}$ on dc-link voltage ($V_{dc-link}$), gate supply voltage (V_{GG}) and external gate resistors ($R_{G(ext)}$) are also discussed in this thesis with theoretical analysis and experimental results presented. The analysis shows that $V_{GE(pre-th)}$ has good immunity to the dc-link voltage. The results for the impact of V_{GG} show that $V_{GE(pre-th)}$ performs well with a stringent 2% maximum fluctuation of V_{GG}. It has been recommended that for gate drivers operating with larger error, a voltage sensor should be added to determine if the same V_{GG} conditions are met when measuring $V_{GE(pre-th)}$. The study of the impact of $R_{G(ext)}$ has concluded that $V_{GE(pre-th)}$ is highly dependent on $R_{G(ext)}$. However, when the same $R_{G(ext)}$ is utilized, the impact of temperature changes on $R_{G(ext)}$ can be ignored. Whereas when $R_{G(ext)}$ is physically changed, different $R_{G(ext)}$ values will lead to different results, but the fundamental $V_{GE(pre-th)}$ principal remains. Therefore it has been recommended that any physical change of $R_{G(ext)}$ of more than 1% require re-calibration of $V_{GE(pre-th)}$.

Although the proposed $V_{GE(pre-th)}$ method was tested on standard 3.3 kV IGBT modules, the structure and failure mechanisms of standard packaged HV IGBT modules are similar. Hence the proposed $V_{GE(pre-th)}$ health monitoring technique is applicable to other HV IGBTs such as 4.5 kV and 6.5 kV IGBT power modules.

8.1 Future work

The proposed method performed well under typical application conditions imposed on the IGBT test rig. However, the IGBT pulse tester used for experimentation is a typical single-phase step-down dc/dc converter or Buck converter which employs only one IGBT power module. Future work is to demonstrate the representativeness and performance of $V_{GE(pre-th)}$ in different operative converter configurations with more than one IGBT power module in use (for instance three phase inverter). This would reveal if the associated electro-magnetic interference (EMI) noise caused by the other IGBT switches would have an impact on the $V_{GE(pre-th)}$ concept.

Future work is also to apply the proposed $V_{GE(pre-th)}$ method to different IGBT types such as press-pack IGBT power modules and determine if measurement of virtual junction (T_{vj}) and detection of IGBT chip losses is also achievable.

Appendices

Appendix A: Datasheet Characteristics of IGBT Modelled in SaberRD, and MAST code of modelled device.

i. Dynex IGBT DIM800NSM33-F Datasheet Parameters Characterized into the IGBT SaberRD Simulation Model

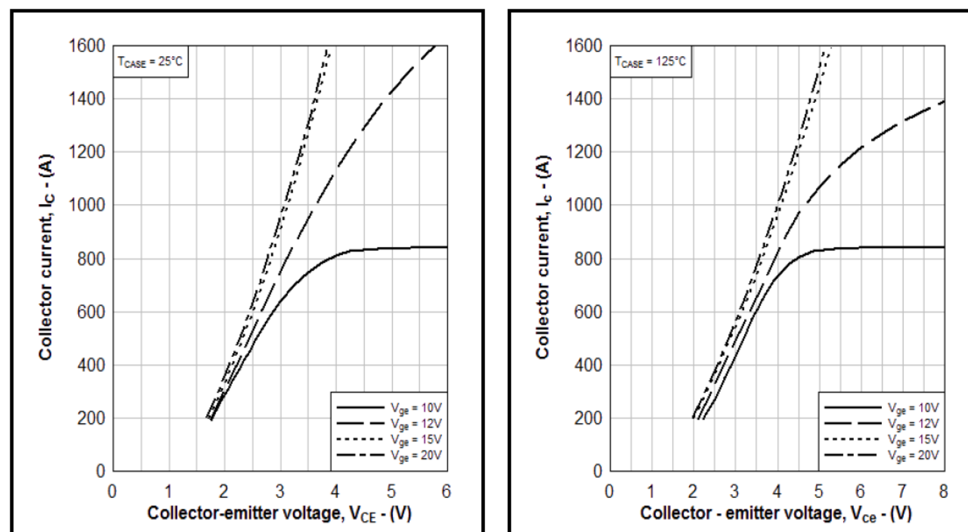


Figure 0.1: IGBT Output Characteristics for 25 °C and 125 °C [57].

ELECTRICAL CHARACTERISTICS

T_{case} = 25°C unless stated otherwise.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CES}	Collector cut-off current	V_{GE} = 0V, V_{CE} = V_{CES}			4	mA
		V_{GE} = 0V, V_{CE} = V_{CES}, T_{case} = 125°C			60	mA
I_{GES}	Gate leakage current	V_{GE} = ± 20V, V_{CE} = 0V			1	μA
$V_{GE(TH)}$	Gate threshold voltage	I_C = 80mA, V_{GE} = V_{CE}	5.5	6.5	7.0	V
$V_{CE(sat)}$ †	Collector-emitter saturation voltage	V_{GE} = 15V, I_C = 800A		2.8		V
		V_{GE} = 15V, I_C = 800A, T_j = 125°C		3.6		V
I_F	Diode forward current	DC		800		A
I_{FM}	Diode maximum forward current	t_p = 1ms		1600		A
V_F †	Diode forward voltage (IGBT arm)	I_F = 800A		2.9		V
		I_F = 800A, T_j = 125°C		3.0		V
C_{ies}	Input capacitance	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		144		nF
Q_g	Gate charge	±15V		20		μC
C_{res}	Reverse transfer capacitance	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		2.2		nF
L_M	Module inductance			15		nH
R_{INT}	Internal resistance			135		μΩ
SC_{Data}	Short circuit current, I_{SC}	T_j = 125°C, V_{CC} = 2500V t_p ≤ 10μs, V_{GE} ≤ 15V $V_{CE\ (max)}$ = V_{CES} – L^* x dI/dt IEC 60747-9		3700		A

Note:

† Measured at the auxiliary terminals

* L is the circuit inductance + L_M

Figure 0.2: IGBT Capacitance, $V_{GE(th)}$, Q_g, L_M and $R_{G(int)}$ [57].

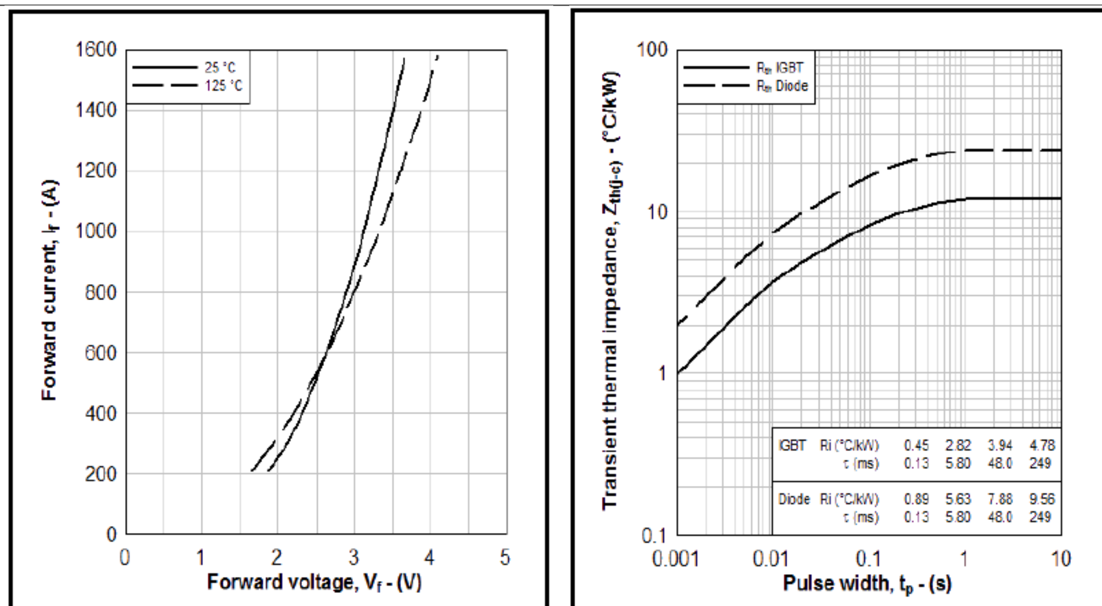
T_{case} = 25°C unless stated otherwise

Symbol	Parameter	Test Conditions		Min	Typ.	Max	Units
$t_{d(off)}$	Turn-off delay time	I_C = 800A V_{GE} = ±15V V_{CE} = 1800V C_{ge} = 220nF L_S ~ 100nH	$R_{G(ON)}$ = 3.9Ω $R_{G(OFF)}$ = 6.2Ω		3.02		μs
t_f	Fall time				270		ns
E_{OFF}	Turn-off energy loss				1050		mJ
$t_{d(on)}$	Turn-on delay time				1300		ns
t_r	Rise time				275		ns
E_{ON}	Turn-on energy loss		$R_{G(ON)}$ = 2.7Ω, $R_{G(OFF)}$ = 6.2Ω		1250		mJ
Q_{rr}	Diode reverse recovery charge	I_F = 800A V_{CE} = 1800V dI_F/dt = 4000A/μs			320		μC
I_{rr}	Diode reverse recovery current				670		A
E_{rec}	Diode reverse recovery energy				300		mJ

T_{case} = 125°C unless stated otherwise

Symbol	Parameter	Test Conditions		Min	Typ.	Max	Units
$t_{d(off)}$	Turn-off delay time	I_C = 800A V_{GE} = ±15V V_{CE} = 1800V C_{ge} = 220nF L_S ~ 100nH	$R_{G(ON)}$ = 3.9Ω $R_{G(OFF)}$ = 6.2Ω		3.1		μs
t_f	Fall time				280		ns
E_{OFF}	Turn-off energy loss				1200		mJ
$t_{d(on)}$	Turn-on delay time				1200		ns
t_r	Rise time				315		ns
E_{ON}	Turn-on energy loss		$R_{G(ON)}$ = 2.7Ω, $R_{G(OFF)}$ = 6.2Ω		1750		mJ
Q_{rr}	Diode reverse recovery charge	I_F = 800A V_{CE} = 1800V dI_F/dt = 4000A/μs			600		μC
I_{rr}	Diode reverse recovery current				800		A
E_{rec}	Diode reverse recovery energy				600		mJ

Figure 0.3: IGBT Switching Times, Energy Losses, Capacitance and FWD Reverse Recovery Characteristics [57].



(a) (b)

Figure 0.4: (a) Diode Forward Characteristics at 25 °C and 125 °C (b) Transient Thermal Impedance [57].

ii. MAST Code of the Dynex 3.3 kV, 800 A IGBT Module (DIM800NSM33-F) Model Created in SaberRD

```
# This template is a dynamic thermal IGBT model produced by the Synopsys
   Model Architect IGBT Tool 1.0.
# It includes an anti-parallel CoPack diode.

element template igbt_model_3300v800a c g e tc = ratings, part_type
electrical c,g,e
thermal_c tc

external number temp, include_stress
string part_type = "IGBT"

# Stress ratings information
igbt1_3x..ratings ratings =
        (tjmax    = 150,
         tjmin    = -40,
         px_jc = undef,
         pdmax_ja = 10400,
         vcemax   = 3300,
         vgemax   = 20,
         icmaxavg = 800,
         icmax    = 1600)
```

```
# Exported model quantities
export val i  ic,ig
export val p  pwrd
export val tc tempj

{
   igbt1_3x..imod
   imod=[(25,7.1362,0.848984,0.129534,455.426u,0.860811,0.811421,0.575246
   ,180.304,540u,38.9n,0.902),(125,6.03745,0.786159,0.220984,455.452u,0.864
   666,0.853428,0.567446,92.6133,540u,60.6n,0.902)]
   igbt1_3x..cap
   cap=(9.1456n,5.08393n,290p,20.4317n,16.2662n,2.0635n,26.7056n,1.28381,
   12.11,1.2735)
   dcopackx..model
   copack=[(25,0.00825468,3.34495f,1.02008,0.0636904,11.0191,39671.2,412.
   299n),(125,0.0154498,9.61533p,0.913811,164.977p,1.90861,27222.1,193.9n)
   ]

   values {
       ic = ic(igbt1_3x.m)
       ig = ig(igbt1_3x.m)
       pwrd  = pwrd(igbt1_3x.m)+pwrd(dcopackx.d)
       tempj = tempj(igbt1_3x.m)
}
l.lc c ci = 20n
l.le e ei = 10n
l.lg g gi = 10n
igbt1_3x.m ci gi ei tj = imod=imod,cap=cap,
part_type=part_type,ratings=ratings
rtherm.r1 tj t1 = rth=11.8548
ctherm.c1 tj 0  = cth=86.8401u
rtherm.r2 t1 t2 = rth=31.7222
ctherm.c2 t1 0 = cth=216.38u
rtherm.r3 t2 tc = rth=51.5805
ctherm.c3 t2 0 = cth=0.00273715
dcopackx.d ei ci tj = model=copack
}
```

Appendix B: Glossary of TSEP Properties Terminology

This appendix defines TSEP properties which are discussed in Chapter 5 "Comparison of TSEPs".

Linearity: The straightness of the TSEP-T_j graph [109]. The more the linearity the less the measurement points required [108]. Also, where the TSEP-T_j graph is exponential, sensitivity increases with temperature hence TSEP may not be precise at low temperatures [108].

Temperature Range: The temperature limits at which TSEP measurement is capable [109].

Sensitivity: The rate of change of TSEP with temperature. Higher sensitivity requires small values and small variations to be detected hence it becomes very difficult to guarantee the TSEP's accuracy, that is, low feasibility due to limited resolution of available sensors and possible need to add subsequent compensating procedures [31].

Accuracy: It is the absolute error in the TSEP-T_j measurement referenced to the validated T_j measurement [109]. In regards to multichip IGBT power modules, TSEP accuracy is a measure of the error in the measured temperature[5] to that of the hottest temperature representing the hottest IGBT chip.

Repeatability: Test conditions/parameters that enable TSEP to produce the same temperature result.

Drift: Changes in test parameters/conditions as well as age that causes TSEP to produce inconsistent results. TSEPs with low drift do not require additional sensors to measure the environmental conditions for the tests.

Immunity: Refers to the effect of noise (from other network or environmental parameters) on TSEP temperature measurement.

[5] In multichip power modules the measured temperature is an aggregate of the different chip temperatures of the IGBT chips in the module

Sampling Rate and Data Memory: TSEPs have different sampling rate and data memory requirements. Dynamic TSEPs require several samples to even out measurement errors hence more data memory required compared to static TSEPs which require one point measurement only.

While static TSEPs do not require high-speed sampling, a large $R_{G(ext)}$ may be utilized to reduce the IGBT switching speed for measuring dynamic TSEPs [104]. However this technique causes higher switching losses which risk destroying the device.

Complexity: It is vital to check that hardware requirements for a chosen TSEP are minimal. Complex TSEP hardware may impair implementation costs as well as reliability of the application.

The number of sensors and hardware required for a particular TSEP is a key measure of complexity. In [21] additional power sources are employed to facilitate $V_{CE(sat)}$ measurement during IGBT off-duty. In another example, [93], [25] and [26] employ an additional sensor for $V_{EE'}$ to trigger $V_{GE(th)}$ measurement. The additional circuitries can be avoided through using different techniques or choosing a different TSEP altogether.

Isolation: Unlike gate-emitter based TSEPs, collector-emitter based TSEPs require isolation especially in high-voltage applications thus adding weight and cost of hardware required.

Self-heating: Self-heating occurs in a device when the main current, I_C, is flowing through the device in the switching and on-state phases. When TSEPs are characterized, the IGBT baseplate temperature is assumed to equal the T_j by maintaining the baseplate at a known temperature long enough before measuring the TSEP. With self-heating, the IGBT case temperature no longer equals T_j hence self-heating causes measurement errors [50].

Appendix C: HV IGBT Test Rig Design and Construction

The research work included the design and construction of a high-voltage (2 kV dc), high-current (2.2 kA dc pulses) IGBT test rig in order to test 3.3 kV, 800 A IGBT modules and validate research findings. The test rig schematic is shown in Figure 0.5.

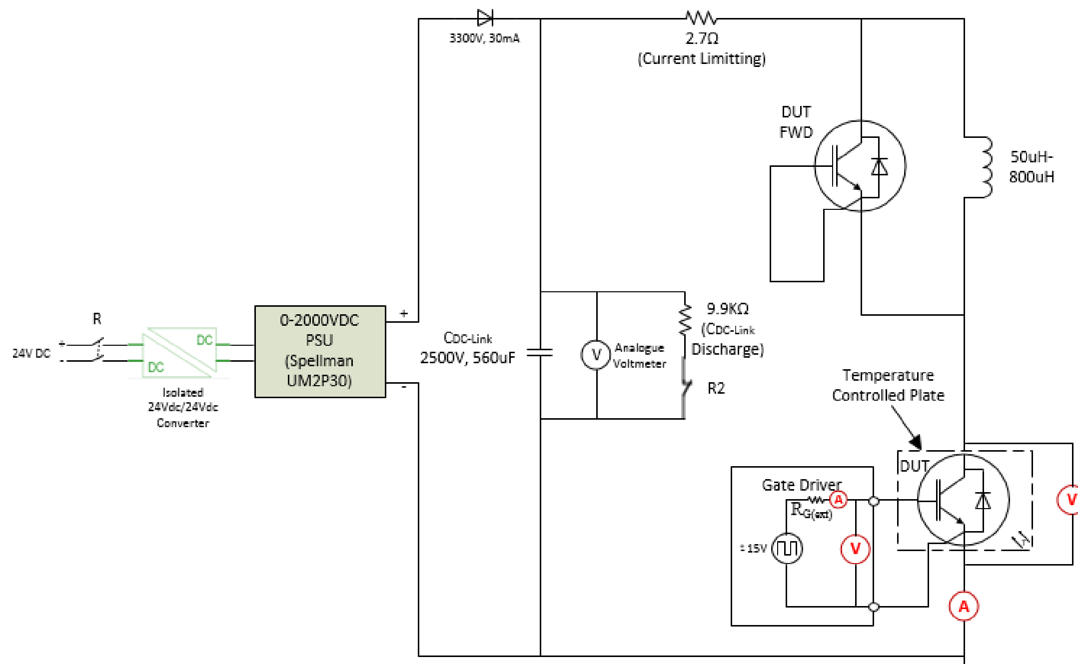


Figure 0.5: IGBT Test Rig Schematic.

The test rig allows altering of power supply (current and voltage), inductive load, duty cycle of the IGBT pulses and IGBT baseplate temperature in order to test the IGBT DUT at different operating conditions. Selection and sizing of the main test rig components are discussed next.

i. HV IGBT Power Modules

3.3 kV IGBT power modules from Dynex Semiconductor ltd have been used in the experiments. To allow comparative studies, dissembled 3.3k V – 100 A, 400 A and 800 A IGBT modules comprising similar IGBT chips were kindly offered by Dynex Semiconductor Ltd who have been interested in the research. Several Dynex 3.3 kV, 800 A closed IGBT module were also acquired as well as some modified modules without resin and with loose covers for access to the interior. The modules without resin

had the busbar left upright to allow easy removal of cover during tests. Some of the IGBT power module samples are shown in Figure 0.6.

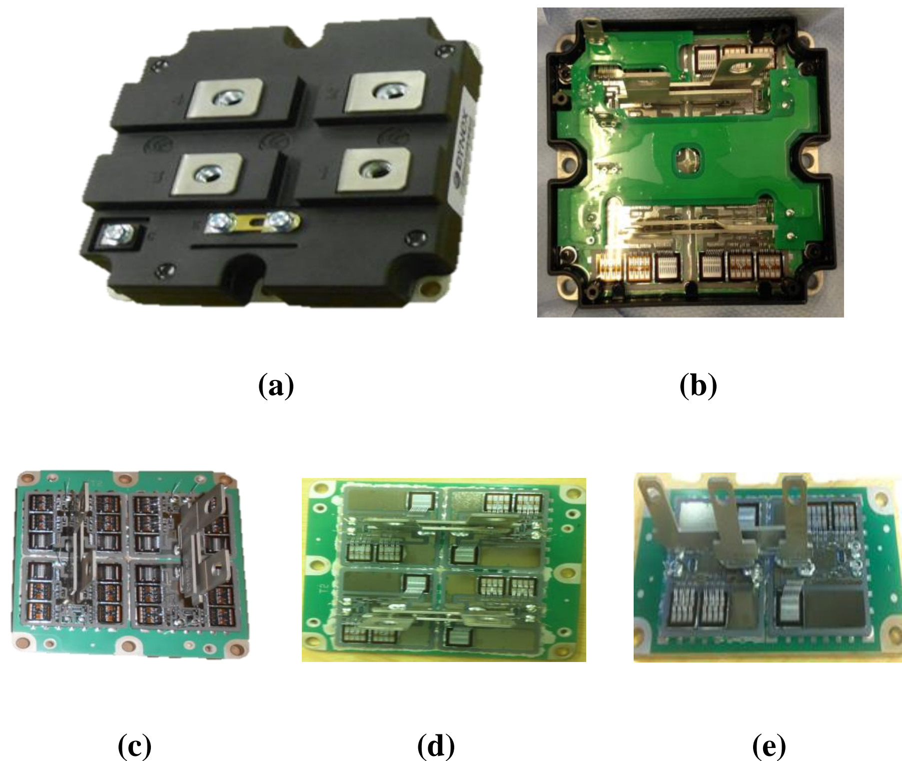


Figure 0.6: Open and Closed 3.3 kV IGBT Power Modules from Dynex Semiconductor Ltd: (a) Closed DIM800NSM33-F, (b) DIM800NSM33-F Without Resin and Busbars Left Upright for Easy Interior Access During Tests, (c) Open DIM800NSM33-F, (d) Open DIM400NSM33-F and (e) Open DIM100PHM33-F.

ii. Inductive Load

To emulate typical application load conditions, the IGBT modules were tested under inductive load. Figure 0.7 shows the inductive air core inductor coils utilized, which are rated at 200 μH, 40 mΩ each. Air core inductor coils are light-weight and allow the load to be purely inductive minimising losses hence improving stability of the dc-link voltage compared to iron cores. Using a connector block shown in Figure 0.7, combination of series and parallel connection of the coils yielded total inductance a ranging from 50 μH to 800 μH. The DIM800NSM33-F IGBT power module shown in Figure 0.7 is employed as free wheel diode across the air coils. Hence its gate and emitter are short circuited so that it is off at all times.

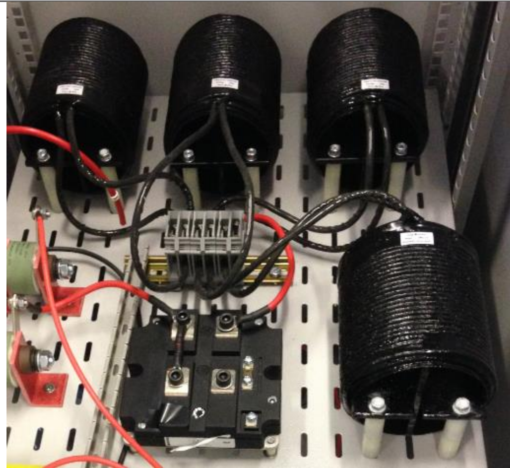


Figure 0.7: 200 μH, 40 mΩ Air Core Inductor Coils and Associated Connector Block and FWD.

iii. High-Voltage Resistors

(a) **(b)**

Figure 0.8: 2 kV Resistors: (a) 2.7 Ω (power circuit current limiting) and (b) 9.9 kΩ (dc-link capacitor discharge).

Figure 0.8 shows HV resistors installed in the IGBT test rig for use as current limitting in the power circuit and discharging dc-link capacitor. Sizing of the resistors is discussed in this section.

DC-link Current Limitting Resistor Sizing

Testing of 3.3 kV IGBT power modules is normally conducted in the range 1.8 kV – 2 kV to prevent overshoot from exceeding the IGBT rating. The test rig has been designed to supply dc-link voltage from 0 to 2 kV. Hence 2 kV dc-link capacitors were

employed. As the peak current rating of the DIM800NSM33-F IGBT is 1600 A and continous rating is 800 A, 2200 A (nearest rating) capacitors were sourced to allow tests up to 1600 A. To prevent the risk of exceeding the device current rating, tests were conducted at 800 A which is within the maximum continous current rating of the DIM800NSM33-F. 35% duty cycle was utilized from the pulse generator to ramp the dc-link current to 800 A. The pulse generator employed is a Tektronix AFG3102.

However if a duty cycle exceeding 35% is accidentally applied, the device maximum current rating is exceeded. To ensure the dc-link current is limited to 800 A of IGBT maximum continous current rating, current limitting resistors were added to the power circuit - a precaution at the expense of the resistor power losses.

Required current limitting resistor size = 2000 V/1600 A = 1.25 Ω.

The nearest standard size from the HV resistors sourced is **2.7 Ω**. Hence two of these were connected in parallel in order to obtain 1.35 **Ω**.

Sizing of dc-link capacity discharge resisor is discussed in Capacitors section below.

iv. DC-link Capacitors

Figure 0.9: DC-link Capacitors

The make and model of the dc-link capacitors in Figure 0.9 is Eaco SHP-2500-280-FS rated at 280 μF, 2500 V dc, 2200 A. Once fully charged, the dc-link capacitors provide

high-voltage (from 0 to 2000 V dc) and high-current (from 0 to 2200 A dc) for IGBT pulse tests.

DC-link Capacitor Sizing

From the IGBT test circuit, assuming duty cycle of 1, the maximum system power (including losses) is

$$P_D = \text{duty cycle x dc-link voltage x dc-link current} = 1 \text{ x } 2000 \text{ V x } 800 \text{ A} = 1.6 \text{ MW}$$

The double pulse duration is 250 μs hence

$$\text{Energy} = 1.6 \text{ MW x } 250\ \mu\text{s} = 400 \text{ Joules}$$

This is the energy the capacitor should be able to support.

From $E=1/2(CV^2)$, required Capacitance = 2 x 400 J/(2000 V x 2000 V) = 200 μF

To be conservative, a 300 μF is the minimum dc-link capacitor size required.

Summary of Capacitor Requirement: **300 μF, 400 Ws, 2000 V** (typical dc-link for 3.3 kV IGBT applications)**, 800 A** (IGBT maximum continous current rating)**, >45 V/ns** **(**IGBT V_{CE} transient).

Despite system losses the dc-link voltage should remain stable (within 5% [119]) for the test duration. Simulation results of different capacitor sizes in Figure 0.10 depict the optimal capacitance between 500 μF and 1000 μF to last at most 3 pulses. Consequently **840 μF** (nearest ideal size) dc-link capacitance were installed using 3 Eaco SHP-2500-280-FS.

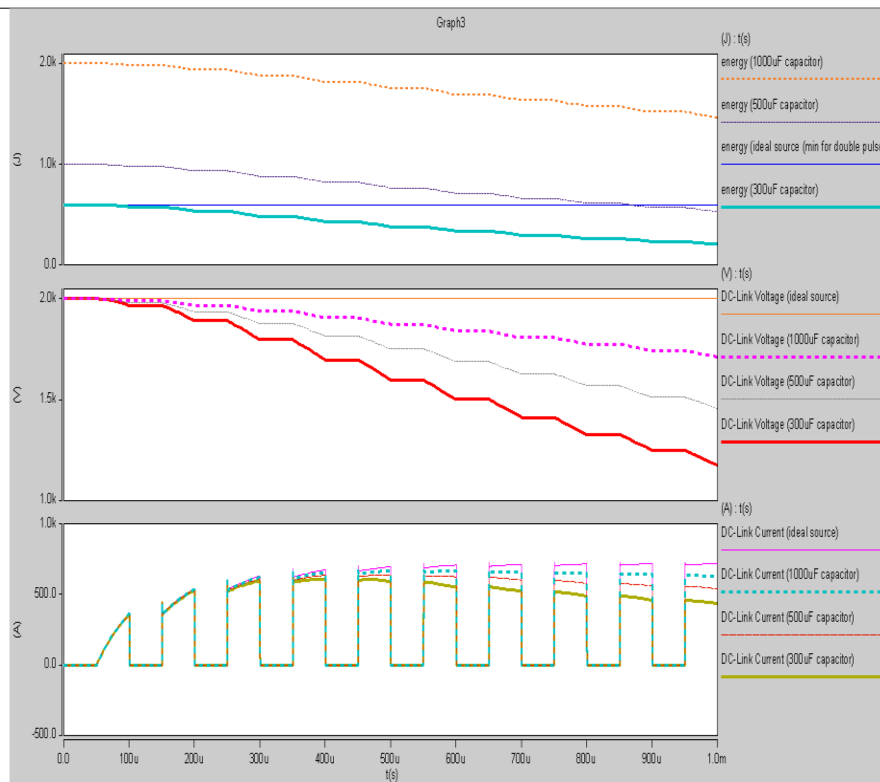


Figure 0.10: Performance for Different Capacitor Sizes for IGBT Pulse Tests.

Scenario of IGBT DUT Failing to Switch-off

As the test rig is a pulse tester, the power circuit components (especially the power cables, inductive air coils and connector block for air coils) were sized according to the cyclic rather than continuous power/current rating in order to minimise cost. However, in the event that the IGBT DUT fails to turn-off there is a risk that the component power/current ratings are exceeded.

Simulation results in Figure 0.10 show that the capacitors will discharge at a rate that allows power to collapse fast enough until the capacitors are fully discharged. This is because the rate of discharging the capacitors is much lower than that of charging them (20 s and 630 s respectively from next section). Consequently the energy profile is not continuously constant thus the components can be de-sized.

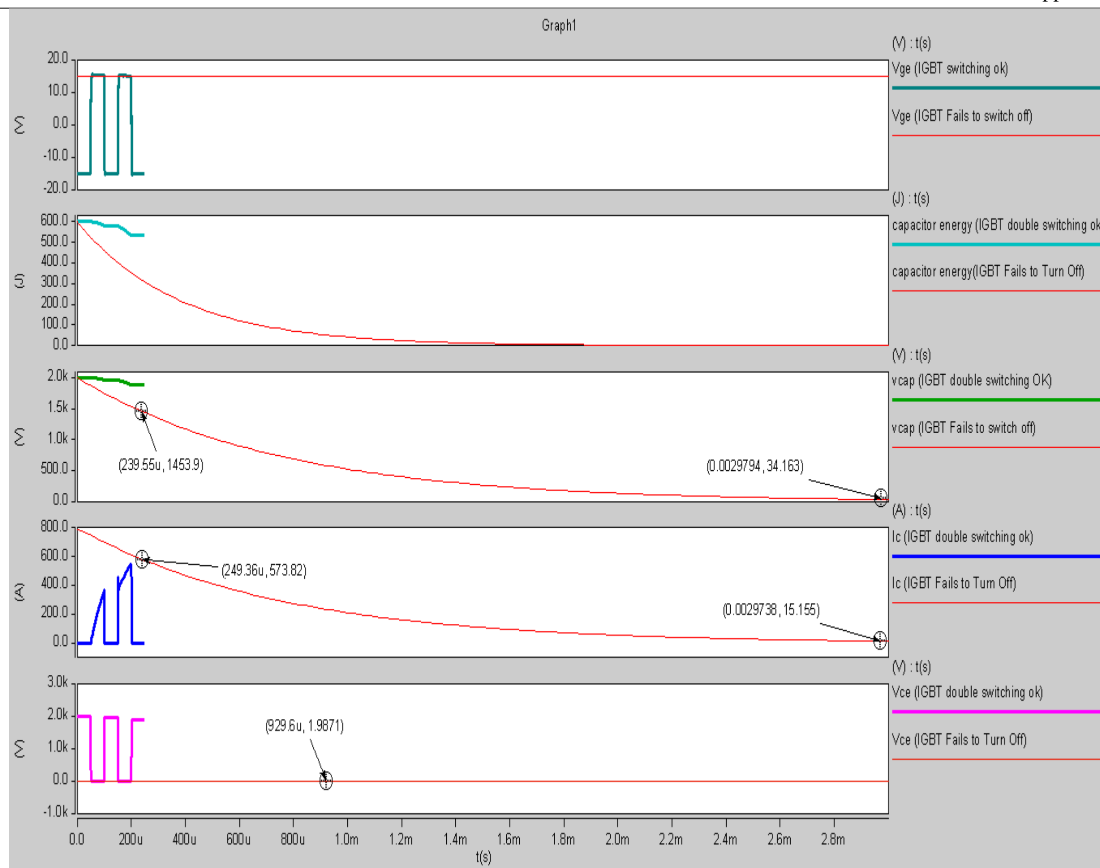


Figure 0.11: No Harmful Effects When IGBT Fails to Turn-off as Capacitor Fully Discharges Within a Short Period (3ms hence within permissible component ratings).

Charging of DC-link Capacitor

A 2000 V, 1600 A power supply is not practical in a laboratory environment. A cheap solution for the power supply was a 2000 V, 15 mA Power Supply Unit (PSU) UM2P30 from Spellman HV Electronics Ltd. The dc-link capacitor charging time is limited by the 15 mA charging current from the UM2P30.

A charging resistor is required to ensure that the PSU short-circuit protection is not activated by an initial zero charge on dc-link capacitor during initial charging. The PSU incorporates the required charging resistance. The required minimum resistor size is simply determine as

2000 V/15 mA = 133333 Ω, nearest size is **150 kΩ.**

Although the PSU provides a small charging current, the waiting time for capacitor maximum charge, prior in preparation for IGBT test, is reasonable.

$$t = CR = 840\ \mu F \times 150\ k\Omega = 126\ s \Rightarrow 37.5\%\ \text{charge} \Rightarrow 100\% \sim 5t = \mathbf{630\ s}$$

Discharging of DC-link Capacitor

The dc-link capacitors need discharging for the following reasons:

- End of test – using a manual key switch on the test rig,
- Door is open – a door micro-switch on the test rig activates the discharge, and
- Emergency push button is pressed.

In order to maintain a stable dc-link voltage during tests, the dc-link capacitor discharge resistor is not permanently online. A switch (R2) shown in Figure 0.5 was employed to facilitate controlled switching-in of the dc-link discharge resistors. As the dc-link current rating is 2200 A, it is not practical/economic to use a switch at this high-current magnitude. A 2 A mercury Reed relay was rather used in combination with discharge resistors which limit the discharge current to 2 A.

$$\text{Required minimum discharge resistance} = 2000\ V/2\ A = 1000\ \Omega$$

Two 9.9 kΩ were sourced for discharging the dc-link capacitors. These were connected in parallel resulting in 4.95 kΩ for a good head room to prevent over current on the reed relay.

The discharge rate is reasonable for safety in the event of a short circuit; dropping of the dc-link voltage in emergency; and general waiting between tests.

$$t = CR = 840\ \mu F \times 4950\ \Omega = 4.2\ s \Rightarrow 37.5\%\ \text{discharge} \Rightarrow 100\% \sim 5t = 20\ s$$

v. Test Meters

6 kV HV differential probes (THDP0100 from Tektronix) were utilized for V_{CE} waveform tracing and 30 V LV differential probes for V_{GE}. Since the IGBT power modules tested were rated at 3.3 kV and inductive load was utilized, 6 kV HV probes

provided enough insulation and good safety headroom allowing for IGBT test voltage overshoot. Shunt resistors (also known as current viewing resistors) have been employed for I_C waveform tracing while miniaturized Rogowski coil meter was utilized for I_G.

All the IGBT waveforms (V_{GE}, I_G, V_{CE} and I_C) were measured on each IGBT test as shown Figure 0.12 which includes V_{GG} and $V_{GE(pre\text{-}th)}$. This allowed TSEP investigations on all IGBT electrical signals as well as easy fault finding in the event of a test rig/component failure. The waveforms were output on oscilloscopes.

The main consideration in selecting the test meters and oscilloscopes was ensuring that their bandwidths can sufficiently capture the IGBT switching transients. For example, THDP0100 bandwidth of 800 MHz can sufficiently sample typical IGBT V_{CE} rise at:

$$dV_{CE}/dt = (1800\text{-}200)\ \text{V}/85.236\ \text{ns} = 18.7\ \text{V/ns} = 18.7\ \text{kV}/\mu\text{s}$$

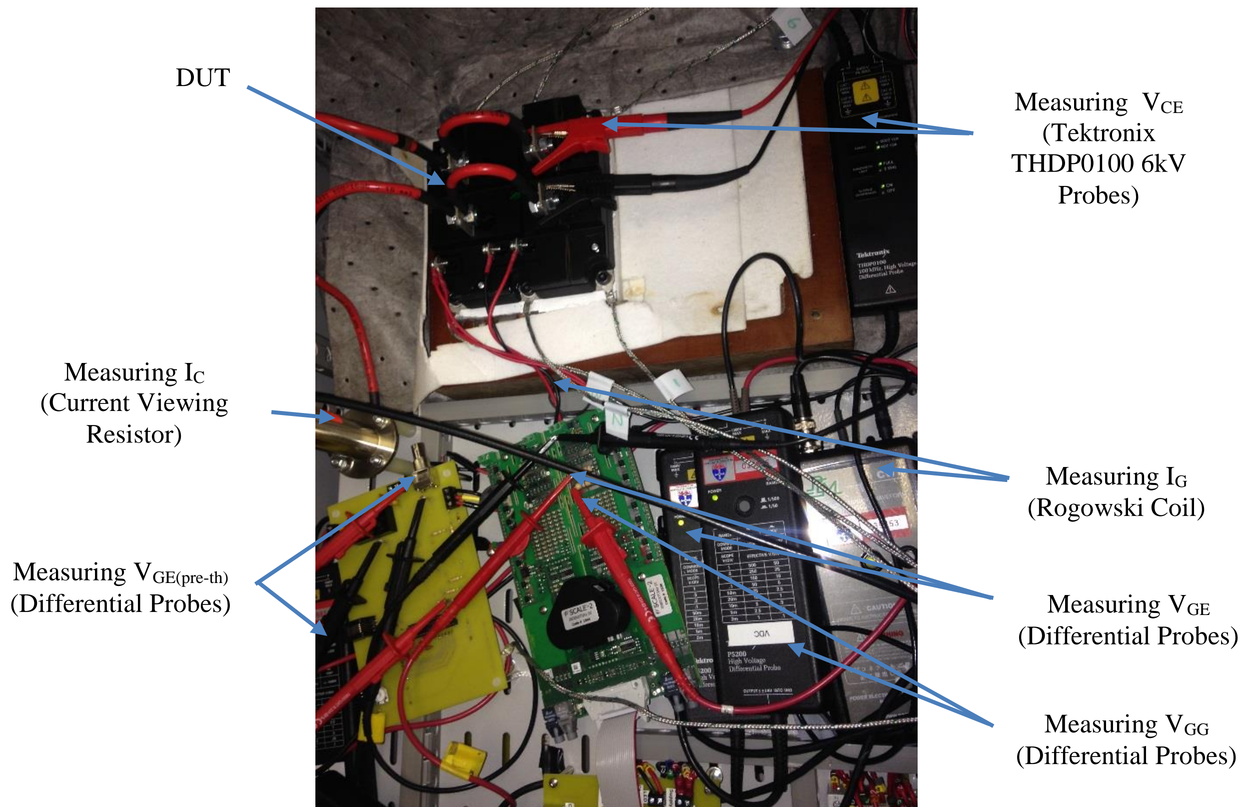


Figure 0.12: Measurements Performed on Each IGBT Test.

vi. Oscilloscopes

Figure 0.13: Agilent DPO3014 and MSO4034 Oscilloscopes.

The make and models of oscilloscopes in Figure 0.13 are: MSO4034 (350 MHz, 2.5 GS/s) and DPO3014 (100 MHz, 2.5 GS/s). MSO stands for Mixed Signal Oscilloscope while DPO stands for Digital Phoshor Oscilloscope. At least six signals had to be monitored on each test: V_{GG} (PWM), $V_{GE(pre\text{-}th)}$, V_{GE}, I_G, V_{CE} and I_C. The DPO3014 and MSO4034 have only four signal ways hence they were both were utilized. The MSO4034 has a bigger screen and was utilized for the four IGBT waveforms V_{GE}, I_G, V_{CE} and I_C and the DPO3014 for V_{GG} and $V_{GE(pre\text{-}th)}$.

Oscilloscope Sampling Frequency Settings

This section describes setting of the sampling rate which is crucial to ensure the oscilloscope captures the fastest transient of the IGBT waveforms.

From datasheet, the smallest transient time is the rise time at 25 °C of 270 ns. Hence minimum sampling frequency required form oscilloscope = 1/270 ns = 3 700 000 Hz x 2 (Nyquist) = 7.4 MHz

This is further multiplied by 5 as a rule of thumb to ensure sufficient sampling since the generic value from datasheet changes from device to device.

Therefore required sampling frequency = 7.4 MHz x 5 (rule of thumb) = 37 MHz

To allow for differences in IGBTs, the oscilloscope samples/s setting applied was **50 MS/s**

Oscilloscope 'Points' Settings

The oscilloscope settings should allow at most 3 pulses to be analysed for each test. The frequency used is 1 kHz typical in HV applications. At this frequency, duration for 3 pulses = (1/1000 Hz) x 3 = 3 ms.

Hence oscilloscope setting of number of points that was applied is

50 MS/s x 3 ms = 150 000 samples = **150 000 points**

vii. Test Rig Enclosure

Due to HV involved, a metal enclosure shown in Figure 0.15 has been utilized. The metal work of the test rig was grounded to earth. All components within the metal enclosure were mounted on sheet metal plates to enable effective grounding of any fault or unwanted discharge. For safety, the enclosure has been fitted with a safety door interlock mechanism using a door solenoid; once the tests are in progress the door cannot be opened. In addition, a door micro-switch was fitted such that power supplies are disabled and dc-link capacitors discharged when the enclosure door is open.

Isolation

Three dc voltages (15 V dc, 24 V dc and 2000 V dc) are utilized in the rig. Isolated dc–to-dc converters provided isolation of LV components (24 V and below) from HV (2000 V power circuit). In addition, the negative terminal of the dc-link capacitors and power circuit was kept separate from that of the LV circuits.

viii. Complete Test Rig

The complete test rig is shown in Figure 0.14, Figure 0.15 and Figure 0.16 including PCBs that provide the necessary controls and isolation as depicted in Figure 0.5 schematic.

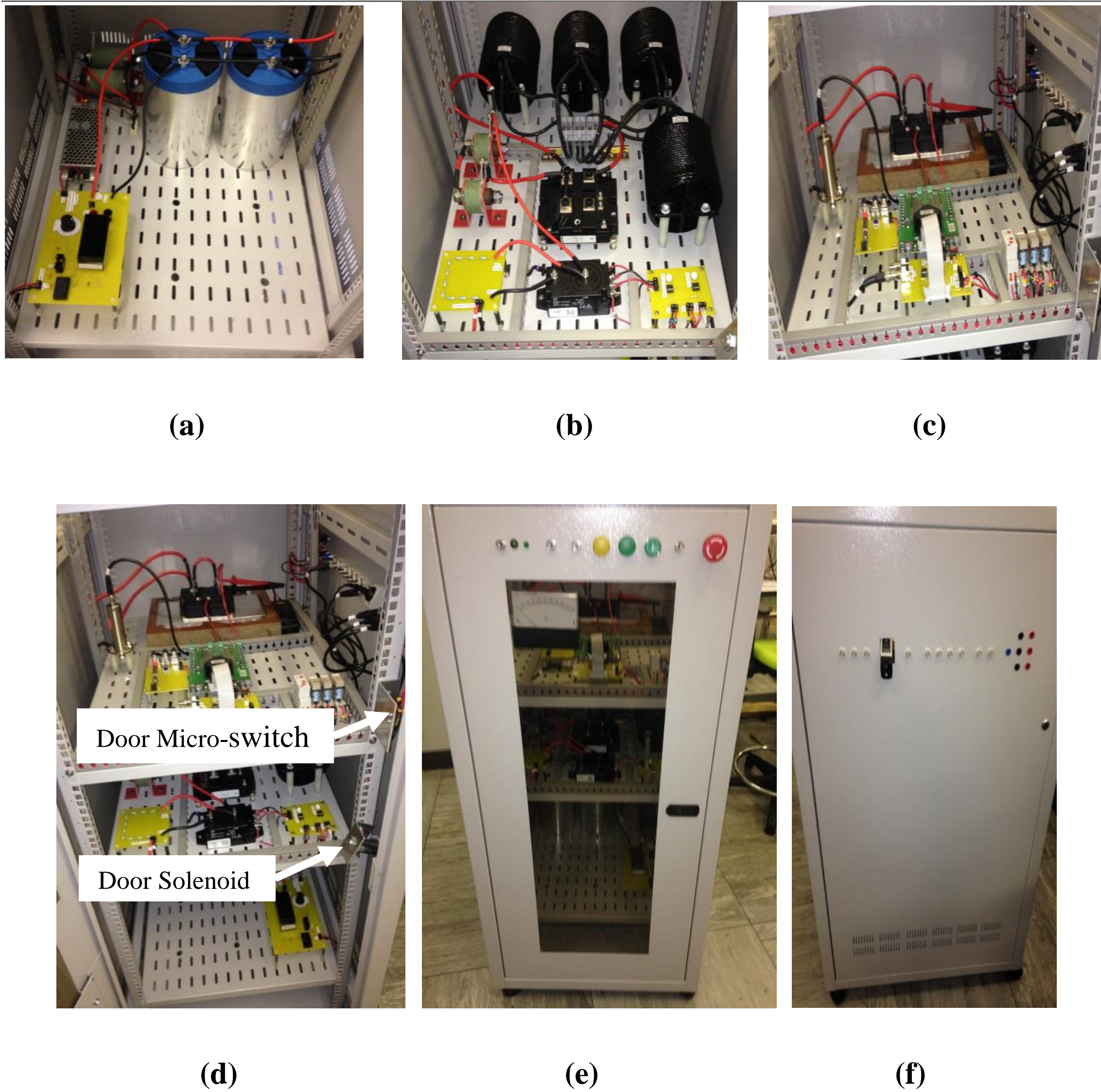


Figure 0.14: IGBT Test Rig Panels and Shelves: (a) Bottom Shelve (dc-link capacitors), (b) Middle Shelve (air coils), (c) Top Shelve (DUT), d) Safety Door Interlocks, (e) Front Panel (control switches and indicators) and (f) Side Panel (auxiliary dc supplies and oscilloscope terminals).

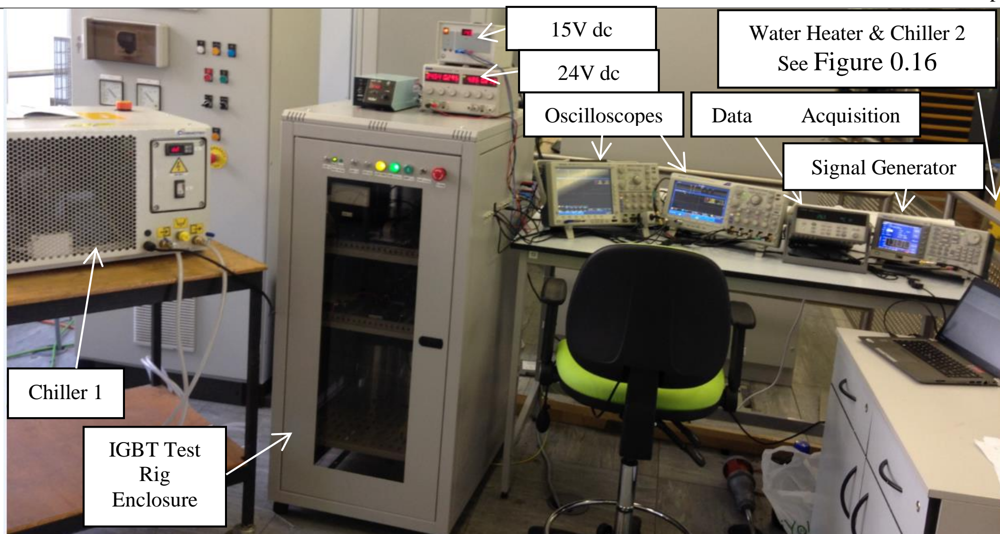


Figure 0.15: IGBT Test Rig Workstation.

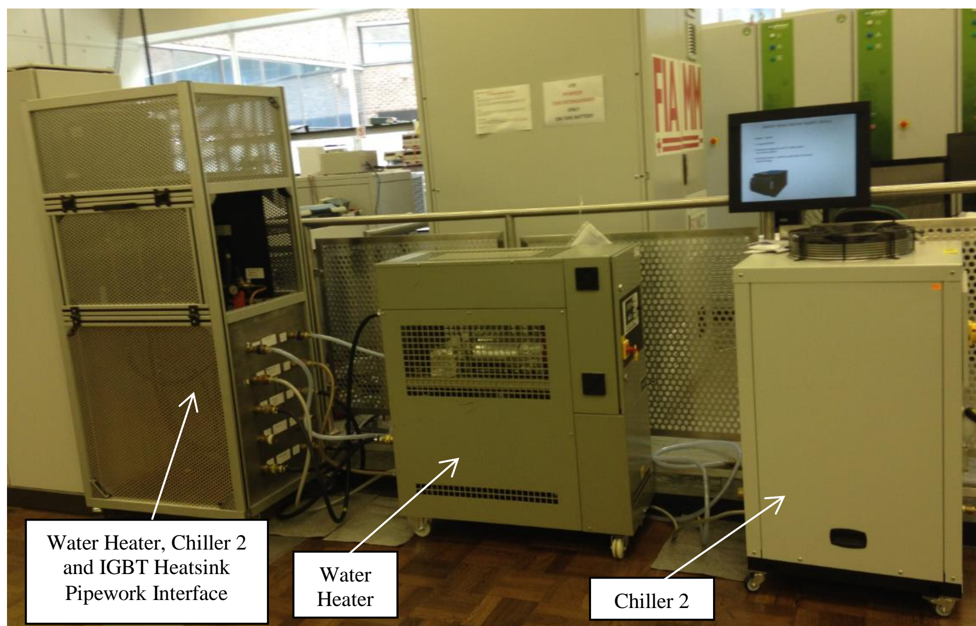


Figure 0.16: Mechanical Rig Linking Water Heater, Chiller 2 and IGBT Heatsink Pipework.

In Figure 0.16 the mechanical rig interfaces the water heater, chiller 2 and IGBT heatsink pipework as illustrated in Figure 0.17. The IGBT heatsink, where IGBT DUT baseplate is mounted, is located within the IGBT test rig in Figure 0.15 and provides controlled temperature from 10 °C (minimum capability of chiller) to 125 °C (precaution for IGBT maximum temperature rating). Thermocouples (Type K Stainless Steel Washer probes with a tolerance of +/-1.5 °C [115]) are connected to the IGBT module baseplate and the baseplate temperature is monitored on the Data Acquisition

Unit shown in Figure 0.15. Figure 0.17 illustrates a configuration for maintaining heatsink 1 and 2 at different temperatures. The IGBT module can either be mounted on heatsink 1 which varies the IGBT baseplate temperature as a whole. Alternatively the IGBT module can be mounted across the heatsinks 1 and 2 so that part of the baseplate and associated chips are at different temperature the remaining part of baseplate and IGBT chips. This kind of set-up allows emulation of typical scenario in real application where the IGBT chips of a multichip IGBT power module often exhibit mismatching properties which causes unequal current sharing hence different T_j's across the IGBT chips [45, 120].

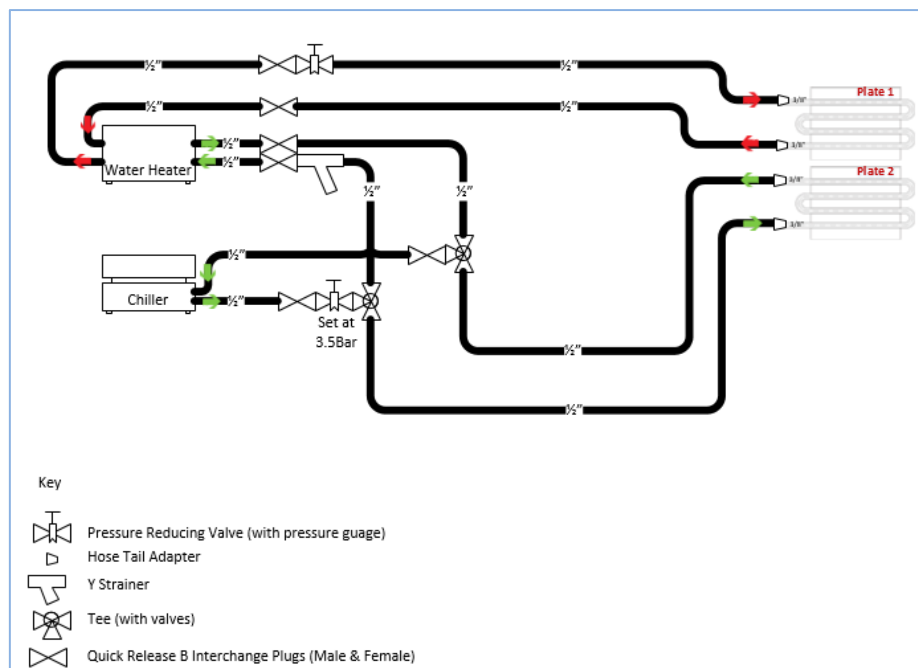


Figure 0.17: Typical Pipework Connection of Mechanical Chiller/Water Heater/Heatsink Mechanical Rig.

Appendix D: In-situ Health Monitoring Circuit

i. C Code for PIC

```
#include <p18f24k22.h>    //header file for device
#include <xc.h>
#include <stdint.h>          //header file for standard types - uint8_t
#include <stdlib.h>
//fuse settings
//#pragma config MCLRE = ON, CP0 = OFF, CP1 = OFF, CPD = OFF, BOREN = OFF, WDT = OFF
//#pragma config PWRT = OFF, OSC = INTIO67, PBADEN = OFF, LVP = OFF, DEBUG = ON

#pragma config PLLCFG=ON
#pragma config PRICLKEN=ON
#pragma config IESO=OFF, FCMEN=ON
#pragma config WRT0=OFF, WRT1=OFF, STVREN=ON

#pragma config MCLRE = EXTMCLR, CP0 = OFF, CP1 = OFF, CPD = OFF, BOREN = OFF, WDTEN
= OFF
#pragma config PWRTEN = OFF, FOSC = INTIO67, PBADEN = OFF, LVP = OFF, DEBUG = ON

#define _XTAL_FREQ 64000000    // device clock frequency
#define FOSC 64000000

void main()
  {
   //Variable declarations
   uint16_t value, dacvalue;

   //Initialise the PIC
   OSCCONbits.IRCF = 0b111;       //use internal 16MHz clock (FOSC=8MHz)
   OSCCON2bits.PLLRDY = 1;
   OSCTUNEbits.PLLEN = 1;

   TRISC = 0b00000000;           //Port C all outputs
   TRISB = 0b00000000;           //Port B all outputs
   TRISA = 0b00000011;           //Port A B7/B6/B5/B4/B3/B2 outputs

   ANSELC = 0b00000000;          //Port C all digital
   ANSELB = 0b00000000;          //Port B all digital
   ANSELA = 0b00000001;          //Port A B7/B6/B5/B4/B3/B2 outputs

   ADCON2bits.ADFM = 1;          //A/D Result Format Right Justified
   ADCON2bits.ADCS = 0b110;
   ADCON0bits.CHS = 0b00000;        //select AN0 for input

   ADCON0bits.ADON = 1;          //A/D Converter is operating

    // Set up the DAC
   VREFCON1bits.DACOE=1;       // enable the DAC output pin (RA0)
   VREFCON1bits.DACPSS=0x00;    // DAC Voltage source is VDD
   VREFCON1bits.DACEN=1;       // turn-on DAC

    do
     {

       while (PORTAbits.RA1==1)
          {
          __delay_ms(0.0012);
```

```
 ADCON0bits.GO_nDONE = 1;        //start A/D conversion
while(ADCON0bits.GO_nDONE == 1);    //wait for A/D conversion to complete

value = ADRESH;                 //read MSB of ADC result

value = value << 8;             //shift left 8 bits
value = value + ADRESL;   //read LSB of ADC result. value now contains a 10-bit ADC
 number

dacvalue = (value >> 5) & 0x1F;

VREFCON2bits.DACR = dacvalue;

 __delay_ms(0.35);                       // wait a little bit

 ADRESH = 00000000;
 ADRESL = 00000000;

 VREFCON2bits.DACR = 00000000;     // Reset D/A Converter


        }
    } while (1);
}
```

ii. C Code for LCD

```
#include <p18f24k22.h>      //header file for device
#include <xc.h>
#include <stdint.h>     //header file for standard types - uint8_t
#include <xlcd.h>
#include <stdlib.h>
#include <string.h>

//fuse settings
#pragma config PLLCFG=OFF
#pragma config PRICLKEN=ON
#pragma config IESO=OFF, FCMEN=OFF
#pragma config WRT0=OFF, WRT1=OFF, STVREN=ON
#pragma config MCLRE = EXTMCLR, CP0 = OFF, CP1 = OFF, CPD = OFF, BOREN = OFF, WDTEN
= OFF
#pragma config PWRTEN = OFF, FOSC = INTIO67, PBADEN = OFF, LVP = OFF, DEBUG = ON

#define _XTAL_FREQ 64000000
#define FOSC 64000000

//set up lcd driver
//MCU              AT89C52
//LCD Drive:       SPLC708D/S6A0069/KS0066U
//-------------------------------------------------------------------------------------
//                  2005.11.14
//                    FDZ81
//-------------------------------------------------------------------------------------
//#include            <reg51.h>
//-------------------------------------------------------------------------------------
//LCM I/O
   #define    LCM_DATA       LATC                   /*  DATA BUS FOR LCD 8bits  */
   #define    E             LATBbits.LATB4          /*  Enable pin of LCD       */
```

```
    #define    RS          LATBbits.LATB3          /*  RS pin of LCD    PIN 4 on LCD     */
    #define    RW           LATBbits.LATB5

    #define LCD_BUS_DIRECTION   TRISC              /*  DATA bus tristate register  */
    #define ENABLE_DIRECTION    TRISBbits.TRISB4   /*  Enable pin tristate register*/
    #define RS_DIRECTION      TRISBbits.TRISB3     /*  RS pin tristate register    */
    #define RW_DIRECTION      TRISBbits.TRISB5     /*  RS pin tristate register    */
//
sbit            RS                  = P3^5;        //Define LCM Wdata/instruction pin
sbit            RW                  = P3^6;        //Define LCM READ/WRITE pin
sbit            E                   = P3^7;        //Define LCM CHIP ENABLE pin
#define         DATA_TYPE_4BIT      0
#define         DATA_TYPE_8BIT      1
#define         DEALY               2
#define         bitDataType         1

//-----------------------------------------------------------------------------------
void Delay10Ms(unsigned char d)
{
        unsigned int t;
        while(d--)
        {
                t = 5000;
                while(t--);
        }
}
//===========================================================================
=====
void LCMBusyCheck(void)
{
        LCM_DATA =0xff;
        while (1)
        {
                RS = 0;
                RW = 1;
                E  = 1;
                if ((LCM_DATA & 0x80) == 0x00)          break;
                E = 0;
        }
}
//===========================================================================
=====
void LCMWriteCommand(unsigned char d)
{
        char t = DEALY;

        t = 10;
        while(--t);
        //LCMBusyCheck();
        RS = 0;
        RW = 0;
        LCM_DATA = d;
        while(--t);
        E = 1;
        E = 0;
        if (bitDataType == DATA_TYPE_4BIT)
        {
                RS = 0;
                RW = 0;
                LCM_DATA = (d << 4);
                t = DEALY;
```

```
                while(t--);
                E = 1;
                E = 0;
        }
}
//==========================================================================
=====
void LCMWriteData(unsigned char d)
{
        char t = DEALY;

        t = 10;
        while(--t);
        //LCMBusyCheck();
        RS = 1;
        RW = 0;
        LCM_DATA = d;
        while(t--);
        E = 1;
        E = 0;
        if (bitDataType == DATA_TYPE_4BIT)
        {
                RS = 1;
                RW = 0;
                LCM_DATA = (d << 4);
                t = DEALY;
                while(t--);
                E = 1;
                E = 0;
        }
}
//==========================================================================
=====
void LCMWriteInitCommand(unsigned char d)
{
        char t = DEALY;

        RS = 0;
        RW = 0;
        LCM_DATA = d;
        while(t--);
        E = 1;
        E = 0;
        if (bitDataType == DATA_TYPE_4BIT)
        {
                RS = 0;
                RW = 0;
                LCM_DATA = d << 4;
                t = DEALY;
                while(t--);
                E = 1;
                E = 0;
        }
}
//==========================================================================
=====
void LCMInit(void)
{
        // set direction of port
        ENABLE_DIRECTION    = 0;
        RS_DIRECTION        = 0;
```

```
        RW_DIRECTION          = 0;
        LCD_BUS_DIRECTION  = 0;
        Delay10Ms(3);
        LCMWriteInitCommand(0x30);
        Delay10Ms(3);
        LCMWriteCommand(0x30);
        Delay10Ms(3);
        LCMWriteCommand(0x38);
        Delay10Ms(3);
        LCMWriteCommand(0x0c);                    //display on,cursor off,blinks off
        Delay10Ms(3);
        LCMWriteCommand(0x06);                    //cursor shift = increment
        Delay10Ms(3);
        LCMWriteCommand(0x01);                    //clear display
        Delay10Ms(3);
        Delay10Ms(44);
        LCMWriteCommand(0x01);                    //clear display
        Delay10Ms(1);

        if(!bitDataType)
        {
                LCMWriteInitCommand(0x20);
                Delay10Ms(1);
                LCMWriteInitCommand(0x20);
                Delay10Ms(1);
                LCMWriteCommand(0x20);
                Delay10Ms(1);
                LCMWriteCommand(0x28);
        }
        else
        {
                LCMWriteInitCommand(0x30);
                Delay10Ms(1);
                LCMWriteInitCommand(0x30);
                Delay10Ms(1);
                LCMWriteCommand(0x30);
                Delay10Ms(1);
                LCMWriteCommand(0x38);
          }
        LCMWriteCommand(0x0c);                    //display on,cursor off,blinks off
        LCMWriteCommand(0x06);                    //cursor shift = increment

}
//======================================================================
=====
void LCMWriteExtendASIC(void)
{
        unsigned char i;

        for(i = 0xc0;i != 0;i++)
        {
                LCMWriteData(i);
        }
}
//======================================================================
=====
void LCMWriteMyChar(void)
{
        unsigned char codedisp1[8] = {0x1f,0x1f,0x1f,0x1f,0x1f,0x1f,0x1f,0x1f};
        unsigned char codedisp2[8] = {0x15,0x15,0x15,0x15,0x15,0x15,0x15,0x15};
        unsigned char codedisp3[8] = {0x1f,0x11,0x11,0x11,0x11,0x11,0x11,0x1f};
```

```
        unsigned char i;

        LCMWriteCommand(0x40);                              //Set CAM address
        for(i = 0;i <8;i++)
        {
                LCMWriteData(codedisp1[i]);
        }
        LCMWriteCommand(0x48);                              //Set CGRAM address
        for(i = 0;i <8;i++)
        {
                LCMWriteData(codedisp2[i]);
        }
        LCMWriteCommand(0x50);                              //Set CGRAM address
        for(i = 0;i <8;i++)
        {
                LCMWriteData(codedisp3[i]);
        }
        LCMWriteCommand(0x80);                              //Set DDRAM address
        LCMWriteData(0);                                    //DDRAM address = 0
        LCMWriteData(1);                                    //DDRAM address = 1
}
//===========================================================================
void main(void)
{
  //Variable declarations
  uint16_t value, dacvalue;

  //Initialise the PIC
  OSCCONbits.IRCF = 0b111;   //use internal 16MHz clock (FOSC=8MHz)

  TRISC = 0b00000000;        //Port C all outputs
  TRISB = 0b00000000;        //Port B all outputs
  TRISA = 0b00000011;        //Port A B7/B6/B5/B4/B3/B2 outputs

  ANSELC = 0b00000000;       //Port C all digital
  ANSELB = 0b00000000;       //Port B all digital
  ANSELA = 0b00000001;       //Port A B7/B6/B5/B4/B3/B2 outputs

  ADCON2bits.ADFM = 1;       //A/D Result Format Right Justified
  ADCON2bits.ADCS = 0b101;   //set ADC clock
  ADCON0bits.CHS = 0b00000;  //select AN0 for input

  ADCON0bits.ADON = 1;       //A/D Converter is operating

  // Set up the DAC
  VREFCON1bits.DACOE=1;          // enable the DAC output pin (RA0)
  VREFCON1bits.DACPSS=0x00;      // DAC Voltage source is VDD
  VREFCON1bits.DACEN=1;          // turn-on DAC

  do
   {
    __delay_us(1.18);          // wait a little bit for Vge(pre-th)

   ADCON0bits.GO_nDONE = 1;        //start A/D conversion
   while(ADCON0bits.GO_nDONE == 1);     //wait for A/D conversion to complete

   value = ADRESH;               //read MSB of ADC result

   value = value << 8;           //shift left 8 bits
   value = value + ADRESL;       //read LSB of ADC result. value now contains a 10-bit ADC number
```

```
dacvalue = (value >> 5) & 0x1F;

VREFCON2bits.DACR = dacvalue;

} while (PORTAbits.AN1==1);

Delay10Ms(11);

        unsigned char  i,j,d;
        unsigned char  ucDisplay[]= " Vge(pre-th) = dacvalue V ";
        unsigned char  ucDisplay2[]= " -- IGBT chips failed, Tvj: ----DegC ";
        unsigned char  ucDiffrenceChar[] = {0x61,0x71,0x81,0x91,0xa1,0xb1,0xc1,0xd1};

        // bitDataType = DATA_TYPE_8BIT;
        // biDataType = DATA_TYPE_4BIT;
        LCMInit();

        LCMWriteMyChar();
        while(PORTAbits.AN1==0)
        {

        LCMWriteCommand(0x80);
                {
                for(i=0;i<39;i++)
                {
                LCMWriteData(ucDisplay[i]);
                 }
                 Delay10Ms(11);

                  for(i=0;i<39;i++)
                   {
                        LCMWriteData(ucDisplay2[i]);
                   }
                   Delay10Ms(11);
                  }

            LCMWriteCommand(0x01);              //clear display
            Delay10Ms(11);
            }
    }
```

iii. Oscilloscope Screenshot for Figure 7.15

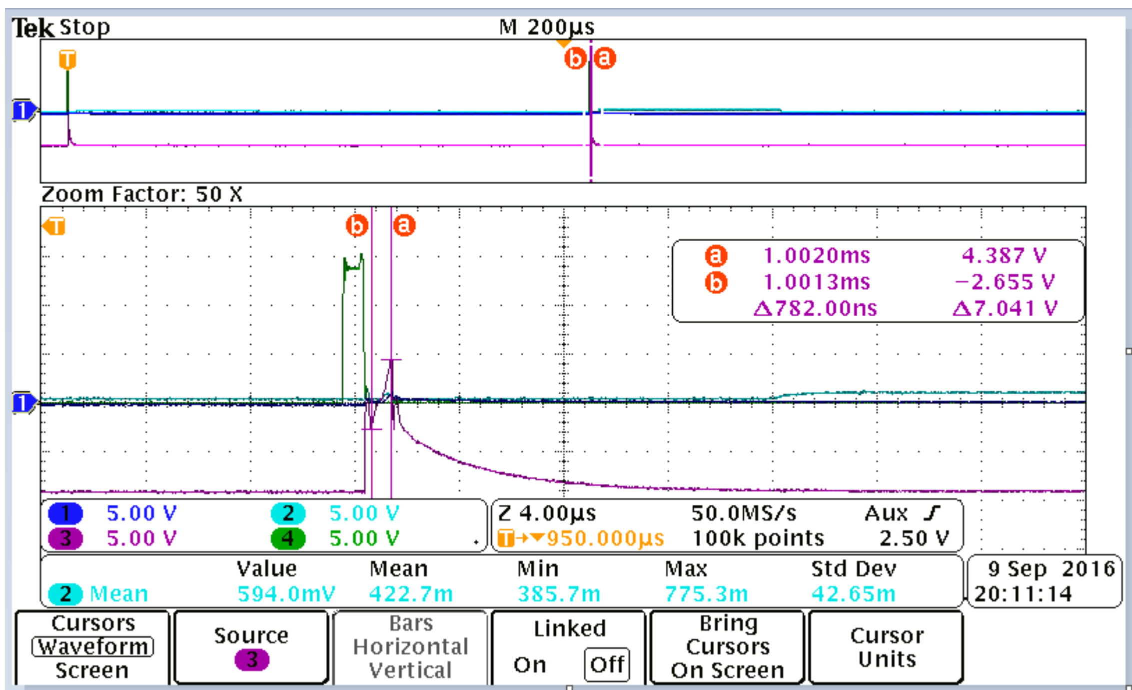


Figure 0.18: Oscilloscope Screenshot for Mode 1 in Chapter 7 tested at V_{CE} = 1800 V, I_C = 800 A: $V_{GD(cs)}$ (green), V_{GE} (pink), $V_{GE(pic)}$ (blue) and $V_{GE(pre\text{-}th)}$ (green).

iv. Oscilloscope Screenshot for Figure 7.16

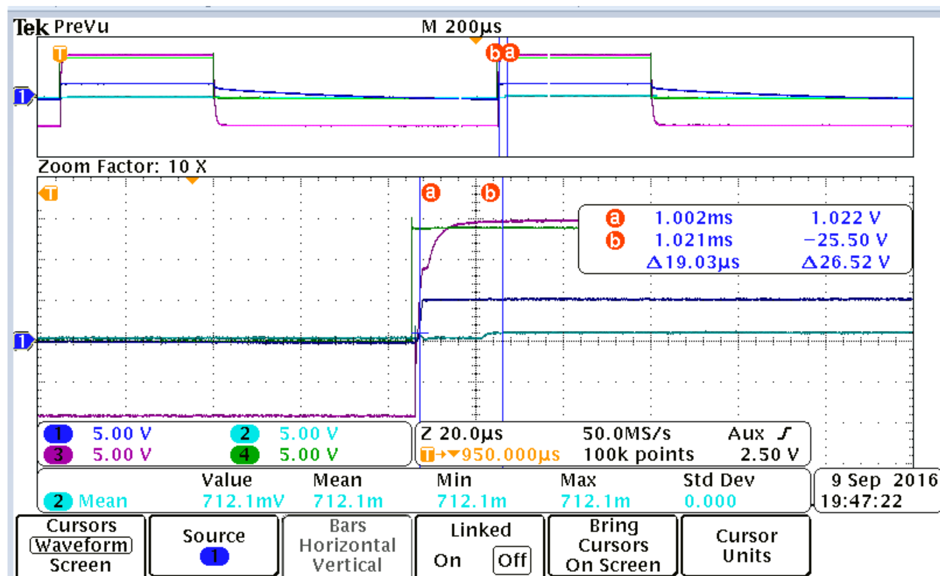


Figure 0.19: Oscilloscope Screenshot for Mode 2 in Chapter 7 tested at V_{CE} = 1800 V, I_C = 800 A: $V_{GD(cs)}$ (green), V_{GE} (pink), $V_{GE(pic)}$ (blue) and $V_{GE(pre\text{-}th)}$ (green).

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