Mitigation of DC Current Injection in Transformerless Grid-Connected Inverters

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Abstract

With a large number of small-scale PV plants being connected to the utility grid, there is increasing interest in the use of transformerless systems for grid-connected inverter photovoltaic applications. Compared to transformer-coupled solutions, transformerless systems offer a typical efficiency increase of 1-2%, reduced system size and weight, and reductions in cost. However, the removal of the transformer has technical implications. In addition to the loss of galvanic isolation, DC current injection into the grid is a potential risk. Whilst desirable, the complete mitigation of DC current injection via conventional current control methods is known to be particularly challenging, and there are remaining implementation issues in previous studies. For this reason, this thesis aims to minimize DC current injection in grid-connected transformerless PV inverter systems.

The first part of the thesis reviews the technical challenges and implementation issues in published DC measurement techniques and suppression methods. Given mathematical models, the performance of conventional current controllers in terms of DC and harmonics mitigation is analyzed and further confirmed in simulations and experiments under different operating conditions. As a result, the second part of the thesis introduces two DC suppression methods, a DC voltage mitigation approach and a DC link current sensing technique. The former method uses a combination of a passive attenuation circuit and a software filter stage to extract the DC voltage component, which allows for further digital control and DC component mitigation at the inverter output. It is proven to be a simple and highly effective solution, applicable for any grid-connected PV inverter systems. The DC link sensing study then investigates a control-based solution in which the dc injection is firstly accurately determined via extraction of the line frequency component from the DC link current and then mitigated with a closed loop. With an output current reconstruction process, this technique provides robust current control and effective DC suppression based on DC link current measurement, eliminating the need for the conventional output current sensor. Results from rated simulation models and a laboratory grid-connected inverter system are presented to demonstrate the accurate and robust performance of the proposed techniques.

This thesis makes a positive contribution in the area of power quality control in grid-connected inverters, specifically mitigating the impact of DC injection into the grid which has influences on the network operating conditions and the design and manufacture of the PV power converter itself.

To my beloved family

&

To the memories of my late grandfather.

This humble work is a sign of my love to you!

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Lastly, I would like to take this opportunity to express my thanks to the School of Engineering and Newcastle University. Without the support mentioned above, this PhD project could not have been accomplished.

List of Abbreviations and Symbols

Abbreviations

AC	Alternating Current
AI	Anti-Islanding
BP	Bipolar Modulation
CCS	Code Composer Studio
CM	Common-mode
CMRR	Common-mode Rejection Ratio
DAC	Digital to Analogue Converter
DC	Direct Current
DG	Distributed Generators
DM	Differential-mode
DMM	Digital Multi-meter
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
GCB	General Control Board
GUI	Graphical User Interface
HC	Harmonic Compensator
HFT	High-frequency Transformer
KVL	Kirchhoff's Voltage Law
LF	Loop Filter
LFT	Low-frequency Transformer
LPF	Low-pass Filter

MAF	Moving Average Filter
MCU	Microcontroller Unit
MMPD	Modified Mixer Phase Detector
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
OSG	Orthogonal Signal Generation
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PD	Phase Detector
PF	Power Factor
PI	Proportional-Integral
PLL	Phase Locked Loop
PR	Proportional-Resonance
PV	Photovoltaic
PWM	Pulse-Width Modulation
RMS	Root Mean Square
SRF-PLL	Synchronous Reference Frame Phase Locked Loop
STATCOM	Static Synchronous Compensator
SSE	Steady-state Error
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
UP	Unipolar Modulation
VCO	Voltage Controlled Oscillator
VSI	Voltage Source Inverter
ZCD	Zero Crossing Detector

Symbols

φ	Phase difference between PLL input and output
ω, ω'	Frequency of PLL input and output
$\emptyset, \emptyset'$	Phase angle of PLL input and output
ε_i	Current error in current control loop
ω_c	Bandwidth of PR controller
ω_{cut}	Cut-off frequency of attenuator
ω_0	Resonant Frequency of PR controller
ω_g	Grid frequency
ω_{res}	Resonance frequency
λ	Grid voltage factor in LCL transfer function
C_s	Capacitor in passive attenuation circuit
C_{DClink}	DC link capacitor
C_f	Filter capacitance of LCL filter
f_{cut}	Cut-off frequency
f_{sw}	Switching frequency
f_{sc}	Cut-off frequency of passive attenuation circuit
$G_{avg}(s)$	S-domain representation of averaging algorithm
$G_c(s)$	Transfer function of current controller
$G_d(s)$	Transfer function of time delay
$G_{ex}(s)$	Transfer function of line-frequency extraction
$G_f(s)$	Transfer function of output ripple filter
$G_{op}(s)$	Open loop transfer function of current control loop
$G_{cl}(s)$	Closed loop transfer function of current control loop
$G_{sin}(s)$	S-domain representation of Sine function
I_{DC}	DC current
I_{AC}	AC current
I_{DE}	DC determination from DC link sensing technique
I_{dcLink}	DC link current
I_{com}	Compensation current from DC suppression loop
I_{dc}	DC current injection

I_g	Inverter output current
I_{gm}	Measurement from current sensor
I_{offset}	Offset in the conditioning circuit
I_{ref}	Reference current
K_p	Proportional gain
K_i	Integral gain
K_r	Resonant gain
K_{rh}	Resonant gain at selected frequency
K_{pwm}	PWM gain
L_i	Inverter side inductance of LCL filter
L_g	Grid side inductance of LCL filter
M_i	Modulation index
p	Fictitious power of power PLL
P_{rated}	System rated power
r	Inductance factor in LCL calculation
R_d	Damping resistor
R_p	Parasitic resistance of laboratory inverter test rig
R_s	Resistor in passive attenuation circuit
R_{shunt}	Shunt resistor in external DC measurement circuit
S_C	Sensitivity of DC current determination from DC link current sensing
S_D	Sensitivity of DC voltage from DC link voltage feedback method
SI_P	Positive saturation index
SI_N	Negative saturation index
$S(t)$	Switching function of H-bridge
t_d	Dead-time
t_s	Steady-state time
T_s	Sample time
U_g	Grid voltage
U_{in}	Inverter output
V_{dc}	DC voltage measurement from two-stage filtering solution
V_{out}	Inverter output voltage

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Chapter 1 Introduction

1.1 Background

In the past century, the burning of fossil fuel has revolutionized the world with rapid industrial development, while there are unavoidable consequences that are seriously affecting public health and the environment. Apart from the obvious issues arising in the fossil fuel supply chain, the most serious risk in terms of universality and irreversibility is global warming associated with the combustion of fossil fuel [1]. It has been reported that over 70% of total greenhouse gas emission is carbon dioxide (CO_2), whilst over 60% of the CO_2 is emitted from the use of fossil fuels [2],[3]. Although there is a notable slowdown in the growth of global greenhouse gas emission, as long as CO_2 is emitted it will continue to build up in the atmosphere [4]. In order to stabilize, or even reduce the effect of global warming, the use of fossil fuel needs to be significantly reduced; and this has led to an increasing demand for clean and sustainable renewable energy resources.

As one of the most effective ways to fight against these environmental concerns, photovoltaic (PV) technology has experienced significant development and huge cost improvements over the past decade. Particularly in recent years, driven by the rising demand for electricity and the increasing competitiveness of solar PV energy, PV capacity has expanded exponentially in some regions [5]. According to data from the Renewables 2017 Global Status Report, additions to the worldwide PV capacity during 2016 reached 75 GW with an increase of 48% compare to 2015, which is greater than the cumulative world capacity five years earlier. Among this amount over 34 GW were contributed from China, representing nearly half of the global additions. Meanwhile the top five markets have been reported to be China, the United States, Japan, India and the United Kingdom, accounting for approximately 85% of additions. By the end of 2016, the total solar PV capacity reached 303 GW. Figure 1.1 shows the global cumulative solar PV capacity and annual additions between 2006 and 2016 [6]. Furthermore, due to the substantial demand from China, IHS Markit predicts another record-breaking year for global photovoltaics in 2018, forecasting new installations to hit 108 GW by the year's end [7]. Given a continued strong growth of PV deployment through to 2022, the global cumulative PV capacity is forecast to expand by over 920 GW. The International Energy Agency (IEA) envisions a contribution of 16% of global electricity from PV generation by 2050; this, in turn will lead to an annual reduction in carbon dioxide emission of 4 Gt in the process [8].

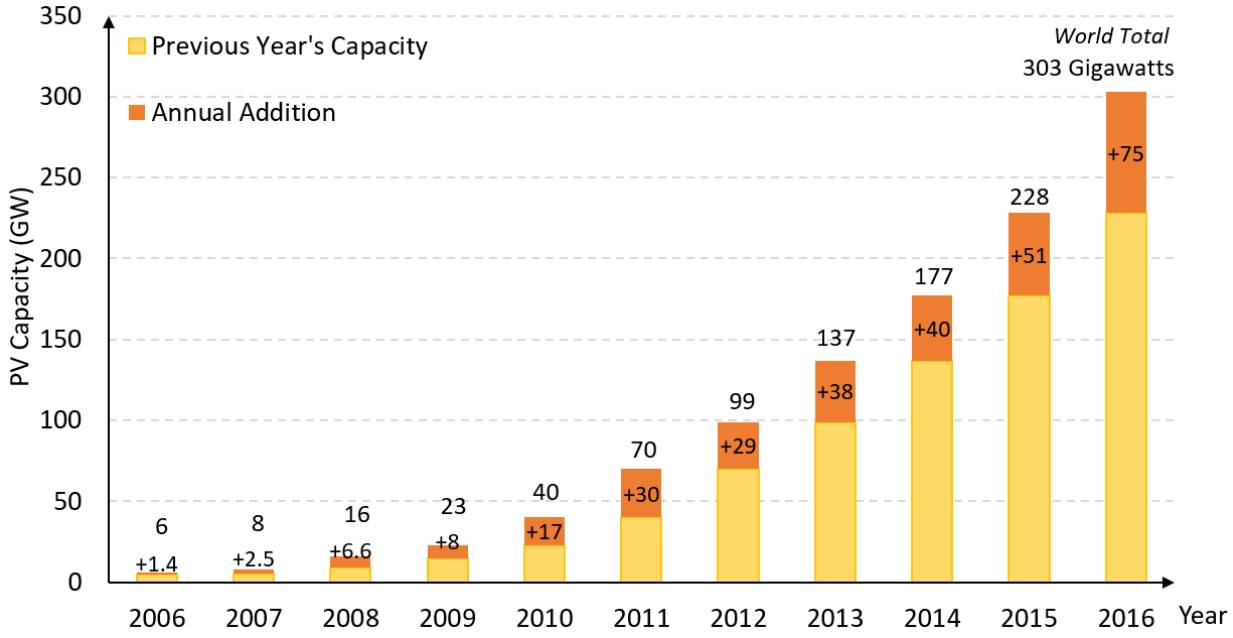


Figure 1.1 World solar PV capacity and annual additions between 2006 and 2016 [6]

While demand for off-grid (stand-alone) PV is growing rapidly, the capacity of grid-connected PV applications is expanding at a faster pace and continues to comprise the vast majority of global solar PV installations. Even though centralized large-scale grid-connected projects have accounted for a rising share of the annual addition compared to other renewable energy sources, one of the advantages of grid-connected PV generation is its wide-ranging power scale [5]. This makes it possible for individuals to implement PV plants, for example, in residential and industrial rooftop systems. Both consumers and power utilities can benefit from the widespread deployment of distributed PV applications which reduce capital expenditure, improve power quality and increase generation and transmission efficiency [9]. In 2016, a capacity of at least 20 GW grid-connected distributed PV systems have been installed worldwide. Supported by new policies established by some countries, there tends to be an increasing demand for small-scale residential PV systems [6].

Although PV panels are the core of a grid-connected PV system, they cannot be directly connected to the grid. Grid connection relies on power electronics technology, which is commonly a voltage source inverter (VSI), to work as an essential interface for a controllable and efficient interconnection between the PV panels and the grid [10]. Meanwhile PV inverter technology has been driven primarily by issues of efficiency and reliability, a large diversity of PV inverter structures are present in both academic research and commercial markets [11].

1.2 An Overview of Grid-Connected PV Inverter System

As stated earlier, PV systems broadly fall into stand-alone and grid-connected systems. The energy generated in stand-alone systems is consumed by local loads in the same place without the need for interaction with the grid [12]. Therefore, no grid-connected VSI is presented in such systems, and they are outside the scope of this study. Different PV inverter topologies in grid-connected systems are generally categorized based on the number of power processing stages, power scale, and the interconnection of the isolation transformer [13].

The single-stage inverter contains only a single power electronic stage between the PV panels and the grid to accomplish all the required functions, such as, maximum power point tracking (MPPT), output current control and voltage boosting. This is a typical configuration in centralized PV systems, in which the inverter must be carefully designed to handle a peak power of twice the nominal power [9],[14]. On the other hand, a two-stage topology employs a DC/DC converter between the PV panels and the inverter, performing voltage amplification and MPPT, while the second stage inverter converts the DC into high-quality AC power [15]. Such configurations can operate with a wide range of PV voltages or power scales, with relatively small DC link capacitors and low ripple content [16],[17]. For small-scale residential PV systems, a single-phase inverter is commonly utilized to interact with the low-voltage distribution grid. In some other cases, a three-phase topology might be utilized which is interfaced to the low- or medium-voltage distribution grid.

The last interconnection with the grid is through an isolation transformer. Conventionally, grid-connected systems typically employ a high-frequency transformer or a line-frequency transformer to provide galvanic isolation between the PV panels and the grid [13],[18],[19]. Such structures prevent the common-mode ground leakage current and DC injection issues, but they are bulky, costly and have less efficiency. Transformerless inverters have attracted increasing attention due to their reduced volume and high-efficiency performance, particularly in low-power applications [20-24]. Without galvanic isolation, some topological modifications and dedicated control schemes are required to ensure the power quality of the injected current.

In this study, the two-stage, single-phase, transformerless grid-connected PV inverter system is mainly considered, and the investigation focuses on the suppression of DC injection. Figure 1.2 shows an overview of a generic two-stage, grid-connected PV inverter system.

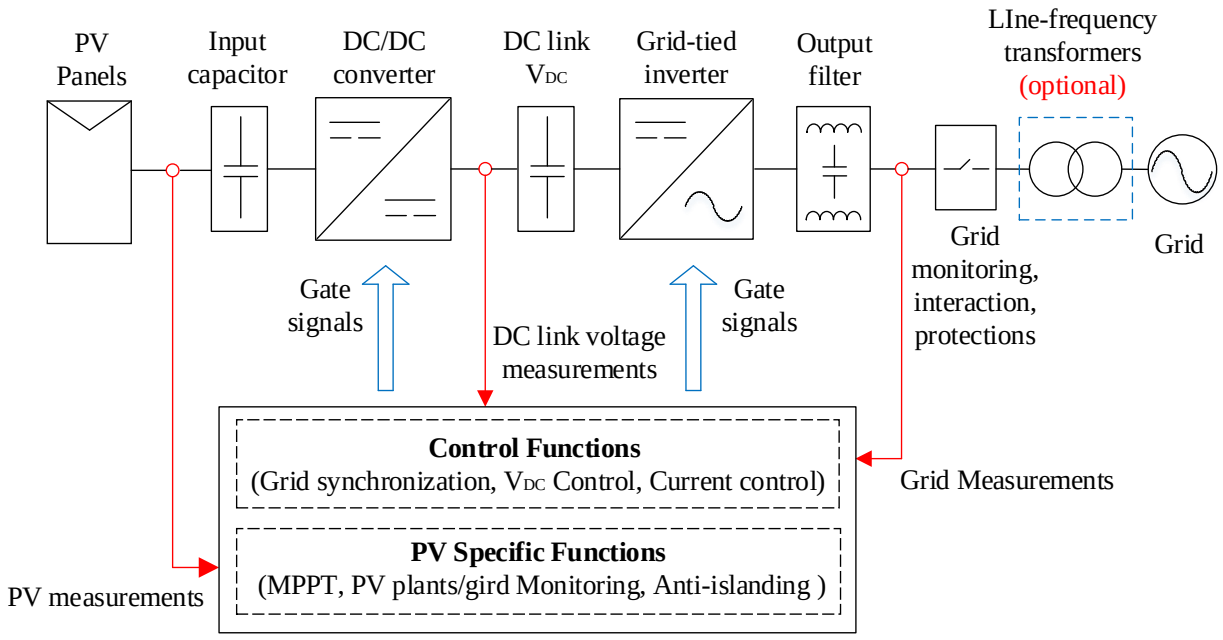


Figure 1.2 An overview of generic two-stage grid-connected PV inverter system [11]

The control functions are implemented to ensure the grid-connected PV inverter system injects a sinusoidal current to the grid at the highest possible conversion efficiency. More specifically, the outer loop, for DC voltage control, balances the active power between the DC side and the grid side by maintaining the voltage across the DC link capacitor at a specific reference level [25],[26]. Meanwhile the current controller and grid synchronization work together as an inner loop to regulate the output sinusoidal current, allowing for the PV inverter and the grid to work in unison. These control functions including output current control and grid synchronization techniques, are discussed in detail in this thesis.

Additionally, PV-specific functions are included to elevate systems robustness, efficiency and reliability [11]. In order to maximize the power extraction from the PV array, effective maximum power point tracking (MPPT) is necessary to track the MPP in all environmental conditions and to then force the PV system to operate at that point [27]. A large variety of MPPT algorithms have been proposed in the literature with tracking efficiencies up to 99% [28-31]. For a two-stage, grid-connected PV system, these algorithms are typically implemented at the DC/DC converter stage. To improve operational safety and reliability, PV plant monitoring and grid monitoring are crucial in grid-connected PV inverter systems [11],[32]. These monitoring systems aim to provide information about the energy potential, operating conditions of PV plant or the grid, and potential faults and energy losses associated with them [32-34]. The data being monitored can then be used

for failure detection or prediction, which is not only significant for the operation and maintenance of the PV plants, but can also ensure the safe and stable operation of the electric power system itself [35]. Meanwhile, the detection of possible island condition is another important feature of distributed power generation as islanding is hazardous to the safety of utility workers and the sensitive equipment that is connected to the electrical network [36],[37]. For this reason, the anti-islanding (AI) protection is required for grid-connected applications according to the standards to protect the integrity and reliability of the power system [38], [39].

1.3 Objectives and Scope of the Research

The utilization of unregulated residential PV systems can have a significant impact on the distribution network. In such systems, power quality aspects have to be addressed so as to ensure reliable grid performance and normal system operation. In recent times, new promising topologies and control methods have been implemented to facilitate less bulky, cost-effective, transformerless solutions. Unfortunately, without galvanic isolation, there are several well-understood technical and safety issues to consider. Among these issues is the risk of DC current flowing into the network which remains a potential concern. Whilst many methods are proposed in the literature there are technical challenges with sensing and controlling DC current injection. Consequently, the present research mainly focuses on the minimization of DC current injection in grid-connected transformerless PV inverter systems.

The specific objectives of the thesis are listed as follows:

- To review the advantages and disadvantages of published DC measurement or suppression techniques along with remaining technical challenges and research barriers.
- To study controller performance against power quality issues including DC and harmonic mitigation in grid-connected PV inverter systems.
- To develop cost-effective solutions to be used to suppress, or compensate for, DC current injection in the grid-connected transformerless inverter.
- To develop simulation models and experimental test rigs in order to validate the proposed DC suppression methods.

1.4 Contribution

The main original contributions of this research are summarized as follows:

- Published DC measurement techniques and suppression methods are categorized based on their desired characteristics. Hardware implementation issues such as the complexity of the design process or cost of components and technical challenges of DC suppression are highlighted.
- Mathematical models of the controller, PWM schemes and output filter are developed to determine the system's stability and the power quality of the injected current. The ineffectiveness of current control in terms of DC suppression is confirmed when the measurement devices suffer from offset-drift and non-linearity.
- A novel voltage filtering DC extraction approach is developed to detect and suppress the DC voltage component at the inverter output. The approach is low-cost, simple and highly effective and can make a positive contribution in any grid-connected PV inverter system.
- A control-based DC current suppression method using a DC link current sensing technique is developed to minimize DC injection for a grid-connected H-bridge inverter. Full mathematical derivations and detailed analyses are presented to validate the robust performance and cost-effective control offered by the proposed solution.

In conclusion, this thesis makes a positive contribution in the area of the power quality control of grid-connected inverters, and specifically in mitigating the impact of DC current injection into the grid, which has an impact on network operating conditions and the design and manufacture of the PV power converter itself.

The following papers have been presented and published in world-class conferences during the course of this project:

- **W. Zhang**, M. Armstrong and M. Elgendy, "DC component detection in grid-connected inverter systems, using a Mid-Ground Low Pass Filter approach," *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, Glasgow, 2016, pp. 1-6.

- **W. Zhang**, M. Armstrong and M. Elgendy, "DC current determination in grid-connected transformerless inverter systems using a DC link sensing technique," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 5775-5782.

In addition, two journal papers presenting the thorough mathematical analyses and the experimental outcomes have been published in IEEE transaction on Energy Conversion:

- **W. Zhang**, M. Armstrong and M. Elgendy, "DC Injection Suppression in Transformer-less Grid Connected Inverter using a DC Link Current Sensing and Active Control Approach," in *IEEE Transactions on Energy Conversion*, vol. 34, no. 1, pp. 396-404, March 2019.

- **W. Zhang**, M. Armstrong and M. Elgendy, "Mitigation of DC Current Injection in Transformer-less Grid-connected Inverters Using a Voltage Filtering DC Extraction Approach," in *IEEE Transactions on Energy Conversion*, vol. 34, no. 1, pp. 426-434, March 2019.

1.5 Thesis Overview

This thesis consists of seven chapters. This chapter introduces the significant development of PV generation in recent years and discusses the general operation of grid-connected PV inverter systems. The objectives and scope are stated, and the contribution of the research is highlighted.

Chapter 2 discusses the DC injection issue in the transformerless grid-connected inverter. The causes and impacts of DC current injection are first stated. In order to regulate the DC current within the suggested guidelines and standards, many measurement techniques and suppression methods have been proposed which are categorized and reviewed in this chapter.

Chapter 3 presents a model and describes the operation of a grid-connected full-bridge inverter system. The grid synchronization techniques, current controllers, PWM schemes and output filters are investigated. Based on the derived control functions, a mathematical model of VSI is developed, and an analysis of its stability is conducted. The simulation results of the VSI system demonstrate the theoretical analysis and reveal the existence of DC current injection.

Chapter 4 first introduces the experimental set-up of the inverter test rig, including the hardware arrangement, controller platform, measurement circuits and auxiliary protection. Then, based on the given parameters, the experimental results of grid synchronization and the current controller are presented. In addition, DC current injection is confirmed in both the designed external measurement circuit and the FFT analysis of output current.

Chapter 5 proposes a novel voltage filtering DC extraction approach for grid-connected PV inverter systems. It utilizes a combination of a passive attenuation circuit and a software filtering stage to extract the DC voltage component at the inverter output, then mitigates it via an extra DC suppression loop. The approach is validated in both simulation and experiments with increased sensitivity and accuracy. Unlike many other solutions in the literature, this method is not specific to any power converter topology.

Chapter 6 investigates an effective DC current suppression approach using a DC link current sensing technique. As no additional hardware is included, this is a high-performance, cost-effective control-based solution for minimizing DC current injection in low-power, single-phase, grid-connected PV applications.

Chapter 7 summarizes the research work carried out in this thesis, identifies the further work and makes suggestions in the area of power quality.

Chapter 2 Review of DC Suppression Approaches for Grid-Connected Transformerless Inverter Systems

2.1 Introduction

An increasing number of small-scale photovoltaic systems have been connected to the distribution network. At the heart of these low-power systems is an electronic power converter that typically injects current with a unity power factor into the grid. As the PV inverter technology is primarily driven by consideration of efficiency and reliability, new promising topologies and control methods have been implemented to facilitate less bulky, cost-effective, transformerless solutions. While the benefits of omitting the transformer are quite obvious, without the galvanic isolation there are several well understood technical and safety issues to consider. Among these issues, the risk of DC current injection flowing into the network remains a potential concern.

This chapter first describes the sources of DC current injection in transformerless PV inverters along with the potential risks for the utility network. In order to limit the DC current of an individual inverter unit, mandatory specific standards have been established in some countries, which are summarized in this chapter. As a result, much research has been conducted to suppress or compensate for DC injection. Based on their characteristics, these published solutions are categorized and then evaluated by highlighting their advantages and disadvantages. Finally, a comprehensive overview of all DC measurement techniques and suppression approaches is presented.

2.2 DC Injection Issues in Transformerless Applications

A line-frequency transformer is usually employed in grid-connected PV applications to provide galvanic isolation between the PV source and the grid. However, a bulky transformer increases the volume and cost of the whole system and reduces conversion efficiency. As stated earlier, grid-connected PV inverters are primarily driven by the efficiency, meanwhile at low power range, shrinking the size and cost are vital for distributed PV systems. In order to retain the isolation, an alternative solution can be developed by inserting a high-frequency transformer into the front stage. This establishes a less bulky system, but increases the total complexity of power processing without improving system efficiency [9, 22, 40]. Consequently, the transformerless structure has attracted

growing attention in low-power single-phase applications since omitting a transformer can lead to an extra 1-2% increase in efficiency and a 20% decrease in the volume of the whole PV system, as demonstrated in Figure 2.1 [41], in which efficiency-volume data are recorded from a database of more than 400 commercial PV inverters.

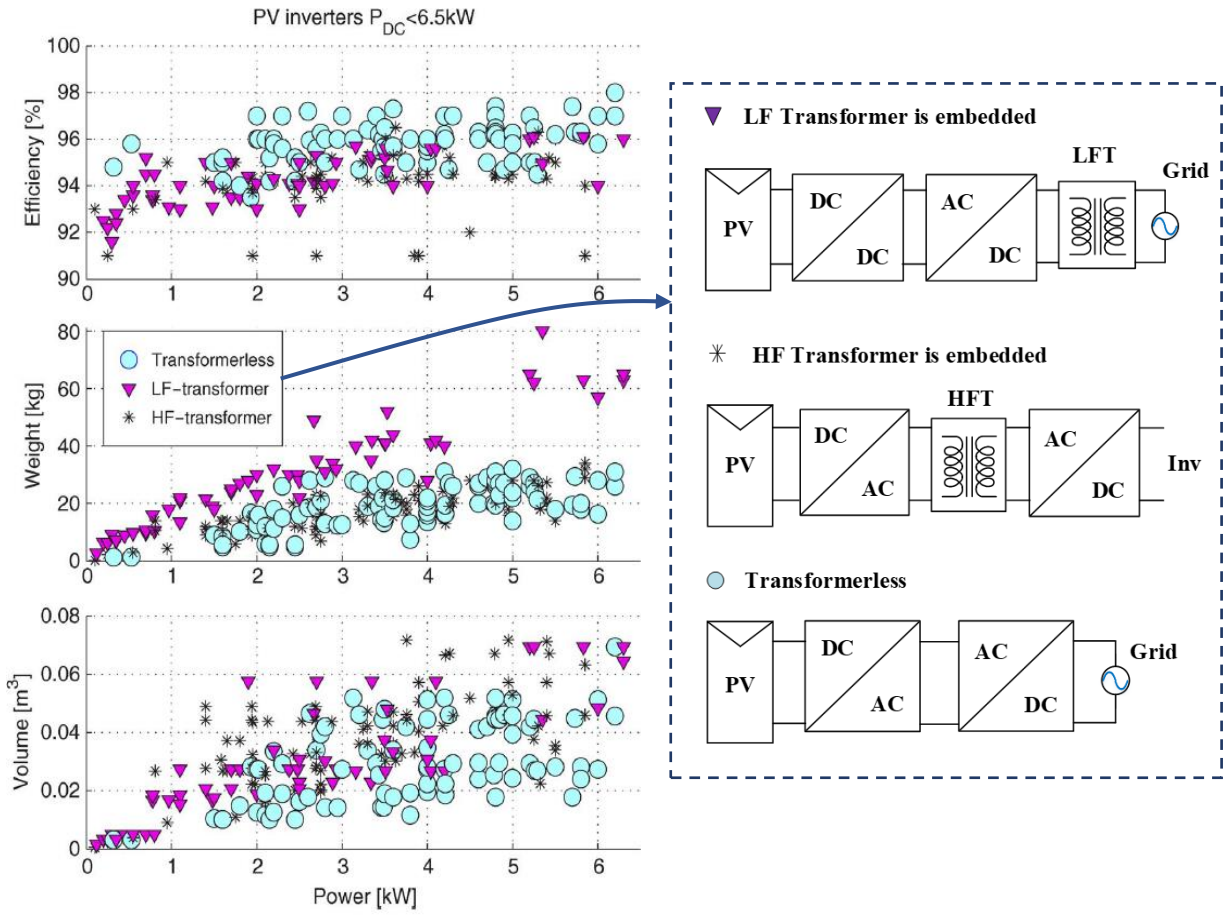


Figure 2.1 Efficiency-volume data from different PV inverter topologies [41]

Nevertheless, without galvanic isolation, the problems of ground leakage current [42-46] and DC injection arise which severely threaten the normal operation of PV systems and the grid. Many novel structures and solutions have been investigated to remove the common-mode leakage current, which solves the problems of electromagnetic interference (EMI) and safety issues brought from high-frequency resonant leakage current [43],[44],[47-52]. However, unwanted DC current injection flowing into the grid remains a significant concern [53].

2.2.1 Sources and Influences of DC Current Injection

There are numerous potential sources of DC current in the utility grid. As reported in [54], while measurements have been made for some domestic equipment or loads such as computers or lighting circuits, the accurate determination of DC injection from the distributed generators (DGs) is still a technical challenge. The first analysis of unwanted DC current from residential distributed generators was published by *Emanuel et al.* in 1984 [55]. As the transformer is universally adopted for grid-connected inverters which removes the DC current before injection to the grid, the problem is not well recognized. At the present time, whereas an increasing number of distributed PV applications have been connected to the grid, and in particular, cost-effective transformerless ones, and thus DC injection has become a major source of dc current in the utility grid.

The DC injection in PV inverter systems may arise due to the accumulation of several causes, including non-ideal semiconductor device characteristics, asymmetries in switching behaviour, imparities in gate driver circuits; small DC bias in current reference signals, quantization errors in digital systems and non-linearity and offset drift in typical Hall-effect transducers [56-58]. Whilst DC current injection from an individual inverter may be small, the accumulative effect from multiple inverter installations can severely threaten the power system in the following ways:

1) The DC component saturates distribution transformers, therefore causing a substantial increasing in the excitation current. This in turn results in additional power losses and overheat issues, and reduces transformer lifetime [55], [59].
2) DC circulation produces increasing even harmonics in parallel-connected inverters or transformer topologies connected to the same point of common-coupling [60].
3) DC current injection can potentially affect the operation of the loads that are connected to the grid; for example, causing torque ripple and extra loss in AC motors [56].
4) The DC current flowing to the earth degrades the grounding power cables over time.

2.2.2 Regulations and Guidelines

Owing to the potential risks of DC current flowing into the utility grid, mandatory specific standards are normally in place in each country to limit dc current injection from individual inverter units. Table 2.1 summarizes the maximum permitted DC injection from grid-connected inverter systems in five of the most representative countries, which are the USA, Japan, China [61], Australia, and the United Kingdom [62].

Table 2.1 Maximum DC current permitted in grid-connected inverters according to mandatory specific standards of each country

Country	***Max DC current permitted with transformer***	***Max DC current permitted without transformer***
USA	0.5% rated power inverter	0.5% rated power inverter
Japan	1% rated power inverter	1% rated power inverter
China	1% rated power inverter	1% rated power inverter
Australia	5 mA	5 mA
The United Kingdom	-	5 mA

The DC current limitations are imposed for transformerless inverters in all five countries. More specifically, Australia and the United Kingdom have absolute limits whilst other countries in the table establish percentage limits referring to the nominal power of the inverter. In addition to the mandatory national standards, DC limits are also given in general international guidelines and recommendations for all types of grid-connected inverters [63-67]. Among these standards, the most commonly adopted is the IEEE 1547 [67], (later amended in [68]), which clearly recommends that the distributed resources (DRs) shall not inject DC current greater than 0.5% of the full rated output current at the point of DR connection.

2.2.3 Classification of Suggested DC Suppression Approaches

Consequently, much research has been conducted aiming to mitigate or suppress DC current injection from an individual inverter unit. Broadly speaking, these solutions mainly fall into four categories: passive cancellation, sensor calibration techniques, active DC suppression approaches, and software solutions.

With regards to passive cancellation approaches, a series DC blocking capacitor approach is common. This is inherent in some inverter topologies; for example, in the half-bridge inverter, but often these converters are not the optimal choice. For this reason, a DC blocking capacitor must be placed between the inverter output and the point of common coupling in many preferred solutions. Whereas the grid frequency is low (50/60 Hz), such systems normally require a bulky, expensive capacitor to minimize the impact on the inverter output. On the other hand, some other studies focus on the calibration of the current sensors employed so that large controller gain can regulate

the DC current component. A typical approach proposes an auto-calibration technique to determine and compensate for the offset drift and non-linearity in the current transducer [69]. In addition to the previously mentioned approaches, other studies have investigated techniques to measure or predict the DC current values via additional hardware. These techniques are normally combined with closed-loop control schemes to compensate for the DC component, which are known as active DC suppression approaches. Last but not least several software solutions exist which their designers claim will remove the DC injection from the control without using extra hardware.

Based on the classification mentioned above, Figure 2.2 summarizes the published DC suppression approaches for the grid-connected transformerless PV inverters. In the following sections, the desired characteristics of individual DC suppression methods are evaluated, along with their advantages and limitations.

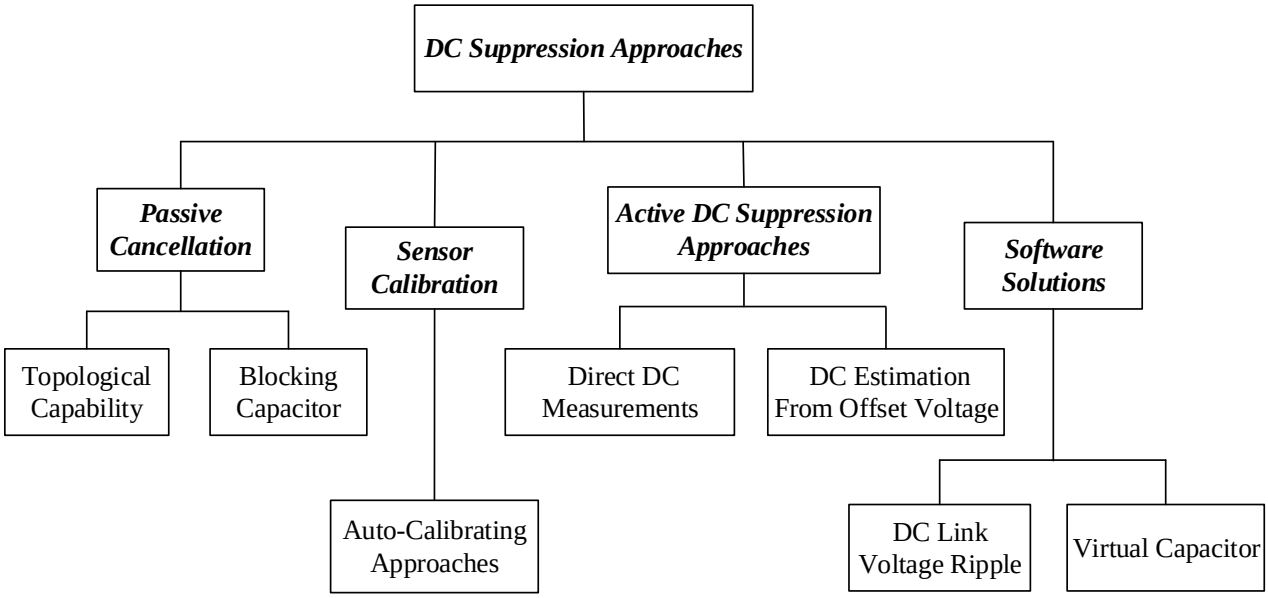


Figure 2.2 Classification of existing DC suppression methods

2.3 Passive Cancellation

Transformerless inverters with a series capacitor in the current path are intrinsically immune to the DC injection issues. However, very few such topologies exist in practice except those based on a half-bridge architecture [70-72]. As shown in Figure 2.3, one of the DC link capacitors is always conducting so that the DC current is blocked regardless of the switching state of the half-bridge inverter. Unfortunately, to reach the same rated output, the DC link voltage required for the half-bridge inverter is doubled compared with a typical H-bridge inverter. Therefore, the implementation of the half-bridge inverter is restricted by the extra component cost and switching losses.

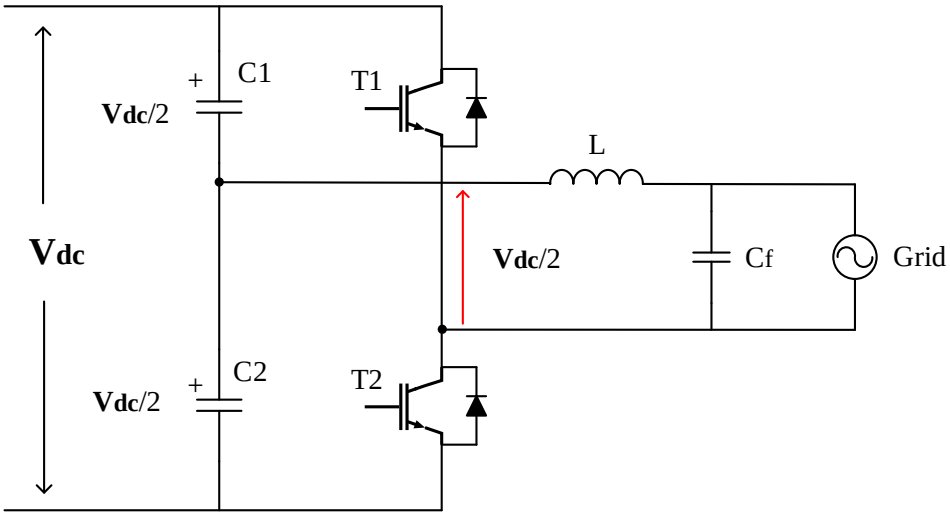


Figure 2.3 Half-bridge inverter

DC blocking capacitors are then considered being placed on the output side of the H-bridge inverter; for example, with an AC capacitor connected to the output of the common coupling point [73]. As the low grid frequency requires a large capacitance to minimize capacitive reactance, the advantage of the transformerless topology is lost by including a large and expensive ac capacitor in the current path. To improve the cost-effectiveness of the blocking capacitor, an alternative passive solution has been proposed based on an electrolytic capacitor [74], as shown in Figure 2.4.

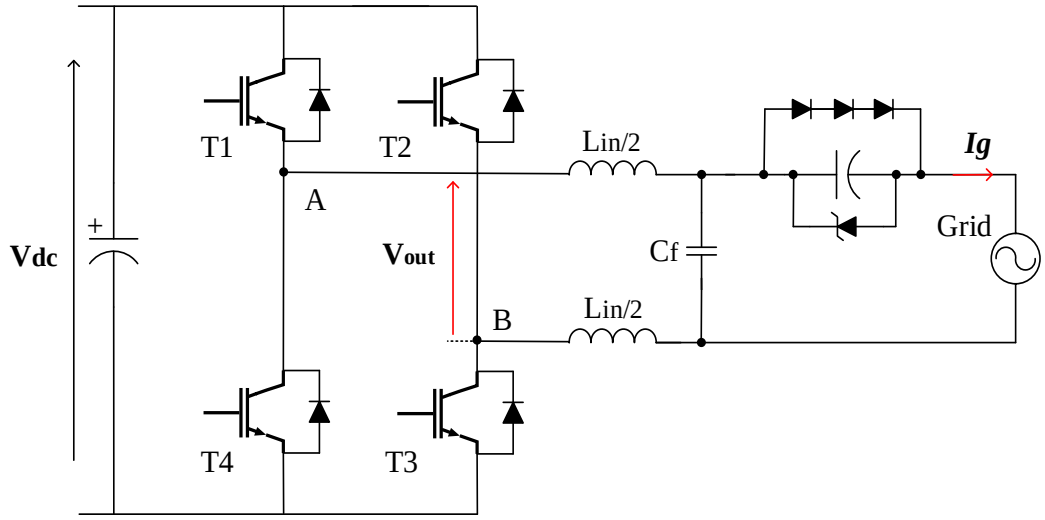


Figure 2.4 Passive cancellation based on electrolytic capacitor [74]

Polarized electrolytic capacitors are not a desirable choice given the AC output of the inverter, as the series connections are prone to the potential risks of reverse polarization and subsequent damage. However, these capacitors provide the necessary high capacitance values and voltage ratings with reduced cost and volume. For this reason, a solution has been proposed that presents a controllable DC voltage offset at the inverter output via an outer voltage loop [74]. The DC offset charges the polarized capacitor to a positive potential and cancels the AC voltage ripple, thus preventing the risks of reverse polarization. In addition, a polarity protection circuit consist of a string of p-n diodes and a Schottky diode, as shown in Figure 2.4, is parallel-clamped across the capacitor to preserve its integrity. The practical results show great DC suppression in the regulated output current, and even with artificial offset introduced the method can limit the DC injection to within 5mA.

Owing to the natural characteristics of blocking capacitors, passive cancellation is able to limit the output DC injection to within the recommended levels. However, the implementation is greatly restricted by the preferred topologies and capacitor selection. Although an alternative low-cost solution has been investigated based on the electrolytic capacitor, this still requires extra voltage measurement circuitry and carefully designed protection. Most importantly, the failure of the series blocking capacitor would shut down the whole system, therefore degrading the reliability of the inverter system.

2.4 Sensor Calibration Techniques

The Hall-effect sensor is widely used in current control applications owing to its cost-effective performance. Consuming little power, the Hall-effect sensor provides a reasonable measurement accuracy and large bandwidth with electrical isolation [75-77]. Unfortunately, this type of sensor is known to suffer from issues of linearity errors and offset drifts. As the gain of current controller at low frequency is typically large, the offset and non-linearity of the measurement chain might in particular introduce a DC component to the output current. Without adopting complicated sensing technologies, the performance of the current sensor is thus hardly improved [78]. Although there are some current sensors that can be used to detect DC current component with higher accuracy, these are not usually employed in PV applications due to cost constraints. As a result, several approaches have been discussed to actively calibrate the Hall-effect current transducer employed. Among these, a typical sensor calibration method was proposed by *Armstrong* [69]. Here, an auto-calibrating technique is presented to determine and compensate for offset drift and non-linearity in the current transducer.

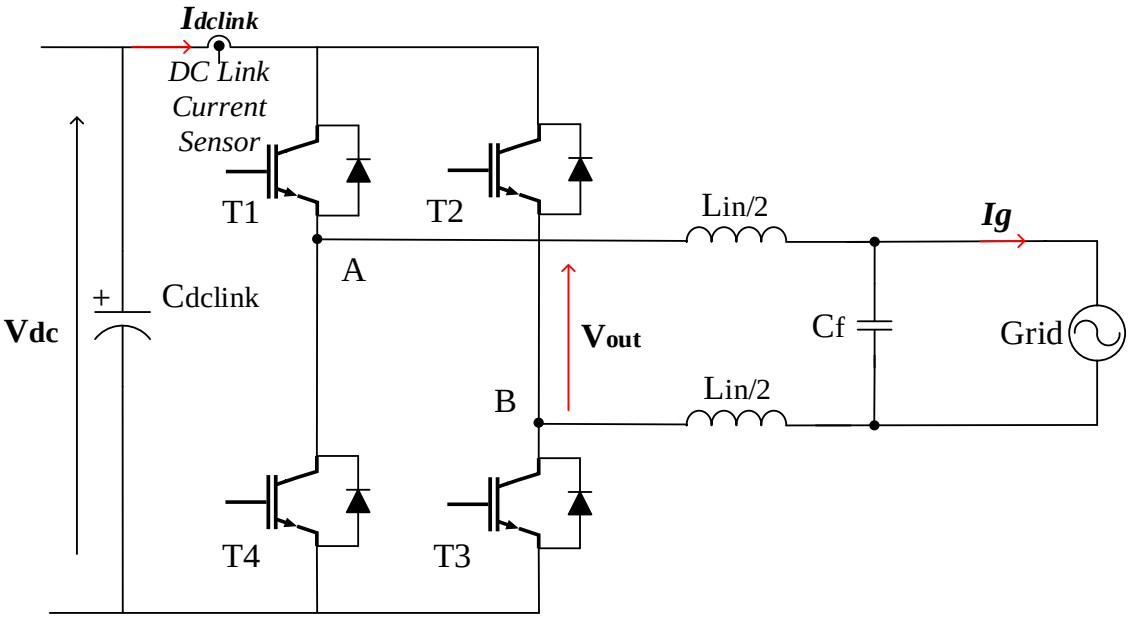


Figure 2.5 Auto-calibration of DC link sensing technique [69]

Conventionally for the H-bridge inverter, the current control loop is carried out based on the output current measurement. The offset of the current sensor adds an undefined DC error in measurement feedback; and this ultimately has an impact on DC injection. For the unipolar switched H-bridge, inverter has two working states, namely *freewheeling state* and *conducting state*. Whilst the DC

link current is either equal to or inverted to the output current during the conducting period, the inductor current simply circulates in the H-bridge during the freewheeling period, therefore leading to a zero DC link current. Whereas a zero current measurement is unlikely to be made, the actual measurement achieved during the freewheeling period is regarded as a real-time sensor offset. Consequently, through inserting a current sensor onto the DC link, the freewheeling and conducting measurements are separately determined by synchronizing the sampler at the peak and zero-crossing points of the triangular carrier, and the actual output current measurement is achieved by subtracting the freewheeling measurements from the conducting measurements.

Furthermore, if the magnitude of the inverter output current is known from the calibrated conducting measurement, the output current waveform can be fully restored using knowledge of the polarity information in the PWM index, which is therefore used for current control, and eliminating the need for the output current sensor.

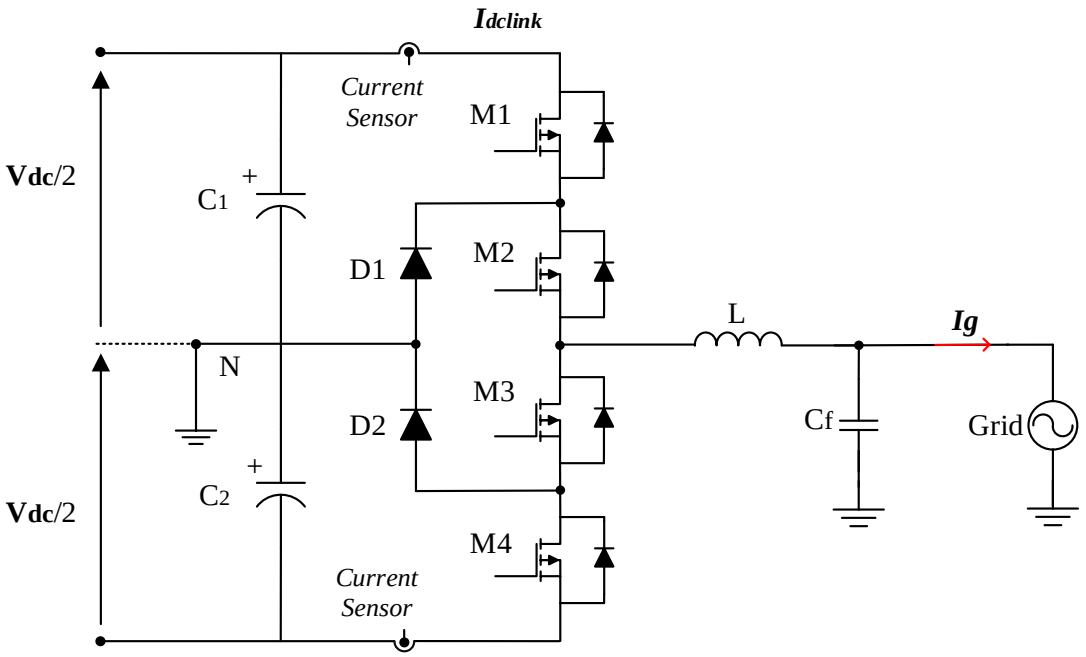


Figure 2.6 Auto-calibrating on three-level diode-clamped inverter [79]

The auto-calibrating technique largely compensates for offset errors in the Hall-effect sensor. The method is also duplicated in a three-level diode-clamped inverter, where two DC link current sensors are separately placed on the positive and negative DC buses [79]. The results of this auto-calibrating scheme show an effective suppression of the DC injection even through some artificial offset drift is produced.

However, this sensor calibration approach is limited to certain switching schemes in which a zero-state is present. The doubled sampling frequency burdens the microprocessor with increased sampling and processing complexity. In addition, the method is restricted to limited DC sources and types of current controller. As a result, more recent research has focused on active suppression methods.

2.5 Active DC Suppression Approaches

As the sinusoidal AC output is significantly larger than its contained DC injection, accurate sensing of the dc current component directly from the inverter output current remains a technical challenge. Several measurement techniques have been proposed to determine DC values via an extra measurement circuit. Then, through dedicated control algorithms, these DC determinations are used to actively regulate the system's DC injection. Based on the measurement feedback, published active DC suppression approaches mainly fall into two categories, namely direct DC current measurement and DC voltage offset measurement techniques.

2.5.1 DC Suppression Based on Direct DC Current Measurement

Several techniques dedicated to the direct measurement of small DC current have been proposed. To overcome the challenge of large AC/DC ratio in terms of accurate DC measurement, a simple magnetic circuitry composed of a magnetic core with compensation winding has been introduced [80]. Such a structure reduces the AC current flux component without influencing the DC flux. Following this, a Hall sensor is used to measure the air gap flux, which is a combination of DC flux and residual AC flux. However, performance greatly relies on the compensation winding, and the DC current evaluation from combined flux measurement remains a tricky issue.

Alternatively, a more recent direct DC current measurement approach has been proposed by *Abdelhakim* [81], which utilizes a coupled inductor combining with a small-range current sensor. Figure 2.7 shows the equivalent operational circuit of the proposed scheme, where a 1:1 couple inductor with a short-circuited secondary winding is employed after the LCL filter. The primary current I_p is the inverter output current which comprises AC and DC components, whilst the secondary current I_s is purely AC current. Through taking both windings through a small-range

current sensor, the AC current component will be cancelled out and only the DC current is measured.

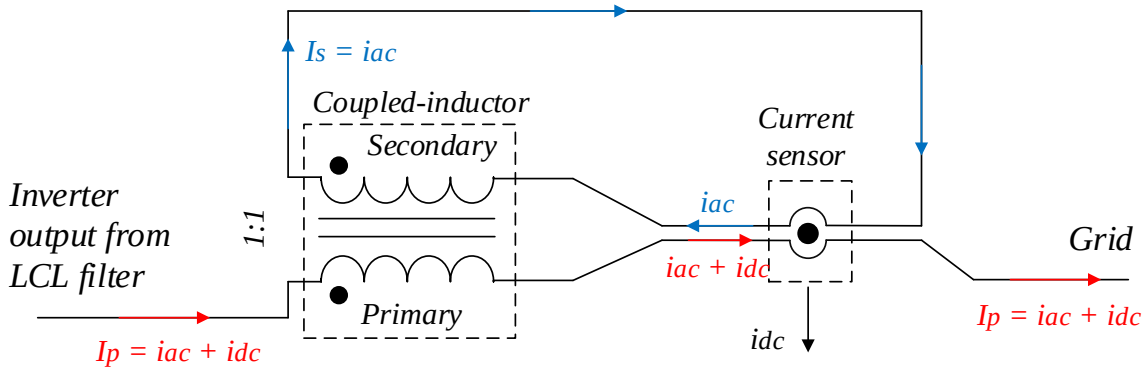


Figure 2.7 Direct DC current measurement technique [81]

Through cooperatively working with the control scheme, the published results in [81] show an effective reduction of DC current from 60mA to 2mA in a 5-kVA three-phase grid-tied system. However, in order to achieve the highest possible performance, the technique requires a well-calibrated high-accuracy sensor with carefully designed coupled-inductors, which adds extra cost and complexity to the system. For this reason, several other techniques have considered the DC current estimation via the detection of the DC voltage offset in the system.

2.5.2 DC Suppression Based on Indirect DC Current Estimations

Due to the parasitic resistance of output filters and the resistive part of grid impedance, there is always a DC voltage component present in PV inverter output in the case of DC current injection. Most indirect measurement techniques rely on measuring this DC voltage, which can then be used to compensate for the DC current with dedicated control schemes. This type of approach was first introduced by *Sharma* [82], where a small 1:1 voltage transformer and an RC circuit were utilized to detect the DC voltage. While the complete removal of AC voltage is unlikely to be achieved considering the phase shift between grid voltage and inverter output, the accurate DC voltage measurement is difficult. Further improvements were achieved by *Ahfock* and *Bowetell* [83], who replaced the small voltage transformer with a 1:1 mutually coupled inductor pair, but here the major concerns were the expensive and bulky inductors and additional power losses. As a result, *Ahfock* and *Bowetell* [84], subsequently propose a double-stage RC circuit solution that is connected across the ripple filter rather than the AC terminals, as shown in Figure 2.8. Owing to the action of the

double-stage RC filter, the output DC offset V_0, contains a relatively low level of AC. This output is then fed into a PI controller with a zero-reference input to regulate the DC current component into an acceptable level. However, except for the inevitable time-delay, where a very low cut-off frequency is required to filter out the acceptable DC voltage, the problem of common-mode voltage needs to be taken into consideration.

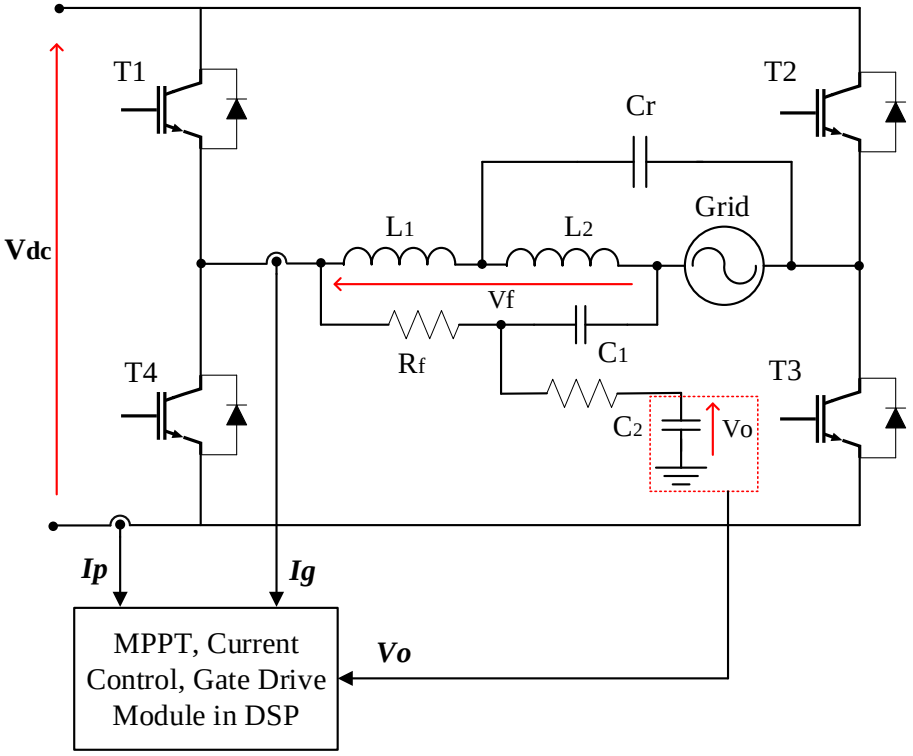


Figure 2.8 Ripple filter offset sensing based on double-stage RC circuit [85]

A double-stage RC filter solution has been employed by connecting an amplifying circuit [85]. This can effectively resolve the common-mode voltage problem, but there is no marked improvement in the time-delay, and the hardware amplification might introduce additional offset and noise.

Alternatively, He and Xu [86] proposed a DC suppression loop in which the DC voltage offset is measured and suppressed at the inverter output through a DC compensation loop, as shown in Figure 2.9. The high-precision differential amplifier presents a high common-mode rejection ratio (CMRR) that accurately detects the inverter output voltage without any measurement offset, whilst the use of a high-order low-pass filter should remove the AC component, achieving high-accuracy DC measurement. The DC suppression is carried out by a feedforward control of compensation

current I_{com} in the current control loop. However, accurate DC extraction cannot be guaranteed owing to the vast difference in magnitude between the DC offset voltage and the fundamental AC voltage. Furthermore, the attenuation of the differential amplifier circuit makes the tiny DC signal challenging to deal with.

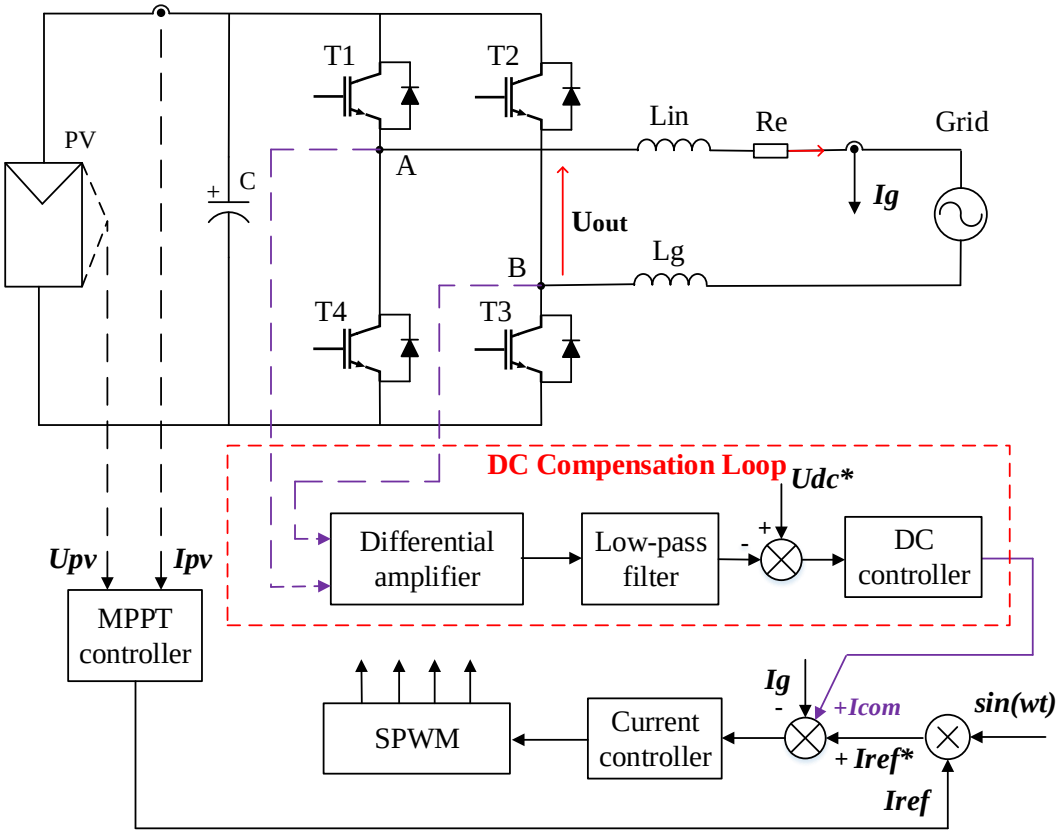


Figure 2.9 DC voltage extraction using differential-amplifier and low-pass filter [86]

In addition to the previously mentioned approaches, other state-of-the-art solutions have been investigated [87-91], based on a non-linear reactor with dedicated control algorithms. It is worth noting that such a technique was first introduced by *Buticchi* for a full-bridge topology [87] as shown in Figure 2.10.

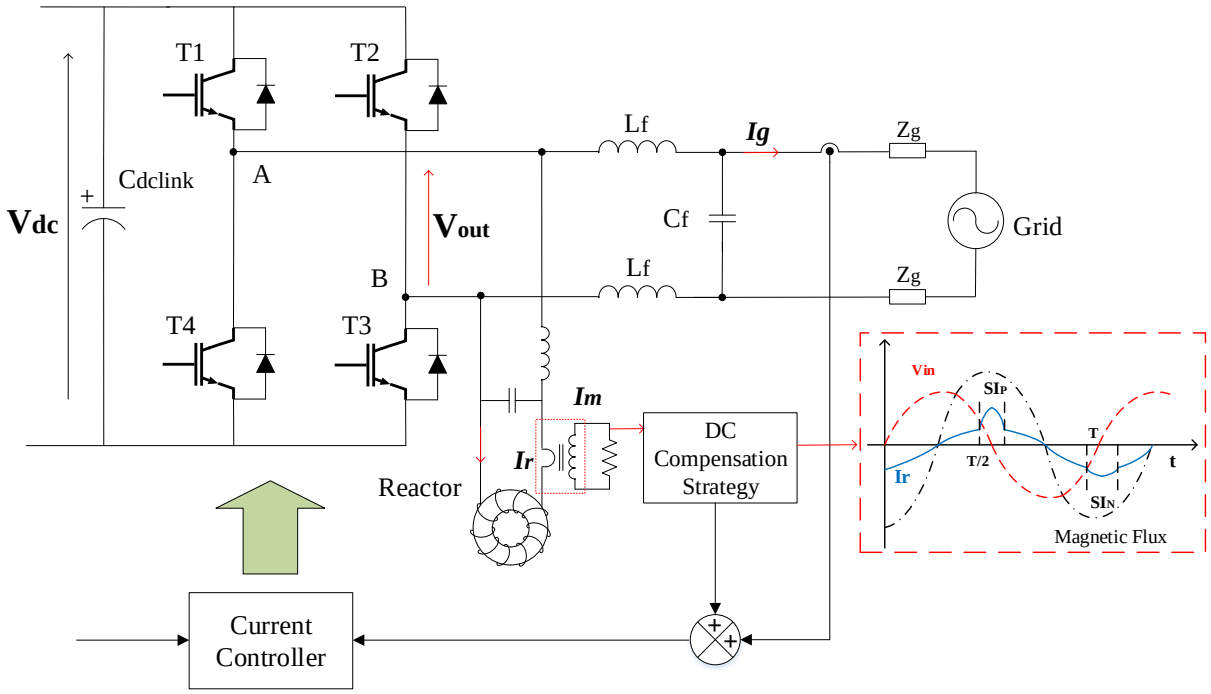


Figure 2.10 System diagram of non-linear reactor solution [87]

This approach aims to compensate for the DC voltage component at the inverter output, and therefore a saturable magnetic circuit is developed consisting of a single winding on a toroidal magnetic core. This magnetic circuit is referred to as a reactor, which is designed to operate at the knee point of the magnetizing characteristic and used to sense the DC voltage at the inverter output. For the purpose of rejecting high-frequency harmonics, the reactor is fed from the inverter output voltage with an LC filter. Meanwhile, a current transformer is utilized to sense the reactor current, as shown in Figure 2.10. The principle of the DC voltage sensing operation is based on the non-linear behavior of the reactor, whose magnetic flux saturates asymmetrically when a sinusoidal input voltage with DC bias voltage is applied. This effectively leads to a noticeable distortion in reactor current at a voltage zero-crossing point. Conversely, the absence of an asymmetrical reactor current distortion indicates that the inverter output is free from the DC voltage offset. Thus, in order to compensate for the DC voltage bias, dedicated closed-loop control is developed by detecting the asymmetrical distortion using two indices, namely the positive saturation index SI_P and the negative saturation index SI_N. Each index is first computed by integrating the reactor current in a small window in the saturation region, which is then regulated by a PI controller with $SI_P + SI_N$ as input. When $SI_P + SI_N = 0$, no asymmetrical current distortion is present and, as a consequence, no DC current injection exists in the inverter system.

This solution has several advantages over prior measurement techniques, including, higher accuracy and sensitivity. This is due to the non-linear magnetic characteristic of the reactor, which guarantees high sensitivity even with low DC voltage value at the inverter output. Through a dedicated control algorithm, effective compensation for the DC injection in the H-bridge inverter is provided. In addition, the technique has been employed to remove the DC component in a distribution transformer [88] and in power lines [89]. However, it is noted elsewhere [90] that the time sampling makes the method susceptible to offset in the signal-processing chain, whilst the use of the LC filter reduces the amplitude of the reactor current. For these reasons, new spectral DC detection algorithms were proposed to achieve better performance [90], [91].

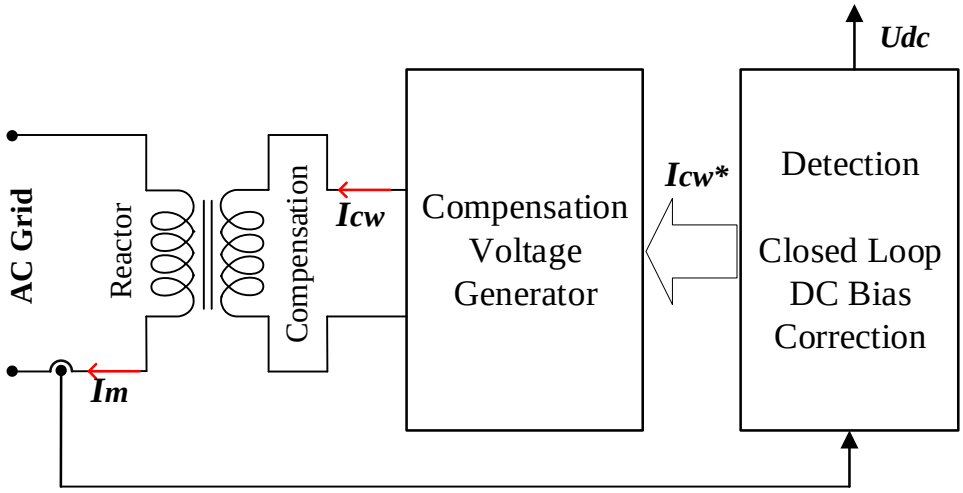


Figure 2.11 DC bias correction based on the spectral content of the reactor current [90]

As described in Figure 2.11, these techniques were developed based on a non-linear parallel-connected reactor, but the LC filter is effectively removed. By identifying the relationship between the amplitudes of even harmonics and the DC bias voltage U_{dc}, the DC bias measurement can be determined from the demodulation process of the reactor current I_m. Furthermore, a closed-loop DC bias correction system is introduced to calculate the reference current I_{cw}^*, and this is then applied to the compensation winding via a compensation voltage generator.

Compared to the previous measurement techniques [87], the removal of the LC filter produces a larger reactor current, thus increasing sensitivity, whilst the spectral demodulation process contributes to robustness against the offset in the signal-processing chain. However, this approach is not suitable for grid-connected inverter applications given the low values of parasitic resistance. Accuracy cannot be guaranteed since the calculated ratio of the reactor current harmonics to the

DC injection $I_{harmonics}/I_{dc}$ is very low. The value of I_2/I_{dc} is around 0.1 based on data published [90]. Moreover, the non-linear reactor must be designed carefully for specific system, which potentially increases the complexity and costs.

2.6 Software Solutions

As opposed to the aforementioned measurement techniques, software solutions aim to obtain DC values from existing measurement feedback, therefore eliminating the need for extra hardware. Several techniques have been investigated in the literature which claim to measure or mitigate DC injection in an effective way. *Wang et al.*[92] proposes a real-time DC current measurement technique using the double integration of the output current. Following this, Guo *et al.*[93] used the output to build another feedback loop to compensate for DC current injection. From a control perspective, this feedback loop acts in the same manner as having a series blocking capacitor, as shown in Figure 2.12. As the system does not employ a real blocking capacitor, this technique is referred to as the virtual capacitor method and has been investigated in several schemes [56, 93-95].

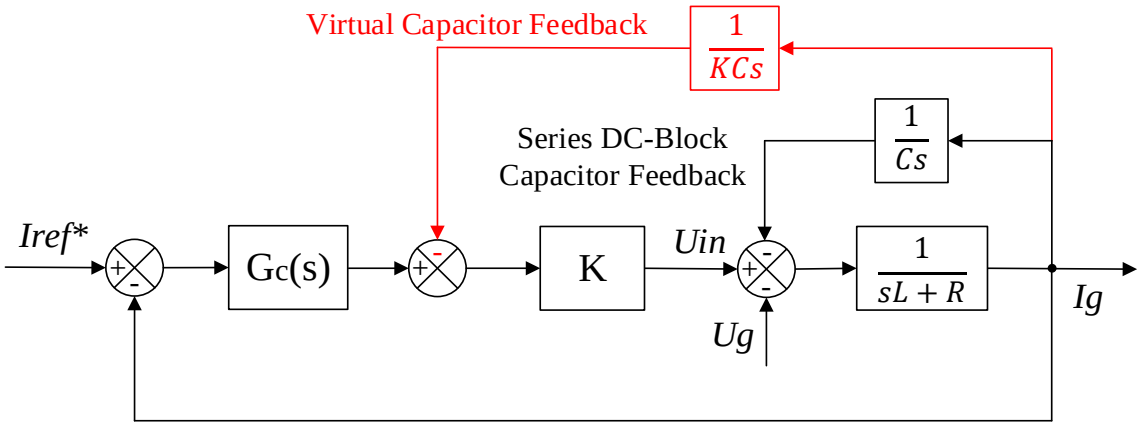


Figure 2.12 Control model of grid-connected inverter with DC-block/virtual capacitor

However, a major concern with the virtual capacitor approach is the accuracy of the current sensing circuit. In other words, if the sensors drift or the DC injection is not correctly sensed, which is normally the case, this output feedback control is likely to fail.

For this reason, by identifying the amplification of DC injection in the DC link line-frequency ripple, an indirect DC estimation method has been introduced based on the software extraction of the DC link line-frequency voltage [96]. As the voltage of the DC link capacitor has already been

sensed in the inverter system, no extra hardware is needed. However, owing to the minimal line-frequency voltage ripple (at millivolts scale) on the DC link capacitor, the accurate measurement of this ripple component from a much larger voltage level is unlikely to be achieved, therefore resulting in degraded DC mitigation performance.

2.7 Comparison of Suppression Methods

Based on the previously stated advantages and disadvantages of each approach, Table 2.2 presents a comparative overview of published DC measurement techniques and suppression approaches.

Table 2.2 Overview of published DC measurement and suppression approaches

DC Suppression Technique	Advantages	Disadvantages
Passive Cancellation		
Half-bridge topology	Intrinsically free of DC injection	Extra component cost and switching losses.
Series DC blocking capacitor	Low-cost, effective DC suppression	Degraded reliability of the inverter system.
Sensor Calibration		
Auto-calibrating technique for DC link current sensor	Actively compensates for sensor offset and non-linearity issues.	Requires a doubled sample frequency, only valid for limited switching schemes.
Software Solutions		
Virtual capacitor using integration of output current	No extra hardware, easy to implement.	Only valid when the current sensing circuit is perfect.
DC estimation from DC link Line-frequency voltage ripple	No extra hardware, robust against DC offset in current sensors.	Degraded performance owing to the minimal line-frequency voltage ripple
Active DC Suppression Techniques		
DC bias current measurement based on a magnetic circuitry	Compensates for AC flux, results in a smaller AC/DC ratio.	Greatly relies on the compensation winding

Direct DC current measurement using coupled inductor sensor circuit	Provides direct DC current measurement.	Requires extra sensor set with carefully designed coupled inductors.
DC voltage measurement using simple 1:1 coupled inductor and RC circuit	Compensate for AC voltage in the measurement output.	Bulky and expensive, extra power losses.
DC voltage measurement using Double-stage RC circuit	Relatively low level of AC voltage remaining	Common-mode voltage issues with inevitable time-delay.
DC voltage measurement using differential amplifier and LPF	Robust against measurement offset and common-mode voltage issues.	Remaining challenge to deal with the output signals of a differential amplifier.
DC suppression based on nonlinear reactor solution	Increased sensitivity owing to the non-linear behaviour of the reactor, real-time DC voltage measurement.	Dedicated design of reactor circuit and strict operating condition, also requires for complicated control schemes.

2.8 Summary

This chapter reviews the DC injection issue in transformerless grid-connected PV inverters. In the first part of the chapter, the sources of DC current and its influence on the power system are discussed. In order to limit the DC injection of an individual inverter unit, international guidelines and recommendations have been established, which are summarized in Table 2.1. As a result, many DC suppression approaches have been proposed to regulate DC current injection within the strict limits of the standards.

The second part of the chapter evaluates published DC suppression approaches in the following categories: passive cancellation, sensor calibration techniques, active DC suppression approaches, and software solutions. While passive cancellation offers effective DC suppression performance, there are practical implementation issues due to the constraints of cost, reliability and efficiency. The sensor calibration techniques compensate for the sensor offset and non-linearity. However, they require a doubled sampling frequency, and the method is only effective for limited modulation schemes. The active DC suppression methods normally require additional hardware, yet the accuracy is quite limited. With regards to software solutions which claim to compensate for any DC injection without using extra hardware, they are only valid when the measurement feedback is perfect.

In summary, as mainstream literature continues to show, DC component mitigation is a challenging problem in grid-connected inverter applications. For this reason, the motivation of the research is to investigate cost-effective mitigation methods for DC current injection, thus facilitating the development of grid-connected power converter and improving grid operating condition. Two novel schemes have been proposed in this thesis to tackle the DC injection issue. Chapter 5 introduces a two-stage DC voltage detection technique which utilities an RC filter attenuation circuit and a software DC-component extraction algorithm. This combination facilitates very accurate DC component extraction with minimal hardware requirements. Unlike many solutions, it is not generally dependent on the power electronic converter topology. Hence, it is a desirable solution for DC current compensation in most grid-connected inverter systems. Chapter 6 introduces a DC suppression method for grid-connected H-bridge inverters based on DC link current measurements. The DC current is extracted from the DC link current waveform and suppressed via an active control loop. Furthermore, fundamental AC current control is simultaneously implemented using the same DC link current measurement, thus eliminating the need for a conventional output current sensor. The DC link sensing technique is recognized as a cost-effective software-based solution for H-bridge inverter which robustly injects high-quality AC current to the network with real-time DC current rejection. Both schemes present a positive contribution in the area of the power quality control of grid-connected transformerless inverter systems.

Chapter 3 Model and Operation of Transformerless H-bridge Grid-Connected PV Inverter

3.1 Introduction

Current control and grid synchronization are the main control functions in the grid-connected PV inverter system which guarantee a high-quality, synchronized, sinusoidal output current to the grid. These functions are typically carried out based on the measurements of injected current and grid voltage, and are capable of handling variation in power and controlling current injection according to specific requirements such as limited THD, and demand as in reactive power compensation [97],[98]. Whereas the control structure and filter selection vary according to the diversity of inverter topologies, the appropriate set-up of the inverter system guarantees efficient and robust interconnection between the PV panels and the electrical power system [99],[13]. Figure 3.1 shows the general structure of a single-phase, grid-connected transformerless PV inverter system.

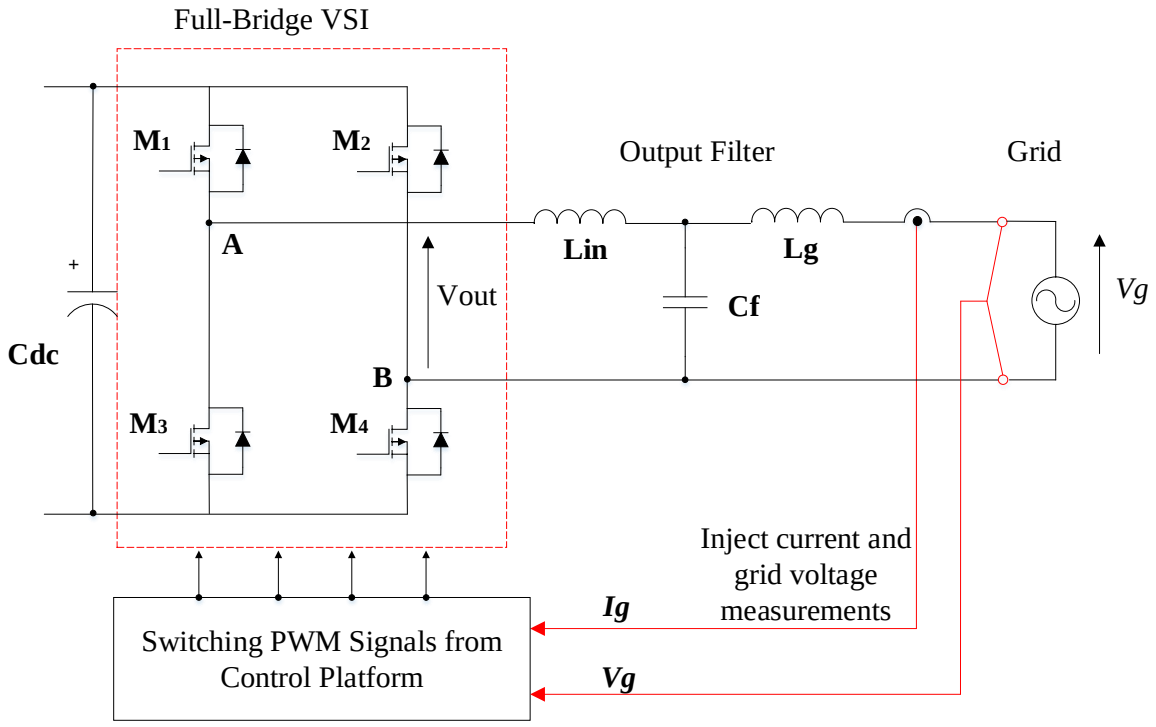


Figure 3.1 Single-phase grid-connected transformerless H-bridge inverter

This chapter describes the operation of the grid-connected H-bridge transformerless inverter. In such a system, the fast and accurate detection of utility voltage and current information is important, since it is used in generating the reference signals. Therefore, the first part of the chapter focuses on grid synchronization issues with the use of phase-locked loop (PLL) techniques. Due to the nature of the single-phase system, the advantages associated with power PLL (pPLL) are discussed, and a modified pPLL is implemented to obtain the grid frequency and phase. The second part of the chapter presents an analysis of the key components in the current control loop, where the proportional-resonance (PR) controller and *LCL* filter are chosen owing to the advantages given in improving the power quality of the injected current. Then, a mathematical model of the inverter system is developed from the given transfer functions of the controller, delay effect, PWM gain and filter, which allows the stability analysis and operational optimization with respect to the gain parameters of the PR controller to be implemented. Following this, a grid-connected inverter with *LCL* filter is simulated in Simulink/MATLAB. By operating the simulation with different controllers, the results verify the improvement in harmonic performance from the PR controller.

Finally, DC injection is observed in the output current measurements, which are sourced from the operation of the asymmetrical inverter and sensing offset. Although the numerical quantification of DC injection from each individual source has not been fully studied, the existence of DC injection is confirmed from the simulation when the inverter is working at non-ideal conditions. Consequently, DC suppression techniques are implemented to demonstrate the proposed concept and its effectiveness in protecting the integrity of distribution network and the grid operation.

3.2 Grid Synchronization

Synchronization with the utility grid is one of the most important aspects of grid-connected inverter systems. Accurate phase and frequency information of the AC-mains should be detected in real time in order to generate the current reference and frequency-adaptive control [100-103] . Initially, for a grid-connected power converter system, the zero-crossing detection (ZCD) technique is used as a simple synchronization method which estimates the frequency by identifying the zero-crossing point of the grid voltage. Following this, the phase angle is obtained from the integration of the estimated frequency. However, as the frequency and phase are updated at the polarity-changing point, the accuracy of detection could potentially be affected by distorted grid voltage. Even by adopting some modifications to the method, the performance is not satisfactory when the grid is

affected by low-frequency harmonics and frequency variations [103-105]. Accordingly, the advanced phase-locked loop (PLL) techniques are investigated for modern synchronous control systems.

The PLL is a closed-loop feedback system that synchronizes the output frequencies with its input signals [99, 106]. It consists of three main elements, namely: a phase detector (PD), loop filter (LF) and voltage-controlled oscillator (VCO). Despite differences in the implementation of each element, the basic PLL structure is shown in Figure 3.2 [107-109].

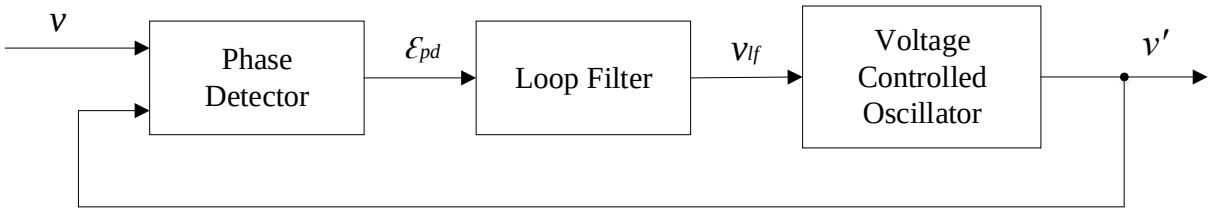


Figure 3.2 Basic PLL structure

All PLL techniques follow this basic structure, and the difference mainly appears in the various implementation methods of the PD. Typically, for single-phase grid synchronization, power-based and transformation-based PDs are the most commonly used techniques, and the corresponding PLL algorithms are referred to as the power-based PLL (pPLL) and synchronous reference frame PLL (SRF-PLL) [100],[103],[110],[111].

3.2.1 The Structure of PLL Techniques

Figure 3.3 shows the control diagram of a standard power-based PLL where the PD is implemented with a sinusoidal multiplier and a low-pass filter. The LF and VCO are separately implemented based on a PI controller and an integrator.

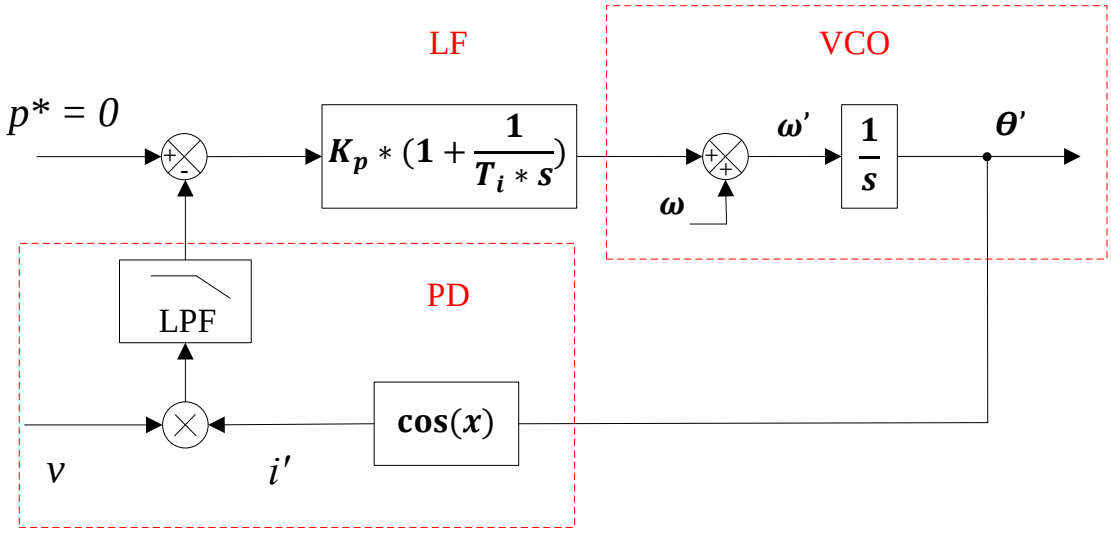


Figure 3.3 Control diagram of power PLL

The operation of the PD block is effectively an emulation of the active power calculation process. Zero output from the PD block denotes a quadrature relationship between the grid voltage v and fictitious current i', and in this case the estimated angle θ' equals the grid angle θ.

From Figure 3.3, the calculation of fictitious power p is given as:

$$p = v * i' = V \sin\theta \cos\theta' \tag{3.1}$$

By applying the product to sum trigonometric identity, Equation (3.1) can be written as,

$$p = \frac{V}{2}\sin(\theta - \theta') + \frac{V}{2}\sin(\theta + \theta') \tag{3.2}$$

Considering $\theta = \omega t + \emptyset, \theta' = \omega' t + \emptyset'$ and assuming $\omega = \omega'$, for a phase difference of φ, the fictitious power can be expressed as

$$p = \frac{V}{2}\sin(\varphi) + \frac{V}{2}\sin(2\omega' + \varphi) \tag{3.3}$$

From Equations (3.2) and (3.3), it can be seen that the information of phase difference is contained in the DC term. Therefore, a low-pass filter is typically used to filter out the undesired double-frequency harmonics. The remaining PD error is then tuned to zero via the LF and VCO, and the phase and frequency information from the PLL is synchronized to the input signal.

Even though some design precautions are taken into consideration, the low-pass filter can hardly achieve a good balance between the harmonic attenuation and dynamic performance. Some improvements in the pPLL have been investigated, such as an adaptive notch filter solution. However, most of the suggested solutions have issues of cost-effectiveness in implementation [100],[107],[109].

A recent pPLL technique, the modified mixer PD (MMPD), was proposed by Thacker *et al.* [110], where the double frequency harmonic is removed via subtracting a sinusoidal product term from the fictitious power. This technique shows a great improvement over the conventional pPLL and its structure is shown below.

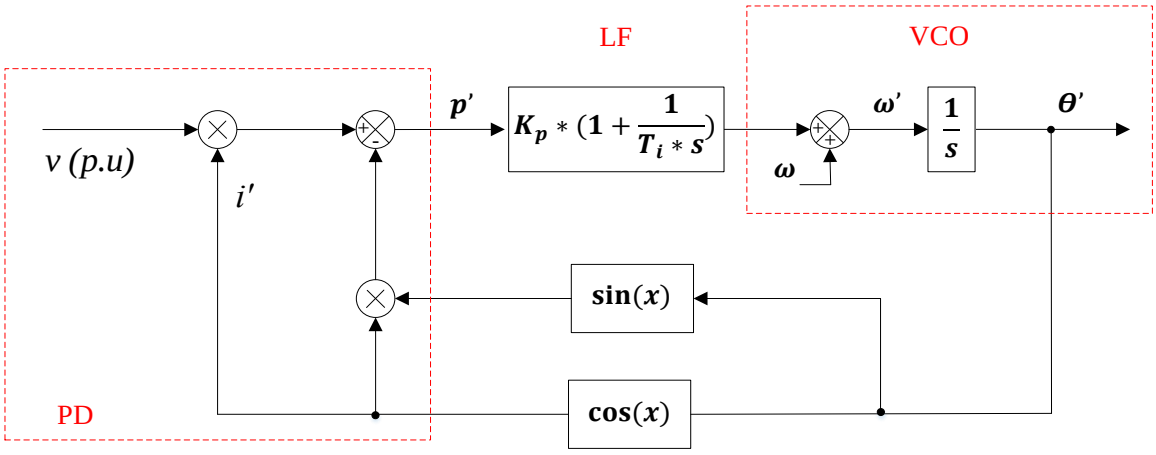


Figure 3.4 Control diagram of MMPD-based pPLL

From Figure 3.4, the fictitious power p' fed into the LF can be written as:

$$p' = V \sin\theta \cos\theta' - \sin\theta' \cos\theta' \tag{3.4}$$

Similarly, giving the difference between the estimated angle $\theta'$and grid phase θ as φ yields:

$$p' = V \sin(\theta' + \varphi) \cos\theta' - \sin\theta' \cos\theta' \tag{3.5}$$

By applying the trigonometric formula, the power error can be derived as a function of grid voltage amplitude V, estimated angle θ' and the phase difference φ, as:

$$p' = \frac{V \sin\varphi}{2} + \sin(2\theta' + \tan^{-1}(\frac{V \sin\varphi}{V\cos\varphi - 1})) \sqrt{\frac{V^2 + 1}{4} - \frac{V}{2}\cos\varphi} \tag{3.6}$$

Assuming that a unity voltage input ($V = 1$) is given, the power error can be simplified as,

$$p' = \frac{\sin\varphi}{2} + \sin(2\theta' + \tan^{-1}(\frac{\sin\varphi}{\cos\varphi - 1}))\sin\frac{\varphi}{2}$$

(3.7)

Here a zero phase difference ($\varphi = 0$) leads to a zero power error ($e_p = 0$). Although a significant ripple reduction can be observed from equation (3.7), the performance of the MMPD technique relies on the unity amplitude of the input voltage. This is realized via the peak voltage tracking system at the input of the PLL. Fortunately, as given in [110], the non-unity voltage input between 0.9 to 1.1 still offers a minimum ripple reduction of 86.4% over the standard pPLL. Consequently, owing to the improved dynamic performance and ripple reduction capability, the MMPD technique is implemented throughout the following simulation and in the experimental inverter systems.

It is worth mentioning that some transformer-based PLL solutions have already been suggested [103], [112]. Their general control diagram is shown in Figure 3.5. As the Park transformation requires a set of orthogonal signals, the relevant orthogonal signal generation (OSG) techniques (T/4 Time-delay, Hilbert Transform, etc.) have to be applied for single-phase VSI [103], which relatively increases the complexity of the PLL structure. Additionally, owing to the presence of an OSG block, these SRF-PLL techniques are more sensitive to variations in grid frequency [107].

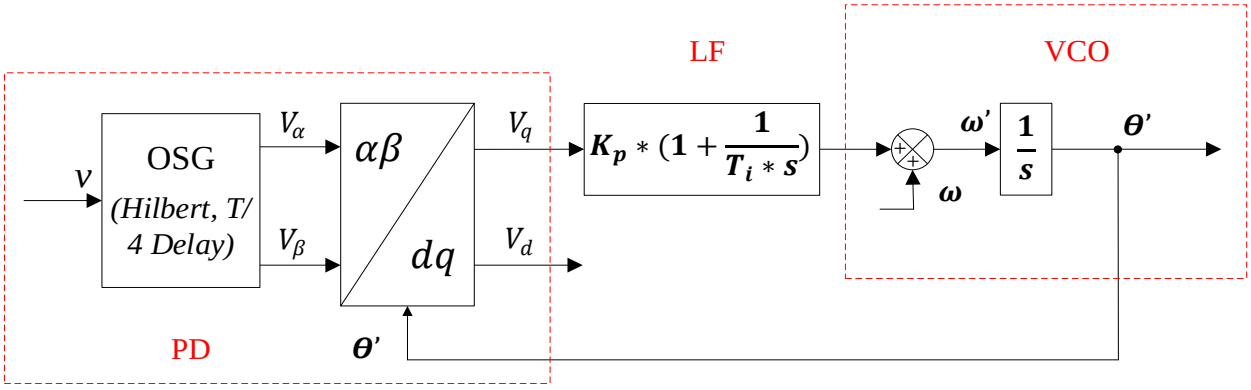


Figure 3.5 General control diagram of OSG-based SRF-PLL techniques

3.2.2 Simulation Performance of Grid Synchronization

The simulation model of the MMPD-based pPLL has been developed, and the results are shown in Figure 3.6. For an idealized grid voltage V_g, the steady-state estimated phase angle θ from the PLL is shown in Figure 3.6(b). From this, a sinusoidal unity voltage v' is constructed in Figure 3.6(c), which is in-phase with the grid voltage. The results in Figure 3.6 shows the accurate performance of grid synchronization in the steady-state.

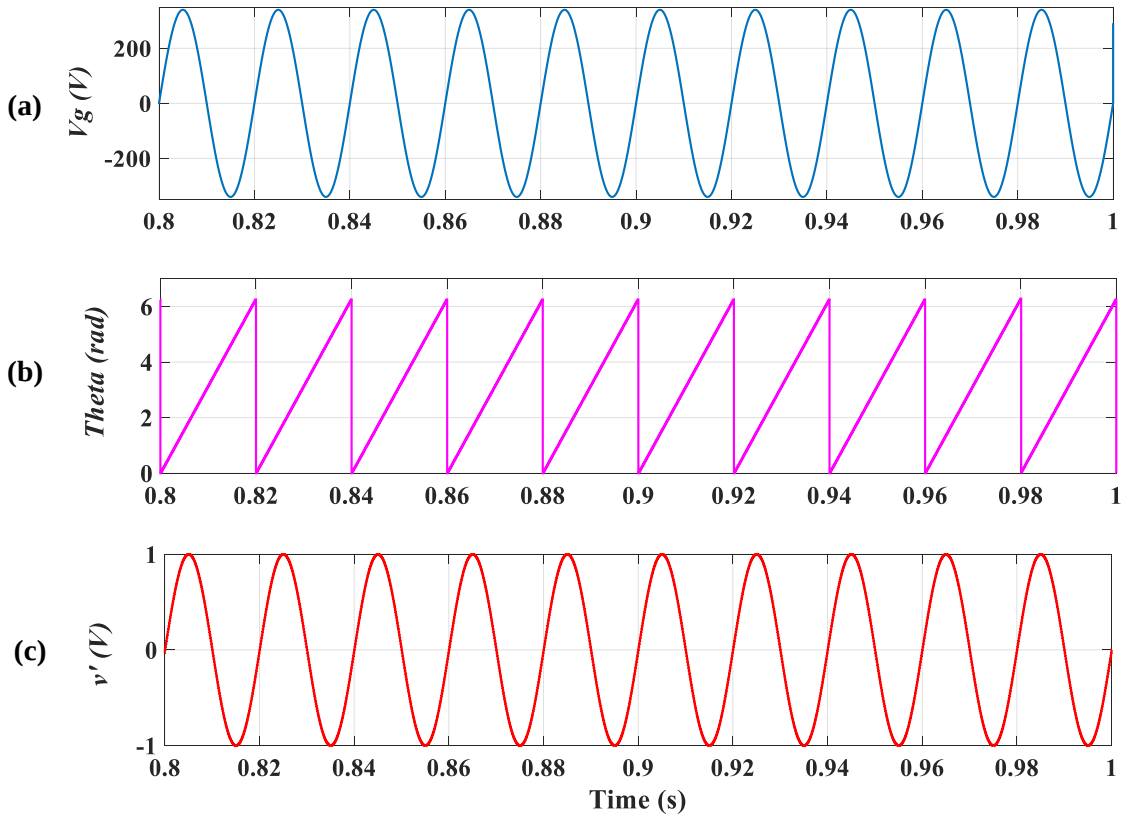


Figure 3.6 Steady-state performance of MMPD-based pPLL

To investigate the dynamic performance of the MMPD-based pPLL, step-changes in frequency (2Hz) and phase (45°) are applied at 1s to the grid voltage. Figure 3.7 shows the frequency output and fictitious power error separately. For comparison purposes, a standard pPLL is constructed in the simulation, where the cut-off frequency of the low-pass filter is selected to be 5Hz. With the same voltage input, the results of the standard pPLL are presented in Figure 3.7 in blue.

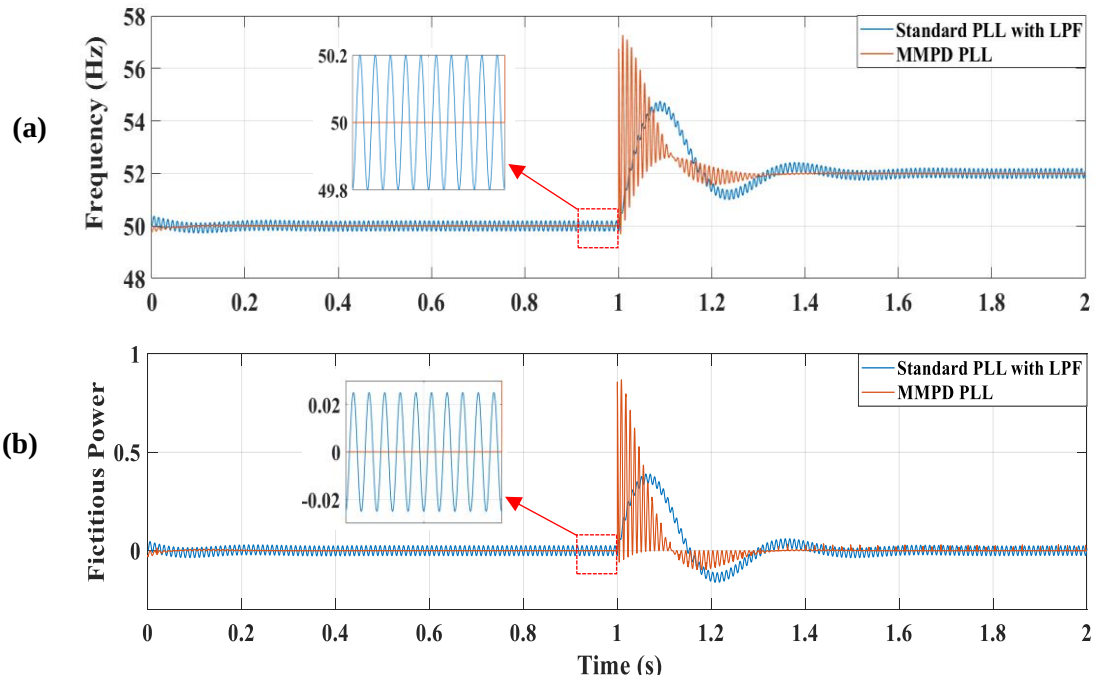


Figure 3.7 Comparison of performance between MMPD-based pPLL and standard pPLL

As shown in Figure 3.7, with a step-change at the time of 1 s, a faster response of the MMPD-based pPLL is observed in both frequency estimation (Figure 3.7 (a)) and fictitious power error (Figure 3.7 (b)). Most importantly, by subtracting the product term from the fictitious power, the double harmonic is entirely removed in the steady-state operation. On the other hand, although the low-pass filter in the standard pPLL reduces the transient overshoot and high-frequency oscillations, without having a very low cut-off frequency, it is unlikely to achieve similar performance as in MMPD PLL. From the zoomed steady-state operation section in the inset in Figure 3.7(a), the estimated frequency is confirmed as 50Hz from the MMPD-based pPLL for the 50Hz grid, whilst an oscillation of $\pm$0.2Hz is observed from the standard pPLL. A similar set of results can also be observed in Figure 3.7(b), where the fictitious power from the standard pPLL oscillates between $\pm$0.025.

The simulations are carried out in the ideal case and the input of the PLL models is a purely sinusoidal grid voltage. This rarely exists in practice, although normal grid operation would not deviate too far. From the simulation results, the advantages of fast response and robust steady-state operation in the MMPD-based pPLL are demonstrated.

3.3 Modelling and Design of the Current Control Loop

The power quality of output current is considered to be one of the most important issues for the voltage source inverter (VSI), and therefore feedback-based current control methods have been intensively investigated [113]. Due to the constraints in design and dynamic performance, implementations of boundary control methods and synchronous frame controllers are limited to certain applications [114-116]. For the single-phase VSI, the proportional-integral (PI) with distinct pulse-width modulation (PWM) has been widely adopted owing to their simplicity and cost-effective performance. To improve the ability to track the sinusoidal reference, some studies have replaced the integral term of the PI controller with a resonance term, and this is known as a proportional-resonant (PR) controller [116-118].

The control diagram of the PI/PR-based current control loop is shown in Figure 3.8, where the $G_c(s)$ and K_{pwm} separately represent the controller and PWM gain, $G_d(s)$ is defined as the time delay introduced to the digital implementation, and $G_f(s)$ stands for the output filter. By introducing the mathematical representations of the controller and modulation schemes, the current control loop based on the PI and PR controller is separately modelled and compared. Following this, the performance of the feedback-based current control method is discussed.

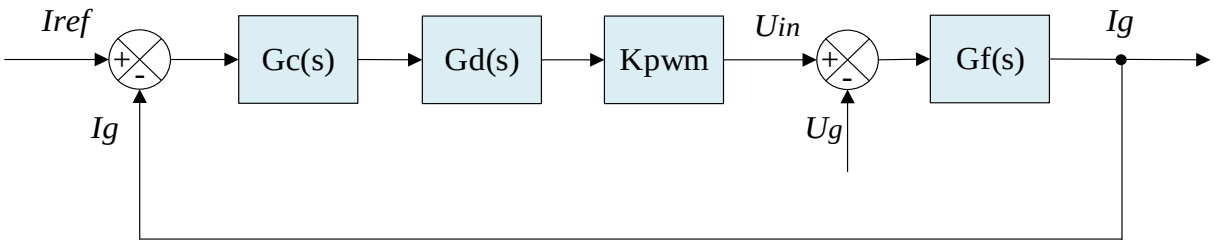


Figure 3.8 PI/PR-based current control loop

3.3.1 PI Controller-based Current Control Loop

A simple and effective PI controller is widely employed in many control systems. As described in Figure 3.9, it uses two gain constants, the proportional gain K_p and integral gain K_i, which are multiplied by the error signal ε_i. The multiplications of the proportional term and integral term are then summed as the controller output [119].

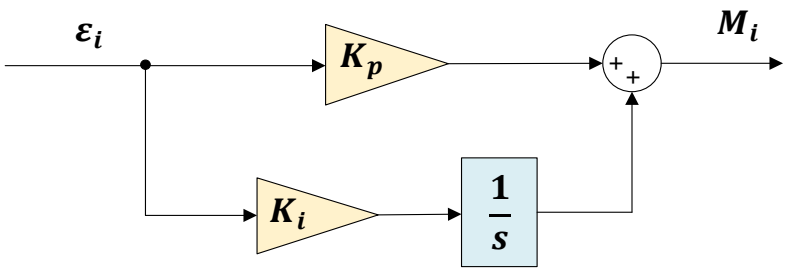


Figure 3.9 General structure of PI controller

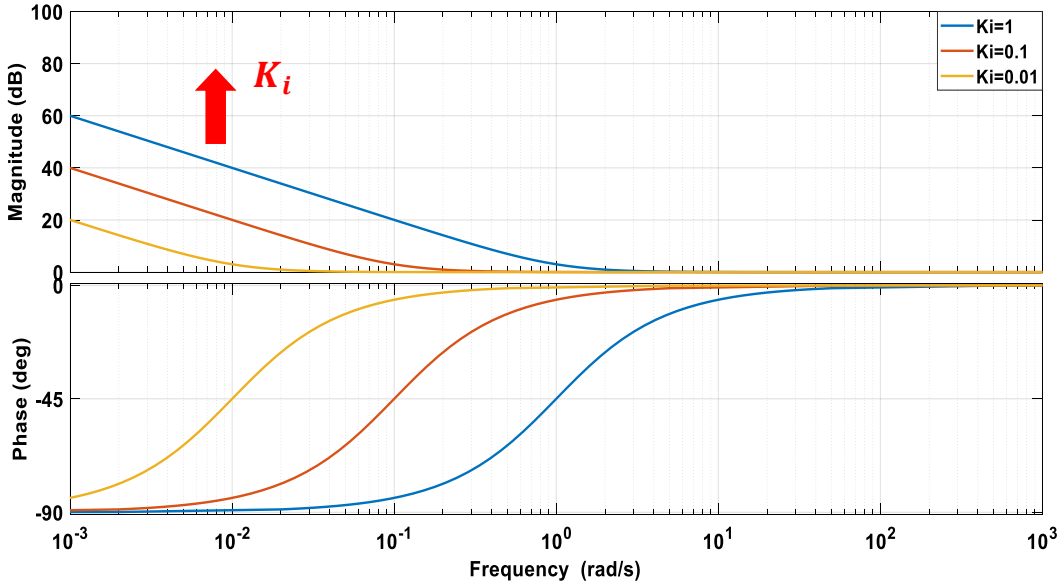
From Figure 3.9, the well-known s-domain expression for the PI controller is given as:

$$M_i(s) = \left(K_p + \frac{K_i}{s}\right) \varepsilon_i(s) \tag{3.8}$$

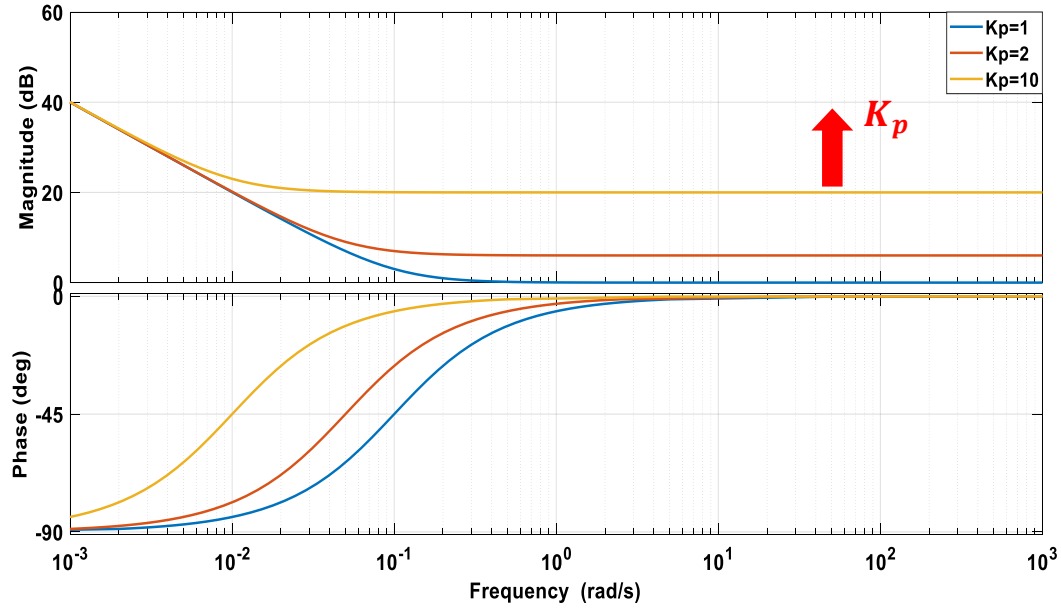
And the transfer function of the PI controller can be written as:

$$G_{PI}(s) = \frac{M_i(s)}{\varepsilon_i(s)} = \frac{K_p s + K_i}{s} \tag{3.9}$$

The dynamic performance of the controller has a significant dependency on the gain constants. The proportional gain K_p relates to the overshoot and response time, whilst the integral gain K_i is proportional to both the magnitude and duration of the steady-state error (SSE). For both proportional and integral terms, high gain values could induce unstable operation of the system. Therefore, many tuning techniques, including formula-based, rule-based and optimization-based methods, and improvements have been suggested in [120]. Here, variations in K_p and K_i are investigated based on the Bode plots shown in Figure 3.10. With a fixed proportional gain $K_p = 1$, the increase in the integral constant K_i yields a greater gain at low-frequency. As the gain keeps ramping up at lower frequencies, an infinite DC gain (0 Hz) is obtained by including the integral term. On the other hand, the proportional constant K_p provides a constant gain throughout the frequency spectrum, as shown in Figure 3.10 (b). Thus, for the PI controller, an adequate gain at a selected frequency (for example, the grid frequency) requires a large K_p, which could potentially cause the system to be unstable.



(a) K_i varying from 0.01 to 1; K_p fixed at 1



(b) K_p varying from 1 to 10; K_i fixed at 0.1

Figure 3.10 Bode plot of PI controller

Based on the diagram shown in Figure 3.8, the s-domain expression of the grid current can be derived by regarding the current reference I_{ref} and grid voltage V_{gird} as two separate inputs, which can be written as:

$$I_g = \frac{G_c(s)G_d(s)K_{pwm}G_f(s)}{1 + G_c(s)G_d(s)K_{pwm}G_f(s)} I_{ref} - \frac{G_f(s)}{1 + G_c(s)G_d(s)K_{pwm}G_f(s)} V_{gird}$$

(3.10)

Assuming a simple inductor is used as the output filter $G_f(s)$, thus yields:

$$I_g = \frac{G_c(s)G_d(s)K_{pwm}}{sL + R + G_c(s)G_d(s)K_{pwm}} I_{ref} - \frac{1}{sL + R + G_c(s)G_d(s)K_{pwm}} V_{gird}$$

(3.11)

As mentioned previously, the proportional gain K_p is limited in order to guarantee the stable operation of the current control loop, which leads to an insufficient gain of $G_c(s)$ at the fundamental frequency. In this case, the grid voltage term is not negligible, which creates a steady-state error in tracking the grid reference. This is proven in Figure 3.10, where the integral term itself has a zero gain at the high-frequency periodical disturbance and integer multiple harmonics.

Consequently, although the advantages of the PI controller are quite clear, this solution is prone to two main drawbacks for current-controlled inverters: an inability to track a sinusoidal reference without SSE, and a poor disturbance rejection capability [121-123]. By replacing the integral term, the current control loop based on the proportional-resonant structure can be used to overcome these issues.

3.3.2 PR Controller-based Current Control Loop

Figure 3.10 shows the structure of the PR controller, which consists of a proportional term and a resonant term. The proportional gain K_p determines the system dynamics in terms of bandwidth and phase, while the resonant term provides an infinite gain at frequency ω_0. Conceptually, this is similar to the integrator in the PI controller whose infinite DC gain yields a zero DC error. An ideal PR controller is capable of eliminating the steady-state error or harmonics at the frequency ω_0, whilst producing no phase shift or gain at other frequencies[116],[124],[125].

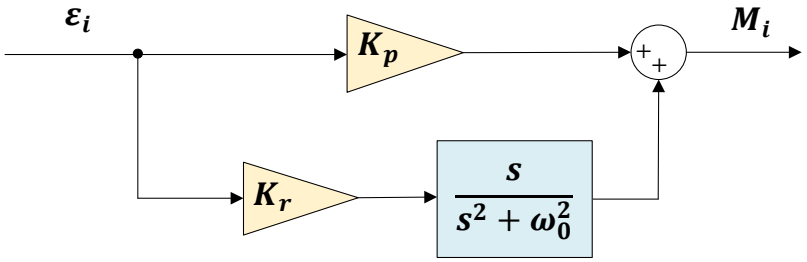


Figure 3.11 Structure of ideal PR controller

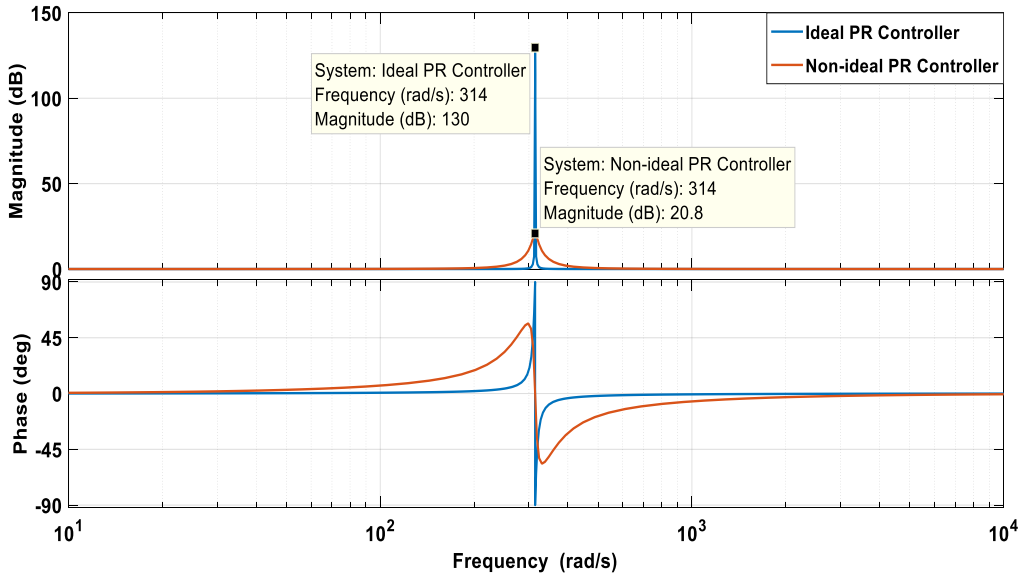
Based on Figure 3.11, the transfer function of the PR controller is given as:

$$G_{PR}(s) = \frac{M_i(s)}{\varepsilon_i(s)} = K_p + \frac{K_r s}{s^2 + \omega_0^2} \tag{3.12}$$

However, the realization of the ideal resonant transfer function cannot be achieved owing to the component tolerance in the physical circuit and finite precision levels in digital systems. Even through it is theoretically possible, the infinite gain would potentially lead to system stability issues. Thus, the non-ideal form of a PR controller is given in equation (3.13), where ω_c is the bandwidth around the resonant frequency ω_0 [117]:

$$G_{PR}(s) = \frac{M_i(s)}{\varepsilon_i(s)} = K_p + \frac{2K_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{3.13}$$

From the Bode plot in Figure 3.12, it can be seen that the gain at frequency ω_0, which is set to 50Hz in this case, is much reduced with a broader bandwidth in the non-ideal PR controller. Nevertheless, this realizable finite gain is still large enough to force a neglectable steady-state error.



Ideal PR Controller: $K_p = 1, K_r = 10, \omega_0 = 314$ *rad/s*

Non-Ideal PR Controller: $K_p = 1, K_r = 10, \omega_c = \pi, \omega_0 = 314$ *rad/s*

Figure 3.12 Bode plot of ideal and non-ideal PR controller

Besides its effective control at the resonant frequency ω_0, the PR controller can be designed to compensate for selected harmonic orders. This is accomplished by cascading several compensation blocks, which are tuned to resonate at the desired harmonics as shown in Figure 3.13 [125]. Since these harmonic compensators only compensate for the frequencies that are close to the selected harmonics, the dynamic performance at the fundamental frequency ω_0 would not be affected [126].

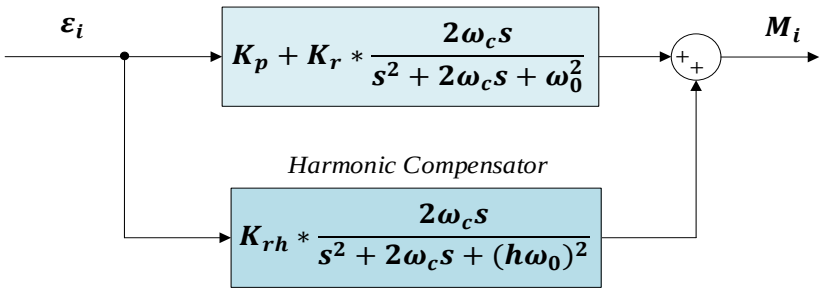
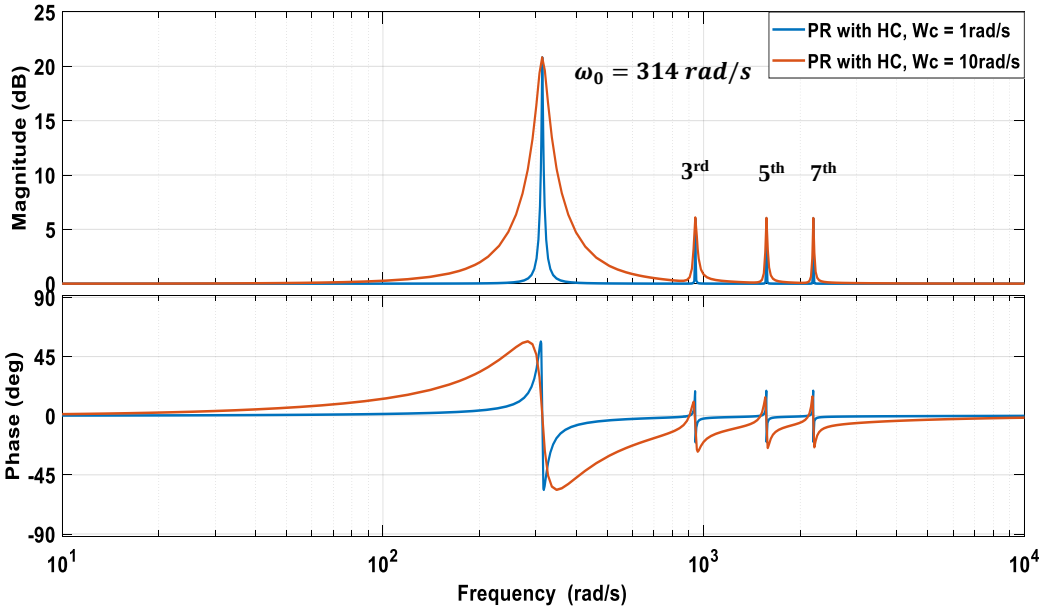


Figure 3.13 PR controller with harmonic compensator

Figure 3.14 shows the Bode plot of the PR controller with harmonic compensators designed for the 3rd, 5th and 7th harmonics. For the same set of PR gain parameters (K_p=1, K_r=10), the unity harmonic resonant gain K_{rh} provides a resonant peak at those selected frequencies, which regulates the current harmonics errors in the same manner as with the fundamental frequency. At the same time, the different values of ω_c have a significant impact on the bandwidth of the resonant peaks. Although the smaller value of ω_c sharpens the selectivity of frequencies as shown in the Bode plot, it in turn would degrade the robustness of the controller and its sensitivity to variations in frequencies [127]. Typically, a value of ω_c between 5 to 15 rad/s has been found to provide a good compromise [128].



PR Controller with Harmonic Compensator (HC): K_p = 1, K_r = 10, ω_0 = 314 rad/s

ω_c = 1 or 10 rad/s, K_{rh} = 1

Figure 3.14 Bode plot of PR with compensation at 3rd, 5th and 7th harmonics

Based on the characteristics of the PR controller, the grid current expression in equation (3.11) is re-evaluated below. As the gain at the fundamental frequency is significantly large, the effect of grid voltage can be neglected, and the grid current is simply given as:

$$I_g = \frac{G_c(s)G_d(s)K_{pwm}}{sL + R + G_c(s)G_d(s)K_{pwm}} I_{ref} \qquad (3.14)$$

Equation (3.14) shows that the use of the PR controller allows a zero steady-state error operation in tracking the sinusoidal current reference. Similarly, the simple cascading of the harmonic compensators (HCs) provides large gain at the selected frequencies, which eliminates the dominant harmonics without affecting the controller dynamics. These advantages make the PR control scheme preferable for single-phase grid-connected VSI systems.

3.3.3 PWM Schemes and Delay Effect

A. PWM Schemes

Pulse-width modulation (PWM) techniques have been universally adopted in VSI applications owing to their advantages of simplicity and loss-reduction. In the full-bridge topology, sinusoidal PWM (SPWM) is generated by comparing the sinusoidal control signal with a pre-set triangular carrier. As the switches in each leg of the H-bridge should not conduct simultaneously, two main modulation strategies are normally implemented, namely bipolar (BP) and unipolar (UP) modulation.

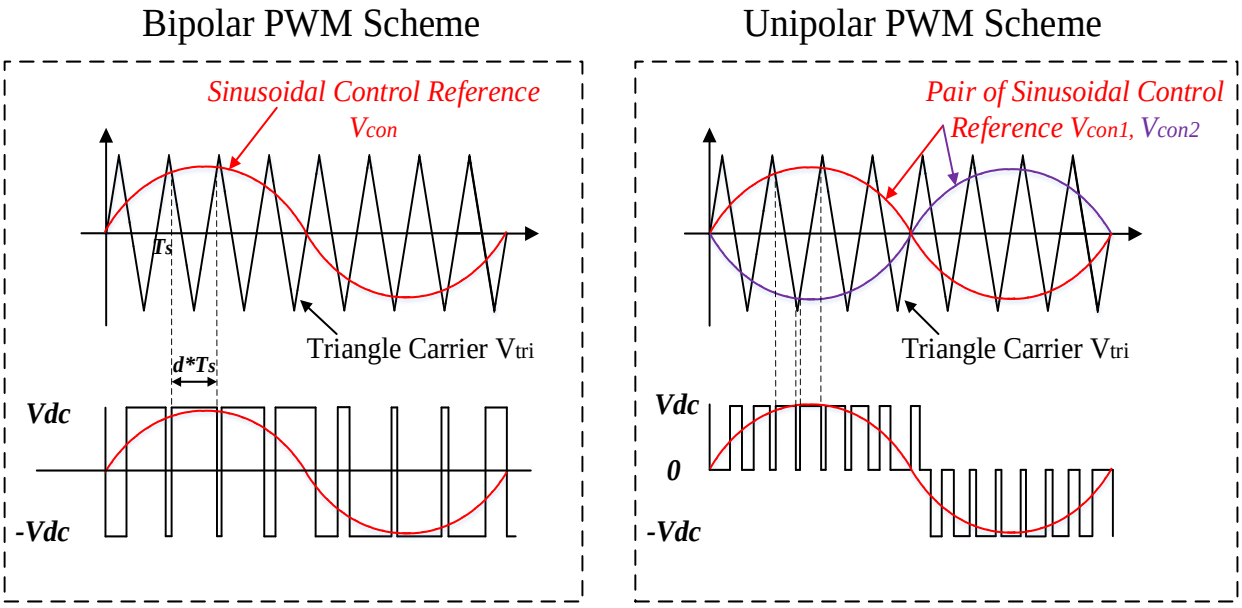


Figure 3.15 Bipolar and unipolar PWM schemes

Figure 3.15 shows the operation of bipolar and unipolar PWM schemes. As only one control reference is used in the bipolar scheme, in this case the switches in the H-bridge are switched synchronously in the diagonal from the Leg A top and Leg B bottom to the Leg A bottom and Leg B top. Although the implementation of the bipolar scheme is relatively easy, the converter suffers from a higher current ripple and increased core losses. In the unipolar scheme, the two legs are operated according to its separate control references, V_{con1} and V_{con2}. As shown in the unipolar PWM switching scheme, the two sinusoidal modulating signals are of the same amplitude and frequency but are $180°$ out of phase with each other. This yields an extra zero output state, which is also known as the freewheeling state which happens when two top switches or bottom switches of each leg are conducting. This halves the output PWM voltage and doubles the switching ripple. Thus, for the same fundamental output voltage, the advantages of lower filtering requirements and higher efficiency are achieved in unipolar modulation [99],[129],[48]. The following simulations and practical experiments apply unipolar switching modulation as the PWM scheme. The mathematical representation of the VSI and PWM is given as a unity static gain of $K_{pwm} = 1$.

B. Delay Effect

The delay effect has to be considered, as the current control is implemented digitally. Generally, there are two types of delay: PWM and computation delay. The PWM delay represents the time distance between the updating instant of the modulating reference and the instant when the gate pulse is determined, and computation delay is introduced by the computation device [130].

Figure 3.16 shows a single-update PWM model, where the PWM updates at the beginning of each switching period whilst the current sample is normally taken at the middle of the switching period. As the sampled current is used to calculate the PWM reference, which is only updated at the next updating instant, the PWM delay and computation delay are given respectively as half of the duration and the full duration of the modulation period [99],[131]. With a given modulation period (sample time) of T_s, the Laplace transfer function of delay effect is described in equation (3.15):

$$G_d(s) = \frac{1}{1 + 1.5T_s\, s} \tag{3.15}$$

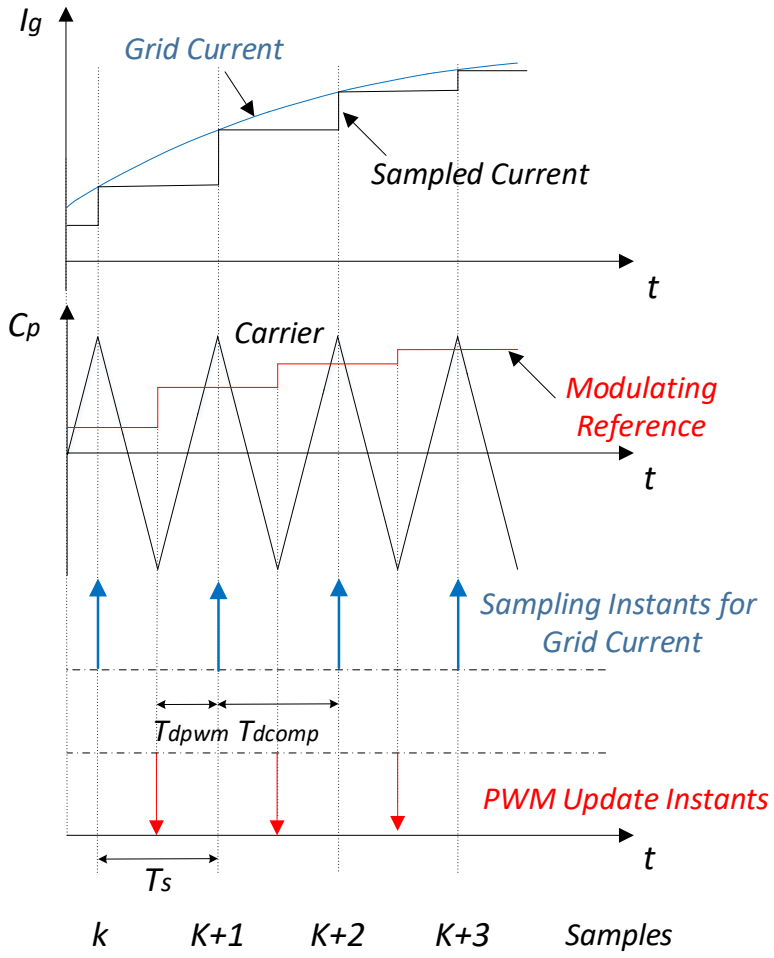


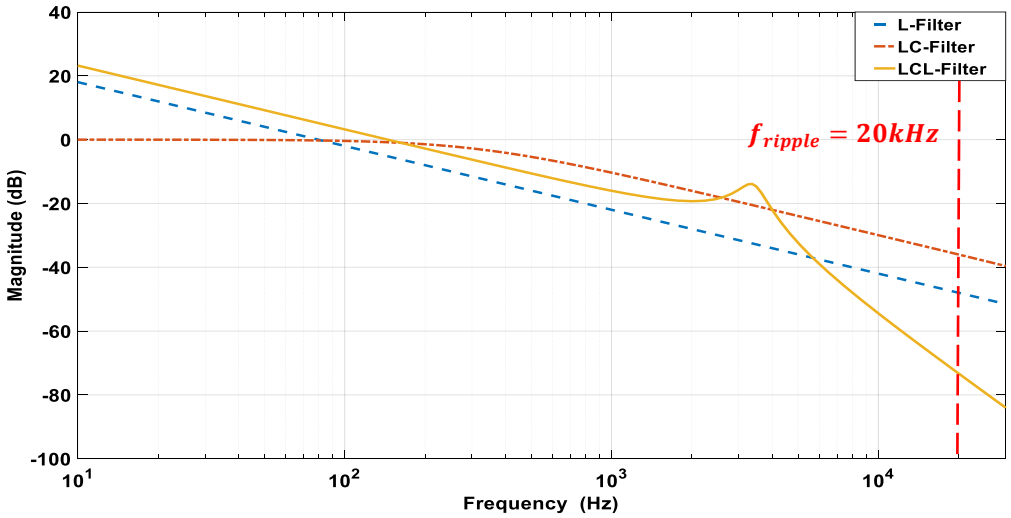
Figure 3.16 PWM and computation delays in digital PWM implementation

Based on the control diagram shown in Figure 3.8, this section has investigated the typical current control loop of the VSI. The transfer functions of the PI/PR current controller $G_c(s)$, PWM gain K_{pwm} and time delay $G_d(s)$ are separately given and analyzed. As the inverter output voltage operates at switching frequency, an output filter $G_f(s)$ is connected to the inverter output which provides adequate attenuation of the switching harmonics. In the following section, the selection and determination of the output filter is illustrated in detail.

3.4 Grid Filter Determination

In grid-connected inverter systems, a passive filter is inserted between the inverter output and the point of common coupling (PCC) to limit the voltage harmonics and current ripple. Traditionally, the implementation of the output filter is a simple first-order *L* filter. Due to insufficient attenuation, this filter requires either a high switching frequency or a large inductance value to meet the grid interconnection requirements, which in turn degrades the dynamics and efficiency of the whole system [132],[133]. By connecting a shunt capacitor, the second-order *LC* filter improves the filtering performance of the *L* filter with a smaller inductor. However, as its resonant frequency has a great dependency on the grid impedance, the *LC* filter is not recommended, especially when the system is connected to a weak grid [134],[135]. Hence, there has been increasing interest in the use of higher-order filters, as they offer better filtering performance with reduced size and cost [133].

Among the high-order grid interface filters, the third-order *LCL* filter is the most commonly used solution for grid-connected PV applications. Compared with *L* and *LC* filters, it provides higher attenuation of the switching harmonics and better decoupling between the filter and the grid impedance. Such a filter also allows the inverter to operate with a lower switching frequency, thereby achieving reduced switching losses [132],[134],[136]. Figure 3.17 shows a frequency analysis of filter variants (*L*, *LC*, *LCL*), where the *LCL* filter gives a significantly larger attenuation of the switching frequency ripple.



L-Filter L=2mH, LC-Filter L= 0.5mH, LCL-Filter L_i= 0.8mH, Grid-side L_g= 0.3mH.

Figure 3.17 Bode plot of filter variants

3.4.1 Parameter Selection of Single-Phase LCL Filter

Figure 3.18 shows the typical schematic circuit of a single-phase *LCL* filter, where the L_i and L_g are separately known as the inverter-side and grid-side inductors. The C_f is the filter capacitor. The selection of these filter parameters is a complicated process since further criteria have to be considered such as the resonant frequency, and fundamental voltage drop across the inductors. Generally, the inverter-side inductor L_i is determined based on the output current ripple, whilst the grid-side inductor L_g is determined based on the high-frequency attenuation. The capacitor rating is sized according to the fundamental reactive power limit [137],[138]. Moreover, to avoid the stability issue brought about by the undesired resonance frequency of the *LCL* filter, some modifications are implemented either in the controller or filter structure. These solutions are separately referred to as active damping and passive damping [136],[139],[140]. Some suggested guidelines and design have been studied elsewhere [135],[138],[141],[142], where the parameters of the *LCL* filter can be selected and optimized according to the requirements of different applications.

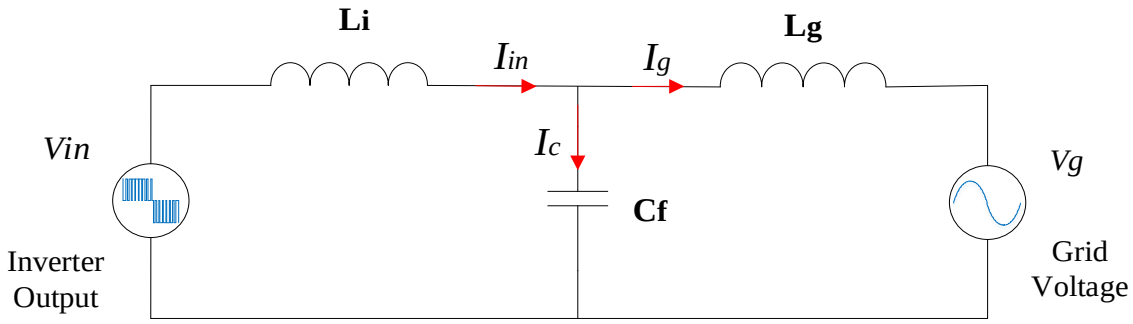


Figure 3.18 Schematic circuit of single-phase LCL filter

To meet grid interconnection standards, the design of the *LCL* filter in the grid-connected PV inverter system should meet the following criteria [133]:

1) The filter capacitance is limited to decrease the capacitive reactive power within 5%.
2) The selection of inverter-side inductor should limit the ripple current to lower than 20%.
3) The current harmonics higher than 35th should be less than 0.3% of the fundamental harmonic.
4) The resonance frequency should be located at between the times the line frequency and one half of the switching frequency.

Following this, the values of inductance and capacitance can be determined based on the design procedure. The filter capacitance C_f is determined from the base capacitance:

$$C_f = 0.05 * \frac{P_{rated}}{{U_g}^2 \omega_g}$$

(3.16)

where P_{rated} is the system rated power, U_g is the grid voltage, and ω_g is the grid frequency. The determination of inverter-side inductance is given as:

$$L_{in} = \frac{V_{DC}}{16 f_{sw} \Delta I_{rated}}$$

(3.17)

where the V_{DC} is the DC link voltage, f_{sw} is the switching frequency, and ΔI_{rated} is the ripple factor. The grid-side inductance can be selected as a function of L_{in}. As described in equation 3.18, the inductance index r ($0 \leq r \leq 1$) is determined by the switching harmonic attenuation ratio.

$$L_g = r L_{in}$$

(3.18)

With the selected inductance and capacitance, the resonance frequency of the *LCL* filter can be calculated as:

$$\omega_{res} = \sqrt{\frac{L_i + L_g}{L_{in} L_g C_f}}$$

(3.19)

From the criteria above, the calculated resonance frequency should be located in the range in equation (3.20). In this way, the filter guarantees the line-frequency operation of the system, whilst offering a sufficient attenuation of the switching frequency ripple.

$$10\ \omega_g \ \leq\ \omega_{res} \ \leq\ \frac{\omega_{sw}}{2}$$

(3.20)

Due to its simplicity and high reliability, the passive damping solution is adopted with a damping resistor in series with the filter capacitor. The selection of the damping resistor is given as:

$$R_d = \frac{1}{3 \omega_{res} C_f}$$

(3.21)

3.4.2 Mathematical Analysis of the LCL Filter

Based on the equivalent circuit shown in Figure 3.18, Figure 3.19 describes the mathematical model of the *LCL* filter, where the inverter-side inductor, filter capacitor, damping resistor and grid-side inductor are represented as s-domain transfer functions. The two inputs are the inverter output $U_{in}(s)$ and grid voltage $U_g(s)$, and the output is the grid-side current $I_g(s)$. $I_{in}(s)$ and $I_c(s)$ are separately known as the current flowing through the inverter-side inductor and the filter capacitor.

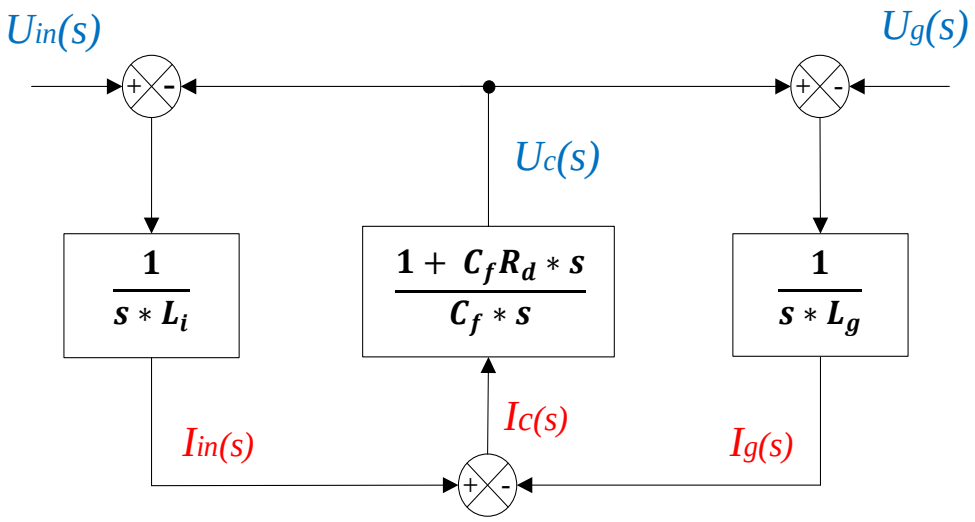


Figure 3.19 Mathematical model of LCL filter

Applying Kirchhoff's voltage law (KVL) to the *LCL* model, the voltage across the inductors is given as:

$$U_{in}(s) - U_g(s) = sL_{in}I_{in}(s) + sL_gI_g(s) \tag{3.22}$$

Ultimately, the transfer function of the *LCL* filter should be derived as a relationship between the grid current and input voltages. According to the Kirchhoff's current law (KCL), the inverter-side current $I_{in}(s)$ is the sum of the grid current $I_g(s)$ and the capacitor current $I_c(s)$, yielding:

$$U_{in}(s) - U_g(s) = sL_{in}[I_g(s) + I_c(s)] + sL_gI_g(s) \tag{3.23}$$

Thus the expression for the capacitor-grid voltage network shown in Figure 3.18 can be written as:

$$U_c(s) - U_g(s) = sL_g I_g(s)$$

(3.24)

Representing the capacitor branch voltage $U_c(s)$ by the capacitor current $I_c(s)$, yield:

$$\left(\frac{1}{C_f s} + R_d\right) I_c(s) - U_g(s) = sL_g I_g(s)$$

$$I_c(s) = \frac{U_g(s) + sL_g I_g(s)}{R_d + \frac{1}{C_f s}}$$

(3.25)

Thus, substituting the $I_c(s)$ with equation (3.25), equation (3.23) can be expressed as a function of grid current $I_g(s)$ and voltage inputs $U_{in}(s) - U_g(s)$, as follows:

$$U_{in}(s) - U_g(s) = sL_{in} * [I_g(s) + \frac{U_g(s) + sL_g I_g(s)}{R_d + \frac{1}{C_f s}}] + sL_g I_g(s)$$

(3.26)

Then, by rearranging equation (3.26), the transfer function of the *LCL* filter is given as:

$$\frac{I_g(s)}{U_{in}(s) - \lambda U_g(s)} = \frac{C_f R_d s + 1}{C_f L_{in} L_g s^3 + (C_f R_d L_g + C_f R_d L_{in}) s^2 + (L_g + L_{in}) s}$$

(3.27)

where the grid voltage factor $\lambda = \frac{1 + C_f R_d s + C_f L_{in} s^2}{C_f R_d s + 1}$. The full derivation of equation (3.27) is presented in Appendix A.

As the magnitude and phase angle of the grid voltage factor at line-frequency are zero, λ can be equivalently replaced by a unity static gain. This is also proved from the Bode plot analysis shown in Appendix A. Hence, the transfer function of the grid-side current to voltage inputs is written as:

$$\frac{I_g(s)}{U_{in}(s) - U_g(s)} = \frac{C_f R_d s + 1}{C_f L_{in} L_g s^3 + (C_f R_d L_g + C_f R_d L_{in}) s^2 + (L_g + L_{in}) s}$$

(3.28)

This *LCL* model is utilized throughout the project, where the filter parameters C_f, L_{in}, L_g *and* R_d are separately determined using equations (3.16) to (3.21). As the filter model is included in the current control loop, the analysis given in the following section is based on the selected filter parameters.

3.5 Mathematical Model of Grid-Connected VSI System

By replacing the control blocks with the mathematical models, the grid-connected VSI can be equivalently developed as shown in Figure 3.20. To achieve zero-SSE operation, the grid current $I_g(s)$ is controlled at the reference current $I_{ref}(s)$ via the PR controller, whilst the *LCL* filter is connected to provide sufficient attenuation to the switching frequency ripple. As the aim of developing this model is to analyze the system stability and sensitivity to gain parameters, this can be done based on the overall open-loop and closed-loop transfer functions.

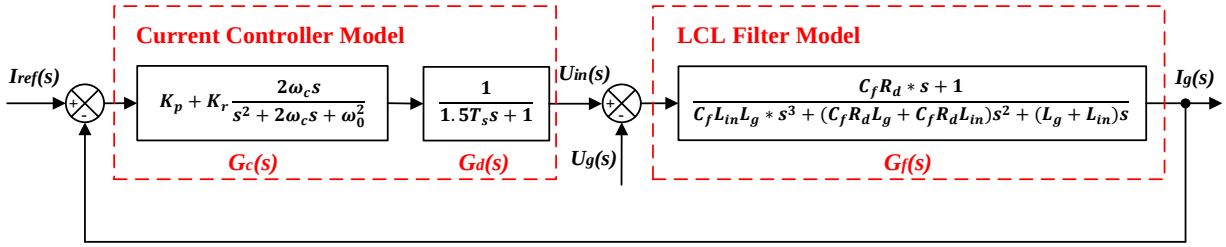


Figure 3.20 Mathematical model of grid-connected VSI

It has been proven that the effect of grid voltage $U_g(s)$ can be neglected with the use of a PR controller. Therefore, the open-loop transfer function is derived as the series of the controller model and LCL filter, yielding:

$$G_{op}(s) = G_c(s)G_d(s)G_f(s)$$

$$G_{op}(s) = \frac{C_f R_d K_p s^3 + \left[2\omega_c C_f R_d (K_p + K_r) + K_p\right] s^2 + \left[K_p \omega_0^2 C_f R_d + 2\omega_c (K_p + K_r)\right] s + K_p \omega_0^2}{1.5 T_s C_f R_d L_g\, s^6 + A s^5 + B s^4 + C s^3 + D S^2 + (L_g + L_{in}) \omega_0^2\, s} \quad (3.29)$$

Where the coefficients A, B, C, D are separately given as follows:

$$A = C_f R_d L_g (3\omega_c T_s + 1.5T_s + 1) + C_f R_d L_{in} 1.5T_s$$

$$B = C_f R_d L_g (1.5T_s \omega_0^2 + 2\omega_c + 3\omega_c T_s + 1) + C_f R_d L_{in} (3\omega_c T_s + 1) + (L_g + L_{in}) 1.5T_s$$

$$C = C_f R_d L_g (\omega_0^2 + 1.5T_s \omega_0^2 + 2\omega_c) + C_f R_d L_{in} (1.5T_s \omega_0^2 + 2\omega_c) + (L_g + L_{in})(3\omega_c T_s + 1)$$

$$D = (C_f R_d L_g + C_f R_d L_{in}) \omega_0^2 + (L_g + L_{in})(1.5T_s \omega_0^2 + 2\omega_c)$$

The open-loop transfer function $G_{op}(s)$ represents a 6th order system with complicated coefficients. As a simulation of the 2-kW single-phase grid-connected inverter has been established to verify the operation of the control scheme, these coefficients can be determined accordingly from the system parameters. In the simulation, the inverter is operated from a 400 V DC link voltage at a switching rate of 20 kHz, which feeds a current demand of 8.7 A to a 230 V AC grid. Table 3.1 shows the system's operational parameters and optimized filter values. The resonance frequency of the filter is 4.33 kHz, which fits perfectly the range given in equation (3.20).

Table 3.1 VSI simulation parameters

Parameters	***Value***
DC Link Voltage, V_{DC}	*400 V*
Rated Power, P_{rate}	*2 kW*
Grid RMS Voltage, V_g	*230 V*
Grid Frequency, f_g	*50 Hz*
Rated RMS Current, I_g	*8.7 A*
Switching Frequency, f_{sw}	*20 kHz*
Sampling Frequency, f_s	*20 kHz*
Proportional Gain, k_P	k_P
Resonant Gain, K_r	K_r
Bandwidth Coefficient, ω_c	*6.28 rad/s*
Controller Sample Time, T_s	$5 \times 10^{-5}\ s$
Inverter-side Inductance, L_i	*3.69 mH*
Grid-side Inductance, L_g	*0.46 mH*
Filter Capacitance, C_f	*3.3 μF*
Damping Resistance, R_d	*2.2* Ω
Resonant Frequency, f_{res}	*4.33 kHz*

Figure 3.21 shows the Bode plot of the open-loop transfer function with the set of gain parameters $K_P = 2, K_r = 55$, where the gain margin and phase margin are confirmed separately as 29.1dB and 54.4° respectively. Although it has a fair distance from being unstable, the stability margin still depends closely on the gain constants. An increase of proportional constant K_P would reduce the gain and phase margins, whilst an increase of resonance constant K_r would lead to a smaller phase margin. High values of either gain constant might potentially result in the unstable operation of the current control loop. Hence, the gain constants of the PR controller should be carefully tuned to provide adequate gain at the selected frequency, meanwhile guaranteeing a stable operation of the VSI system.

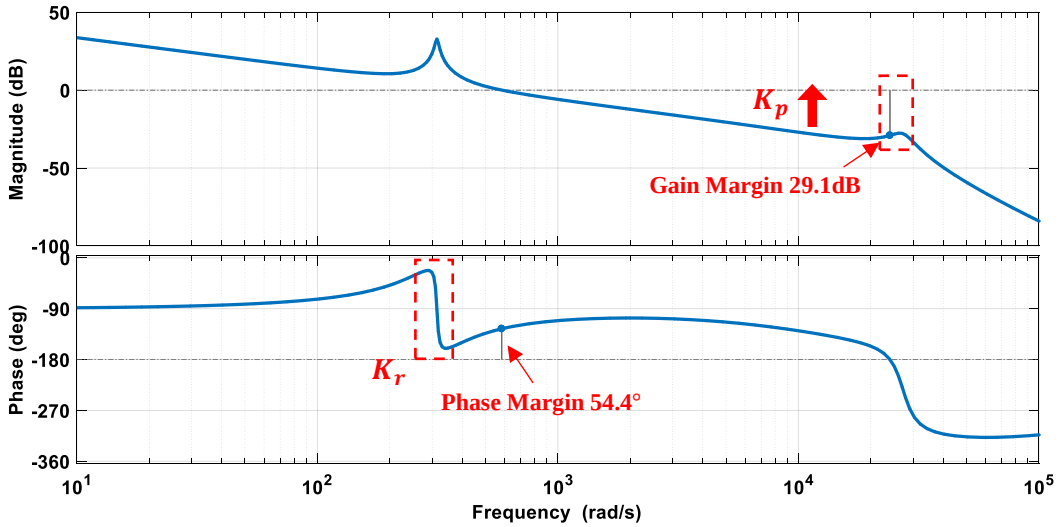


Figure 3.21 Bode plot of open loop system

This is also proven in the closed-loop transfer function derived from the open-loop transfer function as follows:

$$G_{cl}(s) = \frac{I_g(s)}{I_{ref}(s)} = \frac{G_{op}(s)}{1 + G_{op}(s)}$$

$$G_{cl}(s) = \frac{C_f R_d K_p s^3 + \left[2\omega_c C_f R_d (K_p + K_r) + K_p\right]s^2 + \left[K_p \omega_0^2 C_f R_d + 2\omega_c K_p + 2\omega_c K_r\right]s + K_p \omega_0^2}{1.5 T_s C_f R_d L_g s^6 + As^5 + Bs^4 + C's^3 + D'S^2 + Es + K_p \omega_0^2}$$

(3.30)

where the determinations of C', D', E are listed as:

$$C' = C_f R_d L_g(\omega_0^2 + 1.5T_s\omega_0^2 + 2\omega_c) + C_f R_d L_{in}(1.5T_s\omega_0^2 + 2\omega_c) + \left(L_g + L_{in}\right)(3\omega_c T_s + 1) + C_f R_d K_p$$

$$D' = \left(C_f R_d L_g + C_f R_d L_{in}\right)\omega_0^2 + \left(L_g + L_{in}\right)(1.5T_s\omega_0^2 + 2\omega_c) + \left[2\omega_c C_f R_d\left(K_p + K_r\right) + K_p\right]$$

$$E = \left(L_g + L_{in} + C_f R_d K_p\right)\omega_0^2 + 2\omega_c K_p + 2\omega_c K_r$$

Similarly, by substituting these complicated coefficients for the system parameters in Table 3.1, the system stability can be analyzed with the z-domain closed-loop transfer function. This is accomplished by discretizing the continuous s-domain transfer function using the 'c2d' function in MATLAB. Owing to its ease of implementation and the good preservation of the frequency response, the Tustin transformation method is selected, as described in equation (3.31), which arranges the poles and zeros to correspond on the left-hand plane of the s-domain (stable) within the unit circle in the z-domain [143].

$$G_{cl}(z) = G_{cl}(s)\big|_{s=\frac{2}{T_s}\frac{z-1}{z+1}} \qquad (3.31)$$

In figure 3.22, the poles and zeros of the discrete closed-loop transfer function are recorded for a fixed K_r with different K_p values. The arrows indicate the direction of pole movement with increasing K_p. If the system is stable, all three pole-pairs (P_1, P_2, P_3) of $G_{cl}(z)$ should be located within the unit circle. It can be clearly observed that a greater value of K_p causes the pole-pair P_1 to move outside the unit circle, and the system has become unstable. Furthermore, simply reducing K_p would not guarantee a stable operation as it in turn moves the pole-pair P_3 towards the outside. This links back to the stability margin analysis in the Bode plot of the open-loop transfer function, where zero magnitude occurs around the fundamental frequency with a -180° shift in the phase diagram. Thus, the gain constant K_p should be carefully tuned to obtain stable operation. It is worth mentioning that simplification and approximation would cause the mathematical model to differ from the simulation model and experimental test rig. Therefore, the stable range of K_p from the stability analysis would not fit the stable working range in simulations and experiments very well. However, the stability analysis based on the transfer function is still vitally significant, as it shows the sensitivity of the system to changes in gain parameters.

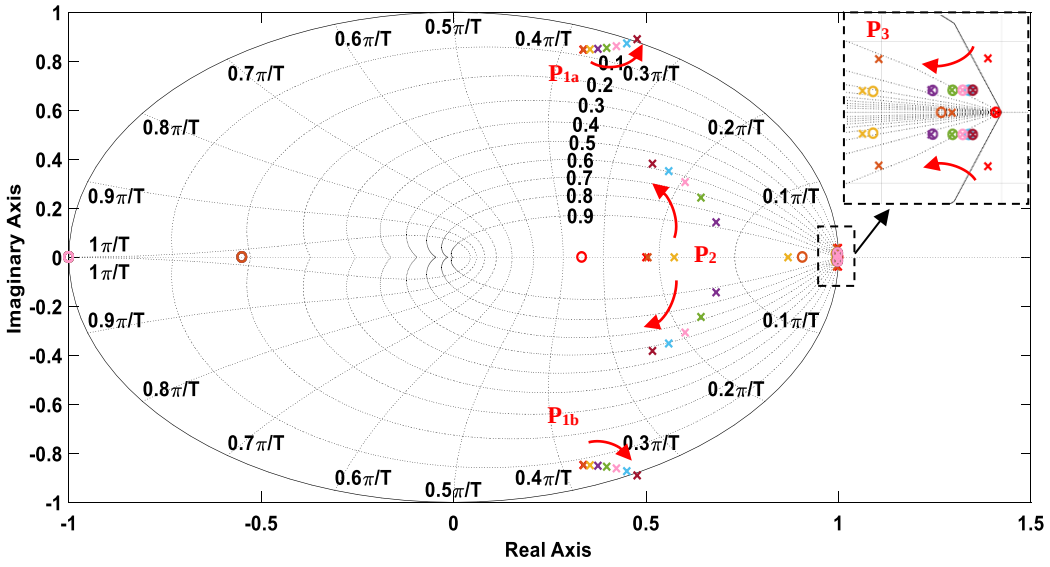


Figure 3.22 Pole-zero plot for a varying K_p

Figure 3.22 shows the pole-zero plot for a fixed K_p with varying K_r, where the arrows indicate the direction of pole movement with the increase in K_r. The pole-pairs P_1 and P_2 are not sensitive, whilst the P_3 moves a long way toward the outside of the unit circle with the increase of K_r, causing the system to become unstable. Hence, the resonance gain also characterizes the system stability, which needs to be carefully tuned.

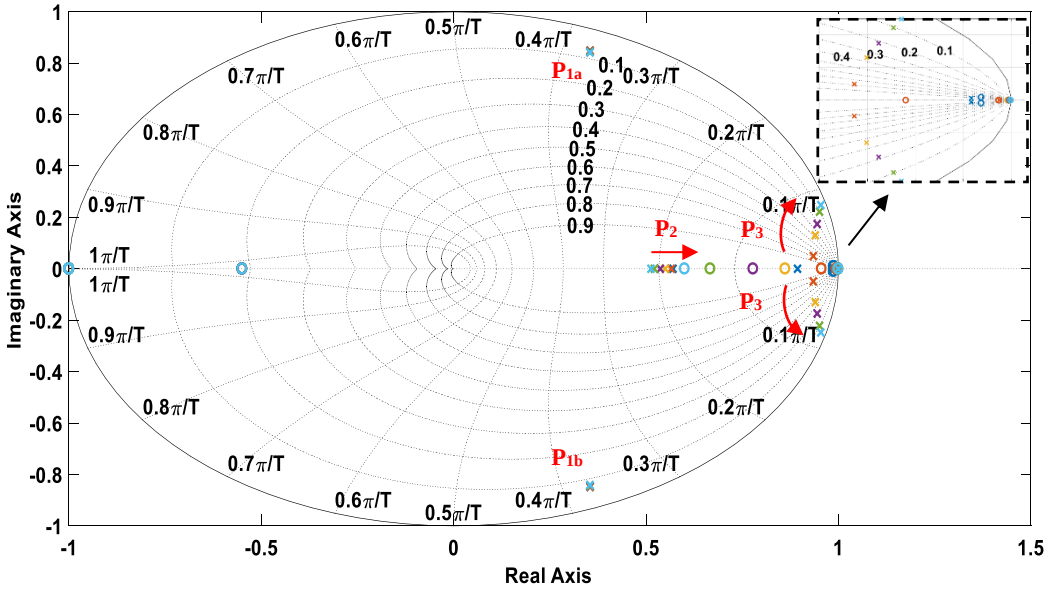


Figure 3.23 Pole-zero plot for a varying K_r

3.6. Simulation of Single-Phase Grid-Connected PV Inverter System

Given the system parameters in Table 3.1, the results of grid-connected PV inverter simulations are reported in this section. The performance of the PR controller and harmonics compensator (HC) is verified by separately connecting the inverter system to the ideal and real grid models. Beyond that, sources of DC injection are introduced into the simulation model. This proves the existence of DC injection in the output current, even with a properly tuned current controller.

3.6.1 Simulated VSI System Connected to the Ideal Grid and the Simulated Grid Model.

Figure 3.24 shows the performance of grid current operation and harmonic distribution when the simulated inverter is connected to a 230 V-RMS AC voltage source (ideal grid). At 2 kW rated power, the PR controller adjusts the grid current to the demand current (RMS-8.7 A, PEAK-12.3 A) with an SSE less than 0.02 A, achieving a total harmonic distortion (THD) of 0.03 %. Although the results are perfect, the real grid voltage would never be purely sinusoidal. Thus, a more realistic grid voltage model is required to further investigate the controller performance.

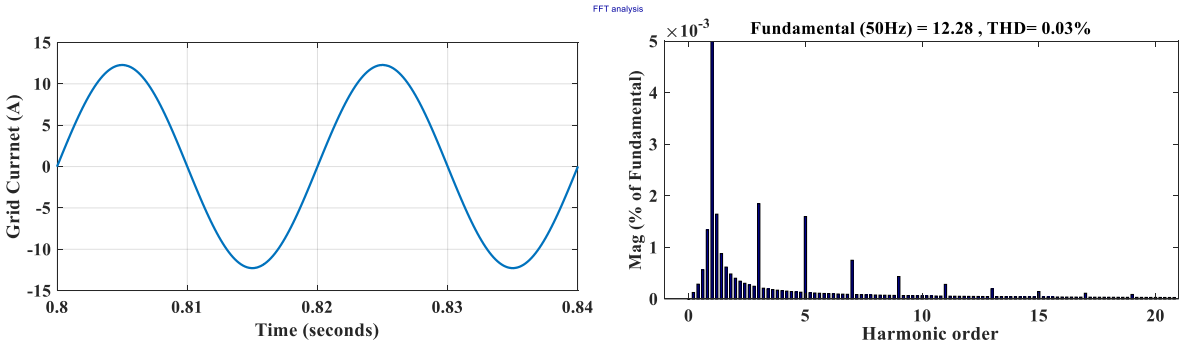


Figure 3.24 PR controller with ideal grid

The grid model is developed from the real harmonics data obtained using a fast Fourier transform (FFT) analysis of the experimental grid voltage. Figure 3.25 shows the harmonic distribution of the simulated grid model, where the fundamental component is 324.5 V and the dominant harmonics appear the on 3rd, 5th, 7th and 9th. By connecting the PV inverter simulation to the new grid model, the results of the PR-based current operation are shown in Figure 3.26. The simulation model of the PV inverter system and the structure of the grid model are presented in Appendix B.

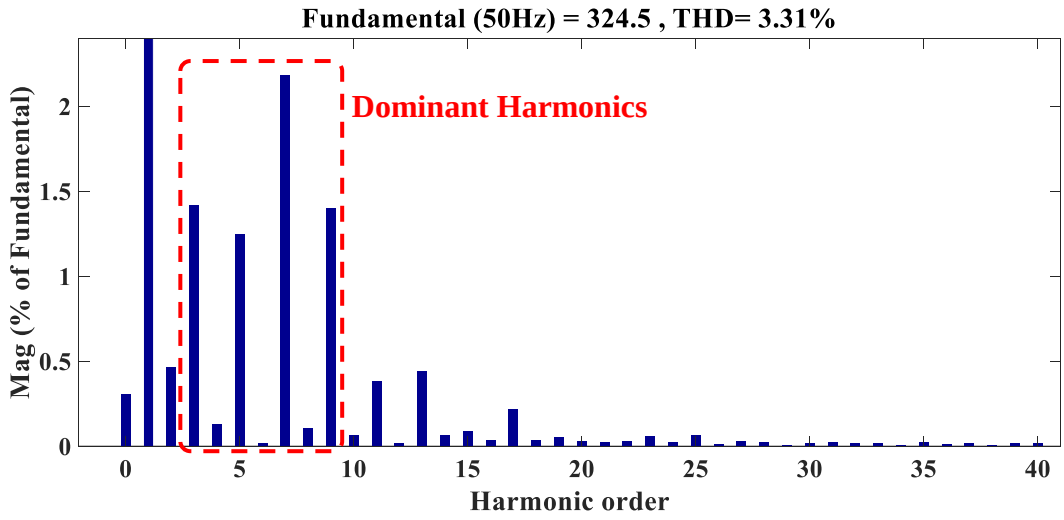


Figure 3.25 Harmonic distribution of the simulated grid voltage model

Due to the impact of grid harmonics, the grid current waveform is slightly distorted compared with the results of which connected to an ideal grid. This is shown in the harmonic distribution in Figure 3.26, where obvious increases of harmonic components are observed. In particular, the dominant harmonics 5^{th} ,7^{th} and 9^{th} separately reach 0.3 %, 0.6 % and 0.47 % of the fundamental. These elevated harmonics overall result in an increased THD of 0.85 %.

One of the advantages of using a PR controller is its effective harmonic compensation at selected frequencies. By designing the harmonic compensator (HC) at these dominant harmonics (5^{th}, 7^{th} and 9^{th}), the improvements in harmonic performance are clearly shown in Figure 3.27.

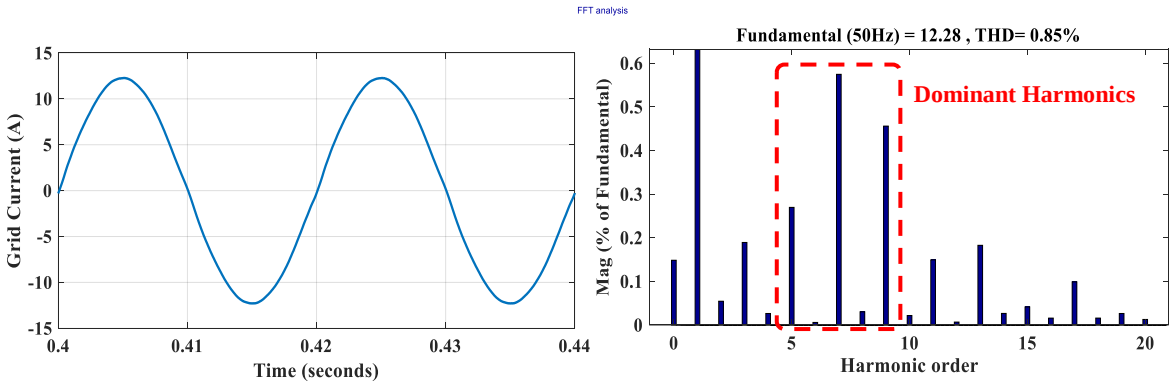


Figure 3.26 PR controller with real grid voltage model

The HC only compensates for the frequencies that are close to the selected harmonics, having no impact on the fundamental frequency. Therefore, the use of the PR controller with the HC greatly mitigates the designated dominant harmonics, leading to an improved THD of 0.36 % and a less distorted current waveform as shown in Figure 3.27.

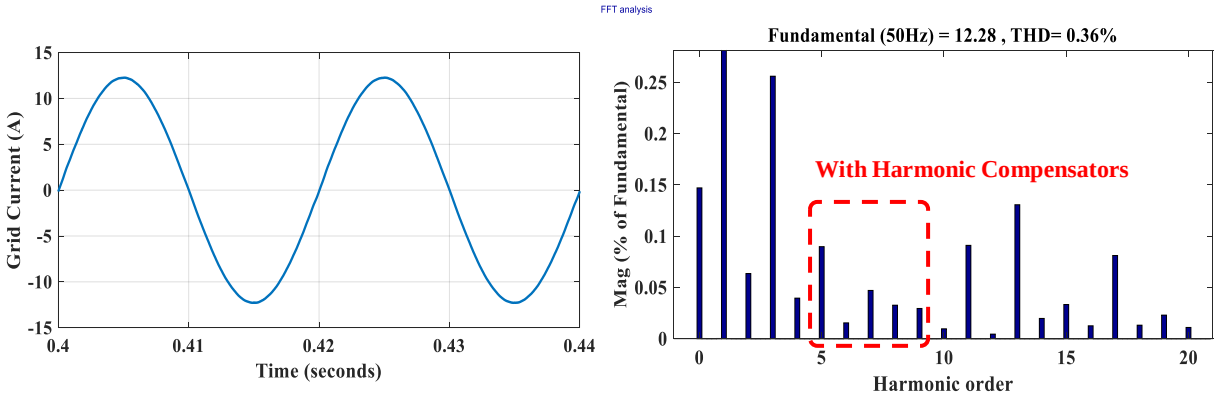


Figure 3.27 PR+HC with real grid voltage model

For comparison purposes, the results of the PI-based VSI simulation are also reported, based on the same parameters in Table 3.1. As shown in Figure 3.28, the dominant harmonics from the FFT analysis display the same trend as for the PR controller, which are separately confirmed as 0.4 % (5^{th}), 0.83 % (7^{th}) and 0.7 % (9^{th}) of the fundamental. These harmonics lead to a higher THD of 1.25 % and a more distorted current waveform. With a given reference of 12.3 A, the fundamental of injected current is confirmed as 12.32 A. Even though the results demonstrate the effective operation of the PI controller, the PR controller still shows a significant improvement in harmonics mitigation, especially when including the harmonic compensator.

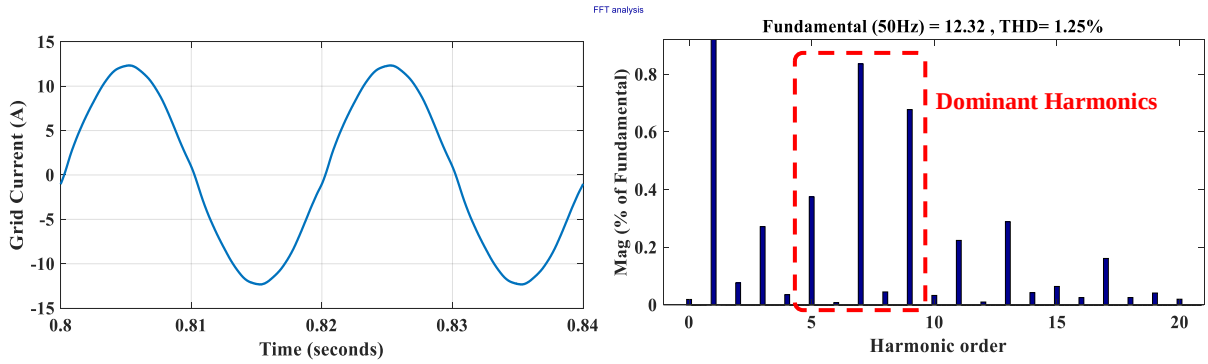


Figure 3.28 PI controller with real grid voltage model

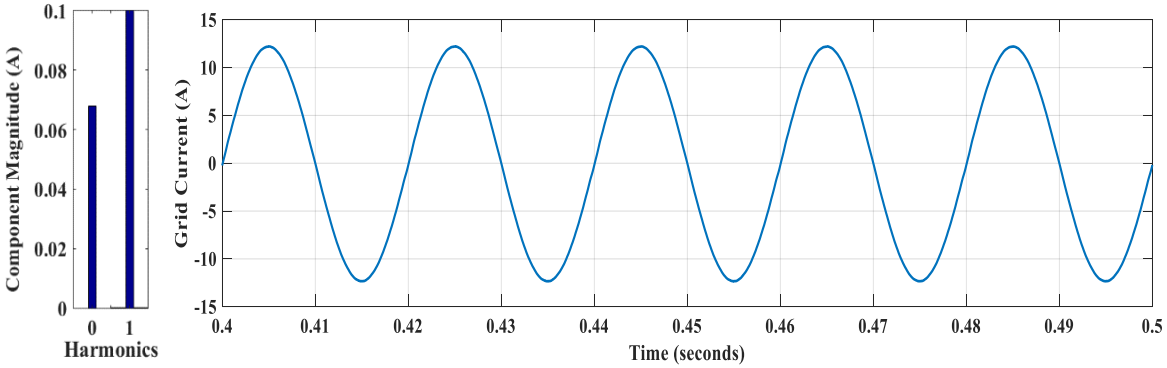
3.6.2 Simulation with Taking into Consideration DC Injection

The DC injection in the grid-connected VSI system can normally be attributed to several sources, such as the asymmetrical switching behaviour of the power switches, possible imparities in the gate drive signals, current controller errors, truncation errors during digital quantization, and offset drift in the conditioning circuit and current sensing devices [56],[69],[86],[74]. However, for the controllers that have a large gain at very low frequency (for example PI controller), the major cause of DC injection can be mainly summarized as non-ideal current sensing [144]. In this case, the controller is capable of compensating for DC injection in the output, as long as it is correctly sensed. This is still challenging, as the offset itself produces a DC component in the system output [96]. In contrast, controllers that have limited DC gain (such as PR controller) show poor performance in the mitigation of DC injection. Thus, the DC component in the output is sourced from the non-ideal operation of the inverter and the DC harmonics of the grid model. This has been validated by the results of FFT analysis shown in Figures 3.27 and 3.28, where more effective DC suppression is observed from the PI controller connecting to a real grid model (with 0.63 V DC harmonics). Furthermore, Table 3.2 below shows the sensitivity of DC injection to the non-ideal inverter and grid operation in the PR-based VSI simulation. Compared with the PI controller, which compensates for all the DC injection, an increase in the DC component is confirmed from the FFT analysis of the simulation by varying the operating conditions of the inverter and the harmonic profile of the grid.

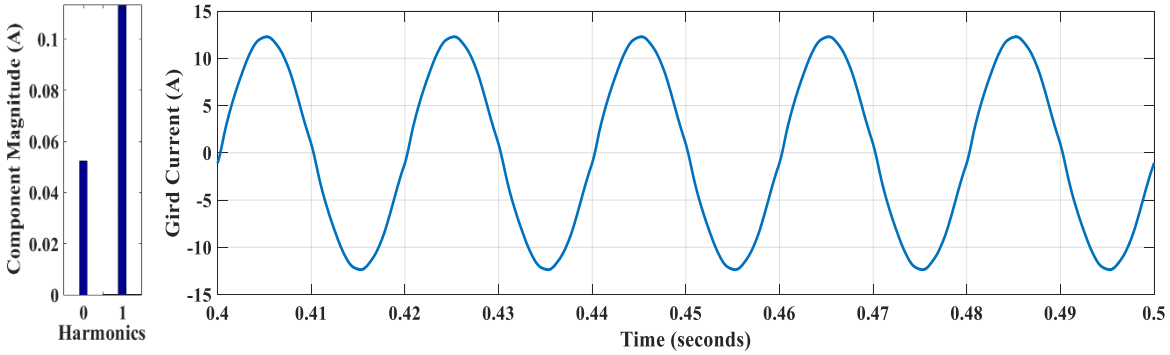
Table 3.2 Sensitivity of DC injection to the non-ideal inverter and grid operation

DC Sources	Parameter Variation	Change in DC Injection
Non-identical Voltage Drop	**0.5 V** Voltage Imbalance	**0.1%** of Fundamental
Different On-state Resistance	**0.05 Ohm** difference in a Switch	**0.03%** of Fundamental
Imparity on Gate Drive Signal	**50 ns** of Imparity Gate Signal	**0.08%** of Fundamental
DC Voltage in Grid Model	**0.5 V** Voltage in Grid Model	**0.1%** of Fundamental

Even for those controllers with a large gain at low frequency, the precondition of effective DC compensation depends on precise DC measurements. Unfortunately, sensing devices such as Hall Effect current sensors and circuits are prone to linearity errors and offset drift, which produce an extra amount of DC injection in the output. In the simulation, the offset error can be simulated by deliberately adding 50 mA DC to the sensor output. Figure 3.29 below shows the results of output current from the PR and PI controllers.



a. Output current and FFT analysis from PR controller



b. Output current and FFT analysis from PI controller

Figure 3.29 Results of grid current taking into consideration offset drift

It is virtually impossible to recognize any change from the output current waveform, due to the great difference in magnitude between the DC and AC components. However, the FFT analysis confirms the increase in DC injection with the offset error in the simulation. For the PR controller, this offset error simply adds to the previous DC injection, resulting in a DC magnitude of 68 mA. Meanwhile for the PI controller, the DC injection is around 50 mA. These results highlight the difficulty of achieving a DC-free sinusoidal output current from a grid-connected VSI, where even DC gain of the controller is large.

The current error in the controller can be calculated as the difference between the current reference I_{ref} and current measurement I_{gm}. With the sensor offset I_{offset}, the expression for current error I_{error} is given as:

$$I_{error} = I_{ref} - I_{gm} = I_{ref} - (I_g + I_{offset}) = (I_{ref} - I_{offset}) - I_g \quad (3.32)$$

where the I_g is the real output current. Consequently, from equation (3.32), the existing DC injection in the simulation can be equivalently replaced with DC onto the sinusoidal current reference. This is used throughout the simulations in the following chapters, providing validation for the proposed DC determination and suppression with a pre-known DC reference.

3.7 Summary

This chapter has investigated the control and operation of a grid-connected VSI system. For grid synchronization, the MMPD pPLL technique is selected, which has been proven to give improved dynamic performance and ripple reduction capability. As the power quality of injecting current depends on the controller and the output filter, the advantages of the PR controller and *LCL* filter in such a VSI system have been confirmed by investigating the gain distribution throughout the frequency spectrum. Following this, the mathematical model of the grid-connected inverter with an *LCL* filter has been developed. Based on the given system parameters, stability and sensitivity analysis have been performed according to the open-loop margins in the s-domain and closed-loop pole-mapping in the z-domain. From both sets of results, the proportional gain and resonant gain of the PR controller have been found to remain in a limited range which guarantees stable operation. Finally, the inverter system is simulated in Matlab/Simulink, and the results have been reported. By comparing the injected current connected to different grid models and controllers, an improvement in harmonics mitigation from the PR controller is confirmed.

Furthermore, regardless of the controllers that have been used, DC components are found in the output of the simulated VSI system with taking into consideration the non-ideal inverter's operating conditions, current sensing offset and the DC bias of the grid. Thus, in transformerless topologies, the potential risks of having DC injection flowing to the grid have been proven, and the need for DC mitigation methods in such topologies is significant to improve grid operating condition. Based on the theoretical analysis and simulation results, the following chapter illustrates an experimental implementation of the grid-connected VSI system and proposed solutions to DC injection issue.

Chapter 4 Implementation of Single-Phase Grid-Connected Inverter System

4.1 Introduction

This chapter presents the experimental hardware implementation and operating performance of the grid-connected H-bridge inverter system. The first part of the chapter illustrates the hardware arrangement and grid connection sequence based on the overall schematic diagram. The real-time control and data acquisition of the inverter unit are realized via the host computer connected to the control board. Following this, the parameters of the experimental inverter prototype are given. Based on the graphs of the test rig, the practical hardware arrangement, including controller platform, measurement circuits and auxiliary protection, are illustrated in detail.

The second part of the chapter presents the experimental results of the established inverter system. Before injecting any current into the network, the grid phase angle and frequency acquired from a software implemented PLL are verified. Subsequently, the output current and voltage waveforms when the inverter is separately operated by PI and PR controller at different power factors are presented. Based on the harmonic data given by the FFT analysis, the controller performance is fully evaluated. Finally, the DC injection issue in the inverter system is highlighted in this chapter, where the existence of DC components is confirmed in the controller by the FFT analyses and the specially designed DC measurement circuit.

4.2 Hardware Implementation of Grid-Connected VSI Test Rig

An experimental grid-connected inverter test rig is designed and developed to investigate power quality issues, and particularly, DC injection in the output current. As the inverter is practically implemented in the laboratory and connected to the utility grid, a DC measurement circuit is utilized to confirm the presence of DC current components. Meanwhile, auxiliary protection is required in the experimental system to prevent the DC from being injected into the main grid supply. In addition, the verification of the proposed DC mitigation methods is required in this low-power prototype. Hence the hardware arrangement and implementation are carefully designed.

4.2.1 Overall Experimental Setup

Figure 4.1 shows the schematic diagram of the experimental system, including the hardware connection sequence, sensing devices and measurement circuit, real-time control implementation, and auxiliary protection. The MOSFET H-bridge inverter is operated from the DC power supply via DC link capacitors, and connected to the grid via the *LCL* filter, a variac and an isolation transformer. Although the research focuses on the transformerless topology, since the inverter system is connected to the utility grid, the presence of DC injection during the experiments would potentially threaten the sensitive equipment connected to the same common coupling point. Thus, an isolation transformer is employed purely for protection purposes. In this way, the DC current injection can still be monitored at the inverter side but will have no impact on the grid. The variac inserted before the isolation transformer is used to match the voltage of the grid connection point to the operating DC link voltage. Such an arrangement allows for low-voltage experiments under grid-connected conditions.

In addition to the measurements of grid voltage and output current used for grid synchronization and current control, two more measurements are taken in the experimental system, namely the current flowing through the DC link and the voltage from the passive attenuation circuit. These measurements are separately used for determining the DC injection in two proposed DC mitigation methods, which will be introduced in the following chapters. All the measurements are sampled by the analogue-to-digital converter (ADC) and are processed by the control algorithms in the digital signal processor (DSP) unit. The desirable PWM outputs are interfaced with the gate drive circuit via the general control board (GCB), operating the MOSFET H-bridge at switching frequency. The control algorithms are written in the C language, which are downloaded to the DSP via Texas Instruments™ Code Composer Studio (CCS) Version 6.2. To implement real-time control and data acquisition, a host computer is connected to the general control board via an external XDS100v2 JTAG emulator, and communication is based on a graphical user interface (GUI) coded in Matlab.

The auxiliary contactor circuits are also designed and installed in the experimental inverter system. These protective contactors are fully operated by the switchgear, providing safe and flexible testing conditions. In addition, an external shunt resistor with an RC circuit is employed at the inverter output for the purpose of monitoring the DC current component.

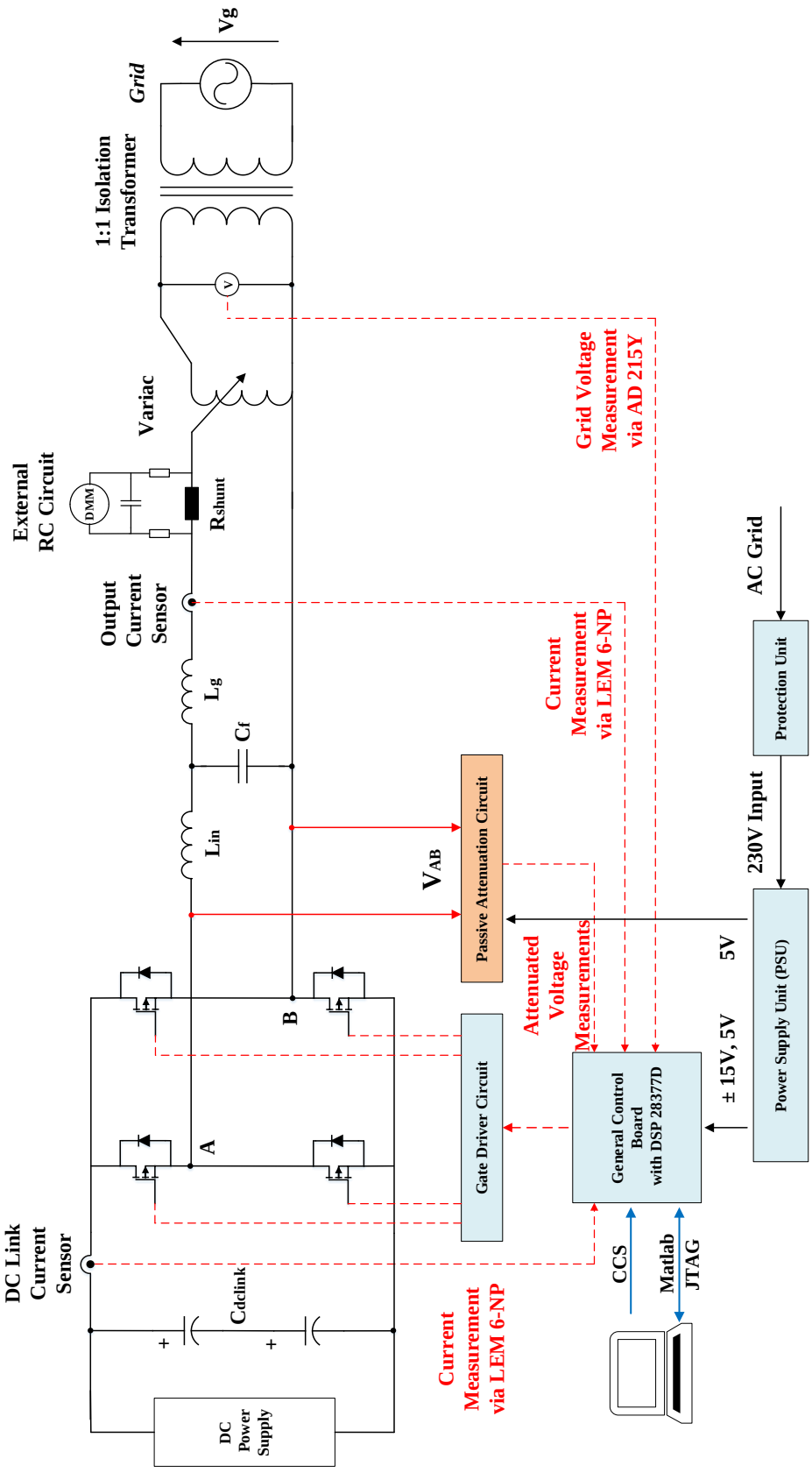


Figure 4.1 Schematic diagram of experimental system

The experimental inverter prototype operates from a 50 V DC power supply, at a switching frequency of 20 kHz and fed into the 230 V utility grid through a variac with a connection voltage of 35V and an isolation transformer. A summary of the key system parameters is presented in Table 4.1.

Table 4.1 Experimental system parameters

Parameters	***Value***
DC Link Voltage, V_{DC}	50 V
Rated Power, P_{rate}	200 W
Grid RMS Voltage, V_g	230 V
Voltage at Vpcc, V_{pcc}	35 V
Grid Frequency, f_g	50 Hz
Switching Frequency, f_{sw}	20 kHz
Sampling Frequency, f_s	20 kHz
Controller Sample Time, T_s	5×10^{-5} s
DC Link Capacitors, C_{dclink}	2200µF
Inverter-side Inductance, L_{in}	0.6 mH
Grid-side Inductance, L_g	0.1 mH
Filter Capacitance, C_f	10 µF
Shunt Resistor, R_{shunt}	0.1 Ω
Cut-off Frequency of External DC Measurement Circuit, f_{cEMC}	0.35 Hz
Parasitic Resistance of Test Rig, R_p	0.36 Ω
Resistors in Attenuation Circuit, R_s	72 kΩ
Capacitors in Attenuation Circuit, C_s	10 µF
Cut-off Frequency of Passive Attenuation Circuit, f_{cut}	0.22 Hz

4.2.2 Test Rig Setup

The experimental single-phase grid-connected inverter system has been established in the Electrical Power (EP) Laboratory at Newcastle University. Figure 4.2 shows an overview of the inverter test rig, where the hardware units are connected in the same order as in the schematic diagram via 4 mm shrouded safety test leads. For safety reasons, the inverter unit and control equipment are enclosed in a safety box. The switches on top of the enclosure separately operate the connection of the DC side and AC side, and the connection status is indicated by the green lights. An emergency button is also in placed to allow the system to be immediately shut down when any fault occurs.

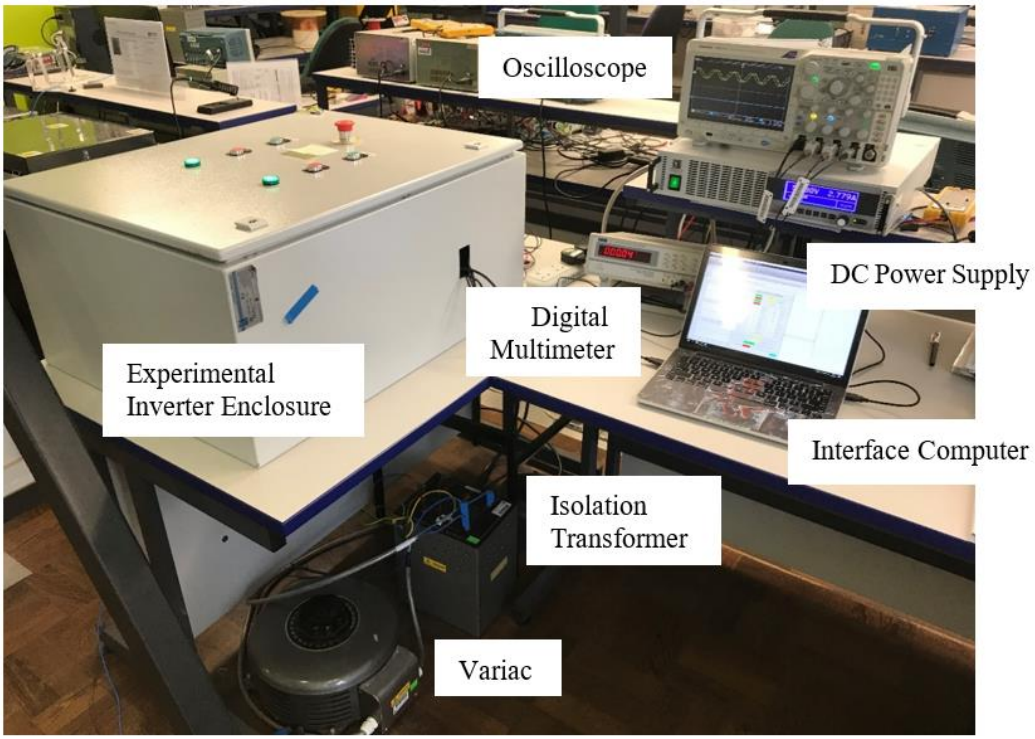


Figure 4.2 Overall experimental set-up

Figure 4.3 shows the internal layout of the safety enclosure, where the H-bridge inverter, *LCL* filter, control equipment, sensing devices and auxiliary protections are clearly observed. Since their connection sequence and arrangement have been explained in the schematic, the following sections focus on the design and functionality of the individual parts.

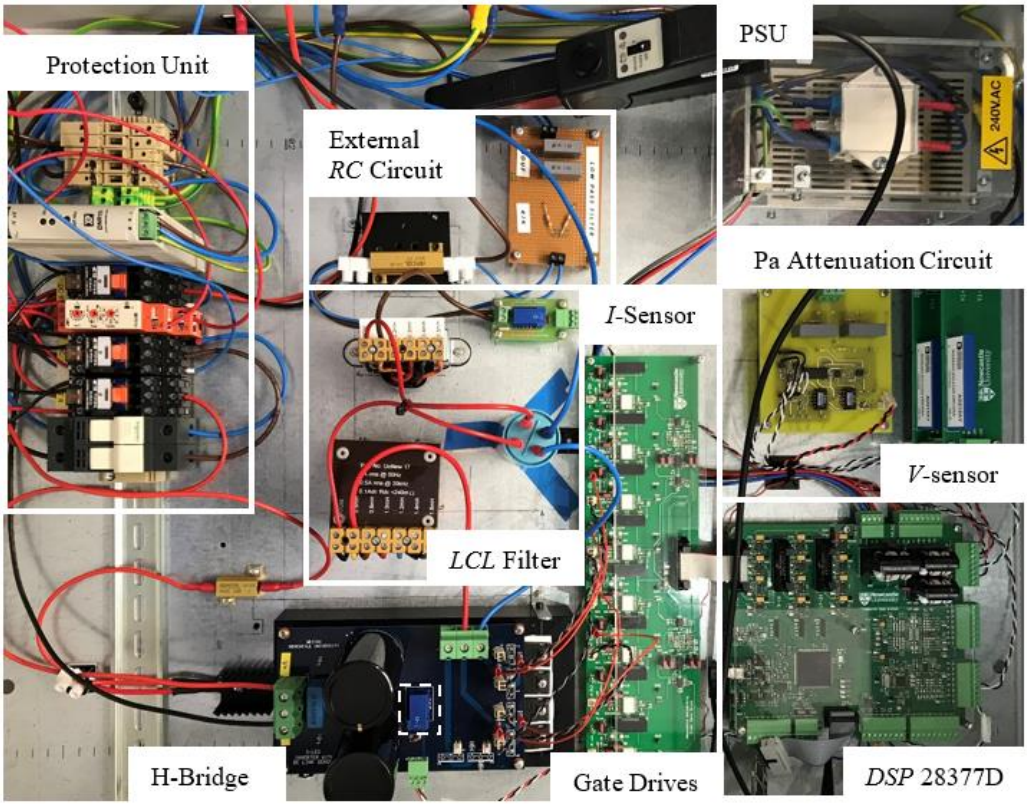


Figure 4.3 Internal layout of inverter enclosure

The experimental H-bridge inverter is carefully designed with a DC link that consists of two series-connected 2200 µF/250 V electrolytic capacitors. This structure halves the voltage rating of the DC link capacitor and therefore reduce the size and cost. Each capacitor has a parallel-connected 150 kΩ resistor, which prevents voltage imbalance if one of the capacitors fails. In addition, a 150 nF ceramic capacitor is placed across the DC link to remove high-frequency oscillations. Since Silicon Carbide (SiC) MOSFETs have improved switching characteristics over Silicon MOSFETs, the inverter employs four C3M0120090D SiC power MOSFETs as switching devices. Besides that, a current sensor, the LTS 6-NP, is designed at the positive DC link to determine the DC injection. This would potentially compromise the desirable low inductance layout of the power circuit. Hence, a bus bar with laminated structure has been incorporated into the DC link rails to minimize the stray inductance in the commutation loop [145]. In this structure, the positive DC link layer is split by a narrow gap and re-connected via the DC link current sensor. The use of the laminar bus bar minimizes the effect of the inclusion of the DC link current sensor and optimizes inverter performance. The schematic design of H-bridge and its PCB layout are shown in appendix C.

An *LCL* filter is connected to the inverter output, the parameters of which are determined using the procedure described in Chapter 3 and listed in Table 4.1. The output current measurement from the

filter is taken via a Hall effect transducer LTS 15-NP, whilst the grid voltage measurement is taken across the isolation transformer via an isolation amplifier AD215Y. The measurements are then fed into a general control board (GCB), where a 32-bit floating-point microcontroller unit (MCU) Texas Instruments™ TMS320F28377D is utilized for processing the control algorithms. As the F28377D has four 12-bit analogue-to-digital converter (ADC) modules with separated voltage reference input, there are twelve analogue inputs designed in the GCB for the collection of the sensor measurements. In addition, the digital-to-analogue converter (DAC) output is also utilized for the real-time monitoring of the processing parameters from the MCU on the oscilloscope. The GCB board is capable of making up to twelve pairs of PWM outputs, where every four pairs are interfaced with an eight-gate-drive board (EGDB) via a 14-way ribbon cable. The gate drive circuit allows for the independent or complementary operation of each pair of PWM outputs. In this project, the unipolar modulation scheme only requires two pairs of PWM outputs to operate the four switches in the H-bridge.

As mentioned in the schematic diagram in Figure 4.1, the experimental inverter test rig employs a 0.1ohm shunt resistor on the output path to monitor the DC current component. A simple RC circuit with a cut-off frequency of 0.35 Hz is connected across this resistor. The filter output voltage, to all intents DC, is measured by an isolated digital multi-meter (DMM). To note that this external shunt RC circuit performs no part of the control scheme and is used purely for evaluation purposes.

4.2.3 Passive Attenuation Circuit

Figure 4.4 shows the prototype of the passive attenuation circuit which is designed primarily for DC voltage determination. The determination process will be fully illustrated in Chapter 5. The attenuation board is directly connected to the inverter output and powered up by the GCB. The mounting scheme of the passive attenuator RC circuit is designed as the through-hole type, and therefore the resistors and capacitors can be easily replaced when the board is connected to different power applications. Here, the values of the resistor and capacitor are selected to be 72 $k\Omega$ and 10 µF, resulting in a cut-off frequency of 0.22 Hz. For the purpose of achieving safe and accurate voltage measurements, the input and output of the passive attenuation circuit are separately powered by two isolated DC/DC converters and galvanically isolated by a capacitive isolation amplifier ISO124. The attenuated AC voltage is then sensed and shifted with a 1.5 V DC reference to fit in the ADC input range 0-3 V. By feeding these two voltage measurements to the GCB, the

attenuated output is then restored in the software. The schematic in appendix C clearly presents the arrangement and connection of the RC attenuator, voltage measurement amplifiers, isolation and output protections.

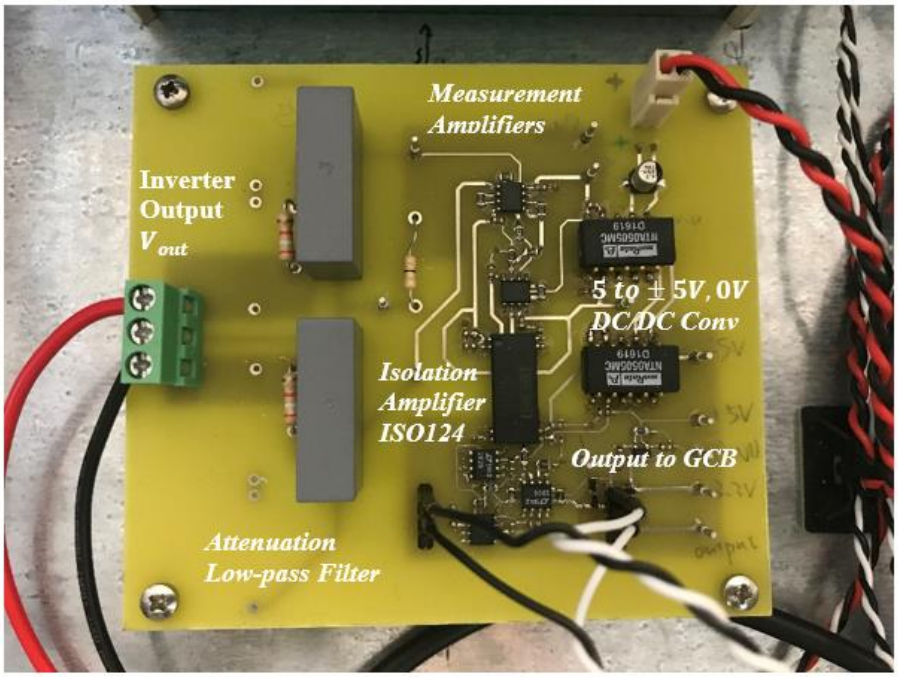


Figure 4.4 Passive attenuation circuit

4.2.4 Protection Design

Besides the transformer used to provide galvanic isolation between the experimental system and grid, an auxiliary protection unit is designed and installed to guarantee the safety of personnel and power components such as Sic MOSFETs and DC link capacitors. Figure 4.5 shows the schematic of the protection circuit, where the fuses and an emergency stop button are placed on the main power path. These can be used to automatically disconnect or manually shut down the experimental system in case of any emergency. The connections of the DC power supply and AC grid to the inverter are operated by the switchgear circuits and DC relays. Furthermore, a pre-charge resistor in series with the DC link input is employed to limit the inrush current when the system is first turned on. With the use of a timer and a relay, this resistor is then disconnected from the main circuit after a time delay of 8 s. A blocking diode is also placed alongside the resistor to prevent the reverse current flowing into the DC power supply. Figure 4.6 shows the experimental arrangement and connection of the protection unit.

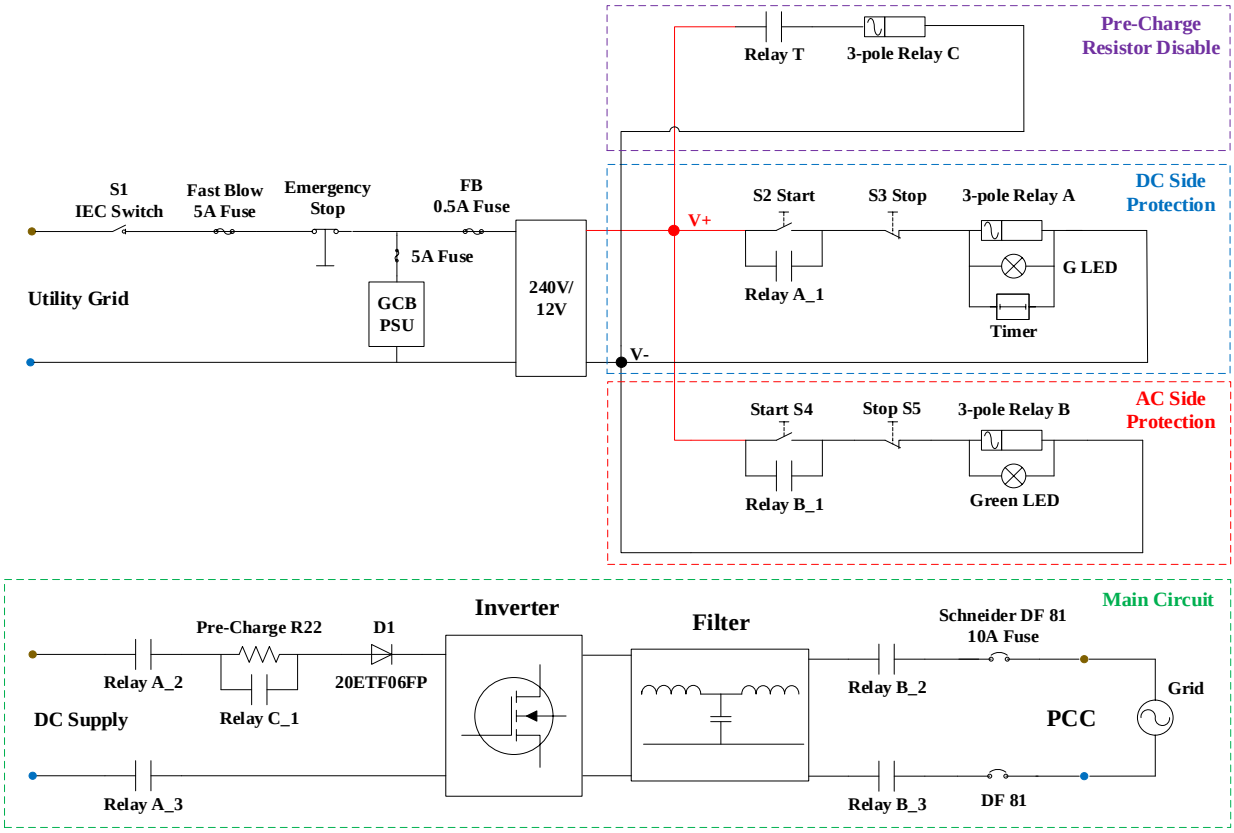


Figure 4.5 Schematic diagram of the protection unit

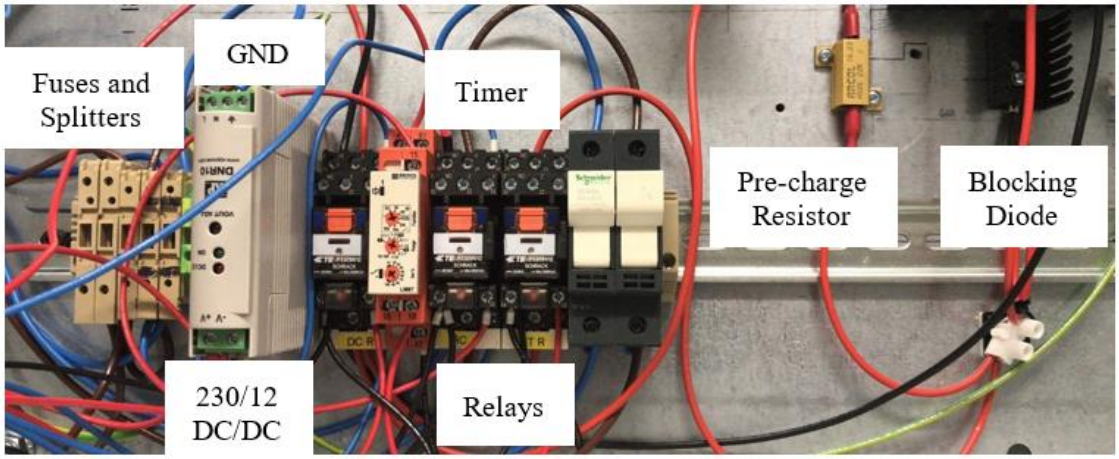


Figure 4.6 Experimental protection unit

4.2.5 Real-time Graphical User Interface

Real-time control and data acquisition are realized by connecting the F28377d-based GCB with a host PC that runs the graphical user interface (GUI). The interface is coded in MATLAB containing a number of widgets, as shown in Figure 4.7. Three identical graphical axes on the left are used to display the data collected in the data store arrays s1-s8. Each graphical axis has a pop-up menu to select a data array, which is essential as it enables the graphical axis to monitor any parameter within the software. The push-buttons at the top right are used to activate and deactivate the operational conditions on the target board and to initialize the data storage process. These operations can be indicated by the indicators at the side. Below the push-buttons, there are two columns of data boxes which are used to display the numerical data such as sensor measurements and loop counts whilst the target is running. The sliders at the bottom right are used to send data to the target. At present, two sliders are set up to change the current demand from 2 A to 7 A and DC reference from 0 mA to 100 mA. The other two sliders are used as switches to operate the H-bridge in different control schemes.

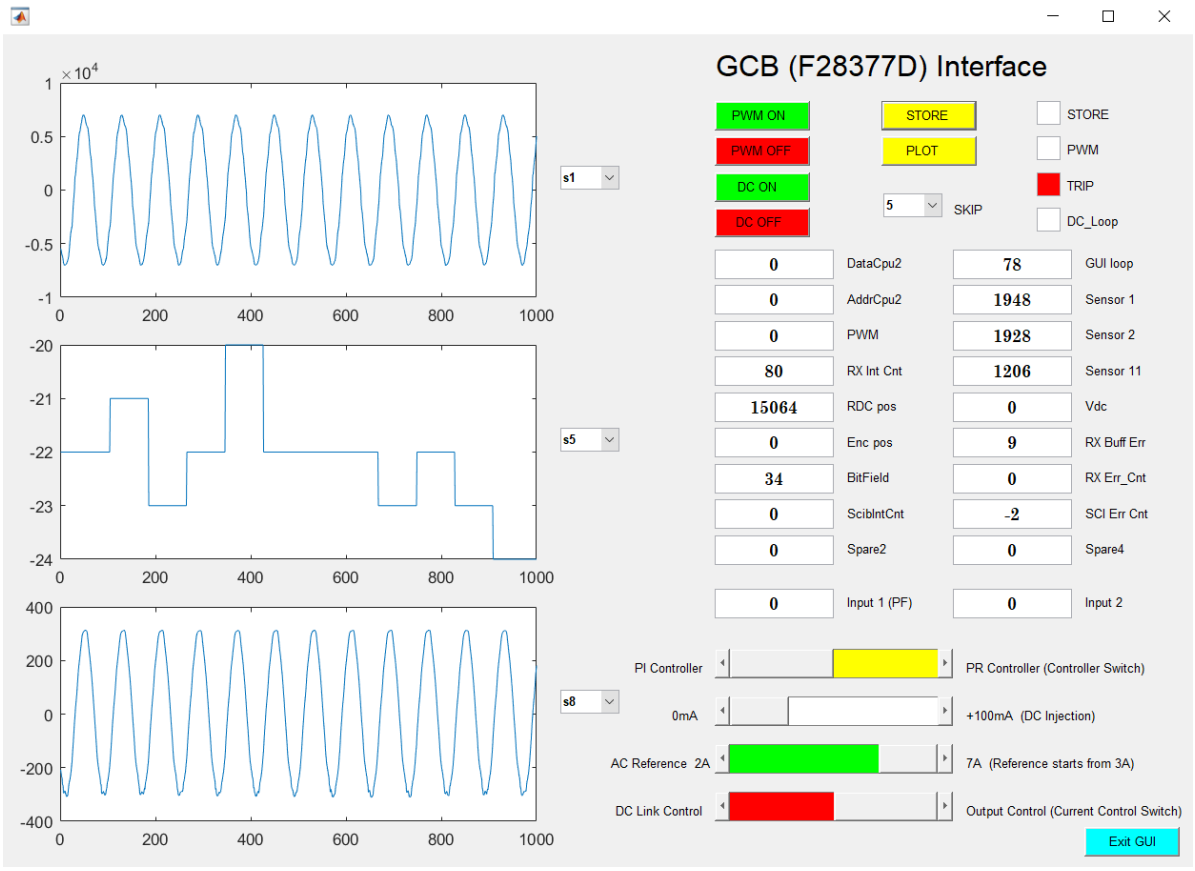


Figure 4.7 MATLAB GUI appearance

4.3 Experimental Results for Single-Phase Grid-Connected PV System

This section presents the results for the developed experimental inverter system based on the PI and PR controller. The inverter functionality is confirmed by the operating current and voltage waveforms, whilst the harmonic performance is investigated via an FFT analysis of the injected current. Furthermore, the DC injection issue is first evaluated from harmonics data at different operating conditions. Then, the exact DC current component in the experimental system is recorded using the external RC circuit.

4.3.1 Performance of Grid Synchronization

Before injecting any power to the utility grid, the grid information is required in order to operate the experimental inverter appropriately at the desired condition. As the grid voltage measurement is readily available in the microprocessor, grid synchronization can be digitally realized based on the modified mixer phase detector (MMPD) pPLL. In the simulation, this technique has been proven with the advantages of fast responses and double-harmonic reduction. Figure 4.8 shows the experimental results of the MMPD-based pPLL, where the grid current is correctly synchronized to the grid voltage at the unity power factor.

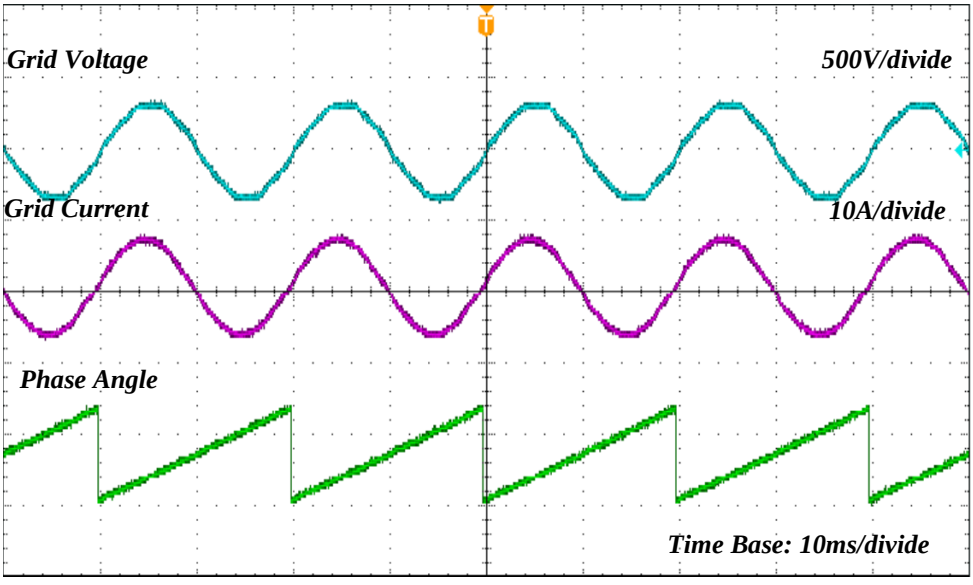


Figure 4.8 Grid synchronization

4.3.2 Operation of PI Controller at Different Power Factors

The inverter is first controlled via a PI controller with the gain parameters carefully tuned as proportional gain $K_p = 0.1$ and integral gain $K_i = 0.045$. For a given current demand of 7A, Figure 4.9 shows the inverter's operational performance at unity power factor. The sinusoidal output current is injected to the grid with respect to the voltage of the common coupling point (V_{pcc}). Meanwhile, the inverter output voltage is also recorded, which consists of 50 V PWM voltage pulses at doubled switching frequency. Since the inverter is operated from a unipolar scheme at a unity power factor, these voltage pulses have the same polarity as the grid current during the positive and negative periods.

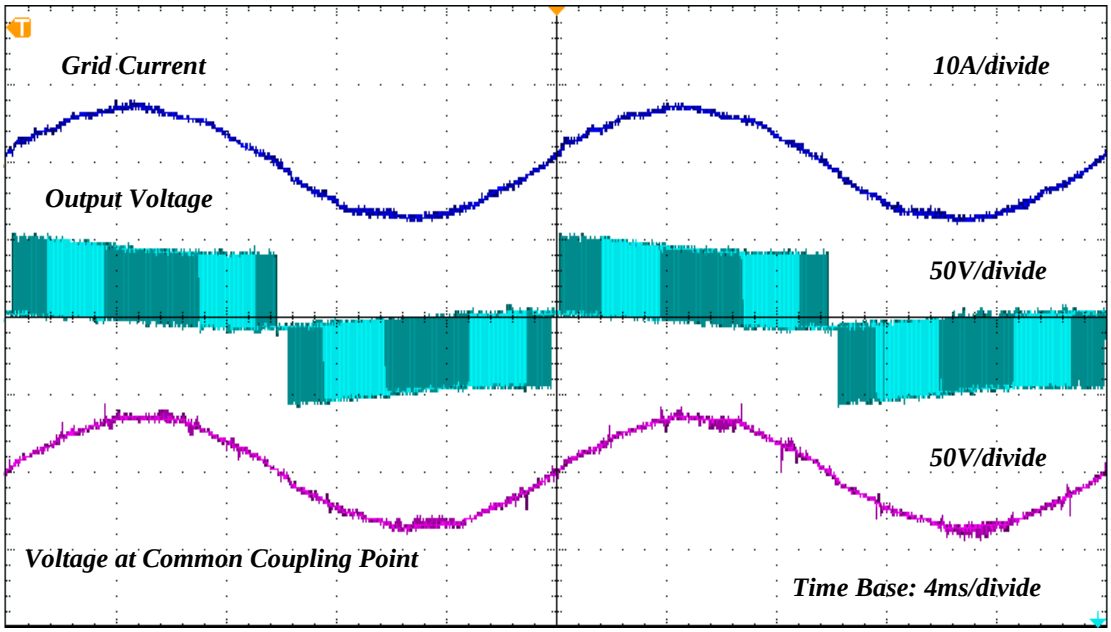


Figure 4.9 PI operation at unity power factor

By knowing the phase angle of the grid from the PLL, the inverter can be operated at a non-unity power factor to provide reactive power compensation. Figure 4.10 shows the inverter operation at a power factor of 0.9, where a phase shift is clearly observed between the injected current and the V_{pcc}. Meanwhile, there are portions of output voltage pulses that have the opposite polarity to that of the grid current. Except for the phase shift, the injected current exhibits a similar waveform to that of with the unity power factor. The results of the PI controller verify the operating performance of the experimental inverter at different power factors.

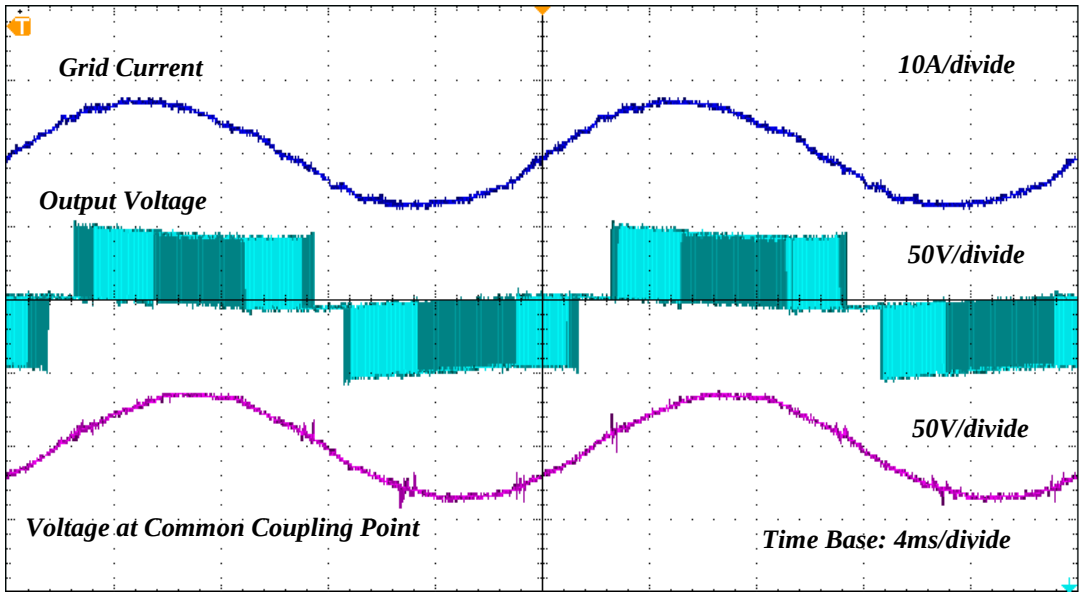


Figure 4.10 PI operation at power factor of 0.9

4.3.3 Operation of PR Controller at Different Power Factors

By applying the same current demand, the inverter is controlled via a PR controller. The controller parameters are tuned as proportional gain $K_p = 0.15$, resonant gain $K_r = 180$ and bandwidth $\omega_c = 5\,rad/s$. The operating current and voltage waveforms in Figures 4.11 and 4.12 present similar results to those of PI controller, thus verifying the performance of the PR controller at different power factors.

However, it can be observed that the experimental current waveforms for both PI and PR controller are more distorted compared with the simulation results, especially around the zero-crossing sections of the modulation index. This is due to the non-ideal characteristics of the experimental inverter and important protective techniques that have been applied; in particular, the dead-time. Such operational implementations cause additional high-order harmonics and an increase of the THD in practice. Based on the results for the PI and PR controllers, the following section investigates the harmonic performance of the injected current at different power factors.

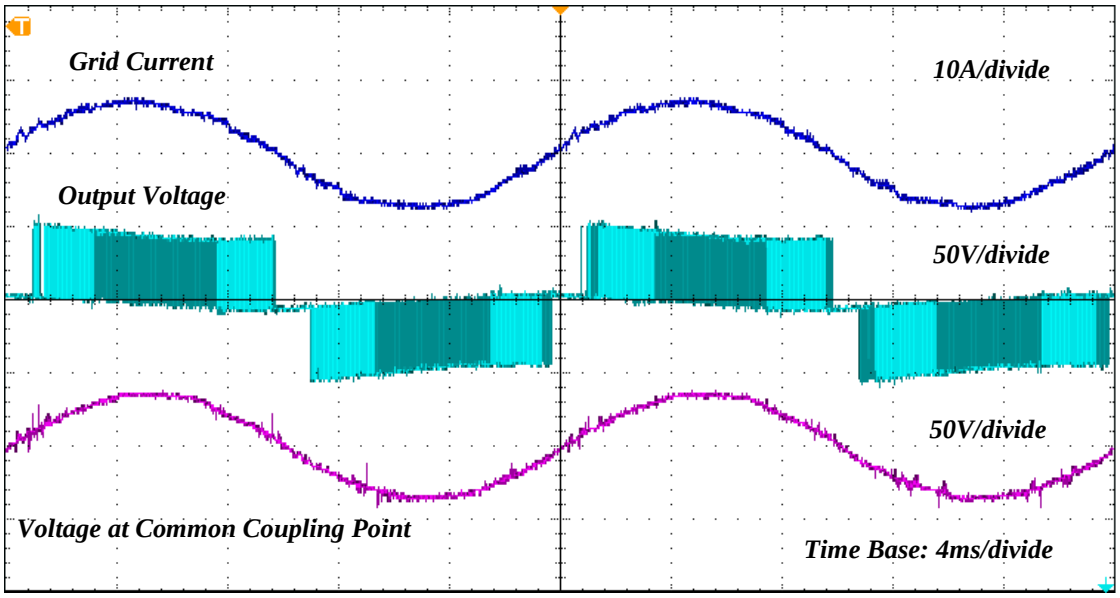


Figure 4.11 PR operation at unity power factor

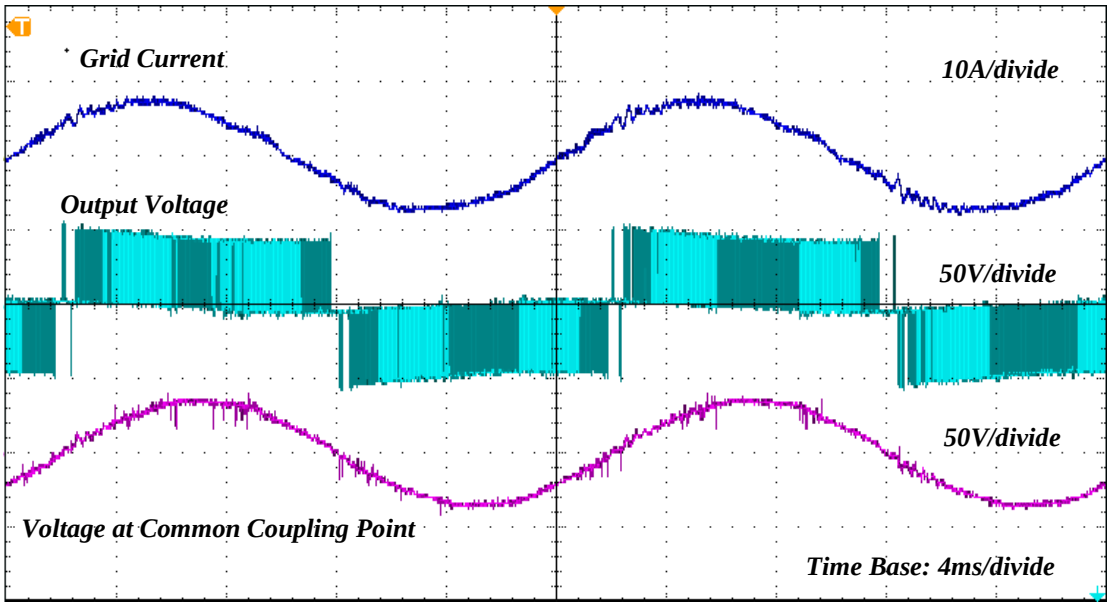


Figure 4.12 PR operation at power factor of 0.9

4.3.4 THD Requirements and Comparison

The total harmonics distortion (THD) and current harmonic injections are specifically limited in the guidelines and recommendations for grid-connected systems [63-67]. Table 4.2 shows the commonly adopted IEEE standard for interconnecting distributed resources to the grid network, where the odd harmonics of injected current shall not exceed the limits stated below [67, 68].

Table 4.2 Maximum harmonic current distortion in percent of current

Individual Harmonic Order h (odd harmonics)	$h < 11$	$11 \leq h \leq 17$	$17 \leq h < 23$	$23 \leq h < 25$	$35 \leq h$	***Total demand distortion (TDD)***
Percent (%)	***4.0***	***2.0***	***1.5***	***0.6***	***0.3***	***5.0***

As the sensor measurements in the GCB board are digitally collected by data store registers, the measurement data can then be transmitted from the microprocessor to the Matlab workspace via the GUI interface, which allows for further FFT analysis using Matlab/Simulink®. Figure 4.13 shows the harmonic distribution of injected current with the application of the PI and PR controllers.

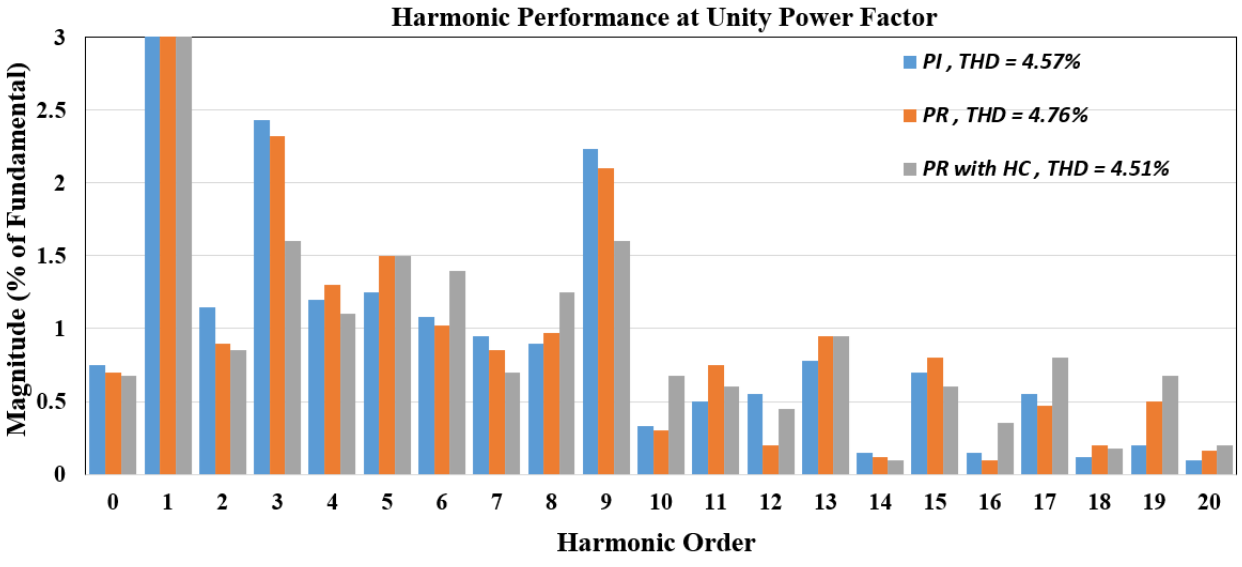


Figure 4.13 Harmonic performance at unity power factor

From the harmonic performance at unity power factor, the THD and harmonics of the injected current meet the stated standards with a THD of 4.57% from the PI controller and 4.76% from PR controller. The figure shows the magnitude of all harmonics between the DC and the 20th harmonic, in which the dominant ones appear at the 3rd and 9th harmonics, reaching 2.4% and 2.2% of the fundamental. By employing the compensators at the 3rd and 9th harmonics, control based on the PR with the HC shows a mitigated harmonic at the selected frequencies and an improved THD. Consequently, although the difference in using PI and PR controller can barely be recognized from in current waveforms, the advantage of the PR controller in harmonic mitigation is validated from the FFT analysis, especially with the inclusion of the 3rd and 9th harmonic compensators.

In addition, certain amount of DC current injection exists with all control methods. From the previous analysis, it is known that the DC injection comes from the non-ideal operation of the inverter unit and errors in current sensing. However, the quantification of DC injection from specific sources is not fully understood. According to the IEEE standard, the DC current of an individual inverter is limited to 0.5% of the full rated output current [68]. For transformerless topologies, even stricter regulations are established in some countries (shown in Table 2.1) since the cumulative effect of DC injection from multiple transformerless inverter installations would adversely affect grid operation. Therefore, the harmonic performance of the injected current indicates a severe DC injection issue in the experimental inverter system, where the DC component reaches 0.7% from the PI controller and 0.6% from the PR controller.

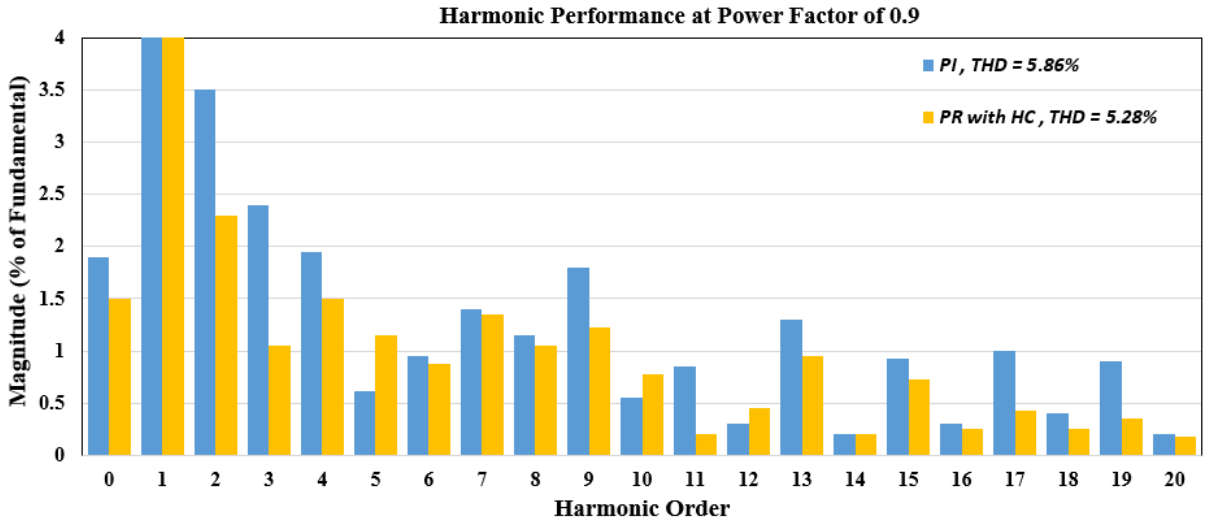


Figure 4.14 Harmonic performance at power factor of 0.9

The harmonic performance of the injected current at a power factor of 0.9 is shown in Figure 4.14, where the PR controller achieves an improved THD with a perceptible mitigation of the dominant harmonics. Besides this, there is a substantial increase in the DC component compared with that in the analysis at unity power factor, reaching 1.5% for the PR and 1.9% for the PI controller. Consequently, DC injection remains a significant concern in non-unity power factor operation.

4.3.5 DC Current Injection of the Experimental Inverter System

To investigate the exact DC current injection at the inverter output, the DC component is filtered by the external shunt RC circuit and measured via an isolated digital multi-meter (DMM). By operating the inverter unit with an increasing current demand, Figure 4.15 summarizes the DC measurements using the PI and PR controllers at different power factors. It is shown that the magnitude of DC injection escalates with the increase in inverter power in all situations, particularly, this is true at non-unity power factor, where the DC components exhibit greater magnitude with faster growth. Moreover, owing to the difference in DC gain, an evident DC variance is observed when applying the PI and PR controllers. The measurements from the external RC circuit match the results of the prior FFT analysis, which also confirms the DC injection issue in the experimental inverter system.

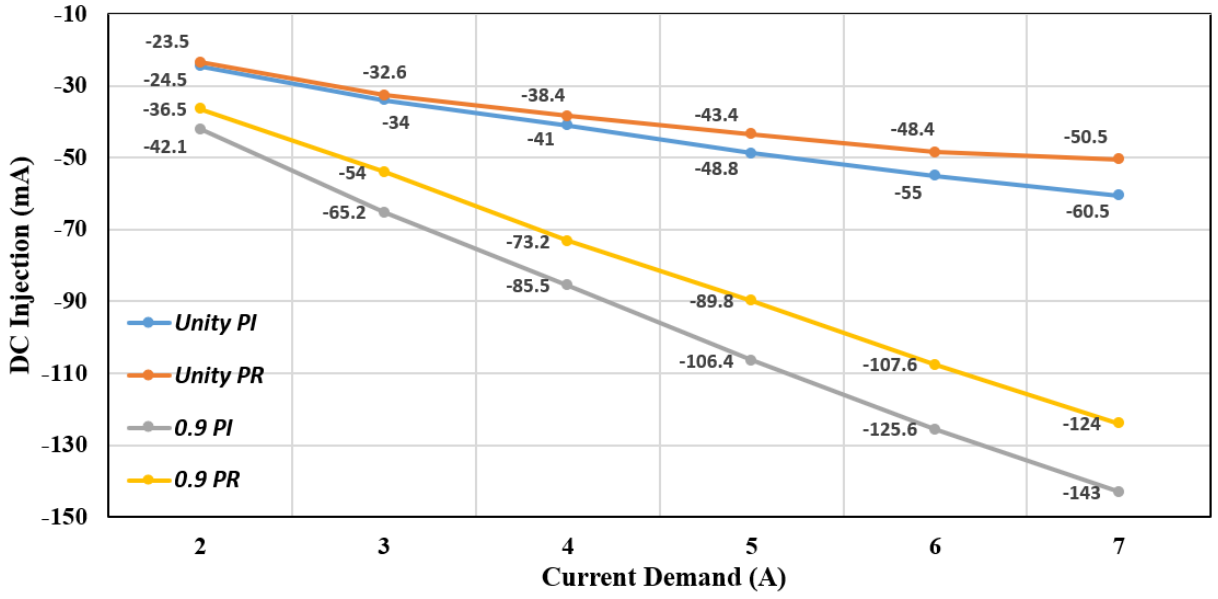


Figure 4.15 DC injection with controllers at different PF

4.4 Summary

This chapter has illustrated the implementation of the experimental grid-connected inverter system. Based on the schematic diagram and the layout of the test rig, the hardware arrangement, connection sequence and auxiliary protection are clearly presented. The designs of the key components, such as the inverter with a DC link current sensor and the passive attenuation circuit, are described in detail. Based on the developed inverter system, the experimental results using the PI and PR current controllers are presented. The FFT analyses confirm that the PR controller gives improved harmonics mitigation and advanced THD performance. Most importantly, the FFT analyses and measurements from the external RC circuit have proven that the experimental grid-connected inverter system suffers from severe DC injection issues. Since the DC injection cannot be improved by conventional controller, DC suppression methods are investigated in the forthcoming chapters.

Chapter 5 Mitigation of DC Current Injection in Transformerless Grid-Connected Inverter Using a Voltage Filtering DC Extraction Approach

5.1 Introduction

Previous chapters have revealed the DC injection issue in both simulated inverter models and experimental systems. As an increasing number of low-power transformerless PV applications are being connected to the distribution network without galvanic isolation, the cumulative DC injection into the grid from individual inverters is of significant concern. As already stated, most published DC suppression techniques suffer from challenging issues either in implementation or accuracy. This chapter investigates a voltage filtering DC extraction approach to mitigate the DC current injection in grid-connected VSI systems. The approach employs an isolated RC attenuation circuit and a software filtering algorithm to facilitate the DC voltage extraction at the inverter output. From the detected DC voltage, DC current injection is mitigated through an active DC suppression loop. The principle and advantages of the proposed method are first fully illustrated, following this the effectiveness and performance of the DC determination and mitigation is validated via simulation and experimentations.

5.2 Overview of DC Voltage Migitigation Approach

Typically, the single-phase inverter output is a 380-400V PWM frequency switching waveform that is connected to the grid via an output filter. Due to the non-ideal semiconductor characteristics and asymmetrical inverter operations stated in chapter 2, the PWM waveform of the inverter output also contains a minimal DC voltage offset (in millivolts scale), which originated from the DC current injection and parasitic resistance of the system. Put simply:

$$V_{DC} = I_{DC}\left(R_e + R_g\right) \tag{5.1}$$

where R_e and R_g are the values of ESR of the filter and grid respectively.

Figure 5.1 shows a block diagram of a typical transformerless inverter with the proposed DC suppression method. Whilst the classic current control loop maintains the general operation of the inverter, an extra closed-loop to suppress the DC voltage offset is integrated into the feedback path. DC detection consists of a passive attenuation circuit directly connected to the inverter output and a digital filtering algorithm. The passive attenuation circuit reduces the AC voltage component to the nominal ADC voltage input but, importantly, without suppressing the DC component. To achieve this, a low cut-off frequency is required, and this results in the DC component becoming a more significant element in the filter output. The filter output voltage is then digitized and presented to the microcontroller. With a much smaller AC/DC component ratio, the software filtering stage is implemented on the microprocessor to accurately extract the DC voltage component found in the inverter output voltage. The following sections describe the rationale and design considerations for the passive attenuation circuit and software filtering algorithm.

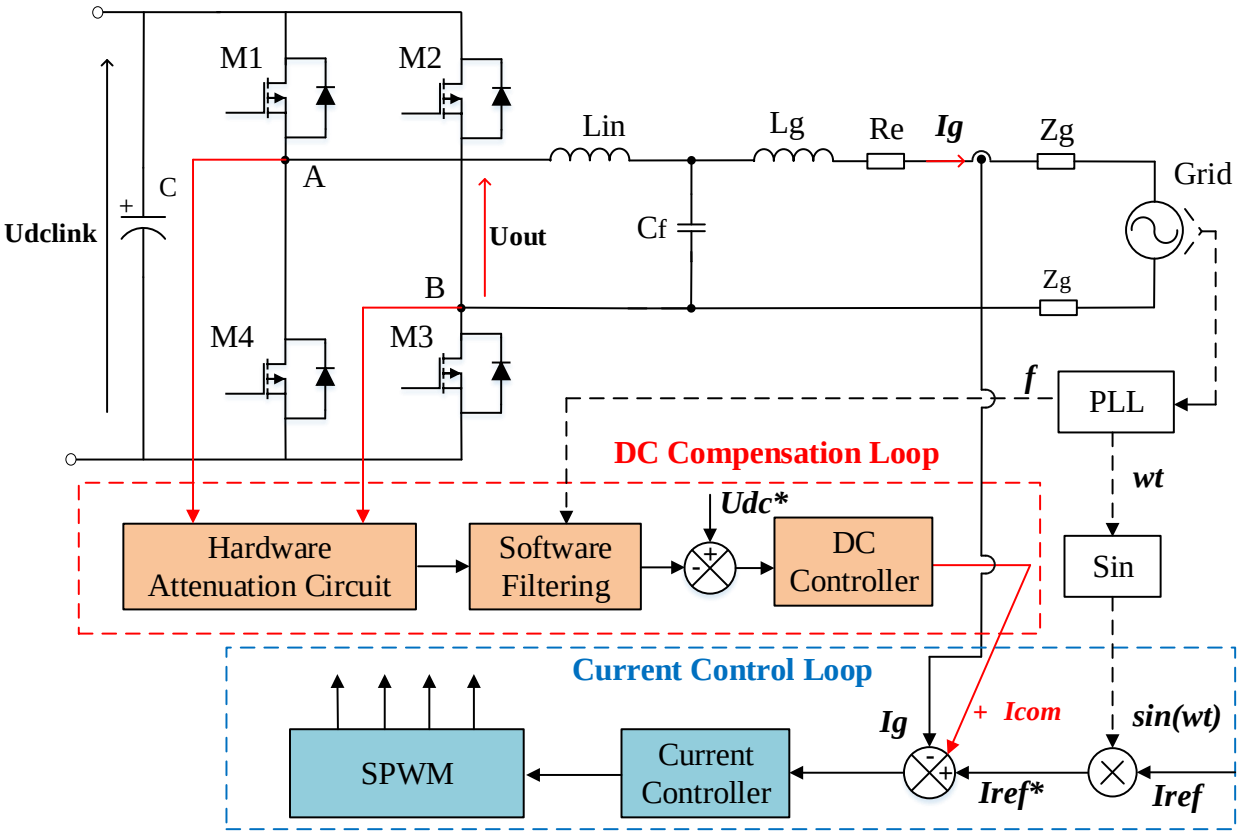
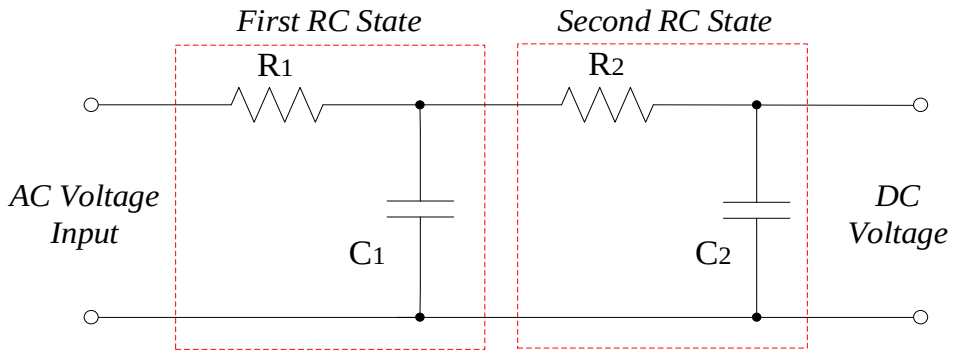


Figure 5.1 Diagram of proposed DC mitigation in transformerless grid-connected VSI

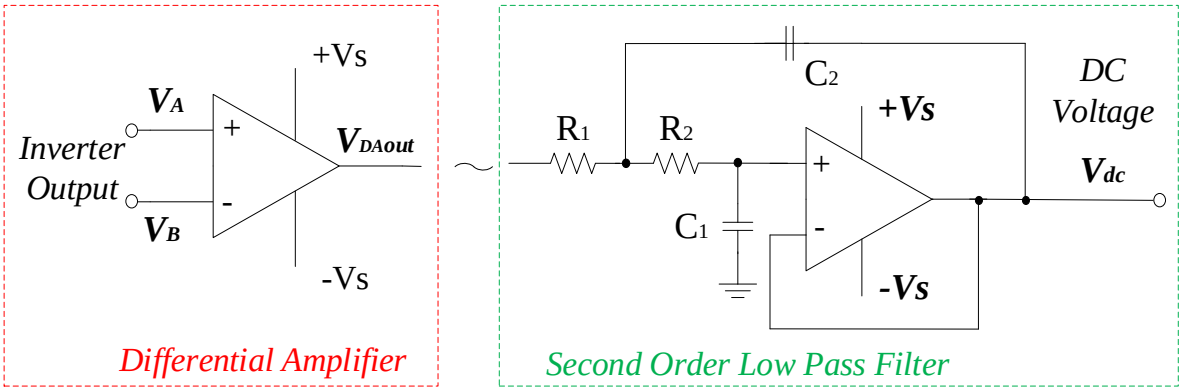
5.2.1 Passive Attenuation Circuit

The RC low-pass filter is a simple and effective way of removing AC signals whilst preserving the DC component of the input signal. In previous studies, with an appropriate cut-off frequency, a traditional second order low-pass filter as shown in Figure 5.2(a) is capable of achieving a small DC voltage across the second stage capacitor C_2 [85], [84]. This is a hardware-only solution, where the AC content cannot be completely eliminated by the LPF, and a very low cut-off frequency and consequently bulky components are needed. Moreover, the high common-mode voltage across the capacitor results in problems with interfacing with the digital controller hardware. A simple and low-cost voltage divider can be used to overcome this problem; however, this is not a particularly robust solution. It also adds a further stage to the process, and therefore represents an additional source of potential loss of accuracy.

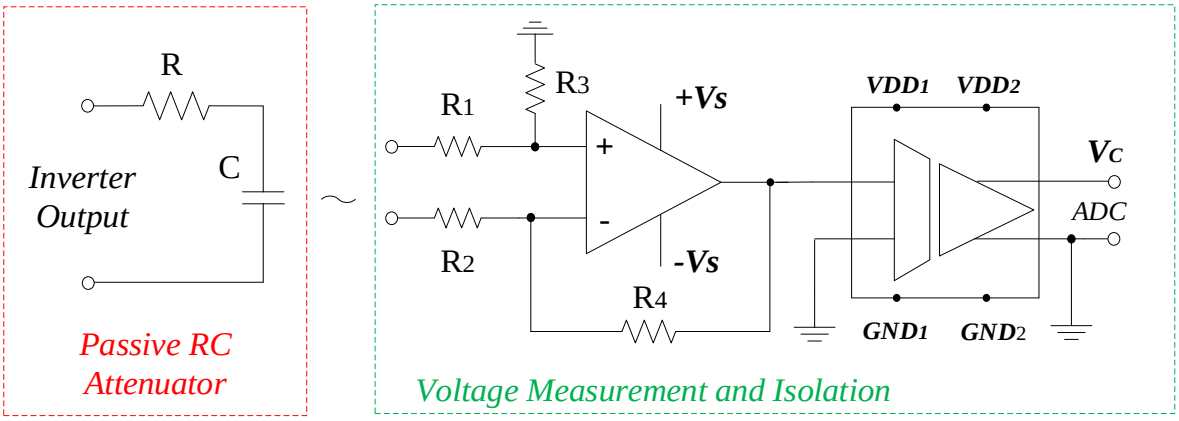
Alternatively, the use of an isolation amplifier with a high common mode rejection ratio (CMRR) can resolve the problem. As shown in Figure 5.2(b), a high-precision differential amplifier is introduced which bridges the low-pass filter and the inverter output [86]. This is still a hardware-only solution, although it does resolve the issue of common-mode voltage using the high CMRR and the isolation of the differential amplifier, thus eliminating the need for an additional voltage divider stage. However, the use of the differential amplifier itself degrades the accuracy as a result of reducing the output voltage within the amplifier supply rails $\pm V_s$. Since the AC voltage component is attenuated in a similar fashion to the DC voltage component, the difficulty of extracting a minute DC still exists, but becomes even harder due to the much smaller voltage scale involved. This, in turn, has an impact on the overall accuracy of the results. Ideally, even with the differential amplifier, the cut-off frequency of the low-pass filter should be set as low as possible to maximize AC signal attenuation. However, practical limitations have to be observed; for example, a very low cut-off frequency requires increasingly large and more expensive capacitors to be used, and a significant measurement delay is introduced.



(a). Filtering based on second order passive low-pass filter [84], [85]



(b). Alternative active low-pass filter solution [86]



(c). The proposed passive attenuation solution

Figure 5.2 Previous suggested and proposed DC voltage extraction methods

As the precision of DC extraction is normally limited when solely based on a hardware filtering solution, the method proposed in this chapter combines simple hardware and software stages to extract and eliminate the DC injection. The hardware stage is a passive attenuation circuit that scales down the inverter output voltage to the input range of the ADC of the microcontroller (0 to

3V for the DSP used in this investigation). The circuit is directly connected to the inverter output, in which a simple first-order RC low-pass filter is incorporated as the attenuator. An appropriate cut-off frequency guarantees that the residual AC component falls into the ADC range, whilst fully preserving the DC component. Although this DC component is still small, the AC/DC ratio is substantially better thus improving sensitivity. Figure 5.2 (c) shows a simplified schematic diagram of the passive attenuation circuit. The attenuated voltage is accurately sensed by the instrumentation amplifiers. As the accurate detection of the minimal DC components may still be technically challenging, a secondary filtering stage is proposed to overcome this issue. Once the voltage measurement is sampled by the system, the extraction can be carried out based on a digital signal processing technique. It is worth mentioning that an isolation amplifier is included in the passive attenuation circuit. This provides electrical isolation and a safety barrier between the analogue measurement and digital input. Although such a device potentially increases the cost of the overall circuit, the weight and size of the system are greatly reduced compared with implementing of a bulky line-frequency transformer. Most importantly, with a higher power rating, the price of isolation will stay fixed while the costs of mains transformers are significantly rising.

The use of the RC filter is 1st order and it has a higher cut-off frequency compared to previous methods [85], [84] and hence smaller size and lower cost. Moreover, the DC/AC ratio is much higher than in published work [86] as there is no attenuation of the DC component. By adding the software filtering the proposed method outperforms the sensitivity and accuracy in prior research**.**

Once the output of the passive attenuation circuit has been sampled by the system microprocessor, the residual AC component is passed through a digital signal processing technique that is used to extract the DC component. The advantages of applying a secondary digital filtering stage are that, firstly, it offers a very flexible solution. The type and tuning of the filter can be modified in software, and it can be readily adjusted until an optimal solution is achieved. Secondly, it can alleviate some of the demanding very low cut-off frequency requirements of the passive filter; thus some of the burden can be taken up by the digital filter stage. For the purpose of DC component extraction, the remaining periodic AC quantities from the attenuation circuit are removed using an integration and averaging process, which is also known as a moving average filter (MAF).

5.2.2 Digital Moving Average Filter

In general, the output voltage from the passive attenuation circuit contains both AC and DC components, and mathematically this can be presented as:

$$V_c(t) = V_{AC} + V_{DC} = V_{AC}\, sin(wt + \varphi) + V_{DC} \tag{5.2}$$

Ideally, over one mains frequency period (T), the integral of the AC voltage is zero. For a continuous system, this can be expressed as a sliding window integration as in equation (5.3):

$$A_1(t) = \frac{1}{T}\int_{t-T}^{t} V_{AC}(\tau)dt = \frac{1}{T}\left[\int_{0}^{t} V_{AC}(\tau)dt - \int_{0}^{t-T} V_{AC}(\tau)dt\right] = 0 \tag{5.3}$$

Therefore, the DC component can be determined by simply averaging the integral output:

$$A_2(t) = \frac{1}{T}\int_{t-T}^{t} V_C(\tau)dt = 0 + \frac{1}{T}\int_{t-T}^{t} V_{DC}(\tau)dt = V_{DC} \tag{5.4}$$

From equations (5.2) to (5.4), the implementation of periodic integral averaging (once per mains cycle) is required to extract the DC offset from the attenuated output. Due to the relatively low frequency of the mains AC voltage and the potential impact of measurement noise, the performance of a one-off periodic integration calculation has been shown to be unsatisfactory. Therefore, a sample-based moving average filter (MAF) is applied to improve the accuracy of offset detection. Assuming N samples are taken over a given mains cycle, the periodic integral can be updated as each new sample arrives. As such, a rolling average over the last 360° of mains frequency is obtained, which effectively produces a real-time update on the DC component, as shown in Figure 5.3. Mathematically, this can be expressed as:

$$A(k) = \frac{1}{N}\sum_{k_{M-(N-1)}}^{k_M} [V_{ac}(k) + V_{dc}(k)] = V_{dc} \tag{5.5}$$

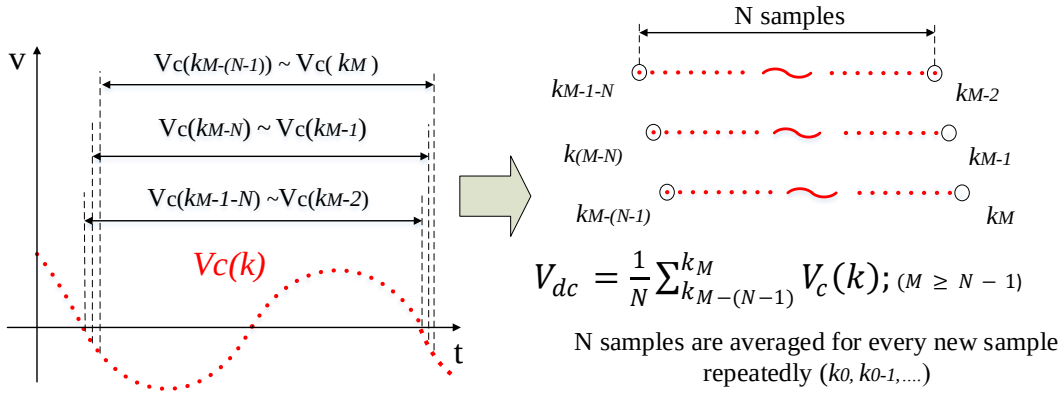


Figure 5.3 Diagram of moving average filter applied to attenuated voltage

In equation (5.6), $V_c(k_M)$ is the current sample at the output of the attenuation circuit, and $M \geq N-1$. Initially, an average of the first N samples from $V_c(k_{M-(N-1)})$ to $V_c(k_M)$ are calculated to derive the DC component present in the sampled signal. In the next discrete step, the average is taken from $V_c(k_{M+2-N})$ to $V_c(k_{M+1})$, and this iterative process continues so long as the system is operational. Since the average calculation is repeated at each sampling point, the impact of noise is greatly suppressed, and the robustness of the DC voltage offset detection is guaranteed. The fundamental frequency of the attenuated output is the same as the grid frequency, f_g, which in the UK is 50 Hz. Thus, the window frequency of the MAF is set to 50 Hz as well to provide the attenuation of the AC signal. Assuming the microprocessor ADC channel has a sampling frequency f_s, of 20 kHz, the number of samples acquired over one mains period N can be calculated as:

$$N = \frac{f_s}{f_g} = 400 \tag{5.6}$$

Therefore, in order to achieve DC offset voltage in this case, the MAF calculates the rolling average of the latest 400 samples:

$$V_{dc} = \frac{1}{400}\sum_{k_{M-399}}^{k_M} V_c(k) \tag{5.7}$$

The window frequency of the MAF is synchronized to the grid voltage via the system phase lock loop (PLL), as shown in Figure 5.1, thus any deviation in grid frequency can be taken into account. In other words, the number of samples N is adaptive with respect to the real time measured grid frequency.

5.2.3 DC Extraction Sensitivity and Frequency Analysis

A. Analysis of Proposed DC Voltage Suppression Loop

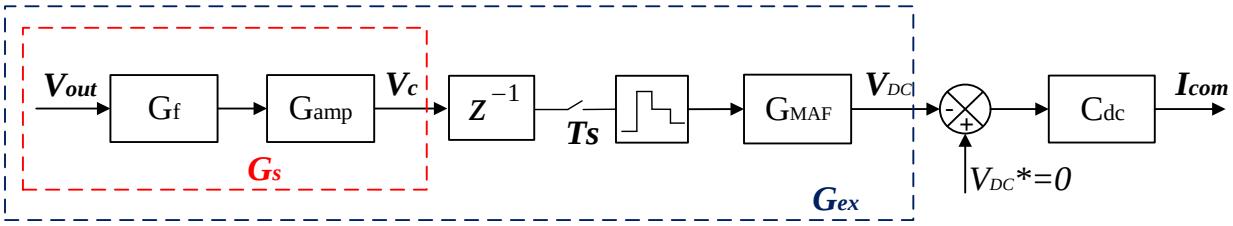


Figure 5.4 Control diagram of DC voltage suppression

The control diagram of the DC suppression loop is shown in Figure 5.4. The hardware attenuation circuit is composed of a RC attenuator G_f, which has a cut-off frequency ω_{cut}, and a voltage measurement amplifier G_{amp} of unity gain. The transfer function of the circuit G_s can be expressed as in equation (5.8):

$$G_s(s) = G_f\, G_{amp} = \frac{V_c(s)}{V_{out}(s)} = \frac{\omega_{cut}}{s + \omega_{cut}} \tag{5.8}$$

By considering the sampling process in the ADC with a sample time of T_s, the z-domain representation of the attenuated output V_c can be obtained as:

$$G_{scale}(z) = \frac{V_c(z)}{V_{out}(z)} = \frac{1 - e^{-\omega_{cut}T_s}}{z - e^{-\omega_{cut}T_s}} \tag{5.9}$$

$$V_c(z) = \frac{1 - e^{-\omega_{cut}T_s}}{z - e^{-\omega_{cut}T_s}}\, V_{out}(z) \tag{5.10}$$

The secondary MAF is then implemented in the microprocessor to filter out the DC component. As it is an average of N V_c samples with a sliding window at line frequency, a mathematical representation in the z-domain can be derived in equation (5.11), based on the formula of geometric series.

$$G_{MAF}(z) = \frac{V_{dc}(z)}{V_c(z)} = \frac{1 + z^{-1} + z^{-2} + z^{-3} + z^{-4} + \cdots z^{-N+1}}{N} = \frac{1 - z^{-N}}{N(1 - z^{-1})} \tag{5.11}$$

Thus, a z-domain transfer function of the DC extraction process can be obtained as:

$$G_{ex}(z) = \frac{V_{dc}(z)}{V_{out}(z)} = \frac{(z^N - 1)(1 - e^{-\omega_{cut}T_s})}{N(z^N - z^{N-1})(z - e^{-\omega_{cut}T_s})} \tag{5.12}$$

The inverter output voltage contains AC quantities at the integer multiple harmonics and switching frequency. Given the rolling samples $N = 400$, a sample frequency $f_s = 20\ kHz$ and the cut-off frequency $\omega_{cut} = 1.38\ rad/s$ (0.22 Hz) of the RC attenuation filter, the frequency response of the extraction is shown in the magnitude plot in Figure 5.5. With the combination of the passive RC attenuator and software MAF, increasing attenuation is observed over the frequency spectrum. The large attenuation at integer harmonics removes the redundant AC components, resulting in a precise DC measurement. This DC measurement is fed to a simple DC controller $C_{dc}(z)$, and the DC voltage offset can be completely removed via the compensation current to the current reference. Therefore, whilst the classic current control loop maintains the general operation of the inverter, the suppression loop robustly removes any DC current component.

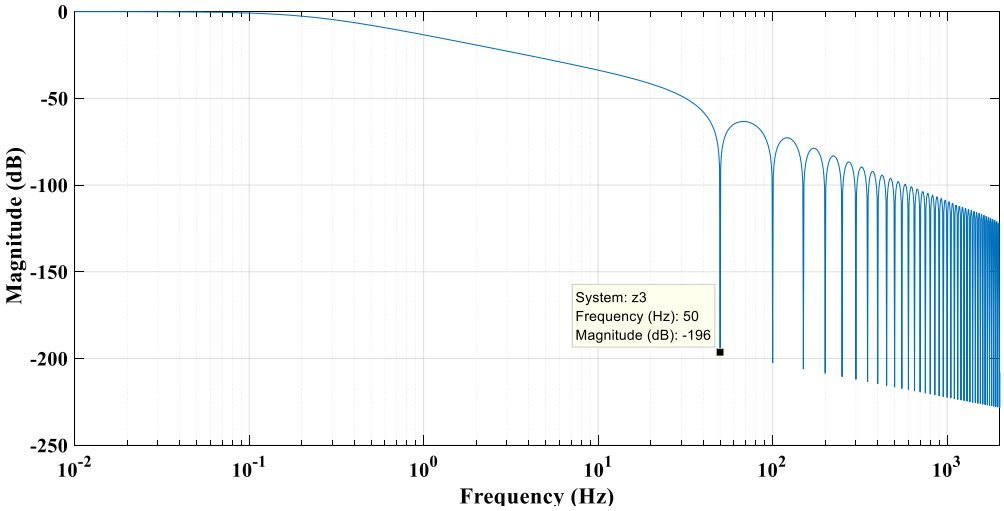


Figure 5.5 Frequency response of DC extraction

B. Analysis of Detecting Sensitivity to Potential Errors

The sensitivity of DC detection is clearly improved with the use of the attenuation circuit and software filtering. However, the actual accuracy in terms of residual DC bias is analyzed by taking into consideration the potential errors in the operating process. Compared to current transducers, the op-amps used in the passive attenuation circuit have much better characteristics in terms of

offset drift and non-linearity. Careful calibration can remove the primary offset voltage V_{os}, however, the offset voltage drifts with operating temperature. For precision op-amp, the temperature coefficient V_{Tos} lies in the range 0.1-10 $\mu V/℃$. Thus, the accuracy-sensitivity to temperature S_T can be presented as:

$$S_T = \frac{V_{Tdrift}}{V_{dcs}} = \frac{V_{Tos}\,\Delta T}{I_{dcs}(R_e + R_g)}$$

(5.13)

where the I_{dcs}, V_{dcs} are the maximum DC current injection given in norm, and its corresponding DC voltage value. ΔT is the temperature change in during the operating condition, and the V_{Tdrift} is the voltage offset drift with temperature.

In addition, the ADC can potentially introduce errors into the software filtering stage, thus affecting the accuracy of the DC extraction. With the exception of the calibrated offset and ADC quantization errors, neither differential non-linearity (DNL) nor the integral of DNL (INL) errors can be easily corrected. In a K-bit ADC, the accuracy-sensitivity to DNL and INS errors are given as:

$$S_{DNL} = \frac{A + B}{2^K}$$

(5.14)

where A and B are the DNL and INL error in least significant bit (LSB).

Lastly, as the number of samples N in the MAF is an integer, mismatch errors are introduced by neglecting the fractional component of calculated samples in (5.6). As might be expected; the lower the sampling frequency, the greater the errors. The average sensitivity to the mismatch errors of MAF S_{MAF} can be represented as:

$$S_{MAF} = \frac{X}{N}$$

(5.15)

where X is the neglected fraction in integer sample number.

The overall sensitivity to potential errors S_e in the proposed DC detection process can be obtained as:

$$S_e = S_T + S_{ADC} + S_{MAF}$$

(5.16)

With the use of high resolution 12-bit ADCs and a sampling frequency of 20 kHz, S_{ADC} and S_{MAF} are minimal and can generally be neglected. This is confirmed in (5.17), where the maximum ADC errors of ±2 LSB and a maximum fraction of 0.5 are introduced. As the typical V_{Tos} and I_{dcs} are given as $0.6\ \mu V/℃$ and 5 mA (readily obtained from the component datasheets and norm), with an operating temperature change ΔT of 50 ℃ and parasitic resistance of 0.3 ohms, the overall sensitivity to potential errors of the DC detection system is:

$$S_e = \frac{30\mu V}{5 * 0.3\ mV} + \frac{2}{2^{12}} + \frac{0.5}{400} = 2.17\% \tag{5.17}$$

5.3 Simulation Results

The novel DC suppression method is verified based on the simulated inverter model that has been developed in Chapter 3. The simulated inverter system is controlled to inject a unity power factor of current to the grid using the PR controller approach. The suppression loop is constructed and connected to the inverter output in the same manner as shown in Figure 5.1. To confirm the performance of the DC measurement, a measurement offset is manually introduced into the current sensor, yielding a pre-determined DC component in the inverter output. This has been explained in equation (3.32). The suppression is separately tested by connecting the inverter to an ideal grid and a real grid model. As the parameters of the simulated inverter have been listed in Table 3.1, Table 5.1 here only summarizes the parameters of the passive attenuator and the MAF filter.

Table 5.1 Simulation parameters

Parameters	***Value***
Sensor Measurement Offset, I_{off}	0.05 A
Parasitic Resistance of LCL filter, R_e	0.1 Ω
Resistance of Grid Impedance, R_g	0.3 Ω
Resistors in Attenuator, R_s	72 kΩ
Capacitors in Attenuator, C_s	10 μF
Sample Frequency, f_s	20 kHz
Window Frequency of MAF, f_w	50 Hz
Cut-off frequency of RC attenuator, f_{cut}	0.22 Hz

The characteristics of the attenuating low-pass filter are also presented in Table 5.1. The values of the resistor and capacitors are carefully designed to attenuate the fundamental frequency of the inverter output within the ADC input range. By substituting the filter parameters, the cut-off frequency is calculated as:

$$f_{cut} = \frac{1}{2\pi RC} = \frac{1}{2\pi * 72 * 10^3 * 10 * 10^{-6}} = 0.22\ Hz \tag{5.18}$$

The steady state time t_s can be then obtained as:

$$t_s = 5 * \tau = 3.6\ s \tag{5.19}$$

The low cut-off frequency introduces an inevitable time delay in the DC determination which is calculated as in (5.19). This, however, will not significantly affect the DC suppression response. The sampling frequency is 20 kHz, and the grid frequency is 50 Hz. Hence equation (5.6) applies, and the DC component is acquired from 400 samples.

5.3.1 DC Compensation with the Idealized Grid

The simulation is firstly run for 10 s with a connection to an idealized grid and the DC controller is not enabled until 5 s. Given the artificial DC sensor offset and parasitic resistance, the capabilities of DC determination and suppression were separately tested, and the results are reported below.

The steady output from the attenuator is captured in Figure 5.6, where the switching harmonics of the inverter output voltage have been eliminated, and a mains frequency component dominates. The use of the low-pass filter significantly attenuates the fundamental voltage within $\pm 1.5\ V$. The frequency spectrum of the inverter output voltage and attenuated output voltage are presented in Figures 5.7 and 5.8 respectively. As expected, the large number of frequency components in the inverter output current is greatly attenuated. With a complete preservation of the DC component, the ratio of AC to DC is significantly reduced, facilitating further DC extraction with improved sensitivity.

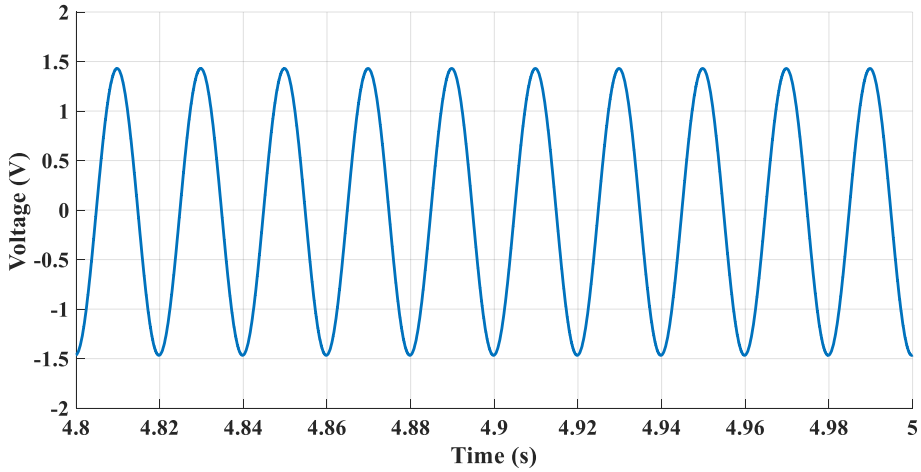


Figure 5.6 Voltage output from attenuation circuit

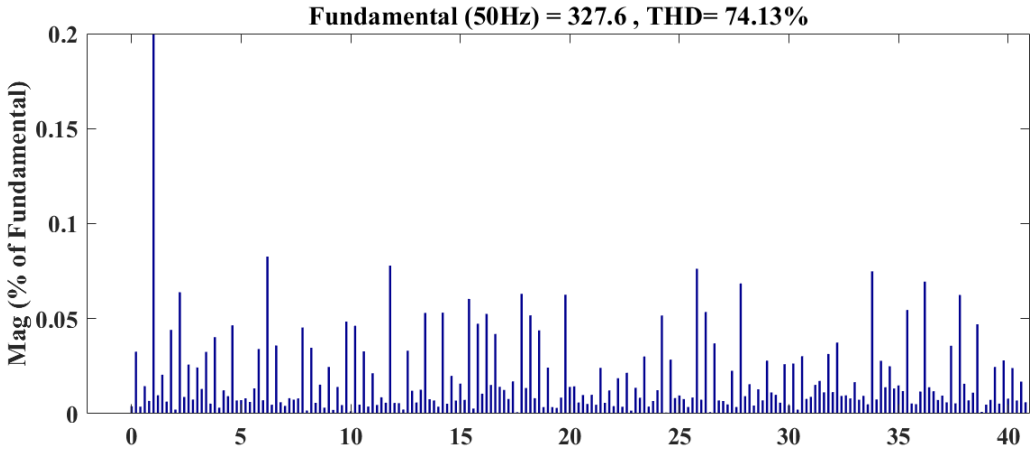


Figure 5.7 FFT analysis of inverter output voltage

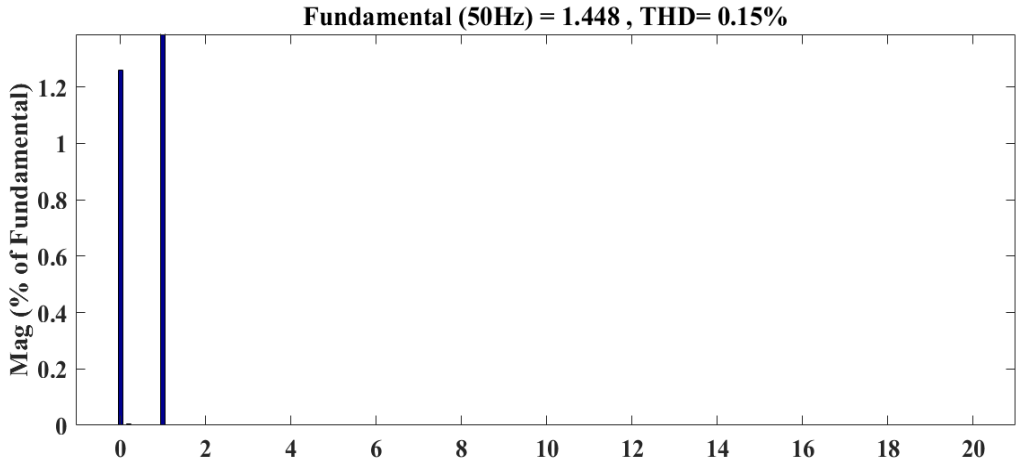


Figure 5.8 FFT analysis of V_c

In the simulation, the moving average filter is developed based on equation (5.11). The measurements of DC voltage from MAF and compensation current from the DC controller are shown in Figure 5.9. The settling time of the circuit shows good agreement with equation (5.19). Based on the known offset of 50 mA, the corresponding DC voltage can be calculated as 20 mV according to equation (5.1), which meets the steady-state measurement result. A high overshoot is observed at the beginning of the measurement transient. This is introduced by the accumulation period of MAF, which happens only at the initial stage of DC measurement.

By enabling suppression at 5 s, the steady compensation current from the DC controller is confirmed as -50 mA with a transient of less than 2 s. This current added up to the reference of the current control loop will eliminate the DC injection. As shown in the results, the compensated DC measurement is effectively zero at the steady state.

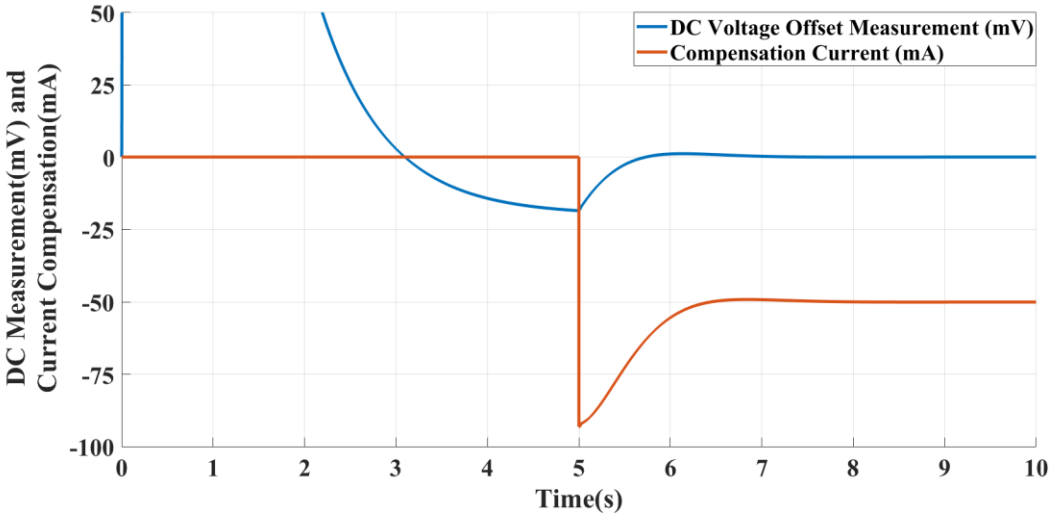


Figure 5.9 DC voltage compensation

5.3.2 DC Compensation with DC Bias at the Point of Common Coupling

It is important to notice that the proposed DC compensation is capable of compensating for DC current components produced by other electric applications, particularly if they are connected to the same PCC. This is verified by connecting the simulated inverter system to a grid model where a DC bias of 10 mV is introduced. Without changing the artificial sensor offset and the operating parameters, Figure 5.10 presents the results of the DC measurement and compensation current from the suppression loop.

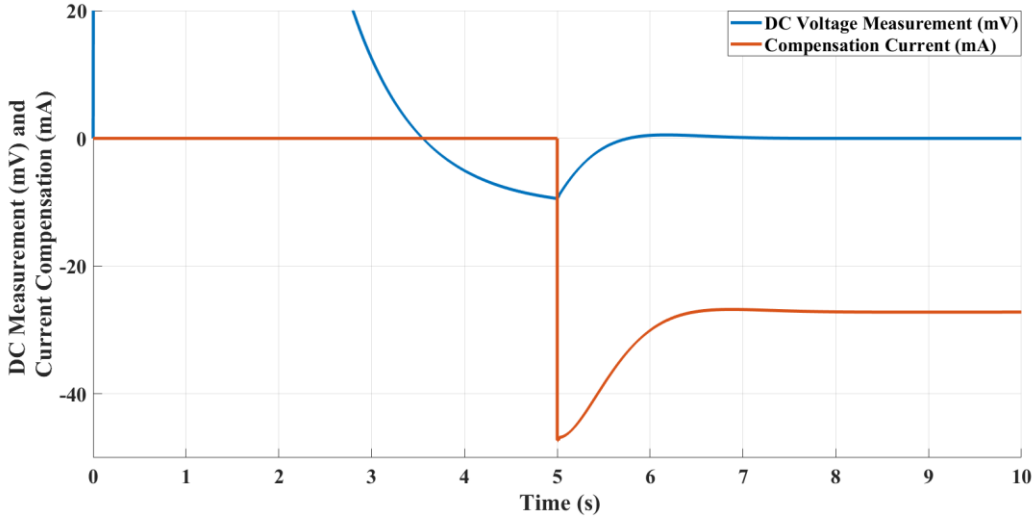


Figure 5.10 DC offset compensation at V_{pcc}

With the same sensor offset and controller set-up, compard with the results in Figure 5.9, both DC voltage measurement and compensation current have changed. The steady-state DC measurement is confirmed as -10 mV, whilst the compensation current from suppression loop is -25 mA. A zero DC voltage measurement is still obtained with the engagement of the suppression loop. In this case, according to KVL, the DC voltage at the inverter output can be calculated mathematically as:

$$V_{DC} = V_{pcc,dc} + I_{DC}\left(R_e + R_g\right) = 10\,mV + (-20\,mV) = -10\,mV \tag{5.20}$$

As aforementioned, the DC voltage mitigation technique operates the H-bridge inverter to act as a compensator, which cancels the DC bias appearing in the point of the common coupling. Therefore, the DC current injection from the compensated output current can be calculated as:

$$I_{DC,comp} = \frac{V_{DC}}{R_e + R_g} + I_{offset} = \frac{-10}{0.4} + 50 = 25\,mA \tag{5.21}$$

In this case, the compensation current from the proposed suppression loop only compensates for 25 mA DC current injection, whilst the remaining DC current are injected to cancel out the DC voltage bias of 10 mV at V_{pcc}. This is also confirmed by the FFT analysis of compensated output current, where the DC current component of the injected current has a magnitude of 25 mA.

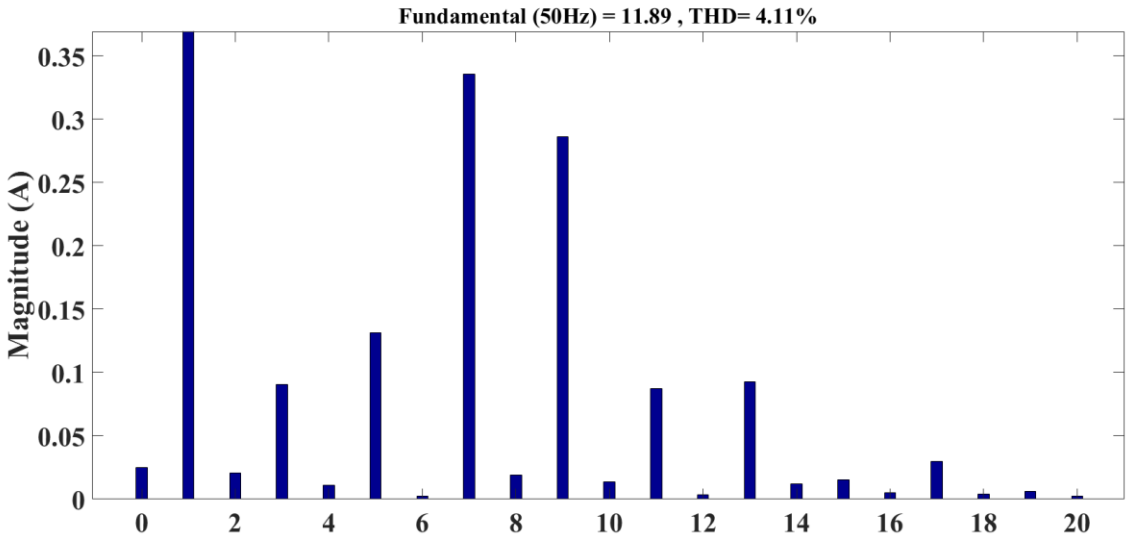


Figure 5.11 Harmonic distribution of output current

5.4 Experimental Results

The proposed DC suppression method is verified experimentally based on the H-bridge inverter test rig introduced in Chapter 4. As shown in Figure 4.3, the designed passive attenuation circuit is directly connected to the inverter output, whilst its output is interfaced with the general control board. Similarly, the performance of DC voltage determination is demonstrated via deliberately injecting a DC current into the current reference. From the experimental set-up, the accuracy of DC measurement and effective DC suppression are reported in this section. As aforementioned, an isolation transformer and a variac are employed in the experimental inverter system, where A DC bias of -4 mV is measured at the PCC via digital multi-meter. The performance of the designed circuit and proposed mitigation can be validated from the external DC measurement circuit, and the experiments are carried out based on the same parameters as summarized as in Table 4.1.

5.4.1 Experimental Validation of DC Voltage Measurement

A. Performance of Passive Attenuation Circuit

The inverter rig is operated from a 50 V DC link voltage at 20 kHz switching frequency, injecting a 5 A RMS current to the grid at unity power factor. As shown in Figure 5.12, the inverter output is a switching frequency waveform, which has an alternating polarity based on the grid current. The variable duty cycles of the PWM voltage pulses show a large number of frequency components at the inverter output.

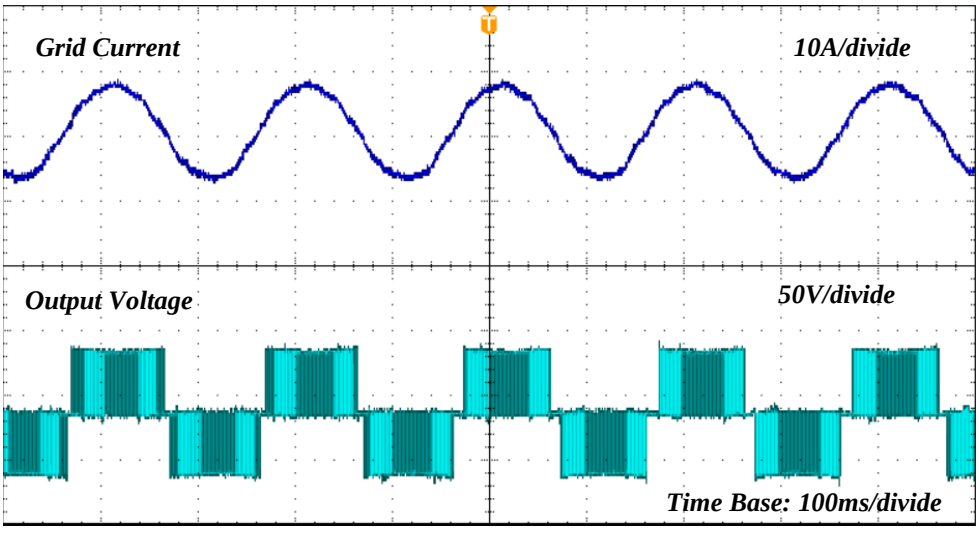


Figure 5.12 Inverter output voltage

Figure 5.13 shows the attenuated inverter output voltage which is dominated by the line frequency component. Since the attenuator provides a great attenuation of the frequency harmonics, but not the DC component, the residual AC voltage has an amplitude of only 0.3 V, taking into account that the RC filter is designed for the rated DC voltage. This facilitates the process of DC extraction as it further reduces the ratio of AC and DC components. However, owing to the features of MAF shown in Figure 5.5, where an enormous attenuation is applied to the fundamental and integer harmonics, the residual AC component would hardly affect the DC extraction at all even with the rated DC link voltage. As mentioned before, deviation in grid frequency is compensated by synchronizing the window frequency to the mains frequency via PLL. In this investigation, no significant changes were observed in laboratory grid voltage frequency (always between 49.5 to 50.5 Hz; corresponding N from 396 to 404). However, in weak grid applications, greater variation might clearly be observed, hence the need to update N.

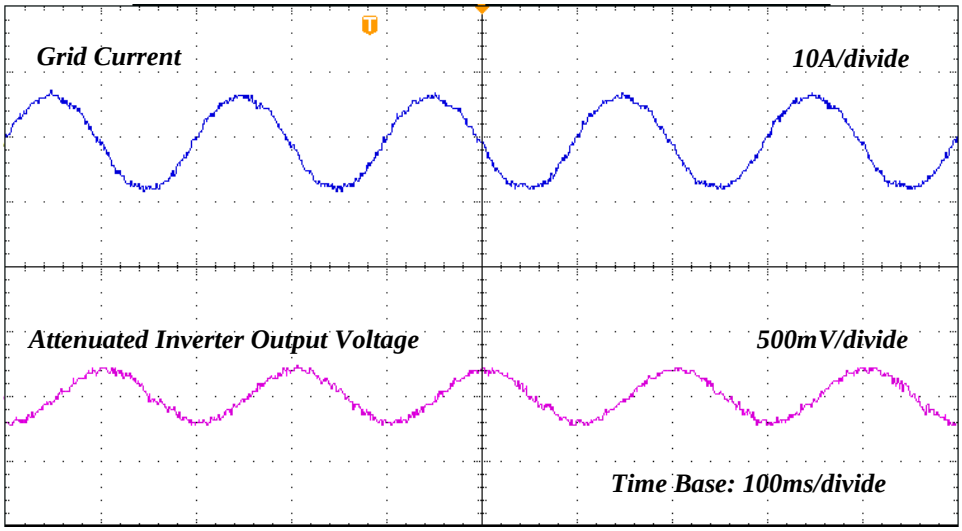


Figure 5.13 Voltage output from passive attenuation circuit

B. DC Voltage Measurement with Given DC Reference

By using the external measurement circuit mentioned in Figure 4.1, the DC current injection in the test rig is first measured at -58 mA without applying any DC bias to the current reference. Figure 5.14 shows that a DC of 50 mA and 100 mA is separately injected into the current reference at 6.4 s and 12.8 s. The DC current injection in the test rig is respectively measured at around -8 mA and 42 mA (50 mA and 100 mA higher than -58 mA). As expected, Figure 5.14 shows that the DC voltage measurement follows the step change in the DC reference with a response time of 1.8 s.

This is confirmed with the R_s, C_s given in Table 4.1, based on equation (5.19). A significant amount of noise is revealed owing to the high scale factor of the oscilloscope. Fortunately, this is primarily introduced by the DAC and measurement probes and does not actually exist in the processing signals. The accuracy of extraction is confirmed by capturing the steady DC voltage measurements under each condition (Section A, B, C) digitally.

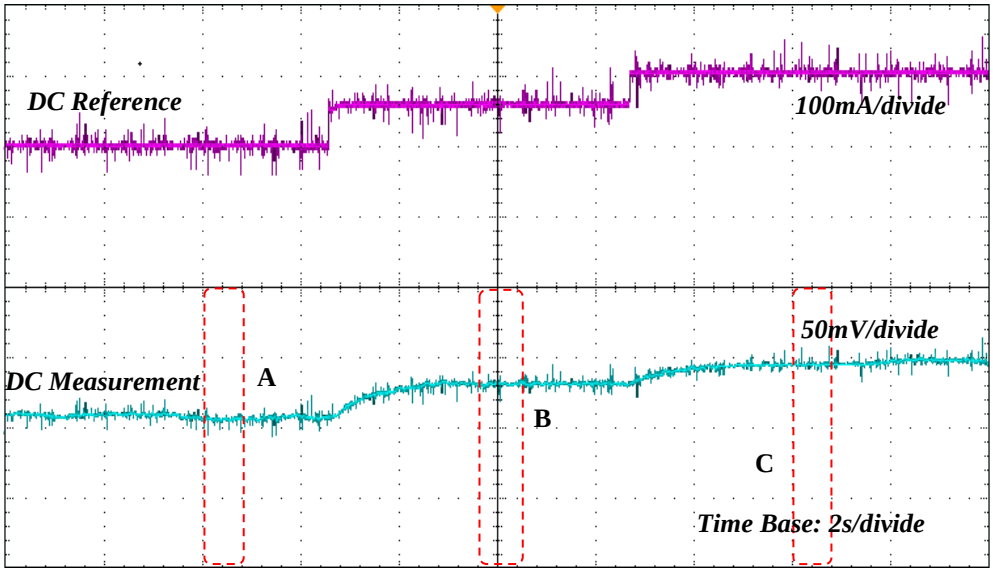


Figure 5.14 DC voltage measurement with given DC reference

Figure 5.15 shows the steady-state digital DC voltage extraction of Section A, B and C from the DSP via the GUI interface, which are separately confirmed as -24 mV ($\pm$1 mV), -6mV and 12 mV ($\pm$1 mV), where a DC bias of -4 mV comes from V_{pcc}. With a step change of 50mA current in the DC reference, the responses show a step of 18 mV. The resistance of the output path can in turn be calculated as 0.36 Ohm at the time of measurements. The corresponding DC current injection can be then calculated according to equations (5.1) and (5.21). Based on the DC voltage extractions of the inverter unit and the DC bias voltage at PCC, the levels of DC current injection under the three conditions are confirmed as -56 mA (-20 mV), -5.5 mA (-2 mV) and 44 mA (16 mV), which shows good agreement with the results from the external DC measurement circuit. Since the deviation in the measurement is approximately $\pm$1 mV, the accuracy of proposed DC extraction is validated. From this, the DC current component can be mitigated through digital control methods.

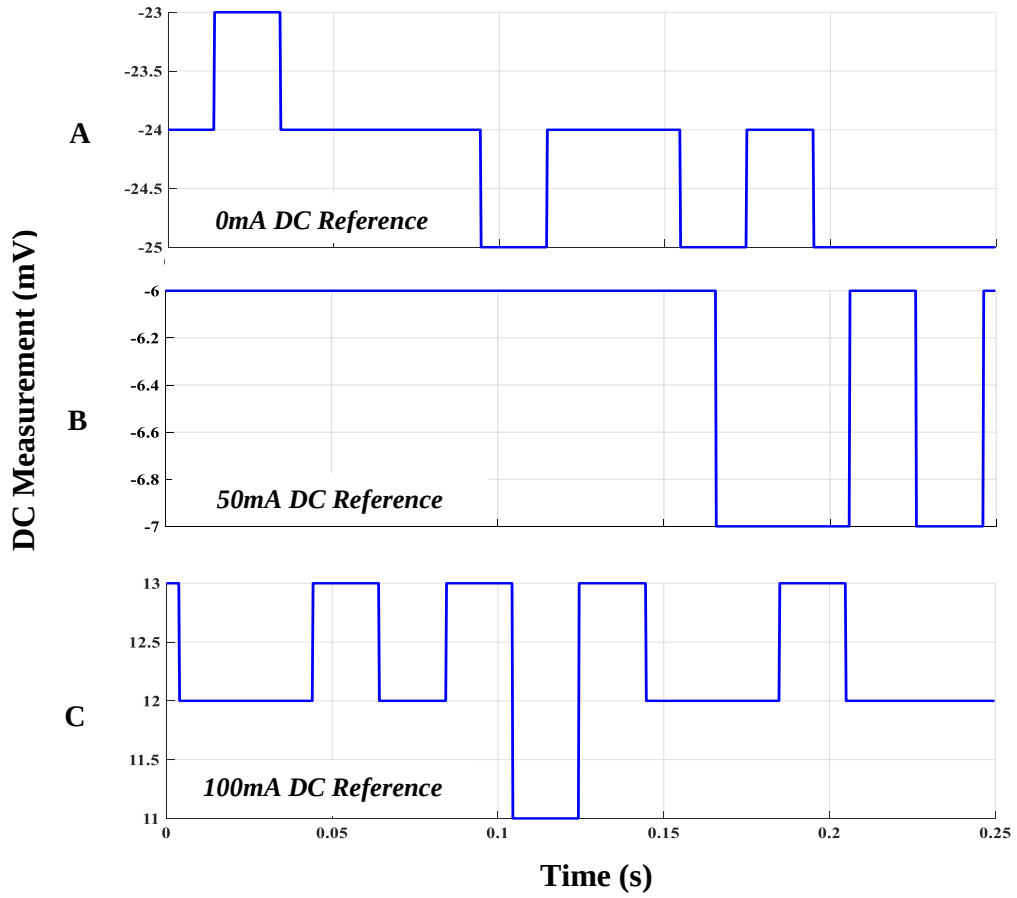


Figure 5.15 DC voltage measurement in the microprocessor

5.4.2 Experimental Validation of DC Suppression

A. Compensation of Natural DC Injection

Initially, the performance of DC suppression is verified only taking into consideration the natural DC injection in the test rig. Figure 5.16 shows the waveforms of DC voltage measurement and compensation current, where the DC injection is determined using the proposed extraction method. By enabling the suppression loop at the time point of 3.5 s, a compensation current starts to arise, which gradually causes the DC component in the system to decline. From the zoomed dynamic response, it can be clearly seen that the DC voltage measurement converges to zero with a damping response of less than 3 s. As the deviation in the proposed DC detection has been proven to be within ± 1 mV, the compensation current performs with a small oscillation of 3 mA due to the parasitic resistance in the output path. Despite this, the DC component is still substantially

mitigated by the proposed suppression loop. Whilst the DC voltage measurement reaches zero at steady-state, the compensation current added up to the current reference is confirmed at around 60 mA, which not only cancels the DC current injection of the inverter unit, but also compensates for the DC voltage bias at the point of common coupling.

Owing to different controller gains in the suppression loop, the dynamic response of experimental suppression in Figure 5.16 shows larger overshoot and oscillations than that of simulation result in Figure 5.10. However, the steady-state DC suppression in experimental inverter unit validates the result reported in simulation model, and both of which show great agreements with Equations (5.20) and (5.21).

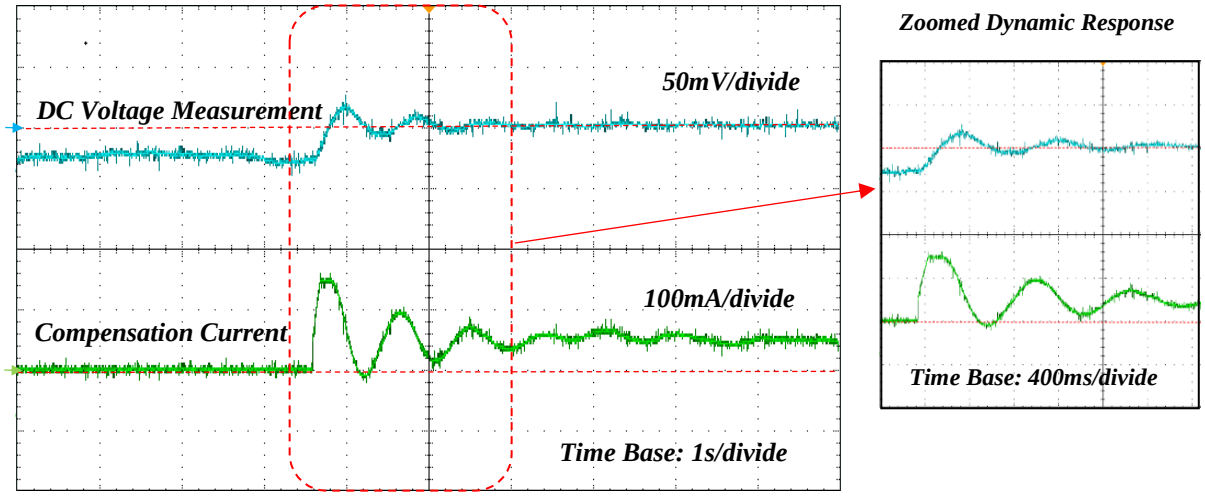


Figure 5.16 DC voltage offset compensation

B. Validation of Proposed DC Suppression Loop by Injecting Different DC References

By deliberately introducing a DC into the current reference, the DC component in the sinusoidal output current is calculated separately by switching the proposed DC suppression on and off. The process is repeatedly performed for DC reference levels from 0 to 100 mA in steps of 10 mA, and the results are recorded in Figure 5.17. Compared with the ramping DC injection observed in the conventional current control, the implementation of the proposed DC suppression effectively limits the DC component of the output current within 5 mA, regardless of the change of the DC reference.

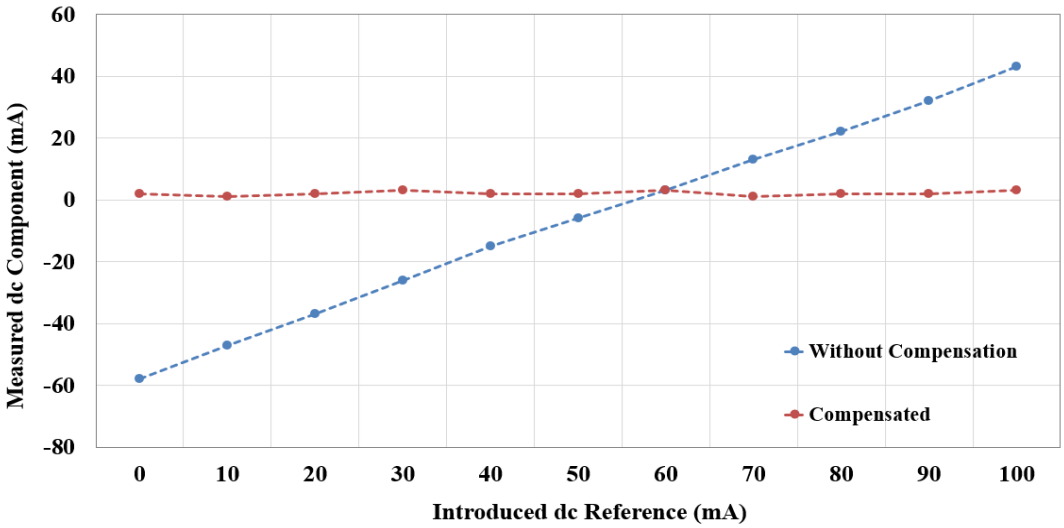


Figure 5.17 Averaged DC injection with and without the DC suppression loop

C. Harmonic Performance of the Output Current

As the DC suppression is linked to the current control of the inverter system, it is important to make sure that the DC suppression loop does not affect the quality of current injected to the grid. For this reason, the harmonic distribution is analyzed for the natural output current and compensated output current separately via FFT Analysis. Figure 5.18 shows the per-unit magnitude of harmonics between the 0^{th} and the 20^{th} order. The fundamental and multi-integer harmonics show good similarity, with values of the averaged total harmonic distortion (THD) at 4.73% and 4.65% respectively. This analysis confirms that the output current is free of any effect from the proposed DC suppression loop. Meanwhile, the DC component, which appears at a magnitude of 0.75% in the output current, has been removed after the compensation.

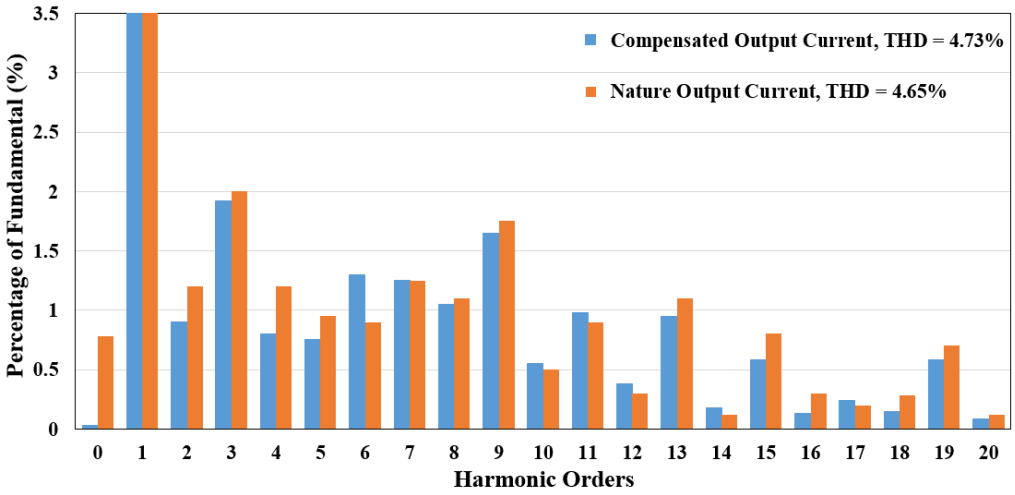


Figure 5.18 Harmonic distribution of natural/compensated output current

5.5 Summary

This chapter investigates a novel DC suppression method for grid-connected transformerless PV inverter systems. As the accuracy of the miniscule DC extraction from a very large AC signal is challenging in previously suggested approaches, the proposed method has introduced a passive attenuation circuit and a software moving average filter. Such a combination provides a robust DC determination of the DC component with increased accuracy and sensitivity. The attenuation of the frequency spectrum has been demonstrated in a frequency analysis and Bode plot. Following this, DC mitigation is established via an extra DC suppression loop with a simple DC controller.

The simulation models at rated power have shown the capability to suppress DC current, as well as of compensating for the voltage bias at the point of common coupling. In the results of experiments, in which a set of step-changed DCs was introduced onto the current reference, the performance of DC measurement and the effectiveness of DC suppression have been proven under grid-connected conditions. In both the simulation and experimental results, it has been shown that the output current is not affected by implementing the DC suppression loop. The harmonic performance shows a similar THD in the compensated output current, whilst the DC component is significantly mitigated. In conclusion, the present DC suppression approach is simple and highly effective, which makes a positive contribution towards in any grid-connected PV inverter system; unlike many other solutions presented in the literature, it is not power converter topology specific.

Chapter 6 DC Injection Suppression in Transformerless H-bridge Inverter Using a DC Link Sensing Approach

6.1 Introduction

Whilst the performance of the proposed DC voltage mitigation method has been confirmed in the previous chapter, there may be some uncertainty as to the extra cost added to the inverter system owing to the use of an isolation amplifier in the passive attenuation circuit. For this reason, this chapter presents a novel control-based DC suppression method for a single-phase grid-connected transformerless full-bridge inverter, using a DC link current sensing technique. In the first part of the chapter, the DC extraction from the DC link current waveform is investigated, and mathematical derivations are carried out to prove the concept of the new technique. From this, an active control loop is implemented to suppress the DC current at the inverter output. Furthermore, fundamental AC current control is simultaneously implemented using the same DC link current measurement, thus eliminating the need for a conventional output current sensor. Hence, overall, no additional hardware is used in the system. The proposed DC link sensing technique is first verified with a simulated inverter model at the rated power. Then, by implementing the technique with the experimental inverter system, the performance of DC determination, suppression and current control is demonstrated. Compared with the results when operating with conventional current control, the robust and effective performance of the proposed approach is confirmed.

6.2 Mathematical Analysis of DC Link Current

The study focuses on a unipolar PWM switched transformerless H-bridge inverter, which is a well understood and widely adopted power converter topology for single-phase PV applications, as aforementioned, due to its smaller output filter requirement. Figure 6.1 shows the block diagram of the DC link current sensing technique, where the DC injection and injected current are determined from the DC link current measurement. The reconstruction of output current and the DC suppression loop allow the current control loop and DC mitigation to be implemented without using any additional hardware. In this section, the mathematical relationship between DC injection and the DC link current is derived based on a simplified switching model of the H-bridge inverter.

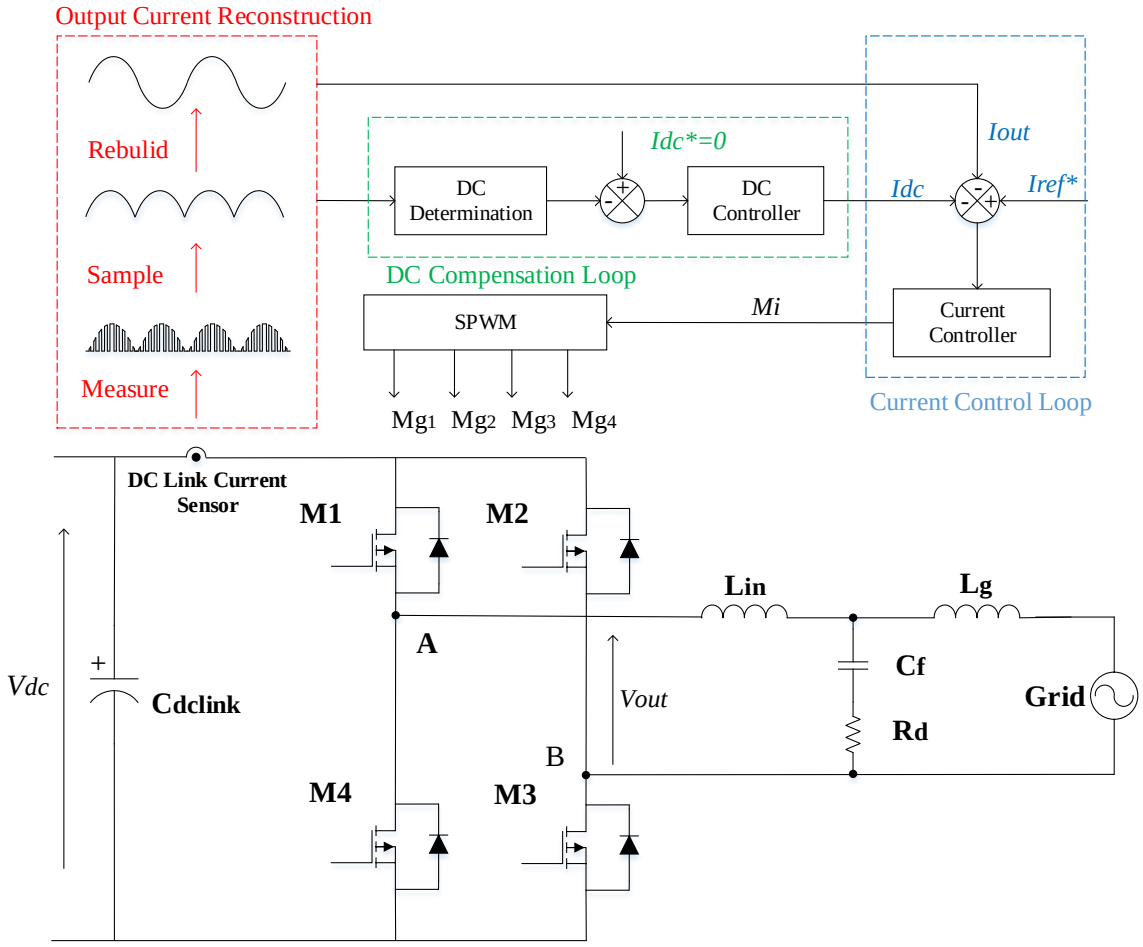
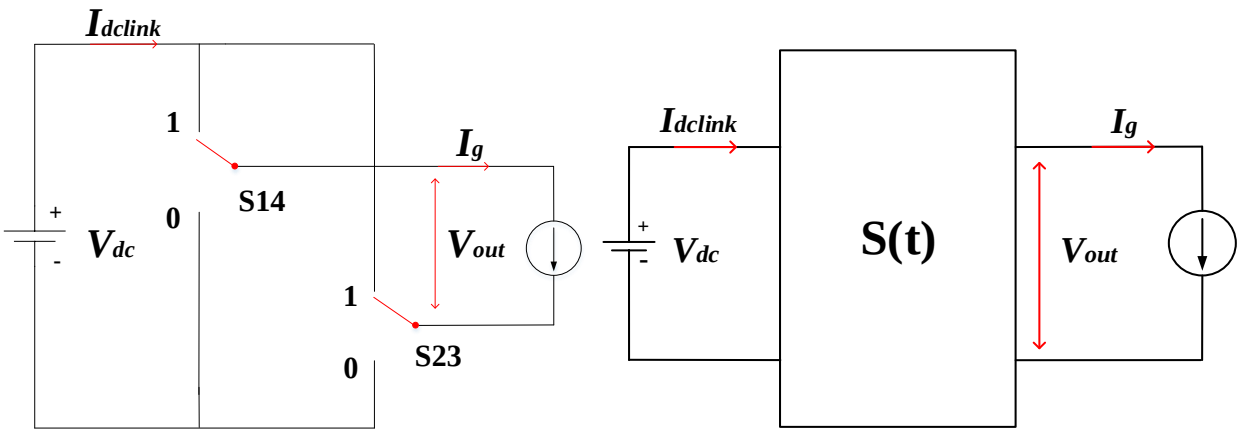


Figure 6.1 Block diagram of DC link sensing technique

6.2.1 H-bridge Modelling and DC Injection Analysis

As shown in Figure 6.1, the top and bottom switches in each leg of MOSFETs H-bridge structure are activated complimentary, and they can be separately represented by two integrated switches S_{14} and S_{23}. The equivalent model is presented in Figure 6.2 (a), where the one and zero in the switching terminals separately stand for the positive and negative connection with the DC voltage source. For unipolar PWM scheme, the four key switching states for the H-Bridge are listed in Table 1; two states (1&2) are referred to as *conducting states*, the other (3&4) are referred to as *freewheeling states*.



(a). Integrated Switch of H-bridge *(b). Simplified Switching Model*

Figure 6.2 Modelling of H-bridge inverter

Table 6.1 Unipolar switched H-bridge voltage levels and current states

State	Switches States				Integrated Switch		V_{out}	I_{dclink}
	M1	M2	M3	M4	S_{14}	S_{23}		
1	On	Off	On	Off	1	0	V_{dc}	I_g
2	Off	On	Off	On	0	1	$-V_{dc}$	$-I_g$
3	On	On	Off	Off	1	1	0	0
4	Off	Off	On	On	0	0	0	0

Based on Table 6.1, the relationship of voltage and current between DC side and AC side can be expressed as:

$$V_{out}(t) = (S_{14} - S_{23}) * V_{dc} \tag{6.1}$$

$$I_{dclink}(t) = (S_{14} - S_{23}) * I_g \tag{6.2}$$

Thus, a switching function $S(t)$ is introduced, which is defined as:

$$S(t) = S_{14} - S_{23} \tag{6.3}$$

Consequently, the H-bridge inverter is equivalently modelled as shown in Figure 6.2 (b), where the switching function $S(t)$ sits in the middle, representing the mathematical relationship between DC input and AC output. Neglecting high-frequency components, the line frequency representation of $S(t)$ is [96],

$$S(t) = M_i * sin(\omega t + \varphi_1) \tag{6.4}$$

M_i is the modulation index, ω is the fundamental frequency of the grid and φ_1 is the phase difference with respect to the grid voltage. From this, with reference to Figure 6.2 (b), the following voltage and current can be express:

$$V_{out}(t) = V_{dc} * S(t) = V_{dc} * M_i * sin(\omega t + \varphi_1) \tag{6.5}$$

$$I_{dclink}(t) = I_g * S(t) = I_g * M_i * sin(\omega t + \varphi_1) \tag{6.6}$$

6.2.2 Conducting DC Link Current

As in most transformerless application, the inverter output current normally contains a fundamental AC component and DC component. This can simply be expressed as:

$$I_g(t) = I_{AC}\, sin(\omega t + \varphi_2) + I_{DC} \tag{6.7}$$

In Equation (6.7), I_{DC} is the magnitude of the DC injection, I_{AC} is the magnitude of AC output current, φ_2 is the phase difference with respect to the grid voltage.

Substituting (6.7) into (6.6) yields:

$$I_{dcLink}(t) = [I_{AC} sin(\omega t + \varphi_2) + I_{DC}]\, M_i\, sin(\omega t + \varphi_1)$$

$$= \frac{M_i * I_{AC}}{2}[(1 - cos2\omega t)cos\varphi_1 cos\varphi_2 + sin2\omega t(sin\varphi_1 cos\varphi_2 + sin\varphi_2 cos\varphi_1) +$$

$$(1 + cos2\omega t)sin\varphi_1 sin\varphi_2] + I_{DC} M_i\, sin(\omega t + \varphi_1) \tag{6.8}$$

As described in Equation (6.8), the DC and second harmonic component of DC link current are determined by AC and phase angles, whilst the line frequency component is solely introduced by DC injection. Assuming neglectable filter phase shift and unity power factor operation $\varphi_1 = \varphi_2 = 0$. In this case, it can be shown that:

$$I_{dcLink}(t) = \frac{M_i I_{AC}}{2}[1 - \cos(2\omega t)] + I_{DC} M_i sin(\omega t) \quad (6.9)$$

Equation 6.9 shows that the inverter AC output current results in the second harmonic component of the DC link current. Furthermore, it shows that the DC current component in the inverter output results in a fundamental frequency component in the DC Link current. Thus, importantly, accurate measurement and extract of the fundamental of the line-frequency component in the DC link facilitates determination of the DC component in the inverter output.

6.2.3 Analysis of Conducting Sampling with Deadtime Effect

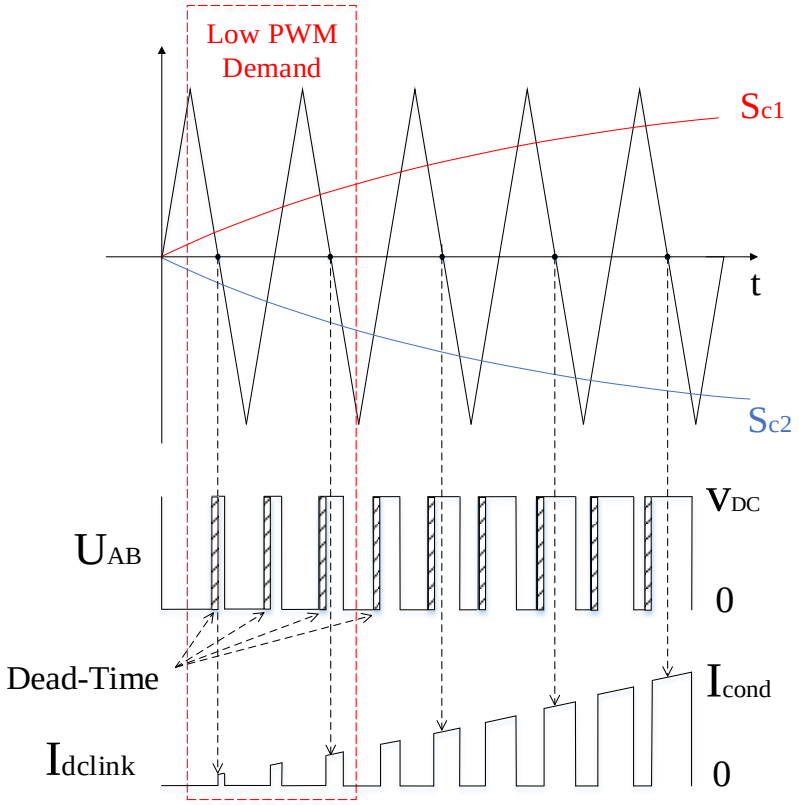


Figure 6.3 Conducting sample of DC link current measurement

As shown in Table 6.1, in a unipolar switched H-bridge inverter, the DC link current has the same magnitude as the output current during conducting state, whilst there is no current in the DC link during a freewheeling state. Consequently, the DC link current is made up of a train of PWM related current pulses. Previous studies have proven that, without over-modulation, the freewheeling measurement and conducting measurement can be separately determined by

sampling at the peak or zero-crossing point of the modulating triangular carrier [69]. Therefore, the peak sampling utilized in conventional current control results in a series of zero measurements. To fully preserve knowledge of the DC link current, the samples have to be taken at the point where the triangular modulation signal crosses zero. To correctly operate the power switches in each inverter leg, deadtime has to be inserted between the required switching edges [146]. Although it is a small amount of time depending on the characteristic of the switches, its presence still reduces the duration of the conducting states as shown in Figure 6.3. At low PWM demands, where the conducting pulses are narrow, the deadtime can eliminate the conducting pulses, or result in a zero-state measurement. Fortunately, as few PWM pulses are affected, the impact is limited. The reduction in conducting period introduced by deadtime can be calculated as:

$$P_{red} = \frac{t_d}{T} = t_d f_s \tag{6.10}$$

For a 20 kHz switching frequency with a deadtime of 500 ns, the duty cycle reduction is 1% in each pulse.

6.2.4 DC Injection in Conducting DC Link Current

When the system is working at unity power factor, the DC link conducting measurement is equal to the absolute inverter output current as shown in Figure 6.4. Considering potential DC current injection, the conducting DC link current can be expressed as:

$$I_{Cond}(t) = \left|I_g(t)\right| = \left|I_{AC} sin\omega t + I_{DC}\right| \tag{6.11}$$

$$I_{Cond}(t) = \underbrace{\frac{4 * I_{AC}}{\pi}\left(\frac{1}{2} - \sum_{n=1}^{\infty} \frac{1}{4n^2 - 1} cos2n\omega t\right)}_{Even\ Harmonics} + \underbrace{\sum_{n=1}^{\infty} \frac{4I_{DC}}{(2n-1)\pi} sin[(2n-1)\omega t]}_{Odd\ Harmonics} \ (n = 1,2,3 \ldots) \tag{6.12}$$

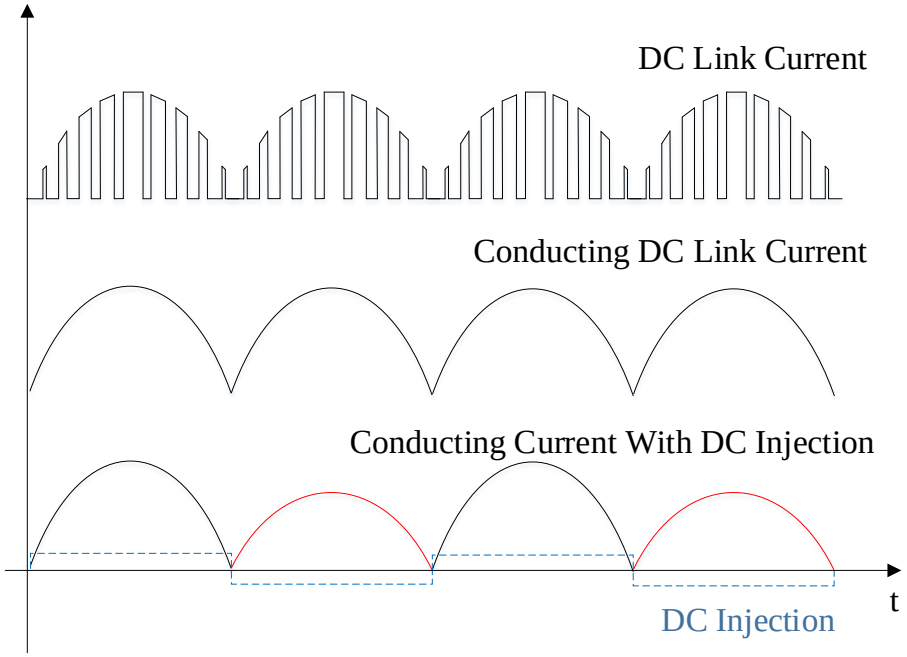


Figure 6.4 Conducting current at unity power factor

Depending on the polarity of conducting states, the DC injection is observed as a square wave and shifts the conducting DC link current measurement as shown in Figure 6.4. The frequency spectrum of the DC link current can be determined via Fourier analysis, as defined in Equation (6.12). From this, it can be seen that the even harmonics in the DC link current waveform are attributed to the fundamental AC component, whilst the odd harmonics are attributed to the DC current injection component in the system. Simplification of (6.12) can be achieved by considering the impact on the line frequency ripple only, in other words, n equals to 1. Thus:

$$I_{Cond}(t) = \frac{2I_{AC}}{\pi} - \frac{4I_{AC}}{3\pi} cos2\omega t + \frac{4I_{DC}}{\pi} sin\omega t \tag{6.13}$$

Comparing with (6.9), the line frequency component in conducting DC link current is proportional to the DC current injection as described in (6.13). However, the magnitude of the line frequency component is now greater compared to (6.9), assuming Mi < 1. Therefore, the ability to extract the DC component accurately is improved.

6.3 Proposed DC Suppression Approach

The proposed DC suppression approach is shown in Figure 6.5. The approach is based on digitally sampling the DC link current during conducting periods. For a grid connected inverter system, a phase-locked loop (PLL) is generally utilized to provide synchronization with the grid. The output of the PLL is utilized by the proposed scheme for phase detection.

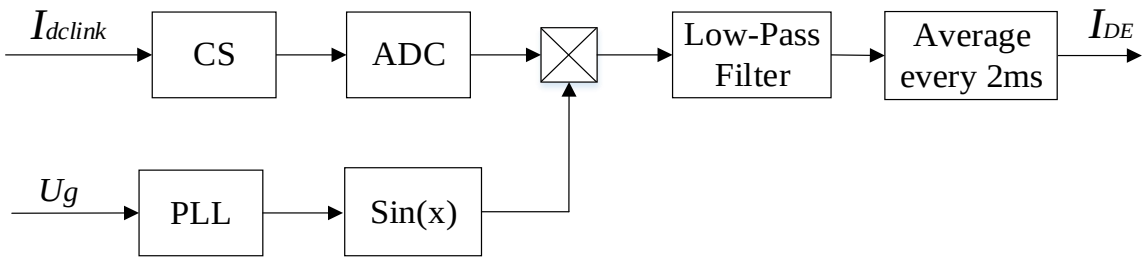


Figure 6.5 Block diagram of the proposed extraction

Based on Fourier signal analysis technique, the line frequency of the conducting current is obtained by multiplying with a sine function at the same fundamental frequency.

$$I_{Ex}(t) = I_{Cond}(t) sin\omega t \tag{6.14}$$

Then, through substituting I_{Cond} by (6.13), the frequency components of I_{Ex} can be express as:

$$I_{Ex}(t) = \frac{2I_{AC}}{\pi} sin\omega t - \frac{4I_{AC}}{3\pi}\cos 2\omega t sin\omega t - \frac{2I_{DC}}{\pi}\cos 2\omega t + \frac{2I_{DC}}{\pi} \tag{6.15}$$

As described in (6.15), I_{DC} can now be determined from a DC quantity, rather than the line frequency component in (6.13). For the purposes of DC extraction, the remaining ac quantities are redundant, and they can be removed using a digital low pass filter. As a practical point, owing to the narrow frequency range between the low-frequency AC components and DC quantity, a low cut-off frequency (< 1 Hz) is required to effectively isolate the DC component. As a further improvement, an averaging algorithm is implemented following the filter, as shown in Figure 6.5. This is required to remove the high frequency terms first expressed in (6.12), which reflects the complete characteristic behavior of the DC link conducting current.

The averaging algorithm is simple to implement, and also relieves some of the burden on the low pass filter. With the combination of low pass filter and average algorithm, the DC injection can be accurately determined from the resulting DC component at the output:

$$I_{DE} = \frac{2}{\pi} I_{DC} \tag{6.16}$$

The frequency components in (6.15) are derived from fundamental frequency of the conducting current only. As described in (6.12), the conducting current contains a wide range of frequency components, the frequency response of the proposed approach is analyzed to validate the extraction of the line frequency component.

6.3.1 Analysis of Frequency Response of Extraction

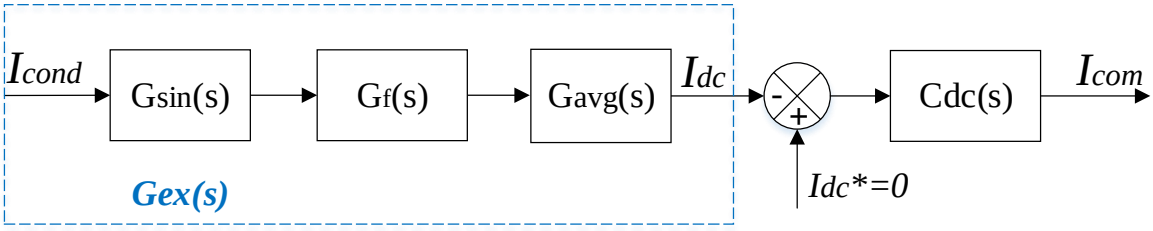


Figure 6.6 Control diagram of the DC suppression loop

The control diagram of proposed DC determination is shown in Figure 6.6. As the line frequency component of the conducting current is obtained via multiplying the sine function of grid information, this process can be expressed as an s-domain transfer function Equation (6.17), where ω_0 is the fundamental frequency of the grid.

$$G_{sin}(s) = \frac{\omega_0}{s^2 + {\omega_0}^2} \tag{6.17}$$

$G_{sin}(s)$ provides an infinite gain at the AC frequency ω_0 and an adequate attenuation on other frequencies, as shown in bode diagram in Figure 6.7.

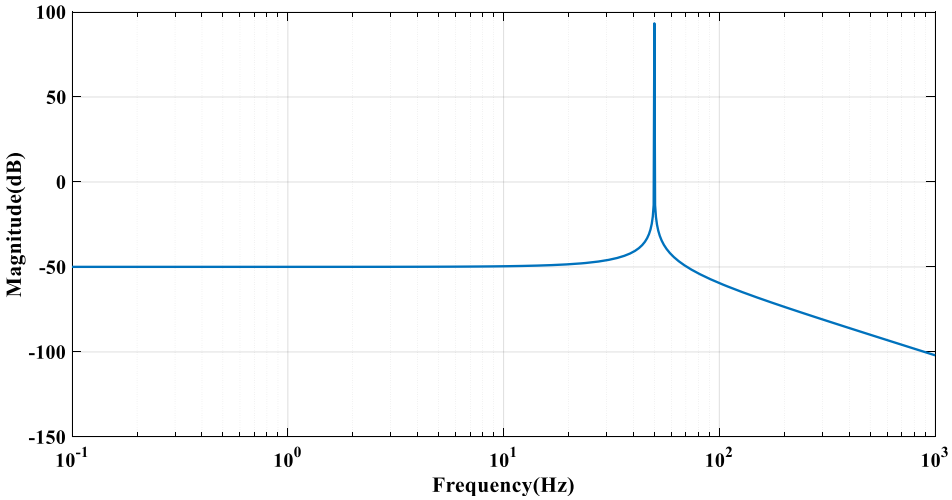


Figure 6.7 Frequency response of the sine function

A low pass filter $G_f(s)$ ($\omega_{cut}/(\ s+\omega_{cut})$), where $\omega_{cut}$is the cut-off frequency, and the averaging $G_{avg}(s)$ is then applied to further eliminate the high-frequency components. The continuous averaging can be similarly expressed as the sliding window integration in Equation (5.2), where T is the average period.

Based on (5.2), the s-domain representation of averaging can be then derived as (6.18)

$$G_{avg}(s) = \frac{Y(s)}{U(s)} = \frac{1 - e^{-sT}}{T\ s} \tag{6.18}$$

Significant attenuation is found at each integer harmonic of fundamental frequency, $n\omega_0$. This is because the output of the average filter is effectively zero for periodic signals (e.g. sin and cos). Given (6.18), the transfer function of the proposed line frequency extraction process can be expressed as:

$$G_{ex}(s) = \frac{I_{DC}(s)}{I_{Cond}(s)} = \frac{\frac{1}{T}\omega_0\ \omega_{cut}\ (1 - e^{-Ts})}{s^4 + \omega_{cut}s^3 + {\omega_0}^2 s^2 + {\omega_0}^2\omega_{cut}s} \tag{6.19}$$

With grid frequency $\omega_0 = 314\ rad/s$, cut-off frequency $\omega_c = 31.4\ rad/s$, and applying 50 Hz ($T = 0.02\ s$) averaging, the frequency response of (6.19) is shown in Figure 6.8. As shown, the low-pass filter and averaging process significantly attenuates the integer harmonics ($n\omega_0$). Given

the attenuation is more than -100 dB for all frequencies above 100 Hz, the proposed extraction effectively eliminates all existing harmonics in (6.12) with the exception of the line frequency component, therefore preserving a precise line frequency component of DC link current.

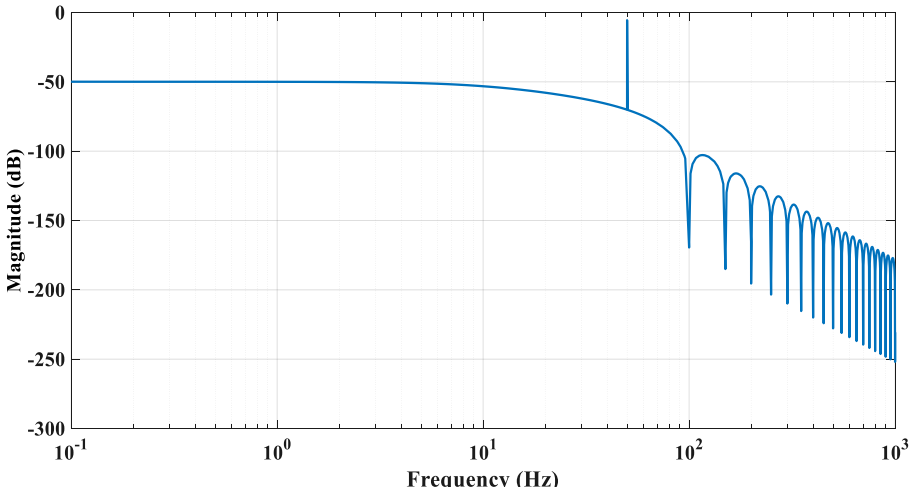


Figure 6.8 Frequency response of the line frequency extraction

In summary, through the time-domain derivation in (6.13), (6.15) and the frequency-domain analysis in (6.19), the DC current injection can be accurately determined by extracting the line frequency of conducting DC link current. Through feedforward the high-resolution DC measurement to a simple DC controller $C_{dc}(s)$, the DC current can be completely removed via the compensation current to the current reference, as shown in Figure 6.6.

6.3.2 Current Control and DC Suppression based on DC Link Sensing Technique

Generally, a conventional single-phase grid-connected inverter system is controlled using current measurement at the inverter output. However, for the proposed DC suppression approach, a current sensor must be placed in the DC link. The use of two current sensors is undesirable because it increases the cost and complexity of the system, but a simple reconstruction can be carried out which eliminates the need for the conventional output current sensor. Through the aforementioned conducting DC link current sampling, the magnitude of the inverter output current is known. Nevertheless, knowledge of the polarity is required to fully restore the output current waveform digitally. As reported in [69], the PWM index can be used to determine polarity information. With positive PWM demand, the polarity of the conducting DC link current is the same as that of the

inverter output current. For negative PWM demand, the conducting current is obtained by inverting the conducting DC link current measurement.

Figure 6.9 illustrates the flow chart of the DC link sensing technique, where the proposed DC suppression and current reconstruction operate in parallel. Then, the current control loop is implemented in the same manner as with the conventional inverter, where a PI or PR controller is typically applied to ensure the power quality of the current injected into the network.

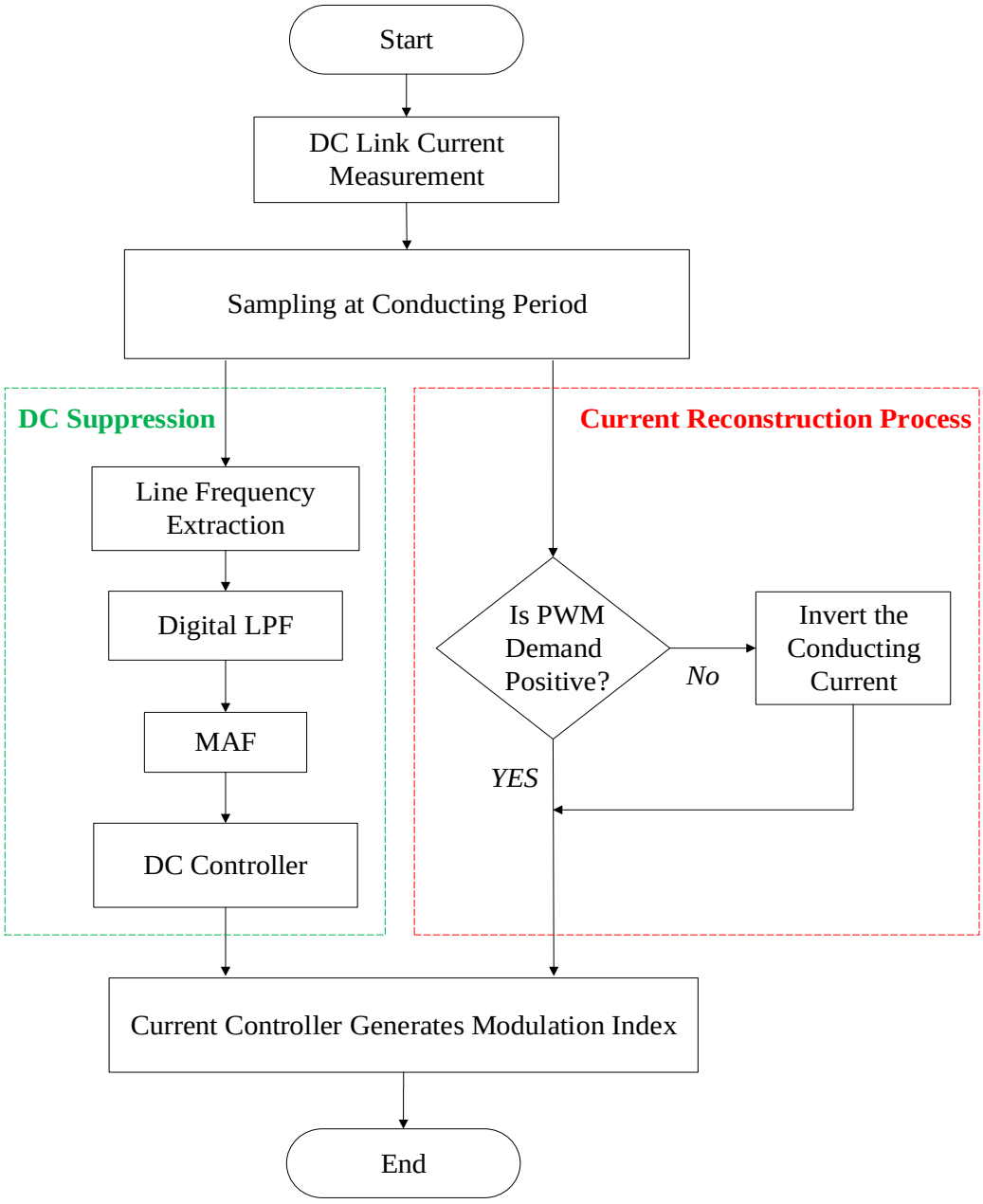


Figure 6.9 Flowchart of proposed DC link sensing technique

6.3.3 Analysis of DC Link Current Control with DC Suppression

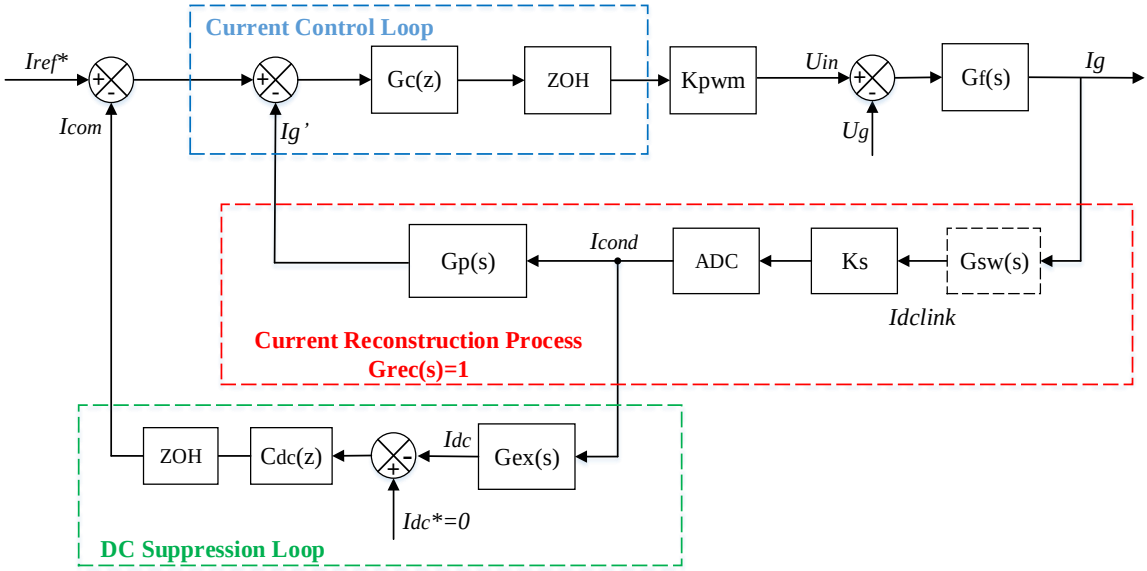


Figure 6.10 Scheme diagram of DC link sensing H-bridge inverter with DC suppression

The control diagram of the DC link sensing technique, including current reconstruction and DC suppression, is shown in Figure 6.10. $G_{sw}(s)$ and $G_p(s)$ represent the switching function and polarity information from the PWM unit respectively. Following the reconstruction, provided the current waveform is obtained accurately, the transfer function of the current reconstruction may be expressed as:

$$G_{rec}(s) = \frac{I_g{}'(s)}{I_g(s)} = 1 \tag{6.20}$$

Since the output current is available from the current reconstruction process, a conventional current loop can be implemented as shown in Figure 6.10, where $G_c(z)$ is a typical PI or PR controller. With including the DC suppression loop, the overall transfer function of the proposed approach is derived as:

$$I_g(s) = \frac{G_c(z)e^{-sT_s}\,K_{pwm}G_f(s)[I_{ref}(s) - I_{com}(s)] + G_f(s)U_g(s)}{1 + G_c(z)\,e^{-sT_s}\,K_{pwm}\,G_f(s)} \tag{6.21}$$

where K_{pwm} is the PWM gain, $G_f(s)$ is the transfer function of the output filter, T_s is the sample time. $I_{ref}(s)$ is the sinusoidal current demand and $I_{com}(s)$ is the compensation current from the DC suppression loop.

Known from the controller analysis in chapter 3, the gain of $G_c(z)$ at fundamental frequency can be very large through using PR controller, and the effect of grid voltage $U_g(s)$ can be neglected. Therefore, with the use of PR controller in the current control loop, the transfer function of the proposed DC link sensing approach is derived as such;

$$I_g(s) = \frac{G_c(z)e^{-s*T_s}\, K_{pwm}\, G_f(s)}{1 + G_c(z)\, e^{-sT_s}\, K_{pwm}\, G_f(s)} \left[I_{ref}(s) - I_{com}(s)\right] \tag{6.22}$$

As described in (6.22), the proposed technique is thus capable of injecting the desired fundamental AC current into the grid, whilst robustly removing any DC current component.

6.3.4 Analysis of Offset in Current Sensor and Conditioning Circuit

In conventional output current control, offset of the current sensor and signal conditioning circuit adds an undefined DC measurement error in the controller, which ultimately has an impact on the DC injection. In DC link current sensing control, the measurement offset is defined as ΔI_{offset} , and thus the DC link current can be presented as:

$$I_{dcLink}(t) = \frac{M_i I_{AC}}{2}[1 - \cos(2\omega t)] + I_{DC} M_i sin(\omega t) + \Delta I_{offset} \tag{6.23}$$

It can be seen that this offset introduces a DC component to the DC link current measurement, whilst the DC injection I_{DC} at output is related only to the line frequency component of DC link current. Therefore, unlike conventional output current control, offset of the current sensor and signal conditioning circuit will not contribute to any DC injection to the system. Moreover, with appropriate sensor calibration [69], ΔI_{offset} can be minimized to a point where it can to all intents and purposes be neglected.

6.3.5 Analysis of the Detecting Sensitivity Compared to the Previous Study

According to the extracted DC current component I_{DE} given in (6.16), the sensitivity of the proposed DC determination can be calculated as:

$$S_c = \frac{I_{DE}}{I_{dclink}}$$

(6.24)

As prior stated that the DC link current I_{dclink} has the same amplitude as output the current I_{AC}, with an output current I_{AC} = 11.8 A (peak current of a 2 kW PV system) and a DC injection I_{DC} = 50 mA, from (6.16), the sensitivity of the DC link sensing technique is equal to:

$$S_c = \frac{\frac{2}{\pi} I_{DC}}{I_{AC}} = 2.7 \ \frac{mA}{A}$$

(6.25)

Whilst in [96], where the line-frequency DC link voltage $V_{dclinkLFripple}$ is utilized for determining the DC current injection, the sensitivity S_D is calculated as:

$$S_D = \frac{V_{dclinkLFripple}}{V_{dclink}}$$

(6.26)

Assuming the small DC link voltage ripple is precisely sensed and extracted, with grid frequency ω_g= 50 Hz, DC link capacitor C_{dclink} = 2200 μF and DC link voltage V_{dclink} = 400 V, given the same amount of DC current injection, the sensitivity of the approach S_D is calculated as:

$$S_D = \frac{\frac{I_{DC}}{j\omega_g C_{dclink}}}{V_{dclink}} = 0.18 \ \frac{mV}{V}$$

(6.27)

Regardless of the difficulties in measuring the miniscule line-frequency DC link voltage component in [96], compared (6.25) with (6.27), it is obvious that the DC link current sensing technique significantly improves the DC detecting sensitivity over DC link voltage feedback. Furthermore, as the output current restoration stated eliminates the need for output current sensor, the DC link current sensing technique is still recognized as a control-based solution, and no extra hardware is needed.

6.4 Simulation Validation

To verify the mathematical analysis, a grid-connected transformerless H-bridge inverter system with a DC link current sensor is first implemented in the simulation. The operating parameters are deliberately set to be identical to those the models designed in Chapters 4 and 5, in which the inverter system is operated from a 400 V DC link voltage and switched with a unipolar modulation at 20 kHz. With the reconstruction process and current controller, the output current at various power factors is recorded, demonstrating the effectiveness of the DC link current control technique. Meanwhile in the DC determination process, the window frequency of MAF and the cut-off frequency of digital LPF are selected at 50 Hz and 10 Hz respectively. DC determination and suppression are then verified in the same procedure, by introducing a predetermined DC into the current reference.

6.4.1 Operation of DC Link Current Control in the Simulated Inverter Model

A. Unity Power Factor Operation

Figure 6.11 shows the current operation of the simulated inverter at unity power factor. With a properly tuned controller, the DC link current control performs in the same way as in the conventional control, operating the inverter to inject an 8.3A RMS sinusoidal current into the grid. It can be seen that the output current and unity grid voltage are perfectly in phase.

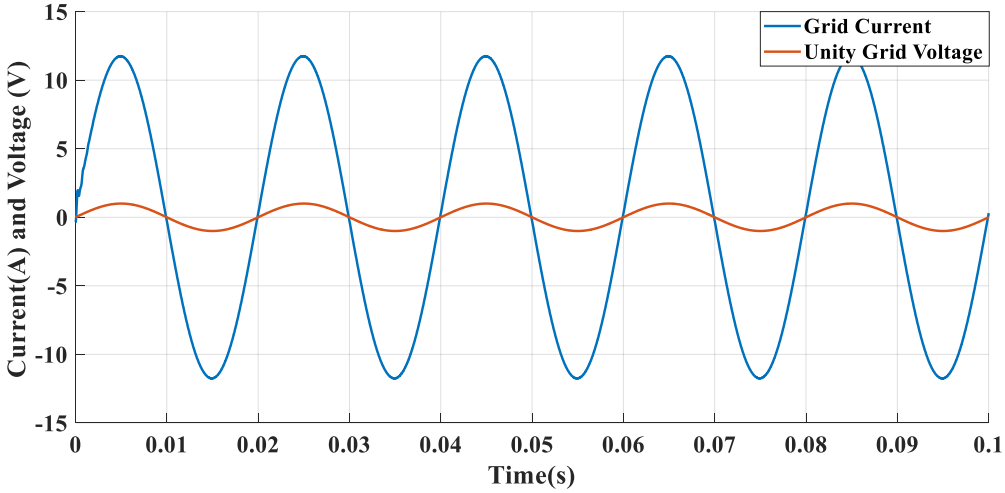


Figure 6.11 Output current and unity grid voltage at unity power factor

The DC link current measurement and post-processed currents (conducting DC link current and reconstructed current) are presented in Figure 6.12. At unity power factor, the current flowing through the DC link is a train of positive current pulses, where each pulse is characterised in terms of switching frequency and PWM demand. Through the aforementioned conducting current sampling process, the obtained a continuous half sine-wave, is the conducting DC link current shown as the red trace in Figure 6.12. With the polarity information readily available from the PWM demand, the output current is then reconstructed as shown as the yellow trace.

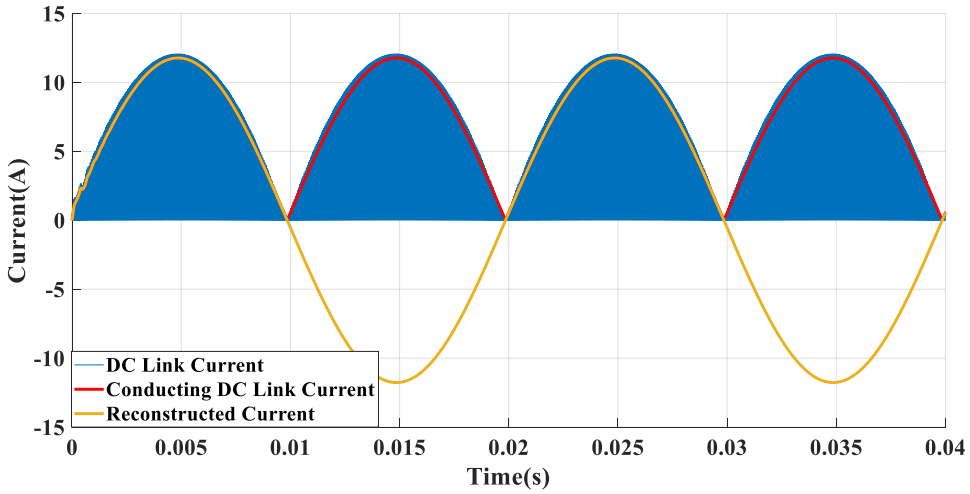


Figure 6.12 Current measurements of DC link control technique at unity power factor

B. Non-Unity Power Factor Operation

The results of the inverter operation at a power factor of 0.9 are also presented in Figure 6.13, where a phase shift is observed between the grid current and unity grid voltage. Compared with operation at unity power factor operation, in this case a short period of transient current spikes is observed before the current measurement reaches steady state. Moreover, portions of negative current appear in the steady DC link current measurements, as the PWM polarity also flips in that period while the rules of output current reconstruction remain consistently with unity power factor.

The operation of DC link current control has been validated with different power factors. Owing to the idealized simulation models, both the DC link current controller and conventional controller perform perfectly in controlling the fundamental current and suppressing the harmonics. Therefore, a more convincing comparison of the two control methods is reported in the experimental section.

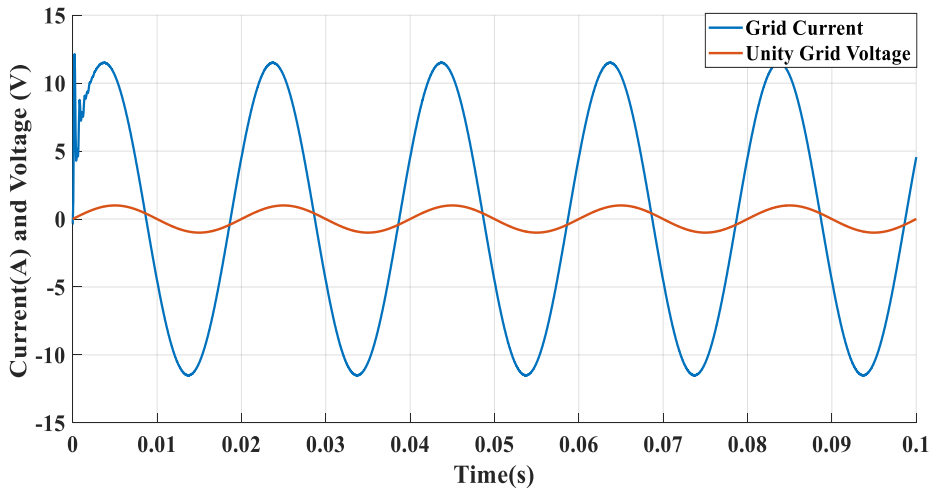


Figure 6.13 Output current and unity grid voltage at PF = 0.9

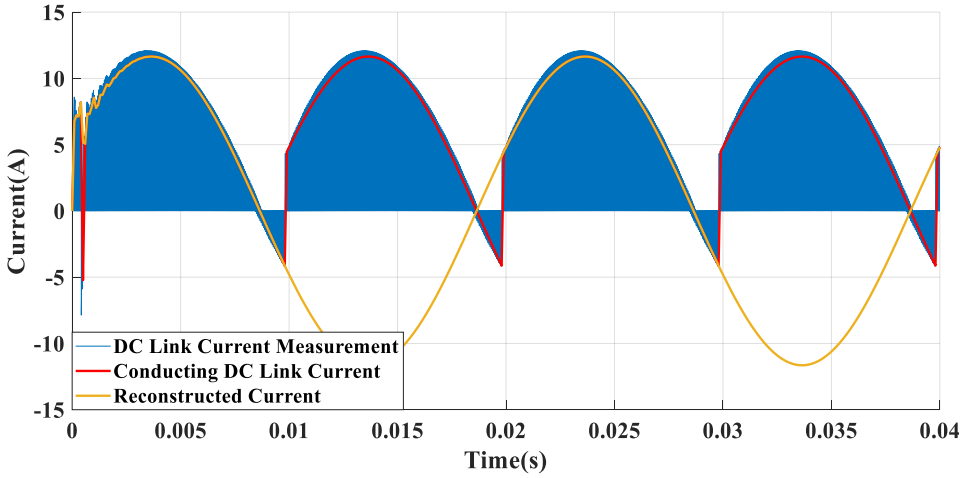


Figure 6.14 Current measurements of DC link control technique at PF = 0.9

6.4.2 Simulation Results of DC Determination

As shown in Figure 6.15, by multiplying the conducting DC link current with the sine function of the grid phase, the Fourier current I_{Ex} obtained is a periodical current with a fundamental frequency of 50Hz. As in equation (6.12), this current is a superposition of different frequencies, where the DC component is proportionally related to the DC injection. By applying the proposed digital filter, the DC component is separated from the Fourier current, therefore facilitating the determination of the DC injection.

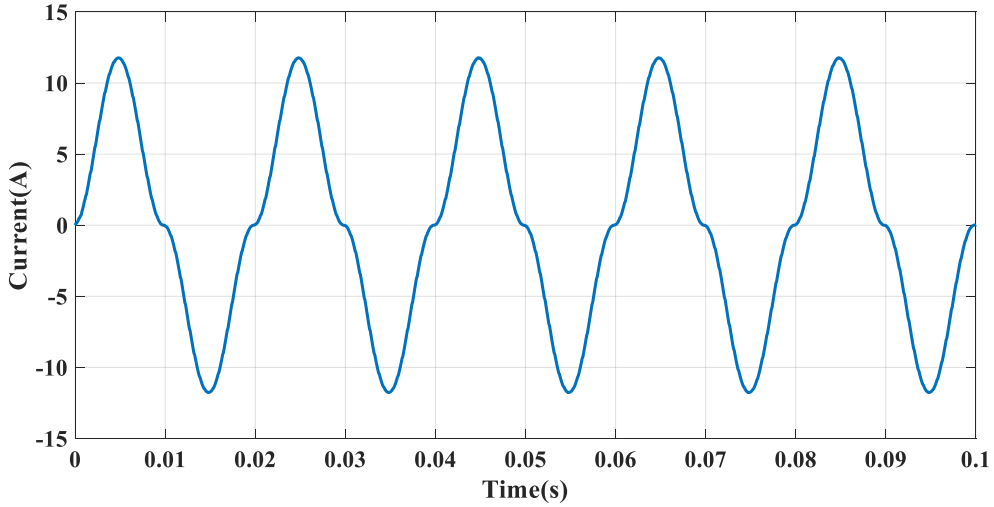


Figure 6.15 Fourier extraction current

As state earlier, the performance of the proposed DC determination can be verified by injecting a predetermined DC into the current reference. Figure 6.16 shows the DC measurement over 0.8 s. Initially, no DC is injected, and the steady calculation is effectively zero. The high overshoot in the transient response is introduced due to the accumulation period of the averaging, and it can be greatly minimised by setting a reasonable DC boundary in the experimental tests. In this case, it quickly falls back to the steady state. Given a 50 mA step-change to the DC reference at 0.3 s and 0.6s, the steady calculated DC components from the proposed technique are confirmed as 50 mA and 100 mA, with a transient delay of less than 0.1 s. Consequently, the fast and accurate response of the DC determination method is confirmed.

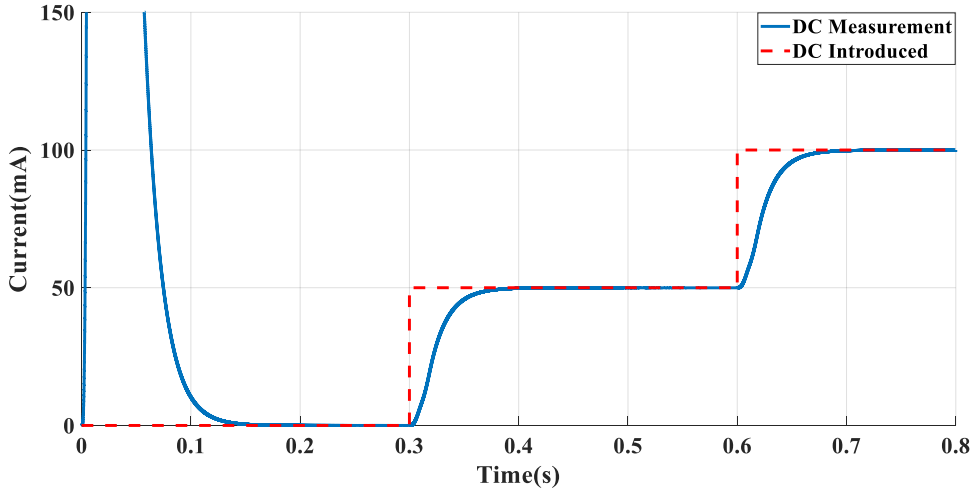


Figure 6.16 DC measurement

6.4.3 Simulation Results of DC Suppression

Figure 6.17 shows the results of DC suppression from the proposed DC link sensing technique, where a DC reference of 100 mA is introduced at 0.3 s and suppression is engaged at 0.6 s. It is clearly shown that the measurement firstly catches the predetermined DC reference, reaching a steady calculation of 100 mA. Then, at the time point of 0.6 s, suppression starts to operate. A compensation current of -100 mA is confirmed from the suppression loop, which operates the inverter to remove the DC injection in the system. At steady state, even with the injection of a 100 mA DC reference, the suppression still guarantees a DC-free output current operation.

It worth mentioning that the response time of DC determination and suppression in the DC link sensing technique is much quicker than those methods introduced in Chapter 5. This is primarily due to the different functionality of the low-pass filter. In Chapter 5, an adequate attenuation from LPF has to be applied to fit the inverter output within the ADC range; however, the DC injection here is determined from the DC link current measurement, and thus a very low cut-off frequency is not required.

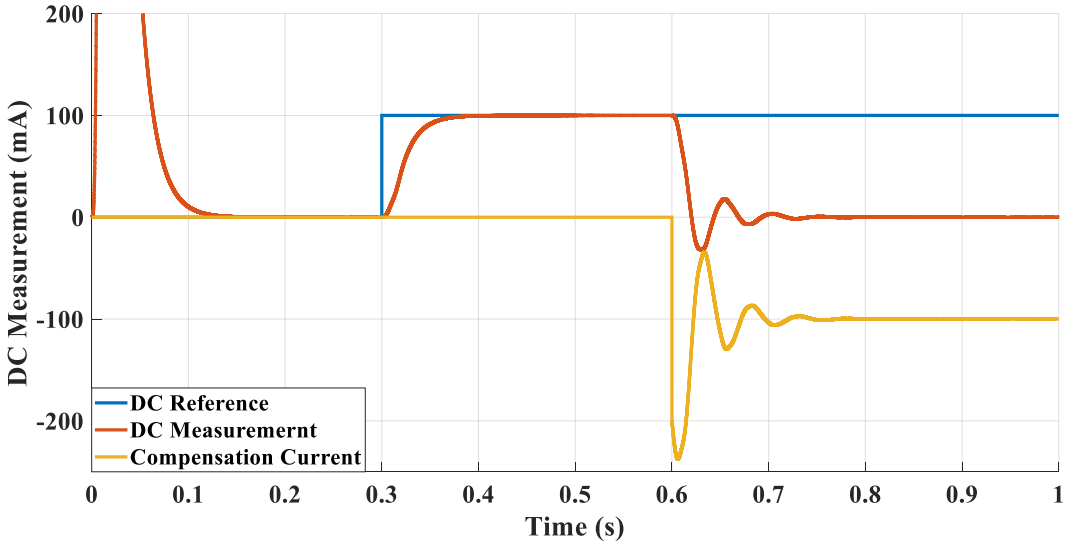


Figure 6.17 DC suppression with a DC reference of 100 mA

6.5 Experimental Results

The technique is then verified using the experimental grid-connected inverter system introduced in Chapter 4. With the same parameters as set in Table 4.1, the inverter system is operated with a 20 kHz unipolar PWM switching scheme from a 50 V DC link, and the measurements of the conventional output current sensor are also recorded for comparison purposes only. The experimental operation of DC link current control is presented in detail. Based on the aforementioned shunt external RC measurement circuit, the DC component is externally determined from the measurement of the isolated digital multi-meter, which confirms the performance of the proposed DC determination and suppression.

6.5.1 Experimental Operation of DC Link Current Control

The inverter is controlled via a proportional-resonant controller, with the parameters carefully tuned as proportional gain $K_p = 0.18$, resonant gain $K_r = 200$ and bandwidth $\omega_c = 5\, rad/s$. With a given current reference of 7.0 A, Figure 6.18 shows the inverter operation at unity power factor, in which the output current is injected with respect to the grid voltage.

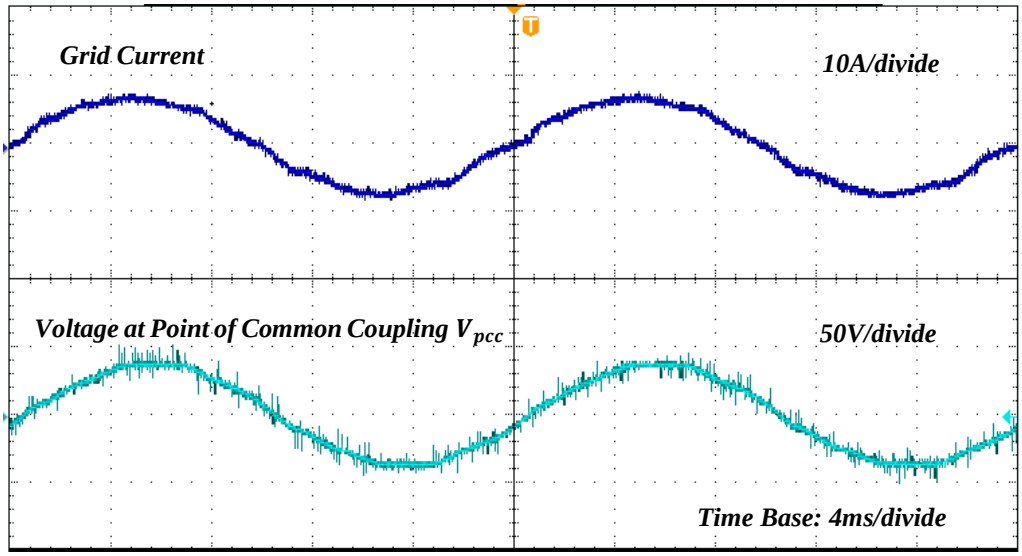


Figure 6.18 Unity power factor operation of DC link current control

As the controller is implemented with DC link current, the DC link current sensor measurement is presented in Figure 6.19, which is a series of positive PWM current pulses at unity power factor. Figure 6.20 shows the DC link current pulses with different values of PWM modulation index, in which the width of the current pulse varies with the change in modulation indices. The greater the modulation index, the wider the pulse. It is known that each pulse is characterized by the switching frequency and PWM demand. Furthermore, the transition between the freewheeling state and conducting state is represented by the rising edge of a single current pulse. There is a short period of oscillation before the pulse reaches steady state. Fortunately, according to the concept of conducting sampling, the samples are effectively taken at the mid-point of the pulses, resulting in accurate DC link current measurements.

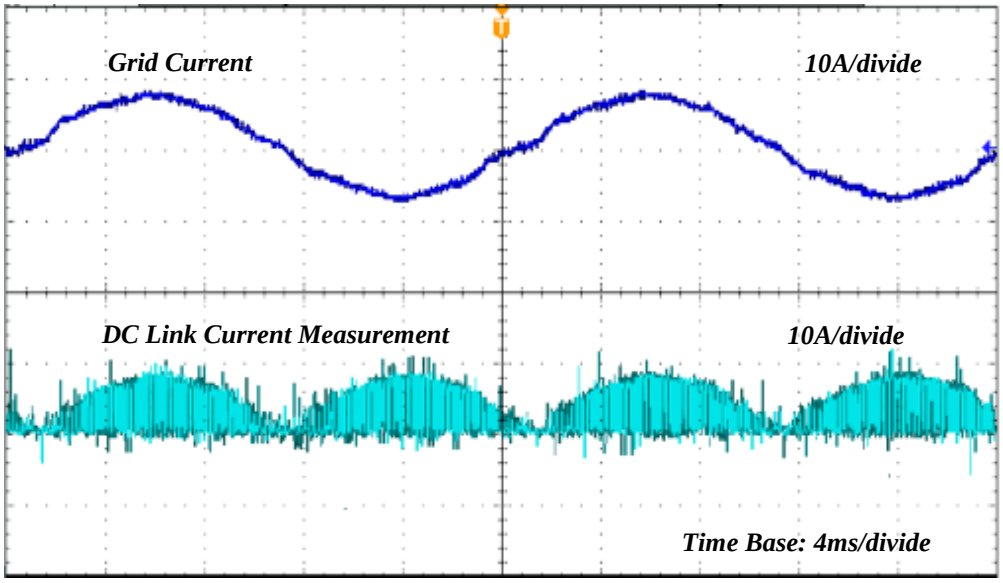


Figure 6.19 DC link current measurement over two cycles

For comparison purposes, through the use of DAC, Figure 6.21 separately shows the conducting current and software-reconstructed output current in the microprocessor. With 20k Hz sampling, the conducting DC link current waveform obtained is the mathematical absolute of output current, and the output current reconstructed from it behaves in an identical manner to the output current measurement achieved via output current sensor.

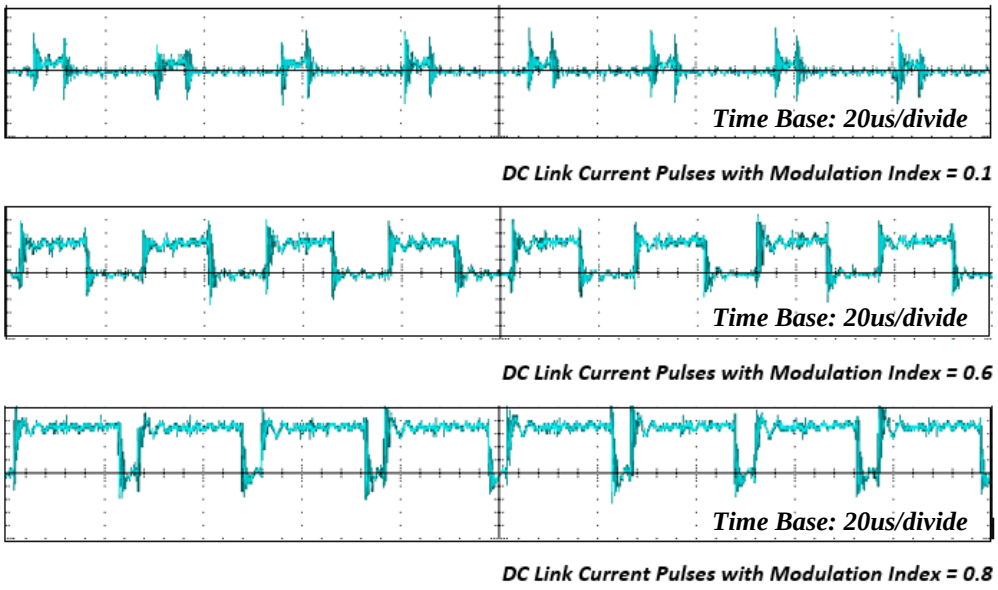


Figure 6.20 DC link current pulses with different PWM modulation index

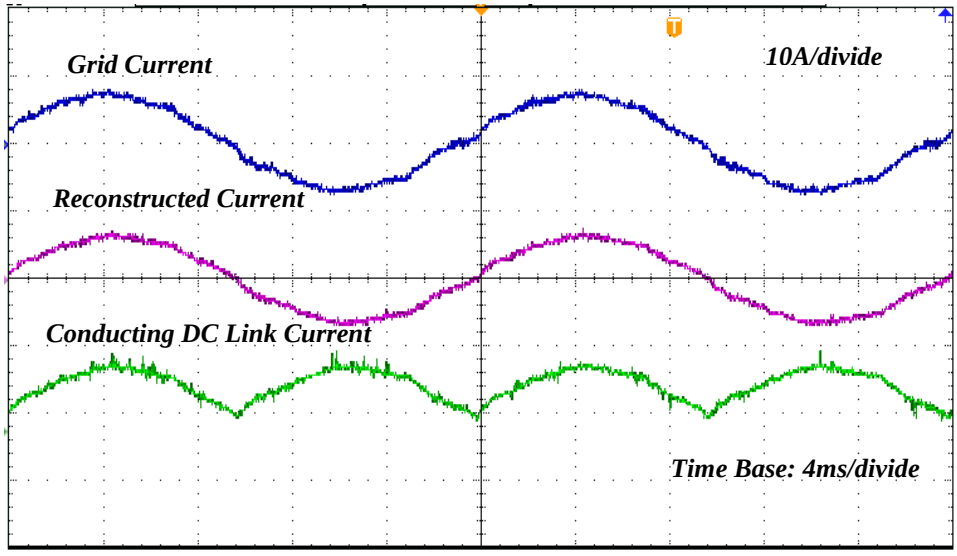


Figure 6.21 Post-processed current measurements

Validation at non-unity power factor is also confirmed when the inverter operates at a power factor of 0.9. Unlike unity power factor, the DC link current waveform now exhibits periods of negative magnitude pulses, which are measured during the conducting current period. However, from the control perspective, this is not an issue. The polarity of the PWM demand is reversed during this period, and hence the reconstruction is not affected. These are shown in Figures 6.22 to 6.24, which show great agreements with the simulation results in Figure 6.14.

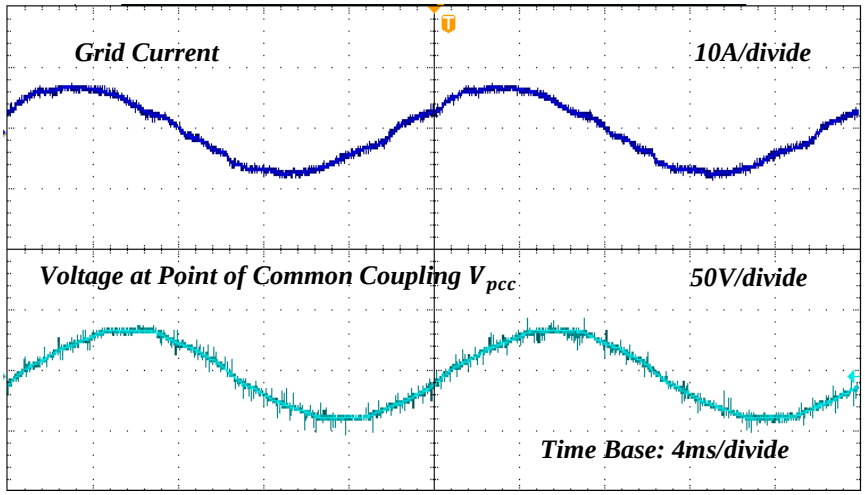


Figure 6.22 Output current and grid voltage at PF of 0.9

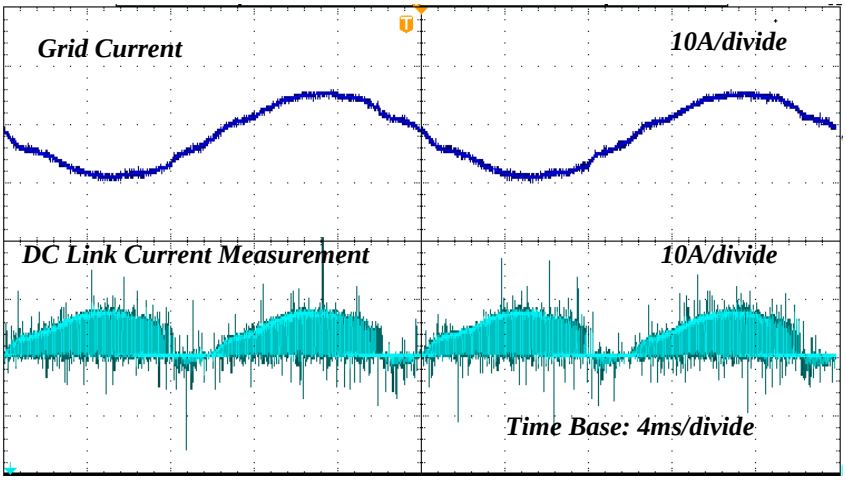


Figure 6.23 DC link current measurement at PF of 0.9

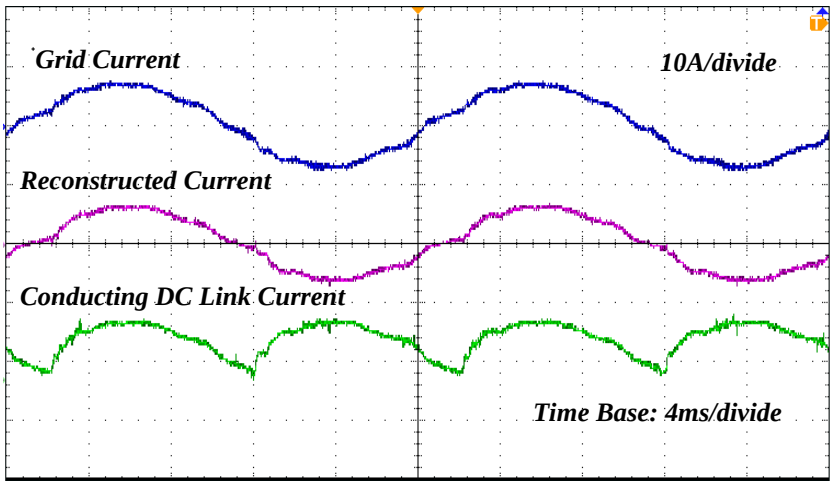


Figure 6.24 Post-processed current measurements

6.5.2 DC Determination and Suppression in the Experimental Inverter Unit

With the conducting DC link current and grid phase information accessible from previous current control, the DC injection can be accurately determined using the proposed technique. Similar to the simulation, a predetermined DC component is introduced into the system to validate the performance of DC measurement by injecting a DC bias into the current reference.

A. DC Determination

Figure 6.25 shows the introduced DC bias reference and the extracted DC current measurement using the proposed technique. To properly present the digital DC measurement from DAC, a large-scale factor of the oscilloscope is required, which inevitably leads to the probe pick-up noise in both traces. However, the noise spikes do not exist in the real digital signal. Initially, without introducing any DC current, the measured DC injection is small (within 10 mA) owing to the offset rejection of the aforementioned DC link current control. Then, a 50 mA step change bias signal is injected into the DC reference at 3.8 s, followed by a further 50 mA step at 6.0 s. As shown in Figure 6.22, the DC injection is rapidly and accurately extracted by the proposed measurement scheme. The steady state DC current measurements are confirmed as 55 mA and 105 mA, accurately matching the measurements from the external DC measurement circuit. As such, the accuracy of the DC determination is validated.

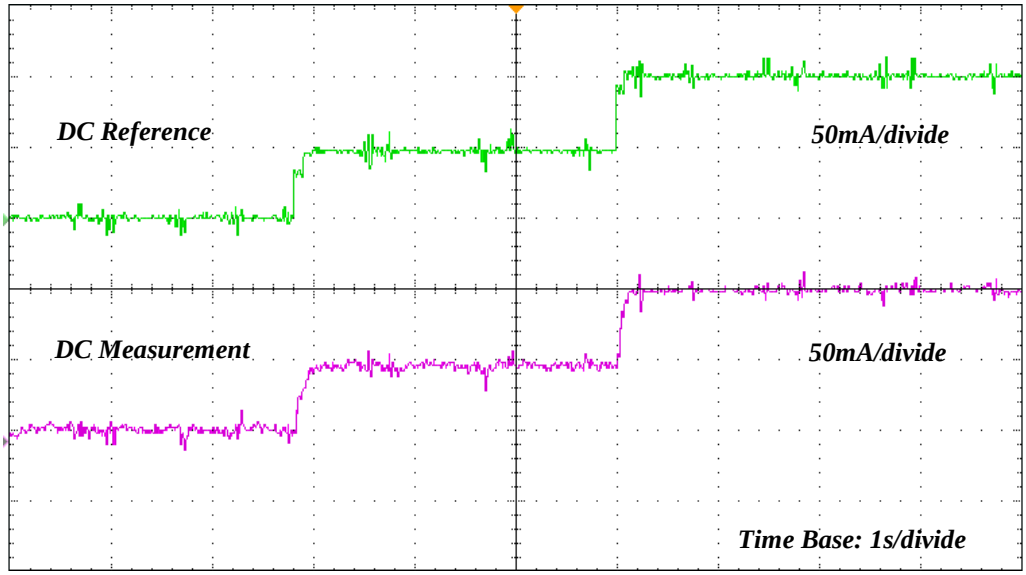


Figure 6.25 Experimental DC determination

B. DC Suppression

As the DC suppression is carried out based on real-time DC measurement, Figure 6.26 shows the compensated DC measurement when enabling the proposed closed loop suppression approach. Here, a 100 mA DC bias is added to the current reference. Through enabling the DC suppression at 6.0 s, an inverse compensation (-100 mA) is produced, which counteracts the DC injection in the system. As shown in Figure 6.26, although the 100 mA DC reference still exists, the DC measurement falls back to zero when the suppression loop is activated, thus confirming the effectiveness of the scheme.

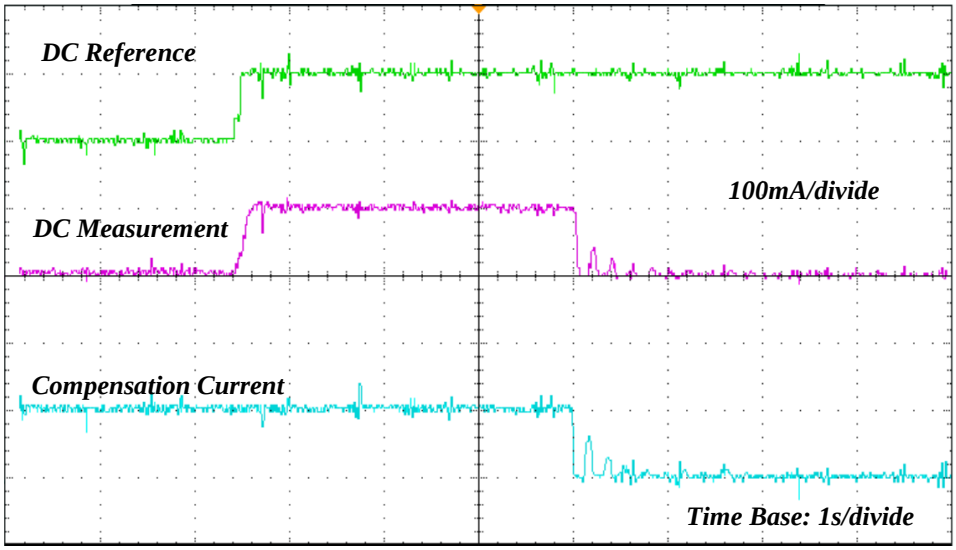


Figure 6.26 DC measurements with suppression enabled

The transient characteristics of the DC suppression approach are presented in Figure 6.27, alongside the actual output current injected into the grid. When the DC suppression mechanism is enabled, the DC component is fully suppressed within 0.1 s, demonstrating the real-time capabilities of the scheme. Meanwhile, even with a significant step in DC current component, the output current remains robust and stable. The DC measurement and suppression achieved in the experiments align with the simulation results reported in the previous section, which verifies the high-performance of the proposed DC link current sensing technique. Moreover, Figure 6.28 shows the averaged DC measurements of the conventional output current control and the proposed DC link sensing approach when gradually increasing the DC bias into the reference at various power factors. For comparison purposes, the results obtained using conventional current control are also reported.

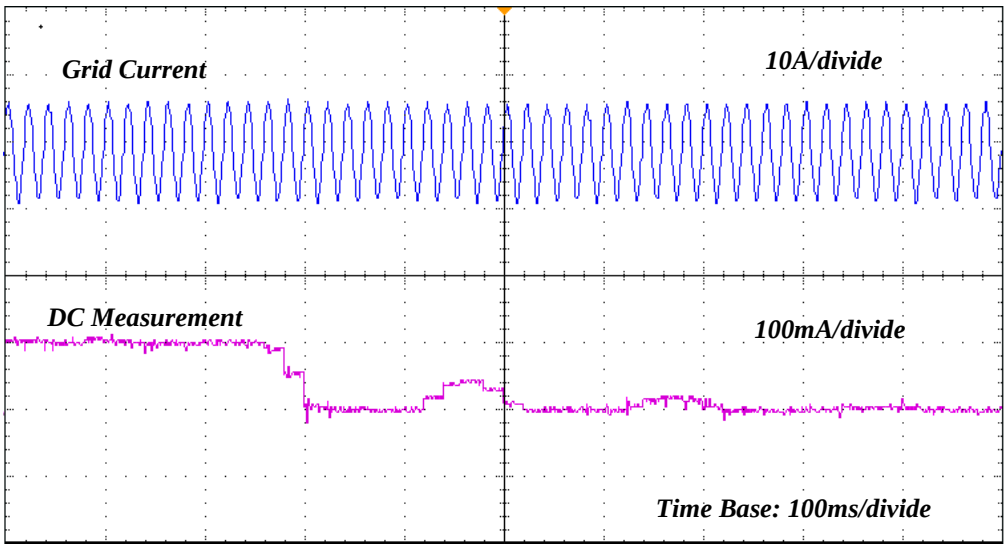


Figure 6.27 Dynamic transient of DC suppression

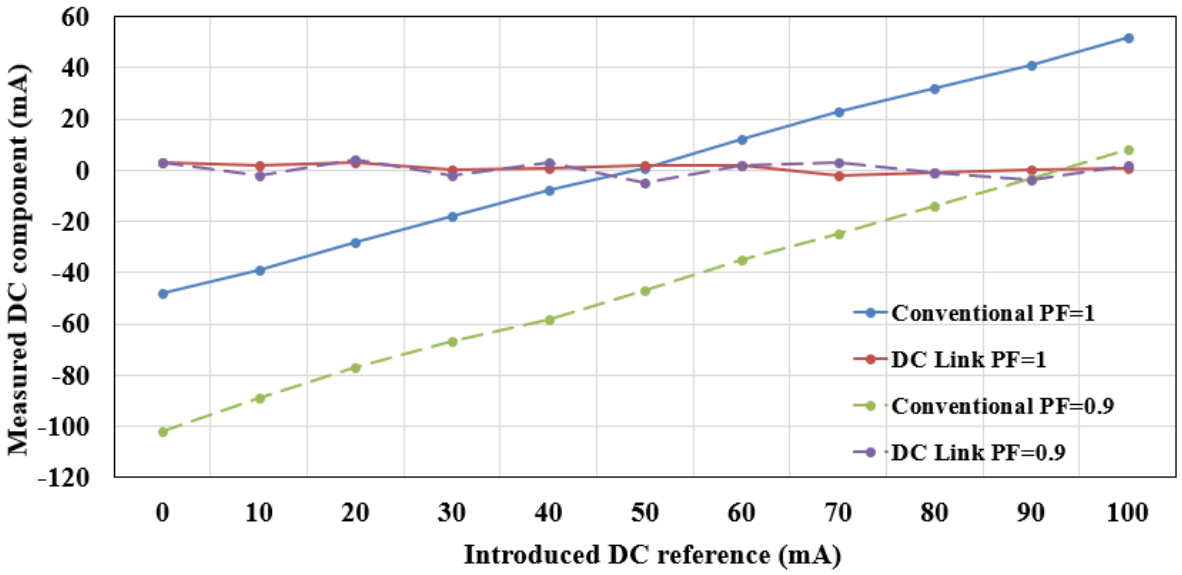


Figure 6.28 Comparison of DC measurement at different PFs

It is clear that the conventional current control is incapable of removing the DC injection, and the DC measurement varies from -100 mA to 50 mA while the DC injection is directly proportional to the bias signal imposed. However, with the DC link sensing and suppression approach, the averaged DC component is effectively limited to within 5 mA regardless of any DC current introduced. This level of performance is within the limits of most international recommendations regarding DC current injection.

C. Harmonic Analysis of Control Methods

The output current harmonic spectrum for both control techniques are recorded in Figure 6.29. Compared with the output current control which naturally contains a DC injection of 0.45%, the DC component in the proposed DC link sensing technique is greatly compensated, staying at 0%. Whilst the advantages of DC suppression are quite obvious, the DC link current control does suffer from the degradation of odd harmonics; particularly of the 7th harmonic, which is primarily a result of the grid harmonics reaching 2.7% of the fundamental. Owing to the DC component at the point of common coupling, a certain amount of even harmonics are drawn from the inverter when DC current is injected into the transformer from the utility side [60]. Nevertheless, the good performance of even harmonics still results in a total harmonic distortion (THD) of 4.65% within the standard requirement [67]. With further harmonic compensation in the current controller, the DC link current control technique is capable of injecting an offset-free AC to the utility network, with a better power quality. Figure 6.29 validates the performance of DC link current control and the suppression of DC injection.

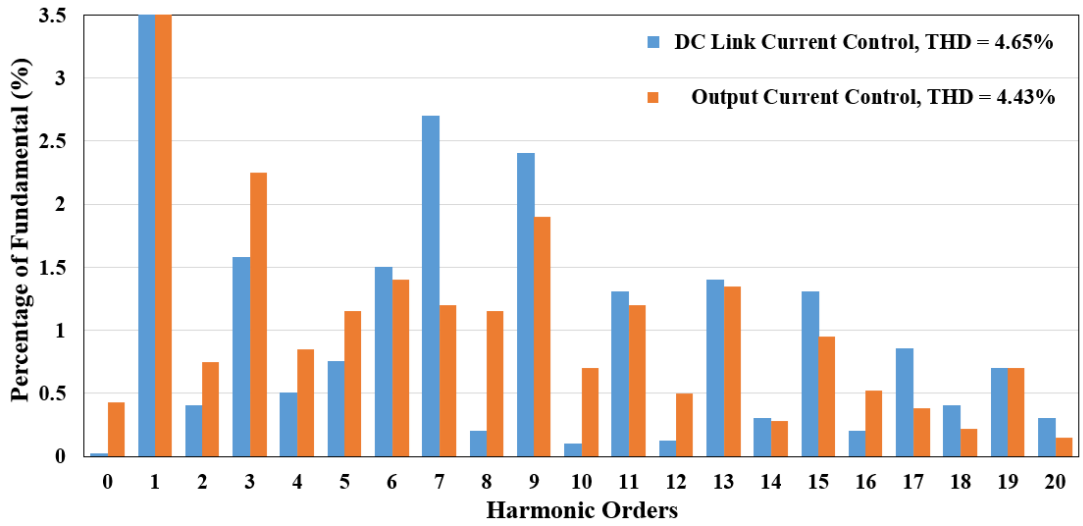


Figure 6.29 Comparison of frequency spectrum at unity power factor

6.6 Summary

This chapter presents an effective DC current suppression approach for single-phase transformerless grid-connected full-bridge inverter systems. Using a DC link current sensor, DC current injection is accurately measured by extracting the line frequency component of the DC link current waveform and it is then mitigated using an active DC suppression loop. The output current reconstruction process permits closed loop current control via the DC link current sensor, thus eliminating the need for the conventional output current sensor. Based on the switching model of the H-bridge, a full mathematical derivation and detailed analysis of the proposed DC suppression are presented. Furthermore, the performance of current control and DC suppression have been validated in simulation model and the experimental test rig. Compared with the conventional current control and the proposed DC voltage suppression method in Chapter 5, the advantages of the DC link sensing technique are summarized below:

- Low-cost: the technique includes a robust current control and an effective DC suppression, and thus, no additional hardware is needed. The harmonic performance and THD of DC link current control has been demonstrated in the experimental results.
- Effective and fast-response of DC suppression: the technique shows effective DC suppression independent of its causes. The fast-dynamic response shows the capability to compensate for a time-varying DC injection.
- Sensor-offset immunity: the DC link current control does not suffer from any measurement offset as it is the line frequency component that is related to DC injection.

All in all, the DC link sensing technique is an effective and low-cost solution for limiting DC injection in grid-connected transformerless application.

Chapter 7 Conclusions and Future Work

7.1 Conclusions

While a growing number of cost-effective transformerless power converters are being used in small-scale renewable energy systems, power quality issues brought about by the absence of galvanic isolation have been well recognized. In particular, the potential risk of DC current flowing into the network remains a significant concern. This may arise due to the asymmetrical operation of gate drives, non-identical characteristics of semiconductor switches and the non-linearity and offset drift of current transducers. Furthermore, excessive DC current from multiple grid-connected inverter units may saturate the power transformer in the grid, increase power losses, and degrade power cables over time. Although much research has been proposed to detect or suppress DC current injection in recent years, technical challenges and implementation issues still remain, which are highlighted in this thesis. This has been the motivation of the research that aims to guarantee high-quality grid operating condition when increasing the number of the connected transformerless distributed renewable generators.

In order to thoroughly analyse the controllers' performance, a grid-connected inverter is first mathematically modelled, which is then developed into a simulation model and implemented experimentally. The advantages of PR controller in tracking AC current reference and harmonic mitigation have been confirmed, whereas the existence of DC current injection is observed regardless of the use of PI or PR controller. As a result, the present research focuses on the minimization of DC current injection in grid-connected PV inverter systems. Since complete DC mitigation via conventional current control is particularly challenging, two different approaches, a DC voltage mitigation approach and a DC link current sensing technique, are developed in this thesis to regulate the DC component at the level of the individual inverter unit. The DC voltage mitigation approach aims to improve the accuracy and sensitivity of DC voltage extraction at the inverter output. The passive attenuation circuit resolves the problem of common-mode voltage without losing accuracy, whilst the use of a secondary digital filtering stage takes up some of the burden of the passive filter, achieving a more precise DC extraction. This allows for further control and compensation simply via a DC suppression loop. As the approach is directly connected to the inverter output, it is not specific to any power converter topology, which also can be used for DC measurement or mitigation in different grid applications such as distribution power transformers.

On the other hand, the DC link current sensing approach is a cost-effective control-based solution for grid-connected full-bridge systems. The DC current injection is determined by extracting the line frequency component of the DC link current waveform and then mitigated via the use of an active DC suppression loop. Furthermore, the output current reconstruction process permits closed-loop current control via the DC link current sensor without requiring a conventional output current sensor, and its high sensitivity and offset immunity have been proven.

The theoretical analyses have verified the proposed DC suppression methods, whose performance are further confirmed by simulation models in MATLAB/Simulink and experimental results from the laboratory inverter unit. In specific, while a DC injection of -55 mA is measured by using conventional control in the experimental inverter unit, both proposed DC suppression approaches are capable of limiting the DC current in the output within 5mA, achieving a 90% DC rejection. In addition, this level of suppression is confirmed even with a given DC offset into the reference. The excellent DC regulation meets the DC requirements in all international grid interconnecting guidelines and standards.

In conclusion, although the DC voltage mitigation approach requires for an isolated passive attenuation circuit, which increases the cost of the overall system in some extent, compared with published methods, it is still a simple, effective and high-accuracy solution that is applicable for all grid-connected inverter systems. In contrast, the DC link sensing technique is recognized as a cost-effective, software-based solution for H-bridge applications, which robustly injects high-quality AC current to the network with real-time DC current rejection. Consequently, it is convinced that the present research significantly improves grid operating conditions and facilitates the development of PV power converters, which makes a positive contribution in the area of the power quality control of grid-connected transformerless inverter systems.

7.2 Future Work

Based on the work presented in this thesis, some further research areas are suggested as follows:

- Modification of conventional current controller - PIR Controller

The performance of the conventional PI/PR controller has been investigated in the thesis. To improve the power quality control of grid-connected transformerless inverter systems, an investigation of the combination of conventional PI and PR control, referred to as a PIR controller, is suggested in future work. Such a combination would involve a decent DC gain owing to the

integration, and in the meantime it would preserve the characteristics of harmonic mitigation and sinusoidal reference tracking. Although this type of controller still suffers from measurement noise and non-linearity issues, it would be interesting to investigate how much this type of controller could improve the power quality in the DC link current control.

- Optimization of sampling process in grid-connected PV inverter systems.

From the experimental results, the change in sampling points over the triangular carrier has an impact on DC injection at the inverter output. By changing the sampling point, a variation in dc current up to 50 mA in the output current is confirmed by the external RC circuit that. Future work is suggested to investigate the reason behind, and therefore optimizing the sampling process in the grid-connected PV inverters.

- Operating the experimental inverter unit at rated power level.

The experimental inverter unit is currently operated from a DC link voltage of 50 V and connected to the grid via variac. Although the concept of the proposed DC determination and suppression methods can be proven with such voltage levels, it is still suggested to elevate the operating voltage to rated level in future work. In addition, to improve common-mode performance at rated voltage level, the practical arrangement needs to be carefully modified, such as using split inductors to minimize the EMI issue.

- Widespread applications for DC voltage mitigation approach

The DC voltage offset has significant impacts on the distribution transformers and loads in the grid. As the DC voltage mitigation approach is not only limited to grid-connected inverter applications, it can also be used to compensate for the DC bias in the distribution transformer, or the DC voltage offset at the point of common coupling in the power grid.

- Expanding topological applications for DC link sensing technique

The DC link current sensing technique can be applied to different topologies. For example, in three-phase H-bridge inverter systems, each phase current can ideally be achieved by sampling the DC link current waveform at specific points with the same reconstruction process as previously stated, therefore eliminating the need for three current sensors at the inverter output. Meanwhile, these DC link current measurements can be used to determine the DC current injection. Similarly, this technique is suggested for three-level diode-clamped inverters or other widely adopted topologies.

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Appendix A Full Derivation of LCL Transfer Function

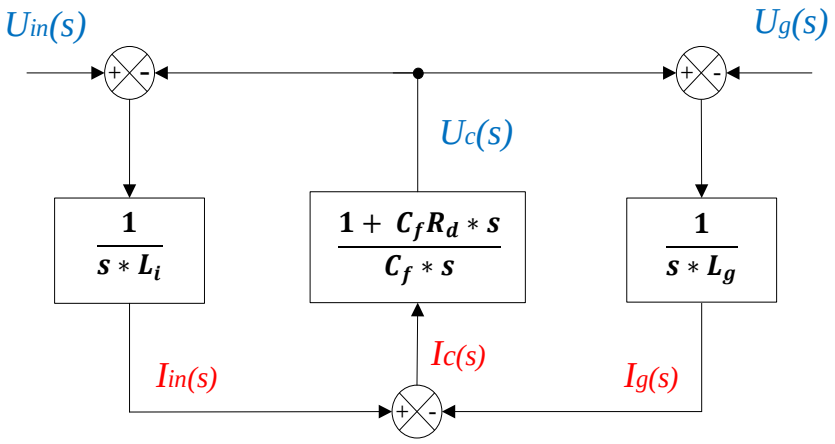

Figure A.1 Mathematical model of LCL filter

Based on mathematical model of LCL filter in Figure A.1, the full derivation of LCL filter can be presented as follows:

$$U_{in}(s) - U_g(s) = sL_{in}\, I_{in}(s) + sL_g[\, I_{in}(s) - I_c(s)]$$

$$U_{in}(s) - U_g(s) = sL_{in}\, I_{in}(s) + sL_g[\, I_{in}(s) - \frac{U_{in}(s) - sL_{in}I_{in}(s)}{R_d + \frac{1}{C_f s}}]$$

$$U_{in}(s) - U_g(s) = sL_{in}\, I_{in}(s) + sL_g I_{in}(s) - L_g s\, \frac{U_{in}(s)}{R_d + \frac{1}{C_f s}} + L_g s\, \frac{sL_{in}I_{in}(s)}{R_d + \frac{1}{C_f s}}$$

$$U_{in}(s) - U_g(s) = sL_{in}\, I_{in}(s) + sL_g I_{in}(s) - \frac{L_g C_f s^2}{C_f R_d s + 1} U_{in}(s) + \frac{L_g C_f L_{in} s^3}{C_f R_d s + 1} I_{in}(s)$$

Rearranging the input $U_{in}(s)$, $U_g(s)$ and output $I_{in}(s)$, yield:

$$U_{in}(s) + \frac{L_g C_f s^2}{C_f R_d s + 1} U_{in}(s) - U_g(s) = sL_{in}\, I_{in}(s) + sL_g I_{in}(s) + \frac{L_g C_f L_{in} s^3}{C_f R_d s + 1} I_{in}(s)$$

$$\left(1 + \frac{L_g C_f s^2}{C_f R_d s + 1}\right) U_{in}(s) - U_g(s) = (L_{in}s + L_g s + \frac{L_g C_f L_{in} s^3}{C_f R_d * s + 1})\, I_{in}(s)$$

$$\left(\frac{1 + C_f R_d s + L_g C_f s^2}{C_f R_d s + 1}\right) U_{in}(s) - U_g(s) = (L_{in}s + L_g s + \frac{L_g C_f L_{in} s^3}{C_f R_d s + 1})\, I_{in}(s)$$

$$U_{in}(s) - \frac{C_f R_d s+1}{1+C_f R_d s+L_g C_f s^2} U_g(s) = \frac{L_{in}s+L_g s+L_{in}C_f R_d s^2+L_g C_f R_d s^2+L_g C_f L_{in} s^3}{C_f R_d s+1+L_g C_f s^2} I_{in}(s)$$

$$\frac{I_{in}(s)}{U_{in}(s)-\frac{C_f R_d s+1}{1+C_f R_d s+L_g C_f s^2}U_g(s)} = \frac{C_f R_d s+1+L_g C_f s^2}{L_{in}s+L_g s+L_{in}C_f R_d s^2+L_g C_f R_d s^2+L_g C_f L_{in} s^3}$$

$$\frac{I_{in}(s)}{U_{in}(s)-\frac{C_f R_d s+1}{1+C_f R_d s+L_g C_f s^2}U_g(s)} = \frac{C_f R_d s+1+L_g C_f s^2}{C_f L_{in} L_g s^3+(L_g+L_{in})C_f R_d s^2+(L_g+L_{in})s}$$

(A.1)

Figure A.2 shows the bode plot of grid voltage factor ($\frac{1+C_f R_d s+C_f L_{in} s^2}{C_f R_d s+1}$), in which the magnitude and phase angle at line-frequency are zero. Therefore, this grid voltage factor equivalently equals to a unity static gain, and the transfer function of grid-side current and voltage inputs can be simplified as:

$$\frac{I_g(s)}{U_{in}(s)-U_g(s)} = \frac{C_f R_d s+1}{C_f L_{in} L_g s^3+(C_f R_d L_g+C_f R_d L_{in})s^2+(L_g+L_{in})s}$$

(A.2)

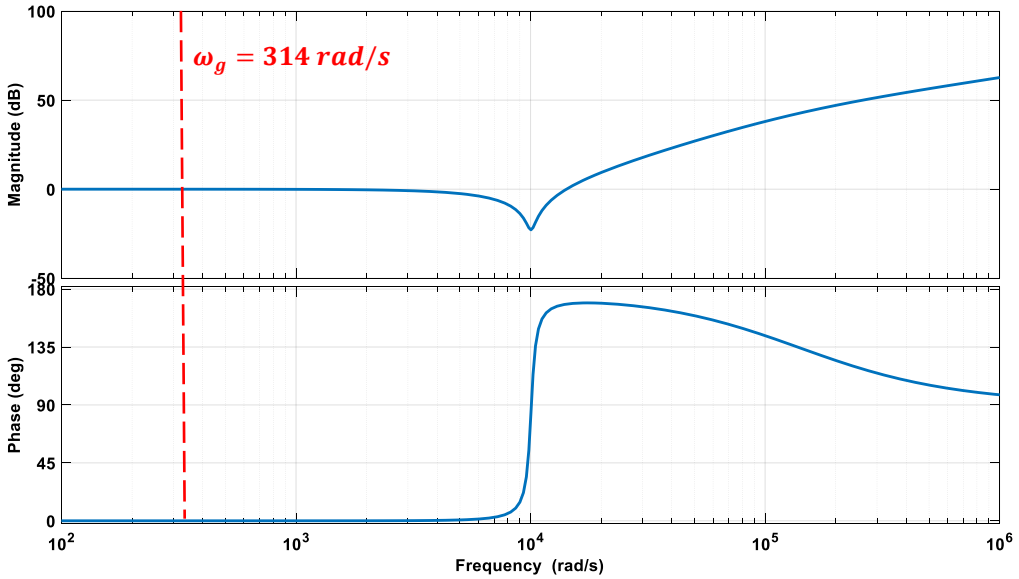

Figure A.2 Bode plot of grid voltage factor

Appendix B MATLAB/Simulink Models in the Thesis

B.1 Simulation models of Transformerless Grid-Connected H-bridge Inverter

The MATLAB/Simulink model of grid-connected H-bridge inverter is presented with including the possible dc injection sources, such as: measurement offset and imbalance voltage drop.

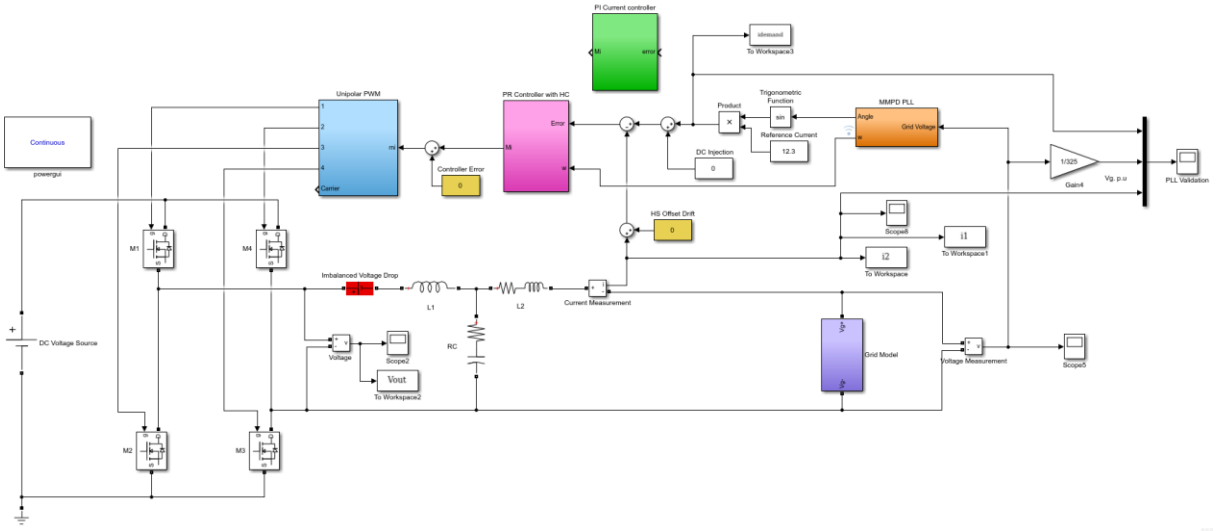

Figure B.1.1 An overview of transformerless grid-connected inverter

The implementation of Unipolar PWM scheme in Simulink with considering dead-time effect.

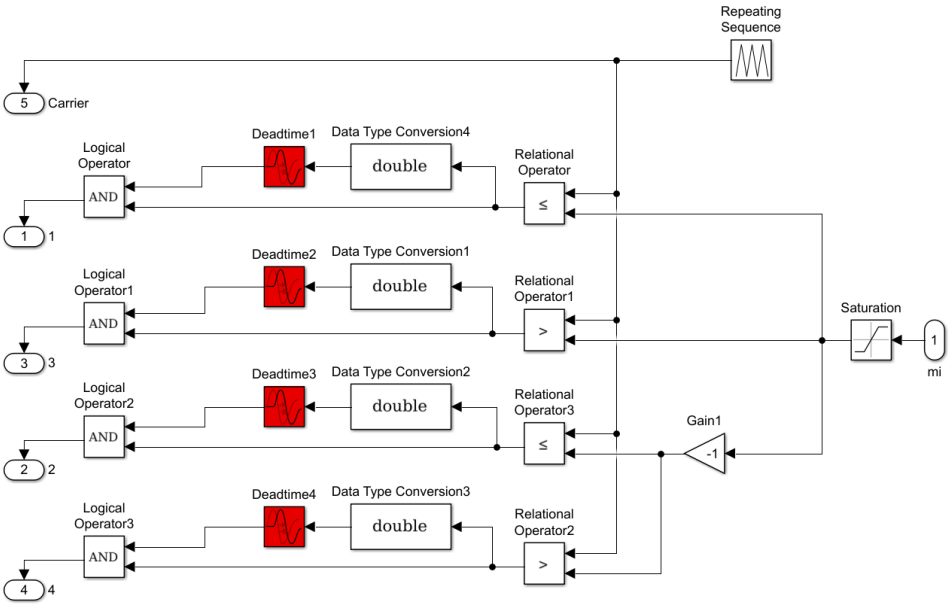

Figure B.1.2 Unipolar PWM scheme with considering dead-time effect

The model below shows the implementation of MMPD technique for grid synchronization.

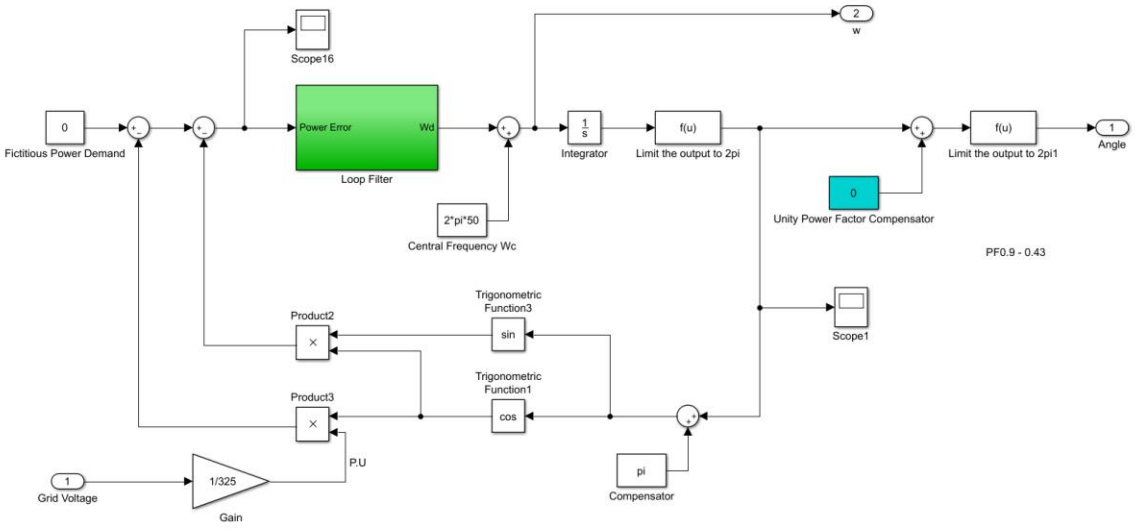

Figure B.1.3 Simulation model MMPD pPLL technique

The model below shows the grid model developed based on the data harmonics of laboratory grid voltage.

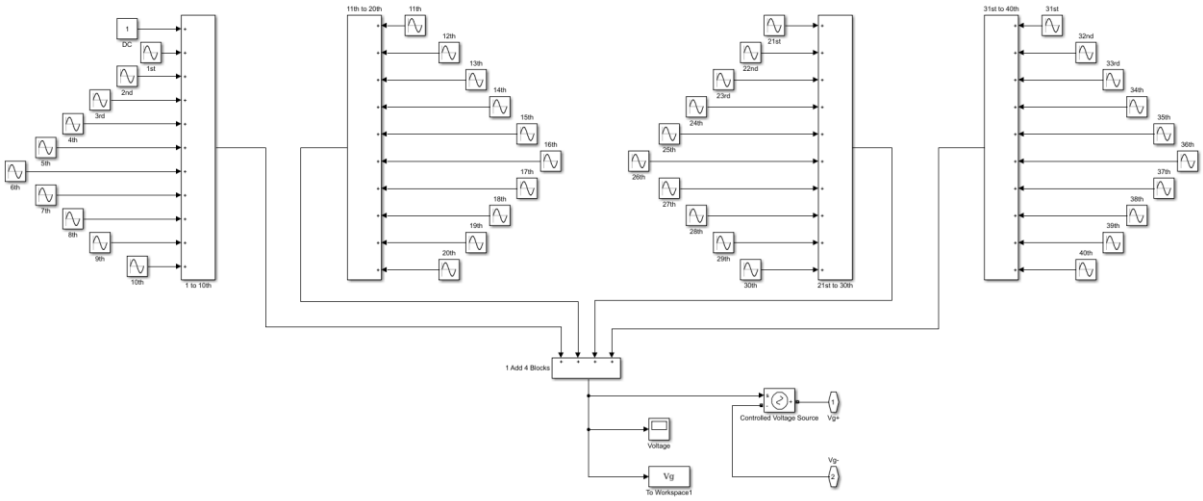

Figure B.1.4 Grid model based on laboratory data

B.2 Simulation model of DC Link Sensing Technique

The MATLAB/Simulink model of grid-connected H-bridge inverter using a dc link sensing technique is presented, where the output current measurement is only used for power quality analysis.

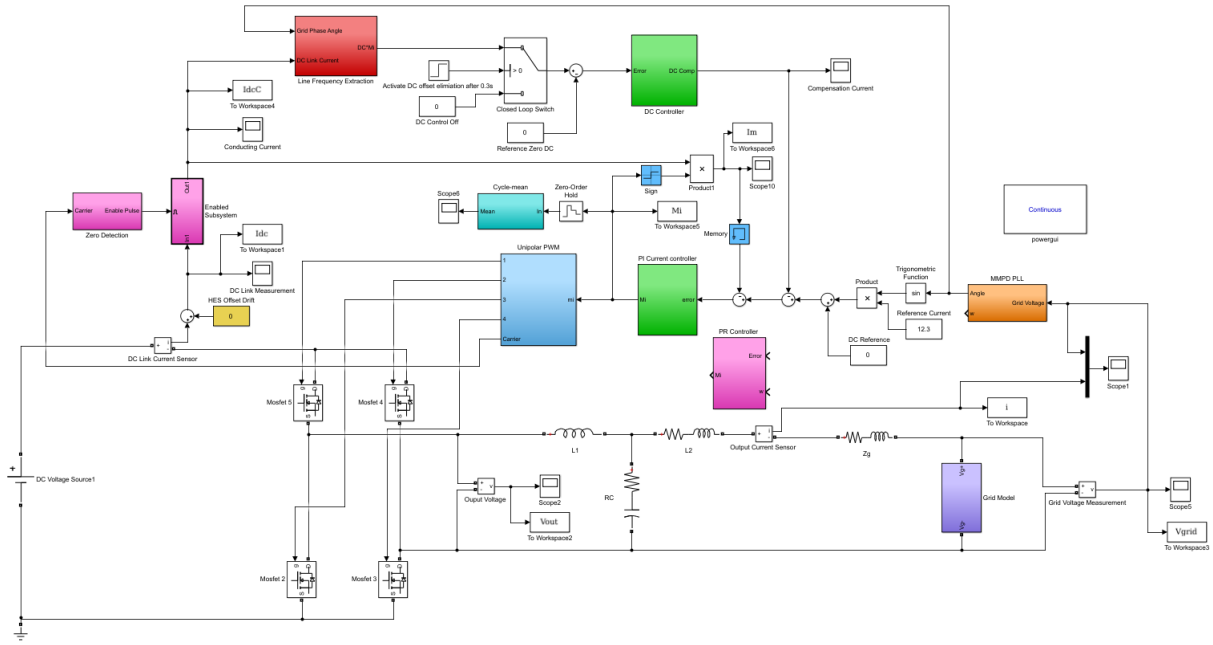

Figure B.2.1 An overview of grid-connected inverter using DC link sensing technique

The model below shows the generation of conducting sampling enable signal.

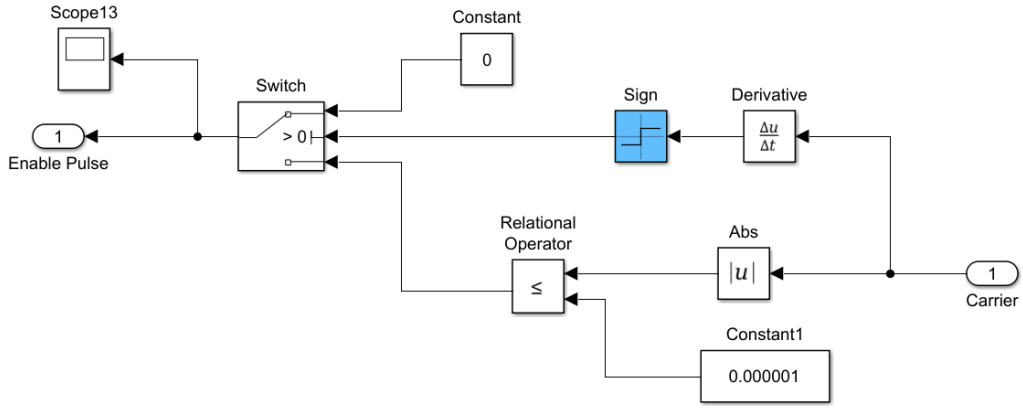

Figure B.2.2 Conducting sampling enable

The model bellows shows the digital Line-frequency extraction from conducting dc link current measurement.

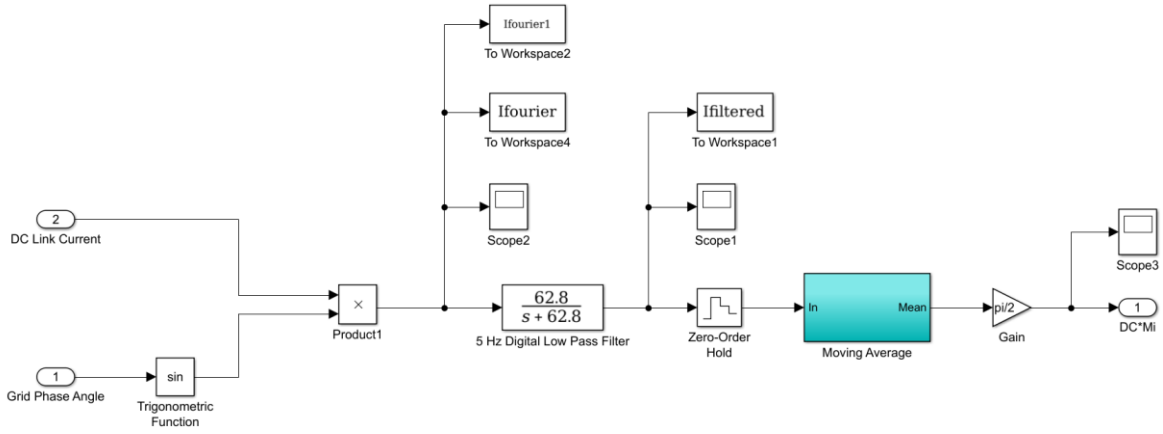

Figure B.2.3 Proposed line frequency ripple extraction

Appendix C Schematics and PCB Design

In this research, two electronic circuits, namely passive attenuation circuit and H-bridge with including DC link sensor, are designed by author using Multisim and Ultiboard. Their schematics and PCB layouts are shown below.

C.1 Schematic of DC Link H-bridge Inverter

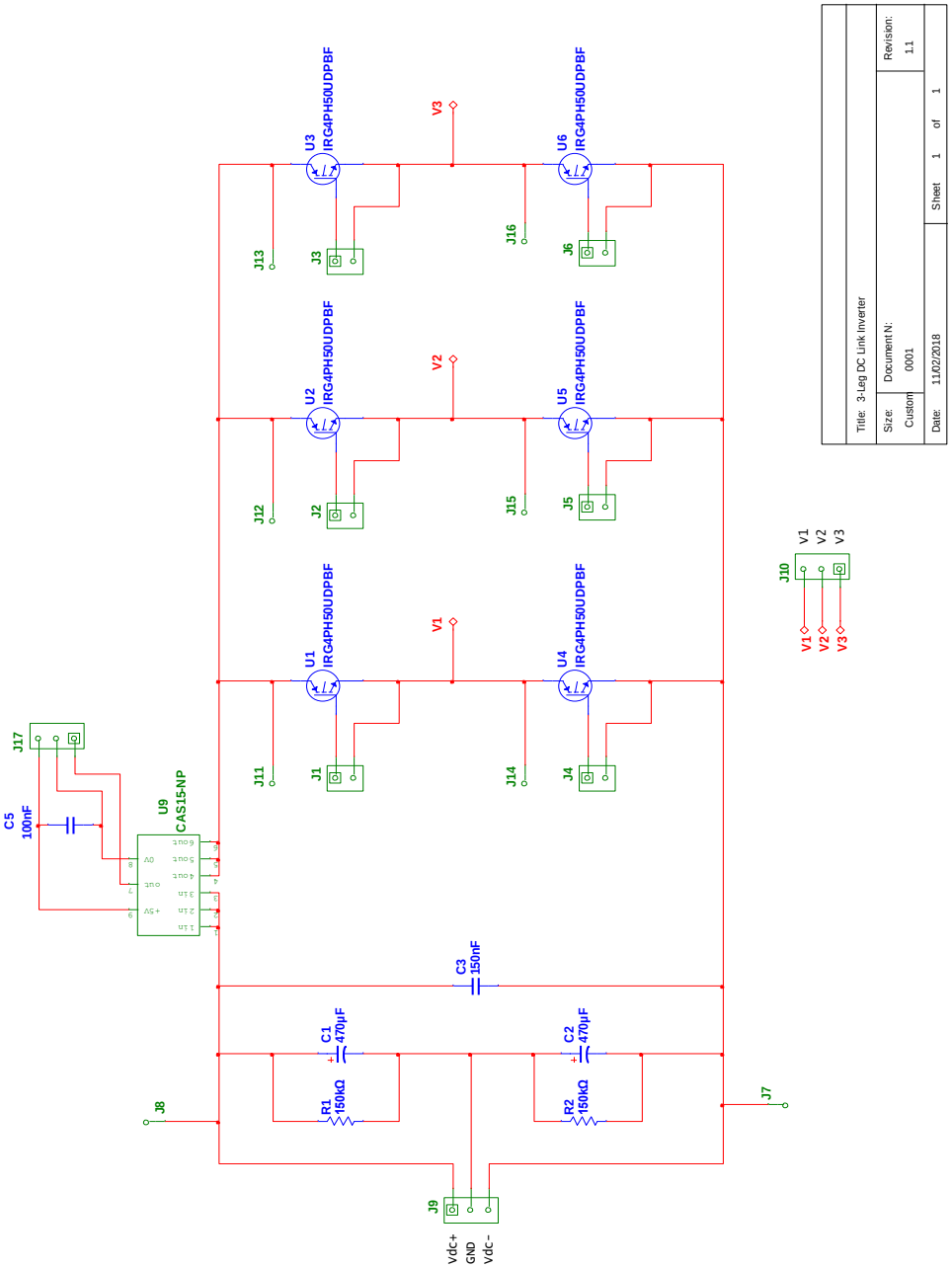

Figure C.1 Schematic diagram of three leg DC link H-bridge inverter in Multisim

C.2 Schematics and PCB Design of Passive Attenuation Circuit

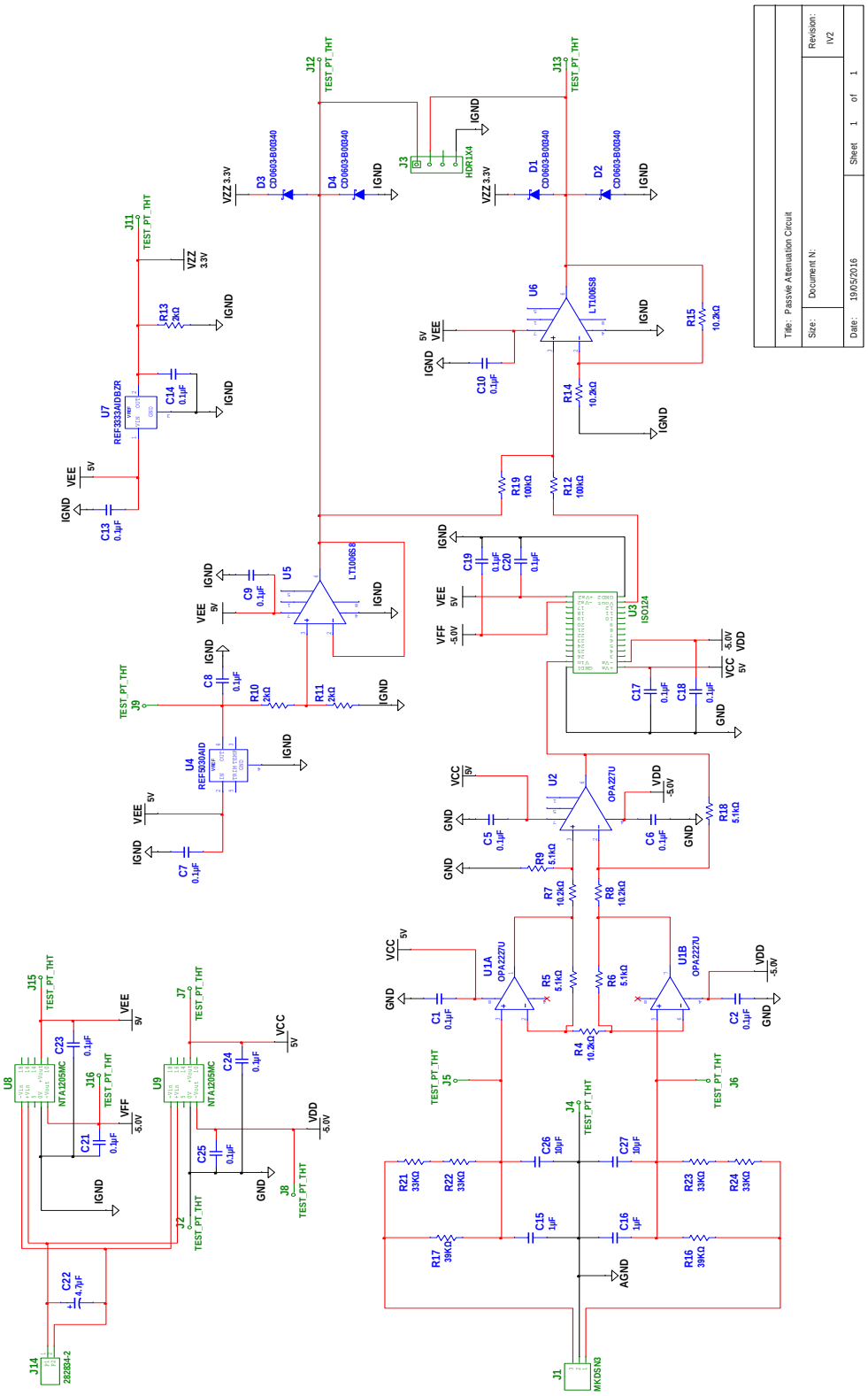

Figure C.2 Schematic diagram of passive attenuation circuit in Multisim

C.3 PCB Design of DC Link Inverter and Passive Attenuation Circuit

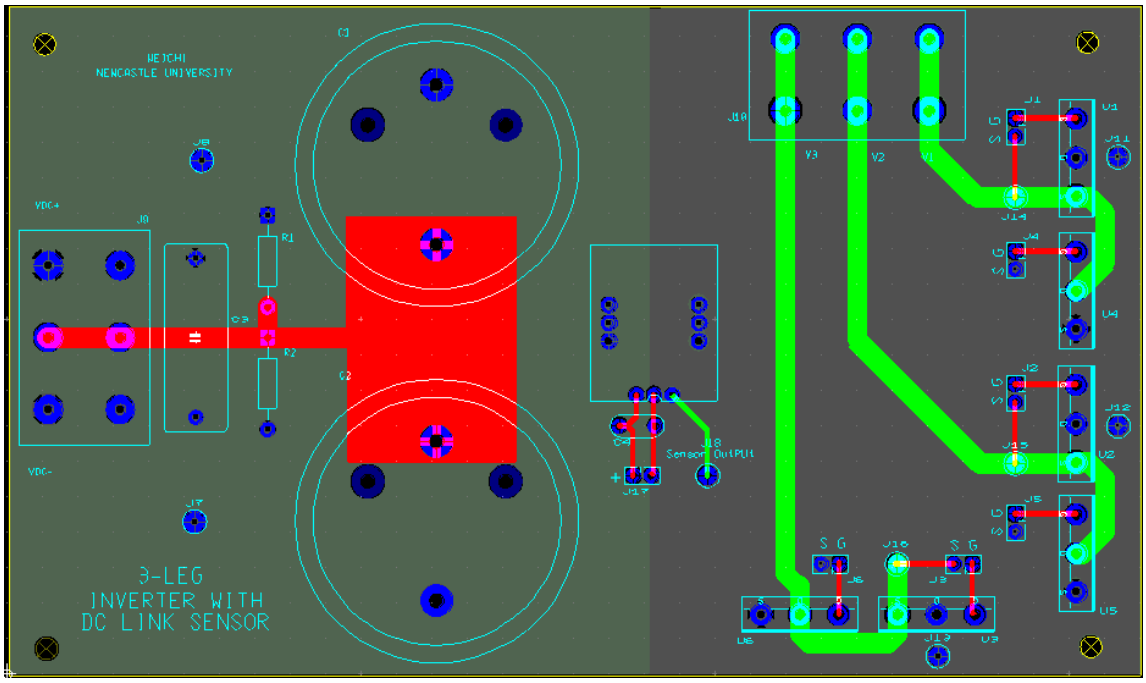

Figure C.3.1 PCB design of DC link inverter

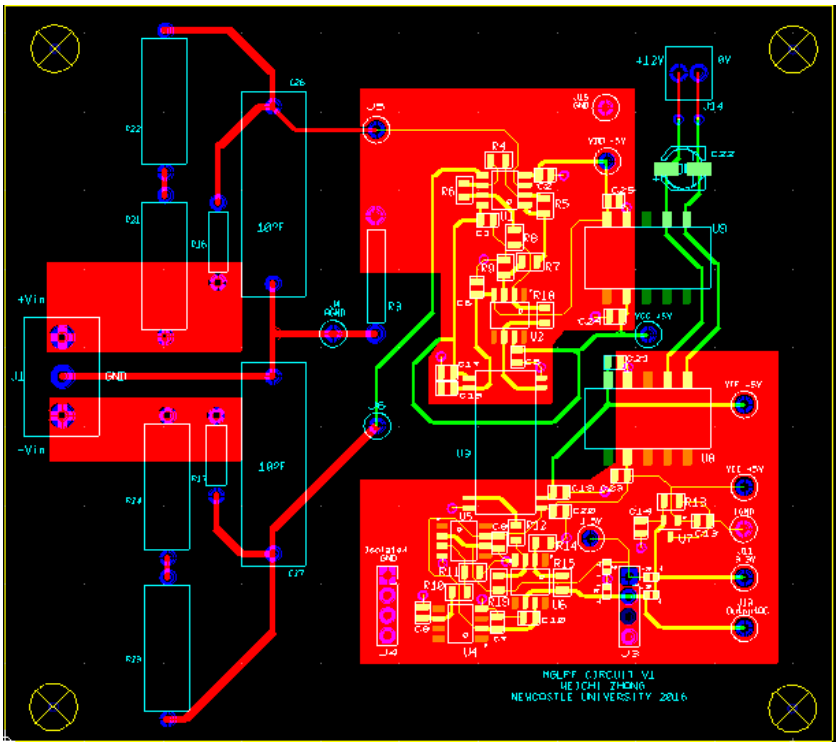

Figure C.3.2 PCB design of passive attenuation circuit

Appendix D Software Control Code

TMS320F28377D is dual-core microprocessor where each of the two CPUs has an associated control law accelerator (CLA) that acts as an independent processing core. It is a 32-bit, float-point processing unit which has equal computational capability to the CPU. In this project, only CPU1 and its associated CLA are used to carry out the converter control. Whilst the variable definitions such as the statements associated with CPU and CLA communication and appropriate configurations and initialization functions for the registers such as system clocks, peripheral interrupt expansion (PIE), ADC, DAC, GPIO and ePWM are implemented in the in CPU1, the converter control algorithms and sample data processing are carried out in the highest priority task Cla1Task1 of CLA to allow for a computational enhancement during each interrupt execution.

The following shows the code of converter functions (sample processing, PLL, current controller, proposed DC extraction techniques associated with suppression, etc.) that are executed during the interrupt.

```
// CLA1 C Task prototypes
__interrupt void Cla1Task1();
__interrupt void Cla1Task2();
__interrupt void Cla1Task3();
__interrupt void Cla1Task4();
__interrupt void Cla1Task5();
__interrupt void Cla1Task6();
__interrupt void Cla1Task7();
__interrupt void Cla1Task8();

// Task definitions
//-----------------------------------------------------------------------------
// At present this CLA task is used for inverter control

interrupt void Cla1Task1 (void)
{
      float kpc,kic;                          // Kp and ki for current controller
      float k_pll;                            // Static gain of OSG-SRF PLL
      float vd,vq;                            // rotating-frame dq voltage in PLL
      float i_demand;                         // Sine Demand Current
      float i_error;                          // Current error
      float iex_3;
      float iaverage_c;      // DC Measurement before compensation in DC Link Sensing
      float vaverage_c;      // DC Measurement before compensation in MGLPF
      int ipi_md;
      int ipi_m;                               // Modulation index of PI Controller
      int theta_3;                             // Angle in Open loop
      float dc_error;                          // DC error in DC suppression loop
      float kpd,kid;                           // PI Controller in Suppression Loop
```

```
    //float vgpu;                                 // Grid Voltage per unit
// Kp and Ki for PLL, kts- integration gain for digitized integrator
      float kpp,kip;
    //float p_error;                              // error in pll
    //float wf;                                   // grid frequency in Herz
      float ppll;                                 // Generate power pll
      float e_pll1,e_pll2;                        // Error in QSG
      float wc_r;                                 // 2*wc in PR controller
        float kp_r,kr_r;                    // Kp and Kr in the PR Controller
        float pr_error1, pr_error2;         // Error 1 and Error2 in the PR Controller

// Set test point high (HSEC-100) for execution time measurements
       GpioDataRegs.GPBSET.bit.GPIO54 = 1;

       __mdebugstop();

#if EMULATOR // Get sensor data from plant emulator on CPU2
       sen1 = iaM;
       sen2 = ibM;
       sen3 = icM;
       isoamp = vdcM;
#else
// get sensor data (CLA1 can access ADCs directly)
         sen1 = AdcaResultRegs.ADCRESULT0;     // Sensor1  (J17-1)      (HSEC-15)
         sen2 = AdcbResultRegs.ADCRESULT0;     // Sensor2  (J17-3)      (HSEC-18)
         sen3 = AdccResultRegs.ADCRESULT0;     // Sensor3  (J17-5)      (HSEC-31)
         isoamp = AdcdResultRegs.ADCRESULT2;   // Sensor4  (HSEC-34)
         sen9 = AdcbResultRegs.ADCRESULT2;             // Voff  1.5V offset
         sen10 = AdccResultRegs.ADCRESULT1;            // Vmg Output of MGLPF
         sen11 = AdcdResultRegs.ADCRESULT1;            // VPCC (upper ISO-AMP)
         sen12 = AdcdResultRegs.ADCRESULT3;            // Inverter Output Voltage
#endif

#if 1
// Scale sensor inputs, Current are displayed in mA
    ilink = 1000*ADC_SCALE*CURRENT_SENSOR_SCALE1*DIVIDER_SCALE*(sen1 - CS_OFFSET1);
// DC Link Current Compensator
         //if(ilink<0)
         //  ilink = ilink*(-1);
         //ilink_f = ilink_f + gamma*(ilink-ilink_f);
// Grid Current Restore
     ig  = 1000*ADC_SCALE*CURRENT_SENSOR_SCALE2*DIVIDER_SCALE*(sen2 - CS_OFFSET2);
// Grid voltage restored from sen11 or sen12
     vg = V_ADC_SCALE*VOLTAGE_DIVIDER_SCALE*VGCB_DIVIDER_GAIN*(sen11 - VS_OFFSET1);
// Calculate the VPCC Voltage corresponding to the sen11
         vmg   = ADC_SCALE*(sen10  - sen9);
#endif

#if 0
// 50Hz Sinewave islanding test
       theta_1 += omega;
           if(theta_1>=360)
             theta_1 -= 360;
       //theta_3 = (int)theta_1;
       theta_2 = (int)theta_1;
       sinwt   = 2000*sin_t[theta_2];
#endif
```

```
#if 1
//*****************Phase Lock Loop (PLL)*********************//
// Calculate the Load p.u Voltage, Vpcc voltage is measured on transformer secondary
side
        vgpu = vg/313;
        //vgpu = 1*sin_t[theta_3];                          // Grid voltage per unit
//******* Conventional Power PLL PLL****************//
       //ppll = vgpu*cos_t[theta_g2];                    // Power Pll
       //ppll2 = ppll2 + beta*(ppll-ppll2);              // Low Pass Filter
        //p_demand = 0;                                  // Power demand set to zero
        //p_error = p_demand - ppll2;                    // Conventional Power pll

// Thacker Power PLL (Same as MMPD)
        ppll = vgpu*cos_t[theta_g1];
        ppll2 = sin_t[theta_g1]*cos_t[theta_g1];
        p_error = ppll - ppll2;

// Kp and Ki in Loop Filter
             kpp = 3000;                 // KP and Ki for power PLL
             kip = 2000;

#if 0
//***************SRF-PLL Synchronous Reference Frame- PLL******************//
// Quadrature Signal Generator (QSG)
         k_pll   = 0.2;       // Static Gain to settle the sine and cosine to AMP 1
         e_pll1  = vgpu - valpha;                                  // Error 1
         e_pll2  = k_pll*e_pll1 - vbeta;                           // Error 2
         valpha1 = kts*wg*e_pll2;               // Valpha before the integrator
         if(release)
         valpha  = valpha + valpha1;            // Valpha
         vbeta1  = kts*wg*valpha;
         vbeta   = vbeta + vbeta1;

// Reference frame Park Transformation
         vd =  valpha*cos_t[theta_g3] + vbeta*sin_t[theta_g3];
       vq = -valpha*sin_t[theta_g3] + vbeta*cos_t[theta_g3];
         p_demand = 0;
         p_error  = p_demand - vq;

         kpp = 5;
         kip = 0.15;
#endif

       w_demand = kpp*p_error + pd;                  // Output of Loop Filter
       if(release)
         pd = pd + kip*p_error;

// Loop Filter Clamp
       if(pd>= 50)
       pd = 50;
       if (pd<=-50)
       pd = -50;
// Voltage Controlled Oscillator (VCO)//
       wg = w_demand + 2*PI*50;                    // Central frequency 2*PI*50
// Integration, frequency to degree (rad/s to rad), wgd global survive between ISR
      wgd = wgd + kts*wg;
       if (wgd > 2*PI)
```

```
            wgd = 2*PI;
      if(wgd>=2*PI)                          // limit the wgd from 0 to 2PI
            wgd -= 2*PI;
// Converting the angle from radian to degree (wgd*10 to reserve the fraction part)
      theta_g = R2D*wgd;
      theta_g1 = (int)(theta_g);          // restore the theta_g back to 0 to 360
//*****Angle Compensator for SRF-PLL Synchronous Reference Frame- PLL *****//
      //theta_g3 = theta_g1 + 90;         // theta_g3 need to compensate with 180

// Make sure theta_g3 is maximum 360+90, theta_g2 won't go above 450 when control
      //if(theta_g3 >= 450)
      //      theta_g3 = 450;
      // if(theta_g3 >= 360)               // Ensure theta_g2 is from 0 to 360
      //     theta_g3 -= 360;

// Unity Power Factor Compensator//
      if(controller_switch==1)                 // Enable PR Controller
      {
            {
               theta_g4 = theta_g1 + 8 ;   // pll compensator for PR Controller
            }
      }
      else
      {
// Enable the ac current control by slider1 and then disable the compensator
         if(ac_control_en==1)
          {
// PLL Compensator for Output Current PI Controller
             theta_g4 = theta_g1 + 10 ;
          }
// The default control method is dc link current control
        else
            {
                theta_g4 = theta_g1 + 10 ;
            }
      }
// Ensure that the output phase theta_g4 is from 0 to 360
          if(theta_g4 >= 360)
                theta_g4 -= 360;
// Generate a idemand current based on PLL, used for testing the PLL function only
           vpl = 313*sin_t[theta_g4];
           theta_3 = (int)(theta_g4);
#endif

#if 0
// Digital Averaging Process for 20KHz  Moving Average for dc link sensing technique
     if(x<400)
     {
           //*rear=(int)sen9-(int)sen10;       // For MGLPF
           //*rear=iex_2;                       // For dc link sensing
          *rear=ilink;                    // For DC link Current Sensor Calibration
           sum+=*rear;

// display average as DC value, if average is integral, then average=(int)sum/400;
          if(rear==v+399)
            {
                average=(int)sum/400;
```

```
            }
          else
            {
                rear++;
            }
     }
     else if(x>=400)
     {
          sum-=*front;                        // Subtract the oldest sample
// Connect the array with pointer front and rear,  the front pointer always leads to
the oldest sample and the rear always leads to the newest sample.
          if(front==v+399)
//if *front is the last data in array(v[399]), then it shifts to the first data for
next data.
                front-=399;
          else
                front++;
          if(rear==v+399)
                rear-=399;
          else
                rear++;
          //*rear=(int)sen9 -(int)sen10;       // display average as DC voltage value
          //*rear=iex_2;                       // For DC link sensing
          *rear=ilink;                         // DC Link Current Calibration
          sum+=*rear;
//DCA algorithm deal with the new sample, involving the Latest sample in the average.
          average=(int)sum/400;
     }
     x++;
#endif

#if 1
// Low pass filter - DC Extraction for DC Link Sensing Technique
// Extraction current input into the low pass filter, Not Necessary to put ilink_f
cause there will be a low LPF below
       iex_1 = ilink*sin_t[theta_3];
       iex_2 = iex_2 + alpha*(iex_1-iex_2);       // Low Pass Filter
     //iex_3 = iex_2;
// Averaging Algorithm for DC Current Extraction
     if(x<400)
// Averaging every 2ms   (sample frequency 20kHz, 400 Samples in 2ms)
     {
        sum_1 += iex_2;                           //Average for DC Link Sensing
        sum_2 += vmg;                             //Average for MGLPF
          x++;
     }
     if(x==400)
     {
        iaverage_c = (int)sum_1/400;
        vaverage_c = (int)sum_2/400;
          x-=400;
          sum_1 = 0;
          sum_2 = 0;
#endif
```

```
#if 1
// DC Extraction Calibration
     iaverage = iaverage_c - 17 ;       // 10mA offset is measured from multi-meter
     vaverage = vaverage_c - 8;         // calibration based on multi-meter
#endif


#if 1
// DC Current Suppression Loop
     if(dcloop_en==1)
     {
     kpd = 0.01;
     kid = 0.003;
     dc_demand = 0;
// DC Suppression based on current extraction from DC Link Sensing
     //dc_error = dc_demand - iaverage;
// DC Suppression based on voltage extraction from MGLPF(Voltage Mitigation)
     dc_error = dc_demand - vaverage;
         if(!release)
             {
                   dcd = 0;
             }
     icom = kpd*dc_error+dcd;            // Compensation current to reference
        if(release)
        dcd = dcd + kid*dc_error;

//  integrator clamp /The icom will not exceed the 0.2A.
       if(dcd > 200)
             dcd = 200;
       if(dcd < -200)
             dcd = -200;
     }
     else
     {
        icom = 0;
     }
#endif

#if 0 // MAF
// Digital Averaging Process for 20KHz for Mid Ground Low Pass Filter
     if(x<400)
     {
           *rear=(int)sen9-(int)sen10;           // For MGLPF
           sum+=*rear;
         if(rear==v+399)
           {
//display average as DC voltage value, if average is integral, then ave=(int)sum/400;
                vaverage=(int)sum/400;
           }
         else
           {
                rear++;
           }
     }
     else if(x>=400)
     {
         sum-=*front;                        // Subtract the oldest sample
```

```
// Connect the array with pointer front and rear,  the front pointer always leads to
the oldest sample and the rear always leads to the newest sample.
          if(front==v+399)
// if *front is the last data in array(v[399]), then it shifts to the first data for
next data.
                front-=399;
          else
                front++;
          if(rear==v+399)
                rear-=399;
          else
                rear++;
          *rear=(int)sen9 -(int)sen10;   //  display average as DC voltage value
          sum+=*rear;
//DCA Algorithm deal with the new sample, involving the latest sample in the average.
          vaverage=(int)sum/400;
     }
     x++;
#endif

#if 1
// Output current reconstruction
         if(mbb-1250>=0)        //mbb is the modulation index that used for T1/T2
         sign = 1;
         else if(mbb-1250<0)
           sign = -1;
         irb = ilink*sign;
         //irb = ilink_f*sign;
#endif

#if 1
// ********************Current Controller Setup**********************
         if(controller_switch==1)           //Enable PR Controller
         {
// Construct the demand current
                  i_demand = idemand*sin_t[theta_3]+idc_r;
// Enable the ac current control by slide the slider1
                if(ac_control_en==1)
                     {
// Current Control based on Grid Current
                           i_error  = i_demand-ig+icom;
                           kp_r = 0.12;
                           kr_r = 150;
                           wc_r = 10;      // 2*wc in PR controller is 10, wc=5 rad/s.
                     }
// The default control method is dc link current control
                   else
                   {
// Current Control base on Reconstructed Current
                           i_error  = i_demand-irb+icom;
                           kp_r = 0.18;
                           kr_r = 250;
                           wc_r = 10;
                   }
// Output Modulation index ipi equals to proportional gain*current error and resonant
                   ipi = kp_r*i_error + pr_r;
```

```
// when the release is not activated, the current accumulator is set to zero, the
release is activated by enabling the PWM
                if(!release)
                       {
                            pr_r = 0;
                       }
// First feedback error after gain kr_r
                    pr_error1 = kr_r*i_error - pr_r;
                    pr_error2 = pr_error1*wc_r - pr_beta;
// Second feedback error after wc
                    pr_r1 = kts*pr_error2;

                     if(release)              // activate when the release is 1
              pr_r = pr_r + pr_r1;            // First integration on open loop
              pr_beta1 = pr_beta1 + kts*pr_r; //The integration on the feedback loop
              pr_beta = pr_beta1*wg*wg;

// Anti-wind up for pr_r (Resonant Controller)
                    if(pr_r >  1250)
                    pr_r =  1250;
                     if(pr_r < -1250)
                    pr_r = -1250;
          }
//*************PI Current Controller Kp and KI *****************//
         else
          {
// Construct the demand current
             i_demand = idemand*sin_t[theta_3]+idc_r;
// Enable the ac current control by slide the slider1
              if(ac_control_en==1)
                    {
// Current Control based on Grid Current
                          i_error  = i_demand-ig+icom;
// Conventional Current Controller Gain Kp and Ki
                          kpc = 0.1;
                          kic = 0.04;
                    }
                else      // The default control method is dc link current control
                {

// Current Control base on Reconstructed Current
                          i_error  = i_demand-irb+icom;
// DC Link Sensing Controller Gain Kp and Ki
                          kpc = 0.18;
                          kic = 0.09;
                }
                   //i_error  = i_demand-ig+icom;
                   //i_error  = i_demand-irb+icom;

                 if(!release)
// when the release is not activated, the current accumulator is set to zero
                    {
                          id = 0;
                    }
// Current PI controller
                  ipi = kpc*i_error+id;
              if(release)
```

```
                id = id + kic*i_error;
// current integrator clamp
                    if(id >  1250)
                    id =  1250;
                    if(id < -1250)
                    id = -1250;
        }
#endif
#if 0
// Non-Unity Power Factor Compensator enable, BB Control.
//if(ac_control_en==0)
// Modulation Compensator for Dead-time Effect on Non-Unity Power Factor for DC Link
Current Control
                     if(ipi <  60 && ipi >0)
                           ipi =  60;
                     if(ipi > -60 && ipi <0)
                           ipi = -60;
#endif

#if 1
// Normalization of the Current PI Controller
     ipi_m = (int)ipi;

// Dead-time Compensation
     ipi_md = ipi_m + sign*0.04*1250;

    if(ipi_md >  1250)
      ipi_md =  1250;
      if(ipi_md <= -1250)
            ipi_md = 1250;

// Modulation index in 20KHz
      if(ac_control_en==1)
      {
            maa = 2500;
      }
      else
      {
          maa = 1050;                          // Set up the sampling point
      }
      mbb = 1250 + ipi_md;
 // Gate Drive 3, 4 control the Leg A, the mid-point of which is connected to Lin and
Lg and Current Sensor, Live.
      mcc = 1250 - ipi_md;
// Gate Drive 5, 6 control the Leg B, the mid-point of Which is connected to C and
Natural
#endif

#if 0
// PWM Generator Testing Open Loop
        maa = 1250;
        mbb = 1250 - 500*sin_t[theta_2];
        mcc = 1250 + 500*sin_t[theta_2];
#endif

#if 1
// PWM Used for generating SOC and Interrupts
```

```
        EPwm1Regs.CMPA.bit.CMPA = (uint16_t)(maa);
// Modulate leg T3/T4 (output bridge)
        EPwm2Regs.CMPA.bit.CMPA = (uint16_t)(mbb);
// Modulate leg T1/T2 (output bridge)
        EPwm3Regs.CMPA.bit.CMPA = (uint16_t)(mcc);
#endif


// Set test point low (HSEC-100) for execution time measurements
        GpioDataRegs.GPBCLEAR.bit.GPIO54 = 1;
        __mnop;
        __mnop;
        __mnop;
}
//--------------------------------------------------------------------------------
// Testing only
interrupt void Cla1Task2 (void)
{
        float xn = 55, yn = 0;
        __mdebugstop();
        //GpioDataRegs.GPBSET.bit.GPIO55 = 1;
// Set test point high (HSEC-100) for execution time measurements
        yn = __sqrt(xn);
        yn = __meinvf32(xn);
        //GpioDataRegs.GPBCLEAR.bit.GPIO55 = 1;
// Set test point low (HSEC-100) for execution time measurements
}
//--------------------------------------------------------------------------------
// Testing only
interrupt void Cla1Task3 (void)
{
        float xn = 55, yn = 0;
        __mdebugstop();
//      GpioDataRegs.GPBSET.bit.GPIO56 = 1;
// Set test point high (HSEC-100) for execution time measurements
        yn = __sqrt(xn);
        yn = __meinvf32(xn);
        yn = __sqrt(xn);
        yn = __meinvf32(xn);
//      GpioDataRegs.GPBCLEAR.bit.GPIO56 = 1;
// Set test point low (HSEC-100) for execution time measurements
}
//--------------------------------------------------------------------------------
// Testing only
interrupt void Cla1Task4 (void)
{
        float xn = 55, yn = 0;
        __mdebugstop();
        //GpioDataRegs.GPBSET.bit.GPIO57 = 1;
// Set test point high (HSEC-106) for execution time measurements
        yn = __sqrt(xn);
        yn = __meinvf32(xn);
        yn = __sqrt(xn);
        yn = __meinvf32(xn);
        yn = __sqrt(xn);
        yn = __meinvf32(xn);
        //GpioDataRegs.GPBCLEAR.bit.GPIO57 = 1;
```

```
// Set test point low (HSEC-106) for execution time measurements
}
//---------------------------------------------------------------------------
interrupt void Cla1Task5 (void)
{

}
//---------------------------------------------------------------------------
interrupt void Cla1Task6 (void)
{

}
//---------------------------------------------------------------------------
interrupt void Cla1Task7 (void)
{

}
//---------------------------------------------------------------------------
// Initialise CLA globals
// CPU1 executes this task with a software trigger to initialise CLA global variables
interrupt void Cla1Task8 (void)
{
       angle_f = 0;
       angle1 = 0;
       zd=0;
       zq=0;
       id=0;
       dc_demand=0;
       dcd=0;
       p_demand=0;
       pd=0;
       release = 0;
       ppll2 = 0;
//     w_demand = 0;
//     wgd = 0;
       sum_1=0;
       sum_2=0;
       theta_g3=0;

// Global Variables for DCAA
#if 1
      front=rear=&v[0];
      x=0;
      x_1=0;
#endif
}
// end of file
```