ADVANCED MODELLING AND DESIGN CONSIDERATIONS FOR INTERCONNECTS IN ULTRA-LOW POWER DIGITAL SYSTEMS

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DECLARATION

I hereby declare that this thesis is my own work and effort and that it has not been submitted anywhere for any award. Where other sources of information have been used, they have been acknowledged.

Newcastle upon Tyne 2021

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CERTIFICATE OF APPROVAL

I confirm that, to the best of my knowledge, this thesis is from the student's own work and effort, and all other sources of information used have been acknowledged. This thesis has been submitted with my approval.

ALEX YAKOVLEV

To my greatest supporters that is my wonderful father who is my role model
To my wonderful mother
To my beloved wife
To my lovely kids Maryam, Abdu Allah and Abdu Alrahman
To my family
— Mohammed

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ABSTRACT

As Very Large Scale Integration (VLSI) is progressing in very Deep submicron (DSM) regime without decreasing chip area, the importance of global interconnects increases but at the cost of performance and power consumption for advanced System-on-Chip (SoC)s. However, the growing complexity of interconnects behaviour presents a challenge for their adequate modelling, whereby conventional circuit theoretic approaches cannot provide sufficient accuracy. During the last decades, fractional differential calculus has been successfully applied to modelling certain classes of dynamical systems while keeping complexity of the models under acceptable bounds. For example, fractional calculus can help capturing inherent physical effects in electrical networks in a compact form, without following conventional assumptions about linearization of non-linear interconnect components.

This thesis tackles the problem of interconnect modelling in its generality to simulate a wide range of interconnection configurations, its capacity to emulate irregular circuit elements and its simplicity in the form of responsible approximation. This includes modelling and analysing interconnections considering their irregular components to add more flexibility and freedom for design. The aim is to achieve the simplest adaptable model with the highest possible accuracy. Thus, the proposed model can be used for fast computer simulation of interconnection behaviour. In addition, this thesis proposes a low power circuit for driving a global interconnect at voltages close to the noise level. As a result, the proposed circuit demonstrates a promising solution to address the energy and performance issues related to scaling effects on interconnects along with soft errors that can be caused by neutron particles.

The major contributions of this thesis are twofold. Firstly, in order to address Ultra-Low Power (ULP) design limitations, a novel driver scheme has been configured. This scheme uses a bootstrap circuitry which boosts the driver's ability to drive a long interconnect with an important feedback feature in it. Hence,

this approach achieves two objectives: improving performance and mitigating power consumption. Those achievements are essential in designing ULP circuits along with occupying a smaller footprint and being immune to noise, observed in this design as well. These have been verified by comparing the proposed design to the previous and traditional circuits using a simulation tool. Additionally, the boosting based approach has been shown beneficial in mitigating the effects of single event upset (SEU)s, which are known to affect DSM circuits working under low voltages.

Secondly, the CMOS circuit driving a distributed RLC load has been brought in its analysis into the fractional order domain. This model will make the on-chip interconnect structure easy to adjust by including the effect of fractional orders on the interconnect timing, which has not been considered before. A second-order model for the transfer functions of the proposed general structure is derived, keeping the complexity associated with second-order models for this class of circuits at a minimum. The approach here attaches an important trait of robustness to the circuit design procedure; namely, by simply adjusting the fractional order we can avoid modifying the circuit components. This can also be used to optimise the estimation of the system's delay for a broad range of frequencies, particularly at the beginning of the design flow, when computational speed is of paramount importance.

PUBLICATIONS

Journal publications:

1. **Mohammed Al-daloo**; Ahmed Soltan; and A. Yakovlev, *Advanced Interconnect Circuit Modelling Design Using Fractional-Order Elements*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019.

2. **Mohammed Al-daloo**; Mohamed A. Abufalgha; A. Yakovlev; and B. Halak, *Bootstrapped driver with the Single Event Upset effect*, IEEE Transactions on Circuits and Systems I, 2020.

Conference publications:

1. **Mohammed Al-daloo**; A. Yakovlev; and B. Halak, *Energy efficient bootstrapped CMOS inverter for ultra-low power applications*, IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 516-519, 2016.

2. **Mohammed Al-daloo**; Ahmed Soltan; and A. Yakovlev, *Overview Study in On-chip Interconnect Modelling approaches and its trend*, In 2018 7th International Conference on Modern Circuits and Systems Technologies (MOCAST), pp. 1-5, IEEE, 2018.

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ACRONYMS

FDTD Finite-Difference Time-Domain

BIBO bounded-input bounded-output

IGFET Insulated-gate field effect transistor

KVL Kirchhoff's voltage law

KCL Kirchhoff's current law

SiO_2 Silicon dioxide

Si Silicon

MoC Method of Characteristic

LTI linear time-invariant

TEM Transverse electromagnetic

TL Transmission Line

TLM Transmission line modelling

IoT Internet of Things

IoE Internet of Everything

NoC Networks-on-Chip

IC integrated circuit

CMOS complementary metal-oxide-semiconductor

MOSFET metal-oxide-semiconductor field-effect transistor

MOS metal-oxide-semiconductor

NMOS N-type metal-oxide-semiconductor

PMOS P-type metal-oxide-semiconductor

SEU single event upset

LET Linear Energy Transfer

SET Single Event Transient

DSM Deep submicron

NoC network-on-chip

R_q sheet resistance

SoC System-on-Chip

PV Parameter Vector

ULP Ultra-Low Power

VLSI Very Large Scale Integration

Part I

Thesis Chapters

1

INTRODUCTION

The motivation for the work, a summary of the technical contributions made by the author, and the structure outline of the thesis are stated in this chapter.

1.1 MOTIVATION

Generations of constant improvements in complementary metal-oxide-semiconductor (CMOS) technologies design and fabrication have been catalysed by the demand for lower cost, higher density and more energy-efficient integrated circuit (IC). Such technology trend has led to a relentless shrinking of electronic systems, which has approached the realm of a very deep submicron scale. On the other hand, the reduction in the cost per transistor keeps following an exponential trend, which somehow depends on Moore's law, and will continue despite the end of this law [10]. At the same time, the projection of energy consumption promises a reduction by two orders of magnitude according to the Koomey's and Gene's laws [117]. Thus, based on those trends, it will be increasingly possible to see systems that are small, very inexpensive and extremely low power and pervasive in space.

The demand and supply effect of those technological applications and trends is coming together and creating a novel paradigm, under the so-called Internet of Things (IoT). This new paradigm is swiftly gaining ground owing to the promises of creating huge value and delivering unprecedented benefits to society [17]. The concept of IoT firstly appeared in a presentation in 1999 in the context of a large-scale network of a variety of things or objects such as mobile phones, sensors, tags and actuators [14]. In the general term, the IoT locates at the intersection of the pervasive networking (the Internet), cloud and its significant data, the unprecedented form of mostly real-time aggregated data from the physical world and many other infrastructures. This is occurring through the introduction of ubiquitous, distributed sensors and nodes of an extremely miniaturized integrated system with

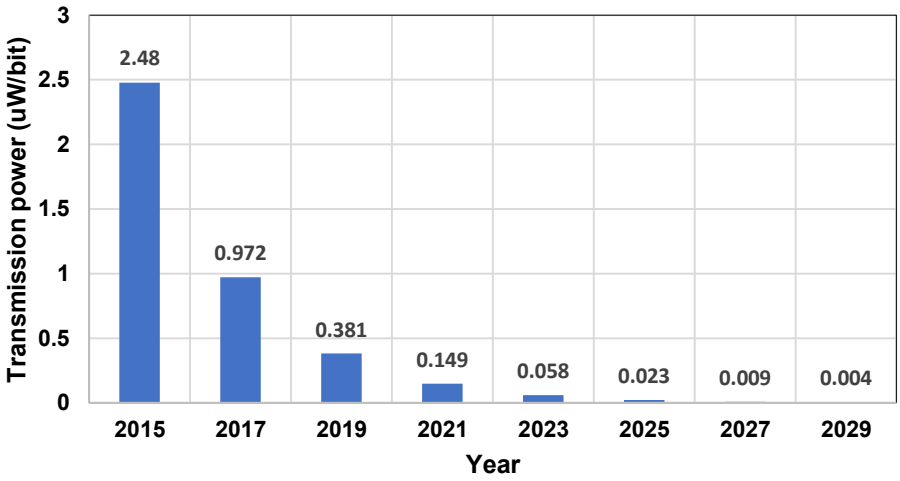


Figure 1.1: Trend of limitations for power consumption based on IoT data in [99].

a very long lifetime and low power consumption [66, 9]. Based on this general term, IoT has already become a reality due to the number of computing devices connected to a global network which surpassed the worldwide population [66].

Regardless of the wide claims regarding IoT in the community of chip design, it is still in their technological infancy and there are many challenges that should be addressed. For instance, the challenges of energy efficiency to maintain power source, cost and reliability, among others need to be tackled [10]. Specifically, in terms of low power requirements for emerging IoT applications, the overriding concern is power where such applications mostly require to consume a certain amount of power [99], as predicted in Figure 1.1. Hence, it is important to work in the direction of locating new solutions which are expected to run at very low voltages [103].

Deep submicron (DSM) technology has created considerable possibilities for digital system design, but has also added a new type of design problems. In the 22nm technology node and beyond, the circuit performance has become more sensitive to the parasitics of interconnect and, thus, more sensitive to interconnect variability [28]. Accordingly, the precision of interconnects fabrication processes has great importance as a direct consequence of the reduction in devices feature size [152]. Additionally, as the feature size and power supply reduce, the sensitivity of the integrated circuits to process variability and single event upset (SEU) has increased. These issues should be considered

in driver circuits design as it noticeably affects the testability, reliability and yield [5].

1.1.1 *Interconnect power consumption*

Given the increasing use of portable devices which depend on batteries as a power source, saving energy has become one of most important criterion in Very Large Scale Integration (VLSI) design. The recent emerging improvements in semiconductor technology accompanied by a reduction in size and cost of fabrication, have urged such a trend of energy-constrained and IoT-oriented applications [183, 10]. This is to meet the requirements of energy-efficient architectures associated with the delivery of fast-growing IoT services.
The fact of the huge dimensions of interconnects compared to those of transistors, which is caused by aggressive technology scaling, leads the load capacitance to be dominated from the power consumption point of view [184, 55]. Hence, the interconnects appear to represent a puzzle in terms of achieving a high-performing digital system with good power efficiency, where its driver accounts for a large percentage (approximately 50%) of the whole system's power dissipation [183]. However, to be exact, it ought to be known which parts of the system are involved when referring to energy and power. Benini et al. [24] defined it as "the minimum power dissipation per bus transition for only their low power encoder and decoder". This would be correct in ideal cases, but actually some messages are dropped because of noise, and in this case retransmission or redundant bits are needed. Meanwhile, the term "energy per transmitted word" is used by Worm et al. [204], that is to include the energy of successful transmission and retransmission processes together. At the circuit level, power consumption P practically takes place when the capacitance of the interconnection is pulled up to supply voltage V_{DD} and then pulled down to the ground, wherein $P \propto fV_{DD}^2$ [150] and f is the frequency of this event. Thus, the energy dissipation depends on basic system features as shown [212]:

$$E = \alpha_a C_{eff} V_{DD}^2 \tag{1.1}$$

where E is the energy consumption of a wire, α_a is an activity factor and C_{eff} is the effective wire capacitance. Overall, it is clear that equation 1.1 and power expression identify the system components that are involved in power dissipation and guide researchers in designing approaches to mitigate the power dissipated in logic circuits. The issues of wires have been exacerbated with technology scaling due to the increase in the parasitic capacitance of interconnects which results from decreased space between wires and the wire to ground. Moreover, increases in clock speed and energy densities and reduced supply voltage make the system more vulnerable to noise [49]. Also, with the advantages of the semiconductor technology scaling, the microelectronic circuit's susceptibility to radiation-induced soft errors has raised. Consequently, the reliability issue of these circuits becomes another concern to IC's designers [162].

In order to overcome such challenges, many techniques have been proposed; for instance, reducing the swing voltage or the activity over links using coding, implementing circuits with scaled supply voltage, or a bootstrap technique [55].

1.1.2 *On-chip interconnect model*

Circuits for advanced applications should be premeditated effectively with a high awareness of the interconnect circuits as a crucial part of the chip structure. Estimating the influence of the interconnect on the circuit performance is necessary for the circuit and interconnect joint optimisation. This is because the IC is fundamentally a combination of semiconductor devices and interconnections.

In recent years, most research has not only been interested in transistors and ways to employ them optimally but also in interconnection between devices, which received a comparable interest [29, 55]. Interconnections are simply wires, made of poly-silicon or metal, which link an enormous number of components to transfer data and signals inside a chip, with lengths reaching more than 10 mm in some large chips [56]. In general, the interconnect model can be represented as a set of values of inductance, capacitance and resistance within high frequency nano-scale systems [96]. This is because the simplest form of interconnect is a strip of metal in parallel with a ground plane,

and therefore just a capacitor could be a representative of the wire [183].

At the present time, SPICE like [136] simulators represent the gold standard for the IC designers to simulate the circuit performance. These simulators can accept nearly any circuit, regardless of whether it is linear or nonlinear, and define the voltage waveform on all nodes. However, the process of simulating complete systems using such simulators is very costy. In addition, it is effective to hundreds of nodes [130, 202].
Hence, economical alternatives are used for these simulators. Among these alternatives; Relaxation and iteration simulation methods, solving Maxwell's Equations for interconnections, delay models based on RC tree and transmission line model analysis [197]. These delay models are primarily based on either numerical or analytical techniques. Accurate interconnect models, such as RLC transmission lines and efficient solutions to analyse on-chip interconnects are required in IC design process [197, 163].

With the continuous decrease of on-chip clock periods, the timing characteristics of on-chip signals need to be precisely controlled and determined. Accordingly, accurate interconnect model is important to the process of IC design. However, the attainment of an accurate model for the on-chip line requires a realistic consideration of its parameters. Achieving this is difficult due to the variance of the parameters. For instance, the distributed RLC model is a good approximation to a transmission line model, but it is accurate only up to a certain frequency [159], depending on the number of sections per wavelength.
Currently, designs at a very high-frequency region with considerably improved cut-off frequency near 300GHz at recent technology nodes have become possible due to the advance scaling of CMOS technology [179]. Therefore, frequency dependent components, in particular inductive and capacitive elements, are crucial especially when there is a very high operating frequency [95]. Hence, this draws the attention to the effects that have been discarded in the early assumptions to model interconnections. Thus, this effect should be considered during modelling this important component of IC circuits.

Fractional order calculus has the ability to represent systems with complex nonlinear phenomena high-order dynamics using fewer parameters [149, 80]. This is because its arbitrary order

of the derivatives provides an additional degree of freedom to fit a specific behaviour [75, 80]. Based on that, fractional elements modelling can be used effectively for a non-uniform transmission line with a distributed parameter system. Thus, adding such parameters, i.e. that relate to the fractional-orders elements, would extend the interconnect model representation and have a higher degree of control on its characteristics.

1.2 THESIS SCOPE AND CONTRIBUTIONS

This thesis opens a new research direction in the development of on-chip interconnections modelling. The scope of this thesis is to study interconnect design techniques that are suitable for DSM System-on-Chip (SoC) in the IoT realm. This includes a study to seek to extend existing classical interconnects models in the context of generalising architectures, i.e., that use fractional calculus. Though present fractional approaches have discussed the transmission lines, they have not covered the interconnection structure. The objective, here, is to add more flexibility and freedom for design to achieve the simplest adaptable model with acceptable accuracy. As a result, the suggested model can be applied for computer simulation of interconnection management. Additionally, to address Ultra-Low Power (ULP) design limitations, the thesis proposes a low power driving circuit design by running the global interconnect under the transistor voltage threshold and resolves their circuit level challenges. Accordingly, the proposed implementation achieves reduction in energy consumption compared with conventional designs with enhancing performance and improving tolerance to soft errors. Specifically, errors are caused by the radiation impact, for instance the strikes of neutron and alpha-particle.

The major contributions of this thesis can be summarized as follows:

- Several techniques related to the interconnect structure analysis and modelling are outlined in this work. The models are categorized into two main classes; the integer order models and the fractional order models. All major modelling issues and challenges are discussed for different approaches, where a comparison is made for a number of them. From that perspective, this research proposes a

fractional on-chip interconnect modelling approach that has the ability to supersede models using the classic approaches in the DSM regime. Additionally, this research can be the basis for any research intending to take advantages of using these methods and to address their challenges.

- With regard to tackling ULP design challenges, a new design of an interconnect driver has been developed and analysed. This design uses a bootstrap circuitry which boosts the low input voltage of the driving circuit, while this boosted circuit itself feeds the voltage pumping components simultaneously. Hence, this approach has achieved a number of goals; improving performance, decreasing the power consumption, reducing the size and being immune to noise. For ULP circuits design, these improvements are essential and they have been validated by comparing the proposed design with previous and traditional circuits using Cadence simulation tool. On the other hand, the results revealed that the developed design mitigates the effects of single event upsets such as those caused by neutron particle strikes.

- We proposed a new general formula for RLC interconnect circuit model in CMOS technology using fractional-order elements approach. The study is based on approximating an infinite transfer function of the CMOS circuit with a non-integer distributed RLC load to a finite number of poles. It shows better accuracy compared to the results of integral order modelling as demonstrated by performing simulations.
  As such, delay calculations employing our analytical model are within 0.4ps absolute error of COMSOL-computed delay across a range of interconnect lengths. Furthermore, although the model has only been designed based on RLC segments, the effect of conductivity G has been implicitly taken into account due to utilising fractional order element in the shunt admittance.
  A number of analyses were carried out at different levels of the design to evaluate its effectiveness. First, we demonstrated the significant effects of generalising parameters gained by modelling the fractional order impedance and propagation constant of the transmission line for a range

of frequencies. The most important effects are increased flexibility and freedom to design the system. Second, using Matlab we assessed the potential of the proposed approximated model besides the exact one, which shows similarity in the fundamental features of the system such as stability and resonance. Third, the proposed approach showed that with a very small tuning for the generalising parameters we can achieve improvement in the model accuracy. We believe that the proposed approach can be used with already existing simulation tools with a minimal loss in time.

1.3 THESIS ORGANIZATION AND KEY FINDINGS

This thesis is organized into five chapters, as shown in Figure (1.2).

Chapter 1 "Introduction": introduces the motivations, objectives, contributions and structure of this thesis.

Chapter 2 "Background and Literature Review": provides background information and presents a brief literature review on topics relevant to this thesis. Discussing the limitation of on-chip interconnect circuits is introduced. Also, a coherent overview of recently reported works regarding the essential on-chip modelling approaches is stated which can be used for any research intending to take advantages of using these emerging methods and to address their challenges. Furthermore, a device-level comparison of different types of these techniques is provided.

Chapter 3 "Fractional Modelling For Interconnect System": presents a new introduction for interconnect delay time in the fractional order domain as well as a general expression for RLC interconnect network model in CMOS technology based on a second order approximate transfer function.

Chapter 4 "Ultra-Low Power Driver Scheme Incorporating a Bootstrap Configuration": proposes low power driver based on a bootstrap technique that has been implemented to produce circuit design where simulation results of this circuit are compared with conventional one from point of view energy and power consumption.

Chapter 5 "Conclusions and Future Work" outlines the conclusions of the study and explore the implications of the presented work and draw the horizon for prospective future research.

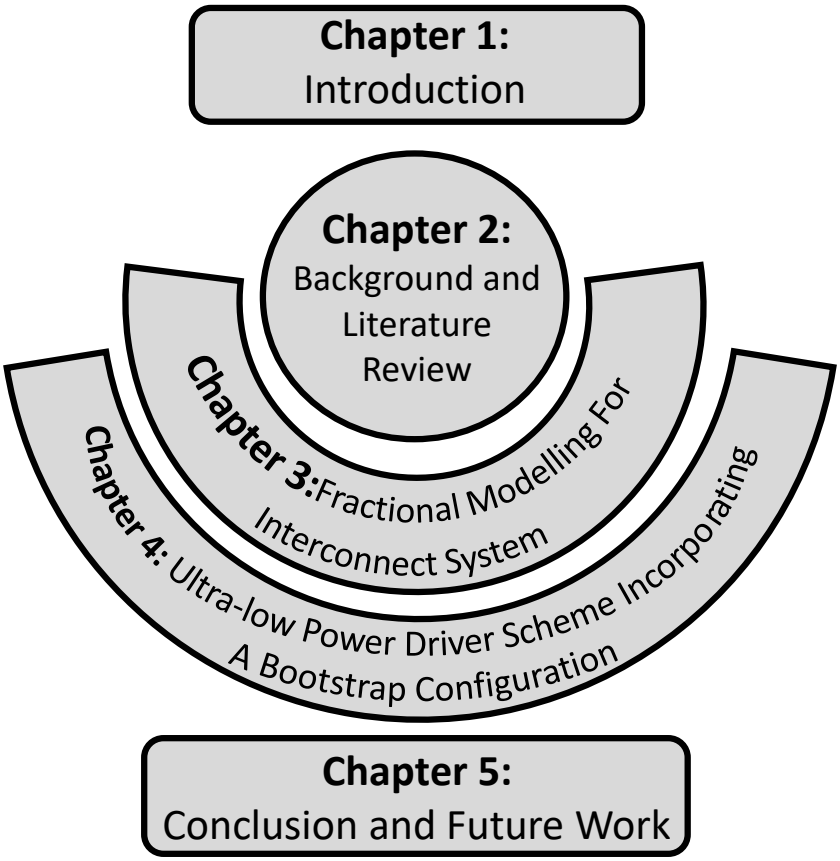


Figure 1.2: Thesis organization.

2

BACKGROUND AND LITERATURE REVIEW

The information in this chapter is intended to present the reader with the basic concepts behind interconnect circuitry to understand the motivation and the choices made in the context of this work.

2.1 INTRODUCTION

Internet of Things (IoT) as a multidisciplinary paradigm, where almost every object around us will be connected and networked through miniature computing systems, has evolved to Internet of Everything (IoE) which is shaping the society and creating multiple industries [99, 178]. This calls for unusual breakthroughs in a number of disciplines of the entire stack such as designing, modelling and other disciplines [28].
The industry of semiconductors will continue to be a key enabler of this paradigm mainly through miniature computing systems and sensors [99]. Many devices, including embedded devices, in the realm of IoT generally need an energy-efficient hardware due to the limitation of the energy budget. Hence, ultra-low-power System-on-Chip (SoC) is widely used to enable portable devices powered by batteries [178].

The modern digital system comprises sets of chips on boards, sets of circuit boards placed in framework and frameworks housed in a rack. At every single level of the structure, signals are transmitted and received on different types of interconnections. However, this communication is mostly implemented by traditional global interconnects through multiplexers and buffers for high-speed, which have a high-power consumption. Given low-power consumption is a major requirement, scaling down the supply voltage to the voltage of the transistor threshold serves reducing energy [154]. Yet, doing so causes significant interconnect delay because of the exponentially decreased current of drivers in sub-threshold [55]. On the other hand, upsizing the drivers does not assist much because the delay depends on the

transistor size linearly, but exponentially on the supply voltage in the sub-threshold [55, 154].

A good device model is essential in the analysis and design of interconnect circuits in deep submicron complementary metal-oxide-semiconductor (CMOS). Interconnect is a term used for the wiring utilised to connect the active components within the integrated circuit (IC). Its purpose is to convey clock and other signals and deliver power/ground to the circuit/system functions on a CMOS chip [61, 21]. According to the signal frequency and wires length, it is determined whether or not the wires should be treated as a transmission line [61].
The ideal wire refers to the interconnect that is treated as a lossless equipotential circuit, which is a reasonable assumption. The actual wire, however, representing a load to the signal driver needs time for the signal to deliver information and it drains power. The non-ideality, as an inherent property, of the wire introduces parasitics which depend on the wire's dimensions. Also, depending on the fall (rise) times of the signals with which they are gated along the wire properties, the electrical circuit model of the interconnect differs [116]. This will be discussed in Section 2.2.2 after underlining the basic concepts behind the analytical model. This chapter, also, introduces basics and fundamental concepts related to interconnect circuits. Section 2.6 reviews the the three main techniques of on-chip interconnect modelling; Section 2.7.1 implements a case study, in a comparison of selected cases, then a section for studying the impact of inserting fractional elements has been presented, after that, a section for introducing the modelling of the interconnect, while the final section is the conclusion.

2.2 BASICS OF ON-CHIP INTERCONNECTIVITY CIRCUIT

2.2.1 *Analytic Modelling*

Wires of on-chip interconnect structure are considered to be composed of four main parasitic components; resistance (R), capacitance (C), inductance (L) and conductance (G). These parts are used to model the wiring which is extremely useful in timing investigation, particularly in assessing the interconnect delay. The discussion, in this section, follows the description in [144].

RESISTANCE: a conductor with rectangular cross-sectional, as shown in Figure 2.1, is a reasonably good approximation for an on-chip wire whose length is X. The resistance R of such a simple strip of material is obtained by [20]

$$R = \frac{\rho}{tw} X \tag{2.1}$$

where t and w are the thickness and the width of the interconnect, respectively, and ρ is the resistivity of the material. Since the thickness t is often one for each technology, it is usual to incorporate the resistivity and the thickness into a single constant named the sheet resistance (R_q) of the material, given as.

$$R_q = \frac{\rho}{t} \tag{2.2}$$

Then the resistance is given by

$$R = \frac{R_q}{w} \tag{2.3}$$

The sheet resistance (R_q) provides the resistance of a square cross-section of a specific material for a constant height. Several materials such as silver, aluminium and copper are used as conductors. Although silver has the lowest conductivity, its high cost implies that it is implemented only for special applications. On the other hand, the most regularly used is aluminium, which is economically the best, and copper which is more expensive but has better conductivity [20].
However, for higher complexity structures including combinations of round and square cross-sections, curves and corners, the resistance is assessed by using tools known as field solvers. Such tools are used to accurately extract parasitics by solving Maxwell's equations in 2 and 3 dimensions [63].

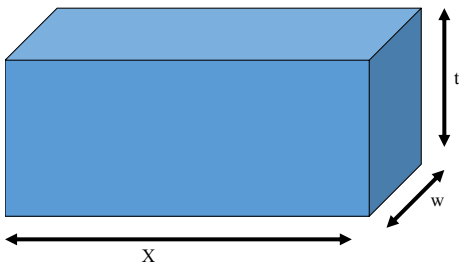


Figure 2.1: Cross sectional dimensions of a conductor.

Also, it is important to be aware that it is common to treat the resistor ideally but this is not always the case. In high frequencies, the current density with depth into the conductor is not uniform but drops away exponentially because of the skin effect phenomenon [61]. A cut-off frequency of this phenomenon can be determined, and an empirical approximation for it is given as [46]

$$f_c = \frac{\rho}{\pi\mu\delta_c^2} \tag{2.4}$$

where μ refers to the permeability, and δ_c to the skin depth. Less than this frequency, the current is supposed to be spread consistently across the whole cross-sectional area of the conductor leading to a frequency-independent resistance given in (2.3), whereas above the cut-off frequency the resistance increases with the square of the frequency.

CAPACITANCE: the capacitance is the ability of the metal conductor to store an energy in electric field form between its surface and another surface. The value of this capacitance is given by

$$C = \frac{Q}{V} = \frac{\iint_s \varepsilon \vec{E} d\vec{S}}{\int_c \vec{E} d\vec{l}} \tag{2.5}$$

where the Q is the charge stored by the conductor, E the electric field and S is a closed surface. In an interconnection architecture, this appears between a metal part under interest and its surrounding such as the ground and power planes, other wires and substrates. Assuming the E field is entirely contained within the two surfaces, the capacitance of the microstrip line structure given in Figure 2.2 can be calculated as follows

$$C = \frac{w\varepsilon}{h} X \tag{2.6}$$

The equation (2.6) underestimates the parasitic capacitance of a wire if applied to the excessive aspect ratio (h/w) wires in DSM technologies. Also, it does not reflect how strong the function is between the parasitic capacitance and the geometry. Therefore, tools known as 3-D field solvers are required to take into account the fringe components of the E field to the capacitance and to obtain an accurate value [63]. However, over the years, empirical formulas have been developed with fair accuracy, and are very

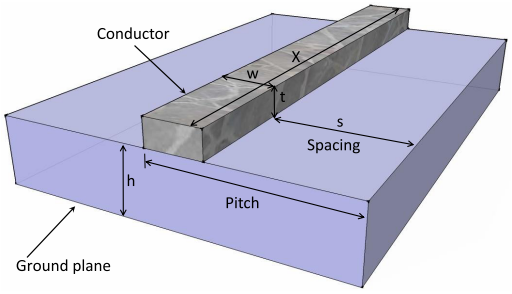


Figure 2.2: Structure of a conductor.

important in understanding the consequence at system level [203]. For instance, an evaluation for the capacitance between the wire and ground plane C_g based on curve fitting approach is given in [175] as

$$C_g = \varepsilon[1.15(\frac{w}{h}) + 2.4(\frac{t}{h})^{0.222}] \tag{2.7}$$

This value in addition to mutual capacitance C_c is used to determine a total capacitance for a conductor surrounded by two adjacent conductors, as follows

$$C_T = C_g + 2C_c \tag{2.8}$$

The total capacitance obtained by this equation is in good agreement with that predicted by the field solver. But it is still inaccurate as the ratio (h/w) continues to decrease. Also, the individual components are not destined to provide the total decomposition into the ground and coupled components since the presence of the adjacent wires significantly affects the electric field around the middle conductor. Since then, formulas which better partitioned the components into coupling components and ground have been reported in [42, 122, 216]. They are in effect a modification of equations in [175] to render the decomposition more accurate, which can be suitably used for parasitic extraction of Deep submicron (DSM) geometries as reported in [83]. These equations have been reproduced in [83], as follows

$$C_f = \varepsilon[0.075(\frac{w}{h}) + 1.4(\frac{t}{h})^{0.222}] \tag{2.9}$$

$$C_f' = C_f[1 + (\frac{h}{s})^{\varpi}] \tag{2.10}$$

$$C_g = C + C_f' + C_f \tag{2.11}$$

where C_f and C_f' refer to the fringing components with and without a surrounded conductor, respectively and ϖ is a curve fitting constant computed from a database of values produced by a field solver. The values of C_f' and C are per unit length. These formulae 2.5, 2.11, 2.9 and 2.10 are deemed to be convincing where their accuracy is reported [144, 83] to be over 85% of the actual value when the following inequalities are satisfied

$$0.3 < \frac{w}{h} < 30 \qquad 0.3 < \frac{t}{h} < 10 \qquad 0.3 < \frac{s}{h} < 10 \tag{2.12}$$

INDUCTANCE: the parasitic inductance is a measure of the distribution of the magnetic field created by the current passing through the conductor. The basic definition of the inductance is

$$L = \frac{\oint B dS}{I} \tag{2.13}$$

where B denotes the magnetic field induced from the current I. This parasitic depends on the global surrounded more than the parasitic capacitance. That is clear in the definition where this equation yields self-inductance if S is induced in the same circuit. Whereas it defines mutual inductance in case of S following another conducting track. The loop created by the signal wire and the return path, which is fundamentally in the power distribution network, can potentially extend to hundreds of micrometers away from the wire under study. Therefore, the extraction of parasitic inductance for a given wire is vastly complicated, as it depends not only on the features of that specific wire, but also probably on the features of thousands of other wires. Thus, it would appear that expensive 3-D numerical methods are required for good accuracy.

To overcome this problem, the concept of partial inductance approach is reported for the first time in [165]. This technique avoids the need to define the return loop by assuming the current

return at infinity. Hence, this causes the inductance to be only dependent on the geometry of the wire. Later, this approach was simplified and a close form solution had derived to the following [155]

$$L_s = \frac{\mu_0}{2\pi}\left[X\ln(\frac{2X}{w+t}) + \frac{X}{2} + 0.2235(w+t)\right] \tag{2.14}$$

$$L_m = \frac{\mu_0}{2\pi}\left[X\ln(\frac{2X}{d}) - 1 + d\right] \tag{2.15}$$

where L_m and L_s are mutual and self inductance, respectively, μ_0 is the permittivity of the dielectric and d is the distance between the centres of the two wires under study. However, the best precise evaluation can be achieved by field solvers such as FASTHENRY [187] and a 3-D inductance extraction tool which are popular and available for free.

2.2.2 *Electrical level modelling*

Equivalent lumped element circuit approximations can be used to illustrate the interconnection properties. Also, it can be assumed that those circuit elements are constant throughout all time and frequency, but such an assumption can not always apply. Figure 2.3a shows a lumped element circuit approximation of an RLGC interconnection. The propagation behaviour of a large number of these two-port circuits, that are chained together, can resemble the behaviour of its equivalent interconnection [130].

Generally, propagation along a general RLGC interconnection is described by partial differential equations [43] as follows

$$\begin{aligned} \frac{\partial v(x,t)}{\partial x} + L\frac{\partial i(x,t)}{\partial t} + Ri(x,t) = 0 \\ \frac{\partial i(x,t)}{\partial x} + C\frac{\partial v(x,t)}{\partial t} + Gi(x,t) = 0 \end{aligned} \tag{2.16}$$

Conventionally, one or more of the terms in these equations (2.16) can be neglected, depending on the signal frequency and on values of interconnection parasitics R, L, G and C. Accordingly, different propagation models result, while the more prevalent models are listed in Figure 2.3.

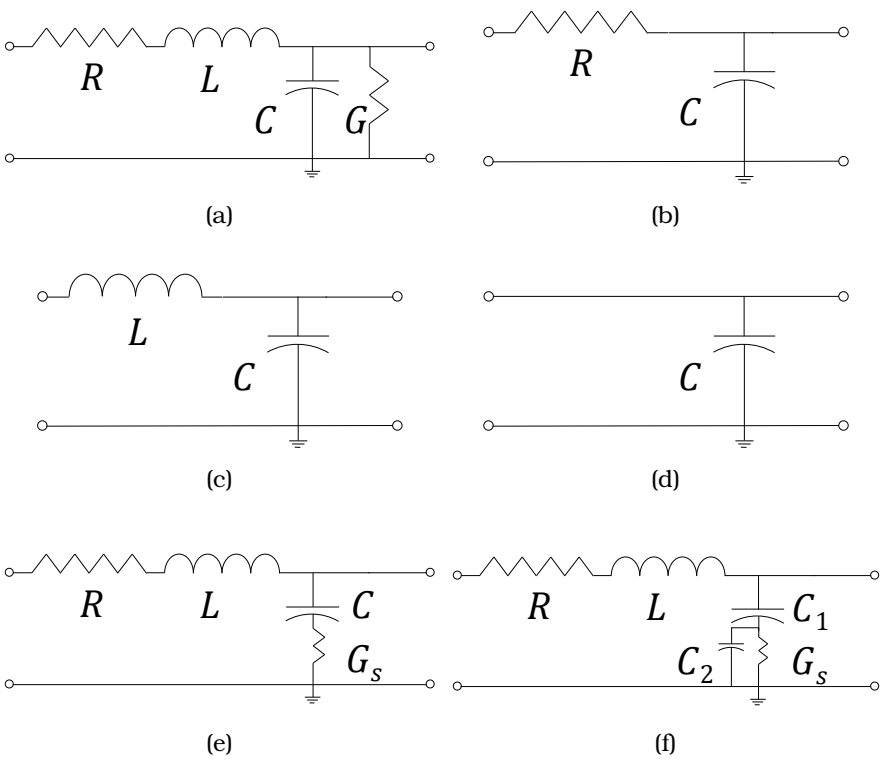


Figure 2.3: Lumped element approximations for propagation classes: (a) RLGC propagation, (b) RC propagation, (c) LC propagation, (d) tracking propagation, (e) and (f) propagation of resistive substrate.

- RC propagation dominates over other propagation models particularly for silicon metal-oxide-semiconductor (MOS) technologies. This class is used in a case of very fine line width, which results in a large R, and closely situated to the ground line, which results in a large C and a small L. With the absence of G and L terms in (2.16), as shown in Figure 2.3b, the diffusion partial differential equation is applied [131].

- Transverse electromagnetic (TEM) propagation or LC propagation class includes the L and C terms, shown in Figure 2.3c, as wL >> R. This type of interconnection is a lossless transmission line. It is preferred over the RC class because of its faster, i.e., wave-like propagation. Therefore, efforts have been made to guarantee this class in Wafer Scale Integration circuitry, typically by elevating the interconnection over the ground plane. This class exists in Gallium-Arsenide technologies. However, decreasing the R term below wL with

typical switching speeds and dimensions of MOS technologies is not easy to achieve [131].

- However, it is satisfactory to consider the interconnection such a single node which propagates signal instantaneously if its time constant is much shorter than the one of the input signal. Figure 2.3d illustrates the class of tracking propagation where a single lumped capacitor is used to model the entire interconnection [167].

- There is a transition region, as one would expect, between the former two propagation classes when the inductive and resistive components have similar magnitudes. This class exhibits wave-like propagation but has considerable resistive component as lossy transmission lines. For instance, [214] investigated the signal propagation on metal strips on top of a highly resistive silicon substrate. Owning to the non-ideal ground plane, the transmission line model more resembles propagation classes in Figure 2.3e and 2.3f. In addition, [87] reported some speed advantages to a lossy substrate. Though, this is resulting in more challenging differential equations.

2.2.3 *Importance of Transmission Line (TL) effect*

In the past, until 1990s, wavelength of digital signals was much more than the electrical lengths of on-chip interconnects. This is due to the on-chip digital performance being under 1GHz and that the run length was relatively short. Therefore, a lumped circuit of RC model was adequate to simulate the interconnect circuit [61]. Nevertheless, recently, this has altered because of significant improvements in the performance of IC, which affects not only digital circuits but also analog circuitry [178]. Mainly, these developments are in two directions; speed and dimension. Regarding the speed, faster circuits have been developed with multiple on-chip clocks global of a few Gigahertz and local of approximately 10GHz [61]. Larger chips of around 2cm have been constructed with fine lithography resulting in longer interconnects owing to cross-sectional measurements of less than a micron [61]. As a consequence for these changes, the RC modelling became applicable in some cases only [18]. In recent years,

there has been a growing number of studies that consider the issue of whether inductance should be included in the interconnect model [21, 96, 98, 196]. Though their investigations were in different ways, the obtained expressions are for the most part equivalent. This discussion reconfirms the conclusions in [144]. From the signal timing point of view, to consider the circuit as the transmission line, it has to satisfy the inequalities,that is

$$\frac{t_r}{2\sqrt{lc}} < X < \frac{2}{r}\sqrt{\frac{l}{c}} \tag{2.17}$$

where t_r is input signal slew rate, l, c, r are per unit length parasitic of the wire with X length. Whereas the wire conductance to ground can be ignored for the most of Very Large Scale Integration (VLSI) circuit applications. Now from the standpoint of the qualitative sense, in the first inequality, the gating signal is quite slow for the combined capacitive and inductive reactance to compete with the resistance. If not, the link has to be sufficiently long for the delay at the speed of light in the medium to be comparable to the rise time. However, on the other side of the inequality, if the link is too long, the loss is quite enough to conceal the inductive effect. If not, and the reactance at the highest frequency of operation (determined by the driver's output rise time) is comparable with the series resistance, the inductance effects cannot be ignored.
The transmission line effect drew the attention of a vast number of researchers and this will be discussed concisely in the next section and more in Section 2.5.

2.2.3.1 *Importance of TL in fractional order domain*

The effect of the transmission line has become more significant, especially in global interconnects, with increasing on-chip signal frequencies. Equations (2.16) describes this effect and were solved for the first time by Heaviside [85]. Fundamentally, this classical model considers that the magnetic effects are represented by the serial inductive elements, and likewise, parallel capacitive elements can be used to model capacitive phenomena. The energy losses during the transmission, which are commonly in the form of current leakage and voltage drop, are modelled by means of parallel conductive and serial resistive, respectively. The derived result of that is Telegrapher's equations which can

fully be fitted for plenty of practical applications [48].
Nevertheless, these equations may not be sufficient to handle certain effects, such as memory effects in magnetization and polarization processes and the effect of accumulation of electrical charge on the wire. Neglecting such effects was well understandable which is based on particular circumstances considering large-scale structures and signals with a low frequency. However, this must be re-considered when dealing with modern VLSI systems. For the purpose of addressing this, numerous models of transmission line have been developed recently. Many studies have utilized fractional elements rather than traditional elements. Accordingly, different generalization models have been developed-the most prevalent models are listed below.

- The time fractional Telegrapher's equations were considered in [140, 40] by means of numerical and analytical methods on bounded and unbounded domains, while the forcing term is presented in [107]. The time-fractional of this equation has been studied with only two different orders of fractional differentiation zero and two [16]. On the other hand, [38] considered multi-term time-fractional Telegrapher's equations to obtain the highest derivative in processes of diffusion type. In this study, a fractional differentiation with n order has been assumed, where n is an integer. Furthermore, [47] developed an analytical and numerical scheme for the one dimensional and two dimensional.

- The space fractional Telegrapher's equations have been considered in [141, 86]. [141] analysed and discussed the fundamental solution of the equation with fractional order between zero and two using Fourier transform. [86] introduced a procedure for applying the matrix to solve the equation in fractional domain in space and time, one at time, using the wavelet approach.

- The space and time fractional Telegrapher's equations were considered in [68, 34], where fractional Laplacian was used to solve the equation, which is assumed comprising of two fractional variables with two different orders of time-fractional derivatives. In [153], a similar assumption was examined using the method of the joint Laplace and Fourier transform. [33] and [207] used the same method

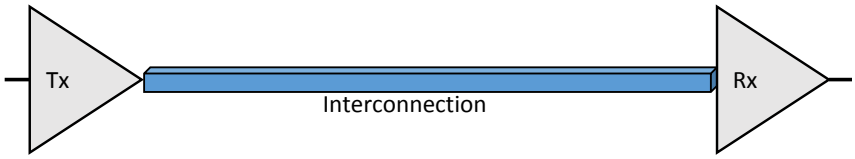


Figure 2.4: A simple interconnect structure.

but proposed the case of two different sequential orders of time-fractional derivatives with a non-symmetrical space fractional derivative.

2.3 INTERCONNECT SYSTEM LIMITATIONS

The circuit model is extremely valuable for designing and analysing a new circuit and estimate the performance of the present techniques. To understand design environment simply, it should probe the parameters of devices (transmitter and receiver) and wires (interconnection), as illustrated in Figure 2.4. For that, it would be convenient to study their inherent attributes separately and then combining the results together to have an integrated model.

2.3.1 *Fundamental limits*

In this section, unchanged and immutable limits of interconnect are discussed which are fundamentally based on principles represent the physical world. These limits cannot be changed with the increase of device structure complexity, novel circuits techniques, or inventive architectures [49, 129].
The first fundamental limit is based on Shannon's communication theorem related to the capacity of the channel, where the equation below represents the maximum channel capacity $C_{b/s}$ with effect of a white Gaussian thermal noise [180]

$$C_{b/s} \leqslant B_r \log_2 \left(1 + \frac{P_s}{kTB_r}\right) \tag{2.18}$$

where B_r is the bandwidth of the receiver, P_s is the average signal power of the input, kTB_r is the Johnson thermal noise power delivered to a matched load, k is the Boltzmann's constant ($1.38 * 10^{-23}$J/K), and T is the room temperature (300 K). It can

be concluded the minimum energy per bit $E_{b(min)}$ by assuming $E_b = P_s/C_{b/s}$ and based on (2.18) [49]:

$$E_{b(min)} = \ln(2)kT \tag{2.19}$$

This is the minimum energy transfer of a binary transmission on interconnect, less than that makes the transition undifferentiated from the white noise and whatever the encoding techniques to error correction used. This energy also governs the limitation of a lowest swinging on buses.
Secondly, the function of interconnect is to transmit signal swinging events which are normally generated by computational elements. Therefore, the essential limit on interconnect performance is established by the shortest delay between a switching event in a transmitter and a transition detected at a receiver, with the assumption that interconnect is lossless and noise free to find the shortest delay. The speed of transmission is generally known depending on the speed of an electromagnetic wave propagating in free space which is quantified by Maxwell's equation, Then Helmholtz derived an equation that describes the propagation of the electric field and formed free space wave travelling speed C_o to [102]

$$C_o = \frac{1}{\sqrt{\mu_0 \varepsilon_0}} \tag{2.20}$$

where μ_0 and ε_0 are the permeability and the permittivity of free space, respectively. Then the speed of the communication between the transmitter and the receiver should not exceed the latency τ of the channel [183]. Hence,

$$\tau \geqslant \frac{X}{C_o} \tag{2.21}$$

This fundamentally means that the electromagnetic propagation in free space limits interconnects performance.

2.3.2 *Limitations of the device*

The basic MOS scaling principle started by Dennard [52], who predicts how IC operating ranges and layouts will alternate as inevitable enhancements in IC technology occur. The principle assumes a proportional scaling down in all dimensions; the

reduction amount is denoted by $S_r > 1$, where any dimension $X \to X' = X/S_r$. It additionally assumes retention of constant electrical fields, leading to a voltage reduction by $v' = v/S_r$. According to this scaling theory, we are able to predict interconnection propagation times for a scaled design. By recalled (2.1) and (2.6), the change in line resistance and capacitance can be calculated respectively as

$$R' = \rho \frac{X'}{t'w'} = S_r R \tag{2.22}$$

$$C' = \varepsilon \frac{w'X'}{h'} = \frac{C}{S_r} \tag{2.23}$$

Since $R'C' = RC$, the interconnection propagation times defined by the RC product remain firm. The scaling theory precisely predicts that interconnections will not gain in speed, MOS transistors do. Time delay constant τ of a distributed RC is given by

$$\tau = rcX^2 \tag{2.24}$$

where X is interconnect length, r and c are the distributed resistance and capacitance per unit length, respectively. This equation clearly shows that the delay of an unbuffered long link is quadratic in its length. From these arguments, it can be concluded unquestionably that the latency value of interconnect will not change despite interconnect ideally minimized. In other words, the negative effect of the interconnect on performance would not mitigate in spite of a new emerged technologies as a result of not only its transistors numbers is increase but also die area as shown in Figure 2.5. Without changing this scenario, interconnection delay will remain dominant in the scaling process.

2.3.3 *Limitations of the circuit*

To this end, the interconnect issues have been listed separately. Hence, to have the understanding of interconnect circuit limitations, an assumed basic model with main involved parameters has been used. The approach, in this section, deals with a single

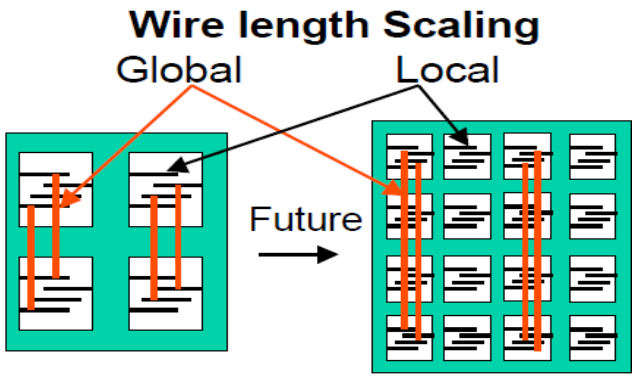


Figure 2.5: global interconnect effect with new generations.

interconnect. Also, it does not taken into consideration the noise impacts and accuracy was sacrificed for simplicity in order to deduce the main factors that affect the performance of such a system.

The model shown in Figure 2.6 consider a line with RC distributed parameter that is driven by a simple inverter has loaded with capacitor of c_t and an internal resistor of R_t with neglecting source capacitance c_p considering C compensates this parasitic. This model imitates a point-to-point interconnect on single-layer driven by a CMOS device and connected to the next gate. We have assumed this model because it is used over a wide range of VLSI design theories [20]. In addition, the effects of the line inductance has been deliberately ignored. Since, in the approach here, what is important is the impact of the line RC delay and not the characteristic impedance of signal lines in VLSI circuits [20]. At this point, as an intuitive prediction from the model, it is clearly elucidated from the structure that the transistor parameters have an impact on the line and the crosstalk issue.

For this interconnection, a differential equation can be given as:

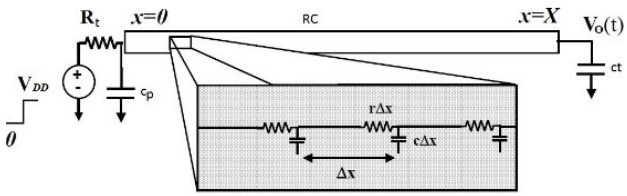


Figure 2.6: RC interconnect model with resistive source and capacitive load.

$$\frac{\partial^2 V}{\partial x^2} = rc\frac{\partial V}{\partial x} \tag{2.25}$$

where r and c are the unit length resistance and capacitance of interconnect respectively. The far end voltage can be revealed in a form of an expanded series. This technique was presented in [171, 172] to describe the system in Figure 2.6 as follows

$$\frac{V_o(x,t)}{V_{DD}} = 1 - exp\left(-\frac{\frac{T_d}{RC} - 0.1}{R_T C_T + R_T + C_T + 0.4}\right) \tag{2.26}$$

where T_d is the delay time , R_T=R_t/R , and $C_T = c_t/C$. Rearranging the (2.26) by solving T_d in term of V a formula can be obtained [172] for the delay time t_V from the initial (t = 0) to the time when far end voltage reaches (V_o/V_{DD}). Hence,

$$t_V = RC[0.1 + ln(\frac{1}{1 - V_o/V_{DD}})(R_T C_T + R_T + C_T + 0.4)] \tag{2.27}$$

This form can be simplified by assuming a large interconnect. Thus, its capacitance C will be the most effective capacitance component (i.e., $c_t << C$) and transistor equivalent resistor will be the dominant (i.e., $R_t >> R$). Then, to find the approximation circuit delay, the RC distributed model has been combined in [176] and the time of transient voltage on interconnect model in [49] to produce

$$T_d = 2.3 R_t C \tag{2.28}$$

From this equation, it can be concluded that there are main factors affecting the performance of the system. These factors are the line capacitor, which is proportional to the interconnection dimensions, and the transistor resistance, which is a function of its size. In simple words, it clearly illustrates the most effective components that govern the operating point for a particular wire length. These components can be classified into technology-dependent parameters, such as ϵ, conductor width and hight from the ground, and the parameters of the operation point which are related to the relevant transistors.

2.4 POWER IN CMOS CIRCUITS

CMOS can be in two different states; a dynamic state during the signals or clocks transitions and a static state during no transitions [20, 157]. Accordingly, power dissipation sources are divided in two major classes: dynamic and static. These two components have an essential difference that is the former proportional to the switching frequency and the activity in the network, whilst the latter is independent of both. Normally, dynamic power P_d outweighs static power but, recently, leakage has emerged as a major power component, particularly, in sub-threshold systems and nanometre technologies where the device size down-scaling has led to very thin gate oxides [209]. Therefore, both should now be treated alike. The model shown in Figure 2.6 will be proposed, since it includes the most effective system components [20], where the total power P_T for that system is

$$P_T = P_d + P_{lk} \tag{2.29}$$

where P_{lk} represents the leakage power, which can be presented as following [191]

$$P_{lk} = V_{DD} I_{lk} \tag{2.30}$$

where I_{lk} is typically a particular fabrication technology parameter, as it is originating in the substrate conduction and affected by the sub-threshold voltage [209]

$$I_{lk} = 1.5 I_{off} W_t \tag{2.31}$$

where W_t is the transistor width and I_{off} is the transistor current in off state which depends on V_{DD} and the size of the devices [191]. Depending on these formulae, it is apparent that the solution to reduce the leakage power dissipation is scaling down the supply voltage, the main contributor to the leakage power. This is based on an ideal assumption that when the transistor is a turned-off switch, the current between drain and source is zero, while in fact, this is not the case. Whereas the weak-inversion current I_{off}, occasionally called sub-threshold leakage, is proportional to V_{gs}. In other words, the voltage scaling-down has to be within some trade-off according to the report in [157, 209],

which classify the reducing supply voltage as the major reason causing the drain-source leakage to increase exponentially, as provided approximately by:

$$I_{off} = I_0 \times 10^{(V_{gs} - V_{th}/S_{th})} \tag{2.32}$$

where I_0 is the current when $V_{gs} = V_{th}$, V_{th} is a threshold voltage and S_{th} is the sub-threshold swing where the drain current changes 10 times to V_{gs} change.
Secondly, power consumed during circuit switching activity is generally represented by [21]

$$P_d = \alpha_a C_{eff} V_{DD}^2 f \tag{2.33}$$

where α_a represents activity factor that its value is 0.15 [21], C_{eff} is equivalent the circuit capacitance, in this case (C, c_p and c_t), and f is the operating frequency.
Finally, it is often assumed that the N-type metal-oxide-semiconductor (NMOS) and P-type metal-oxide-semiconductor (PMOS) transistors of a CMOS gate do not become ON at the same time, but such an assumption is certainly not correct, as the finite slope of the input signal during transient produces a direct current path between supply voltage and ground for a short period of switching time T_{rise}. The power dissipation due to these short-circuit currents I_{sc} is proportional to the switching activity as well as the ratio between the slopes of the input and output signals as shown in following equation [157]

$$P_{sc} = \alpha_a T_{rise} V_{DD} I_{peak} f \tag{2.34}$$

where I_{peak} is the peak current which depends highly on V_{DD} [191] unlike I_{off}. This part of power considerably impacts the receiver circuits among the interconnect components, since it is highly dependent on the input signal slope [188].
In conclusion, based on the study for driving circuits parameters, it is certain that the intrinsic circuit power dissipation can be effectively reduced by scaling down the supply voltage.

2.4.1 *Ultra-Low-Power (ULP) techniques for driving on-chip interconnect*

In the past, the power issue was neglected and designers concentrated on performance, cost, chip area and reliability. This has changed due to the demands on emerging applications for low power and not high performance, for example in portable devices, wireless sensor networks, self-powered devices and biomedical systems [56, 78]. These applications are required to be lower in weight with longer energy source life, and to have no cooling systems. Since reduced power consumption could achieve these aims, the trend to use circuits with Ultra-Low Power (ULP) budgets seems to be the solution [56]. In the same work, it is reported that sub-threshold design shows the ability to meet the needs of the ULP design. The sub-threshold system means designing the circuits to operate in a supply (V_{DD}) no more than the transistor threshold voltage (V_{th}) [56]. This approach has emerged as the best way to fulfil energy efficiency [115], because of the reduction in sub-threshold's current driving compares to superthreshold's current and the dynamic power strongly depends on V_{DD}, see equations (2.29) and (2.33).

However the sub-threshold circuit has a frequency limited to tens of MHz [115], while in the conventional circuits the switching is at hundreds of MHz [100, 188]. This subject has received great research attention recently as an essential part of IoT requirements [78, 31, 10]. Nevertheless, with new generations of scaled technology, challenges of design reliability and the trade-off between having an energy-efficient system or one with low performance are among the major concerns in this subject [10].

There are many studies that have initiated utilising the low power consumption links as several industrial, standardization bodies are actually involved in the activity of development of solutions to fulfil the technological requirements [17]. The efforts regarding the IoT paradigm are varied and came from different scientific areas. Specifically, however, the approaches concerning on-chip interconnect circuits and the system's power dissipation can be classified into data link layer and higher techniques, physical layer techniques, and both [183]. The challenges in this field are varied, nevertheless what is important is the way to deal with these issues and the results would obtain. Designers

trying to cope with this issue have to deal not only with power dissipation, but also parasitic impedance, link delay, CMOS buffer design among other issues [56].

2.4.1.1 *Link layer techniques*

These techniques achieve power saving in network-on-chip (NoC) by using coding to modify the transmitted data, in a way, to minimize the data transition activity that takes place through interconnects. However, these techniques will not be discussed here as they are beyond the scope of this thesis.

2.4.1.2 *Physical layer techniques*

On the other hand, equation (1.1) gives designers an obvious platform for prospective schemes to satisfy the demand for an energy-efficient system, to:

- optimize the spacing and sizing of wires;
- adapt the repeaters, driving and driven circuits' design;
- reduce the supply voltage that provides the power for interconnects drivers and repeaters.

Low swing signalling is a powerful method to minimize the energy consumed due to that energy is directly related to V_{DD} and V_{swing}, but with trading off to raise the latency [183, 56, 78]. This has led many researchers [93, 198, 161] to explore this solution and have achieved roughly five-fold improvements in energy consumption for interconnect circuits with certain frequency [93].
However, using signals with low voltage swing requires a special receiver design to sense these small changes in voltage level [198]. Furthermore, other researchers have cleverly combined this technique and conventional methods [161] to design adaptive link voltage scaling systems. Through adaptive voltage scaling not only is the magnitude of voltage changed but also the operating frequency is altered to meet a varied performance to the same system. Jeong et al. [105] reported that their adaptive technique led to an improvement of 43% in power saving compared to traditional techniques.

Another group of developers [121, 73, 208, 54] have implemented a dual voltage buffer technique. Some of these [121, 73]

used two transistors with different threshold voltages in designing the buffer, reporting around a 40% improvement compared to a single threshold. This method is called dual V_{th}. Others [208, 54] used a dual supply voltage (low and High V_{DD}) and achieved approximately 50% reduced power consumption by interconnects compared to single supply voltage methods. Ho et al. [210] introduced an interconnect driver that reduces the static leakage current by using a bootstrapped inverter and an active reduction technique.

A well-known technique is repeater insertion. Many studies [201, 74, 22, 77] have been carried out to find the optimal design of this method from points of view of the ultimate cost, power, area, and delay that are to record energy saving from 20% to 25%.

The quasi-resonant approach has achieved impressive results up to 91.1% improvements in power consumption by adding spiral inductors to on-chip interconnects to achieve a balance among electromagnetic fields and reducing the proportion of energy converted to heat [166], while other approaches [82, 92] add shunt conductance to obtain a distortionless interconnect implemented on-chip. However, these methods have a primary disadvantage of requiring a large area for inductors. A number of studies have been conducted to explore the performance of sub-threshold circuits in ULP design. For instance, Gupta et al. [78] looked at the performance of devices and circuit optimization in sub-threshold design in terms of speed and robustness.

2.4.1.3 *Other techniques*

Other techniques combine two or more of the previous approaches to cope with the inherent drawbacks of individual methods. For instance, reducing the V_{swing} on wires increases the probability of error, and one solution to overcome this is to use an error control coding method with schemes which have low link swing voltage [27, 25]. In another example, Deodhar and Davis [53] have given a solution for the problem of voltage scaling weakness by inserting repeaters to improve throughput.

From the literature, power consumption could be reduced by optimizing the threshold voltage to achieve the maximum drive current and hence achieve better performance, but at the cost of an increase in the standby power [104]. In addition,

techniques such as switching activity reduction, interconnect pipelining and parallelism and logic optimization could be used [55, 127]; however, each method has its own design cons that make it inadequate to achieve the desired consumed power [127]. Another proposed solution for power dissipation reduction is via energy recovery/quasi adiabatic computation [108], but this is not easy to implement because it requires the use of high quality inductors [78]. A further useful technique in ULP is to force the circuit operate with a value of V_{DD} lower than the V_{th} of the devices. Hence, the power consumption will be considerably decreased [183, 150, 56].

Overall, a considerable amount of studies have been accomplished related to design an ultimate interconnect circuits to cope with global interconnects challenges with presenting of sub-threshold design [49]. Subsequently, the bootstrap technique with feedback technique is adopted in this thesis, while the minimum operating voltage is used to reduce the power that interconnects circuits consumes. The proposed circuit has shown its ability to be reliable, efficient regarding energy and power dissipation and has less influence on the performance and area consumption [7].

2.5 OVERVIEW AND ANALYSES FOR ON-CHIP MODELLING TECHNIQUES

On-chip interconnect is becoming significantly dominant in large IC designs, where interconnection networks are extensively used in SoC in the realm of IoT [178]. Even with single-chip multiprocessors framework, these networks are deployed representing a scalable solution related to the communication of interprocessor [185]. These interconnects are driven by equally important circuits which are CMOS technology. These two components of VLSI systems, which considerably affect signal integrity, have attracted the attention of researchers since the emergence of this technology [46, 185]. Most of these studies are vital at predicting the signal delay and electromagnetic interference for analysis and pre-design of high-performance CMOS integrated circuits, as accurately as possible.

However, efforts to ascertain a model of CMOS gate driven interconnect composition have encountered the issue of increasing

the sensitivity of circuit performance to interconnect parasitic [145]. Hence, in the DSM nodes, the sensitivity to the variability of interconnecting parameters has also increased [152]. Therefore, the accuracy of interconnecting fabrication processes has become greatly important. In order to achieve a precise model, it requires a realistic account for the interconnect parameters to be taken. However, some of the parameters, particularly inductive and capacitive elements, are not constant with frequency varying.

Hence, the holistic approach needs to combine a precise model of the CMOS gate to transistor level circuit and the transmission line model that governs the diffusion on the interconnect. Therefore, many attempts have been undertaken to gain a realistic view in this direction; thus, a variety of models have been developed with different contributions. These attempts ranged from using a simple or accurate model trade-off of the two main components of the on-chip interconnect structure to use an accurate model for both, which means more complex models [8, 148].

The motivation behind the work in this section is to demarcate these approaches by means of a broad brush, as shown in Figure 2.7. This supposes to assist the interested researcher in pursuing previous studies as mentioned in subsequent sections and to assist in following the most appropriate approach that fits their application.

2.6 THE MAIN INTERCONNECTS MODELLING APPROACHES

In this section, several techniques related to the interconnect structure analysing and the modelling are outlined. Empha-

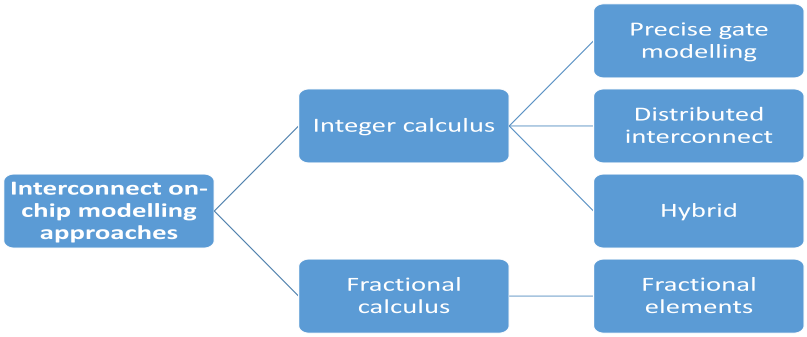


Figure 2.7: The interconnect on-chip modelling approaches.

sis has been placed on modelling approaches, starting from a one-dimensional and simple lumped issue and stretching to the more general three-dimensional nonuniform problem. The complicated models commonly utilise distributed parameters to imitate the line electromagnetic and attenuation phenomena. These parameters are therefore normally used alongside the quasi-TEM assumption to describe the behaviour of the transmission line as differential equations. However, Telegrapher's equations are valid if these assumptions can be applied in the frequency range [43, 148]. Specifically, the longitudinal field components of magnetic and electric are much smaller than those diagonally across the line. Therefore, many works have recently facilitated Fractional calculus to apply its advantages on and generalise the operation of a conventional one. Consequently, in this section, both approaches are stated.

2.6.1 *Approach based on integer-order elements*

Numerous ways have been reported to submit a realistic line model. Depending on the purpose of design considerations, each model has its own strengths and limitations compared to others. However, all these approaches started based on modelling the CMOS/interconnection structures. These interconnections are simply two or more conductors, normally Cu or Al symbolised as a strip link separated from a ground plane by an insulator, generally Silicon dioxide (SiO_2) or Silicon (Si). Several of its widespread forms in electronic systems are the stripline, microstrip and coplanar line [185] as illustrated in Figure 2.8.

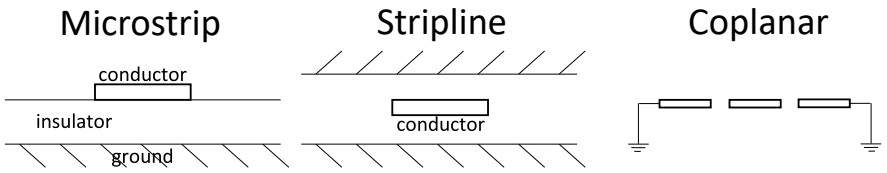


Figure 2.8: Some of interconnects structures.

In fact, such structures are to guide the flow power through the longitudinal direction (let be z direction) of the link to restrict the power as much as possible from scattering in other directions so minimal losses achieved. The transmission line model primarily has four parameters that are the inductance of the line L, the ca-

pacitance between the line and the ground C, the resistivity loss of the line R and the dielectric loss of the surrounded material G. The parameters distributed in series for R and L and in parallel for G and C along the line, as a small sections of Δz, as shown in the Figure 2.9, to obtain the line differential equations. $R\Delta z$, $L\Delta z$, $C\Delta z$ and $G\Delta z$, in this figure, represent the parameters per the section equivalent circuit, whereas the v(z,t) and I(z,t) denote the voltage and current of the travelling signal, respectively.

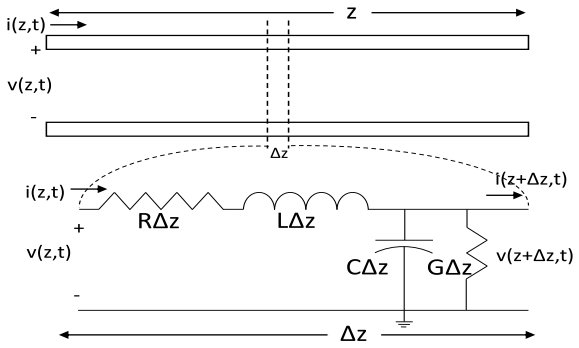


Figure 2.9: The RLGC unit of the transmission line equivalent.

Subsequently, by applying Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) to the circuit and dividing the result by Δz and letting Δz to zero, the partial differential equations will be given

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t} \tag{2.35}$$

$$\frac{\partial i(z,t)}{\partial z} = -Gi(z,t) - C\frac{\partial v(z,t)}{\partial t} \tag{2.36}$$

These time-domain equations are termed Telegrapher's equations [43]. To transfer it to frequency domain, Fourier transform is applied to have

$$\frac{\partial V(z)}{\partial z} = -RI(z) - j\omega LI(z) \tag{2.37}$$

$$\frac{\partial I(z)}{\partial z} = -GV(z) - j\omega CV(z) \tag{2.38}$$

These equations are the basis for single and multiple conductors modelling solutions [170]. With increasing the speed of the interconnects circuits and the need for full-wave solutions, the modelling of high-speed interconnects has encountered issues of being physically consistent. In order to be physically consistent, the electrical interconnect model must satisfy the fundamental properties of causality, stability, and passivity.
The property of stability is related to the boundedness of the system responses. Considering the stability definition of the so-called bounded-input bounded-output (BIBO), the system is stable if for all bounded inputs the output is bounded [84]. The stability can be guaranteed in such a system if and only if all $h(t)$ elements are thus [195]:

$$\int_{-\infty}^{+\infty} \left|h_{ij}(t)\right| dt < +\infty \tag{2.39}$$

The $h(t)$ is the impulse response of the system, with its elements $h_{ij}(t)$ being the response at port i when an ideal impulse is applied at port j, with setting all other inputs to zero.
Passivity is also one of the main properties that have a direct effect on transmission line model to be physically consistent [123]. Regarding electrical circuits, the passivity is that the passive circuit absorbs real power and, hence, the total energy delivered to the circuit is positive. Mathematically, the passivity definition depends on the representation adopted for the n-port network, where [211] identified representations of impedance or admittance. A multi-port network is considered to be passive if [195]:

$$\int_{-\infty}^{t} v^{T}(\tau) i(\tau) d\tau \geqslant 0 \tag{2.40}$$

for all admissible port currents $i(\tau)$ and voltages $v(\tau)$ and all t. Integral in (2.40) represents the aggregate net energy absorbed up to instant t by the system. Therefore, in any passive system, this energy must be positive for all t. This condition is satisfied if two states hold; the absorbed energy is more than the generated, and any potential generation happens after absorption.
Given this, it is not surprising that every passive system is causal, because the noncausal systems first generate energy and then absorb it, which has been proven in [195].

Even though the transmission line is passive in terms of physical reality, its model could be lacking the passivity owing to the errors presented during the different approximations [170]. Accordingly, interconnects as passive systems must be characterized by a model has passivity or, otherwise, nonphysical and unexpected results may occur. In order to check the passivity of a model, frequency sweeping of the singular values of the transfer function is performed. This technique is called the straightforward approach which consumes time for a large model due to a large frequency band involved. On the other side, poor sampling may lead to inaccurate results [170].

2.6.1.1 *The precise gate modelling with lumped circuit approach*

In this section, attention is drawn to approaches that have focused on a precise gate model, while the associated interconnect load has been approximated to a simple lumped circuit. Shichman and Hodges [182], described the Insulated-gate field effect transistor (IGFET) as a new equivalent circuit in which the drain current varies quadratically to the adequate gate voltage. This model, a well-known square law model which is designed to be compatible with the computer-aided analysis of the CMOS switching components, has therefore been used extensively. However, the model's accuracy decreases when the metal-oxide-semiconductor field-effect transistor (MOSFET) channel length is reduced. Hence, Sakurai et al. [173] proposed an Alpha-power law model (2.41) where he had included the effects of carriers' velocity saturation, the drain/source resistance parasitic and the slope of the input waveform. Therefore, it has been extensively implemented into the latest formula, i.e. the alpha-power law model model, for the short channel transistors representation.

$$I_D = \begin{cases} 0, & V_{GS} \leqslant V_{th0} : \text{cutoff region} \\ k_l(V_{GS} - V_{th0})^{\alpha_s/2}, & V_{DS} < V_{D-SAT} : \text{linear region} \\ k_s(V_{GS} - V_{th0})^{\alpha_s}, & V_{DS} \geqslant V_{D-SAT} : \text{saturation region} \end{cases} \tag{2.41}$$

where V_{D-SAT} is the saturation voltage of the drain terminal, k_s and k_l are the transistor transconductance in saturation and linear regions, respectively, α_s denotes the velocity saturation index and V_{th0} is the threshold voltage when bias is zero.

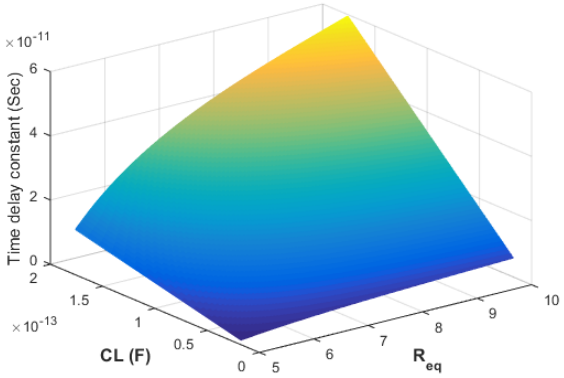


Figure 2.10: Time delay constant of first approach with C_L and R_{eq}.

However, the alpha-power model has two primary curtailments, which are the considerable simplifying of the interconnect load to a lumped capacitor C and the invalidity of neglecting the p-channel transistor when the input slope is slower than the output ramp. Despite that, its approximation is valid given that it is normally in VLSI that the output ramp is exceeded by one-third of the input ramp. Additionally, Sakurai expressed the delay t_{pHL} and t_{pLH} as follows

$$t_{pHL}, t_{pLH} = (\frac{1}{2} - \frac{(1-\nu_r)}{(1+\alpha_s)})t_T + \frac{(C_L V_{DD})}{(2I_{D0})} \tag{2.42}$$

where $\nu_r = \frac{V_{TH}}{V_{DD}}$, t_T is the input waveform transition time and I_{D0} is the current of the drain at ($V_{GS} = V_{DS} = V_{DD}$). Figure 2.10 demonstrates the interaction of the parameters to form the design delay constant, which will be discussed in Section (2.7). Subsequently, [60] has comprehensively investigated Sakurai's model for any rise time in the input signal and different outputs loading. The analytical scheme presented in [60], used the curve fitting technique to evaluate the output transition time and delay of CMOS driver and a capacitor load. This work achieved an analysis accuracy within 3% of the SPICE results. Furthermore, based on the alpha power model, a study [26], has been conducted to include the impacts of gate-drain coupling capacitance and short-circuit current. They introduced an analytical model for the short-channel of the inverter circuit, which considered most of the affecting factors. Moreover, in comparision with SPICE simulation, this model showed less than 3% error.
The improvement in the ICs scaling down maximises the inter-

connect impact, that makes describing the interconnect as a capacitor imprecise. In addition, with the output impedance of the CMOS gate becoming more comparable with the interconnect resistance (R), many researchers [156, 81, 37], have involved this resistance in the CMOS gate driving interconnect modelling. The advantage of models including the (RC) line and CMOS gate is that they are reliable and simple. Moreover, Kaushik et al. [113] explored the inductive L effect of the interconnect to analyse the CMOS gate driving RLC structure. However, the principal drawback of the solutions, which have been mentioned above, is related to neglecting the transmission line behaviour of the interconnects.

2.6.1.2 *The distributed circuit approach*

A considerable amount of research has focused on the interconnect model and signal diffusion in the wires medium. This is different from the perspective of the previous approach, which represented the driver component as a simple linear resistance in the CMOS gate driven interconnect circuit. The value of the resistor is identified during MOS switching from the rate value of the equivalent PMOS and NMOS resistances R_{eq} in the saturated state [46], as given by

$$R_{eq} = \frac{3}{4}\frac{V_{DD}}{I_{sat}}(1 - \frac{7}{9}\lambda V_{DD}) \tag{2.43}$$

where V_{DD} is the supply voltage, I_{sat} is the drain saturation current and λ is the channel length modulation. Based on this simple model, Elmore delay model [169] for RC networks was introduced initially, then extended to be lumped RLC by [110], who proposed an analytical approach and [98], who used the curve fitting method. The issue of crosstalk noise for coupled RC lines has been studied in [177, 65, 57, 19]. Sakurai [177] proposed compact expressions describing this issue under worst case time delay τ and derived the following form of a distributed RC line

$$\tau = 0.7693 R_{eq} C_{int} + 0.377 R_{int} C_{int} \tag{2.44}$$

where R_{int}, C_{int} are interconnected parameters. Figure 2.11 shows the influence of the design parameters on the time delay

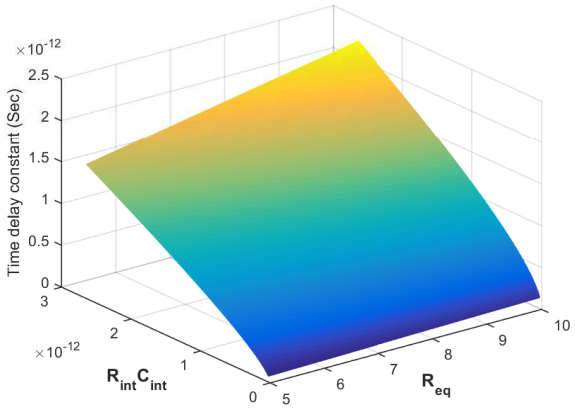


Figure 2.11: Time delay constant of second approach with $R_{int}C_{int}$ and R_{eq}.

constant, which will be discussed in Section (2.7).
Bai et al. [19] calculated the victim's receiver effective resistance efficiently where nonlinearity is considered. Considering the transmission line influence, Sakurai's model [177] was extended by Davis and Meindl [50], who derived a compact analytical expression describing the high-speed transient response for a distributed RLC interconnect and, in [51], a crosstalk model for two and three coupled distributed RLC lines was also proposed. These expressions involve the values of the mutual and self-inductance and given a physical explanation and accurate estimation of propagation delay, crosstalk and transient response for global lines. [6] proposed a crosstalk model for two coupled lossless transmission lines based on even-odd mode propagation. Subsequently, to capture the maximum noise value, the model was improved for low-loss transmission lines effect.

The multiconductor transmission lines transient analysis is of interest for researchers to obtain comprehensive solutions adopting numerical methods, For instance, the Method of Characteristic (MoC) [206], the method of asymptotic waveform evaluation (AWE) [30], the cascaded ABCD matrixes based method [128], the method of Finite-Difference Time-Domain (FDTD) [146, 164, 119] and so on have been reported. These solutions are commonly used in commercial circuit simulators. Nevertheless, the numerical techniques depend on the direct or indirect discretization of Telegrapher's equations, which means the transmission line is divided into sections of small length and then finds the total solution. This requires managing the inefficiency challenge when

modelling long lines because of the direct proportion between the sections number for a transmission line and its length. Thus, the simulation requirements will be higher if the length of the transmission line is longer.
However, attempts to discover a more accurate model that covers most parameters in interconnecting circuits are ongoing.

2.6.1.3 *The hybrid approach*

Substantial research has developed mixed but complicated time/frequency models to solve the challenge of obtaining a precise analysis and evaluation of the CMOS gate driven interconnect structure. Most of these studies, in this approach, attempted to establish an aggregate model incorporating both previous approaches, i.e., the precise gate modelling approaches and the distributed circuit approaches. Thomas et al. [194] constructed a direct link between SPICE and FDTD software to analyse hybrid systems. Additionally, [139] disintegrated the hybrid system analysing the passive part, which is the on-chip interconnect and used the FDTD method to analyse an active part which was analysed using SPICE. However, the direct method is complicated and obviously relies on the SPICE circuit analysis simulator.
Therefore, to reduce this complexity macromodelling techniques [217, 58, 39, 218] and model order reduction algorithms [138, 59, 35, 213, 72, 12, 125, 147, 205] have been adopted to construct a less complex model of the interconnect system from various characteristics in the frequency and time domains, acquired from empirical experiments directly or from a full-wave electromagnetic simulator, such as a Fast Field Solver [187]. The most popular algorithm among those is the one based on generalising the MoC method [217, 58, 39, 218]. In general, these methods used delay formulas based on

$$t_d = l\sqrt{L(\infty)C(\infty)} \tag{2.45}$$

where $L(\infty)$ and $C(\infty)$ are the interconnect parameters at DC and the highest frequency. The essential challenge with this algorithm is the lack of passivity, consequently solutions have been suggested to overcome this issue by changing the methodology [58, 39] where the curve fitting is the key feature in this case. Several other researchers [138, 59, 35, 213, 72, 12, 125, 147, 205]

proposed algorithms guaranteeing the passivity of the macromodel by using approximation methods, such as passive reduced order interconnect macromodelling algorithm (PRIMA) [138], matrix rational approximation [35], discrete model based on compact finite differences [35], integrated congruent transformation [213], [72], a method of partial element equivalent circuit [12], and macromodels based on FDTD [125, 147, 205]. Nevertheless, in these algorithms, SPICE or any circuit simulator is expected for the analyses of nonlinear components with the interconnect macromodels.
In addition, the numerical approach is commonly used to comprehend the nonlinear digital components and transistors behaviours based on extending FDTD solver [189, 151, 120, 71, 76, 112, 124]. The study in [76] reported discrete-time behavioural modelling to represent the digital drivers and receivers where it used a resampling method to match the FDTD scheme and discrete-time model. Although, the attempts [189, 151, 120, 71, 76] have not employed an accurate transistor-level circuit for crosstalk and delay prediction, the equations of distributed lumped components have been solved by Newton-Raphson iteration which makes the analysis even slower. Kaushik and Sarkar [112] introduced a crosstalk model presenting the effects of the CMOS gate nonlinearity. An Alpha power-law model was used, in addition to transmission line behaviour for only two coupled lines. Subsequently, Li et al. [124] utilised the FDTD solver to analyse more than coupled lines driven by the CMOS gates based on a numerical method to analyse a single RLGC line. However, they neglected transistor finite drain conductance; thus, the model will be inaccurate with technology scaling down.

2.6.2 *Approach based on fractional order elements*

The idea of the generalisation of integer order integral and differential equations to non-integer order integration and differentiation is a part of mathematics; nevertheless, it did not gain the attention due to its complexity compared to integer calculus and the absence of the applications that can be applied in [90]. In the recent decades, interest in fractional calculus has been steadily increasing. There are many formulations of fractional op-

erators. Particularly, Caputo [90] provided one for the fractional derivative (D^{α}) and integral (J^{α}), supposing that $\alpha > 0$. Then

$$J^{\alpha} f(t) = \frac{1}{\Gamma(\alpha)} \int_0^t (t-\tau)^{\alpha-1} f(\tau) d\tau, \alpha \in \mathbb{R}, t > 0 \tag{2.46}$$

$$D^{\alpha} f(t) = D^{\alpha}(J^{m-\alpha} f(t)), m-1 < \alpha \leqslant m, m \in N \tag{2.47}$$

suppose that $\alpha > 0$ and $f(t)$ is a function. It is obvious from both equations above that the superiority of the global feature of this derivative function in comparison to the classical one, i.e., the ability to memorise previous events or the history of a certain function to calculate its derivative unlike the integer-order derivative. In this direction, many natural phenomena and physical applications can utilise this facility to model long memory dependence inherent attribute. Moreover, improving the design flexibility, optimisation freedom of the system and response fitting due to the added parameter (α), can be added. Therefore, during the last three decades, numerous studies related to this subject have been presented in different fields, such as bioengineering circuit theory, mechanical, chemistry and electromagnetic, introducing its theoretical and experimental verification based on fractional calculus [142, 90].

Within the relevant field, fractional order mathematical models are gaining importance because studies have been carried out to fractionalise electromagnetic equations. Engheta [64] discussed solving inhomogeneous Helmholtz's equations by applying the general fractional operator and introducing the analysis without a loss of generality, while Naqvi and Rizvi [134] improved the solution by considering it in multilayers with parallel plane interfaces. Later, Maxwell's equations were then generalised in fractional space [221] and an exact solution to the cylindrical wave equation was presented in [220]. Moreover, fractional calculus was applied in many engineering domains, for instance, RC, RL and RLC circuits [160, 159]. The idea of a fractional order model was investigated to realise that the I-V relation in the capacitors and inductors would correlate with this model [106, 186].

Furthermore, the distributed segments of the transmission line using fractal components are examined in [95, 179]. Addition-

ally, the generalisation concept of the Transmission line modelling (TLM) using fractional order elements was discussed in [95] depending on lossless line, whereas the analysis of the model causality of RLGC transmission line with measurement verifications at THz was considered in [179]. Recently, [45] proposed a transmission line model utilising fractional calculus to include the phenomenon of accumulating the charge along the line and hereditary effects of the line capacitive and inductive.
The approach here is evidently considering again the transmission line scheme illustrated in Figure 2.9, although this time the integral elements of line inductive and capacitive are substituted with fractional ones to build the segments as shown in Figure 2.12. By proceeding through similar conventional procedures,

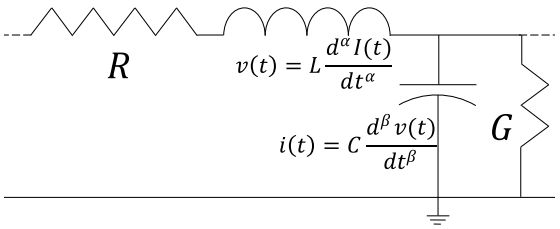


Figure 2.12: Fractional order model of the transmission line segment.

the Telegrapher's equations will be obtained as follows

$$\frac{\partial V(z,t)}{\partial z} = -(R + (j\omega)^{\alpha} L) I(z,t) \tag{2.48}$$

$$\frac{\partial I(z,t)}{\partial z} = -(G + (j\omega)^{\beta} C) V(z,t) \tag{2.49}$$

Then, the characteristic impedance (Z_0) and the propagation constant (γ) can be found

$$Z_0 = \sqrt{\frac{R + (j\omega)^{\alpha} L}{G + (j\omega)^{\beta} C}} \tag{2.50}$$

$$\gamma = \sqrt{(R + (j\omega)^{\alpha} L)(G + (j\omega)^{\beta} C)} \tag{2.51}$$

where ω is the angular frequency and α and β are fractional parameters of L and C components, respectively, and $\alpha, \beta \in (0, 1]$. The principal reason for this expansion is the expectation that

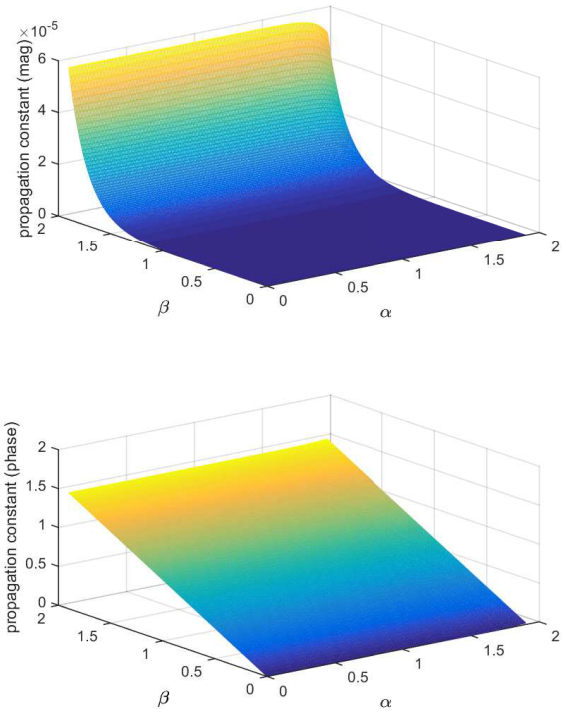


Figure 2.13: Propagation constant in the fractional approach with α and β.

the use of this field theory will be a much more effective way of tackling problems related to dispersion and non-quasi-static effect and non-TEM modes, as has been observed up to now with the conventional theory. In other words, the fractional derivatives can be usefully employed for describing a lot of phenomena, such as the loss caused by the effects of frequency-dependent dispersion and non-quasi-static. Moreover, this increases the level of freedom in the design of TLM and the study of its characteristics. In addition, if the fractional orders have been set to one, the conventional formula will be retrieved.

2.7 DISCUSSION AND CASE STUDY

Although the aim of this work is to provide a review regarding the modelling of the on-chip interconnect methods and classify them, it may be beneficial to discuss the highlighted points and comment on the principal differences. The calculation of the delay time in each approach represents one of the principal differences in how the on-chip parameters are affected.
In our experiments, the transistors are selected to have the sym-

metrical characteristics and have the same rise/fall, so the CMOS drivers' channel length is 0.18μm, while the widths are 20μm and 10μm for PMOS and NMOS, respectively, and in all cases, the conductance G was disregarded because of its negligible value. These parameters are representative of the node technology and here it is 180nm technology. Figure 2.10 displays the parameters that affect the time constant of the interconnect structure in the first approach. Furthermore, the linearity impact of the load capacitance C_L and the equivalent transistor resistor on the time delay constant, can be seen. However, the effect of C_L is greater and overestimated, which may be because this approach was developed with a high scale of technology.
Figure 2.11 identifies the prime parameters affecting the second approach time constant calculation. The counted parameters in this approach have a balanced impact on delay calculations and the interconnect parameters and especially its resistance value were calculated due to scale down development.
The third approach normally uses a micromodel to extract or estimate the time delay and rely on it. Nonetheless, despite evaluating the delay time accurately, this is limited to the conditions and hypotheses of the proposed model.
Figure 2.13 not only demonstrates the propagation constant in the conventional case but as a function in α and β. In Figure 2.13, the strength of the fractional approach is evident where the flexibility of calculating and freedom of design can be seen. This method is the key solution in relation to utilising the complexity of the third approach to reform the close-forms of the first and second approaches; therefore, it seems to be the future of interconnect modelling.

2.7.1 *Case study*

Three examples are given in this section to study the mentioned models where the transient responses were reproduced using Matlab and Cadence toolkit.

Case 1: RLC interconnect of length 1mm is analysed. The voltage source of the line is unit step waveform with rise/fall times τ=10ps and the voltage source of the line is the power supply voltage. The load capacitance is CL=50fF and the interconnect

parameters are C=350aF/μm, L=0.9pH/μm and R=10mΩ/μm. Linear driver [51], lossless line [112] and FDTD solution [124] have been implemented as shown in Figure 2.14.

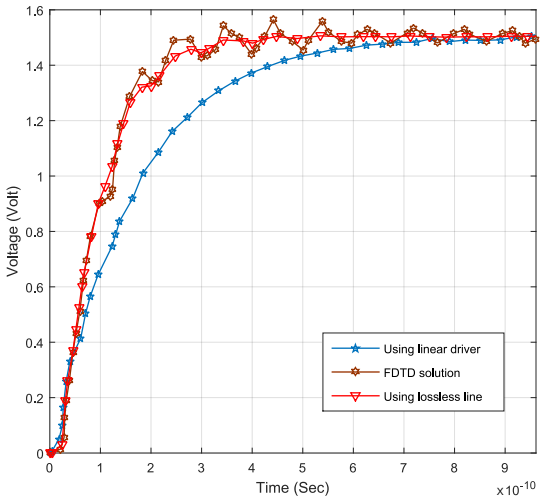


Figure 2.14: Time domain responses of the RLGC interconnects.

The figure clearly indicates that the overrating of propagation delay has been calculated by the linear driver model, in contrast to the two other models. These two closely match each to the other, while underestimating to ripples value in the waveform for lossless line solution.

Case 2: In order to elucidate the passivity effect of the MoC, a comparison was completed between MoC [206] and passive MoC [58] solution methods, as shown in Figure 2.15. The figure illustrates the transient responses of these selected models at the far end of the RLC interconnect of length 10cm, corresponding to a unit step input voltage with a fall/rise time of 0.2ns. The interconnect parameters are C=2.24pF/cm, L=4.87nH/cm and R=6.79Ω/cm. The transient response shown in Figure 2.15 clearly states the issue of the nonpassive feature which yields an unstable output and produces oscillation response when implements the related model.

Case 3: Figure 2.16 shows the percentage error, by using Matlab analysis, for different delay models compared to Elmore delay. The results were obtained to a unit step input signal applied to a line of length 100μm and the parameters are R=0.015Ω/μm, C=0.176fF/μm and L=2.46pH/μm with source resistive 30Ω and capacitive load 1.8fF. The models show different responses for

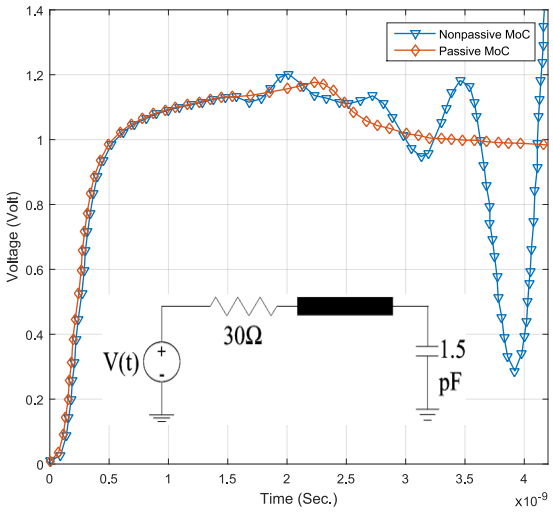


Figure 2.15: Far end transient response of passive and nonpassive MoC.

one system, and this is because of each of them have their own approach to the system. For instance, Ismail [98], which has the highest error percentage, has used the curve fitting approach to allocate the parameters in this model and to some extent, he overestimated the inductance value. The next in percentage error value was [173] (named Sakurai I in figure) and that is because this model concentrates somewhat on the value of the capacitance of the driver load rather than the other parameters. However, his second model [177] and Davis model [50] show the lowest error percentage. The reason for this similarity is that Davis's work was of high consistency with Sakurai's model. Finally, Dounavis's model [58] saw approximately 2% error in advance of the exact value.

Finally, all four models employed to describe a CMOS gate driving a line are overviewed in Table (4.2). In this table, a variety of approaches such as pure device models, closed-form interconnect models for single lines, macro or reduced-order models that model large interconnect systems, and finite-element models have been included regardless of these approaches complexity. This table offers the key points and fundamental considerations for each model depending on the basic of the approach and the cases studied in the previous section. In addition, the formula has been used in the model that provides the mathematical view,

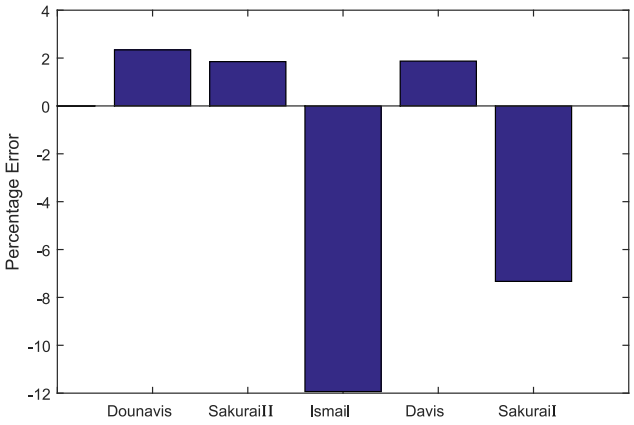


Figure 2.16: Transient response of different approaches.

if the author mentioned the formula, it was because several studies did not mention a close-formula, specifically those rely on the micromodel or prototype model to calculate the delay or estimate it.

2.8 SUMMARY

The primary conclusion to be extracted from this chapter is that interconnections are playing a dominant role in affecting the digital VLSI circuits performance. Therefore, signal propagation on-chip carriers must be interpreted much more precisely. It is preferable to consider the interconnect scheme options earliest in the design flow in order to ensure chip yield and to avoid high design expenses by relying on costly full chip verification and correction methods at a post-layout stage. Consequently, an analytical model has been concluded to connect between the design space and the performance of the interconnect circuit. A summary of transmission line models has been exhibited in this chapter. Different interconnect scheme options have been reviewed as well.

Table 2.1: On-chip interconnects modelling approaches summary

The approach	The Benefit	The drawback	The formula, if mentioned.
The integer-order approach.			
The precise gate modelling with lumped circuit.			
Shichman and Hodges [182]	These models have been extensively used in computer-aided analyses of CMOS switching circuits.	The proposed models do not give accurate results as the channel length is reduced.	$I_d = K_1(V_{GS} - V_T)^2(1 + l\|V_{GS} - V_{GD}\|)$ $K_1 = \frac{\mu C}{2}\frac{W}{L}$
Sakurai et al. [173]	It has been widely used for the representation of short-channel transistors.	The approximation is valid if the input slope exceeds one-third of the output slope, which is usually true in VLSI. A C load represents interconnect.	$I_{D0} = \frac{W}{L_{eff}}P_C(V_{GS} - V_{TH})^\alpha$ $t_{pHL}, t_{pLH} = (\frac{1}{2} - \frac{(1-v_T)}{(1+\alpha)})t_T + \frac{(C_L V_D D)}{(2I_D 0)}$
Dutta et al. [60]	The accuracy of the analysis is within 3 % of SPICE results.	Neglect transmission line effect of interconnects.	$t_{rout} = (1 + \frac{a_1}{\tau_0}) * t_{rin} * \text{Slope}, \tau = \frac{t_{rin}}{t_o}$
[81, 37, 156]	This generic linear RC model has the advantage of being simple,and reliable.		$V_{(t)} = V_{s(t)}e^{-\frac{t}{R_{dr}C_{eff}}}$ [81] It is valid up to some time-point.
Kaushik [113]	Studying the inductive,effect of interconnects.		Four regions of CMOS operation are considered for fast and slow input ramps to obtain the output voltage expression.
The distributed circuit approach.			
Rubinstein [169]	Simplicity.	Neglect inductive effect of interconnects.	$V_{out(t)} = V_{DD}(1 - e^{\frac{-t}{RC_T}})$
Kahng et al. [110]	More accurate, model for lumped RLC nets used analytic approach.		$\frac{V(1,t)}{V} = \nu = 1 - e^{-(\frac{t}{R_T C_T + R_T + C_T + 0.4})}$
Ismail et al. [98]	Model for lumped RLC nets used curve fitting method.	Not very accurate	$t_{pd} = 1.047e^{(\frac{\eta}{0.85})} + 1.39\eta, \eta = \frac{1}{2}\frac{\sum_k C_k R_k}{\sqrt{\sum_k C_k L_k}}$
Davis and Meindl [50, 51]	These give an explanation for the transient response of, high-speed distributed resistive-inductive-capacitive interconnect.	Complex	$\tau = 0.7R_o C_o k + 1.4L\sqrt{R_o C_o \tau(2c_{gnd} + 4c_m)} + 0.4\frac{(2c_{gnd}+4c_m)L^2}{k}$
[146, 164, 119]	These general solutions for transient analysis of multi-conductor transmission lines (MTL) are numerical methods.	The linear approximation of CMOS driver is not accurate since CMOS transistors operate partially in linear state and partially in saturation state during switching.	Non.
[30]			In conventional AWE techniques delay factor ($e^{(-s\tau_0)}$)
[206]			, [206] is extracted prior to any approximation.
[128]			Non.
The hybrid approach.			
[217, 58, 39, 218]	A popular way for analysis of hybrid systems to,construct a link between FDTD, software and SPICE software.	The difficulty with MoC-based algorithms is the potential loss of passivity.	$t_d = l\sqrt{L(\infty)C(\infty)}$ $\tau = (L(\infty)C(\infty))/(L(\infty)G(0) + R(0)C(\infty))$
[138, 59, 35, 213, 72, 12, 125, 147, 205]	These guarantee the macromodel passivity.	A circuit simulator is required for system-level analysis of interconnect macromodels combined with nonlinear elements.	Extract from SPICE model (algorithm).
In [76]	Extended FDTD scheme to include nonlinear components such as transistors and nonlinear digital components.	This FDTD scheme did not include a precise transistor -level circuit for the delay and crosstalk prediction.	Line delay is calculated empirically.
Kaushik [112]	Included the nonlinear effect of CMOS gate and transmission line,effect of interconnects.	This model is based on even-odd mode, hence only suitable for two coupled lossless lines.	Analytical expressions for Four regions of fast and slow input ramps input for CMOS gate, that is driving an inductively and capacitively coupled interconnect, are found.
Li et al.[124]	Gives analyse time delay of CMOS-gate-driven single RLGC line.	This model is highly inaccurate under the conditions when the technology is scaled down, due to the ignorance of finite drain conductance.	used $V_{in}(t) = \begin{cases} V_{DD}(1 - \frac{t}{\tau}) & 0 \leqslant t < \tau \\ 0 & t \geqslant \tau \end{cases}$ with Alpha law to represent input.
The fractional order approach			
[95]	Who introduced the concept of transmission line modelling in the fractional-order domain and effect of the fractional-order parameters to compensation for power loss.	These approaches neglect the CMOS driver effect, where they were more interesting about solve the transmission eq. using fractional elements.	$\gamma = \sqrt{L_d C_d}\omega^{(\frac{\alpha+\beta}{2})}(\cos\frac{(\alpha+\beta)\pi}{2} + j\sin(\frac{(\alpha+\beta)\pi}{2})$
Yang et al. [179]	Included (RLGC)		
[45]	Included the effects of charge accumulation along the line.		He used the Laplace transform for deriving the analytical solution of voltage and current propagation problems in integral form.

3

FRACTIONAL MODELLING FOR INTERCONNECT SYSTEM

3.1 INTRODUCTION

IoT interconnected objects have emerged and raised the amount of processed data to reshape the future of the interconnect structure. This explosion in the data volumes will require novel methods to deal with transmitting and receiving such data. It is commonly known that the delay in the interconnect dominates the delay issue in the VLSI circuits, because of the die area increase and the aggressive scaling of technology. Figure 3.1 shows clearly the exponential increase of wire delay with 1mm length to transistor delay [15]. For example, depending on the prediction, the delay of a node at the 45nm technology reached approximately 83ps, whilst the 1mm wire will produce a signal propagation delay up to 523ps [181, 29]. For this reason, in the high-speed interconnect networks as ICs packages, certain phenomena as transmission-line effects have emerged. Second-order lumped models have been used to accurately evaluate the delay for RLC interconnect lines, i.e., the representation for interconnects whose inductive impedance becomes more and more significant [163].
Furthermore, substantial research on establishing the balance between simplicity and accuracy have not come to an end with extant studies. However, achieving an accurate model for the interconnect circuit necessitates that a realistic account requires to be taken for the parameters of the transmission line. This has made it necessary to define the variance of the transmission line parameters, specifically, the parameters vary with frequency, i.e., inductive and capacitive elements. The recent advances in computer technology and emerging TeraHertz era clearly reveals such issues in forms of charge accumulation and memory effects [75, 219]. Assumptions that ignore these issues are reasonable if it has been considered that good conductors carry low-frequency signals in large-scale systems.

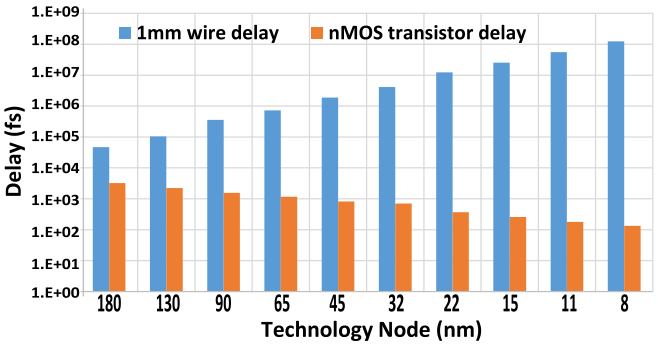


Figure 3.1: Wire delay to transistor delay ratio increases exponentially [15]

In addition, it is worth saying that a traditional elements model is insufficient to describe, especially in high frequencies, the transmission line performance because of the frequency-dependency effects. Accordingly, the parameters of the TL integer-order model must be estimated at the required frequencies and values of complex permittivity, which is cumbersome in case of a wide frequency range of interest. Moreover, the imaginary and real parts of both permeability and permittivity in a propagation media, in the physical aspect, comply with the Kramers-Kronig relation and are not independent of each other [23]. Hence, the causality issue also has an effect on TL model. In other words, it has been deliberately ignored certain effects, such as memory effects in magnetization and polarization processes, accumulation of electrical charges on the wire and so on. Neglecting such effects was well understandable which is based on particular circumstances considering large-scale structures and signals with a low frequency. However, this must be re-considered when dealing with modern VLSI systems [45, 219]. For the purpose of addressing this, fractional elements have been utilised rather than traditional elements.

Thus, as an attractive alternative, much research has started recently based on Fractional calculus [41, 142, 90]. These mathematical phenomena provide a more accurate description of a real object than the integer-order methods [41]. This is because it increases parameters in the design and, hence, increases the design flexibility to address such issues.

In this work, it has been generalised that the CMOS circuit driving a distributed RLC load to the fractional order domain. This will make the on-chip interconnect structure easy to adjust by including the effect of the fractional order elements on the in-

terconnect timing, which was not considered before. Additionally, it can be used to optimise the system delay time for a specific frequency. The aim is to achieve the simplest adaptable model with the highest possible accuracy. In accordance with the previous chapter, we make the following fundamental contributions:

1. this chapter presents a balanced background of the relevant subject;

2. bringing the on-chip interconnect system to an innovative region of design flexibility based on fractional order elements, where a new general formula for RLC interconnect network model in CMOS technology is introduced;

3. the approach here adds an important feature of robustness to the circuit design where by changing the fractional order it means there is no need for changing the circuit components any more;

4. simulations based on Matlab software illustrated the obtained advantages of the suggested approach. In addition, a number of experiments have been carried out using a numerical multiphysics tool (COMSOL) as an emulated environment to verify the model.

To the best of the author's knowledge, this is the *first* demonstration of a complete interconnect structure implemented in fractional order domain.
A single interconnect line with source and load impedance has been considered which is widely implemented in many application [197]. The approach here considered a TL whose integer elements of line inductance L and capacitance C were substituted with fractional ones to build the segments whereas the resistance R component is implemented in integer order. The value of G can be disregarded because of its negligible value, and the fact that its value, in this approach, will be compensated by the real part of the shunt impedance Y. By including these elements, i.e. the fractional, the impedance of the L and C of the interconnect will not be purely imaginary any more. Their impedance will be a real and imaginary part for both of them and proportional to α and β orders, respectively, to imitate the reality and have a more accurate model. In addition, these pa-

rameters will make it easier to optimise the model to fit different circumstances impacts.

The remainder of this chapter is organised as follows: Section (3.2) reviews some fundamental fractional definitions and properties and relevant works. Section (3.3) presents the generalising model of the interconnecting system. Then, the impact of inserting fractional elements are presented and discussed in section (3.4) while, the final Section (3.5) concludes the work.

3.2 BACKGROUND

The concept of the generalisation of integer-order of the integral and differential equations to the non-integer-order of integration and differentiation is a part of mathematics science named fractional calculus. Its continuous integro-differential operator ${}_aD_t{}^{\alpha}$ is defined as [149]

$$ {}_aD_t{}^{\alpha} = \begin{cases} \frac{d^{\alpha}}{dt^{\alpha}} & (\alpha) > 0, \\ 1 & (\alpha) = 0, \\ \int_a^t d(\tau)^{-\alpha} & (\alpha) < 0, \end{cases} \tag{3.1} $$

where a and t are the operation limits of calculation, i.e., the initial and the required time, and α is the operation order which is in general $\in \mathbb{R}$ but it could also be a complex number [143]. However, it did not gain adequate attention in the previous research due to its complexity compared to integer calculus and there was an absence of applications that it can be applied in [90].

3.2.1 *Basic definitions*

There may be as yet no confined definition of fractional operators, but there are two definitions implemented for the common fractional differ integral, namely; the Riemann-Liouville (R-L) definition and the Grunwald-Letnikov (G-L) definition [48]. The R-L is presented here:

$$ {}_aD_t{}^{\alpha} f(t) = \frac{1}{\Gamma(n-\alpha)} \frac{d^n}{dt^n} \int_a^t \frac{f(\tau)}{(t-\tau)^{\alpha-n+1}} d\tau \tag{3.2} $$

where $t > 0$, $(n-1 < \alpha < n)$, $\alpha \in \mathbb{R}^+$, n is an integer and $\Gamma(.)$ is the Gamma function, which is widely used in this domain, and is defined as [90]

$$\Gamma(z) = \int_0^\infty e^{-t} t^{z-1} dt \tag{3.3}$$

Gamma function is the generalisation of the factorial expression where it can be applied for positive real numbers.
On the other hand, the G-L definition is given here:

$${}_aD_t{}^\alpha f(t) = \lim_{h\to 0} h^\alpha \sum_{j=0}^{\left[\frac{t-\alpha}{h}\right]} (-1)^j \binom{\alpha}{j} f(t-jh) \tag{3.4}$$

where $\binom{\alpha}{j} = \frac{\Gamma(\alpha+1)}{\Gamma(j=1)\Gamma(\alpha-j+1)}$ represents the generalisation of Newton's binomial and $[\frac{t-\alpha}{h}]$ indicates that the integer part based on floor-function. Furthermore, the R-L fractional is a form of the Laplace transform method, which is usually used for solving engineering problems, has been derived [48] as follows:

$$\int_0^\infty {}_aD_t{}^\alpha f(t)dt = s^\alpha F(s) - \sum_{k=0}^{(n-1)} s^k {}_0D_t{}^{\alpha-k-1} f(t)\Big|_{t=0} \tag{3.5}$$

where s is the Laplace transform variable, which is equivalent to $j\omega$, for a limit $(n-1 < \alpha \leqslant n)$. With zero initial conditions, applying this to the fractional derivative of (3.2) yields $\mathcal{L}\,{}_aD_t{}^\alpha f(t) = s^\alpha F(s)$. Hence, this can be used to define a fractional general device which has an impedance proportional to s^α [118]. Accordingly, regular circuit elements resistor, capacitor and inductor can be considered special cases of this device when its fractional order is 0, -1 and 1, respectively.

3.2.2 *Basic properties*

Fractional calculus can be used to model high-order dynamics systems and complex nonlinear phenomena employing fewer coefficients. The arbitrary order, i.e., changed depending on the domain and boundary conditions, of the derivatives grants an additional degree of freedom to implement a particular behaviour [80]. Consequently, the fractional order derivative, unlike the integral order one, at a specific point of a function is not determined by an arbitrarily small neighbourhood of that point. This

property is valuable when considering a system with long-term memory.

This kind of derivatives and integrals has several main properties. First and foremost, the fractional derivative ${}_0D_t{}^{\alpha}f(t)$ is not just an analytical function of t but also of the fractional order α. Also, the identity operator of the operation ${}_0D_t{}^{\alpha}f(t)$ is fulfilled when $\alpha = 0$

$$ {}_0D_t{}^{0}f(t) = f(t) \tag{3.6}$$

While, if $\alpha = n$ and n is an integer, the operation ${}_0D_t{}^{\alpha}f(t)$ will give similar results as traditional differentiation of n. Besides this, the fractional order form shares the integer-order in potentially useful properties, such as a property of the linear operations:

$$ {}_0D_t{}^{\alpha}(af(t) + bg(t)) = a\,{}_0D_t{}^{\alpha}f(t) + b\,{}_0D_t{}^{\alpha}g(t) \tag{3.7}$$

and the semigroup property (the additive index law):

$$ {}_0D_t{}^{\alpha}\,{}_0D_t{}^{\beta}f(t) = {}_0D_t{}^{\beta}\,{}_0D_t{}^{\alpha}f(t) = {}_0D_t{}^{\beta+\alpha}f(t) \tag{3.8}$$

Not only that but also the fractional order derivative can be an exchange with the integer order derivative if β in (3.8) is assumed to be an integer.

It is obvious from the equations above that the non-local feature of this derivative function is comparable to the classical one. Yet, this derivative function with non-integer-order parameters, intuitively, the flexibilities in fine-tuning the gain and phase characteristics will be superior. For instance, [80] reported that a model of the 4th order can be approximated by a compact fractional order system with just a single term ($s^{0.5}$) and valid for a specific frequency range.

These flexibilities produce a fractional model that controls tuning variables which make it a robust model system with fewer controller parameters to adjust. Thus, utilising few tuning variables, the fractional system model delivers similar robustness to that which can be achieved by a highly complex system model.

Also, in order to accomplish analysis in the fractional domain, a number of useful functions have been found [149]. The Gamma function, which has been mentioned before, is one of these

functions. The value of $\Gamma(z) = 1$ and the basic property of this function is

$$\Gamma(z+1) = z\Gamma(z) \tag{3.9}$$

Another function is the Mittag-Leffler introduced by Humbert and Agarwal in 1953 [149]. It is a basic function in the fractional analysis, as the functions of exponential are in integer-order analysis, and defined by a series expansion

$$E_{(\alpha_1,\alpha_2)}(P) = \sum_{n=0}^{\infty} \frac{(P)^n}{\Gamma(n\alpha_1 + \alpha_2)} \tag{3.10}$$

which represents the Mittag-Leffler function for two parameters α_1 and α_2. The standard definition of this function, i.e., for one parameter, is

$$E_{(\alpha_1)}(P) = \sum_{n=0}^{\infty} \frac{(P)^n}{\Gamma(n\alpha_1 + 1)} \tag{3.11}$$

In fact, this function is simply the generalization of the exponential function [90].

3.2.3 *Relevant approaches*

There have been numerous studies dedicated to the fractional calculus subject across a variety of domains, such as bioengineering circuit theory, mechanical, chemistry and electromagnetic, whereby theoretical and experimental verification based on fractional calculus was introduced [142, 90].

These various studies and techniques have been presented in Sections (2.2.3.1) and (2.6.2). Those studies have been mentioned in Section (2.2.3.1) investigated the related case from a purely mathematical point of view, whilst those have been listed in Section (2.6.2) are more oriented toward the basics of interconnection.

What these previous studies attempt to achieve fundamentally is a general model that can cover most phenomena of the transmission line, which is part of our work objective. In this work, for the first time, we target the CMOS driving interconnect circuit design, using fractional order elements.

3.3 THE GENERALISING MODEL OF THE INTERCONNECTING SYSTEM

Under requirements of high frequencies and frequency-dependency effects in the interconnecting systems, it is increasingly imperative that the system's response is predicted accurately. This endorses this work for more general interconnect model design. The previous studies related to fractional order transmission line have not discussed CMOS driving interconnect circuit. The approach here is considering the transmission line scheme illustrated in Figure 2.12, where the integral elements of line inductance L and capacitance C are substituted with fractional ones to build the segments. The resistance R and conductance G components are implemented as integral-order. These two last elements (R and G) can also be fraction-order but this was not taken into account in this study.
Consequently, the connection between the line capacitance charge $q(t)$ and voltage, as well as the line inductance flux $\Phi(t)$ and current, has become more general to consider effects such as memory. The memory effect is the instantaneous change rate that depends on the past state [200].

Accordingly, these relationships of electromagnetic and the current-voltage characteristics of both the inductor and the capacitor have been modelled based on Riemann-Liouville derivative R-L, with $t > 0$ and $\alpha, \beta \in (0, 1]$

$$i(t) = {}_0D_t{}^{\beta} q(t) = C\frac{d^{\beta} v(t)}{dt^{\beta}} \tag{3.12}$$

$$v(t) = {}_0D_t{}^{\alpha} \Phi(t) = L\frac{d^{\alpha} i(t)}{dt^{\alpha}} \tag{3.13}$$

where β and α represent the fractional order derivative of the inductance and capacitance parameters, respectively. Similar fractional order constitutive equations (3.12) and (3.13), particularly the right-hand side, are used in modelling a non-integer capacitor and inductor [160, 159, 106, 186]. Note that fractional order models in (3.12) and (3.13) can describe elements with performance between a resistance, when $\alpha, \beta = 0$, and a reactance, when $\alpha, \beta \neq 1$.
Such an element in (3.13) can be considered as a series con-

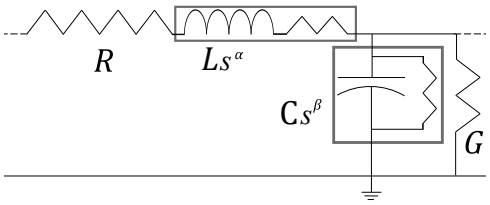


Figure 3.2: A transmission line segment with impedance and admittance of fractional order elements.

nection between a classical inductor with frequency-dependent inductance and a frequency-dependent resistor. Meanwhile, the element in (3.12) can be seen as a parallel connection between a frequency-dependent capacitor and a frequency-dependent resistor. Figure 3.2 shows the influence of implementing fractional elements on the shunt admittance and the series impedance of the transmission line segments. Eventually, these fractional parameters indicate the frequency-dependent loss, where part of the stored energy in a particular device transfers into lost energy. This is one of the main advantages of using such elements over the integer-order elements.

In addition, with the broad similarities in the properties between fractional and integer calculus, the new TL model can be analysed in a similar manner as the integer TL. Thus, the non-integer model will not add further complexity for the analysis, yet adds more flexibility for adjusting and controlling the model.

Recall equations (2.48) and (2.49), and after using the fractional Laplace transform, the transmission line equations will be

$$\frac{-dV(z)}{dx} = (R + s^{\alpha}L)I(z) \tag{3.14}$$

$$\frac{-dI(z)}{dx} = (G + s^{\beta}C)V(z) \tag{3.15}$$

Then, by setting $R = G = 0$ (lossless line) and derivative (3.14) and (3.15) with respect to z, we have

$$\frac{d^2V(z)}{dz^2} = (s^{\alpha+\beta}LC)V(z) \tag{3.16}$$

$$\frac{d^2I(z)}{dz^2} = (s^{\alpha+\beta}LC)I(z) \tag{3.17}$$

Hence, the equations (2.50) and (2.51) can now be reconsidered. In this case of the lossless line, the propagation constant of the line will be $\gamma = \sqrt{s^{\alpha+\beta}LC}$. This expression can be rearranged in terms of the attenuation constant (a_r) and the phase constant (b_i) in a real and imaginary form ($a_r + jb_i$). This yields

$$\gamma = \sqrt{LC}\omega^{(\alpha+\beta)/2}\cos\frac{(\alpha+\beta)\pi}{4} + j\sqrt{LC}\omega^{(\alpha+\beta)/2}\sin\frac{(\alpha+\beta)\pi}{4} \tag{3.18}$$

In (3.18), when $\alpha+\beta \in (0,2)$, both the real and imaginary parts of γ are greater than zero. Although the assumption relates to lossless, it confirms the decaying effect when a wave propagates through a media. On the other hand, when $\alpha+\beta = 2$ as in the integer case, the attenuation constant becomes zero and there is no energy loss accordingly. What is more, it can notice that the frequency dependency of the fractional order is non-linear. Not only that but the phase velocity (u) will also be affected, as it is well known that its value is the proportionality between the angular frequency and the phase constant $\frac{\omega}{b_i}$. By implementing the definition of the phase velocity and using the imaginary part of (3.18), we obtain the following

$$u = \frac{1}{\sqrt{LC}\omega^{\frac{(\alpha+\beta)}{2}-1}\sin\frac{(\alpha+\beta)\pi}{4}} \tag{3.19}$$

As such, one can observe the dispersion effect of the propagation in lossy media. While in the integer order when α and β equal 1, the expression (3.19) becomes $\frac{1}{\sqrt{LC}}$, i.e., frequency-independent.

Similarly, the characteristic impedance (Z_0) can be given as $\sqrt{s^{\alpha-\beta}L/C}$. Based on this assumption, Z_0 is not frequency-independent as in conventional case, and can be represented as

$$Z_0 = \sqrt{\frac{L}{C}}\omega^{(\alpha-\beta)/2}\cos\frac{(\alpha-\beta)\pi}{4} + j\sqrt{\frac{L}{C}}\omega^{(\alpha-\beta)/2}\sin\frac{(\alpha-\beta)\pi}{4} \tag{3.20}$$

Comparing to the non-fractional model, where Z_0 is simply $\sqrt{\frac{L}{C}}$, it can be observed in (3.20) that Z_0 has an imaginary part, which accounts for the dispersion effects. This is in addition to its resistive element which is represented in the real part as the quantity $\cos\frac{(\alpha-\beta)\pi}{4}$ is always non-zero.

3.3.1 *Procedure of TL parameters extraction*

Now, it may be very timely to be aware of determining the fractional parameters α and β based on practical measurements. In order to achieve that, Z_0 and γ are considered at two different frequencies ω_1 and ω_2 that are relevant. That means that choosing different frequency ranges will give different α and β from experiments. Then, based on (3.18) and (3.20), α and β can be evaluated

$$\begin{aligned} \alpha + \beta &= 2\log_{(\omega_1/\omega_2)} \left| \frac{\gamma(\omega_1)}{\gamma(\omega_2)} \right| \\ \alpha - \beta &= 2\log_{(\omega_1/\omega_2)} \left| \frac{Z_0(\omega_1)}{Z_0(\omega_2)} \right| \end{aligned} \tag{3.21}$$

where $\gamma(\omega_1)$, $\gamma(\omega_2)$, $Z_0(\omega_1)$ and $Z_0(\omega_2)$ are the propagation constants and the characteristic impedances at frequencies ω_1 and ω_2, respectively. Expression (3.21) shows that modelling the fractional parameters incorporates the transmission line losses related to the frequency.
Afterwards, the impedance and propagation constant of a transmission line can be calculated from the obtained measurement using a Vector Network Analyzer. The data obtained for the S-parameters is firstly converted into the ABCD-parameters as [70]

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{A+B/Z_0-CZ_0-D}{A+B/Z_0+CZ_0+D} & \frac{2(AD-BC)}{A+B/Z_0+CZ_0+D} \\ \frac{2}{A+B/Z_0+CZ_0+D} & \frac{-A+B/Z_0-CZ_0+D}{A+B/Z_0+CZ_0+D} \end{bmatrix} \tag{3.22}$$

where

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma z) & Z_0 \sinh(\gamma z) \\ \frac{1}{Z_0}\sinh(\gamma z) & \cosh(\gamma z) \end{bmatrix} \tag{3.23}$$

where the right-hand side of (3.23) is a uniform transmission line with length z. Secondly, the de-embedding equations for characterization the IC interconnect are used to calculate Z_0 and γ, which is given by [62]

$$Z_0^2 = Z_L^2 \frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2} \tag{3.24}$$

and

$$e^{j\gamma z} = \frac{1 - S_{11}^2 + S_{21}^2 + \sqrt{(1 + S_{11}^2 - S_{21}^2)^2 - (2S_{11})^2}}{2S_{21}} \tag{3.25}$$

where Z_L is the load impedance of the system under the test. After obtaining Z_0 and γ, the next step is to obtain the TL parameters, which can be calculated easily using the related expressions. Note that following this procedure is not applicable for extracting only the fractional parameters but also other parameters, i.e., R, L, G and C. Since, a similar procedure has been used to calculate the TL parameters from the measured S-parameters [215]. However, there are differences to the procedure here.
One of these differences is that the current procedure needs measurements at no less than two different frequencies. The other one is that, after calculating Z_0 and γ, the step of the calculation of the TL parameters starts by evaluating fractional parameters using (3.21). This is to guarantee incorporating their effect, then the parameters of L and C can be obtained using (3.20) and (3.18). The values of R and G can be calculated using the regular procedure, i.e., using (2.50) and (2.51).

3.3.2 *Characteristic impedance and complex propagation constant in fractional domain*

The model shown in Figure 3.2 represents the transmission line with fractional elements for inductance and capacitance of the interconnection. However, the value of G can be disregarded owing to its negligible value since the leakage between conductors is considerably small. Simultaneously, its value will be compensated by the real part of the shunt admittance Y of the fractional order capacitor. Hence,

$$Y(\omega) = \omega^{\beta} C e^{\frac{j\beta\pi}{2}} = \omega^{\beta} C \left[\cos\frac{\beta\pi}{2} + j\sin\frac{\beta\pi}{2}\right] \tag{3.26}$$

assuming $s = j\omega$. While in the case of a non-fractional order capacitor, the value of β equals one, the real part of (3.26) will be cancelled since $\cos\frac{\pi}{2} = 0$. On the other hand, the value of R was taken into account in the series impedance Z besides L, because of its crucial value, particularly for a long interconnection where the resistance is considerable.

As such, the characteristic impedance $Z_0 = \sqrt{\frac{Z}{Y}}$ for the system is

$$Z_0 = s^{\frac{(\alpha-\beta)}{2}} \sqrt{\frac{L}{C}} \sqrt{1 + \frac{R}{s^{\alpha} L}} \tag{3.27}$$

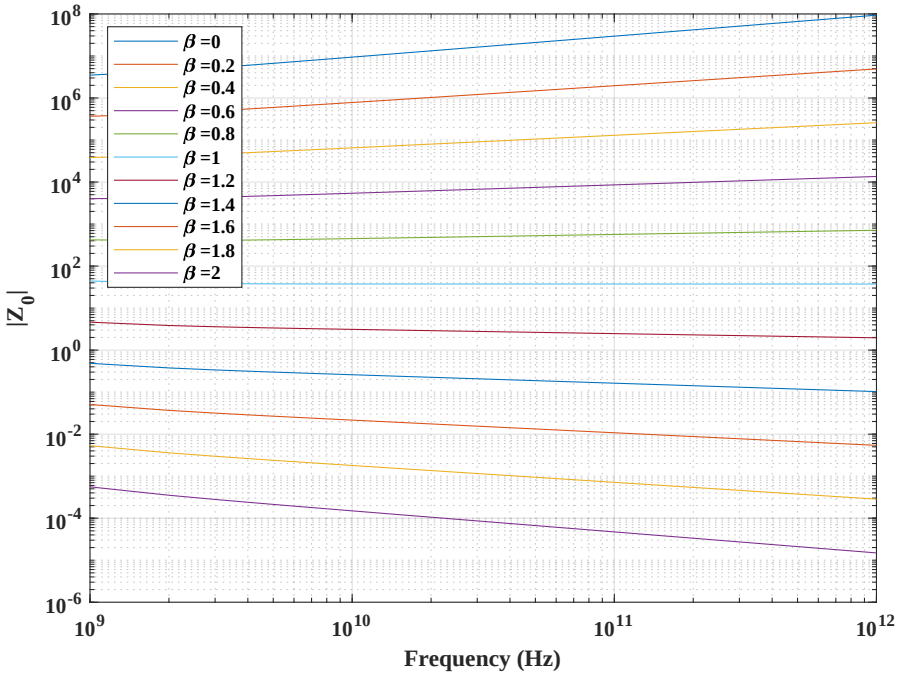
Note that Z_0 depends on lossless impedance $\sqrt{\frac{L}{C}}$ and is non-linearly proportional to the frequency, represented by the frequency variable s. This non-linearity relationship is due to the parameters of α and β. Here, the complex propagation constant of the system $\gamma = \sqrt{ZY}$ is:

$$\gamma = s^{\frac{(\alpha+\beta)}{2}} \sqrt{LC} \sqrt{1 + \frac{R}{s^{\alpha} L}} \tag{3.28}$$

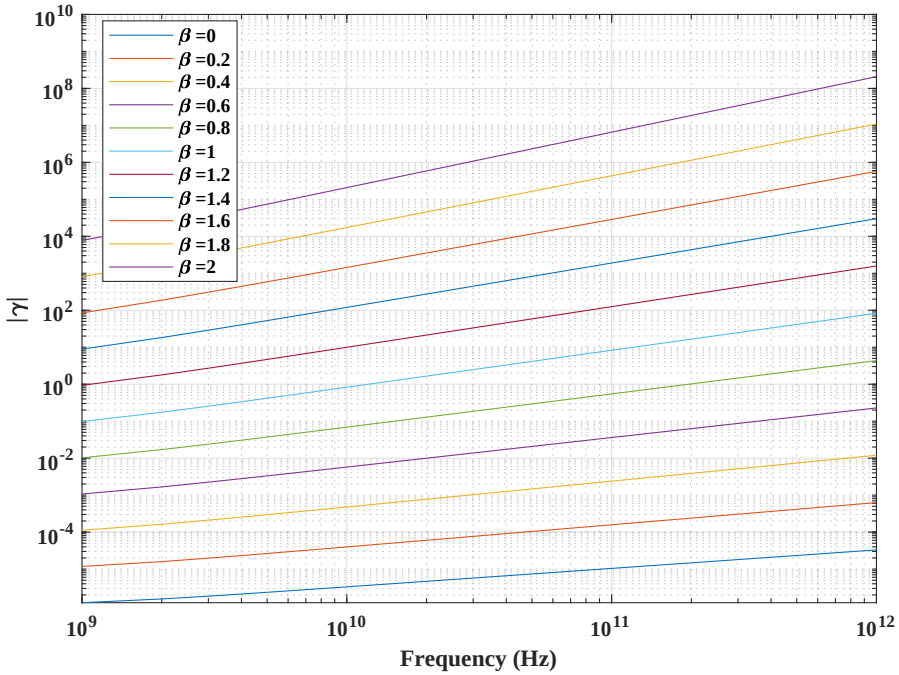
It can be noted that γ is proportional to the frequency and depends on the propagation constant of a loss-less line. Therefore, not only attenuation occurs but also distortion may occur depending on the values of the fractional parameters.

Hence, for investigating this interplay, RLC interconnect of a copper interconnecting material have been considered; the parameters are L=0.246pH, R=1.5mΩ and C=0.176fF, and all of which are in per micrometre length. The calculations of Z_0 and γ magnitudes in (3.27) and (3.28) were implemented for an interconnect length 2mm with a frequency range from 1GHz to 1THz, as shown in Figures 3.3 and 3.4. Then, the results included the calculations to the phase of Z_0 and γ in (3.27) and (3.28) are shown in Figures 3.5 and 3.6.

Figure 3.3 shows the magnitude of Z_0 and γ changing with a range of frequencies when the value of β is varied from 0 to 2 and α value is fixed at 1, which is the value when it is not a fractional order. It can be noted that the dependence of Z_0 on the frequency and the added parameter β is even more significant. It can be seen that the magnitude of Z_0 changes from ascending, in the case of $\beta < \alpha$, to descending with increasing frequency, in the case of $\beta \geqslant \alpha$. In other words, as the value of β changes, the related element, i.e., the fractional order capacitor, effect changes from purely resistive to purely capacitive. This has a substantial effect on the absolute value of γ. Whereby, with increasing the value of β, there is a steadily increase of the γ magnitude in relation to the frequency.

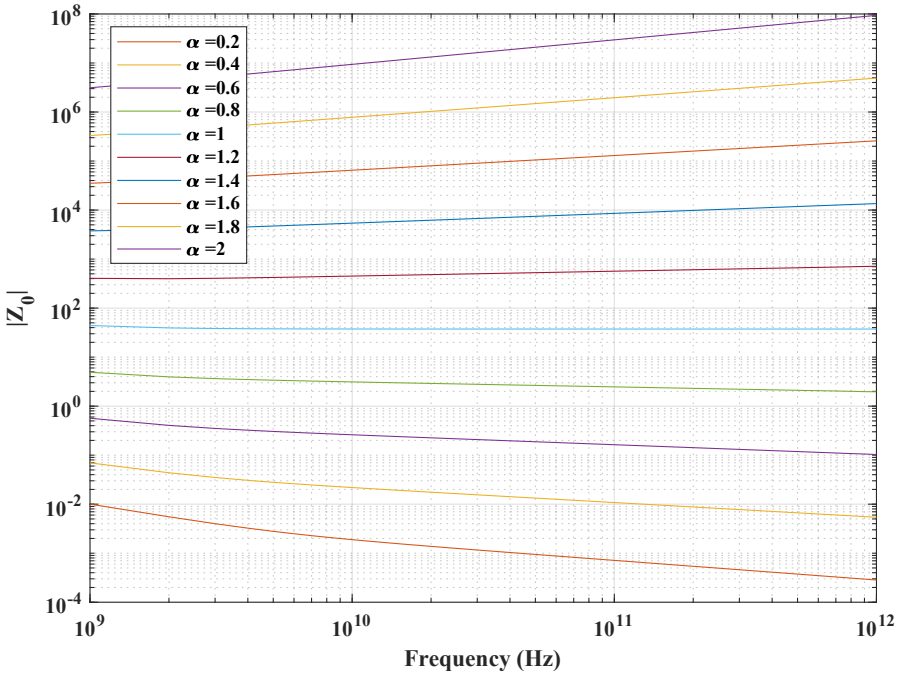


(a)



(b)

Figure 3.3: The magnitude of Z_0 and γ with respect to frequency at $\alpha = 1$ and $\beta = 0 : 2$.



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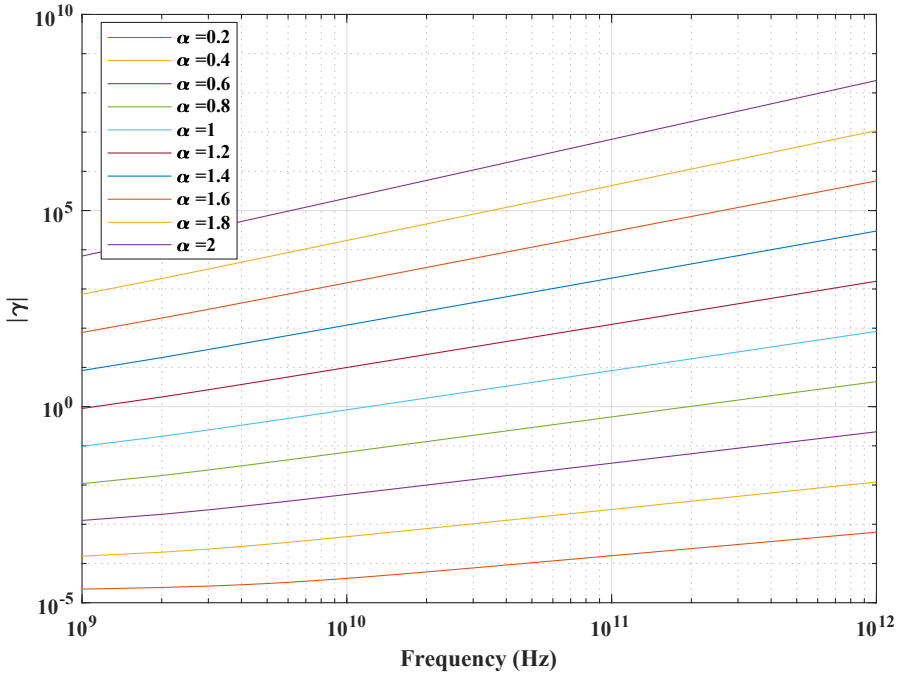


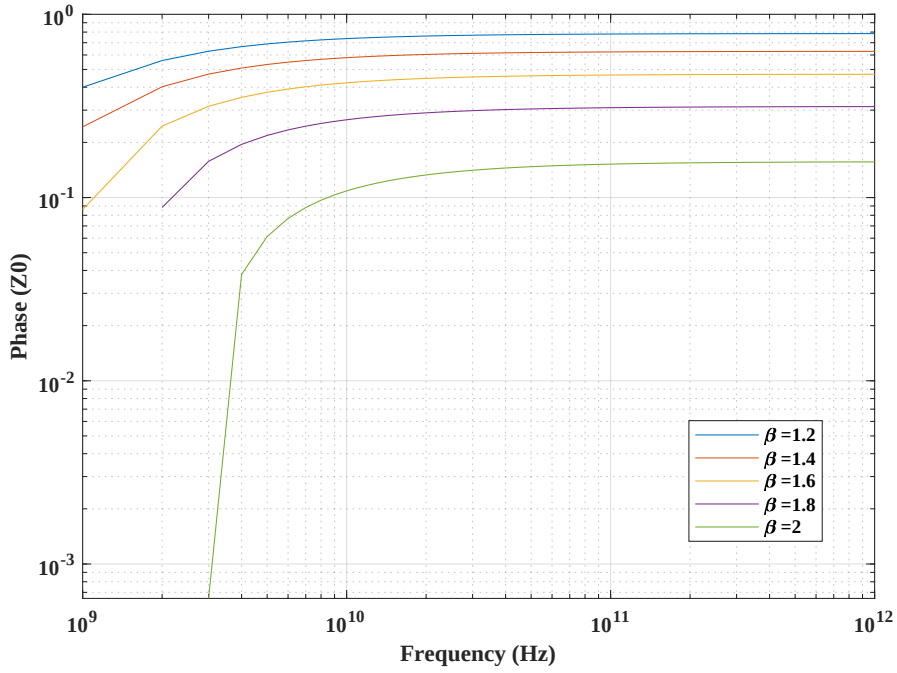
(b)

Figure 3.4: The magnitude of Z_0 and γ with respect to frequency at $\alpha = 0:2$ and $\beta = 1$.

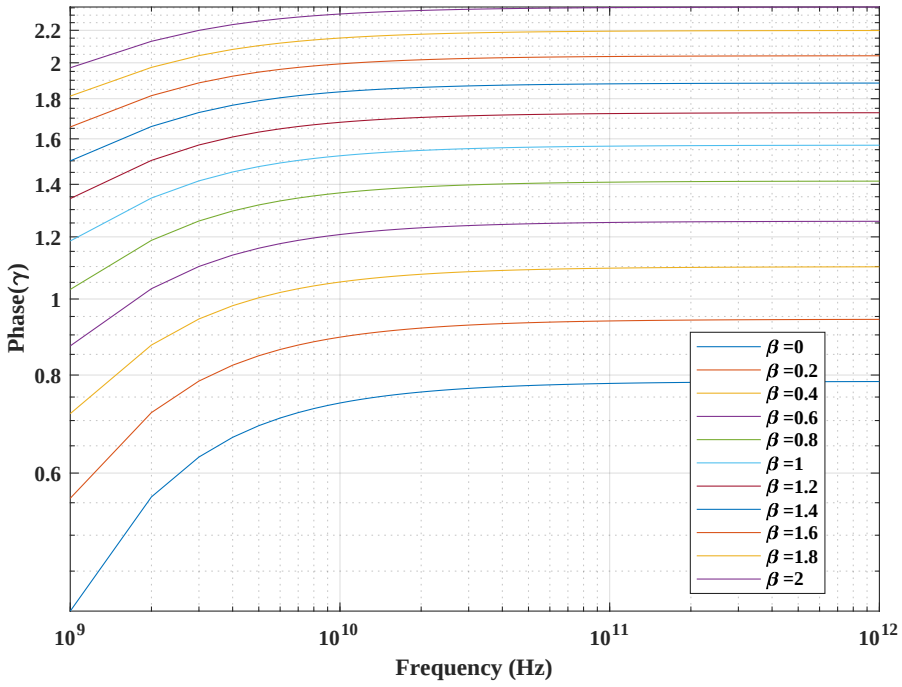
Then, the effect of changing α from 0 to 2 has been tested on the transmission line impedance and propagation constant as shown in Figure 3.4, while the value of β has been set to 1. The figure illustrates a considerable influence of the generalisation parameter α on the interconnecting system. It is notable that its influence on the value of γ has a similar effect to that of the added parameter β.
On the other hand, the impedance magnitude of the TL proportion to frequency significantly increases when the α value goes up. However, this proportion between the Z_0 magnitude and the frequency changes in a manner opposite to the effect of the previous parameter β. Here, the change is from declining of the Z_0, when $\alpha \leqslant \beta$, to rise with the frequency increasing, in the case of $\alpha > \beta$. This is due to the association of this parameter to the fractional order inductance of the line.
In other words, Figures 3.3 and (3.4) demonstrate the area at which the TL behaviour is whether being inductive or capacitive, decreasing or increasing as a function of frequency for different values of the model parameters α and β.

Moreover, comparing the effect of α to the β effect, the β has the bigger effect on the relation between the frequency and Z_0 which is clear by observing the two Figures 3.3 and 3.4. This occurs because the inductance element has a small value and normally its effect against a considerably large value of resistance is to some extent compensated. Furthermore, there is a similarity between the two parameters' effects on the propagation constant γ of the transmission line.

At the same time, the phases of the complex propagation constant and the characteristic impedance have been affected due to adding these parameters. Figures 3.5 and 3.6 show this impact on changing the phase response of the Z_0 and γ to the frequency. These figures illustrate the phase value of the Z_0 turns from positive to negative when the value of β goes higher and vice versa for the value of α. Thus, the parameters of the fractional order, α and β, control the phase angle which is independent of the operation frequencies. There is an alikeness between the impact of these two fractional parameters on γ. Nevertheless, Figure 3.6 demonstrates how the relation of Z_0 and γ to the frequency is changed to the dependency just after being $\alpha > 0$.

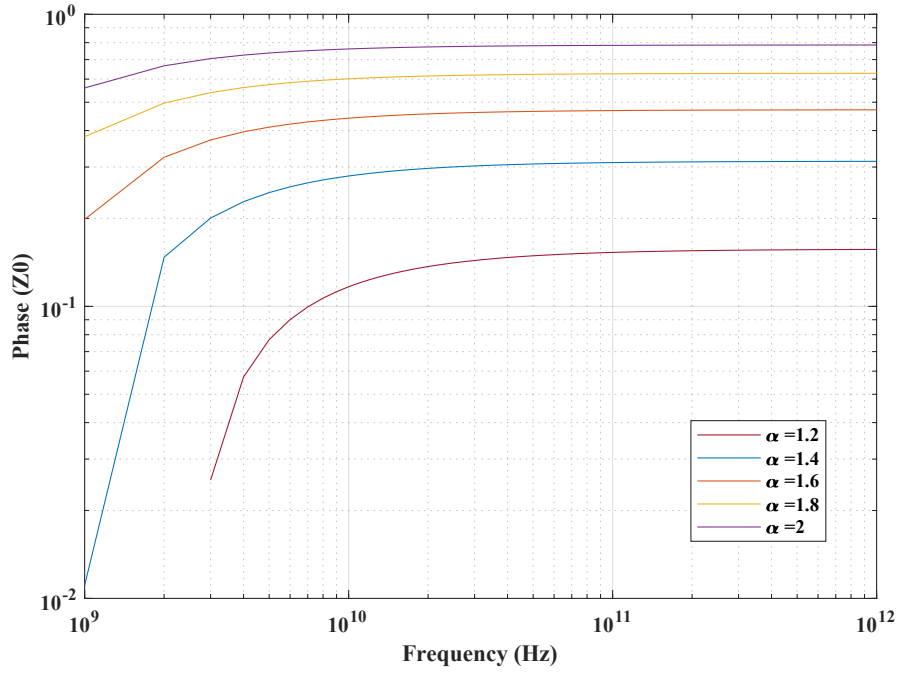


(a)

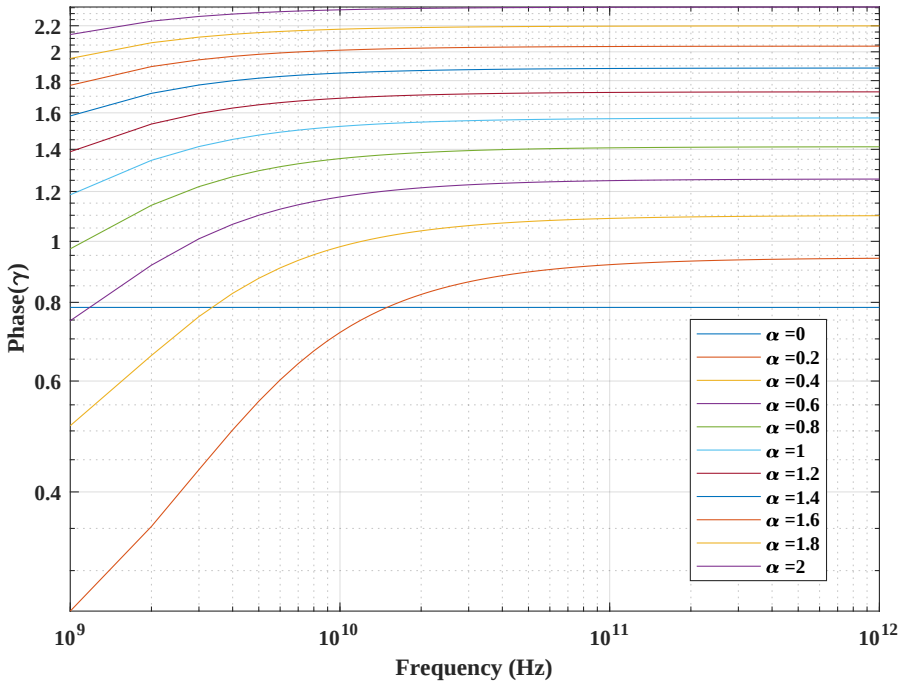


(b)

Figure 3.5: The phase angles of Z_0 and γ, in radians, with respect to frequency at $\alpha = 1$ and $\beta = 0 : 2$



(a)



(b)

Figure 3.6: The phase angles of Z_0 and γ, in radians, with respect to frequency at $\alpha = 0 : 2$ and $\beta = 1$.

Hence, the last term in both (3.27) and (3.28) contributes as part of this dependency.

In general, the propagation constant and characteristic impedance depend on the added fractional order parameters and the frequency. With the ability to have different values around the conventional case ($\alpha+\beta=2$) and ($\alpha-\beta=0$), it gives more general behaviour. This increases the degrees of the design freedom by adjusting the new parameters and, hence, generalising the model of the system.

3.3.3 TL *transfer function with fractional elements*

Here, it has been resort to a two-port network of the transmission line with two ports, i.e., driver and receiver by which the port variables are connected to the chain parameters. Then, it is not difficult after some rearrangements to conclude a formula that relates the signals at the far distance z to those at the line starting point $V(0)$ and $I(0)$. Such a formula had been already found [148] but with integer order elements. This is based on the general form solution of (3.16) and (3.17), as

$$V(z) = Va e^{\gamma z} + Vb e^{-\gamma z} \tag{3.29}$$

$$I(z) = Ia e^{\gamma z} + Ib e^{-\gamma z} \tag{3.30}$$

where Va, Ia, Vb and Ib are variables of reflected and incident travelling waves on a line. These waves are not independent of each other. Substituting these current and voltage components in (3.14) and (3.15), where $\frac{dV(z)}{dz} = ZI(z)$, to eliminate Ia and Ib. Based on this, (3.29) and (3.30) can be expressed respectively as

$$V(z) = Va e^{\gamma z} + Vb e^{-\gamma z} \tag{3.31}$$

$$I(z) = \frac{-Va}{Z_0} e^{\gamma z} + \frac{Vb}{Z_0} e^{-\gamma z} \tag{3.32}$$

To find Va and Vb, we set $z = 0$, thus the above equations reduce to

$$V(z) = V(0)\cosh(\gamma z) - Z_0 I(0)\sinh(\gamma z) \tag{3.33}$$

$$I(z) = \frac{-V(0)}{Z_0}\sinh(\gamma z) + I(0)\cosh(\gamma z) \tag{3.34}$$

The expression that relates the signals at the end and those at the starting point is

$$\begin{bmatrix} V(0) \\ I(0) \end{bmatrix} = \begin{bmatrix} \cosh(\gamma z) & Z_0\sinh(\gamma z) \\ \frac{1}{Z_0}\sinh(\gamma z) & \cosh(\gamma z) \end{bmatrix} \begin{bmatrix} V(z) \\ I(z) \end{bmatrix} \tag{3.35}$$

Subsequently, the transfer function of the structure shown in Figure 3.2 is given by

$$H(s) = \frac{V(z)}{V(0)} = \frac{1}{\cosh(\gamma z) + \frac{1}{Z_0}\sinh(\gamma z)} \tag{3.36}$$

It is evident that this system response is based on the corresponding characteristic impedance and propagation delay which depend on the square root of the frequency variable and, thus, the generalisation parameters α and β.
In the case of adding a driver and a load to the system transient response as shown in Figure 3.7, three cascaded two-port networks can be utilised to represent the overall system [132]. Hence,

$$\begin{bmatrix} V(0) \\ I(0) \end{bmatrix} = \begin{bmatrix} 1 & Z_s \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cosh(\gamma z) & Z_0\sinh(\gamma z) \\ \frac{1}{Z_0}\sinh(\gamma z) & \cosh(\gamma z) \end{bmatrix} \begin{bmatrix} 1 & Z_L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V(z) \\ I(z) \end{bmatrix} \tag{3.37}$$

where $Z_s = R_t$ the driver resistance and $Z_L = \frac{1}{sC_t}$.

3.3.4 *Modelling the system transfer function*

On top of that, the equivalent elementary model of the completed interconnect structure, which has been studied here, is depicted in Figure 3.7. This includes the driver source, capacitive load and the distributed RLC line with L and C fractional elements and their orders are α and β, respectively. This combination can

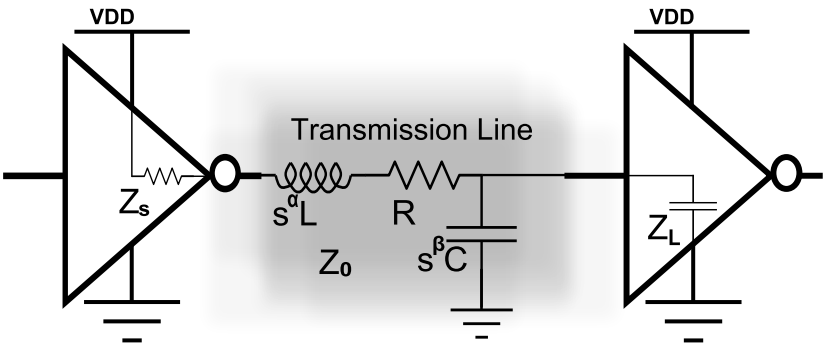


Figure 3.7: The model of a CMOS inverter driving a fractional distributed RLC load.

be considered as a linear time-invariant (LTI) system. The transfer function demonstrating this structure can be given based on (3.37) as follows:

$$H(s) = \frac{1}{(1+\frac{Z_s}{Z_L})\cosh\gamma z + (\frac{R_t}{Z_0}+\frac{Z_0}{Z_L})\sinh\gamma z} \tag{3.38}$$

The inverse Laplace transform of this (3.38) would be very challenging because of the sine hyperbolic and cosine hyperbolic functions in the denominator and the fractional order term in frequency, s^{α} and s^{β}. Therefore, to obtain the poles of $H(s)$, the transfer function is stretched to an infinite power series, i.e., after applying the expansion for the $\cosh(\gamma x)$ and $\sinh(\gamma x)$, whose series expansion can be easily obtained. This yields

$$\begin{aligned} H(s) = \frac{1}{(1+R_tC_ts)\{1+\frac{(x\gamma)^2}{2!}+..\}+(\frac{R_t}{\sqrt{\frac{L}{C}}\sqrt{1+\frac{R}{s^{\alpha}L}}s^{\frac{(\alpha-\beta)}{2}}} \\ +C_t\sqrt{\frac{L}{C}}\sqrt{1+\frac{R}{(s^{\alpha}L)}}s^{\frac{(\alpha-\beta+2)}{2}})\{x\gamma+\frac{(x\gamma)^3}{3!}+..\}} \end{aligned} \tag{3.39}$$

As a result of this, it can be seen that a fractional order LTI system has infinite roots with infinite-dimensional. In other words, using fractional order elements in modelling the LTI system makes it more realistic, i.e., the system becomes more comprehensive of its behaviours in the reality. Hence, it can be said that integer order is a special case of this system. However, to simplify the study of the obtained system, the analysis will be approximated to the second-order components. Also, it can be assumed without loss of generality, that the simplification can reduce fractional order to one dimension [149] of ν, which is called weight in this

work, rather than α and β. As a result of this approximation to achieve a finite transfer function, a fractional order rational function will be obtained.

3.3.4.1 *Second Order Complexity*

The expression (3.39) can be approximated to

$$H_{approx}(s) = \frac{1}{1 + (R_tC_t + RC_t)s + (R_tC + \frac{RC}{2})s^{\beta} + (\frac{R_tC_tRC}{2} + \frac{C_tCR^2}{6})s^{\beta+1} + (\frac{R_tRC^2}{6})s^{2\beta} + (C_tL)s^{\alpha+1} + \frac{LC}{2}s^{\beta+\alpha}} \tag{3.40}$$

The approximation has been done here depending on the first two dominant poles of the exact transfer function and by gathering the first and second order coefficient factors of the polynomial in the denominator, where the coefficients are $g_1 = R_tC_t + RC_t + R_tC + \frac{RC}{2}$ and $g_2 = \frac{R_tC_tRC}{2} + \frac{C_tCR^2}{6} + \frac{R_tRC^2}{6} + C_tL + \frac{LC}{2}$ and the third one is found to be significantly less than the first two coefficients. This means that the approximation will be to somewhat accurate if the global waveform can be introduced. In addition, for a LTI system, the approximation of a model can be to some extent accurate, as long as the chosen poles can emulate the initial effect of the whole poles, such as the first peak of the resonance frequency of the exact model. Moreover, to simplify the analysis in terms of fractional orders, assume the fractional orders of the extended form of (3.39) are dependent on the real value ν where $i\alpha = i\nu$, $j\beta = j\nu$, $i = (1, 2, 3, ..)$ and $j = (1, 2, 3, ..)$.

3.3.4.2 *Delay Modelling*

Now, let us consider $H(s)$ a proper rational function in the complex variable s^{ν}, without loss of generality of the equation, after taking into account that ν is a function of the complex variables β and α [133]. That produces a single fractional order polynomial with roots a_k, where $(k = 1, 2, 3, ..)$, as follows

$$H(s) = \sum_{k=0}^{\infty} \{\frac{b_k}{s^{\nu} - a_k}\} \tag{3.41}$$

The analytic solution for the system can be found, from (3.41), and a new definition for the interconnect system obtained as follows

$$h(t) = \sum_{k=0}^{\infty} b_k t^{\nu-1} E_{(\nu)}(a_k t^{\nu}) \tag{3.42}$$

Thus, after approximating the solution to two poles we will have:

$$\frac{V(t)}{V_{DD}} = (1 - \frac{a_1 t^{\nu-1} e^{a_1 t^{\nu}}}{(a_2 - a_1)\Gamma(\nu+1)} + \frac{a_2 t^{\nu-1} e^{a_2 t^{\nu}}}{(a_2 - a_1)\Gamma(2\nu+1)})/a_1 a_2 \tag{3.43}$$

where $a_1, a_2 = \frac{-g_1 \pm \sqrt{g_1^2 - 4g_2}}{2g_2}$, whereas g_1 and g_2 are the second and third coefficients of the approximated transfer function, respectively. The expression of (3.43) is the general expression for RLC interconnect network model in CMOS technology based on a second order approximate transfer function. It is important to note here that the definition of (3.43) is dependent on the fractional order ν. Hence, the effect of the generalising parameter on the system timing is included in the case of using the formulae of (3.43). In addition, by making $\nu = 1$, the formula of (3.43) becomes comparable with the formula applied by [109] and [196]. In addition, (3.43) leads to a new definition for the delay $t_{0.5}$ which is obtained as follows

$$t_{0.5} = \sqrt[\nu]{\frac{1}{a_2} \ln \left[\frac{(a_2 - a_1)}{a_1} \Gamma(\nu+1)[1 - a_1 a_2 (\frac{V(t_{0.5})}{V_{DD}})] \right]} \tag{3.44}$$

This is after rearrangements and approximation by reducing the third term in (3.43). This is based on the fact that a_1 is smaller than a_2, which means the third term of the time domain response decreases rapidly compared to the second one.

3.3.4.3 *Simple fractional interconnect model*

Furthermore, the general closed form of a CMOS inverter propagation delay has been introduced in this work. Figure 3.7 can be assumed as an equivalent circuit of a CMOS inverter driving an RLC load by ignoring the driver/source resistance and capac-

itance, then assuming a fast ramp signal as input voltage, we get

$$V_{in}(t) = \frac{t}{\tau_r} V_{DD}, 0 < t \leqslant \tau_r \tag{3.45}$$

where τ_r is the rise time of the input signal and for the CMOS current we have used Sakurai model [174], because of its accuracy in the linear and saturation region. This produces

$$I_{Dsat} = \frac{W}{L_{eff}} B(V_{GS} - V_{th})^{\delta} \tag{3.46}$$

As soon as V_{in} starts to reach the V_{th}, i.e., $\tau_n \geqslant t$ the NMOS will start to turn on to obtain the following equation after applying the KVL and KCL to obtain the voltage at the end of the RLC circuit $V_1(t)$

$$V_1(t) = L\frac{d^{\alpha}}{dt^{\alpha}} I_D + RI_D + V_0(t) \tag{3.47}$$

but, $\frac{d^{\beta}}{dt^{\beta}} V_1(t) = -\frac{I_D}{C}$ where the voltage applied to lump circuit V_0 will be

$$V_0(t) = V_{DD} - V_C(t) - V_R(t) - V_L(t) \tag{3.48}$$

where

$$\begin{aligned} V_C(t) =& \frac{B_n \tau_r \Gamma(\delta+1)\Gamma(\beta+1)}{CV_{DD}\Gamma(\delta+\beta+1)} \left(\frac{tV_{DD}}{\tau_r - V_t h}\right)^{\delta+\beta} \\ \approx& \frac{B_n \tau_r}{CV_{DD}(\delta+\beta)} \left(\frac{tV_{DD}}{\tau_r} - V_{th}\right)^{\delta+\beta} \end{aligned} \tag{3.49}$$

$$V_R(t) = RB_n \left(\frac{tV_{DD}}{\tau_r} - V_{th}\right)^{\delta} \tag{3.50}$$

$$V_L(t) = \frac{LB_n V_{DD}\Gamma(\delta+1)}{\tau_r \Gamma(\delta+1-\alpha)} \left(\frac{tV_{DD}}{\tau_r} - V_{th}\right)^{\delta-\alpha} \tag{3.51}$$

Then, $\tau_n < t \leqslant \tau_r$, where τ_n the time needed to reach thermal voltage. The NMOS will carry on to be in saturation region, to have the following:

$$\begin{aligned} V_0(t) =& V_{DD} - \frac{B_n \tau_r (V_{DD} - V_{th})^{(\delta+\beta)}}{C V_{DD}(\delta+\beta)} - R B_n (V_{DD} - V_{th})^{\delta} \\ & - \frac{L B_n V_{DD} \Gamma(\delta+1)}{\tau_r \Gamma(\delta+1-\alpha)} (V_{DD} - V_{th})^{\delta-\alpha} \end{aligned} \tag{3.52}$$

The same equation can be applied when $\tau_r < t \leqslant \tau_{nsat}$, where τ_{nsat} is the time when the NMOS transistor leaves the saturation region. Subsequently, when $t > \tau_{nsat}$, the NMOS inters the linear region and behaves as a conductance ρ_n. Therefore, the time delay $t_{P0.5}$ will be approximated as

$$t_{P0.5} = \left(\frac{2\ln(\frac{V_{nsat}}{0.5 V_{DD} \Gamma(\nu+1)})}{\frac{1+R\rho_n}{L\rho_n} + \sqrt{(\frac{1+R\rho_n}{L\rho_n})^2 - \frac{4}{LC}}} \right)^{\frac{1}{\nu}} + \frac{\tau_r}{2} \tag{3.53}$$

Thus, the time delay can be expressed as a function of the various parameters as

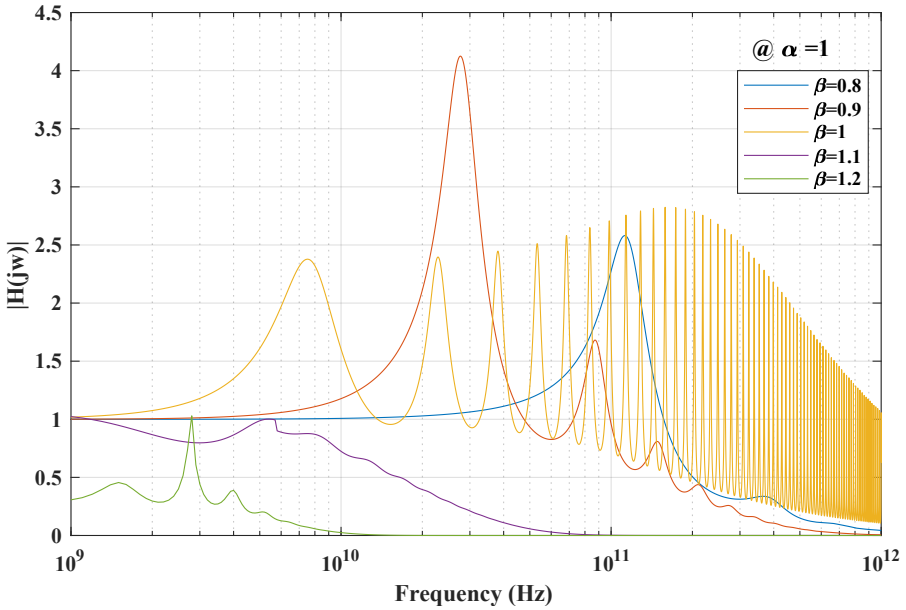
$$Delay = f(\tau_r, V_D D, R, L, C, \rho_n, \nu) \tag{3.54}$$

where ν is the generalising parameter. This expression (3.53) is in accordance with that reported in [193, 55, 177]. Yet, with a new parameter ν, it is easier to adjust the delay model for better accuracy.

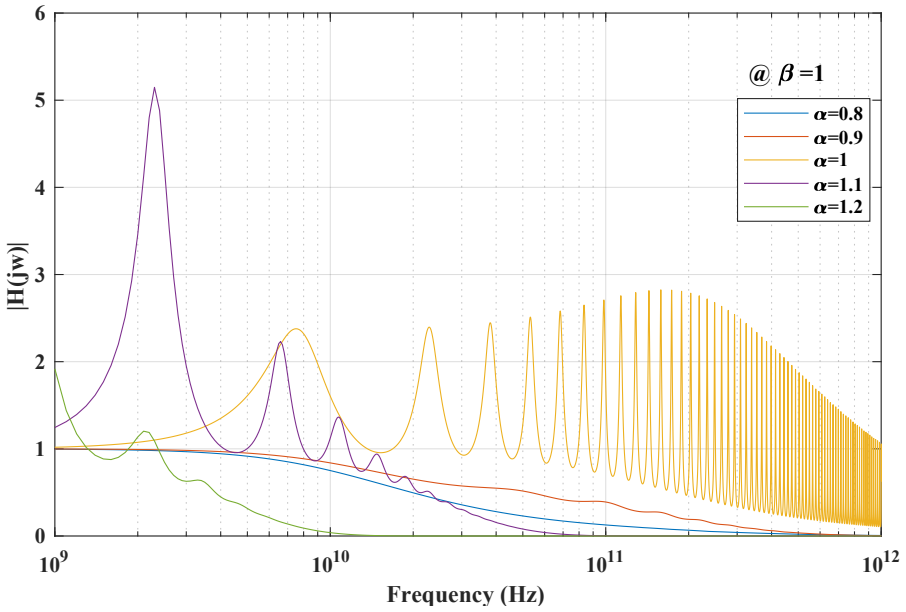
3.4 RESULTS AND DISCUSSION

3.4.1 *System simulation*

Since the main intention is to design a flexible interconnect model with general features, the response of the generalized time-fractional model of interconnect has been analysed. In Figure 3.9, the approximate transfer function response (3.40) is generated with various values of α and β. While Figure 3.8 represents the response of the exact transfer function (3.39) for the same values of α and β. For this investigation, the driver resistance (Z_s) and capacitance (Z_L) are 30Ω and 50fF, respectively, while the interconnect length is 2000μm and its parameters are considered as follows: R=8.829mΩ, C=0.18fF and L=1.538pH per

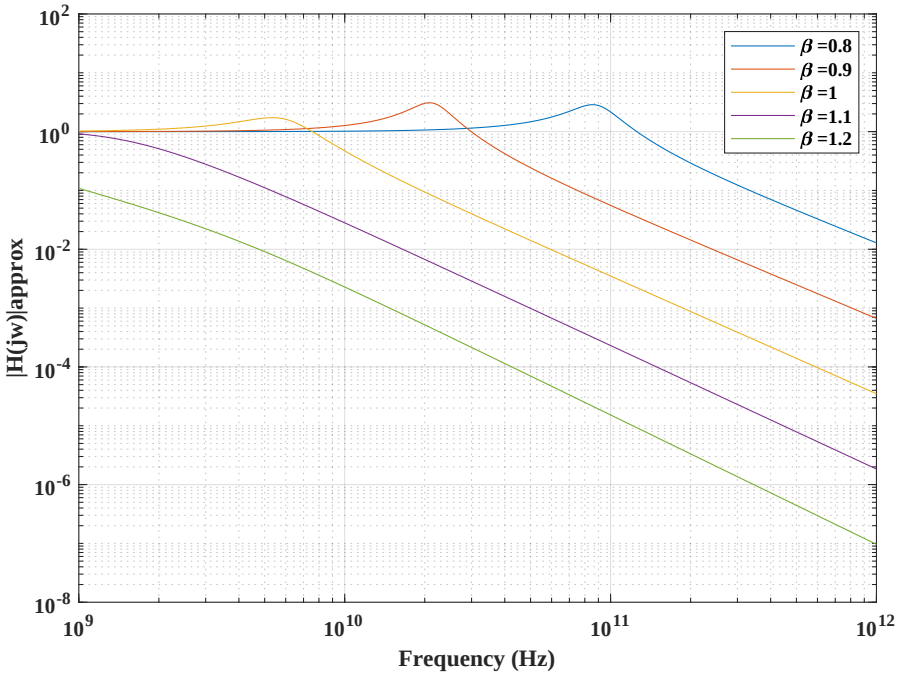


(a)

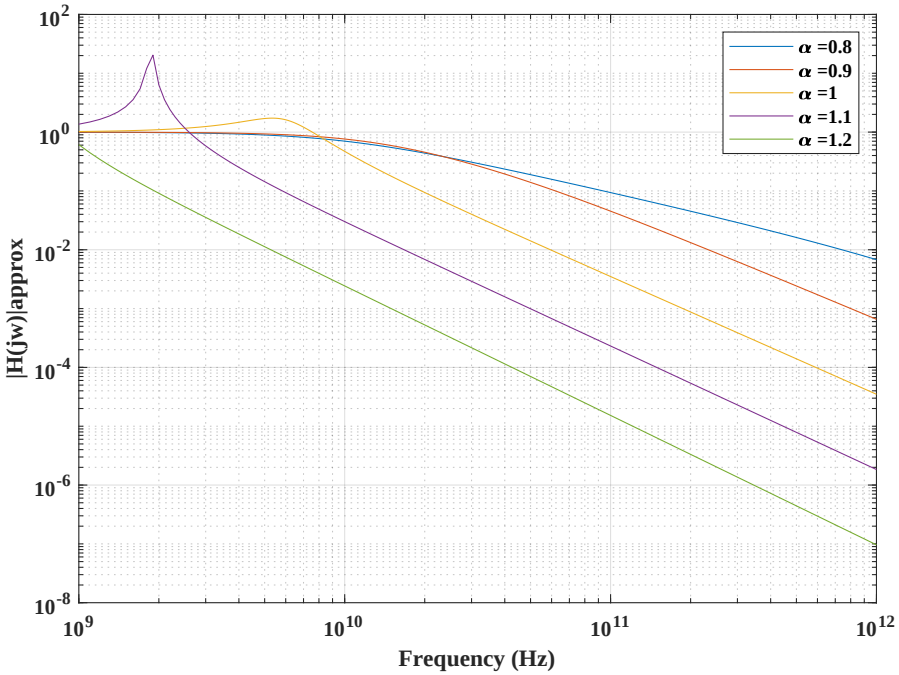


(b)

Figure 3.8: Exact transfer function (3.39) of interconnect with different values of α and β.



(a) With $\alpha = 1$.



(b) With $\beta = 1$.

Figure 3.9: The fractional approximate transfer function (3.40) of an RLC interconnect with different values of α and β.

μm length.
In Figure 3.8, frequency response distributions of the proposed model formula are shown, for the exact case (3.39) with different values of generalising parameters. Figure 3.8 highlights important regions of system behaviour for a set of the modelling parameters. It reveals the stability region for particular values of those parameters, and where the frequency oscillation might be happening for different values of the same parameters. This has been demonstrated by changing β and α not the circuit components. Hence, this undoubtedly brings to the design more flexibility and robustness. The approximate transfer function response, shown in Figure 3.9, records similarity, for a range of α and β, to the exact transfer function response values, it also marks the main features of the system frequency response as well.

In Figure 3.9, for large values of β, a range of high frequencies are redirected to the ground, i.e., attenuated. For α, the figure shows, to some extent, similar effects of β. In other words, α and β represent the frequency dependent loss in impedance and admittance of the interconnect. The reaction between these two parameters within the limit of the (α-β) value determines the behaviour of the interconnect. In addition, the comparison of Figure 3.9 and Figure 3.8 shows that in spite of the approximation that has been done for the system, the first peak harmonic can still be captured, which is directly related to the system instability. This peak represents what can happen in the frequency domain because of the resonance frequency situation. Also, it shows a high accuracy in some cases, i.g., when the value of α is 0.8, compared to the results at the same value in Figure 3.8.

3.4.2 *Model simulation*

In addition, a number of experiments have been carried out using the COMSOL tool as an emulated environment. In these experiments, one microstrip line is designed on a substrate with a 3.38 dielectric constant (ε_r) as shown in Figure 3.10. This line and the bottom ground plane, which are the metallic parts in the design, are generated assuming perfect electric conductor boundary conditions. Vacuum material properties have been used to determine the air space on top of these lines. The air

domain's surfaces are produced using a scattering boundary condition, in order to represent an open domain that can absorb waves. The circuit board has been terminated by 50Ω resistor (Z_L) and excited using a single rectangular pulse representing a one digital bit. The pulse is set to a frequency of 600 MHz, where the data rate is 1.2 Gbit/s.

Based on that, the pulse will travel along the interconnect at approximately 1.6×10^8m/s, as $\upsilon = \frac{c}{\sqrt{\varepsilon_r}}$ [36]. The time required for the signal to pass from one end to the other of a 0.15 m length line, which is chosen on purpose to make the experiment clear, is roughly 0.92 ns. The input signal with this pulse duration is equal to 90% of the line transit time which means the pulse will occupy nearly 90% of the line when passing through it, which is obvious in Figure 3.11a.

That means, from the space point of view, that as pulses reach the line far-end the space change is decreases $\frac{\partial V}{\partial x} < 0$, whilst, from the time point of view, the time change is increases $\frac{\partial V}{\partial t} > 0$. Thus, the aspect ratio of the signal across a line is given by

$$\frac{\frac{\partial V}{\partial x}}{\frac{\partial V}{\partial t}} = -\frac{\partial t}{\partial x} = -\frac{1}{v} \tag{3.55}$$

This gives an understanding of TEM waves moving with a single fixed velocity, which is in accordance with Catt-theory [36]. Here, the velocity of the signal is the factor that relates the proportional between the position change of travelling pulse at forward distance (x) and the change of this pulse at a point with time (t). Taking the above discussion further, Figure 3.11 demonstrates the propagation and reflection of the signal with 600MHz frequency along the transmission line. The coloured bar beside

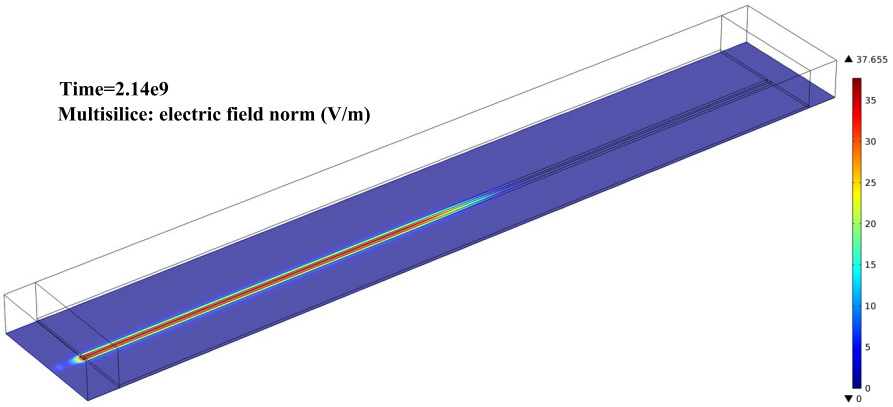
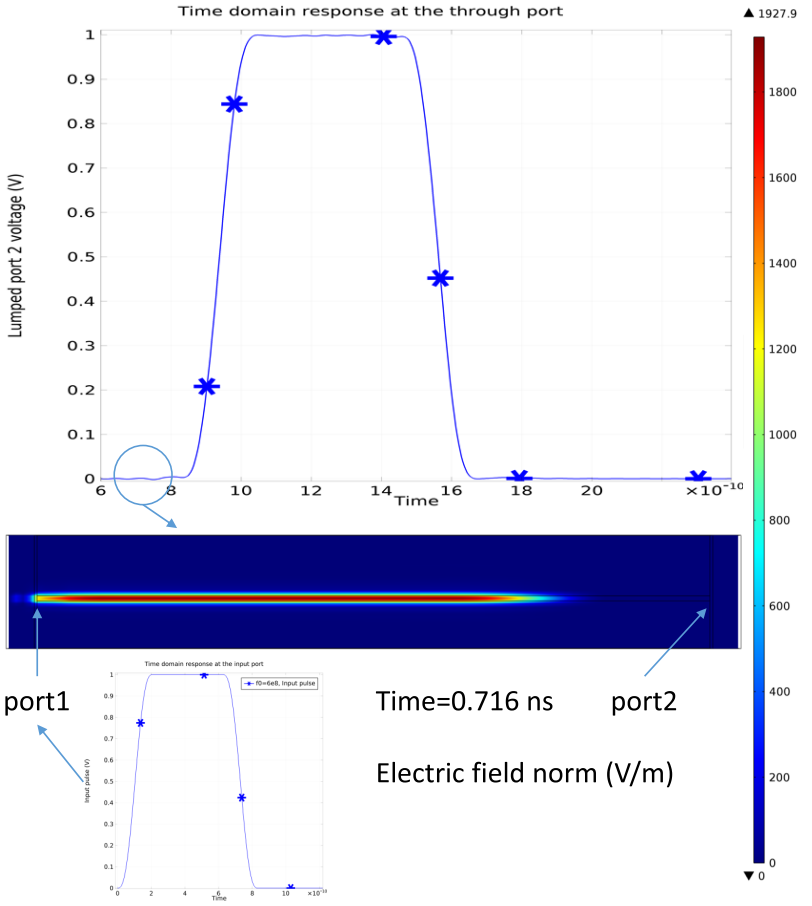
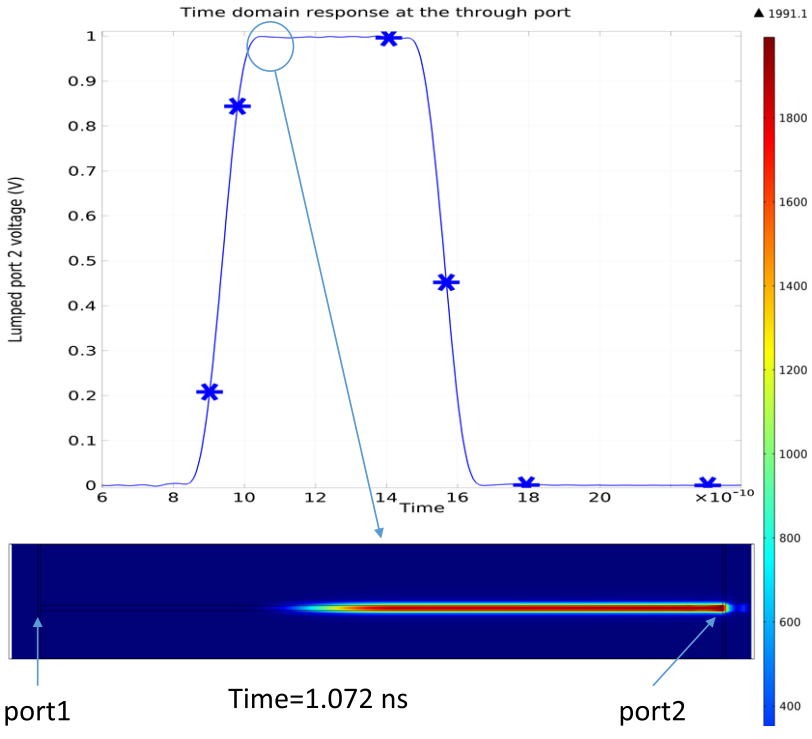


Figure 3.10: A microstrip line with a ground plane.



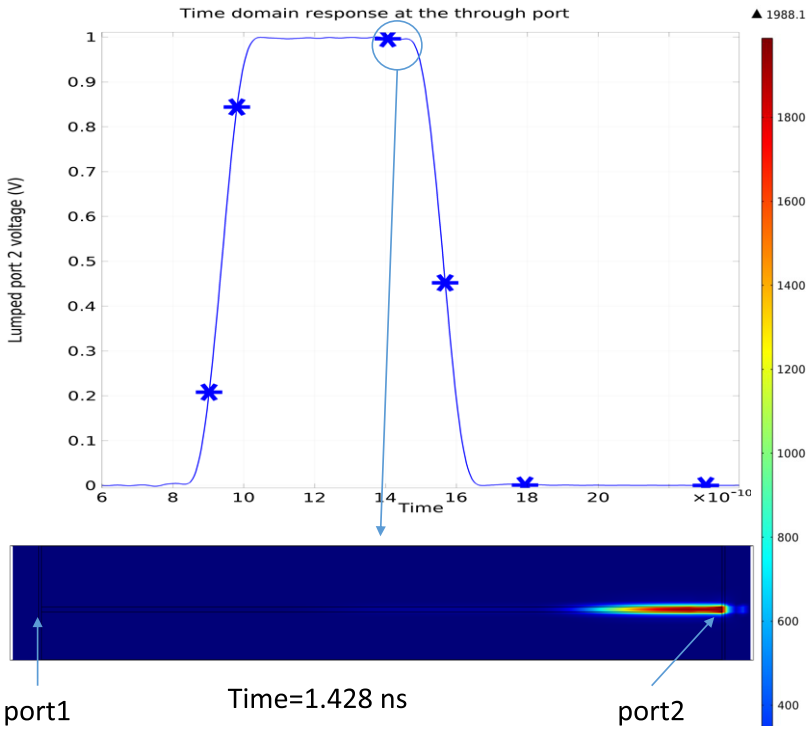
(a)



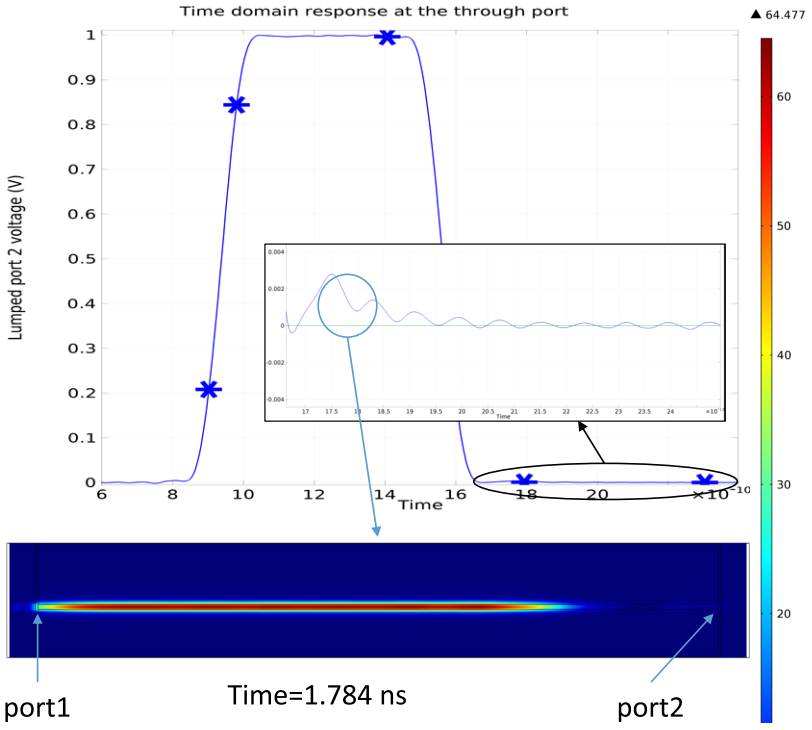
(b)

Figure 3.11: The process of the signal travelling across the interconnect; (a) The pules signal leave the first port, (b) The pules signal arrive at the far-end.

... to be continued



(c)



(d)

Figure 3.11: (continued) The process of the signal travelling across the interconnect; (c) The arrived and the reflected in the signal at the far-end, and (d) Part of the signal reflected from the far-end.

each sub-figure in Figure 3.11 displays the strength of the electric field in Volt per meter unit (V/m). For instance, it is obvious that the electric field in Figure 3.11a is greater than the electric field in Figure 3.11d, as the first one represents a far end signal arriving moment and the last one is the reflecting signal. The refection coefficient is $\rho = \frac{(Z_L - Z_0)}{(Z_L + Z_0)}$ where Z_0 is the line characteristic impedance. In Figure 3.11d, it is apparent that the discharge process exponentially decays and we can come to the conclusion that this exponential process can be approximated to $e^{-\frac{t}{\tau}}$ form, which is according to the discharge analysis of a standard lumped capacitor, this is customary.

The interconnect structure shown in Figure 3.10 has been implemented using COMSOL multiphysics tool that is a cross-platform finite element analysis and allows coupled systems of partial differential equations (PDEs). Based on this structure, a comparison between the results obtained from the proposed analytical model using Matlab with COMSOL results has been provided. The propagation delay is calculated for several line lengths from 0.1 to 2.5 mm as shown in Table (3.1), where the delay was calculated for a pulse travelling from one end to another on the interconnect. We presented the comparison to our model (3.44) with two cases; one with typical weight (when $\nu = 1$) and the other with a different weight (when $\nu = 1.01$). This was accomplished by modifying the model weight manually to properly adjust with one reading of COMSOL. Also, the table depicts the absolute error between our readings and the COMSOL readings. The model, in general, reveals that it has not suffered from a wide variation for different interconnect lengths, providing a good estimate for the signal delay. For instance, the highest recorded error was 9.25ps of the typical weight for a 2.5mm length, whereas the lowest registered error was 0.04ps of the adjusted weight for a 0.5mm length. It was observed that in both cases the Mean Absolute Error (MAE) did not exceed 3.9. On the other hand, the results accuracy of the weight-adjusted model improved by 75%, as it gave MAE within 0.95.

Also, a comparison between different models; the proposal, Elmore, Kahng's model [109] and Ismail's model [97] is made. The results have been obtained using Matlab simulation based on the presented formulae in each approach. Figure 3.12 shows these results, which demonstrate the difference between our

Table 3.1: Simulation results for different line lengths, considering a pulse input and 1 V supply.

Interconnect Length (mm)	Delay (ps)			Absolute Error (%)	
	COMSOL Delay	Proposed Delay @ ν=1	Proposed Delay @ ν=1.01	Proposed with COMSOL @ ν=1	Proposed with COMSOL @ ν=1.01
0.1	4.1	4.72	6	0.62	1.9
0.15	5.32	5.34	6.9	0.02	1.58
0.2	6.44	5.97	7.7	0.47	1.26
0.25	7.51	6.6	8.5	0.91	0.99
0.5	12.52	9.77	12.56	2.75	0.04
1	21.58	16.25	20.78	5.33	0.8
1.5	30.13	22.91	29.2	7.22	0.93
2	38.3	29.75	37.8	8.55	0.5
2.5	46.03	36.78	46.6	9.25	0.57
Mean Absolute Error				3.9	0.95

model and the others. These models either underestimate the inductance such as in Elmore or overestimate its effect as in [109] and [97].

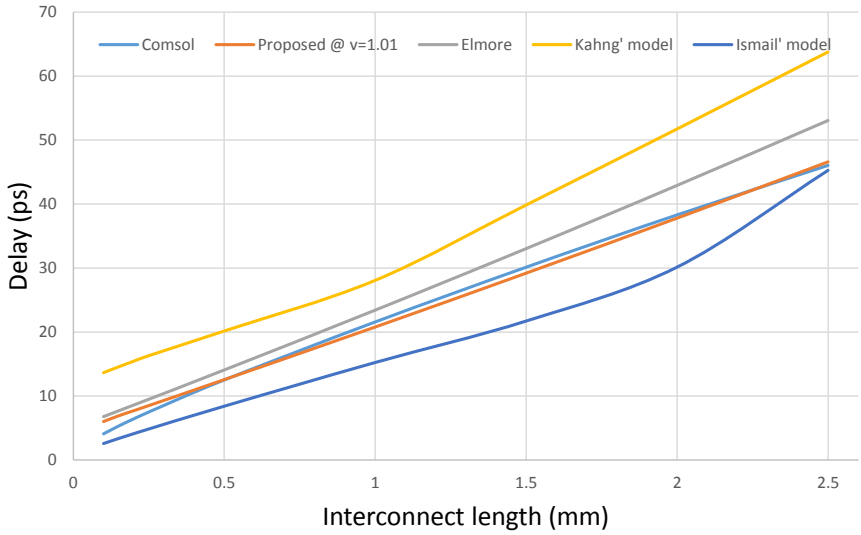


Figure 3.12: Delay time results of different models for a gate driving an RLC transmission line.

The results generally show a compatible accuracy for the proposed model with a comprehensive simulation software. That takes into account the total effects of the critical interconnect elements, such as the equivalent resistor of the nonlinear CMOS transistors, the effect of inductance, the effect of ground capacitance and the frequency-dependent elements.
Besides, to apply the fractional order interconnect model in a simulator such as Cadence Spectre, the model must be converted to the time domain through rational functional approximation [79]:

$$f(s) = \sum_{j=1}^{n} \frac{c_j}{s - a_j} + d + sh \tag{3.56}$$

Here, n is the rational order, c_j and a_j are the residues and poles in complex conjugate pairs, h and d are real. The coefficients in (3.56) can be acquired by the algorithm of vector fitting as introduced in [79]. In this procedure, the error presented by the frequency to time conversion can be mitigated by increasing the rational-fitting order.
This brings us to the conclusion that our model could be used as an alternative to the industry standard simulation tool, currently

for a single line, during the initial stages of the IC design. This is due to the flexibility of the model and simplicity and ease of compatibility for any node technology. Yet, keeping in mind that no analytical model can be used instead of full circuit level simulation tools for calculation during the final stages of the design.

3.5 CONCLUSION

In this chapter, a new definition for interconnect delay time in the fractional order domain and the general expression for RLC interconnect network model in CMOS technology based on a second order approximate transfer function are presented. It is important to note here that the definition of (3.44) are dependent on the fractional order. The suggested formula takes the effect of the fractional order into account when calculating the delay times. The fractional order in the timing formulas adds another degree of freedom, by increasing the adjustable parameters in the design, which widens the optimization space and increases the design flexibility.

4

ULTRA-LOW POWER DRIVER SCHEME INCORPORATING A BOOTSTRAP CONFIGURATION

An insight into analysing and investigating a proposed design (bootstrapped driver) for low energy and robustness to Single event upsets has been presented in this chapter.

4.1 INTRODUCTION

The rapid development of energy-constrained applications has made low power design, a primary concern. This is a paradigm shift from traditional performance-led design to emerging energy-constrained system development. Novel applications such as IoT devices, wearable computing and smart grids mainly require longer energy source life and small silicon costs; on the other hand, their performance is typically considered a secondary concern [7, 99].
Operating of such applications is based on a supply voltage of battery sources or scavenging energy from the environment. Therefore, devices involved in applications of IoT requiring to consume a certain amount of power for the sake of securing extended operability [99], as in Figure 1.1. This requires driving research towards engineering new solutions which are expected to run at low voltages of 300mV or much less [103].

Since the 1980s, scaling the power supply has become an effective way to reduce energy consumption in digital systems. Supply voltages less than the threshold voltage of the CMOS circuits have emerged showing the ability to meet the requirements of ULP regime. This approach is called the sub-threshold logic circuit. However, since CMOS scaling reaching its limits, the issue of global and long interconnects has become an important consideration due to the problem of capacitance [13].

At sub-threshold, this effect is even worse when the conventional CMOS driver needs to be as large as possible to deal with the leak of driving efficiency associated with a scaled power

supply [91]; in addition, it requires to bear with the static current I_{off} issue which is increasing at this region, particularly, in the nanometre regime [114]. Another issue comes with this advancing in semiconductor technology is that the reliability of electronic system has become more susceptible to transient faults caused by the effects of neutron and alpha-particle strikes [4]. A number of investigations have shown that the transient faults are the predominant cause of failures experienced by the state-of-the-art computer systems [101, 94]. Thus, from a system reliability perspective, it is important to consider this type of errors in the analysis of the circuit robustness.

In this chapter, in order to address these limitations, the bootstrap method is proposed because of its capability to improve the driving ability with adding feedback feature to control power consumption, as will be shown later in the results section.
By producing a voltage swing nearly of $2V_{DD}$ to $-V_{DD}$ for the V_{gs} (gate to source transistor voltage) of the NMOS and PMOS independently, the proposed CMOS inverter provides better performance and reduces leakage current. Hence, according to the formula for I-V in a sub-threshold region [55], [190], I_{off} will be reduced exponentially. Furthermore, in order to ensure the reliability of the design against the radiation-induced faults such as single event upset (SEU), an investigation for its impact has been performed. Therefore, the main **contributions** of our proposed approach to the ULP applications are as follows:

1. This work presents an improvement in power dissipation, a smaller footprint occupying, control leakage circuits and a robustness to alpha-particle strikes.

2. The approach here adds an important feature of robustness to the circuit design by connecting the pumped output of driver to (feed) pumping components in the circuit.

3. Simulations based on Matlab software illustrated the obtained advantages of the suggested approach.

4. A number of experiments have been carried out using a 90nm UMC toolkit as an emulated environment to investigate the proposed design.

To the best of our knowledge, this is the first approach that investigates a bootstrapped driver which incorporates feedback

configuration at the output and evaluates it in term of SEU tolerance.

The rest of the chapter is organized as follows. A brief introduction to the sub-threshold mode circuit, the charge boosting and the SEU, which can happen in VLSI circuits, has been presented in Section 4.2. Section 4.3 introduces the operation of the circuit and its structure. Section 4.4 describes the implementation considerations and presents the circuit design and initial simulation results for this circuit comparing it with existing designs , as well as with a conventional driver from the point of view of energy consumption and delay. Finally, the conclusions are presented in Section 4.5.

4.2 BACKGROUND

In this section, a background is introduced in the context of the work regarding the basic concepts of sub-threshold mode circuits, the boosting charge circuits and errors caused by the Single event upset.

4.2.1 *Sub-threshold mode circuits*

The operation region of any circuit depends on the supply voltage at which the circuit operates. This region of operation can be shifted from super-threshold to sub-threshold if the supply voltage is reduced to less than the threshold voltage (V_{th}). The supply voltage considerably above V_{th} and large current drives are what characterize the regime of the super-threshold, also known as the strong inversion region. Contrary, the regime of the sub-threshold, or the weak inversion region, is well-known by less current drives and an operating voltage below V_{th}. Between these two regions, there is a region called the moderate inversion which has a supply voltage near V_{th} and higher current drives as compared to the sub-threshold regime [135].

In the region when the voltage level of circuits is lower than the threshold voltage ($V_{DD} < V_{th}$), the channel between the drain and source region ceases. Nevertheless, the circuits have the ability to operate correctly owing to a steady leakage current flow through the transistor [199]. This happens due to some electrons in the source can overcome barriers and diffuse to the

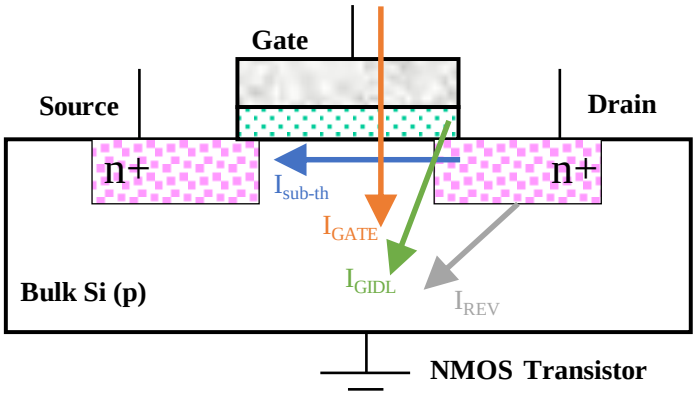


Figure 4.1: MOS device's leakage current sources.

drain. As the gate voltage V_{gs} approaches V_{th}, the flow of the generated charges can become effective particularly in ultra-low power integrated circuits [199]. The sources of this current are mainly four: gate leakage (I_{GATE}), gate induced drain leakage (I_{GIDL}), diode reverse bias junction leakage (drain to the substrate) (I_{REV}) and sub-threshold leakage (I_{sub-th}), as shown in Figure 4.1. Given this type of current is quite small compared to the transition current of the super-threshold, the dissipation of power in sub-threshold circuits is considerably reduced with the drawback [168].

The sub-threshold leakage I_{sub-th} is the dominant component amongst all leakage current components, which flows through the transistor from the drain to the source. This occurs in the weak inversion mode when the operating applied voltage V_{gs} to the transistor is less than its threshold voltage V_{th} [192]. The sub-threshold current can be considered as the total drain current in the sub-threshold regime [199], where its value can be given by the following equation [32].

$$I_{sub-th} = \mu_{eff} C_{ox} \frac{W_t}{L_{eff}} (m-1) V_t^2 e^{\left(\frac{V_{gs}-V_{th}}{mV_t}\right)} \left(1 - e^{\left(\frac{-V_{ds}}{V_t}\right)}\right) \quad (4.1)$$

where μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, W_t is the device width, L_{eff} is the effective length of the device, V_t is the thermal voltage, m is the sub-threshold slope factor and V_{ds} is a voltage of the drain-source. In this model, the first term ($\mu_{eff} C_{ox} \frac{W_t}{L_{eff}} (m-1) V_t^2 e^{\left(\frac{V_{gs}-V_{th}}{mV_t}\right)}$) is basically the current flows by diffusion, while the parenthetical term $\left(1 - e^{\left(\frac{-V_{ds}}{V_t}\right)}\right)$ represents

the roll-off in current which happens when V_{ds} equals a few times V_t. Thus, the sub-threshold current depends on different factors and varies exponentially with the gate voltage V_{gs}.
This expression (4.1) has been discussed further [55], [11] to lead to identify sub-regions in the sub-threshold region. Accordingly, the drain current expression has been modified to interpret the transition zone between sub-threshold and saturation, namely the triode region:

$$I_d = \mu C_{ox} \frac{W}{L} \left((V_{gs} - V_{th}) V_{ds} - 0.5 V_{ds}^2 \right) \tag{4.2}$$

where I_d is the current flowing from drain to source. This empirical model provides decent matching with the empirical data if its parameters are chosen carefully [55].

This relationship between I_{sub-th} and the applied voltage in this regime will exhibit almost linear behaviour in a logarithmic plot. The slope S_t of this linear behaviour is another important characteristic of the sub-threshold region since it represents the effectiveness of the transistor to turn off when V_{gs} is below the threshold voltage. It is defined as [192]:

$$\frac{1}{S_t} = \frac{\partial(\log I_d)}{\partial V_{gs}} \tag{4.3}$$

with some substitution and rearrangement applied, S_t will equals $mV_t \ln(10)$ which is given in millivolts per decade. Its ideal value at room temperature is 60mV/decade. In other words, in order to decrease or increase the current magnitude a one decade in the sub-threshold region, it needs reducing or raising in V_{gs} by no less than 60mV.

4.2.2 *The charge pumping principle*

In our approach, the bootstrap has been used based on a charge pump that is a type of DC-to-DC converters, which utilities a capacitor as a charge holder to generate a voltage higher than the power source voltage [185]. Although the design of this technique is electrically a simple circuit, it is able to achieve a level of efficiency reaching 90-95% [46]. To see how this is possible, consider a simple 4-stages Dickson charge pump as shown in Figure 4.2. When the signal $\phi 1$ is low, D1 will charge C1 to V_{in}.

When $\phi 1$ goes high, the top plate of C1 is pushed up to $2V_{in}$. D1 is then turned off and D2 turned on and C2 begins to charge to $2V_{in}$. On the next clock cycle, $\phi 1$ again goes low and now $\phi 2$ goes high, the top plate of C2 is pushed to $3V_{in}$. D2 switches off and D3 switches on, charging C3 to $3V_{in}$ and so on with charge passing up the chain hence, the name 'charge pump'. The final diode-capacitor cell represents a peak detector and not a multiplier in the cascade [46].

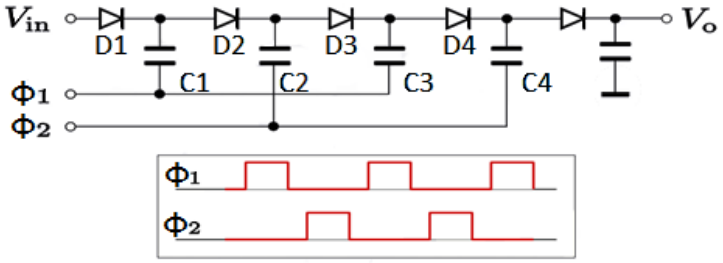


Figure 4.2: Four-stages Dickson charge pump [46].

This technique increases the supply voltage efficiently, however, it only allows a positive voltage; that is, V_o will swing just from 0 to 2 or 3 V_{in}. Therefore, we have modified the cross-coupled MOSFET voltage doubler to give a full swing from -V_{DD} to $2V_{DD}$.

4.2.3 *Single event upsets (SEU)*

Soft errors generated by the radiation impact become increasingly a major concern with improving the scale of microelectronic design to nanometer era. What induces a fault in integrated circuits is the energy transfer from high energy particles (i.e. electrons, protons, energetic heavy ions and alpha particles) to the impinged material. This happens through indirect or direct ionization mechanisms. Amongst these energetic particles, high-speed neutron and alpha particles which emit from cosmic rays and packaging materials, respectively, are the main sources of SEU in semiconductor devices. However, by using packaging materials which have fewer alpha particles emission, neutrons surpasses alpha particles as the cause of soft errors since 1990 [88].

This event affects the functioning of the digital parts of a circuit in a certain aspect, which eventually causes incorrect results. When one of these high-energy particles penetrates a sensitive

region such as the area near the reverse biased drain junction of a transistor, electron-hole pairs are formed, as demonstrated in Figure 4.3. The amount of energy to create the electron-hole

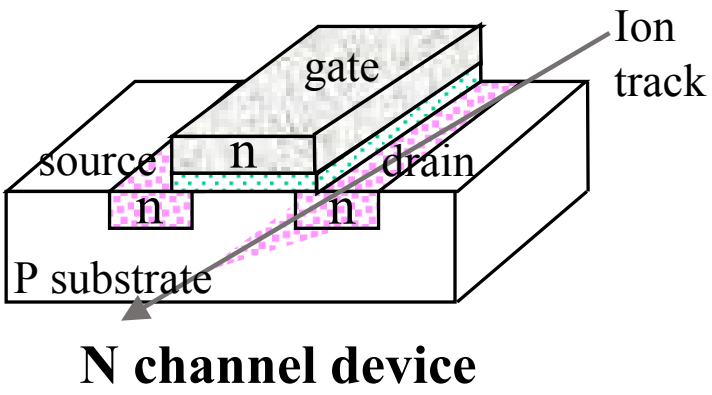


Figure 4.3: Particle strikes an NMOS device.

pairs has been recorded by many studies to investigate this phenomenon. Since 1990, the lowest observed energy causing a glitch, termed Linear Energy Transfer (LET), was $15\text{MeV} \cdot \text{cm}^2/\text{mg}$. While, at a high level of this value, the duration of the measured Single Event Transient (SET) was 40ns which was adequate to introduce an error at the system level. In 2004, however, LET by value at $2\text{MeV} \cdot \text{cm}^2/\text{mg}$, was enough to cause a transient pulse with a duration of a few nanoseconds [67, 94] because of the technological scaling [137]. This confirms that with every new technology node, the susceptibility of circuits to the effects of particle strikes rises.

The particle minimum energy which creates a voltage transition of sufficient strength to switch a logic value on a node is given by [69]:

$$E_{LET_{min}} = 3.6\text{eV}\frac{Q_{crit}}{q} \tag{4.4}$$

where 3.6eV is the energy required to generate an electron-hole pair in silicon and Q_{crit} is the critical charge which is the necessary amount of charge to set off a change in the logical level. The Q_{crit} value of any struck node can be determined as follows:

$$Q_{crit} = C_N V_{DD} + I_{MDP} T_{pulse} \tag{4.5}$$

where I_{MDP} is the maximum drain conduction current of the PMOS transistor, C_N is the capacitance of the affected node and

T_{pulse} is the the transient pulse width [89, 94, 137].
From (4.5), it can be seen that the applied V_{DD} to the node and its capacitance have a direct impact on the Q_{crit} value. Accordingly, decreasing the supply voltage and the node capacitance as a consequence of the technology scaling down will reduce the Q_{crit} value of the node. This leads to an increase in the susceptibility to radiation-induced soft errors in new design technologies.

4.3 PROPOSED CMOS INVERTER

The bootstrap driver fundamentally consists of two combinations. The first one is a pre-driver comprising of:
a) an inverter (PM1 and NM1) for the bootstrap control,
b) pre-charging and pre-discharge transistors (PM2 and NM2) for the bootstrap capacitors C_{bootP} and C_{bootN} and, finally,
c) a driver (PM3 and NM3) for the boosted output.
The second part and how it is fed back by the boosted voltage represents the main difference with reported bootstrap circuits along with the low hardware overhead. In other words, this part has been implemented with minimal components and without the need for additional circuitry such as level shifter and extra V_{DD} supplies. This combination has the ability to theoretically provide a voltage swing between -V_{DD} and 2V_{DD} in order to address the fundamental limitations of the leakage current and poor driving capability in sub-threshold regime. This is through shifting the circuit operation region to above the applied supply voltage.
The second combination is a normal buffer (inverter) with PMOS and NMOS transistors that are driven by the boosting voltage circuit (the first combination). Figure 4.4 shows the circuit scheme of the proposed driver and its main components, where the pre-driver is the circuit on the left which uses the capacitors to boost the voltage. Then the buffer, the circuit on the right, is used to drive the interconnect with a sub-threshold voltage swing from GND to V_{DD}.
Given the exponential behaviour of the current toward the applied voltage in the sub-threshold region, 10 times higher driving current can be expected with at least 60mV boost in the driver voltage [135]. At the same time, this extra voltage suppresses the leakage current, while the PMOS or NMOS is turned off.

Additionally, regarding the hardware overhead, the proposed design has low effect.
We have used this approach to improve the driving capability of the CMOS circuits due to the increase in the sub-threshold swing which increases the driving current exponentially. In this design, using the charge pump as a booster (bootstrap) for the final stage (the second combination) means that its effect will be implicit; in other words, the boosted swing voltage will not be used to charge and discharge the capacitor load (CL), hence this will not have a considerable effect on the circuit power consumption.

4.3.1 *Circuit operation*

The schematic of our approach is depicted in Figure 4.4. There are significant nodes in the design which are highlighted and named VV_{DD}, VGND and B-out. VV_{DD} and VGND are the boosted nodes and act as virtual supply voltage and ground for the PM3 and NM3 driver, respectively. B-out node is boosted above VV_{DD} and below ground depending on voltages of the former boosted nodes.
Figure 4.5 displays transient waveforms of the significant nodes

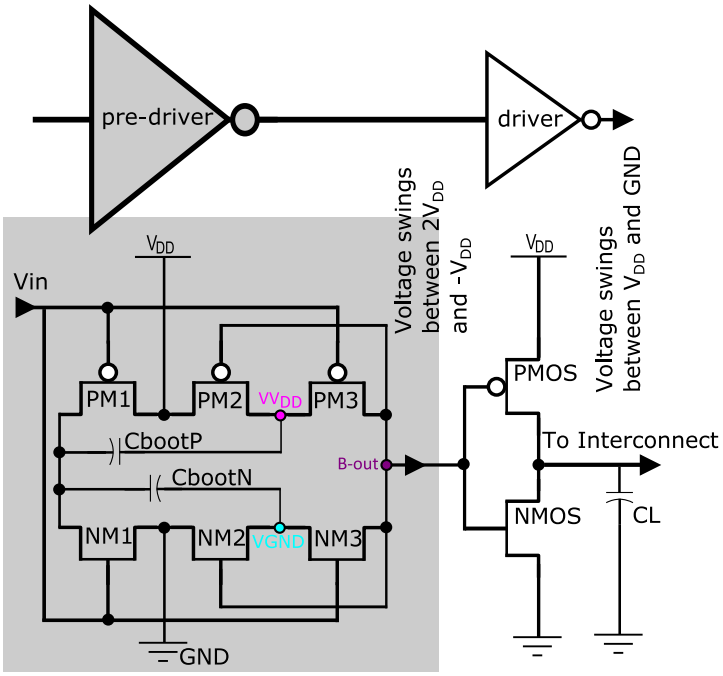
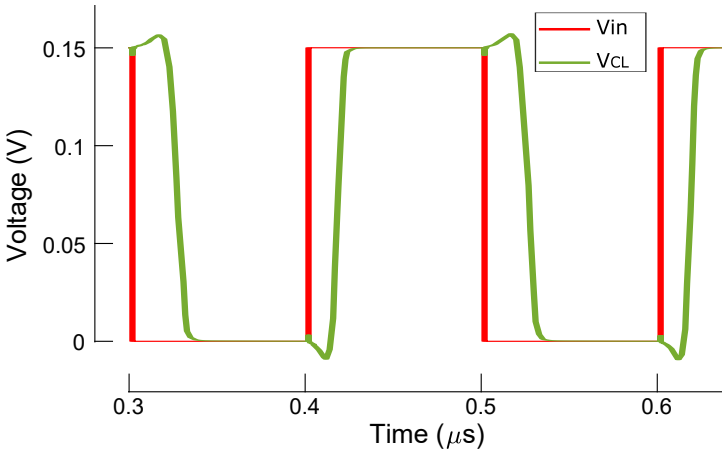
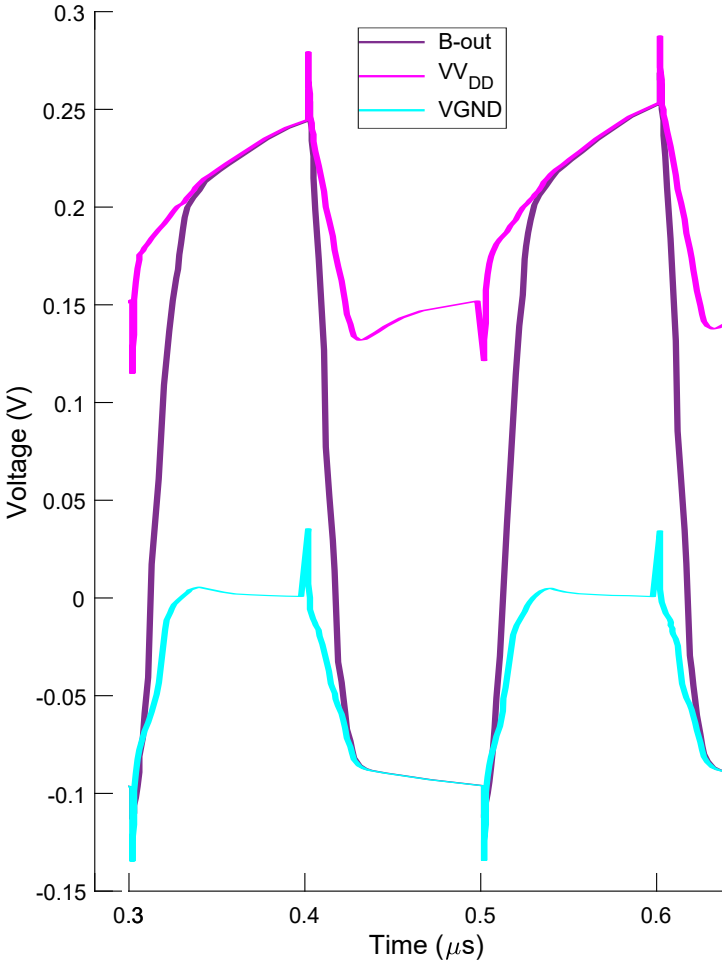


Figure 4.4: Circuit of the proposed driver.



(a) Input and output waveforms.



(b) Significant nodes waveforms.

Figure 4.5: Signal waveforms of the circuit.

besides the input and output signals with a power supply of 150mV. Based on this figure, when V_{in} goes low, the output of PM1 and NM1 inverter will be pushed up. It boosts VV_{DD} above V_{DD} through boost capacitor C_{bootP} that assumed to be pre-charged a voltage near the V_{DD} from the previous cycle. Meanwhile, PM3 is turned on to pass the bootstrapped voltage (above V_{DD}) to B-out. The voltage of B-out does not merely drive NMOS of the second stage better but also turn off PMOS better to reduce the leakage current beside switch on NM2 to the pre-discharge of VGND (C_{bootN}).
A similar but opposite operation takes place in the second state when V_{in} goes high, that is VGND boosted below ground which initially has a voltage of 0 V. At the same time, NM3 is turned on, so the boosted signal at VGND passes to B-out to drive PMOS of the next stage in order to pull up the capacitive load CL. Not only that but also it turns on PM2 better to pre-charge C_{bootP} along with closes NMOS and NM2 better to reduce the leakage current.
The size (W/L) of transistors (PM1, PM3, NM1 and NM3) is 200nm/160nm and (PM2 and NM2) is 120nm/ 80nm, while 25fF MOM (metal-oxide-metal) capacitors were used as the bootstrap capacitors. The circuit has been implemented using the 90nm process.

4.3.2 *Boosting efficiency*

Theoretically, the boosted voltage should present a voltage swing from -V_{DD} to $2V_{DD}$. However, the boosting efficiency (η_B) is influenced by the boosting capacitance and the boosted node capacitance, which has been defined as the ratio between the former capacitance and the sum of both [114]. For example, the capacity of the boost capacitance (C_{bootP}) together with the total parasitic capacitance (C_{B-out}) of the boosted node B-out, which produces due to associated transistors PM2, PM3, NM2, NM3, PMOS and NMOS, determine the efficiency of the boosting during the pulling down case. Accordingly, the voltage of the relevant node can be estimated as follows:

$$V(pulldown) = \frac{C_{bootP}}{C_{bootP} + C_{B-out}} \cdot 2V_{DD} \tag{4.6}$$

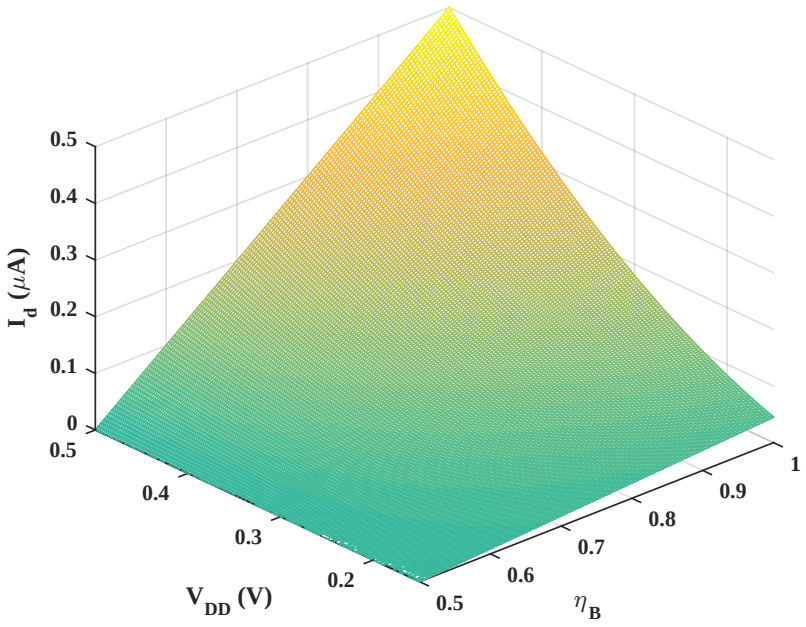


Figure 4.6: Interaction between discharge current and V_{DD} with efficiency

.

Likewise, for the pulling up voltage as:

$$V(\text{pullup}) = \frac{C_{bootN}}{C_{bootN} + C_{B-out}} \cdot -V_{DD} \tag{4.7}$$

Therefore, the efficiency of the boosting depends on the parasitic capacitance of the relevant transistors as well as the boosting capacitance which should be designed to be as large as possible for better efficiency. Consequently, the last stage of the driver circuit is pushed to a higher operation region, i.e. moderate or strong inversion rather than weak inversion based on the amount of boosted voltage.

Owing to the boosted voltage, the discharge current I_d in the components exposed to this voltage will be:

$$I_d = \mu C_{ox} \frac{W}{L} \left((\eta_B \cdot 2V_{DD} - V_{th}) V_{DD} - 0.5 V_{DD}^2 \right) \tag{4.8}$$

As a result, the boosted voltage increases the current driving capability. Figure 4.6 demonstrates this effect, which is a significant potential to fulfil the ULP design requirements regarding the effectiveness and error tolerance.

Similarly, not only will the discharge current be affected by the boosted voltage but also the leakage current and the equiva-

lent resistance (R_{eq}) of the MOS transistor, where the latter will improve according to the following:

$$R_{eq} = \frac{V_{ds}}{I_{sub-th}} = \frac{V_t}{k_t e^{\frac{\eta_B \cdot 2V_{DD}}{mV_t}}} \tag{4.9}$$

where $k_t = \mu_{eff} C_{ox} \frac{W_t}{L_{eff}} (m-1) V_t^2 e^{(\frac{-V_{th}}{mV_t})}$, which represents strength of the transistor. This expression (4.9) has been driven based on (4.1), which can be rearranged to have:

$$I_{sub-th} = \mu_{eff} C_{ox} \frac{W_t}{L_{eff}} (m-1) V_t e^{(\frac{\eta_B \cdot 2V_{DD} - V_{th}}{mV_t})} V_{ds} \tag{4.10}$$

where the booted voltage was taken into account and the last term $(1 - exp(-V_{ds}/V_t))$ of (4.1) has been expanded in Taylor series and truncated to first order. This assumption can be applied for values of V_{ds} lower than V_{th} [158]. Furthermore, the leakage current will be suppressed exponentially depending on this applied voltage.

4.4 IMPLEMENTATION AND RESULTS

In this section, the 90nm process has been utilised to implement the studied circuits and present their simulation results. The device sizes of the circuits are listed in Table 4.1.

4.4.1 *Circuit implementation and results*

The driver circuit has been implemented using Cadence software to measure the performance of the proposed design. The circuit in Figure 4.4 employs a standard performance regular threshold voltage (SPRVT) transistor, 25fF boost capacitors (C_{bootP} and C_{bootN}) of a metal-oxide-metal (MOM) type, and 200fF capacitance connected to the driver output (CL) to emulate the 10mm interconnect.
At this point, it is important to mention that the consumed average total power and the leakage power have been measured separately. The leakage power was observed as the average value from the possible combinations, i.e. high and low logic, of the input signals in a stable state. The average power was counted when a train of pulses is applied to the input. While the delay

was measured using a relevant function that is already built-in in the simulation environment.

The simulation was executed under a 150mV supply voltage and 5MHz frequency as the input frequency of the driver to imitate the worst case transition activity. Under these conditions, the proposed driver achieves an average power consumption of 24nW and 85.5pW as a leakage power dissipation with 10.5ns average input to output delay.

Whilst, under a 200mV supply voltage, the reported driver circuit in [126] reached 0.74μW and 276nW as an average and leakage power, respectively, with 15.1ns as an average circuit delay. In another study [91], the estimated results of the designed driver were 1μW average power with leakage power 107nW and 6.9ns driver time delay. Furthermore, the results of [114] were 1.7μW for total average power and 833nW leakage power where, from the point of view of the power leakage, this was the worst results so far among tested drivers.

Table 4.2 summaries the comparison results of the proposed driver circuit with these works. In terms of the figure of merit (FoM), the power-delay-product (PDP) is an important measurement for evaluating the energy efficiency of a circuit in general. Meanwhile, the metric of the energy-delay product (EDP) was used, because it is preferable for low-frequency circuits [188]. While I_{off}/I_{on} is a critical factor in the design evaluation, particularly regarding ULP circuits [190]. The proposed work demonstrates very good merit for these measurements, comparing to the others. The advantage of the proposed design scheme regarding these measurements is owing to the number of components operating in the boosted voltage as shown in Table 4.2. The boosted components in the table refer to the transistors that are driven by the produced bootstrapped voltage. Accordingly, promoting these components amount in the circuit improves the performance of the circuit as a whole.

Even though the proposed driver achieves the best results for power saving and energy efficiency, it has not provided the best recorded delay time, particularly at $V_{DD} = 0.15V$, which is normal as going deeper in sub-threshold voltage area. Therefore, the EDP metric, which is equal to PDP $\times$ delay, has been applied as another measure to demonstrate that the proposed design

Table 4.1: Devices' sizes.

The work	[91] (nm/nm)	[114] (nm/nm)	[126] (nm/nm)
Inverter No. (NMOS W/L)(PMOS W/L)	2 (200/90)(400/90)	2 (200/90)(400/90)	1 (200/90)(400/90)
Switch No. (NMOS W/L)(PMOS W/L)	1 (200/160)(200/160)	3 (200/90)(200/90)	3 (200/90)(200/90)
Driver No. (NMOS W/L)(PMOS W/L)	1 (285/90)(340/90)	1 (260/90)(300/90)	1 (250/90)(340/90)

Table 4.2: Comparison summary.

Driver	This work		[91]	[126]	[114]
Supply voltage (V)	0.15	0.2	0.2	0.2	0.2
Voltage swing	$-V_{DD}-2V_{DD}$		$-V_{DD}-2V_{DD}$	$GND-2V_{DD}$	$-V_{DD}-2V_{DD}$
Boosted components of total (%)	50		25	25	27
Frequency max (MHz)	5	13.37	10	4	5
Leakage power/Total power (%)	3.57	2.06	10.59	37.29	48.71
Average delay (ns)	10.5	7.1	6.9	15.1	13.9
FoM (pJ)	0.05	0.094	0.1	0.19	0.34
EDP ($\times 10^{-22}$ J$\times$s)	5.24	6.67	6.97	28.7	47.3

is the best in the context of energy saving compared with the reported works.

Moreover, an investigation has been conducted to find the trade-off between the conventional buffer, i.e. regular one with two inverters, and the proposed design from the point of view of energy consumption and circuit delay. Thus, to run this comparison, we repeated the same experiments under the same circumstances except that the boosting technique was not used, in order to design the normal buffer in such a way as to be close to a bootstrap driver design. The results were as predicted, where the conventional buffer, with the same proposed circuit's transistors size where PMOS (NMOS) W/L is 800nm/100nm (650nm/100nm), does not have the capability to drive the same load (200fF) with 150mV as the supply voltage to obtain the same transient response as the design with boosting. The transient response results at the CL for the two drivers are demonstrated in Figure 4.7.

Therefore, the solutions are either splitting the load into 8 parts

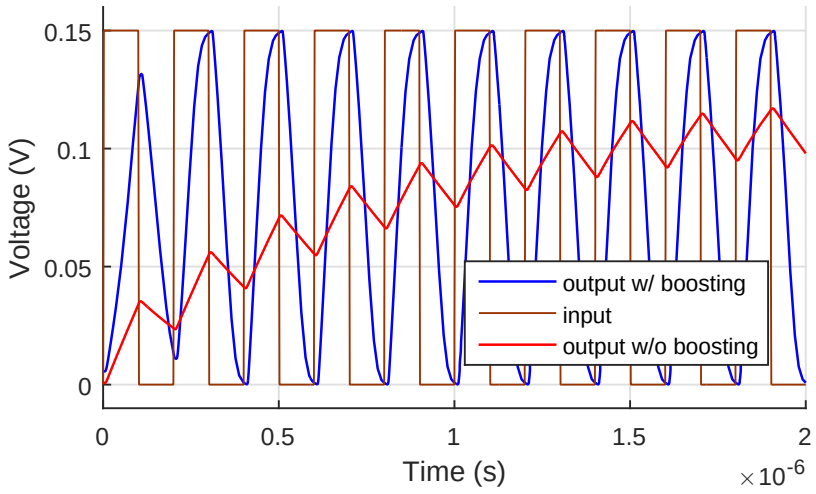


Figure 4.7: Transient response waveforms of drivers at the CL with the same transistors size and conditions.

and using repeaters for each part with 25fF, or increasing the size of the normal buffer transistors so as to have the ability to drive this load. Preliminary results show that both situations lead to a power consumption increase, regardless of the chosen solution. A large transistors buffer, its transistors approximately 12 times are larger than these in the proposed design where PMOS (NMOS) W/L is 12.5µm/100nm, has been implemented

so as to give a fair comparison with the bootstrapped design, where the two drivers are designed to have the same rise and fall output waveform response.

The results of the experiments have been obtained by implementing the UMC 90nm technology using the Cadence Spectre simulation toolkit. The simulation was carried out for a long enough time to ensure that the output of the circuits being examined has reached a steady-state condition.

The bootstrapped driver has shown an improvement of 20.5% in the energy efficiency compared to the conventional driver. While, w.r.t the average power, the driver without boosting has consumed 23.96% more power than the proposed driver. This saving is due to the reduced leakage current which has a main role in the power dissipation of sub-threshold circuits. Table 4.3 lists the results of this comparison when the supply voltage is 150mV, the load is 200fF and the frequency is 5MHz. The table also shows that the estimated chip area of the proposed driver is 112.9μm^2 versus 142.8μm^2 for the normal driver ,where these were measured based on post-layout simulations. However, the improvements in chip area, power and energy consumption of the proposed driver are accompanied by a greater circuit delay, as shown in Figure 4.8. These results are normal from the delay point of view if it has realized that the bootstrapped driver practically has more stage since it involves using capacitors as shown in Figure 4.4. Meanwhile the conventional driver is designed to have two stages, i.e. two regular inverters, which require fewer but larger transistors. Despite that, the main consideration in this report is not the delay but the energy saving which have

Table 4.3: Summary of comparison results.

Item	Buffer without boosting	Buffer with boosting
Average power (nW)	31.45	25.37
Total energy per 10cycle (fJ)	62.9	49.97
Average delay (ns)	9.9	10.5
EDP ($\times 10^{-23}$ J$\times$s)	62.27	52.39
Chip area estimated (μm^2)	142.8	112.9
Load (CL) (fF)	200	
Supply voltage(mV)	150	

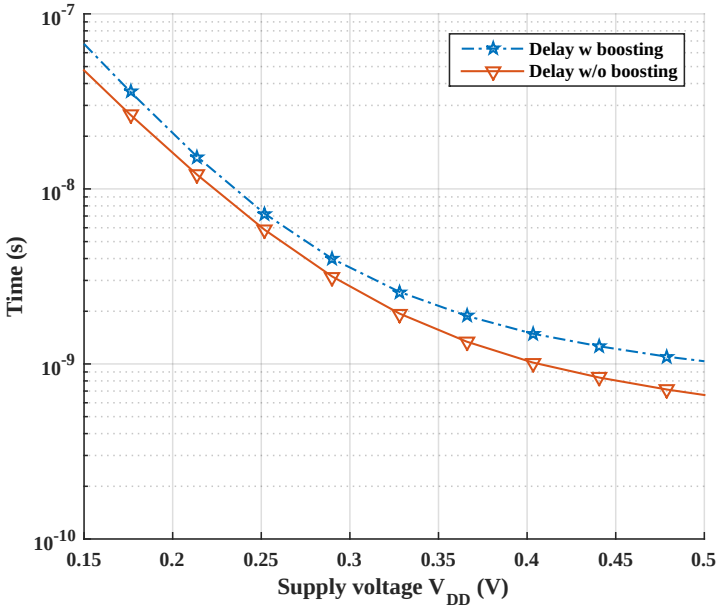


Figure 4.8: Drivers with/without boosting delay with 200fF load and 5MHz frequency.

been achieved by using a boosting technique.
Another perspective is that the buffer's consumption of energy, which is shown in Figure 4.9. Accordingly, the figure provides the outcome of these experiments where the supply voltage has been changed from deep sub-threshold to near super-threshold voltage, which obviously shows the advantage of the buffer with boosting compared to the one without boosting.
On the other hand, Fig. 4.10 shows the improvement of the boot-strapped driver compared to the normal driver from the point of view of leakage power. Furthermore, Fig. 4.11 demonstrates the proposed scheme advantage in the context of the energy efficiency. This efficiency or Power-Down efficiency is calculated in this work based on the following equation:

$$E_{efficiency} = \frac{Useful_{energy}}{Total_{energy}} \times 100\% \tag{4.11}$$

where the dynamic power of the circuit for a certain period of time was deemed as the useful energy. Accordingly, the leakage energy is considered wasted energy. This occurs when the circuit is considered in idling state, i.e. it does not perform any activity. The metric in (4.11) takes into account not only the energy consumed during computing, that is calculated when the circuit

performs an activity due to changes applied to its circuit input, but also the energy consumed during idle state. A higher this metric implies a more energy-efficient solution.

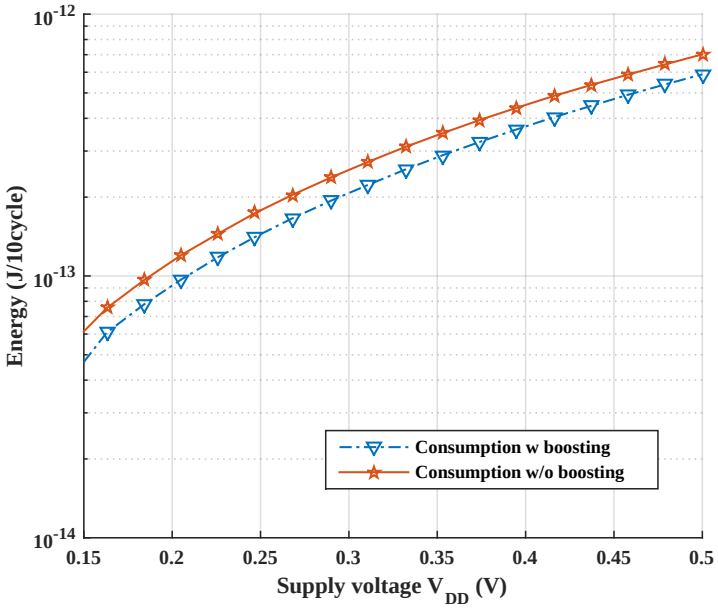


Figure 4.9: Energy consumption of buffers under scaling of supply voltage.

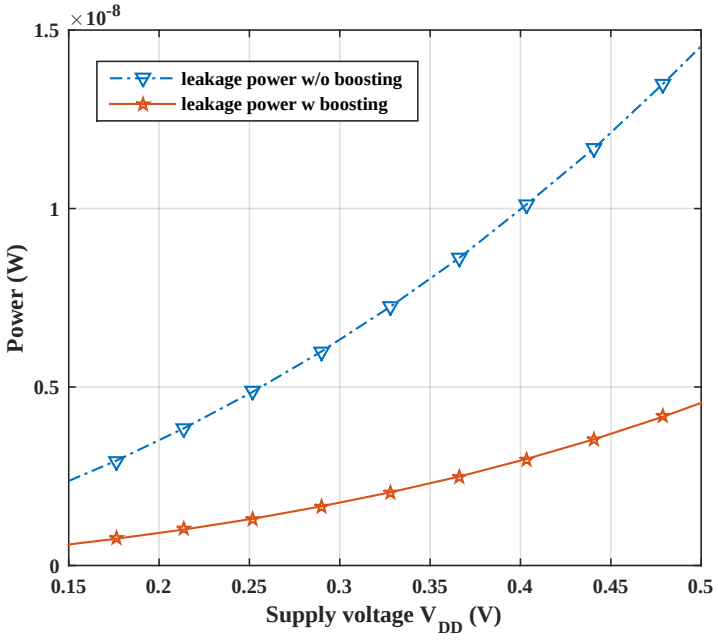


Figure 4.10: Power leakage of the drivers.

From this comparison, the power consumption of the proposed scheme is lower than that of regular or other bootstrap-based

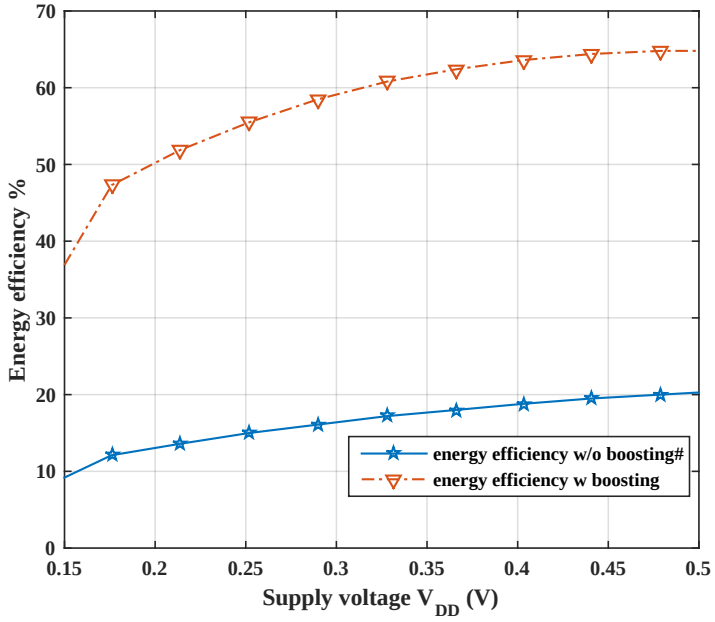


Figure 4.11: Energy efficiency of the drivers.

schemes, by at least 25%. Thus, if the proposed design can make this amount of improvement, then its sustainable battery life can be extended at the same rate for the fixed throughput compared to others. In addition, it demonstrates the ability to operate at extremely low voltage, yet, with effectiveness regarding energy dissipation, which is our main focus. Therefore, the solution presented in this work can be utilised to meet the requirements of IoT applications, such as these are regarding lower supply voltage and provided by sources of batteries and energy collected from the environment.

4.4.2 *Measurement and modelling of an SEU*

The neutron particle strike is chosen to be the cause of the fault in a digital circuit. Therefore, in order to estimate the reliability of the designed circuit, we need to model the transient current pulse that is generated because of the particle strike. This model needs to be chosen carefully, since it has a significant impact on the accuracy of the estimated reliability. A model reported in [111] is used, which has been introduced as follows:

$$I_{SRC}(t) + C_S \frac{dV(C_S)}{dt} = G_{REC}(t) + G_{RAD}(t) \tag{4.12}$$

where C_S is a value used to conserve the deposited charge, its value is assigned arbitrarily and neither critical nor related to any internal capacitor in the circuit. G_{REC} is a dependent current source represents the recombination current in the device. G_{RAD} is a dependent current source and represents the transient current pulse induced from the particle strike. Finally, I_{SRC} represents the current that deposits the required amount of charge into the device, the independent double-exponential current source is used to generate this component of the model.

$$I_{SRC}(t) = \frac{Q_{crit}}{(\tau_F - \tau_R)}[e^{\frac{-t}{\tau_F}} - e^{\frac{-t}{\tau_R}}] \tag{4.13}$$

This current model is the most commonly used model where the two (τ_F and $-\tau_R$) are time parameters representing the falling and rising time constants of the exponentials. Whilst the model in (4.12) is used here because of its ease of implementation in SPICE simulations and for its accuracy [4]. In this model, the effect of a neutron strike is represented as a dependent current source added into a BSIM4 SPICE model of a MOSFET transistor. This model is attached with Cadence simulation tool in circuit-level simulation to inject different SET's in the circuit. Figure 4.12 illustrates using this current source model to generate transient current pulses at a fixed value of supply voltage and different LET values. It is obvious that the current pulse splits into two regions, where the first one is a spike pulse simulating the drift charge collection and representing the instant response of the device which is depending on the LET value. While the second one represents the charge diffusion phase and depicted by the plateau region of the pulse. This part is longer than the first one, where its magnitude also depends on the value of LET. Furthermore, Figure 4.13 shows the response of a regular inverter at different supply voltages to a transient current pulse with LET=50MeV $\cdot$ cm^2/mg produced by using the bias-dependent current source. As can be noted, the amplitude of the transient pulses differs in accordance with the supply voltage values. Hence, this demonstrates the advantage of this model to correlate with the applied voltage of the struck node.

The conventional and the proposed designs have brought to study one more time, in order to test the circuit drivers against the SEU. We attached the current source to all design's nodes

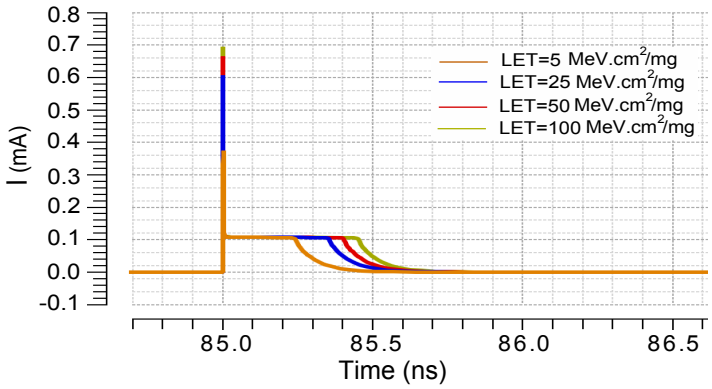


Figure 4.12: Transient current pulses generated at V_{DD} = 1V and different LET values.

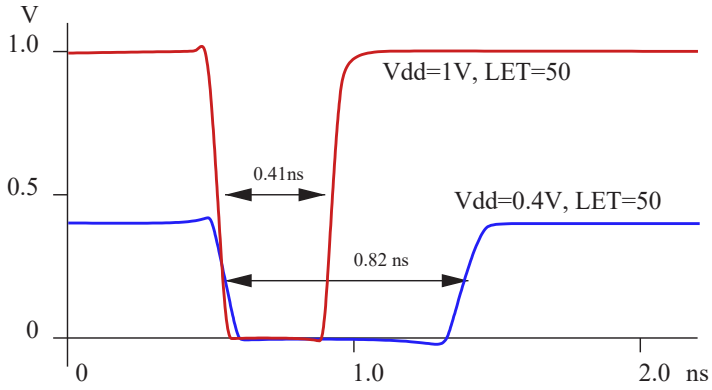


Figure 4.13: Responses of the inverter to a transient current pulse

one after the other, as shown in Figure 4.14, and in each case observed every change in the output voltage swing. For the conventional driver, there are only two nodes to inject the current source. These circuits are implemented in 90nm UMC technology with the same V_{DD}, operating frequency and temperature.

This process enabled us to obtain Parameter Vector (PV) (SET characterised with two parameters, namely, the LET and arrival time) and simulating the circuit in order to determine the critical values of this vector [4]. We repeat this for different V_{DD} values in order to see how the reliability changes under voltage-frequency scaling (the clock period is adjusted to the propagation delay under each V_{DD} value). This approach has been adopted rather than the complex, traditional methods that use multi-iteration statistical procedures. The experiments were carried out for different V_{DD} values from 0.15 V to 0.5 V. This minimum supply voltage is chosen to ensure that the signal integrity of the drivers

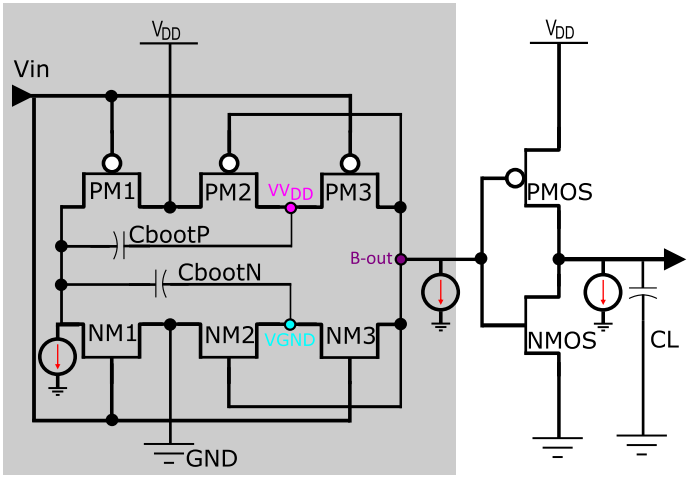


Figure 4.14: Circuit implementation of SEU analysis.

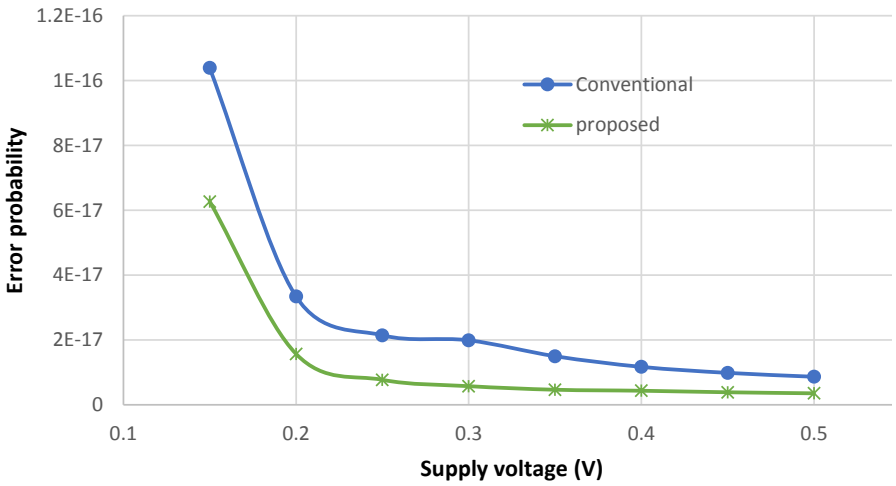


Figure 4.15: Comparison of error probability at different voltages.

is still intact. Figure 4.15 indicates that the proposed driver is better among the two circuits under the test for regarding this kind of soft errors. This improvement is mainly owing to two reasons.
Firstly, based on the results in previous Section 4.4.1, the proposed scheme has enhanced the current and the voltage of the driver internally. Subsequently, the critical charge for the proposed driver has increased as well based on (4.5). Secondly, regardless of the fact that the proposed circuit has been tested more than conventional one because of having more nodes, the boosting stage acts as a mask for glitches generated by SET. This is because the boosted voltage where the produced pulses do not propagate through the next stage and attenuated. Roughly, our circuit achieved 60% improvement relative to the conventional driver.

4.5 CONCLUSION

Interconnect drivers used in ultra-low power regime for clock distribution networks and on-chip buses suffer from considerable performance degradation due to the fact that the supply voltage is scaled down, unlike drivers' capacitive loads which have not. Added to that, there is an issue of performance variability at sub-threshold region. Hence, our approach has proposed using buffers with a charge pump booster, and this has met the expectations of improvements in performance by reducing power consumption and increasing energy efficiency. The reason for this is that the current driving is improved due to the exponential relationship between the transistor drain-to-source current and the gate-to-source voltage. The proposed driver has shown an improvement in the energy efficiency of 20.5% compared to that of a conventional driver and other previously reported boosted drivers. Meanwhile, the driver without boosting consumes 23.96% more power than our driver. The proposed driver circuit achieves a better tolerance to the SEU effect reached 60% compared to the traditional circuit.

5

CONCLUSIONS AND FUTURE WORK

5.1 SUMMARY AND CONCLUSION

Energy, dynamic power and leakage power are all crucial in SoC directed for IoT applications. Design of an energy-efficient system is key to meet requirements of such applications in low power consumption and long shelf life. In order to achieve this, optimizations and innovations are required at all design levels to obtain the targeted energy and power.

Today's SoC technology can reach to unprecedented computing speed that is the main reason for altering the IC design bottleneck from computation capacity to communication bandwidth and flexibility. For submicron technology and very high clock frequencies, on-chip interconnection has been modelled exhibiting transmission line behaviour since a simple RC model has become inadequate.

During the last decades, modelling based on the fractional order elements for a number of physical systems has emerged as realistic approaches. Motivated by the successful applications in many areas of science and engineering, fractional order elements have emerged as a promising paradigm.

This thesis introduces a study into the design of generalised interconnect model and implementation on two levels.

Overall exploring the solutions to tackle challenges associated with interconnect and energy saving trade-off is promising, so our approach is settling down the issue toward ultra-lower power design and dealing with a physical layer.

On the first level, this study describes an energy efficient bootstrapped CMOS inverter for ultra-low power applications. The proposed design is achieved by internally boosting the gate voltage of the transistors (via the charge pumping technique), and the operating region is shifted from the sub-threshold to a higher region, enhancing performance and improving tolerance to SEU effects. Despite the proposed bootstrapped driver has been implemented with a sub-threshold voltage, few transistors engaging

in the sub-threshold region due to the new structure. Our analysis shows that the proposed implementation achieves around 20% reduction in energy consumption compared to conventional designs under a supply voltage of 0.15V V_{DD}.
In addition, features required to facilitate the implementation of SoC circuits in the ULP regime have been considered in this work by providing a long battery life. As the on-chip interconnect experiences poor performance under the sub-threshold regime, the boosted buffer has met the expectations in improving the performance by increasing power-saving and mitigating the effect of temporary faults such as SEUs. The reason behind the improvement is that the proposed design produces a voltage swing to the CMOS driver input more than the applied supply voltage. Consequently, the boosting voltage exponentially enhances the driving current due to the exponential relationship between the drain to source current and the gate to source voltage. The suggested technique has met requirements to have an efficient driver supporting a long interconnect.

On the second level, we proposed a new general formula for RLC interconnect circuit model in CMOS technology using fractional order elements approach. The study is based on approximating an infinite transfer function of the CMOS circuit with a non-integer distributed RLC load to a finite number of poles. Although the proposed model of the interconnects was based on distributed RLC, the interconnect conductivity G effect has been taken into account as a real part of the factional capacitance.
It is accurate because of the effect of adding fractional order variables and since these adapted variables are utilised for tuning the model to match the design regardless of its complexity. A number of analyses were set up at different levels of the design to evaluate the effectiveness of adding fractional order elements. First, demonstrating the significant effects of generalising parameters was gained by studying the fractional order impedance and propagation constant of the transmission line for a range of frequencies.
Second, using Matlab we assessed the potential of the proposed approximated model besides the exact one, which shows similarity in the fundamental features of the system such as stability and resonance.
Third, the proposed approach showed the capability to easily

improve its accuracy only through a very small changing to the generalising parameters. For instance, a small amount of tuning reaches 0.01 of the generalising parameters has achieved up to 15% improvement in the model accuracy. As such, delay calculations employing our analytical model are within 0.4ps absolute error of COMSOL-computed delay across a range of interconnect lengths.

Finally, several techniques related to the interconnect structure analysing and modelling have also been outlined in this work. The models are categorized into two main categories; the fractional order models and the integer order models. All major modelling issues and challenges are discussed for two different approaches. This research forecasts that the new on-chip interconnect modelling approach is substituting the classic modelling in the deep submicron regime.

5.2 FUTURE WORK

Concerns about the wires performance in scaled technologies has led research to explore low power communication system and other modelling methods. This section discusses possible opportunities regarding potential extensions to this work. Several research directions can be followed based on the technique and modelling proposed in this thesis.

Further investigation can carry out based on Monte Carlo simulations to study its reliability against SEU error rather than the method which has been adapted in Chapter 4. After that, a comparison for the obtained results in term of calculation time and accuracy between the two methods will be beneficial for forthcoming research.

The interconnect model employed in this thesis has considered fractional order elements for the communication link. There is still a case where the interconnects active components (CMOS circuit) can be designed to take advantage of a fractional parameter as well. In that respect, CMOS driver will be implemented considering fractional order in the form of a boosting potential. It will be advantageous to design such an interconnect structure and study its optimal performance with best fractional parameters, could accomplish.

The proposed driver scheme presents promising solutions considering ultra-low power design issues. Thus, it could be useful in sub-16nm technologies where the possible density of transistors becomes higher than their maximum density, and they are still able to be connected together by wires. However, based on the demand for high data bandwidth in the deep submicron regime, it is worthy to study the trade-off of upgrading the proposed driver circuits to transmit higher data rate with low voltage supply by incorporating additional mechanisms on the global interconnect lines. In other words, the solution is to merge the boosting approach with another low power technique to have a hyper system. Then depending on overall performance and the trade-off between the delay and energy requirements for the studied system, it could be adapted to switch on the feature of the boosting, both or either one.

One of the biggest challenge encounters the designer in ULP under DSM technologies is dealing with the stochastic error which comes from the system noise, which is inherently random. Generally, the most convenient solutions to describe this type of error is a stochastic model. Added to that, the proposed plan tackles power dissipation of interconnect circuits when voltage swing is just above the thermal noise level. Therefore, this direction will lead to encounter a noisy environment when the bit error rate is high. Accordingly, in high noise situations, more precisely in wireless communications, it is common to use signal spreading technique to address such challenges. This technique has a great advantage that is the spreading signal detectable even though it is hidden under noise. This technique is a modulation method where data is transformed into a transmission signal with a higher bandwidth. That is achieved by an encoding operation which mixes the data signal with an independent code signal. This carrier signal normally has a spectral width larger than that of the information signal to have a lower power density where the power of the original signal spreads over a much wider bandwidth. Then, observing any noticeable improvement can be achieved for bit error rate that is occurring because of noise sources.

Another challenge to consider is the power, voltage and temperature variations in electronic circuits. At sub-threshold, their unwelcome effect becomes even worse. According to this, the pro-

posed driver circuit can verify its ability to provide improvements in increasing robustness against this sort of concern as well as external disturbances and process variations, in the state-of-art applications.

Moreover, in digital systems, the coupling between signal lines, as an inherent issue causes logic failures and timing degradation, must be addressed. Hence, such problems have to consider in the interconnect modelling along with developing techniques to mitigate these issues. Automated design tools are often used to perform net reordering or buffer insertion to moderate this undesirable effect. Although the reordering and insertion solutions are effective, they are not efficient in terms of design time and power consumption. For these reasons, more efficient methodologies are required to combat crosstalk in buses. The model developed in this thesis can be extended to include parallel wires for more accurate estimation of links performance. The focusing can be on coupling and variations noise as it is the main effect of low level voltage digital circuit.

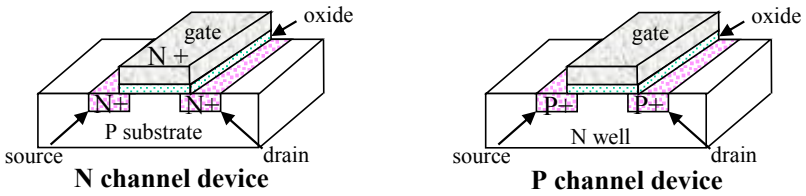
Part II

Thesis Appendices

A

DEVICES

The active part of the interconnect circuit is the driver, which is mostly considered as CMOS inverter. The MOSFET is mainly a four-terminal device, which is the basic component of CMOS. Depending on the applied voltage to the gate terminal, a current flows between the source and drain region. The fourth terminal represents the body which modulates the device parameters and characteristics [44]. There are two main types of MOSFET technology; NMOS and PMOS. The difference between these devices is that NMOS is made by diffusing N-type dopants into an P-type silicon substrate to form the drain and the source, whereas the opposite process occurs to make PMOS, as illustrated in Figures A.1a and A.1b, respectively. A combination of both P-type and N-type devices on the same silicon substrate is CMOS, as presented in Figure (**??**). The output resistance R_t of the driver can be calculated as the output resistances average of NMOS and PMOS transistors. The output resistance of the MOSFET transistor (R_t) is a nonlinear parameter of the supply voltage V_{DD}. A closed-form expression for this parameter is given in (2.43) [46].



(a) (b)

Figure A.1: MOSFET devices: (a) N-type MOSFET and (b) P-type MOSFET.

B

EXPERIMENTAL OF PARAMETERS AND TECHNOLOGY SCALING

In this thesis, the effect of interconnect was studied by considering an interconnection structure which consists of a single signal line. The top layer communication medium in the *90nm UMC* technology has been used (unless declared otherwise). Whereas the wire capacitance (C) and resistance (R) were calculated using equations (2.6), (2.9), (2.10), (2.11) and (2.1). The results in this dissertation are obtained by means of simulations employing Matlab [3], COMSOL [2], and Cadence [1] as circuit design tools. A simulation has been run to exam the assumptions made in Section (2.3) about the effects of the driver and interconnect sizing in addition to voltage scaling on the interconnect circuits performance. In order to do that, a simple circuit that could we simulate for thousands of experiments in a reasonable amount of time is required.
Therefore, we decided to run simulations on a ring oscillator. The ring oscillator is collection of an odd number of cascaded inverters, where the final inverter output feeds back into the first inverter input, and because of the odd number of inverters, the output value must be opposite to the starting input value. Since this final value connects to the inverter chain continuously, that outcomes an oscillating signal that takes a measurable time to propagate through the ring oscillator.
Accordingly, the circuit involved ring oscillator is shown in Figure (B.1), which is implemented by using Cadence/Spectre which is analogue/SPICE tool of the 90nm *UMC* CMOS process.

In the schematic of the ring oscillator, a 3-stages inverter with RC load at the middle is used as optimal to perform unbuffered interconnect circuits simulations [130]. The approach, here, has begun by setting the interconnection with 10μm length as reference then increases this length and testing the effects of changing the supply voltage and the driving circuit size.

This analysis performed by increasing the power supply of the inverter drivers from 100mV to 1V. Typically in the 90nm

technology, the supply voltage is 1-1.2V and threshold voltages are 200 and 250mV for PMOS and PMOS, respectively.
In order to exam the driver and the load effects, their value were gradually changed. Accordingly, the inverters were implemented with a sized channel width $W_n = 120\mu m$ and $W_p = 240\mu m$ to scale-up then 5 and 10 times. Simultaneously, the RC load has been increased to a maximum value that can be driven by the inverters.

Figure (B.2) shows the obtained results for varying the voltage with different size of drivers and their effect on the optimal operating frequency and the length of the interconnection that can be driven. For Figure (B.2b), the circuit operating frequency and the power supply varying are coupled where it is based on the proportional between the supply voltage and the frequency that is almost linear. On the other hand, the frequency has not increased considerably with the increase in the size of the inverters' transistors.
While the ability of the circuit to drive a specific amount of load is slightly improved with the increase in the size of inverters as shown in Figure (B.2a). Whereas the effect of increase the voltage interestingly enhances the driving capability but for a limit when the circuit frequency is appropriate with the delay effect of the interconnection.

This is in accordance with what has been mentioned in Section (2.3). While, after this limit, the wire capacitive load is the culprit for gain roll-off since, at high frequency, its reactance will be decreased and acts as a short circuit.
To sum up, the supply voltage plays a crucial role of escalat-

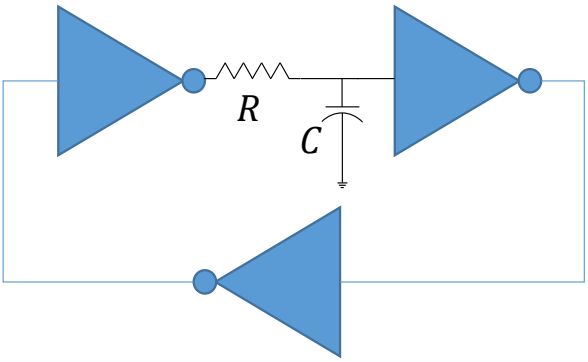
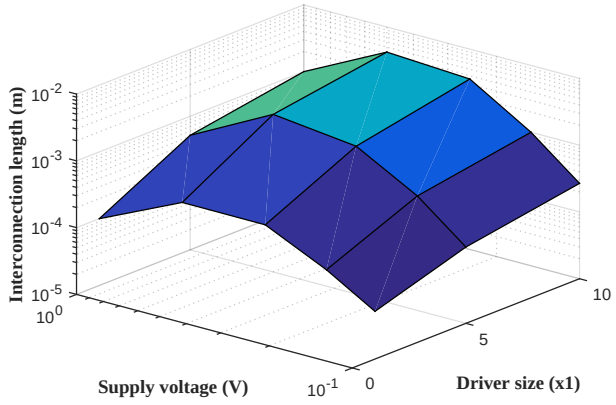
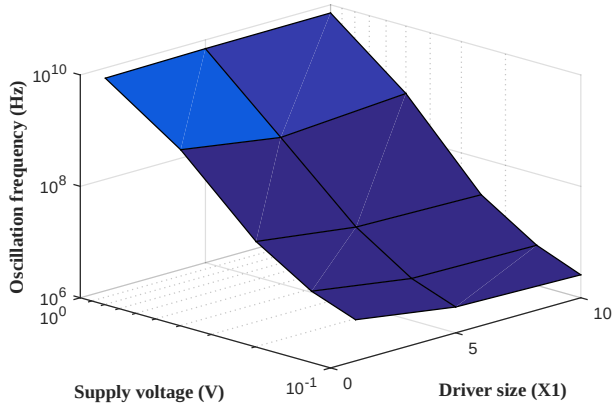


Figure B.1: Ring oscillator schematic.



(a)



(b)

Figure B.2: Impact of the supply voltage, driver size and interconnection length on the interconnect circuits performance.

ing circuit performance but not with wiring latency inflating. The driver size increase shows inconsiderable influence on the circuit operating frequency; however its ability to drive long connection has improved. This analysis shows clearly the biggest challenge of on-chip interconnect design where the delay of the interconnection dominates on top of all other delays.

Part III

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