Switching Transients Optimization and Investigations into Threshold Voltage Shift for SiC MOSFETs using a Current-Controlled Gate Driver

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Abstract

Silicon Carbide Metal-Oxide Semiconductor Field Effect Transistors (SiC MOSFET) show superior properties over conventional silicon (Si) based MOSFETs: featuring higher voltage and temperature operation, low on-resistance and faster switching speed. These characteristics facilitate higher efficiency, power density and arguably better reliability. However, the mainstream commercial SiC MOSFETs are often fitted to the packages that are previously designed for Si-based devices, introducing significant oscillation during the turn-on and turn-off periods. Moreover, oxidation in the gate oxide introduces defects, resulting in a more fragile gate oxide compared to Si MOSFETs . Oxidation introduces the shift of the threshold voltage (V_{th}), which remains a concern for the consumers of SiC MOSFETs.

This thesis investigates the causes of oscillations and causes of the oxidation and proposes methods to minimize their impact on the devices. A detailed analysis on switching transients is presented using a small signal model for every stage in voltage and current changes during the turn-on and turn-off periods. This analysis provides guidance for the design of optimized gate driving signals. The benefits of these gate driving signals are compared with conventional turn-on and turn-off signals and results show that the proposed new signals provide lower voltage and current overshoots and lower losses. For the investigation into V_{th} shift, the phenomenon of V_{th} shift in short gate stress time and long gate stress time is discussed. The gate driver developed to limit oscillations is altered by embedding a new way in measuring V_{th} shift. This allows to receive feedback from the gate oxide degradation. In addition, the same measuring circuit can be used to measure the SiC chip temperature. Thus, the proposed technique can be also be used as a temperature sensitive electrical parameter (TSEP).

COVID-19 Impact Statement

The following parts of this work is disrupted as a result of Covid-19 restrictions:

- Construction of 3rd version gate driver. The pandemic occurred before the design of the 3rd version gate driver, which would provide better performance. Therefore, all the experiments are conducted with the 2nd version gate driver. The output current of the gate driver is limited to 200mA, and time resolution of the gate driver is limited to 13ns. These limitation of the gate driver result in the slow speed in the experiments.
- More experiments under different voltages, currents and temperatures. The plan was to conduct experiments under different test conditions in Chapter 4, which can make the results more convincible. However, the experiment schedule was delayed due to Covid-19 restrictions. Therefore, the thesis only includes experiment results at 250V/10A/25ºC.

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List of Abbreviations

AGD	Active Gate Driver
BPD	Basal Plane Dislocations
BTI	Bias-Temperature Instability
CGD	Conventional Gate Driver
DAC	Digital-to-analog Converter
DSP	Digital Signal Processor
EMI	Electro-Magnetic Interference
ESL	Equivalent Serial Inductance
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GPIO	General-Purpose Input/Output
GTO	Gate Turn-off Thyristor
HTRB	High Temperature Reverse Bias
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
IH	Induction Heating
JFET	Junction Field Effect Transistor
JJE	Jing-Jin Electric
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
SBD	Schottky Barrier Diodes

SCWT	Short-Circuit Withstand Time
SF	Stacking Faults
SiC	Silicon Carbide
SPI	Serial Peripheral Interface
SST	Solid State Transformer
TDDB	Time-Dependent Dielectric Breakdown
TED	Threading Edge Dislocations
TSEP	Thermal Sensitive Electrical Parameter
UPS	Uninterrupted Power Supply
WBG	Wide Bandgap

List of Symbols

C_{DC}	DC Capacitor
C_{Diode}	Diode Cacpacitance
C_{DS}	Drain-Source Capacitance
C_{GD}	Gate-Drain Capacitance
C_{GS}	Gate-Source Capacitance
dI_{DS}/dt	Current Slew Rate
ε_S	Relative Dielectric Constant
E_B	Breakdown Field
E_G	Energy Gap
I_C	Collector Current
I_D	Drain Current
i_{driver}	Output Current of Gate Driver
I_F	Forward Current
I_{gs}	Gate-Source Current
L_p	Parasitic Inductance
L_S	Common Source Inductance
R_g	Gate Resistor
$R_{g,int}$	Internal Gate Resistor
R_{on}	On-state resistance
t_{doff}	Turn-off Delay Time

t_{don}	Turn-on Delay Time
μ_n	Electron Mobility
μ_p	Hole Mobility
v_{driver}	Output Voltage of Gate Driver
V_f	Forward Voltage
V_{goff}	Off-state Gate Voltage
V_{gon}	On-state Gate Voltage
V_{gs}	Gate-Source Voltage
V_{in_SS}	Steady State Input Voltage
V_{in_ST}	Swiching Transient Input Voltage
V_{Miller}	Miller Voltage
V_{on}	On-state Voltage
V_{out}	Output Voltage
$V_{pre\text{-}th}$	Pre-Threshold Voltage
$V_{quasi\text{-}th}$	Quasi-Threshold Voltage
v_s	Saturation Drift Velocity
V_{th}	Threshold Voltage

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Chapter 1 Introduction

Power electronics technologies serve a critical role in alleviating energy problems[1]–[3], including air pollution[4], global warming[5] and fossil fuel shortage[6]. As the key components in power electronics systems, the development of semiconductor devices has significant influence on the overall performance of power electronics systems[7]. In general, the efficiency of power electronics is mainly limited by the performance of semiconductor devices[8]. Si (Silicon) technology has been developed for decades, and the Si-based devices are regarded as approaching their performance limitations[9]–[12]. Therefore, increasing attention is attracted by materials with better properties. SiC (Silicon Carbide) is one of the most promising materials[13]–[20].

1.1. Comparison of Si and SiC

Silicon-based power devices have played a dominant role in power electronics for decades due to its easy availability and low cost[21]. In the voltage range <200V, Si MOSFET (Silicon Metal-Oxide-Semiconductor Field Effect Transistor) is the first choice with its mature trench technologies[22], leading to a reduction of the on-state resistance R_{on}[23]. For higher voltage levels of 600V and 900V, the introduction of superjunction technology is able to reduce the R_{on} in MOSFETs even further at high voltage[23]. However, the technological complexity of power switching devices increases at higher voltage levels. Consequently, higher voltage power devices (1.2kV, 1.7kV, 3.3kV and 6.5kV) are dominated by bipolar devices, such as IGBT (Insulated Gate Bipolar Translator), IGCT (Integrated Gate Commutated Thyristor) and GTO (Gate Turn-off Thyristor). Even with these advancements, Si exhibits some noticeable limitations regarding blocking voltage capability, switching frequency and operating temperature[15], [24], [25]. Nowadays, the typical operating frequency of IGBTs is in the range of 1 – 20kHz[23]; the highest breakdown voltage capability of commercial Si IGBTs is 6.5kV[15]; there is no Si-based device that operates above 200°C[24]. These physical material properties limit the performance of Si-based power converters, resulting in the demand for new materials[24].

SiC material demonstrates superior theoretical characteristics over Si, providing the potential to equip power converters with high blocking voltage capability, high switching frequency and high operating temperature devices. Moreover, SiC is the only compound semiconductor that can be thermally oxidized to form high-quality SiO_2[26], which provides SiC with higher maturity of technological processes for high voltage application compared to other WBG (Wideband Gap) materials like GaN (Gallium Nitride) or GaAs (Gallium Arsenide)[24].

The physical properties of SiC vary with its "polytypes" or crystal structures[26][27]. It is recognized that SiC crystallizes in more than 200 different polytypes, among which the technologically important ones are 3C-SiC, 4H-SiC and 6H-SiC[26]. Presently, 4H-SiC is generally preferred in practical power device manufacture[28]. The typical properties of SiC(4H) are compared with Si[28] in Table 1-1.

Table 1-1 Typical properties of SiC and Si[28]

Properties	**Si**	**SiC(4H)**
Crystal Structure	Diamond	Hexagonal
Energy Gap: E_G (eV)	1.12	3.26
Electron Mobility: μ_n (cm^2/Vs)	1400	900
Hole Mobility: μ_p (cm^2/Vs)	600	100
Breakdown Field: E_B(V/cm) $\times 10^6$	0.3	3.0
Thermal Conductivity (W/cm °C)	1.5	4.9
Saturation Drift Velocity: v_s (cm/s) $\times 10^7$	1.0	2.7
Relative Dielectric Constant: ε_S	11.8	9.7

Table 1-1 shows that, compared to Si, SiC has ten times the dielectric breakdown field strength, three times the bandgap and three times the thermal conductivity. Moreover, both p-type and n-type regions, which are essential for device structures in the semiconductor materials, can be formed in SiC[28]. Therefore, on account of its high efficiency, low power dissipation, reduced chip sizes and possibility to use an easy cooling system[26], SiC power device is predicted to overtake present-day Si power devices, mainly Si-IGBT.

1.2. Application of SiC Devices

Owing to the development of the epitaxial growth of SiC[29], SiC devices have experienced a

rapid growth in both fabrication technologies and market share[17], [30]. The first WBG device, 600V SiC SBDs (Schottky Barrier Diodes) from CREE[31], became commercially available in year 2002, followed by higher voltage SiC SBDs products at 1200V in year 2006 and 1700V in 2010[31]. The main advantage of SiC SBDs is the high switching frequency brought about by the absence of reverse recovery current, making it possible to significantly reduce the volume, weight and cost for the system[20]. Meanwhile, the first SiC MOSFET is announced in 2011 from CREE, rated to 1200V; SiC JFETs (Junction Field Effect Transistor) have been available since 2011 from SemiSouth; 1200V SiC BJTs (Bipolar Junction Transistor) are released in autumn 2013 from Fairchild; 6.5kV/80A thyristors came into market from GeneSiC[31]. The strong momentum of SiC technology development introduces a dramatic increase of up to 39% in the market share of SiC devices every year since 2010[32]. The applications of SiC devices range from low power IT & consumer applications like home appliances to high power applications like power grid and rail transport.

1.2.1. Home Appliance

SiC technologies are not very far from our daily life. Instead, they have improved the user experience of the home appliances that are used every day. Si-based devices already have a dominant market share because of the reasonable price of devices in 600V class, which are frequently used for home appliances. However, the high frequency of SiC-based devices demonstrates strong advantages in smooth wave modulations without distortion and in reducing inductor size. Mitsubishi announced in 2010 hybrid SiC SBDs with Si-IGBTs in the inverter system of their air conditioners[26]. In 2014, SiC MOSFETs were introduced by Mitsubishi to DC converters in their air conditioners, ensuring 45% loss reduction[33]. Apart from the application in air conditioners, SiC presents better performance in IH (Induction Heating) system than Si with its favourable features of high temperature, high frequency and high voltage[34][35]. In fact, the introduction of SiC devices foresees a major revolution in IH technology[36], enabling a new design paradigm with improved levels of efficiency and performance. It is also confirmed in [37] that SiC MOSFETs can be used in induction heating inverters and provide greater efficiency than when using Si MOSFET.

1.2.2. UPS

The demand of UPS (Uninterrupted Power Supply) has been increasing along with the development of data centres. As it is typically housed in an office building, factory building or data centre, a UPS with high-power-density system is highly desirable. In addition, high efficiency and high power quality are also the main drives for innovation in UPS systems[17]. These demands make SiC devices stand out from their Si counterparts. The full-SiC UPS rating at 500kW was announced in 2015 by Toshiba, showing 17% smaller footprint and 18% lighter than its predecessor[17]. Moreover, the conversion loss was reduced by nearly 50%, delivering 98% efficiency over wide load range. Meanwhile, it is reported that a two-level SiC UPS is demonstrated to achieve 97.6% efficiency with 32kHz switching frequency, compared with 96% efficiency in a three-level Si UPS with 16kHz switching frequency[38]. An increasing number of manufactures, such as Mitsubishi, Siemens, and GE, have been attempted to develop UPS with high power rating products using SiC devices.

1.2.3. Electric Vehicle

The most important requirement for power electronics circuits in EVs (Electric Vehicles) is high power density[17], which can be achieved by a transition from Si-based devices to SiC-based devices. It is estimated that the size of the power control unit in an EV can be reduced by 80% with all-SiC devices replacing Si devices[17]. In addition to the high-power-density, the high efficiency and high temperature characteristics of SiC also attract the attention of EV designers. The experimental results from Ford Motor Company illustrate 40% reduction in switching losses by using SiC MOSFET instead of Si IGBT[39]. Meanwhile, the performance of SiC devices remains high at extreme junction temperature of 225^{o}C[40], showing advantage in its lower requirement for large cooling system. As the cost of SiC devices decreases, more and more EV manufacturers will start using SiC MOSFETs as the motor controller in their products[40]: Tesla grouped 24 SiC MOSFET chips on a pin-fin radiator in parallel to achieve a high efficiency inverter with high current output; double-sided welding and double-sided cooling technology were adopted by Denso to pursue small size and high efficiency in its SiC controller; Jing-Jin Electric (JJE) developed high-power-density SiC MOSFET controller up to

40kW/L for VW commercial vehicles; BYD also equipped its EV-HAN serials with full-SiC inverters in July 2020. It was found by Toyota that, under load conditions, the loss of SiC power control unit of the prototype vehicle was reduced by 30% compared with Si IGBT power control unit.

1.2.4. Rail Traction

For rail traction application, SiC devices bring not only the improvement in efficiency, but also revolution in structures and topologies. Traditionally, a three-level topology is preferable because of the limited switching frequency capability of Si IGBTs[26]. With their superior performance of high voltage rating and high frequency, SiC devices are suitable for two-level traction drive system with high efficiency and compact size. Japan is ahead of the world in developing SiC technologies in rail traction application. Hitachi developed a two-level traction drive system with a compact 3.3kV/1.2kA Si IGBT/SiC SBD hybrid module[41]. It is reported that the size of the hybrid module was reduced by 1/3 compared with a conventional IGBT module, while the weight and volume of the new traction inverter are reduced by up to 40%. In addition to the size, the total loss of the inverter decreases up to 35%. Mitsubishi developed a 3.3kV/1.5kA module for all-SiC traction inverters, reducing the size by 55% and the weight 35%[17]. Moreover, owing to the high performance of SiC power devices, transformers could be made compact, and in the motor winding system a change could be made from 4 to 6 poles, leading to a traction system with high efficiency and compact size[26]. Eventually, a weight reduction by 11 tons for 1 train with 16 cars was announced[26].

1.2.5. Aircraft

SiC devices are extremely attractive for electric aircraft application due to the strict requirements of volume and weight. More and more studies are conducted to increase the power density of aircraft converters[42]. A 50-kW SiC two-level three-phase voltage source inverter is demonstrated with a gravimetric power density of 26 kW/kg[43], whose measured efficiency reaches up to 97.91% at 100kHz switching frequency. A German research organization, Fraunhofer, developed a six-phase inverter system with high efficiency of over 98%[44]. Except full electric aircraft, SiC is also deployed in fuel-cell and battery-based hybrid drive for

aircraft[45], showing 99.2% efficiency at 100kHz switching frequency.

1.2.6. Solar Inverter

The development of solar inverter is supported not only by the pursuit of high efficiency but also of high density, especially for rooftop application. However, the desirable weight density, e.g. 1kW/kg, cannot be achieved by most of the commercial products with Si IGBTs, as their weight density is less than 0.38kW/kg[17]. A highly efficient and compact 50kW grid tied solar inverter was developed with Gen2 family of SiC power MOSFET devices[46]. The 50kW interleaved boost circuit is only 7kg, while its peak efficiency reaches 99.4% at 75kHz. High efficiency is also achieved in higher power inverters with SiC devices. A 1-MW solar power inverter was developed with all SiC power modules, whose measured efficiency at the rated output power ranges from 98% to 98.6% depending on the values of DC input voltage[47]. In addition to researches, SiC-based solar inverters are also commercialized by manufacturers like GE[17].

1.2.7. Wind Turbine

The power semiconductor is the backbone of the wind power converter and is also influential for many critical performances, such as cost, efficiency, reliability and modularity[48]. The superior properties of SiC enable its capability of fast switching as well as high power handling for wind turbine applications. A quantitative study shows that SiC MOSFET outperforms Si IGBT over all switching frequency, while the advantages of SiC are more pronounced at higher frequency[49]. Meanwhile, an economic evaluation of SiC MOSFET in wind turbine converters illustrates that the use of SiC modules introduces better ecomonical resutls at the weak-wind site[50]. The reason is the lower conduction losses of SiC-modules than Si-modules when the wind speed is slower than 10m/s. Moreover, the high frequency of SiC devices leads to the optimization of filters and heat-sink, enabling up to 37.8% increase in inverter power density, while the high efficiency of SiC devices saves up to 42.7% of the lost energy per year[51].

1.2.8. Power System

Nowadays, a huge number of power converters, mainly Si-IGBTs, are used in power system.

When SiC power devices are able to replace Si-IGBTs, low-loss and compact systems will be realized. It is illustrated in [18] that a MV-scale grid-connected interface converter is developed with 10 kV SiC MOSFETs for 12.4 kV AC disctribution grid. By replacing the line-frequency transformer in conventional Si-based solution with the high-frequency transformer in SiC-based solution, the passive reduction is achieved. Eventually, the power density is improved. GE develops a SiC-based SST (solid state transformer) with its power rating at 1MVA[18]. SiC MOSFET modules are used in the SST, switching at the frequency of 20kHz. The weight of the SST is 800kg, about 1/3 of a conventional transformer, while the volume is reduced by approximately 50%. Apart from the power density, SiC attracts attention in high voltage application like the circuit breaker. A single 15kV SiC ETO (Emitter turn-off thyristor) is developed for medium voltage applications to provide ultra-fast protection with the capability to turn off more than 125A at 6kV without a snubber[45]. In addition, the high switching frequency introduced by SiC devices enables new grid functions, such as operating as active power filter, to improve power quality and stabilizer to enhance system stability[18].

1.3. Challenges of SiC Devices

Although SiC devices are substituting Si at an increasing number of aspects in power electronics, there are still challenges impeding SiC devices' growth in market share. Special considerations need to be taken into account in order to utilize SiC devices efficiently and reliably[18]. In this section, several typical topics are dicussed. These challenges can be classified into 2 categories: the challenges caused by the fast switching speed and the challenges resulted from material manufacturing. It worth noting that there are other issues introduced by temperature, voltage and current, but these challenges are not the focuses of this work.

1.3.1. Challenges Introduced by High Speed

Every coin has two sides. The high speed of SiC devices brings about not only the benefits, but also challenges. These challenges introduced by high speed exist at both component level and system level[52]. At component level, the challenges include oscillations, crosstalk effect and EMI. At system level, the high switching frequency leads to the difficulties in dead time setting, high bandwidth control and measurement.

A. *Oscillations and EMI*

There is a trade-off between switching loss and switching oscillation for Si devices in practical applications, as higher switching speed introduces higher voltage and current slew rates. The trade-off also applies to SiC devices, while oscillations are even higher due to the capability of SiC devices to operate at much higher frequencies. Sometimes, the introduced oscillation current is so high that it reaches up to twice the value of the load current[52]. Furthermore, ringing can create harmonic spikes in the EMI spectrum. The increased switching speed directly results in higher harmonic contents at MHz+ frequencies due to higher voltage/current slew rate. It is illustrated that once the switching frequency is doubled from 20kHz to 40kHz, the harmonics increase in both the switching frequency region (kHz) and MHz+ region over the whole frequency range.

B. *Crosstalk*

Crosstalk effect is the interaction between two switches in the phase-leg structure, where the switching transient of one device will affect the operating behaviours of its complementary device. Crosstalk effect is introduced by the voltage slew rate and the Miller capacitance[53]. The high voltage slew rate of SiC devices makes the crosstalk effect more severe than Si devices, which may introduce parasitic turn-on and lead to a shoot-through failure[54]. Similar to the crosstalk during turn-on transient, when the device is turned off, it may cause negative gate voltage spike on the complementary device. The negative gate voltage spike may exceed the minimum allowable gate voltage at high switching speed, which affects the gate reliability of the device[54].

C. *Deadtime*

The deadtime is used to prevent shoot through in phase-leg structure converters. The use of deadtime may cause low-frequency harmonics, voltage drop and additional losses. These effects become more severe under higher switching frequency. Furthermore, due to the high switching speed of SiC devices, the duration of deadtime should be set much smaller than needed for Si devices[52].

D. Control and Measurement

The switching frequency is an important factor for the bandwidth of control and measurement, especially for accurate feedback control. When high switching speed SiC devices are utilized in the converters, there is concern about whether the mature control algorithm can still be completed within each short switching period[52]. If the control needs to be implemented within each period, high frequency means the high requirement for reduction in delays, such as processor calculation time, sampling time, PWM delay, etc.

1.3.2. Challenges Introduced by Material Properties

The aforementioned challenges in subsection 1.3.1 are general ones, which also apply to Si devices, but become more severe for SiC devices due to their higher switching speed. In this subsection, the challenges presented are unique for SiC material.

A. V_{th} Shift

BTI (Bias-Temperature Instability) describes the phenomenon that V_{th} (Threshold Voltage) of a SiC MOSFET shifts as a result of bias and temperature stress[55]. It is widely regarded as the most important reliability issue for the development of SiC technology[26]. The mechanism of BTI is generally accepted as the gate charges trapped by the gate oxide defects[56]. Compared with traditional Si materials, due to the additional presence of carbon, the SiC thermal oxidation process is highly complicated[57]. Thermal oxidation in wet or dry atmospheres results in residual carbon in the oxide layer and carbon clusters at the SiO_2/SiC interface[26]. The interface density is dominated by carbon-cluster related centers, responsible for the charge trap phenomenon, which eventually results in the shift of V_{th}.

V_{th} shift introduces various problems: if V_{th} shifts in the positive direction, it might increase on-state resistance; similarly, if V_{th} shifts in negative direction, an undesired leakage current might be introduced. To compensate the effect of the V_{th} shift, SiC MOSFETs often switch over a voltage range much higher than the datasheet threshold voltage limits[55]. For example, the Wolfspeed C2M0080120D commercial MOSFET datasheet quotes a gate threshold voltage ranging from 2.0 V to 4.0 V. Meanwhile, the recommended gate voltage range is -5V to 20V,

which is much higher than the range of its threshold voltage[55]. As a comparison, one of the Si counterparts for SiC MOSFETs, CoolMOS IPD70R360P7S from Infineon, has a recommanded gate voltage range from 0V to 10V, less than half of the range of the aforementioned SiC MOSFET (-5V to 20V). This wide range of a SiC MOSFET suggests that the threshold voltage can vary quite a bit before its effect can be seen in a switching application[55]. Therefore, the manufacturers declares that the SiC devices are stable if they are operating under the recommanded gate conditions. However, these shifts may result in other issues, for example, the unbalanced current sharing for paralleled applications[58], the system error for the junction temperature evaluation using V_{th} as a TSEP[26], even device failure when the increase is large enough[58].

B. TDDB (Time-Dependent Dielectric Breakdown)

Different from BTI, which is not an issue for Si devices due to the absence of carbide cluster, TDDB for Si MOSFETs is arguably one of the most well characterized and cited failure mechanisms[55]. TDDB describes the polarization of dielectric under gate electric field. The polarization will increase with electric field until dielectric breakdown occurs[59]. Voluminous publications have yielded very comprehensive guidelines and standards across all standards bodies[55]. Although the literature is based on Si MOSFETs, the widely-used linear-E model is also applied to SiC MOSFETs[60][61]. The results show that the Si TDDB model[62] can be applied to Wolfspeed Gen2 MOSFETs (C2M0080120D) to predict the lifetime[61]. It is claimed that only minor modifications are needed to accommodate SiC with reference to existing Si documents[55].

C. HTRB (High Temperature Reverse Bias)

HTRB is used to evaluate the high-field reliability of blocking high voltage. Fields are high in the drift region, in some gate oxide regions, and in the device termination region at the device periphery[61], resulting in a wear-out failure over long stress times. HTRB tests are performed with drain bias higher than the maximum recommended operating voltage yet below the avalanche voltage[60]. The experimental results show that post-stress electrical testing of failed devices presents leaky or shorted gate oxide, but the devices still block voltage with low

leakage[60]. This proves that HTRB failures occur in the gate oxide, similar to TDDB. The failure is introduced by the high gate oxide electric fields in the JFET region as a result of high drain bias. Therefore, the linear-E model can also be used to estimate the operating life of SiC MOSFETs.

D. V_f Drift (Forward Voltage Instability)

V_f drift is the phenomenon that the forward voltage of SiC device increases after conducting constant current for a long time[63]. The fundamental cause of V_f drift is widely believed to be the expansion of basal plane dislocations (BPD) into Shockley Stacking Faults (SFs) within device regions that experience conductivity modulation[63]. It is important to note that the observed initial BPD (Basal Plane Dislocations) density is closely related with the epitaxy processing: normal fabrication and handling operations can damage the semiconductor and inject dislocations that can nucleate SFs; growth interruptions can leave a legacy of BPDs at the interfaces[55]. Improvements in manufacturing process have reduced V_f drift significantly to impede the propagation of BPDs into epilayers by preferentially converting BPDs into TEDs (Threading Edge Dislocations) during the initial stages of epilayer growth[55]. As a recent experiment shows, the V_f drift is negligible in medium voltage MOSFET body diode[64].

E. Short-Circuit Ruggedness

The short-circuit ruggedness of power devices is usually represented by the SCWT (Short-Circuit Withstand Time). Typically, Si IGBTs have SCWT of around 10us. This gives sufficient time for over-current detection and protection circuit to turn-off the Si IGBTs[52]. However, due to a smaller chip area, the SCWT for SiC device is much less than their Si counterparts[65]. The short-circuit failure mechanisms of SiC MOSFETs can be thermal generation current induced thermal runaway or high-temperature-related gate oxide damage[66]. During short-circuit (shoot-through) failure, the SiC MOSFET current rise rapidly and the device voltage drop will clearly increase as well. Therefore, the widely used desaturation protection method based on the measurement of MOSFET voltage drop can be applied[52]. Nowadays, fast protection for SiC devices is commercialized on gate driver with activation time less than 2us.

1.4. Motivation and Contribution

Although there are different types of SiC switches, such as JFETs and BJTs, the most popular SiC switch is the MOSFET[17]. SiC MOSFET offers the most desirable features in terms of device performance from a user's perspective[67], including normally-off operation, low conduction loss, low gate charge and low turn-off loss due to the absence of bipolar current tail. Therefore, SiC MOSFET is selected as the research subject in this project to address two major challenges that occur with the device. The two challenges studied are: switching oscillation and V_{th} shift. Despite the fact that structures SiC MOSFETs are different among the manufacturers[68], all SiC MOSFETs suffering from switching oscillation and V_{th} shift. The targets of this project are to reduce the switching oscillation and to detect V_{th} shift. Reducing switching oscillation helps to realize the potential of the high speed of SiC MOSFETs, while detecting the V_{th} shift indicates the health condition of the gate oxide.

The contribution of the project includes the following aspects. Firstly, an active gate driver is designed for SiC MOSFETs with the feature of flexible gate current control. The gate driver serves as the key tool to achieve the goals of reducing switching oscillation and detecting V_{th} shift. Then, the switching transients in both turn-on and turn-off periods are analyzed, before the small signal models of SiC MOSFETs in each detailed switching periods are proposed. Based on the models, the optimized gate current signals are proposed to improve the switching performance of SiC MOSFETs. The effectiveness of the proposed gate current signals is verified in experiments using the active gate driver. The active gate driver is also used in detecting V_{th} shift: a novel method is proposed to detect the value of the V_{th}, in addition, extract the V_{th} shift by decoupling the impact of temperature. With the proposed method, the relation of V_{th} shift and gate stress time is investigated, and a multi-layer trap model is proposed to describe the V_{th} shift over time. Finally, the possible applications of the proposed V_{th} shift detecting method are studied in simulation.

1.4.1. Publications

A. Publications based on this project

1. Wang, X., Wu, H., & Pickert, V. (2021). Phenomenon of Short-Time Threshold Voltage Shift

and Its Application in Junction Temperature Estimation. In *the 1st IEEE International Power Electronics and Application Symposium (IEEE PEAS'2021)*. Accepted.

2. Wang, X., Wu, H., & Pickert, V. (2021). Gate threshold voltage measurement method for Sic MOSFET with current-source gate driver. In *the 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)*(pp. 443 – 447). IET

3. Gonzalez, J. O., Wu, R., Wu, H., Wang, X., Pickert, V., Mawby, P., & Alatise, O. (2021). Optimisation of the Gate Voltage in SiC MOSFETs: Efficiency vs Reliability. In *the 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)* (pp. 820 – 825). IET

4. Wu, H., Wang, X., Ortiz-Gonzalez, J., Alatise, O., & Pickert, V. (2021). Investigation into the Switching Transient of SiC MOSFET Using Voltage/Current Source Gate Driver. In *the 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)* (pp. 657 – 662). IET

5. Wang, X., Wu, H., & Pickert, V. (2020). A cost-efficient Current-Source Gate Driver for SiC MOSFET Module and its Comparison with Voltage-Source Gate Driver. In *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)* (pp. 979-984). IEEE.

6. Zhang, W., Wang, X., Dahidah, M. S., Thompson, G. N., Pickert, V., & Elgendy, M. A. (2020). An Investigation of Gate Voltage Oscillation and Its Suppression for SiC MOSFET. *IEEE Access*, *8*, 127781-127788.

7. Wang, X., Wu, H., & Pickert, V. (2019, March). Design of an advanced programmable current-source gate driver for dynamic control of SiC device. In *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)* (pp. 1370-1374). IEEE.

B. Publications based on other projects

1. Lu, X., Pickert, V., Al-Greer, M., Chen, C., Wang, X., & Tsimenidis, C. (2021). Temperature Estimation of SiC Power Devices Using High Frequency Chirp Signals. *Energies*, 14(16), 4912.

2. Wu, H., Gu, B., Wang, X., Pickert, V., & Ji, B. (2019). Design and control of a bidirectional wireless charging system using GaN devices. In *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)* (pp. 864-869). IEEE.

3. Wu, H., Wang, X., Gu, B., & Pickert, V. (2019). Investigation of a GaN-based Bidirectional Wireless Power Converter using resonant inductive coupling. In *2019 IEEE Wireless Power Transfer Conference (WPTC)* (pp. 263-268). IEEE.

Chapter 2 Literature Review

2.1. Switching Oscillation Suppression Methods

Although the fast switching speed of SiC MOSFET allows it to operate at high frequency, the oscillation in the switching transient introduces reliability concerns. In many reported works[69]–[72] using SiC MOSFET, large overshoot or high frequency oscillation often arises in current and voltage waveforms, which may generate EMI and bring reliability problems. Therefore, various suppression methods are investigated to reduce the switching oscillation.

The mechanism of switching oscillation is generally regarded as the energy release of parasitic inductance and capacitance introduced by high current and voltage slew rate. Fig. 2-1 shows the typical switching power circuit with parasitic parameters. The power circuit consists of a MOSFET as the switching device, a diode as the top device, a DC capacitor as the energy source and an inductor as the load. A gate driver with the gate resistor R_g is used to control the turn-on and turn-off speed of the MOSFET. The parasitic parameters are shown in red, where L_p is the total parasitic inductance in the power loop, including the ESL (Equivalent Serial Inductance) of C_{DC}; C_{Diode} is the junction capacitance of the diode; C_{DS}, C_{GS}, C_{GD} are the parasitic capacitance of the MOSFET; L_S is the common source inductance of the MOSFET. The switching oscillation occurs when the current is transferred between the MOSFET and the diode, introducing energy exchange between the stray inductors and the parasitic capacitances.

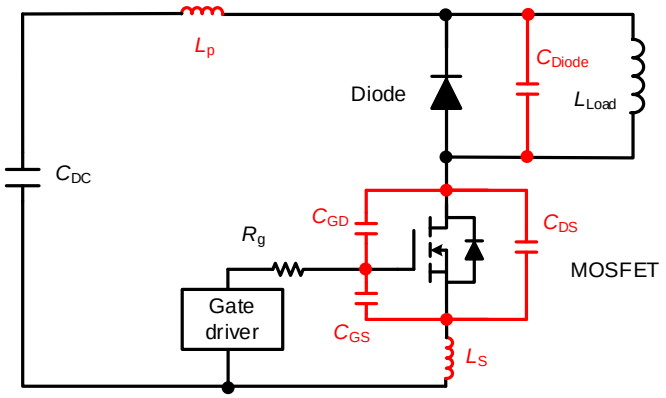


Fig. 2-1 Typical switching power circuit with parasitic parameters

In order to reduce the oscillation, there are various methods proposed from different aspects.

The most direct way is to reduce the parasitic parameters. The oscillation is highly influenced by the parasitic inductance, which can be optimized by the improvement of power circuit integration. Another method is to use snubber circuit added to the power loop to absorb the energy stored in the parasitic inductances or capacitances without influencing the normal operation. The last approach is to reduce the high switching speed of the MOSFET with active gate driver. All three methods are reviewed in this section.

2.1.1. Reducing Parasitic Parameters

The commercialization of TO-247-4L package shows the effort to improve the switching performance of power device by reducing L_S. Many manufacturers have provided products with additional signal source terminal for gate driver, including Wolfspeed, Infineon, Toshiba and so on. As an example of TO-247-4L, TK62Z60X from Toshiba is tested using the power circuit shown in Fig. 2-1, compared with its 3-pin counterpart TK62N60X. The result shows that the turn-on loss is reduced by 19%[73].

Based on the same concept to reduce the parasitic parameters, optimized designs are proposed with more impact circuits for SiC MOSFET modules[74][75]. It is demonstrated in [75] that the design optimizations on layout, chip placement and terminal structure lead to significant reduction of parasitic inductance in both power loop and gate loop. Compared with the commercial package, the proposed design has 96% lower power loop inductance and 76% lower gate loop inductance, bringing 44% less total switching loss and 54% less voltage overshoot at 400V/300A operating condition.

There are other publications presenting optimized designs of the power circuit with less parasitic inductance[69]–[72]. Although this method is effective in improving the performance of the power device, modifications on power circuit are required to apply this method to existing power converters.

2.1.2. Snubber Circuit

A snubber circuit is widely used as the energy-absorbing circuit to suppress the voltage spikes caused by inductance. However, detailed oscillation parameters are required for the design of

the snubber circuit. Therefore, it had not been used in SiC MOSFET circuit until the equivalent circuit models are developed incorporating all parasitic elements in [76]. The switching oscillation phenomenon is analyzed with simplified mathematical formulas, providing the guideline for snubber circuit design. Under the guideline of the models, as shown in Fig. 2-2, a RC snubber is designed to reduce the oscillation, showing a more moderate current oscillation during turn-on and a 22.72% reduction in voltage overshoot during turn-off.

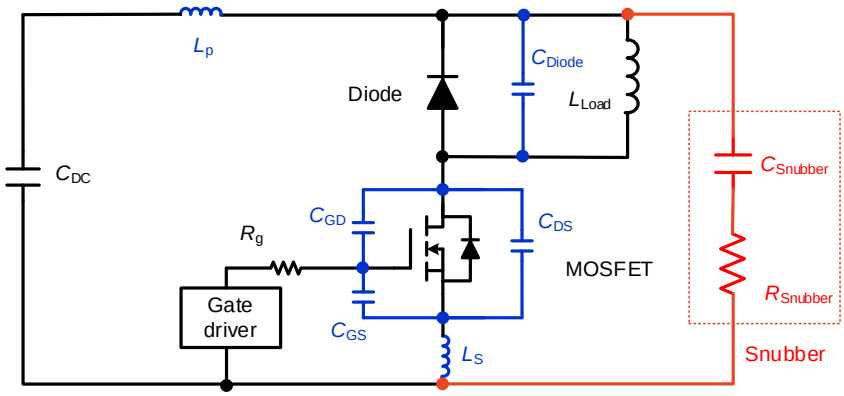


Fig. 2-2 Application of snubber circuit to reduce switching oscillation[76]

Apart from the paralleled snubber circuit, the serial connected snubber circuit (Ferrite Bead) can also be used to reduce the oscillation[77], as shown in Fig.2-3. With the oscillation models, the parameters of a Ferrite Bead are selected to damp the oscillation. It can be seen from the results that with a Ferrite Bead as the snubber of the circuit, the MOSFET shows reduced oscillation than the circuit without a snubber.

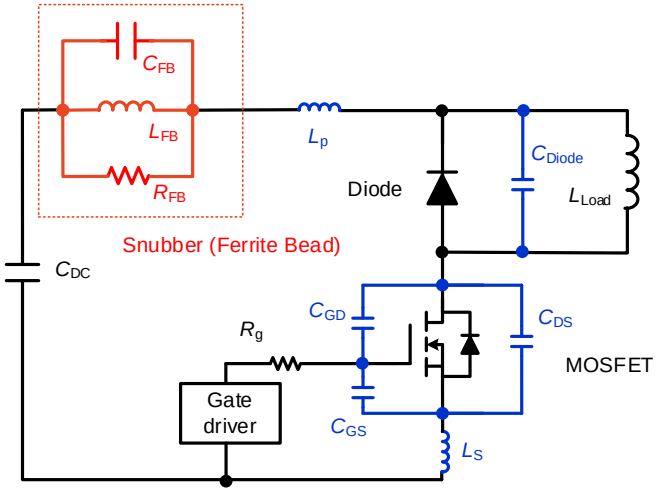


Fig. 2-3 Equivalent circuit of the power circuit with Ferrite Bead as the snubber circuit[77]

The method of adding snubber circuit to damp the oscillation demonstrates effectiveness in reducing the oscillation. However, this method has some inescapable drawbacks. As a method to reduce the parasitic inductance, hardware modifications are required to change the resonant circuit. Moreover, the parameters of the snubber need to be selected based on the switching models of the turn-on and turn-off circuit, increasing the complexity in practice.

2.1.3. Active Gate Driving Method

Different from the aforementioned two methods placed in the power loop, active gate driving method focuses more on the control of the SiC MOSFET. As the control unit for the SiC MOSFET, active gate driver is the key to the approach to reduce oscillation. Considering that the voltage and current slew rates of the SiC MOSFETs are controlled by the gate driver, there are various active gate driver designed aiming at the control of switching speed during the switching transient. Generally, there are three strategies to control the switching speed of SiC MOSFET: variable gate resistance control, multi-step gate voltage control and additional gate current control. The active gate drivers of these three strategies are reviewed in this subsection.

A. Variable Gate Resistance Control

The working principle of variable gate resistance control is straightforward: by adjusting the gate resistance in the different switching periods, the voltage and current slew rate can be changed. The main advantages of the variable gate resistance control are the low cost and easy implementation, making it the most widely used approach to switching speed control[78]. A typical concept of an active gate driver with the variable gate resistance control is demonstrated in Fig. 2-4.

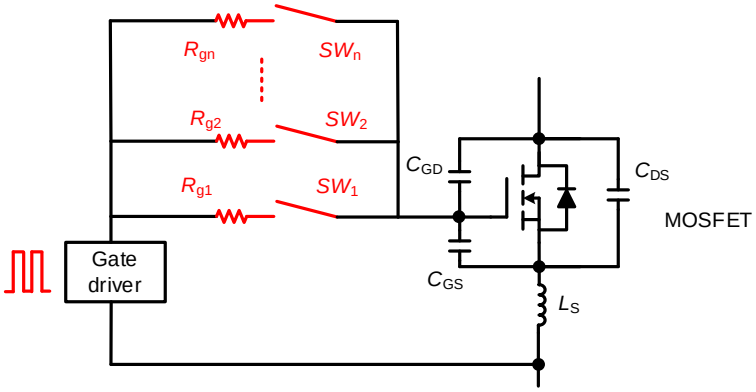


Fig. 2-4 Typical concept of an active gate driver with the variable gate resistance control

Usually, the open-loop control is utilized to suppress the slew rate by increasing the gate resistance during the Miller plateau period, while low gate resistance is used before and after the Miller plateau to reduce false-triggering risk[78]. The examples of active gate drivers with the variable gate resistance control are presented in publications[79][80], showing less oscillations than the CGDs (conventional gate drivers).

B. Multi-step Gate Voltage Control

Instead of the gate resistance, multi-step gate voltage control method focuses on the gate voltage to control the switching transient. There are many publications proposing active gate drivers with multi-step gate voltage control method to control the trajectory of gate voltages. Different from CGDs with only one turn-on gate voltage and one turn-off gate voltage, the active gate driver with multi-step gate voltage control usually has at least one more voltage-source to adjust the output gate voltage. Fig. 2-5 shows a typical concept of active gate driver with the multi-step gate voltage control. The output of the active gate driver changed during the switching transient to tune the slew rate of voltage and current. There are many publications[81]–[84] demonstrating circuits utilizing the concept to achieve gate voltage control. Although different circuits are used in the proposed gate drivers, their functions are all to generate controlled gate voltage trajectories.

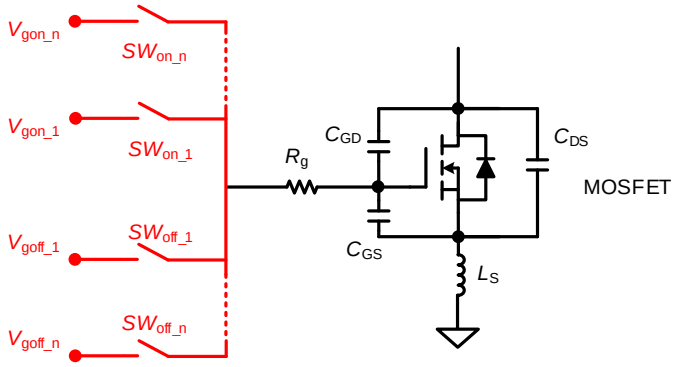


Fig. 2-5 A typical concept of active gate driver with the multi-step gate voltage control

Both open loop control[81][82] and close loop control[83][84] of the switches in the active gate drivers are presented in publications. In close loop control gate driver circuits, the drain current (I_D) is detected and feedback to the controller to slows down the device when the slew rate of I_D is high. Although the gate voltage trajectories are not the same in these publications, they all present better performance than CGDs.

C. Additional Gate Current Control

Another active gate control method is the additional gate current control strategy. Based on a CGD, an additional branch is connected to the gate terminal of the device to adjust its gate current during the turn-on and turn-off transient. The typical concept of the active gate driver with additional gate current control is demonstrated in Fig. 2-6. The working principle of these gate drivers is to generate an additional control gate current during the switching transient to control the switching speed. The current control unit can be a complicated current-source circuit as proposed in the publication[78], or be a simple voltage source with a resistor and some switches[85]. Similar to the multi-step gate voltage control method, both open-loop[85] and close-loop[86] can be applied to the additional gate current method.

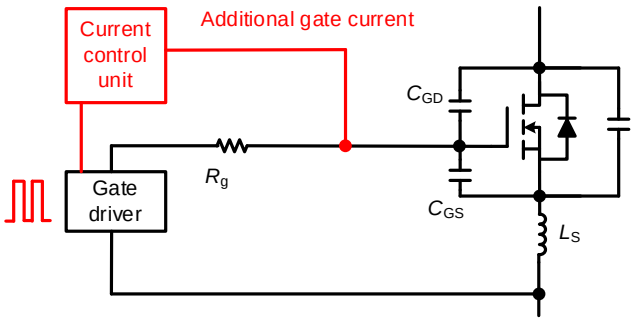


Fig. 2-6 Typical concept of the active gate driver with additional gate current control

D. *Timings to Adjust the Switching Speed*

Generally, the switching speed of an active gate driver can be classified into two levels: fast switching and slow switching. No matter what topology is used, the purpose is to control the switching speed during the turn-on and turn-off transient. The questions left are when to increase the switching speed and when to slow it down. Different publications give different answers to the period and the timings of when low or fast switching should occur. Some examples of the switching speed control strategies are demonstrated in Fig. 2-7. The vertical axial shows the control of the switching speed. "High" stands for high turn-on speed, which can be achieved by a low gate resistor, a high gate voltage or a high gate current; "Low" stands for low turn-on speed, which can be achieved by a high gate resistor, a low gate voltage or a low gate current. A typical turn-on/off transient is presented in the top of the figure, while the examples of switching speed control strategies are demonstrated below the waveforms. As is shown in (a), the turn-on speed is slowed down from the drain current raising period to the time when drain-source voltage reaches zero, while the turn-off speed is slowed down during the drain current decrease period[80]. Different from method (a), methods (b) and (c) demonstrate different control strategies, reducing the turn-on speed at t_2 when the drain current reaches load current[85][87]. After the drain-source voltage drops to zero, the turn-on speed is increased again in (b) while it keeps at low speed in (c).

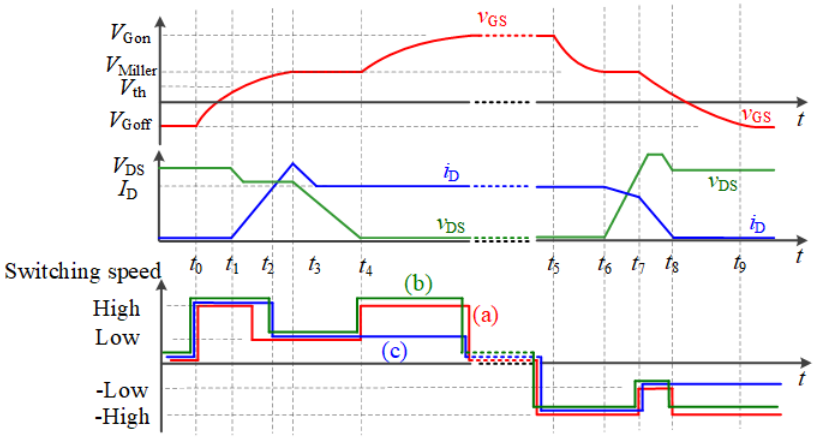


Fig. 2-7 Switching speed control strategies in publications: (a) [80], (b) [85], (c) [87]

It is shown in Fig. 2-7 that, although various active gate drivers are designed and constructed to control the switching speed during the switching transient, the control strategies of when to

reduce the switching speed vary in publications. Therefore, detailed switching models are needed to guide the usage of active gate drivers to achieve high performance with lower loss and lower oscillation.

E. Comparison Between the Voltage-Source Gate Driver and the Current-Source Gate Driver

The gate drivers used for the active gate driving method can be generally classified into two catogaries: voltage-source gate drivers and current-source gate driver. The comparison between the two gate drivers on device performances is demonstrated in 4.1. This section presents the comparison between the two gate drivers on the gate driver loss.

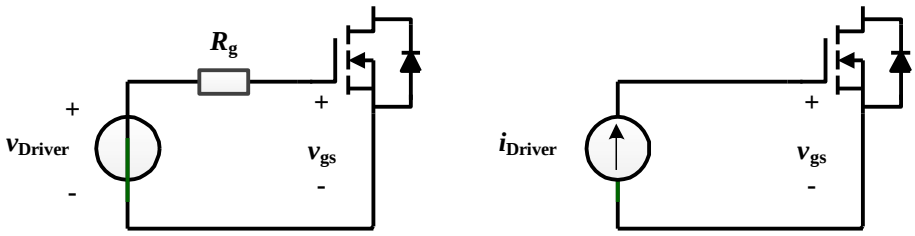
Fig.2-8 illustrates the typical structures of a voltage-source gate driver and a current-source gate driver. It is assumed that the gate-source capacitance is C_{gs}, the gate charge needed for turn-on is Q_{g}, the on-state gate voltage is V_{gon}, and the off-state gate voltage is V_{goff}. Taking the turn-on transient as an example, the typical turn-on gate waveforms are shown in Fig.2-9. For the voltage-source gate driver, the output voltage of the driver v_{driver} changes from V_{goff} to V_{gon} at t_0, resulting in rising of the gate voltage v_{gs} from V_{goff} at t_0 to V_{gon} at t_1 following the exponential function. The turn-on output of the voltage source gate driver can be derived:

$$E_{vs} = \int_{t_0}^{t_1} v_{driver} \cdot i_{gs} dt = v_{driver} \cdot \int_{t_0}^{t_1} i_{gs} dt = v_{gon} \cdot Q_g \tag{2.1}$$

For the current-source gate driver, v_{gs} follows a linear function in a current-source gate driver. The turn-on output of the current source gate driver can be calculated:

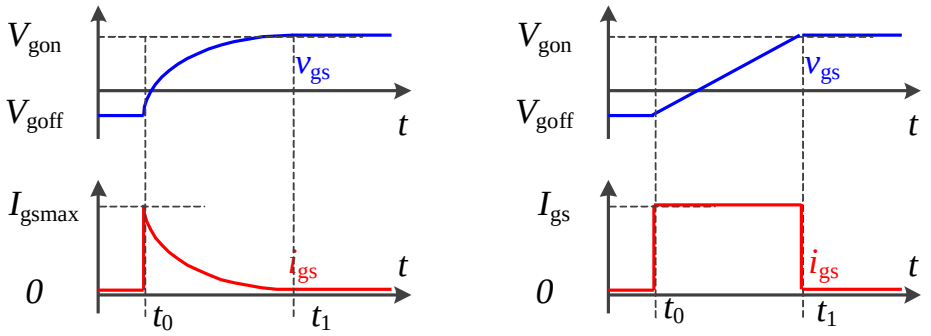
$$E_{cs} = \frac{1}{2} C_{gs} \left(V_{gon}^2 - V_{goff}^2 \right) = \frac{1}{2} \left(V_{gon} + V_{goff} \right) Q_g \tag{2.2}$$

It can be seen that the turn-on output energy of the voltage-source gate driver is only related with the on-state gate voltage and the gate charge, and is not influenced by the gate resitance R_{g}. As part of the energy is consumed by the gate resistor, the power loss of the voltage-source gate driver is higher than the current-source gate driver. Moreover, considering that $V_{\mathrm{goff}} < 0\mathrm{V}$, the power loss on the gate resistor is higher than the charging process of the gate capacitance.



(a) Voltage-source gate driver (b) Current-source gate driver

Fig. 2-8 Typical gate driver structures: (a) voltage-source gate driver (b) current-source gate driver



(a) Voltage-source gate driver (b) Current-source gate driver

Fig. 2-9 Typical turn-on gate waveforms: (a) voltage-source gate driver (b) current-source gate driver

2.2. Investigations on V_{th} Shift

2.2.1. *Importance of V_{th}*

The threshold voltage (V_{th}) is defined as the minimum gate-to-source voltage that is needed to create a conducting path between the source and drain terminals. V_{th} influences not only the performance of SiC MOSFETs in both steady and dynamic state, but also the evaluation of the junction temperature and lifetime prediction.

A. Influences on Steady-state Performance

The on-state resistance of a MOSFET (V_{on}) is determined by the gate voltage and threshold voltage. A MOSFET with high threshold voltage requires a high on-state gate voltage to reduce the on-state resistance. If V_{th} shifts in the positive direction, the on-state resistance might be increased[58]. Similarly, if V_{th} is decreased, a leakage current may be introduced in the off-state[58]. Therefore, V_{th} has significant influence on the on-state resistance and off-state leakage current of the SiC MOSFETs.

B. Influences on Dynamic-state Performance

V_{th} has influences on not only the steady-state parameters like on-state resistance and off-state leakage current, but also on the dynamic parameters during the turn-on transient. According to [88], the current slew rate (dI_D/dt) is also a function of V_{th}. Therefore, the higher the threshold voltage is, the lower the switching speed will be. Furthermore, other dynamic parameters of the SiC MOSFET, such as turn-on delay time and turn-off delay time, are also influenced by V_{th}.

C. TSEP (Thermal Sensitive Electrical Parameters)

TSEPs are the parameters that are sensitive to the change of temperature. Therefore, these parameters can be used to evaluate the temperature of the device after the calibration. One of the most used TSEPs is the on-state resistance R_{on}, or the on-state voltage across the device in its state of conduction V_{on}. R_{on} or V_{on} has good linearity and reasonably good sensitivity to temperature [89]. In addition to R_{on} and V_{on}, dynamic parameters including turn-on/off delay time (t_{don}/t_{doff})[90], turn-on current slew rate (di_D/dt)[88] has become increasingly popular in recent years due to its high sensitivity. However, these TSEPs are all influenced by V_{th}. For example, the increase of V_{th} results in a higher R_{on}, which eventually introduces a measurement error in temperature evaluation. Therefore, V_{th} information is important for TSEP-based temperature evaluation method. Moreover, V_{th} itself is a good TSEP with both good linearity and good sensitivity[89]. In addition, V_{th} has another advantage over other TSEPs, for example V_{on}: V_{th} is independent from the drain current, requiring no current measurement for TSEP evaluation. Consequently, V_{th} is important for TSEP-based temperature evaluation method.

D. Gate Health Indication

V_{th} provides not only the information of temperature, but also the health status of the gate oxide. It is demonstrated that the change of V_{th} is closely related to the gate biased time[91], while a large shift of V_{th} indicates the breakdown of oxide. Therefore, V_{th} information is usually used to evaluate the health condition of the gate oxide. Maintenance is required if the MOSFET has a large shift.

2.2.2. V_{th} Detection

The precondition for the V_{th} shift investigation is to measure V_{th}. The typical V_{th} measurement method is illustrated in Fig. 2-10[92]. V_{ds} is the constant voltage applied across the drain and source terminals of the MOSFET; a current sensor is used to monitor the drain current (I_d) of the device; an adjustable voltage source V_{gs} is applied to the gate of the MOSFET. V_{gs} increases from the off-state voltage (0V for example), until I_d is not zero (10mA for example). The value of V_{gs} is regarded as V_{th}. However, this measurement method is usually conducted under lab environment with a curve tracer, which can hardly be applied in practical applications.

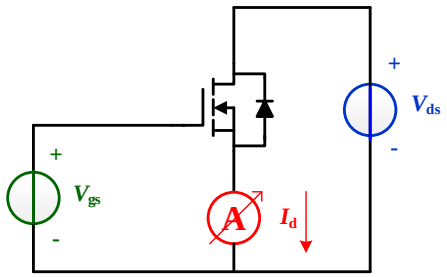
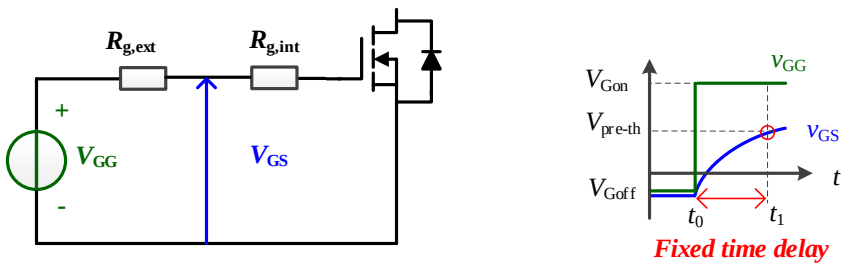


Fig. 2-10 Typical V_{th} measurement circuit

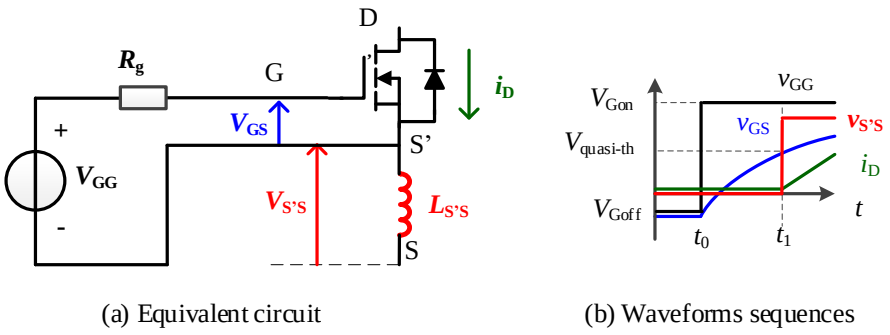
Various V_{th} estimation methods are proposed with the concepts of "quasi-threshold voltage $V_{quasi\text{-}th}$" and "pre-threshold voltage $V_{pre\text{-}th}$" being regarded as TSEPs to evaluate junction temperature. Fig. 2-11 illustrates the definition of the pre-threshold voltage $V_{pre\text{-}th}$[93]. $V_{pre\text{-}th}$ is defined as the gate voltage after a fixed time delay of the turn-on signal V_{GG}, which serves as an indicator of temperature due to the temperature-dependency of $R_{g,int}$. However, no evidence shows that it can be used to estimate V_{th}, although it can be used as a TSEP. In addition, it is more difficult to measure $V_{pre\text{-}th}$ when the device is switching very fast, especially for SiC MOSFET.



(a) Equivalent circuit (b) Waveforms sequences

Fig. 2-11 Definition of pre-threshold voltage: (a) equivalent circuit (b) waveforms sequences

Quasi-threshold voltage ($V_{quasi\text{-}th}$) is another method proposed to estimate V_{th} online[94][89]. For the MOSFETs with an additional Kelvin's source terminal, the voltage across the two source terminals can be used to indicate the change of the drain current. The definition of quasi-threshold voltage is illustrated in Fig. 2-12. During the turn-on transient of the MOSFET, the gate voltage increases from off-state gate voltage (V_{Goff}) until it reaches the threshold voltage. The drain current starts to increase after V_{GS} reaches threshold voltage, introducing a positive voltage across the parasitic inductance between the two source terminals. The gate voltage at the rising edge of $V_{S'S}$ can be regarded as the quasi-threshold voltage. However, there are also limitations for this method: firstly, the package of the MOSFET needs to include two source terminals like TO247-4, secondly, the bandwidth of the sample circuit must be high enough as the switching transient is very short, especially for SiC MOSFET. Therefore, a practical V_{th} measurement method is still needed for V_{th} shift evaluation of SiC MOSFET.



(a) Equivalent circuit (b) Waveforms sequences

Fig. 2-12 Definition of quasi-threshold voltage: (a) equivalent circuit; (b) waveforms sequences

2.2.3. V_{th} Shift over Gate Stress Time

Investigations into V_{th} shift of SiC MOSFET over gate stress time have been conducted in recent years[95]–[98]. In [95], both n- and p-MOSFET devices are tested under positive and negative gate bias stress condition at 125°C. The threshold voltage shift, as a function of stress time, is plotted in Fig. 2-13. It is illustrated that there is a linear relationship between the logarithm of V_{th} shift and the logarithm of the stress time. Similar relation is also proposed in the experiment results from [99], as shown in Fig. 2-14. However, instead of the logarithm of V_{th} shift, some publications[58] show a linear relationship between V_{th} shift and the logarithm of the stress time, as shown in Fig. 2-15. Therefore, further investigation is still needed to describe the relation of

V_{th} shift and the stress time.

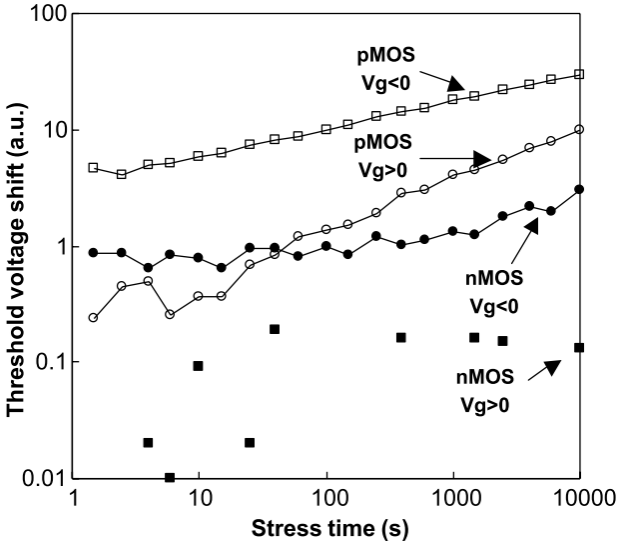


Fig. 2-13 Threshold voltage shift as a function of gate stress time in [95]

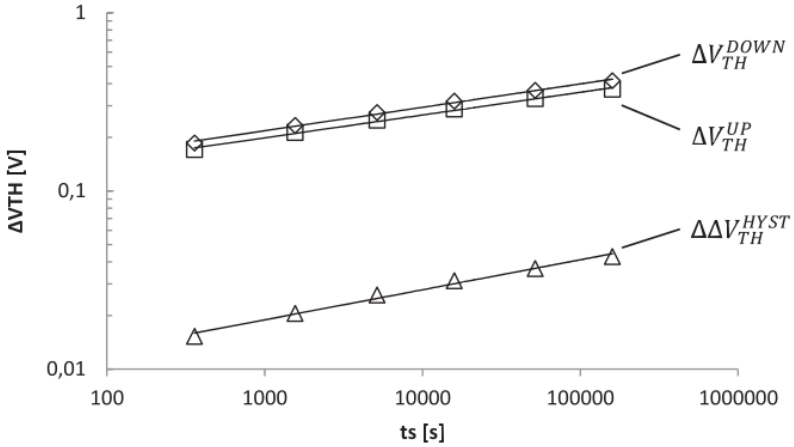


Fig. 2-14 Threshold voltage shift as a function of gate stress time in [99]

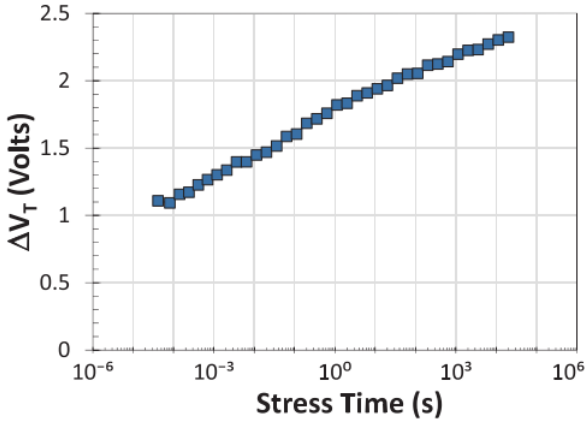


Fig. 2-15 Threshold voltage shift as a function of gate stress time in [58]

2.3. Summary

Three methods of switching oscillation suppression are reviewed, including parasitic parameters reduction, snubber circuit and active gate driving method. Both the first two methods require hardware modification of the power circuit, therefore they are limited in the application of existing converters. In contrast, active gate driving methods address oscillation issues from the aspect of control, requiring no modification on the power circuit. Therefore, this thesis focuses on the active gate driving method to reduce the switching oscillation of the SiC MOSFET.

For the threshold voltage shift issue, the background of V_{th} shift is reviewed, including the significance of V_{th}, mechanism of V_{th} shift, V_{th} detection methods and V_{th} shift over gate stress time. It is concluded that V_{th} is important for safe operation of the SiC MOSFET, but it is difficult to be measured. In addition, the relation of V_{th} shift over gate stress time is still unclear. This thesis proposes a new method to evaluate V_{th} and V_{th} shift of SiC MOSFET. With the proposed method, the relation of V_{th} shift over gate stress time is described with a multi-layer trap model.

It is concluded from the above that oscillation suppression and V_{th} shift detection should be managed by a gate driver. The next chapter proposes a new gate driver that is able to address both challenges.

Chapter 3 Design and Construction of a Current-Controlled Gate Driver

As mentioned in Chapter 2, the active gate driver is selected as the solution for oscillation suppression and V_{th} shift detection. It is reviewed in subsection 2.1.3 that there are 3 strategies for active gate signal control: variable gate resistance control, multi-step gate voltage control and gate current control. The discussion on the 3 strategies is demonstrated in section 4.1, showing that the gate current control strategy is more effective for switching speed control. Therefore, the gate current control strategy is applied to the designed gate driver. The following sections demonstrate the design and construction of the active gate driver.

3.1. Structure Design

3.1.1. Conventional Gate Driver Structure

The structure of a conventional gate driver is shown in Fig. 3-1. The input of a gate driver is the digital signal generated from the controller, while the output is a pulsating voltage commonly producing two voltage levels. In general, the input voltage is 5V for turn-on command and 0V for turn-off command; the input current is less than 1mA. In contrast, the output voltage is around 15~20V when the device is turned on and around -5V~0V when the device is turned off; the output current magnitude reaches to 2~4A[100].

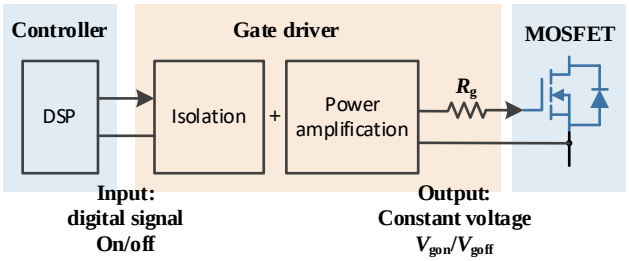


Fig. 3-1 Conventional gate driver structure

In essence, a gate driver is a power amplifier in combination with a high voltage isolator. But the problem is the flexibility. The input of the conventional gate driver only tells the device when to turn on and when to turn off, with no information to indicate the switching speed. The output of the gate driver is the corresponding fixed gate voltage (V_{gon} or V_{goff}), with no voltage

level in between. Moreover, the switching speed is controlled by the gate resistor R_g, providing no flexibility during the switching transient. Therefore, the structure needs to be modified to transfer more information for switching transient control and V_{th} shift detection.

3.1.2. Proposed Gate Driver Structure

In order to increase the flexibility of the gate driver, the proposed gate driver system is illustrated in Fig. 3-2. A digital-to-analog converter (DAC) is used to receive more complex information from the controller with the switching transient control command via SPI (Serial Peripheral Interface) communication. The commands are transferred into an analog input signal containing the information of switching speed. Considering that the gate current is the direct impact factor for the switching speed[101], the input analog signal is converted into a current signal instead of conventional voltage signal after isolated and amplified. Consequently, the output of the gate driver system is the programmed current signal, which is controlled by the SPI communication and can be used to adjust the switching speed. The DAC board can be purchased, while the rest of the signal processing circuit needs to be designed.

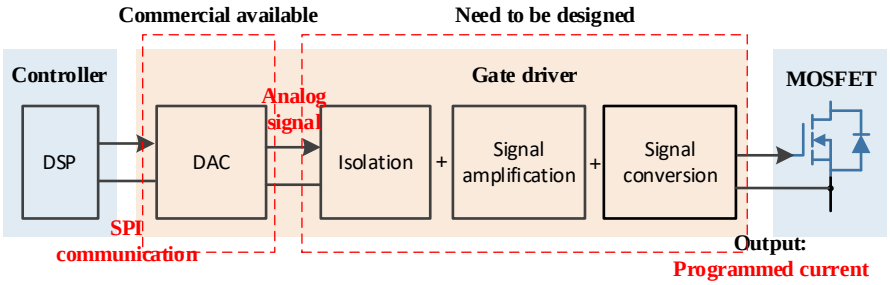


Fig. 3-2 Proposed gate driver system

The control strategy of the proposed gate driver system is presented in Fig. 3-3. There are 2 channels in the DAC, generating the switching transient control signal and the steady-state control signal respectively. The turn-on profile and the turn-off profile are pre-programmed and stored in DAC, which can be manipulated into different shapes. An example is shown in Fig. 3-3. The conventional PWM triggers the first channel of the DAC. The rising pulse of the PWM edge triggers the turn-on profile, and the falling pulse of the PWM edge triggers the turn-off profile. The pre-programmed turn-on and turn-off profiles determine the switching transients. An additional steady-state control signal is generated by the second channel of the DAC, which

is independent from the first channel. This control signal is desigend to tuning the on-state gate voltage and the off-state gate voltage. The reason for changing the on/off-state gate voltage is to manipulate the on-state voltage drop and the off-state leakage current. These two parameters are considered as important indicators for the health condition of the MOSFET. By controlling the on/off-state gate voltage, more information about the on-state voltage drop and the off-state leakage current under different gate conditions can be obtained to estimate the health of the MOSFET. The output of the two channels are added to form one analog signal, which is used to control the output current. It is shown that the shape of the output current follows the analog signal. As a result, the switching speed of the device can be controlled by the gate driver system. Moreover, the steady-state control signal can adjust the level of the on-state gate voltage and the off-state gate voltage, in order to improve the operating condition of the MOSFET. It is worth noting that the detailed circuit for isolation, amplification and conversion are discussed in section 3.3.

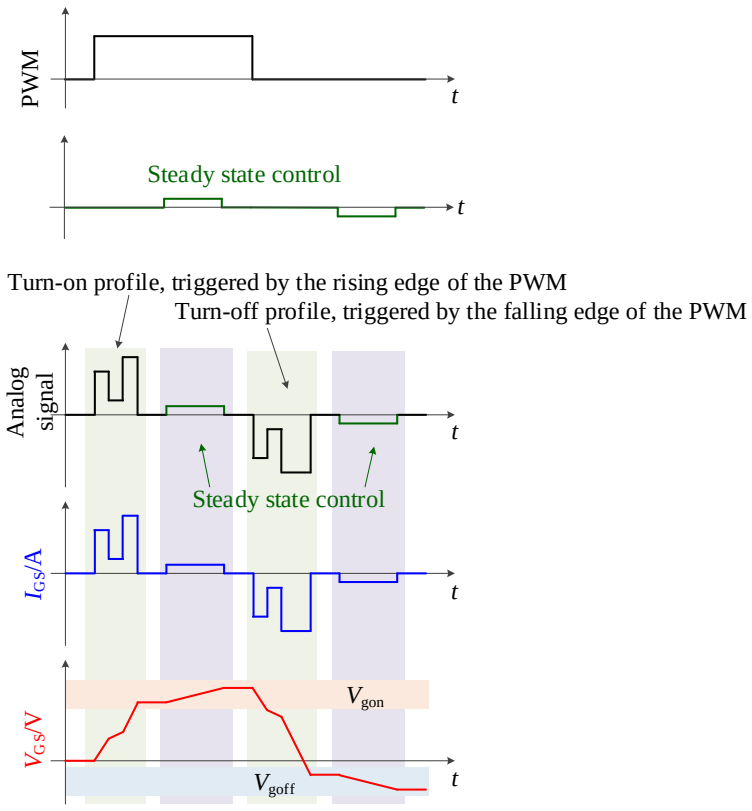


Fig. 3-3 Control strategy of the proposed gate driver system

3.2. Requirements of the Gate Driver

Before designing a gate driver, requirements of the gate drive performance must be clarified. Thus, key parameters for the gate driver are discussed in this section, including output voltage, output current, bandwidth and operating temperature. All these parameters are important for the design of the gate driver: the output voltage is closely related with the power supply voltage level; the output current is limited by the power level of the power supply; the bandwidth is the basic parameter for component selection, as well as the operating temperature. It is worth noting that in the datasheet of a commercial gate driver, there are many more parameters which are used for other functions like protection. In this thesis, only the basic function of a gate driver is discussed. Therefore, only four parameters are discussed in the design.

3.2.1. Output Voltage

The output voltage of a gate driver is directly connected to the gate of the SiC MOSFET. Therefore, the output voltage is of great importance for the performance and reliability of SiC MOSFET[102].

Table 3-1 Typical gate voltage of commercial 1200V SiC MOSFET from manufacturers

Manufactures	Part No		V_{goff}	V_{gon}
Infineon	CoolSiC™ Trench IMW120R030M1H	Limit	-7V	+23V
		Recommended	0V	+15V
ON Semiconductor	NVH4L020N120SC1	Limit	-15V	+25V
		Recommended	-5V	+20V
ROHM	SCT3030KL	Limit	-4V	+22V
		Recommended	0V	+18V
Wolfspeed	C2M0040120D	Limit	-10V	+25V
		Recommended	-5V	+20V

Table 3-1 presents the typical gate voltage of commercial 1200V SiC MOSFET (all available from RS) from various manufacturers. It is shown that the turn-on gate voltage (V_{gon}) ranges from +15V to +25V and the turn-off gate voltage (V_{goff}) ranges from -10V to 0V. According to the voltage levels of these commercial SiC MOSFETs, the output voltage requirement of the

proposed gate driver is in the range of -10V~0V to +15V~+25V.

3.2.2. Gate Current

The gate current has significant influence on the switching time of devices. Considering that the normal operating frequency of the SiC MOSFETs ranges from 20kHz to 100kHz, the average gate current of the gate driver can be calculated:

$$I_{avg} = \frac{Q_G}{\frac{T}{2}} = 2fQ_G \tag{3.1}$$

where I_{avg} is the average gate current, Q_G is the total gate charges, T is the switching period and f is the switching frequency. Based on the gate charges of the commercial SiC MOSFETs shown in Table 3.2, the average output current of the gate driver ranges from 2.4mA to 40mA. Therefore, the average output current requirement of the gate driver is 40mA at 100kHz.

Table 3-2 Typical gate charges of commercial SiC MOSFET from manufacturers

Parameters	Part No	Q_G
Infineon	CoolSiC™ Trench IMW120R030M1H	63nC
ON Semiconductor	NVH4L020N120SC1	220nC
ROHM	SCT3030KL	131nC
Wolfspeed	C2M0040120D	115nC

3.2.3. Bandwidth

Bandwidth is the frequency range of the signals that can pass through the circuit. For the conventional gate driver, the bandwidth is not an important parameter as digital signal is used, whose frequency ranges from 20kHz to 100kHz. However, much higher frequency signal is required to control the switching transient. As is shown in Table 3-3, the typical switching time of commercial SiC MOSFET is around 50ns, the corresponding bandwidth is 20MHz. Therefore, the bandwidth requirement of the proposed gate driver is 20MHz. It is worth noting that higher bandwidth is preferred for the control of the MOSFET, while 20MHz is the lowest requirement to control the switching transient. If the bandwidth is lower than 20MHz, the

switching transient may be finished before the control signal has an effect. In this work, all the components selected for switching transient control are with higher bandwidth than 100MHz, which is 5 times the required bandwidth.

Table 3-3 Typical switching time of commercial SiC MOSFET from manufacturers

Parameters	Part No	t_{on}	t_{off}
Infineon	CoolSiC™ Trench IMW120R030M1H	26ns~53ns	31ns
ON Semiconductor	NVH4L020N120SC1	42ns~69ns	51ns~86ns
ROHM	SCT3030KL	66ns	90ns
Wolfspeed	C2M0040120D	67ns	60ns

3.3. Topology Selection

It is illustrated in section Chapter 3 that the proposed programmable gate driver consists of the following functional circuits: galvanic isolation circuit, signal amplification circuit and signal conversion circuit. As there are many different topologies for each functional circuit, the features of different topologies of the functional circuits are listed and discussed in this section. The final circuit is the combination of the 3 functional circuits. Section 3.4.4 will propose 2 combinations of the listed topologies aiming to achieve the gate driving functions considering the key requirements discussed in this section.

3.3.1. Galvanic Isolation Circuit

Galvanic isolation is a principle of isolating functional sections of electrical systems to prevent current flow between input and output[103]. The SiC MOSFET is working at high-voltage condition, therefore the high voltage from the power device side needs to be isolated to protect the low voltage control circuit. Although different galvanic isolations techniques have been proposed, such as isolation capacitor[104] and hall effect[105]. The two most popular methods for gate driver circuits are transformer and opto-isolator[106].

A. Isolation Transformer

Using an isolation transformer is the most widespread method of galvanic isolation. Unlike

varying the turn ratio of a transformer to achieve different output voltages, in gate driver applications, the winding turns ratio of an isolation transformer is commonly 1:1[107]. Therefore, the voltages of the primary windings and the secondary windings are the same. The isolation transformer is often built with special insulation between primary and secondary windings to withstand the high voltage between them. A common topology of the isolation transformer is shown in Fig. 3-4. T is the isolation transformer to prevent current flow between primary and secondary windings, U1 and U2 are the voltage followers to increase the input impedance and decrease the output impedance of the isolation circuit.

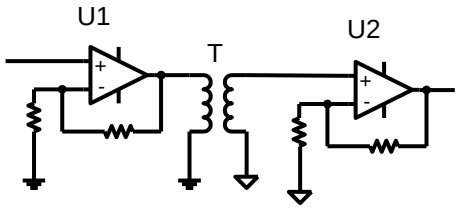


Fig. 3-4 Transformer topology for gate driver isolation

The advantage of the isolation transformer is that the transformer has high operating frequency, which meets the requirement for bandwidth of the gate driver. However, due to the magnetic saturation, the transformer has limits for low frequency signals that will be blocked by the transformer. Therefore, there is a lower frequency limit for the gate driver using transformer for isolation.

B. Linear Optocoupler

As a very popular isolation method, an optocoupler uses light to transfer electrical signals between two isolated circuits. The topology of the linear optocoupler is shown in Fig. 3-5:

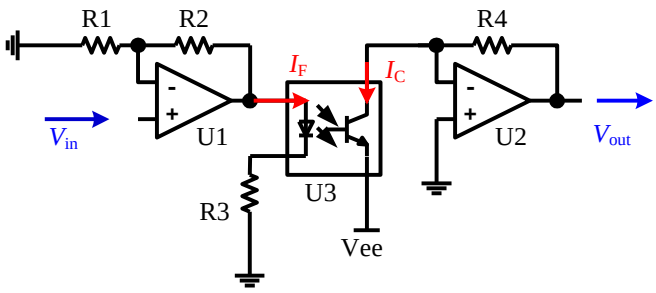


Fig. 3-5 Linear optocoupler topology for gate driver isolation

where I_F is the input of the optocoupler, and I_C is the output of the optocoupler. For the linear optocoupler, the current transfer ratio I_C/I_F is constant. U1 and U2 form the peripheral circuits of the linear optocoupler: a constant negative voltage V_{ee} is applied across the secondary side of the optocoupler, the output current I_C of the optocoupler is in proportion to the input current I_F. The relation of the input voltage V_{in} and output voltage V_{out} can be calculated with equations 3.2 and 3.3:

$$\frac{V_{in}}{R_1} = \frac{I_F \cdot R_3}{R_1 + R_2} \tag{3.2}$$

$$V_{out} = I_C \cdot R_4 \tag{3.3}$$

It is shown that the output voltage is in proportion to the input voltage:

$$\frac{V_{out}}{V_{in}} = \frac{I_C}{I_F} \cdot \frac{R_4(R_1 + R_2)}{R_1 R_3} \tag{3.4}$$

Compared with the isolation transformer, the advantage of an optocoupler is demonstrated at low frequency. This optocoupler is used to isolate the linear signal to control the steady-state gate voltage. As is shown in Fig. 3-3, the steady-state gate voltage is controlled during the on/off state of the MOSFET, therefore it requires lower a lower speed. As there is no saturation issue with an optocoupler, low frequency signals can be easily transferred by an optocoupler. However, the rise time and fall time of the optocoupler limit the transfer of high frequency signals. In digital isolation field, the non-linear optocoupler achieves high speed data transfer with nanoseconds rise/fall time. But for analog signals, a linear optocoupler should be used to reduce signal distortion. Linear optocouplers have much lower speed than non-linear digital optocoupler. The typical rise/fall time of a commercial linear optocoupler is more than 1us, making megahertz frequency signal transfer impossible [108].

C. Combination of Transformer and Optocoupler

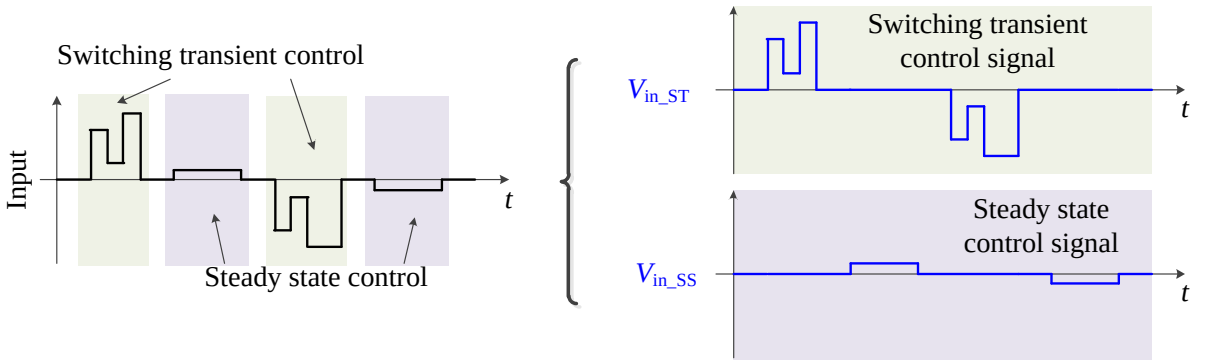


Fig. 3-6 Decomposition of the input signal

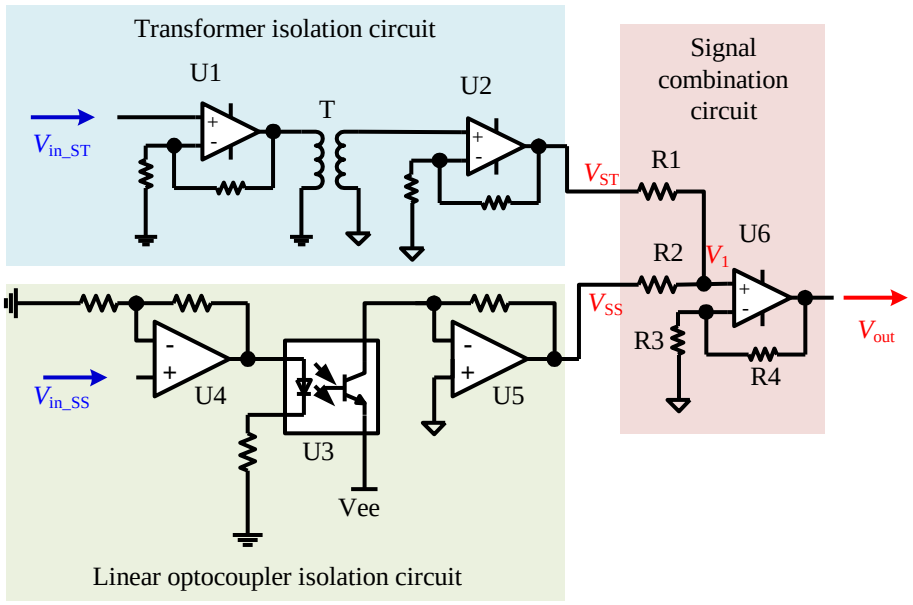


Fig. 3-7 Combined isolation topology

According to the above analysis on the transformer isolation and optocoupler isolation, the transformer has advantages for high frequency signals, but is not able to conduct low frequency signals; in contrast, a linear optocoupler is a good choice for low frequency signals, but has limited bandwidth to transfer high frequency signals. Based on the conceptual waveforms shown in Fig. 3-3, the input signal consists of 2 parts: switching transient control signal (V_{in_ST}) and steady state control signal (V_{in_SS}), as shown in Fig. 3-6. V_{in_ST} is the high frequency signal that is isolated by the transformer, while V_{in_SS} is the low frequency signal that can pass through the linear optocoupler.

The combined isolation topology is illustrated in Fig. 3-7. The switching transient control signal (V_{in_ST}) is isolated by the transformer isolation circuit, while the steady state control signal

(V_{in_SS}) can pass through the linear optocoupler. According to the analysis in previous subsections, the corresponding signals after isolation (V_{ST} and V_{SS}) are in proportion to the input control signals (V_{in_ST} and V_{in_SS}) respectively. The mathematic relation is illustrated in equations 3.5 and 3.6:

$$V_{ST} = K_T \cdot V_{in_{ST}} \tag{3.5}$$

$$V_{SS} = K_{LO} \cdot V_{in_{SS}} \tag{3.6}$$

where V_{in_ST} is the input signal for switching transient control, V_{ST} is the isolated switching transient control signal, V_{in_SS} is the input signal for steady state control, V_{SS} is the isolated steady state control signal, K_T is the scale factor of transformer isolation circuit, K_{LO} is the scale factor of linear optocoupler isolation circuit.

After the isolation, the high frequency switching transient control signal and the low frequency steady state control signal are combined. The output voltage of the combined signal can be described as:

$$\frac{V_{ST} - V_1}{R_1} + \frac{V_{SS} - V_1}{R_2} = 0 \tag{3.7}$$

$$\frac{V_1}{R_3} = \frac{V_{out}}{R_3 + R_4} \tag{3.8}$$

It can be calculated that:

$$V_{out} = \frac{R_3 + R_4}{R_3} \cdot \frac{R_1 \cdot V_{SS} + R_2 \cdot V_{ST}}{R_1 + R_2} \tag{3.9}$$

where V_{ST} is the isolated switching transient control signal, V_{SS} is the isolated steady state control signal, V_{out} is the output of the isolation circuit and R_1, R_2, R_3, R_4 are the resistances of the summation amplifier.

If the values of the resistors are equal ($R_1 = R_2 = R_3 = R_4$), it can be shown that the output voltage is the sum of V_{ST} and V_{SS}.

$$V_{out} = V_{ST} + V_{SS} \tag{3.10}$$

The combined isolation topology is novel to be used in a gate driver to cover a wider range of bandwidth.

In conclusion, the combined isolation topology is selected as the galvanic isolation circuit for the proposed gate driver.

3.3.2. Signal Amplification Circuit

A signal amplifier is used to amplify low voltage signals and to improve the quality of the signal that drives the device. This function can be achieved by the summation amplifier shown in Fig. 3.8. According to (3.9), V_{out} is in proportion to the sum of V_{ST} and V_{SS} if R_1=R_2. R_2 and $R3$ are scale resistors and a scale factor of $\frac{R_3+R_4}{2R_3}$ can be achieved. Therefore, V_{out} can be amplified by increasing the value of R_4. In sum, signal amplification function can be achieved by the circuit shown in Fig. 3-7.

3.3.3. Signal Conversion Circuit

The signal conversion circuit is used to convert voltage signals into current signals, in order to achieve gate current control. This subsection presents 2 typical signal conversion topologies.

A. Current-mirror-based Conversion Circuit

A current mirror is a circuit designed to generate a controlled current regardless of loading. Considering the fact that true current sources do not exist, the current mirror is widely used to emulate a current source.

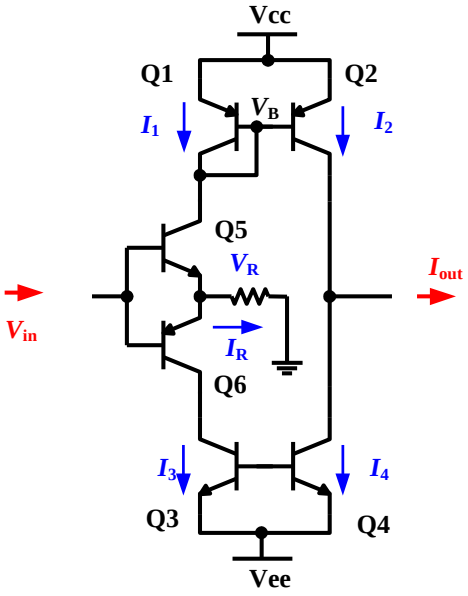


Fig. 3-8 Current-mirror-based signal conversion topology

A basic current mirror consists of 3 BJT pairs. Two BJT pairs have base and emitter terminals shortened, as shown in Fig. 3-8. Q1 and Q2 form pair1 and Q3 and Q4 form pair2. For BJT Q1, the current flowing through Q1 (I_1) is determined by the voltage difference between V_{cc} and V_B; the same applies to Q2. Therefore, I_2 is the same as I_1 if their base terminals and emitter terminals are connected. The same statement applies to current I_3 and I_4. The third pair is Q5 and Q6 that forms a voltage follower, generating a controlled voltage across the resistor. Based on Fig. 3-8, the following equations apply:

$$I_1 = I_2 \tag{3.11}$$

$$I_3 = I_4 \tag{3.12}$$

$$V_{in} = V_R \tag{3.13}$$

$$I_R = \frac{V_R}{R} \tag{3.14}$$

$$I_R = I_1 - I_2 \tag{3.15}$$

$$I_{out} = I_2 - I_4 \tag{3.16}$$

It is calculated that

$$I_{out} = \frac{V_{in}}{R} \tag{3.17}$$

Equation (3.17) shows that the output current (I_{out}) is proportional to the input signal voltage (V_{in}), therefore, it can be used to convert a voltage signal into a current signal. It should be noted that, in order to generate the output current (I_{out}), equal current (I_R) is required to be consumed by the resistor, resulting in losses. This is especially important for the design of the power supply.

The power loss of the right leg of the current mirror can be calculated based on equation (2.2) presented in 2.1.3. Considering the left leg conducts the same current as the right leg, the power loss of the current mirror circuit is twice the loss of a conventional voltage-source gate driver.

B. Howland-based Conversion Circuit

Howland circuits have been widely used as powerful sources over a wide frequency range[109]. Inspired by Howland current source topology, the improved Howland-based signal conversion topology is demonstrated in Fig. 3-9.

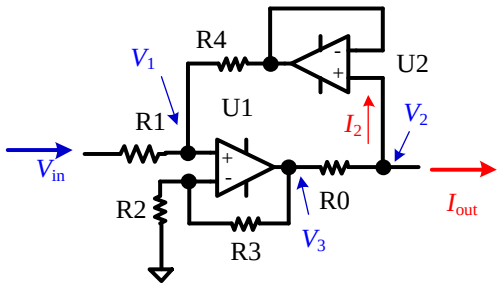


Fig. 3-9 Howland-based signal conversion topology

As it is shown in Fig. 3-9, the proposed Howland-based signal conversion topology consists of 2 amplifiers: U1 is used to generate the output current (I_{out}); U2 serves as the voltage follower. The function of U2 is to increase the impedance of current path I_2, making the value of I_2 so small that it can be neglected. Therefore, I_2 can be regarded as zero in the circuit. The working equations of U1 are shown below:

$$\frac{V_1 - V_{in}}{R_1} = \frac{V_2 - V_1}{R_4} \tag{3.18}$$

$$\frac{V_1}{R_2} = \frac{V_3 - V_1}{R_3} \tag{3.19}$$

$$I_{out} = \frac{V_3 - V_2}{R_0} \tag{3.20}$$

where V_{in} is the input voltage signal, I_{out} is the output current signal, R_0~R_4 are the values of the resistors shown in Fig. 3-9, V_1~V_3 are the voltages of the nodes demonstrated in Fig. 3-9.

It is calculated that the output current is proportional to the input voltage if R_3/R_2 equals R_4/R_1:

$$I_{out} = \frac{V_{in} \cdot R_4}{R_0 \cdot R_1} + \left(\frac{R_3}{R_2} - \frac{R_4}{R_1}\right) \cdot \frac{V_1}{R_0} \tag{3.21}$$

3.3.4. Gate driver circuit

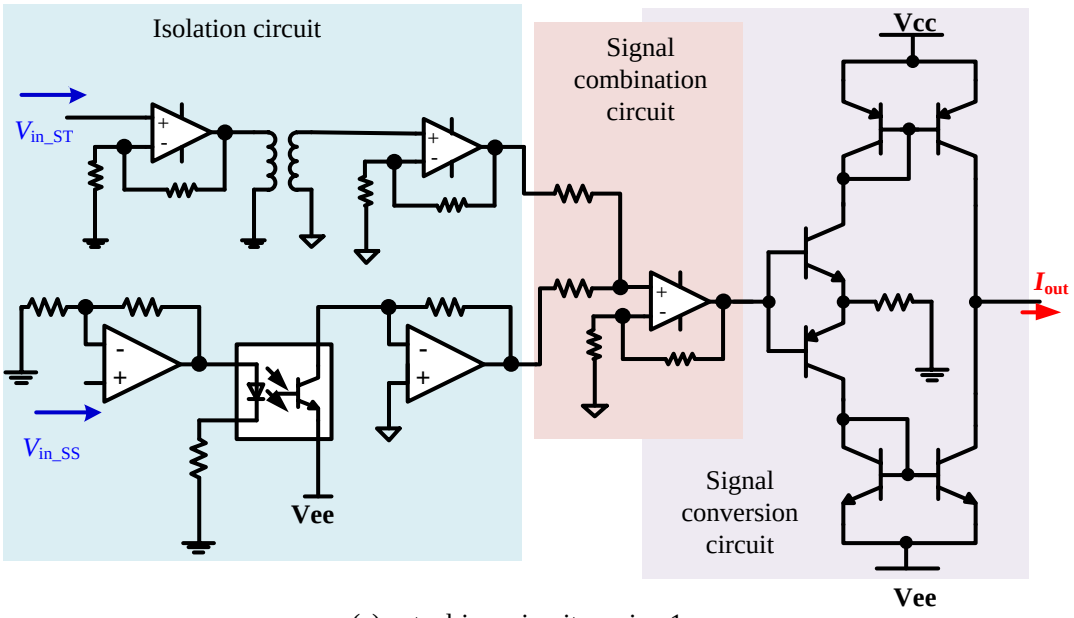
The overall gate driver circuit is the combination of 3 functional circuits: galvanic isolation circuit, signal amplification circuit and signal conversion circuit. The topology of galvanic isolation circuit is the combined isolation circuit of transformer and linear optocoupler; the signal amplification circuit is incorporated in the proposed galvanic isolation circuit; and the signal conversion circuits include the current-mirror-based signal conversion circuit and Howland-based conversion circuit. Therefore, 2 versions of the gate driver circuit are proposed as illustrated in Fig. 3-10. One is using the current-mirror topology and the other is using the Howland-based conversion circuit.

3.4. Gate Driver Construction

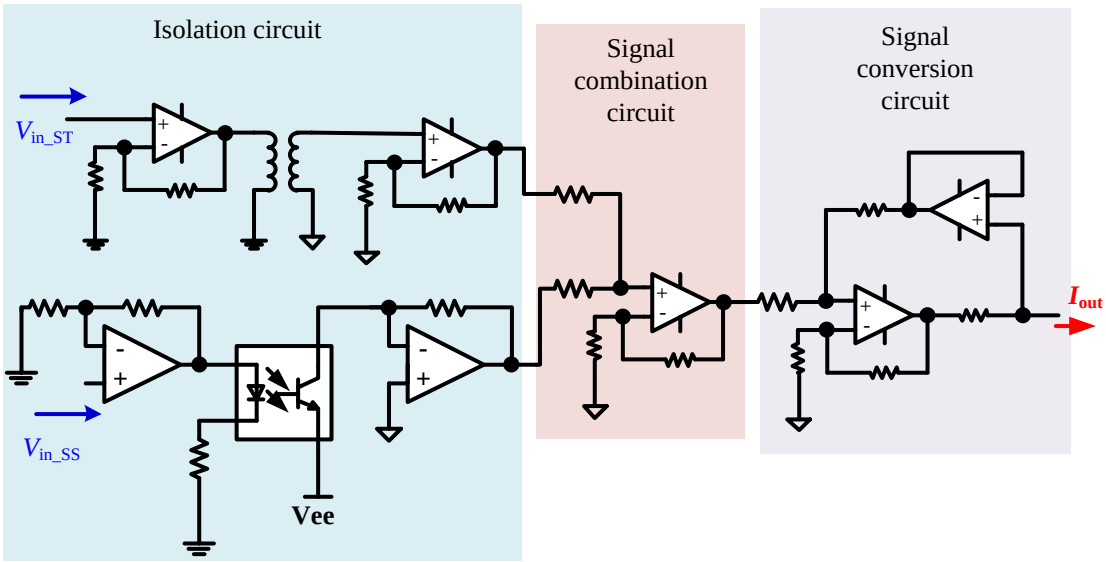
This section demonstrates the practical work on the proposed gate driver circuits, including the component selection and gate driver construction. The complete circuits with the values of all components are presented in Appendix I.

3.4.1. Component Selection

This section illustrates the selection of components used for the gate driver circuit construction, including the components mentioned in the gate driver topologies (transformer, linear optocoupler, amplifier and BJT) and other key components (controller and power supply).



(a) gate driver circuit version 1



(b) gate driver circuit version 2

Fig. 3-10 Proposed gate driver circuit using (a) current-mirror and (b) improved Howland circuit

A. *Controller*

The function of a controller is to generate control signals for the power devices in the power electronic system. For a conventional gate driver, a DSP(Digital Signal Processor) with GPIO (General-Purpose Input/Output) peripheral circuits is enough for controlling the power devices. However, for the proposed gate driver, high frequency analogue control signals are required. A DSP is not enough to generate arbitrary signal waveforms. Therefore, high frequency high

resolution DAC(Digital-to-Analog Converter) is required for the proposed gate driver. The combination of DSP and DAC is therefore used to generate arbitrary control signals for the proposed gate driver circuit.

TMS320F28335 from TEXAS Instruments is selected as the main controller. It is widely used in real-time control applications for processing, sensing and actuation to improve closed-loop performance. The SPI(Serial Peripheral Interface) communication module provides direct connection with DAC to control the generated waveforms.

As for DAC, AD9106 from Analog Devices is sufficient for this work with its integrating on-chip pattern memory for complex waveform generation. The DDS(Direct Digital Synthesizer) in AD9106 allows 12-bit, 180MHz output with a 24-bit tuning word. In addition, the evaluation kit of AD9106 is available with power functions to generate arbitrary waveforms. Therefore, AD9106 evaluation kit is used as the DAC for signal generation.

B. Power Supply

According to the analysis of the output voltage requirement shown in subsection 3.3.1, the output voltage ranges from -10V~0V to +15V~+25V. Therefore, the power supply voltage should cover this output voltage range. Moreover, a negative signal is needed in the gate driver board to generate the output signal, requiring negative power supply. Considering that the maximum supply voltage of amplifiers is usually less than 30V, the voltage difference between positive and negative power supply should be limited within 30V. The following output voltages from commercial isolated power supplies are: ±3.3V, ±5V, ±9V, ±12V, ±15V, ±24V. Therefore, the power supplies used in the proposed gate driver circuit are the serial connected ±9V and +12V power supplies. The positive power supply voltage is +21V while the negative power supply voltage is -9V. The part number of the selected ±9V power supply is the isolated DC/DC converter IH2409S from XP power, +12V selected power supply is the isolated DC/DC converter TMH2412S from TRACO POWER. In addition, 2 IH2409S converters are connected in parallel to increase the output current capability.

C. Transformer

The key parameter for the transformer is bandwidth, whose higher limit should be more than 20MHz as analyzed in subsection 3.3.3. At the same time, the lower limit of the working frequency of the transformer should be lower than 20kHz to ensure the transfer of switching signal. The selected transformer is the isolation transformer TG10-DA1NSLF from HALO Electronics. The nominal bandwidth of TG10-DA1NSLF is 10kHz to 200MHz, covering the required bandwidth of the proposed gate driver.

D. Optocoupler

The linear optocoupler selected for the gate driver circuit is TLP185 linear optocoupler from TOSHIBA, consisting of a photo transistor optically coupled to an infrared LED. The optocoupler is housed in a very small and thin package, making it suitable for high-density application, for example programmable controllers. The typical rise time and fall time are 2us, enough for the steady state control.

E. Amplifier

The amplifier is an important component for the proposed gate driver, as it is used in every of the three functional circuits (isolation circuit, signal amplification circuit and signal conversion circuit). The selected amplifier is the THS4631 from TEXAS Instruments. This amplifier is designed for applications requiring wideband operation, high input impedance, and high-power supply voltages. It provides a 210MHz gain bandwidth product, preventing the distortion of high frequency waveforms. Moreover, the recommended single supply voltage of THS4631 is 30V, meeting the requirement of the gate driver output voltage. In addition, the amplifier has high output current (150mA), making it the better choice for the gate driver circuit than other amplifiers.

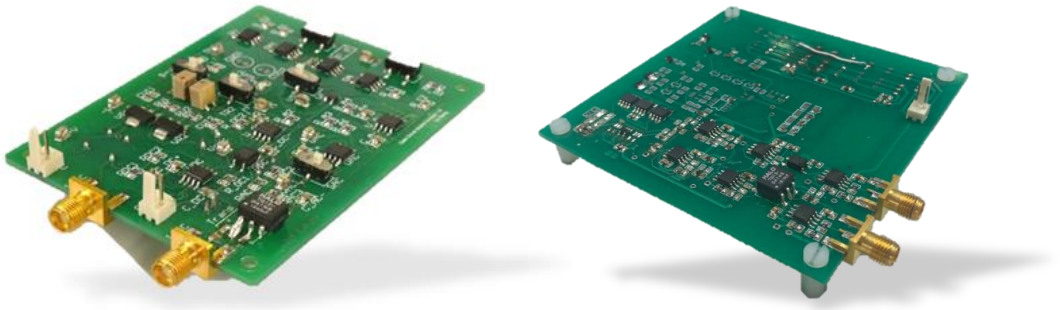
F. BJT

BJT is mainly used in the current-mirror topology. The requirements for BJTs are firstly high collector voltage (up to 30V), followed by high bandwidth (higher than 20MHz) and high output current (more than 40mA). The selected BJT is the complementary transistor NSS40302 from ON Semiconductor, which is designed for use in low voltage, high speed switching

applications. The collector-emitter voltage rates at 40V, and the collector current rating is 3A. Moreover, the 100MHz high bandwidth and the linear gain make NSS40302 an ideal component in analog amplifiers.

3.4.2. Gate Driver Boards Construction

Based on the gate driver circuit topologies shown in Fig. 3-10 and the components selections illustrated in section 3.4.1, 2 gate driver circuits are designed using Altium Designer. 2 versions of the gate driver circuits are constructed, the pictures of the gate drivers are demonstrated in Fig. 3-11.



(a) version 1 **(b) version 2**

Fig. 3-11 Pictures of the proposed gate driver circuits (a) using current-mirror-based circuit and (b) using Howland-based circuit

3.5. Final Version Modification

After the construction of the gate driver boards, there were initially some problems with their operations. Firstly, when the gate driver has no input signal, the output current is zero, meaning it behaves like that the gate driver is disconnected with the load capacitor and the output voltage is unknown. Therefore, the output voltage is sensitive to noise, especially when the load capacitor is small. Moreover, the steady state control is difficult for SiC MOSFET as the gate capacitance is small, and noise in the input signal would result in large output error in the gate voltage. In summary, modification is needed to solve two problems: 1. The output voltage needs to be clamped to a default value (0V) when the input is zero; 2. The steady-state gate voltage (on/off-state gate voltage) needs to be clamped to a reliable voltage source to eliminate the noise

during the on/off-state.

3.5.1. *Modified Control Strategy*

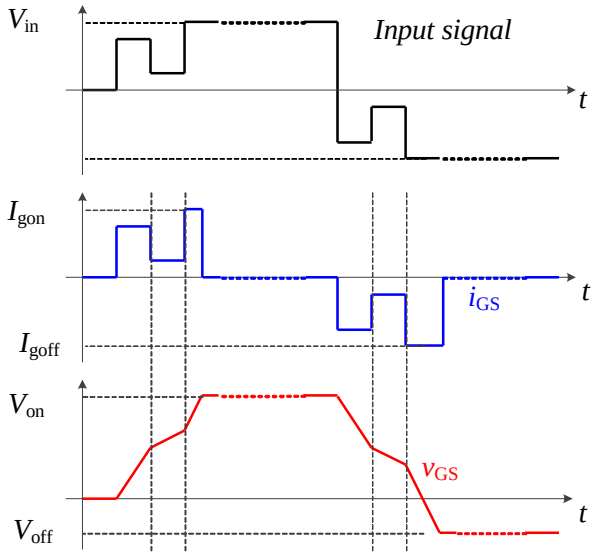


Fig. 3-12 Control strategy after modification

The control strategy after modification is illustrated in Fig. 3-12. In the beginning, the gate voltage v_{GS} is 0V when the input signal is 0. During the turn-on transient, the gate current i_{GS} follows the profile of the input signal v_{in}. Thus, the rising speed of the gate voltage v_{GS} is controlled by the input signal v_{in} until it reaches V_{on}. After the turn-on transient, the gate current i_{GS} becoms 0A while the input signal v_{in} is kept at a positive value to clamp v_{GS} at V_{on}. During the turn-off transient, a negative input signal v_{in} is generated, resulting in a corresponding gate current signal. The gate current follows the profile of the input signal until the gate voltage reaches the off-state gate voltage V_{off}. The input signal is kept at a negative value to clamp v_{GS} at V_{off}. In this control strategy, the steady-state control signal shown in Fig. 3-3 is not needed. Because the voltage is clamped at V_{on} or V_{off} during the steady-state. This method reduces the flexibility of the gate driver as it is not able to control the on/off-state gate voltage, but the benefits are that this method makes it much easier for the control of the gate driver.

3.5.2. *Modified Signal Conversion Topology*

Two topologies of the signal conversion circuit are demonstrated in section 0: current-mirror-based circuit and Howland-based circuit. For the current-mirror-based circuit, it is difficult to

set a default value for the circuit when the input is 0, unless a pull-down resistor is connected to the output terminal. However, this increases loss and complexity. In contrast, simple modification can be conducted on the Howland-based circuit to set a default value, as shown in Fig. 3-13.

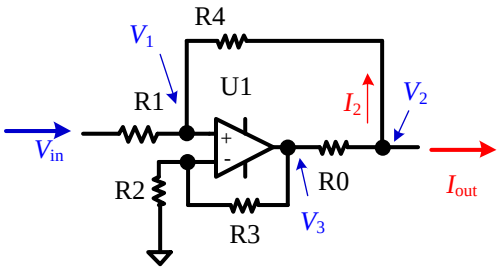


Fig. 3-13 Modified Howland-based signal conversion circuit

The circuit looks like an amplification circuit, but 2 additional resistors, R_0 and R_4, make it work differently from an amplification circuit. The working principle of the proposed topology is similar to the Howland-based signal conversion topology illustrated in subsection 3.4.3 B. The only difference is that I_2 cannot be ignored. Assuming R_1=R_2=R_3=R_4=R, it is calculated from equation 3.5 that $I_{out} = \frac{V_{in}}{R_0} - I_2$. When the input voltage V_{in} is zero, I_2 ensures the output voltage V_2 equals to zero. Moreover, when the input voltage V_{in} is not zero, I_2 is negligible if R>>R_0. Therefore, the signal conversion function is not influenced. Moreover, the signal conversion circuit has become simpler after the modification than the circuit shown in section 0.

3.5.3. Final Gate Driver Circuit

The modified gate driver circuit is proposed as shown in Fig. 3-14, while the picture of the final gate driver board is presented in Fig. 3-15. It is worth noting that the final board is modified from board version 2, therefore it looks very similar to Fig. 3-11(b). In the following chapters, all the experiments are conducted using the final gate driver board.

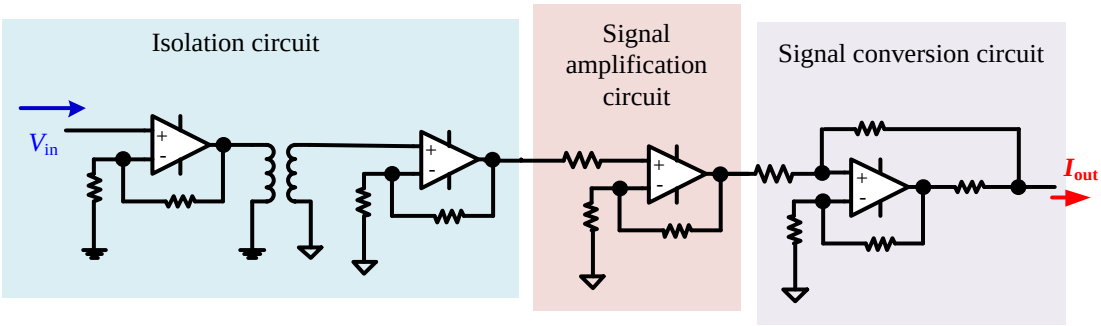


Fig. 3-14 Final gate driver circuit

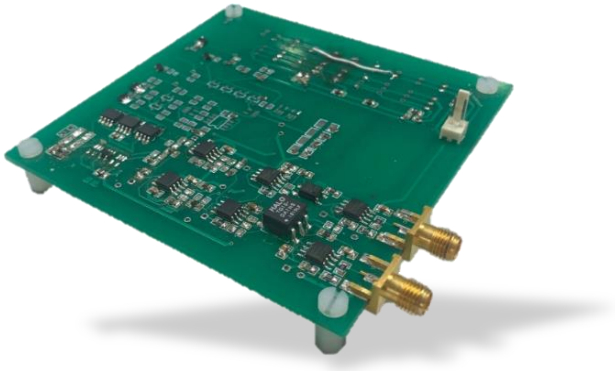


Fig. 3-15 Picture of the final gate driver board

3.6. Summary

This section demonstrates the design and construction of a current-controlled gate driver. The structure and control strategy of the proposed gate driver are demonstrated compared with a conventional gate driver, showing its flexibility on gate current control. The requirements of the proposed gate driver are identified in terms of output voltage, gate current and bandwidth. Three function circuits are included in the gate driver, namely galvanic isolation circuit, signal amplification circuit and signal conversion circuit. The topologies for the three function circuits are illustrated, as well as the component selection. After the construction of the gate driver prototype, the modifications on the control strategy and circuit are demonstrated to improve the performance of the gate driver.

Chapter 4 Switching Transient Optimization

The control over switching transient is widely regarded as a trade-off between oscillation and loss: the switching loss is reduced by increasing d*i*/dt and d*v*/dt, which introduces higher oscillation. However, detailed analysis on the source of oscillation is still needed. In this chapter, the small signal models of the oscillation circuit in different switching periods are proposed and analyzed, illustrating the impact factors of the oscillation sources. Based on the models, U-shape and N-shape gate driving signals are proposed for turn-on and turn-off transient optimization respectively. Experimental results verify that both the switching loss and the overshoots are reduced by the proposed gate driving method.

4.1. Gate Control Strategies

This section presents the comparison among 3 gate control strategies on the switching transient: current-control strategy, voltage-control strategy, and resistance-control strategy.

4.1.1. Current-Control Strategy

When the MOSFET is in saturation region, the drain current (i_D) is determined by the gate voltage, independent from the drain-source voltage (v_{DS}). The quantitative relationship is illustrated in (4.1):

$$i_D = \frac{\mu_n \cdot C_{OX} \cdot W}{2L}(v_{GS} - V_{th})^2 \tag{4.1}$$

where μ_n is the mobility of electrons in the channel, C_{ox} is the capacitance of the gate oxide, W is the channel width, L is the channel length, and V_{th} is the threshold voltage.

The slope of i_D can be derived by differential computing (4.1). The result is shown in (4.2):

$$\frac{di_D}{dt} = \frac{\mu_n \cdot C_{OX} \cdot W}{L} \cdot (v_{GS} - V_{th}) \cdot \frac{dv_{GS}}{dt} \tag{4.2}$$

Considering the capacitive relation between i_{GS} and v_{GS}, the following equation is calculated:

$$i_{GS} = C_{OX} \cdot \frac{dv_{GS}}{dt} \tag{4.3}$$

The relation between i_{GS} and v_{GS} shown in (4.1) and (4.3) is then fed into (4.2), presenting in (4.4) the influence of i_{GS} on di_D/dt.

$$\frac{di_D}{dt} = \sqrt{\frac{2 \cdot \mu_n \cdot W \cdot i_D}{C_{OX} \cdot L}} \cdot i_{GS} \tag{4.4}$$

It is shown that the slope of drain current (di_D/dt) is in proportion to the gate current (i_{GS}). The speed of switching transient can be manipulated by varying i_{GS}.

4.1.2. Resistance-Control Strategy

Resistance-control strategy is the mostly used method to control the switching speed because of its simple structure. A typical gate loop circuit is demonstrated in Fig. 4-1, where R_{G_ext} is the external gate resistor, R_{G_int} is the internal gate resistor, C_{GS} is the gate-source capacitance, L_S is the parasitic source inductance, v_{driver} is the output voltage of the gate driver, i_{GS} is the gate-source current and v_{GS} is the gate-source voltage.

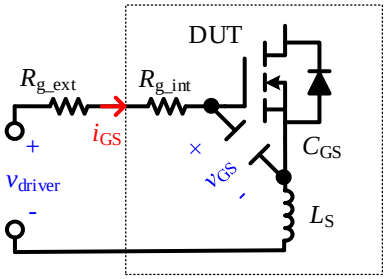


Fig. 4-1 A typical gate loop circuit

The relation between R_{G_ext} and i_{GS} can be described by applying Kirchhoff's law demonstrated in (4.5):

$$v_{driver} = i_{GS} \cdot \left(R_{G_{ext}} + R_{G_{int}}\right) + v_{GS} + L_S \cdot \frac{di_D}{dt} \tag{4.5}$$

The influence of R_{G_ext} on di_D/dt can be derived by substituting i_{GS} with di_D/dt as shown in (4.6)

$$\frac{di_D}{dt} = \frac{v_{driver} - v_{GS}}{L_S + \frac{L \cdot \left(R_{G_{ext}} + R_{G_{int}}\right)}{\mu_n \cdot W \cdot (v_{GS} - V_{th})}} \tag{4.6}$$

It is presented that di_D/dt can be reduced by increasing external gate resistor R_{G_ext}. However, the source inductance L_S also plays an important role: the influence of R_{G_ext} on di_D/dt is

weakened by L_S. This phenomenon is observed in the simulation results shown in Fig. 4-2 as the simulated results from TI software TINA. The turn-on i_D waveform is demonstrated using different gate resistors ranging from 5Ω to 20Ω. It is expected that di_D/dt would decrease when a gate resistor with higher value is used, however, the result shows that di_D/dt is less influenced: the currents are in parallel with each other. The simulation results verify that the control effect of the gate resistor is weakend if the source inductance is large. In the contrast, di_D/dt can be reduced if an additional inductance is added to L_S while the gate resistor is the same. Fig. 4-3 presents the simulation waveforms in the test condition that the gate resistor is kept at 20Ω. An additional inductor is added to the source terminal of the MOSFET. It is shown that the current slope is reduced along with the increase of L_S. In conclusion, the resistance-control strategy is an indirect control strategy to manipulate switching speed. The effect of the gate resistor is weakened due to the influence of L_S.

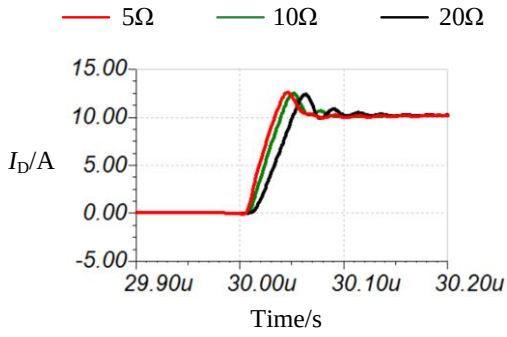


Fig. 4-2 Turn-on i_D simulation results using different gate resistors. Test condition: 250V dc voltage, 10A load current, 15V turn-on gate voltage, device model (SCT3060)

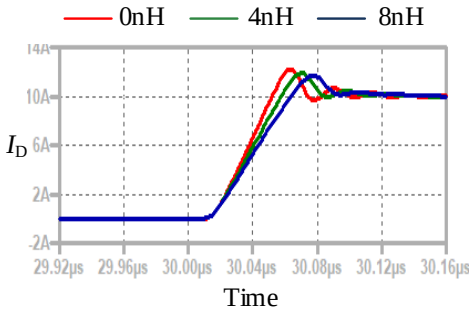


Fig. 4-3 Turn-on i_D simulation results with additional inductance. Test condition: 250V dc voltage, 10A load current, 15V turn-on gate voltage, 20ohm gate resistor, device model (SCT3060).

4.1.3. Voltage-Control strategy

The circuit of the voltage-control strategy is the same as the resistance-control strategy as shown in Fig. 4-1. The difference is that v_{driver} is parameter to be controlled rather than R_{g_ext}. The equation of the voltage-control strategy is also described by (4.6). A similar disadvantage is also observed: the effect of the voltage-control strategy is influenced by L_S. Moreover, the complex relationship makes it difficult to achieve quantitative control over di_D/dt by manipulating the voltage. For example, if the target is to reduce di_D/dt by 50%, it can be simply achieved by reducing i_{GS} by 50% with the current-control strategy. But for voltage-control strategy, complicated calculation is needed before quantitative control can be achieved.

It is concluded that current-control strategy has direct influence on di_D/dt, while resistance-control and voltage-control strategies make hardly impact by changing gate current. Therefore, no matter what strategy is used, the essence of switching transient control is to control the gate current. In this work, in order to decouple the influence of L_S, the current-controlled gate driver is used to control the switching transient. It is worth noting that the methodology discussed in the following sections can also be applied to resistance-controlled gate driver and voltage-controlled gate driver.

4.2. Switching Oscillation Analysis

The schematic of a typical double-pulse test circuit is illustrated in Fig. 4-4, where C_{DC} is the busbar capacitance, L_{load} is the load inductance, L_p is the parasitic inductance in the power loop, C_{Diode} is the junction capacitance of the diode, C_{DS} is the drain-source parasitic capacitance of the device under test. In this section, the small signal models are developed to analyze the switching oscillation.

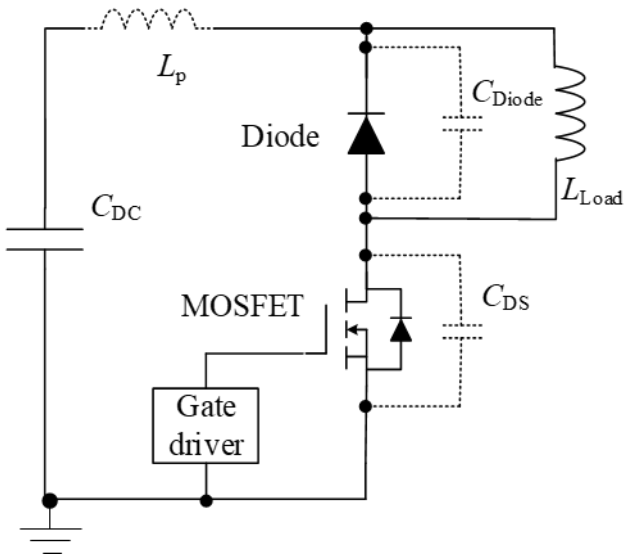


Fig. 4-4 Schematic of a typical double-pulse test

4.2.1. Turn-on Oscillation Model

The conceptual waveforms in turn-on transient used for oscillation analysis are illustrated in Fig. 4-5, where 5 subintervals during t_1~t_5 are identified to carry out the analysis:

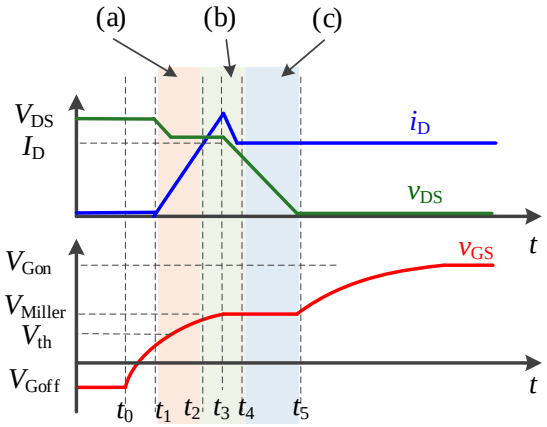


Fig. 4-5 Conceptual waveforms during turn-on transient

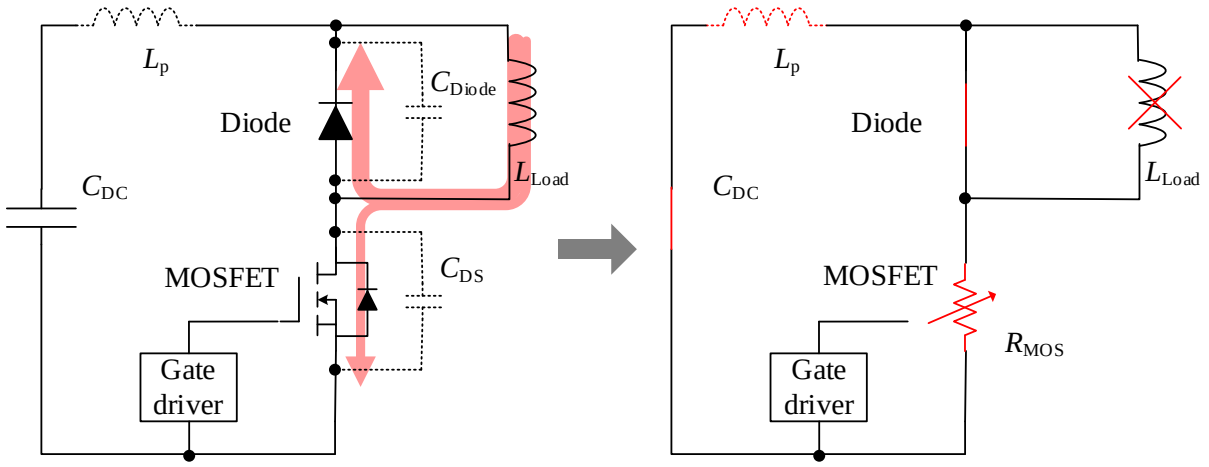
(a) Subinterval t_0~t_1: Turn on preparation stage. The gate voltage of the MOSFET starts to increase from the off-state gate voltage. The increasing of the gate voltage ends when the gate voltage reaches the threshold voltage. This process is the charging process of the gate capacitor.

(b) Subinterval t_1~t_2: Drain current increasing stage. The gate voltage of the MOSFET is higher than the threshold voltage in this period, introducing the increase in the drain current.

Meanwhile, the diode keeps conducting current, resulting in the low impedance of the diode. In the contrast, the MOSFET presents a large resistance because it is not yet in the saturation region. As a result, the diode can be regarded as a short circuit in this period, while the MOSFET performs as a large variable resistor.

(c) Subinterval t_2~t_4: Diode turn off stage. In this period, the drain current is determined by the capacitive current of the diode. The diode can no longer regarded as a short circuit, instead, it starts to withstand high voltage. The MOSFET is still in the pre-saturation region, performing as a variable resistor. The only difference is that the value of the resistor is lower than in (a). Consequently, the diode can be modelled as a controlled current source in the period, while the MOSFET still performs as a variable resistor.

(d) Subinterval t_4~t_5: Drain-voltage decrease stage. The diode stops conducting current in the period, resulting in all the load current flowing through the MOSFET. In this period, the drain-source voltage declines with its slope rate controlled by the gate current. Therefore, the voltage-source model can be used to describe the characteristics of the MOSFET, while the diode can be regarded as open circuit.

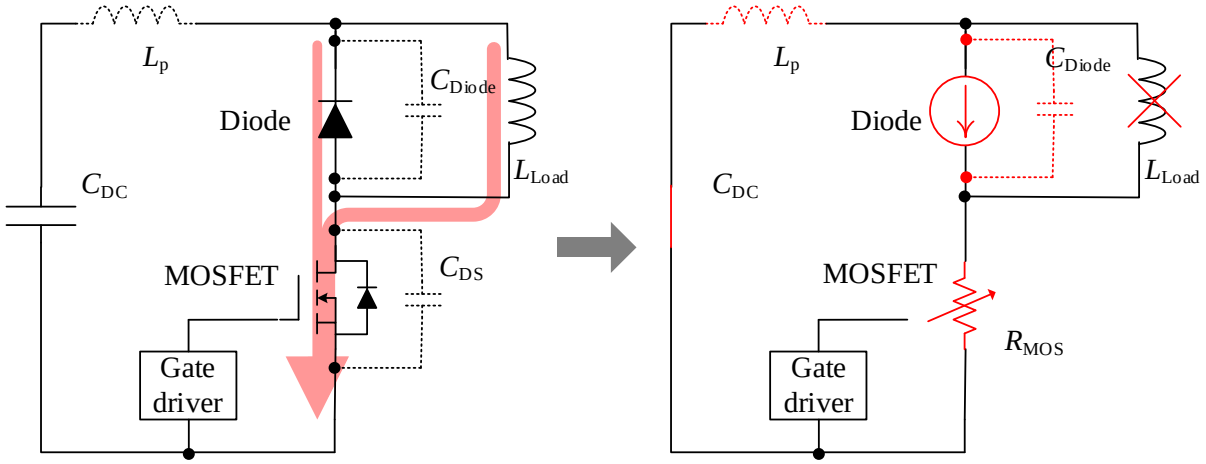


(a) Current path (b) Small signal model

Fig. 4-6 Analysis of the turn-on transient in subinterval a: (a) Current path; (b) Small signal model

The analysis of the switching transient in subinterval a is proposed in Fig. 4-6, including the

current path in the period and the small signal model. Considering that the diode conducts current in this period, the diode is modelled as a short circuit. In the meantime, the MOSFET presents the same effect as a large variable resistor R_{MOS}, whose resistance is controlled by the gate voltage. In addition, the large inductor L_{Load} can be regarded as an open circuit in the small signal model, while the large capacitor C_{DC} can be modelled as a short circuit. Based on the analysis, the small signal model of the switching transient in subinterval a is illustrated in Fig. 4-6(b). It is demonstrated that the small signal model is a first-order circuit, consisting of a resistor R_{MOS} and an inductor L_p. Therefore, there is no oscillation introduced in this period.



(a) Current path (b) Small signal model

Fig. 4-7 Analysis of the turn-on transient in subinterval b: (a) Current path; (b) Small signal model

The analysis of the switching transient in subinterval b is presented in Fig. 4-7. The current flowing through the MOSFET consists of 2 parts: the constant load current from the load inductor and the capacitive current of the diode. Similar to subinterval a, the MOSFET is modelled as a variable resistor. In addition, a current source is used to describe the characteristic of the diode in this period. Based on the small signal model, the following equation is derived according to Kirchhoff's circuit laws in Laplace form.

$$(sL_p + R_{MOS}) \cdot i_D + \frac{1}{sC_{Diode}} \cdot (i_D - I_{Diode}) = 0 \tag{4.7}$$

where L_p is the parasitic inductance in the circuit loop, C_{Diode} is the junction capacitance of the diode, i_D is the drain current of the MOSFET, R_{MOS} is the corresponding resistance of the

MOSFET, I_{Didoe} is the current source used to simulate the performance of the diode. It is worth noting that the resonant components are the parasitic inductance L_p and the junction capacitance of the diode C_{Diode}. R_{MOS} acts like a damping resistor and reduces the oscillation. The role of the damping resistor R_{MOS} is neglected in the oscillation analysis for simplicity.

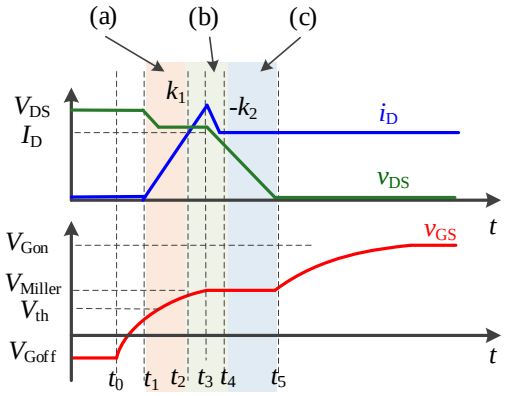


Fig. 4-8 State changes in subinterval b

The state of the current source has changed twice at t_3 and t_4. As is shown in Fig. 4-8, the slope rate of the drain current changes from k_1 to $-k_2$ at t_3, and changes from $-k_2$ to 0 at t_4. The corresponding states of the current source are demonstrated as below:

$$I_{Diode\_t2\sim t3} = k_1(t - t_3) + I_{01} \tag{4.8}$$

$$I_{Diode\_t3\sim t4} = -k_2(t - t_3) + I_{01} \tag{4.9}$$

$$I_{Diode\_t3\sim t4} = -k_2(t - t_4) \tag{4.10}$$

$$I_{Diode\_t4\sim t5} = 0 \tag{4.11}$$

where $I_{Diode\_t2\sim t3}$, $I_{Diode\_t3\sim t4}$, $I_{Diode\_t4\sim t5}$ are the capacitive current of the diode in the period t_2~t_3, t_3~t_4, t_4~t_5, respectively; k_1 and $-k_2$ are the slope rates of the diode in the period t_2~t_3 and t_3~t_4, respectively; I_{01} is the current of the diode at t_3. It is worth noting that k_1 and k_2 are both positive.

The state change of the current source at t_3 can be derived from (4.8) and (4.9).

$$\Delta I_{Diode@t3} = -(k_1 + k_2) \cdot (t - t_3) \tag{4.12}$$

where $\Delta I_{Diode@t3}$ is the current source introduced at t_3 due to the change of state.

Taking the Laplace transform of (4.12) at t_3, the Laplace form of the current source is shown below:

$$\Delta I_{Diode@t3} = -(k_1 + k_2) \cdot \frac{1}{s^2} \tag{4.13}$$

The corresponding current introduced at t_3 can be derived by substituting the current source in (4.7) with (4.13).

$$\Delta i_{D@t3} = \frac{-(k_1 + k_2)\frac{1}{s^2}}{s^2 L_p C_{Diode} + s R_{MOS} C_{Diode} + 1} \tag{4.14}$$

where $\Delta i_{D@t3}$ is the corresponding drain current introduced at t_3. R_{MOS} is the resistance of the MOSFET, whose value is not constant and keeps decreasing until 0 at t_5. It is worth noting that the oscillation is introduced by the diode, where R_{MOS} has no influence on. Therefore, the effect of R_{MOS} is neglected in the analysis on oscillation source to simplify the calculation. The formula (4.15) can be transformed into standard format:

$$\Delta i_{D@t3} = (k_1 + k_2)\left(\frac{1}{\omega} \cdot \frac{\omega}{s^2 + \omega^2} - \frac{1}{s^2}\right) \tag{4.15}$$

where $\omega = \frac{1}{\sqrt{L_p C_{Diode}}}$. The formula (4.15) is transformed back into the time domain:

$$\Delta i_{D@t3} = \frac{k_1 + k_2}{\omega} \cdot \sin\ \omega(t - t_3) - (k_1 + k_2) \cdot (t - t_3) \tag{4.16}$$

The oscillation component is demonstrated in the first part of the formula (4.16) as shown in (4.17).

$$i_{Dring@t3} = \frac{k_1 + k_2}{\omega} \cdot \sin\ \omega(t - t_3) \tag{4.17}$$

where $i_{Dring@t3}$ is the oscillation component introduced at t_3. The oscillation is in the form of a sinusoidal waveform, whose magnitude is $\frac{k_1+k_2}{\omega}$ and radian frequency is $\omega = \frac{1}{\sqrt{L_p C_{Diode}}}$.

Similar analysis can also be applied to the state change at t_4, where the slope rate of drain current changes from $-k_2$ to 0. It can be derived that the oscillation on drain current introduced at t_4 is

presented in (4.18):

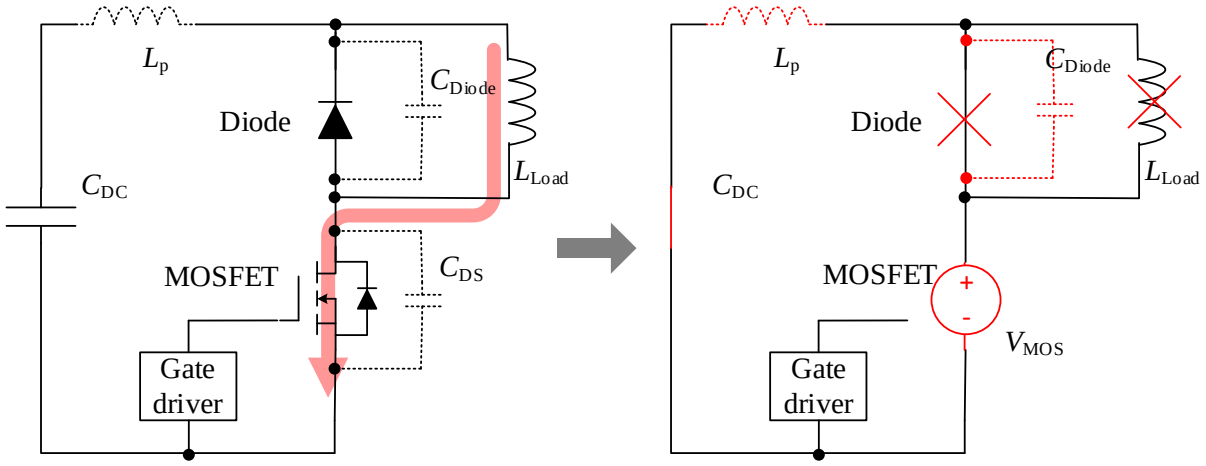
$$i_{Dring@t4} = -\frac{k_2}{\omega} \cdot \sin\ \omega(t - t_4) \tag{4.18}$$

Considering the drain current decline period is relatively short ($t_3 \approx t_4$), the oscillation introduced in the period t_2~t_4 can be calculated as the sum of (4.17) and (4.18).

$$i_{Dring\_t2\sim t4} = \frac{k_1}{\omega} \cdot \sin\ \omega(t - t_3) \tag{4.19}$$

It is shown in (4.19) that the oscillation introduced in the period t_2~t_4 is a sine wave signal, the radiant frequency of the oscillation is $\omega = \frac{1}{\sqrt{L_p C_{Diode}}}$, while the magnitude of the oscillation is $\frac{k_1}{\omega}$, determined by the slope rate of drain current.

Fig. 4-9 demonstrates the current path and the small signal model for the subinterval c. In this period, the diode is totally turned off, which can be regarded as an open circuit in the analysis. For the MOSFET, the voltage of the MOSFET declines in this period, which performs as a voltage source. Therefore, in the small signal model, the load inductor and the diode are modelled as open circuits, the DC capacitor is modelled as a short circuit, and the MOSFET is modelled as a voltage source. The resonant components are the parasitic inductor L_p and the junction capacitance of the diode C_{Diode}. The state of the MOSFET changes at t_5, introducing oscillation in the circuit. The mathematic relationship is illustrated in (4.20) based on the Kirchhoff's law.



(a) Current path (b) Small signal model

Fig. 4-9 Analysis of the turn-on transient in subinterval c: (a) Current path; (b) Small signal model

$$sL_p \cdot i_D + \frac{1}{sC_{Diode}} \cdot i_D + V_{MOS} = 0 \tag{4.20}$$

where v_{MOS} is the voltage of the MOSFET.

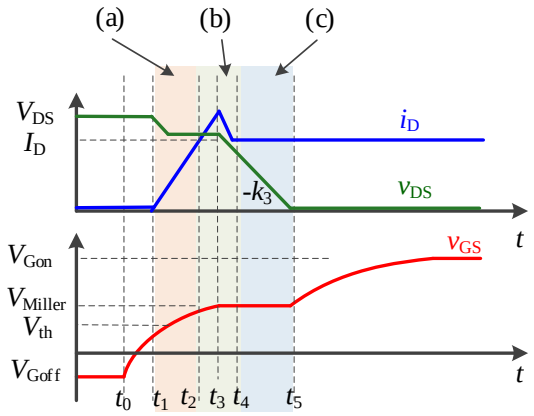


Fig. 4-10 A state change in subinterval c

There is a state change in subinterval c as illustrated in Fig. 4-10. The slope rate of the voltage source changes from $-k_3$ to 0 at t_5. The state change of the voltage source at t_5 can be derived as below.

$$\Delta V_{MOS@t5} = k_3 \cdot (t - t_5) \tag{4.21}$$

where $\Delta V_{MOS@t5}$ is the voltage source introduced at t_5 due to the change of state.

The Laplace form of the voltage source is calculated from (4.23):

$$\Delta V_{MOS@t5} = k_3 \cdot \frac{1}{s^2} \tag{4.22}$$

The corresponding drain current introduced by the change of circuit state can be calculated by substituting (4.22) into (4.20).

$$\Delta i_{D@t5} = \frac{-k_3 C_{Diode}}{s(s^2 L_p C_{Diode} + 1)} \tag{4.23}$$

where $\Delta i_{D@t5}$ is the corresponding drain current introduced at t_5. The formula (4.23) is expressed in the standard form as below:

$$\Delta i_{D@t5} = k_3 \cdot C_{Diode} \cdot (\frac{s}{s^2 + \omega^2} - \frac{1}{s}) \tag{4.24}$$

where $\omega = \frac{1}{\sqrt{L_p C_{Diode}}}$. The formula (4.24) is transformed into time domain:

$$\Delta i_{D@t5} = k_3 \cdot C_{Diode} \cdot \cos\ \omega(t - t_5) - k_3 \cdot (t - t_5) \tag{4.25}$$

The oscillation component is demonstrated in the first part of the formula (4.25) as shown in (4.26).

$$i_{Dring@t5} = k_3 \cdot C_{Diode} \cdot \cos\ \omega(t - t_5) \tag{4.26}$$

The overall oscillation during turn-on transient is the sum of the components introduced in t_2~t_4 and introduced at t_5.

$$\begin{aligned} i_{Dring\_On} &= i_{Dring\_t2\sim t4} + i_{Dring@t5} \\ &= \frac{k_1}{\omega} \cdot \sin \omega(t - t_3) + k_3 \cdot C_{Diode} \cdot \cos\ \omega(t - t_5) \end{aligned} \tag{4.27}$$

It is worth noting that the state change at t_3 is a sharp turning point from k_1 to -k_2, while the state change at t_5 is a relatively slow process from -k_3 to 0. Therefore, the first part $\frac{k_1}{\omega}$ in (4.27) dominates the magnitude of the oscillation. Considering ω is determined by the hardware, the method to reduce turn-on oscillation is to reduce k_1.

4.2.2. *Turn-off Oscillation Model*

The conceptual waveforms in turn-off transient are illustrated in Fig. 4-11, where three subintervals during t_6~t_9 are identified for analysis:

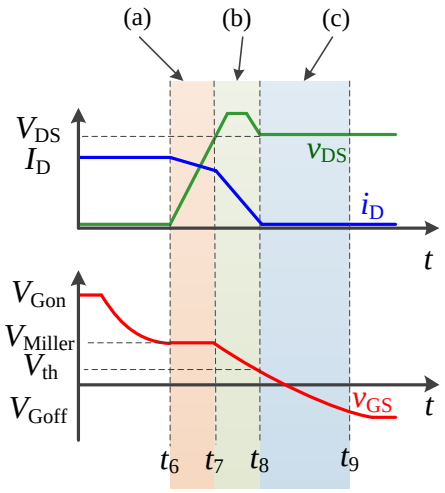


Fig. 4-11 Conceptual waveforms in turn-off transient

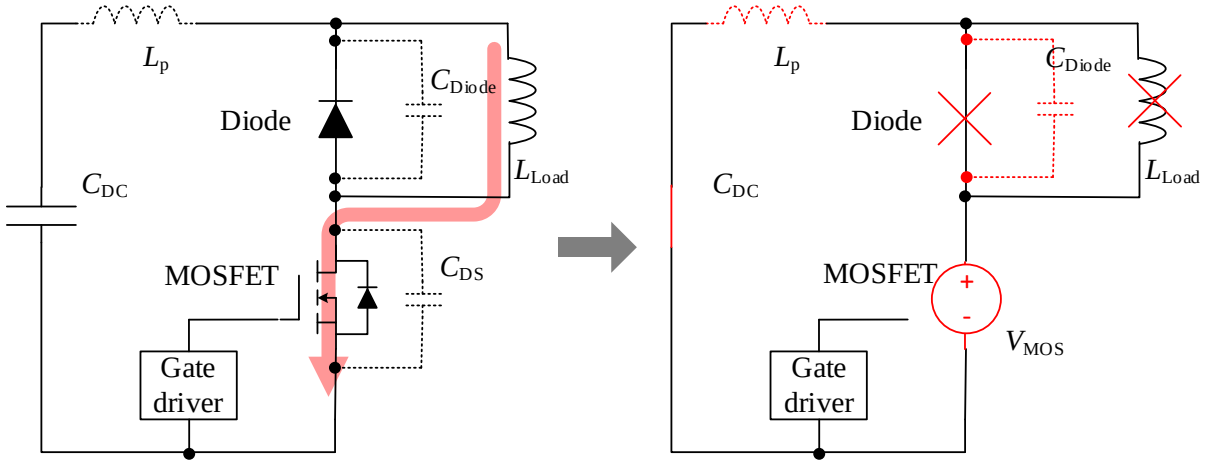
(a) Subinterval t_6~t_7: Drain-source voltage (v_{DS}) increasing stage. The diode is turned off in this period while the MOSFET can be modeled as a voltage source, which is controlled by the gate current. Thereby, a voltage source can be used to describe the characteristics of the MOSFET while the diode can be regarded as open circuit.

(b) Subinterval t_7~t_8: Drain-current (i_D) decreasing stage. The diode is turned on in this period. The MOSFET performs as variable resistor with high impedance. Therefore, a variable resistor can be used to model the MOSFET, while the diode can be simplified as short circuit.

(c) Subinterval t_8~t_9: MOSFET off stage. The MOSFET is regarded as open circuit, while the diode keeps at on-state. Thus, the MOSFET can be modelled as a capacitor, while the diode can be treated as short circuit.

The current path and the small signal model of the turn-off transient in subinterval a are illustrated in Fig. 4-12. In this period, the diode keeps on off-state, which can be regarded as an open circuit in the analysis. For the MOSFET, the slope rate of the MOSFET keeps at k_4 in the period t_6~t_7 as shown in Fig. 4-13. Although there is a state change at t_6, the process for the

voltage slope to change from 0 to k_4 is usually slow, resulting in small oscillation. Moreover, the voltage source performs an increasing impedance when the voltage gets higher. Therefore, the small oscillation introduced at t_6 fades quickly. No oscillation is shown in subinterval a.



(a) Current path (b) Small signal model

Fig. 4-12 Analysis of the turn-off transient in subinterval a: (a) Current path; (b) Small signal model

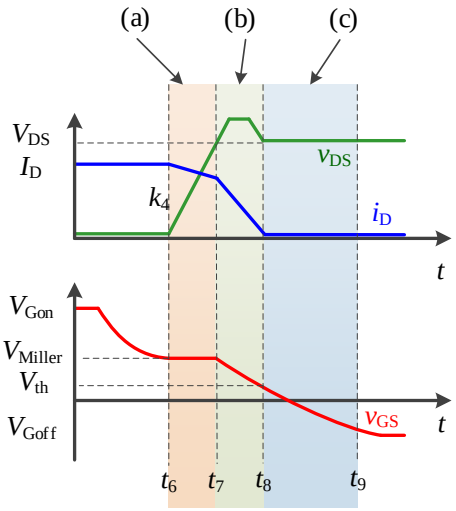
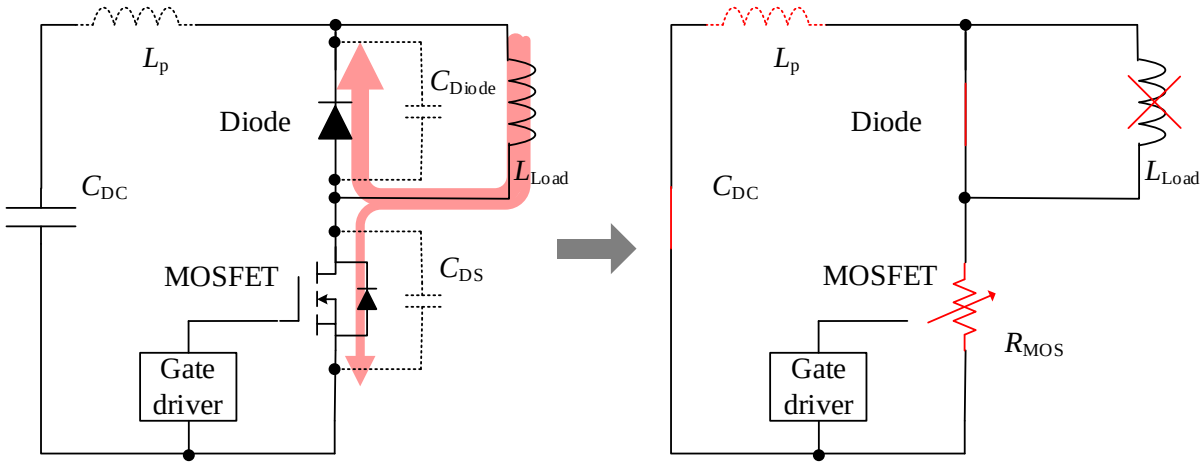


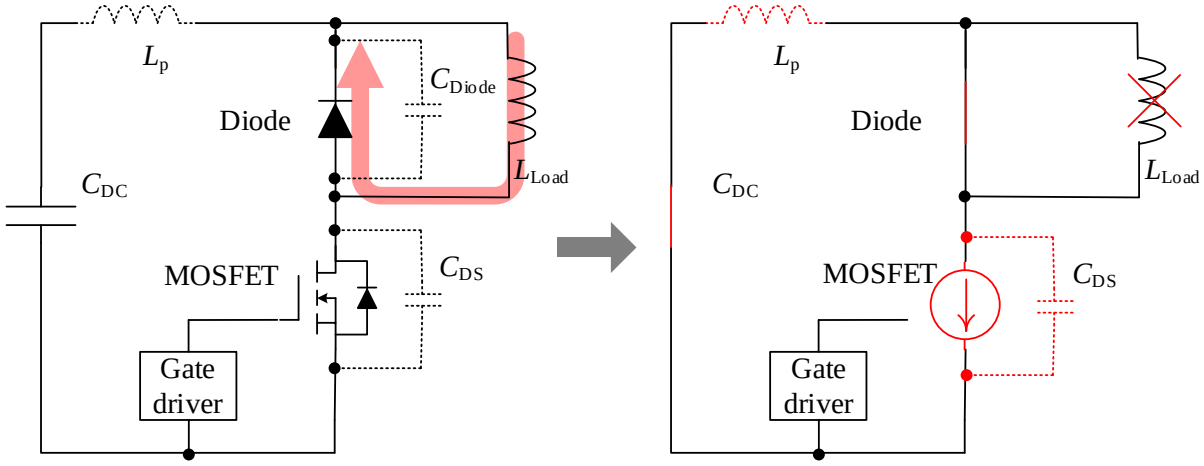
Fig. 4-13 Analysis of the state change in subinterval a

The current path and the small signal model of the turn-off transient in subinterval b are illustrated in Fig. 4-14. The diode starts to conduct current in this period, modelled as a short circuit in the analysis. In the meantime, the MOSFET presents the same effect as a large variable resistor R_{MOS}. It is shown that the small signal model is a first-order circuit, consisting of a resistor R_{MOS} and an inductor L_p. Therefore, there is no oscillation introduced in this period.



(a) Current path (b) Small signal model

Fig. 4-14 Analysis of the turn-off transient in subinterval b: (a) Current path; (b) Small signal model



(a) Current path (b) Small signal model

Fig. 4-15 Analysis of the turn-off transient in subinterval c: (a) Current path; (b) Small signal model

The analysis of the turn-off transient in subinterval c is demonstrated in Fig. 4-15. The current in the MOSFET falls to 0 in this period. Therefore, the MOSFET is modelled as an open circuit in the analysis. All the load current flows through the diode, which performs as a short circuit. However, the slope rate changes in the drain current at t_8 shown in Fig. 4-16 results in the oscillation in L_p and C_{DS}.

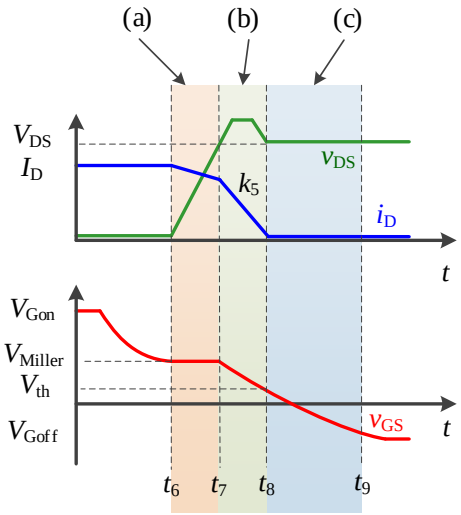


Fig. 4-16 Analysis of the state change in turn-off transient subinterval c

The oscillation source is modelled as a current source I_{MOS}. The drain current before and after t_8 is shown in (4.28) and (4.29):

$$I_{MOS\_t7\sim t8} = -k_5 \cdot (t - t_8) \tag{4.28}$$

$$I_{MOS\_aftert8} = 0 \tag{4.29}$$

The state change in the current source can be derived:

$$\Delta I_{MOS} = k_5 \cdot (t - t_8) \tag{4.30}$$

The Laplace form of the current source is shown:

$$\Delta I_{MOS} = k_5 \cdot \frac{1}{s^2} \tag{4.31}$$

The relationship between the current source and the drain current can be derived according to Kirchhoff's law:

$$sL_p \cdot i_D + \frac{1}{sC_{DS}} \cdot (i_D - I_{MOS}) = 0 \tag{4.32}$$

The drain current can be derived:

$$i_D = \frac{I_{MOS}}{s^2 L_p C_{DS} + 1} \tag{4.33}$$

The corresponding drain current introduced by the oscillation source in (4.31) is shown below:

$$i_{D@t8} = \frac{k_5 \cdot \frac{1}{s^2}}{s^2 L_p C_{DS} + 1} \tag{4.34}$$

The standard form of (4.34) is derived:

$$i_{D@t8} = k_3 \cdot (\frac{1}{s^2} - \frac{1}{\omega} \cdot \frac{\omega}{s^2 + \omega^2}) \tag{4.35}$$

where $\omega = \frac{1}{\sqrt{L_p \cdot C_{DS}}}$.

The Laplace from is inverse transformed into time domain:

$$i_{D@t8} = k_3 \cdot (t - t_8) - \frac{k_3}{\omega} \cdot \cos\ \omega(t - t_8) \tag{4.36}$$

The oscillation component in (4.36) can be extracted:

$$i_{Dring@t8} = -\frac{k_3}{\omega} \cdot \cos\ \omega(t - t_8) \tag{4.37}$$

where the oscillation is a cos waveform, whose radian frequency is $\omega = \frac{1}{\sqrt{L_p \cdot C_{DS}}}$. The magnitude of the oscillation is $-\frac{k_3}{\omega}$. It is shown that the magnitude of the oscillation is determined by the slope rate at t_8.

4.3. Active Gate Driving Signals

Based on the oscillation analysis, the optimized gate driving signals are proposed to suppress the turn-on oscillation and current overshoot, as well as turn-off oscillation and voltage overshoot.

4.3.1. U-Shape Gate Driving Signal for Turn-On Optimization

As is discussed in 4.2.1, the turn-on oscillation is dominated by the transition of di_D/dt at t_3. Therefore, the principle to optimize the turn-on transient is to reduce the slope rate of i_D at t_3. The gate driving signal for turn-on transient optimization is illustrated as the bottom waveform shown in Fig. 4-17. To simplify the calculation, the gradients of i_D and v_{DS} are regarded as

constant under a gate current. This tailored U-shape gate driving signal consists of 2 gate current values: I_{GS_high} and I_{GS_low}. I_{GS_high} is used to generate high di_D/dt during t_1~t_2 subinterval and high dv_{DS}/dt during t_4~t_5 subinterval, which can reduce the turn-on switching loss. Meanwhile, I_{GS_low} is used to reduce the di_D/dt at t_3, which aims to suppress the oscillation and current overshoot. The dip of the gate current starts at t_{U1} and ends at t_{U2}. It worth noting that two more state changes are introduced in the process: high-speed current rising changes to low-speed current rising at t_{U1}, low-speed voltage decline changes to high-speed voltage decline at t_{U2}. The introducing of the current dip changes the steady state of excitation source in Fig. 4-6 and Fig. 4-9. Therefore, the selection of t_{U1} and t_{U2} are discussed using the oscillation models.

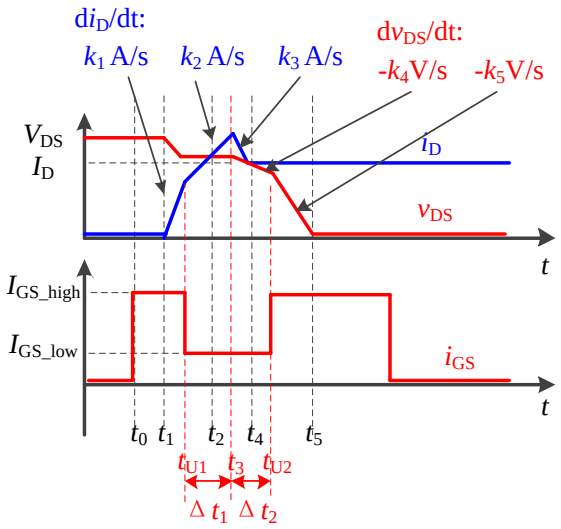


Fig. 4-17 U-shape gate driving signal for turn-on optimization

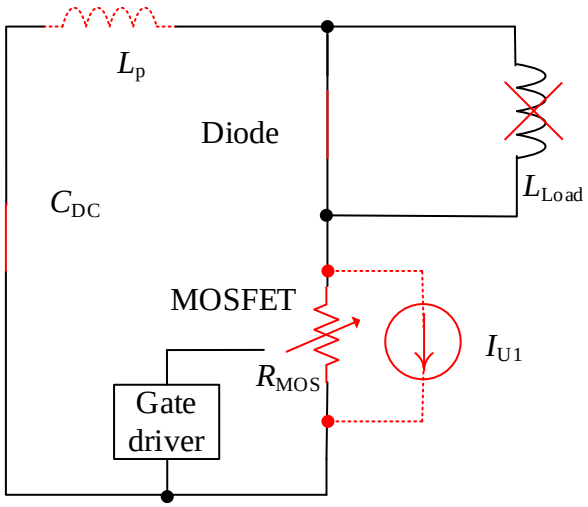


Fig. 4-18 Small signal model introduced by the state change at t_{U1}

Based on the small signal model in Fig. 4-6, the effect of the state changes at t_{U1} is an introduced current source paralleled with R_{MOS} as is shown in Fig. 4-18. The current source represents the behaviour of the MOSFET when its drain current changes rapidly. The excitation source can be derived in (4.38).

$$I_{U1} = -(k_1 - k_2) \cdot (t - t_{U1}) \tag{4.38}$$

The Laplace form of is shown in (4.39).

$$I_{U1} = -(k_1 - k_2) \cdot \frac{1}{s^2} \tag{4.39}$$

The relationship of the drain current and the excitation source is demonstrated in (4.40).

$$sL_p \cdot i_D + R_{MOS} \cdot (i_D - I_{U1}) = 0 \tag{4.40}$$

The corresponding drain current can be calculated.

$$i_{D@U1} = \frac{I_{U1}}{sL_p + R_{MOS}} \tag{4.41}$$

The introduced drain current can be derived by substituting (4.39) into (4.41).

$$i_{D@U1} = -\frac{1}{s^2}\frac{k_1 - k_2}{sL_p + R_{MOS}} \tag{4.42}$$

The standard form of is shown in .

$$i_{D@U1} = (k_1 - k_2)\left(\frac{\frac{L_p}{R_{MOS}}}{s} - \frac{\frac{L_p}{R_{MOS}}}{s + \frac{R_{MOS}}{L_p}} - \frac{1}{s^2}\right) \tag{4.43}$$

Transferred into time domain, the corresponding drain current is shown in

$$i_{D@U1} = k_2 t + (k_1 - k_2)\frac{L_p}{R_{MOS}}\left(1 - e^{-\frac{R_{MOS}}{L_p}t}\right) \tag{4.44}$$

The slope rate of the drain current ($\mathrm{d}i_D/\mathrm{dt}$) can be derived.

$$\frac{di_{D@U1}}{dt} = k_2 + (k_1 - k_2)e^{-\frac{R_{MOS}}{L_p}(t-t_{U1})} \tag{4.45}$$

It is shown in (4.45) that when the gate current changes at t_{U1}, the gradient of drain current starts to decrease from k_1 towards k_2 following an exponential function until t_3. As shown in Fig. 4-17, the transient time $\Delta t_1 = t_3 - t_{U1}$ determines the gradient of drain current (di_D/dt) at t_3. Considering that the turn-on current overshoot ($i_{D\_overshoot}$) is dominated by di_D/dt, it can be inferred that the relation of $i_{D\_overshoot}$ and Δt_1 follows the exponential function.

To verify the analysis, a numerical model is established in LTspice to study the switching transients as presented in Fig. 4-5. In this circuit, a datasheet based Pspice model of SiC MOSFET (SCT3060) is used as the device under test, rating at 650V/39A. The body diode of C3M0065090D is used as the top device, rating at 900V/36A. The parasitic inductance L_p in the simulation is 120nH. The load inductance is 250uH. The simulation is conducted under 400V DC voltage and the simulated load current is 10A. The simulated waveforms of i_D under different Δt_1 are illustrated in Fig. 4-19, where the gate current i_{GS} changes from I_{G_high}(100mA) to I_{G_low}(5mA) at different times to generate different transient period Δt_1. It is shown that a higher Δt_1 introduces a lower i_D overshoot. Moreover, the quantitative relation of $i_{D\_overshoot}$ and Δt_1 is plotted in Fig. 4-20. It is shown that the relation of $i_{D\_overshoot}$ and Δt_1 follows the exponential function. It is worth noting that R_{MOS} is not constant in the subinterval t_1~t_3, consequently, it is difficult to calculate Δt_1 precisely. However, the correlation between di_D/dt and Δt_1 is enough to provide the strategy to reduce the oscillation: a higher Δt_1 results in a lower di_D/dt, lower oscillation, and lower current overshoot.

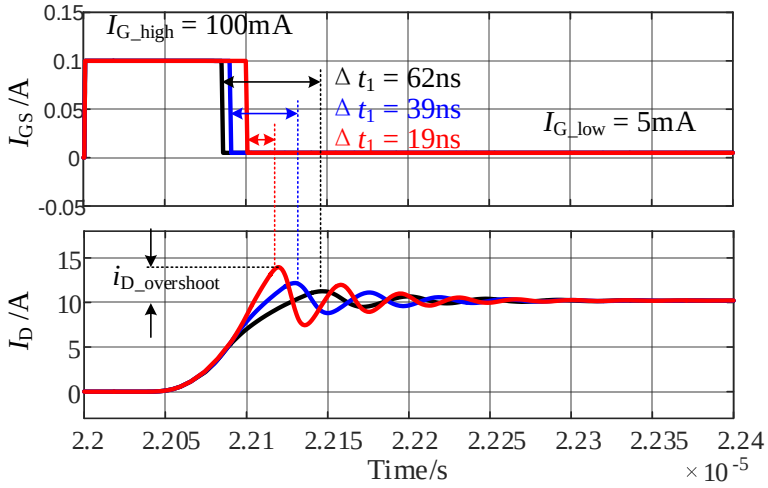


Fig. 4-19 Simulated waveforms of i_D under different Δt_1

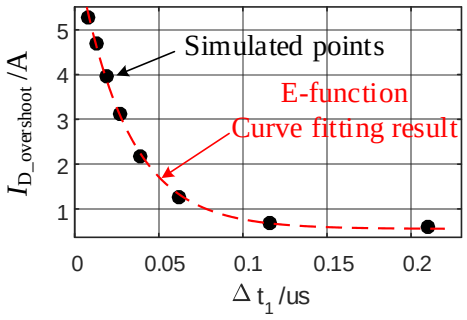


Fig. 4-20 Simulated $i_{D\_overshoot}$ vs Δt_1

According to the analysis in 4.2.1, the oscillation introduced at t_3 is illustrated in (4.46):

$$i_{Dring1} = (k_2 + k_3)\sqrt{L_p C_{Diode}}\sin(t - t_3) \tag{4.46}$$

where i_{Dring1} is the oscillation current on i_D. k_2 and k_3 are the current slopes before and after t_3 shown in Fig. 4-17.

The jump of gate current at t_{U2} introduces a state change in period c as shown in Fig. 4-9. The excitation source V_{MOS} changes from $V_{MOS} = -k_4 t$ to $V_{MOS} = -k_5 t$, where $-k_4$ and $-k_5$ ($k_5 > k_4 > 0$) are the slope of drain-source voltage v_{DS} before and after t_{U2}, respectively. The excitation source change is $V_{MOS} = -(k_5 - k_4) \cdot t$.

According to the analysis in 4.2.1, the oscillation introduced at t_{U2} is illustrated in (4.47)

$$i_{Dring2} = -(k_5 - k_4)C_{Diode}\sqrt{L_p C_{Diode}}\cos(t - t_{U2}) \tag{4.47}$$

where i_{Dring2} is the introduced oscillation component at t_{U2}, $\omega = 1/\sqrt{L_p \cdot C_{Diode}}$ is the radian frequency, the magnitude is $(k_5 - k_4)C_{Diode}\sqrt{L_p \cdot C_{Diode}}$.

It is worth noting that there is another state change at t_5, but the process is usually slow for the voltage to fall to zero. In the contrast, the turning point at t_3 and t_{U2} are very sharp. Therefore, the oscillation introduced at t_5 is neglected.

The ringing of i_D ($i_{D\_ringing}$) consists of the oscillation introduced at t_3 and t_{U2}. Therefore, the expression of $i_{D\_ringing}$ is derived in (4.48) as:

$$i_{Dring} = i_{Dring1} + i_{Dring2} = A\sin[\omega(t - t_3)] - B\cos[\omega(t - t_{U2})] \quad (4.48)$$

where $A = (k_2 + k_3)\sqrt{L_p \cdot C_{Diode}} > 0$ is the magnitude of the oscillation occurs at t_3, $B = (k_5 - k_4)C_{Diode}\sqrt{L_p \cdot C_{Diode}} > 0$ is the magnitude of the oscillation introduced by the jump of gate current at t_{U2}. It is shown in (4.48) that the oscillation is the combination of 2 trigonometric functions. Assuming no control is applied at t_{U2}, the magnitude of the oscillation is A. The introduction of the second cosine waveform at t_{U2} has opposite effect depending on the phase difference: if $\Delta t_2 = t_{U2} - t_3 = \frac{\pi}{2\omega}$, $i_{Dring} = (A - B)\sin[\omega(t - t_3)]$, the oscillation magnitude is reduced from A to A-B; in contrast, if $\Delta t_2 = t_{U2} - t_3 = \frac{3\pi}{2\omega}$, $i_{Dring} = (A + B)\sin[\omega(t - t_3)]$, the oscillation magnitude is increased from A to A+B. It is worth to note that the precondition of the analysis is A>B. If A<B, A can be increased by manipulating Δt_1 as shown in (4.45). As a result, it can be guaranteed that A>B. Therefore, the magnitude of ringing is also influenced by Δt_2.

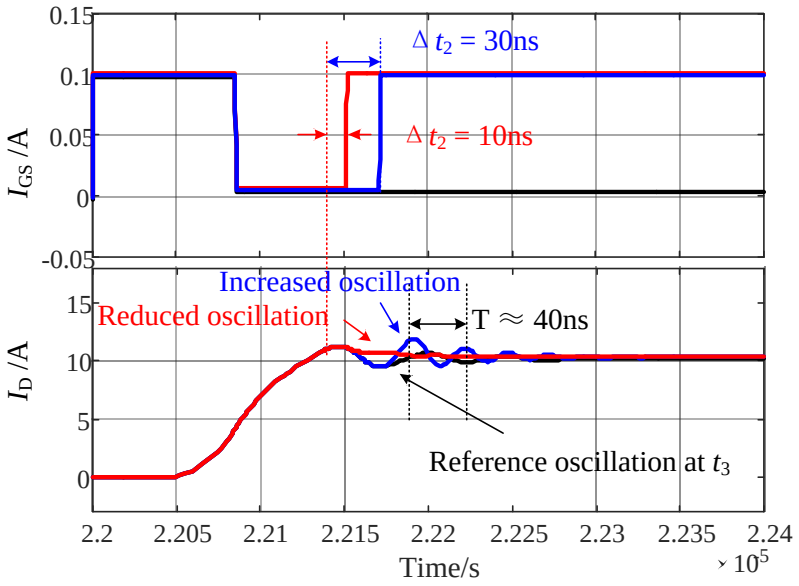


Fig. 4-21 Simulated waveforms of i_D under different Δt_2

The analysis is verified in the simulation shown in Fig. 4-21, where the simulation condition is the same as Fig. 4-19 under 400V/10A. The transient period Δt_1 equals to 60ns, while t_{U2} at different timings are compared. The top waveforms are the gate currents (I_{GS}), the bottom waveforms are the drain current (I_D). The oscillation at t_3 without gate current jump at t_{U2} is demonstrated in black waveforms as the reference oscillation. Compared with the reference oscillation, the oscillation is increased when $\Delta t_2 = \frac{3T}{4}$(as the blue waveforms shown), while it is decreased when $\Delta t_2 = \frac{T}{4}$ (demonstrated in red waveforms). $T = 2\pi\sqrt{L_p C_{Diode}}$ is the period of the oscillation in subinterval t_3~t_5.

Based on the analysis, the position of gate current dip t_{U1} and t_{U2} can be determined. $\Delta t_1 = t_3 - t_{U2}$ has an exponential relation with the overshoot of i_D as shown in Fig. 4-20. $\Delta t_2 = t_{U2} - t_3$ has significant influence on the oscillation: a proper selection of t_{U2} minimizes the oscillation when $\Delta t_2 = \frac{T}{4}$, while a bad timing of t_{U2} increases the ringing when $\Delta t_2 = \frac{3T}{4}$. $T = 2\pi\sqrt{L_p C_{Diode}}$ is the period of the oscillation.

4.3.2. N-Shape Gate Driving Signal for Turn-On Optimization

As is proposed in 4.2.2, the oscillation is determined by the gradient of drain current (di_D/dt) at t_8 shown in Fig. 4-11. Therefore, the N-shape gate driving signal for turn-off switching transient

optimization is proposed in Fig. 4-22. A gate current dip is introduced from t_n to t_8 to reduce the oscillation, where t_8 is the time when i_D reaches 0. The state of the circuit is changed at t_n, as the gradient of i_D drops $-k_6$ to $-k_7$ ($k_6 > k_7 > 0$). The transient period of the introduced state is Δt_3 shown in Fig. 4-22.

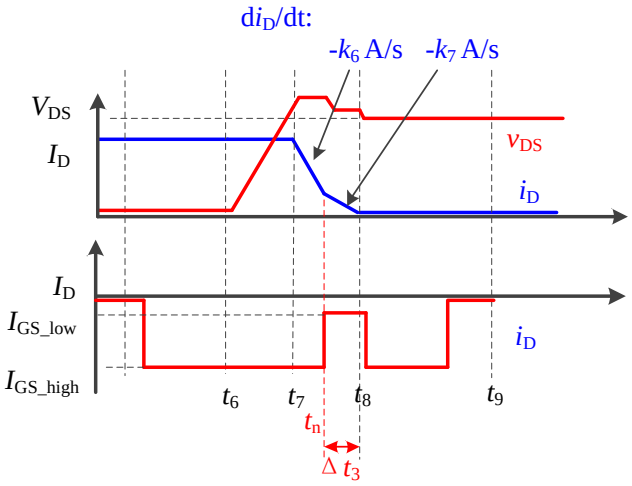


Fig. 4-22 N-shape gate driving signal for turn-off optimization

According to the developed small signal model shown in Fig. 4-14, the state of the voltage source changes from $-k_6 t$ to $-k_7 t$, introducing an excitation source as shown in Fig. 4-23. The excitation source is demonstrated in (4.49).

$$I_{U2} = (k_6 - k_7)(t - t_{U2}) \tag{4.49}$$

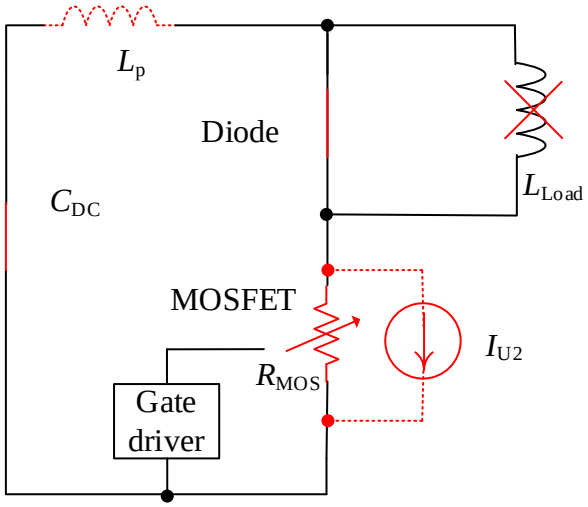


Fig. 4-23 Small signal model introduced by the state change at t_{U2}

Considering that the small signal model is the same as Fig. 4-18, the corresponding drain current can be derived in .

$$i_{D@U2} = -k_7 t - (k_6 - k_7)\frac{L_p}{R_{MOS}}\left(1 - e^{-\frac{R_{MOS}}{L_p}t}\right) \tag{4.50}$$

The gradient of i_D is calculated:

$$\frac{di_{D@U2}}{dt} = -k_7 - (k_6 - k_7)e^{-\frac{R_{MOS}}{L_p}t} \tag{4.51}$$

Similar to the analysis on (4.19), the gradient of drain current starts to decrease from -k_6 towards k_7 in the period Δt_3. According to (4.37), the oscillation is determined by di_D/dt at t_8. As a result, the oscillation is reduced depending on the time interval Δt_3. Moreover, it is shown that the relation of the oscillation and Δt_3 follows the exponential function.

The simulated waveforms of i_D under different Δt_3 verifies that a longer time Δt_3 results in a lower oscillation. The simulation is conducted as shown in Fig. 4-24 under 400V DC voltage and 10A load current. The gate current i_{GS} changes from I_{G_high}(-400mA) to I_{G_low}(-5mA) at different times to generate different transient time Δt_3. The oscillation is quantized by the undershoot of drain current ($i_{D\_undershoot}$). The overshoot of drain-source voltage ($v_{DS\_overshoot}$) is also reduced with a longer Δt_3 due to the decrease of di_D/dt. Moreover, the relation of $i_{D\_undershoot}$ and Δt_3 is plotted in Fig. 4-25s. It is shown that the relation of $i_{D\_undershoot}$ and Δt_3 follows the exponential function.

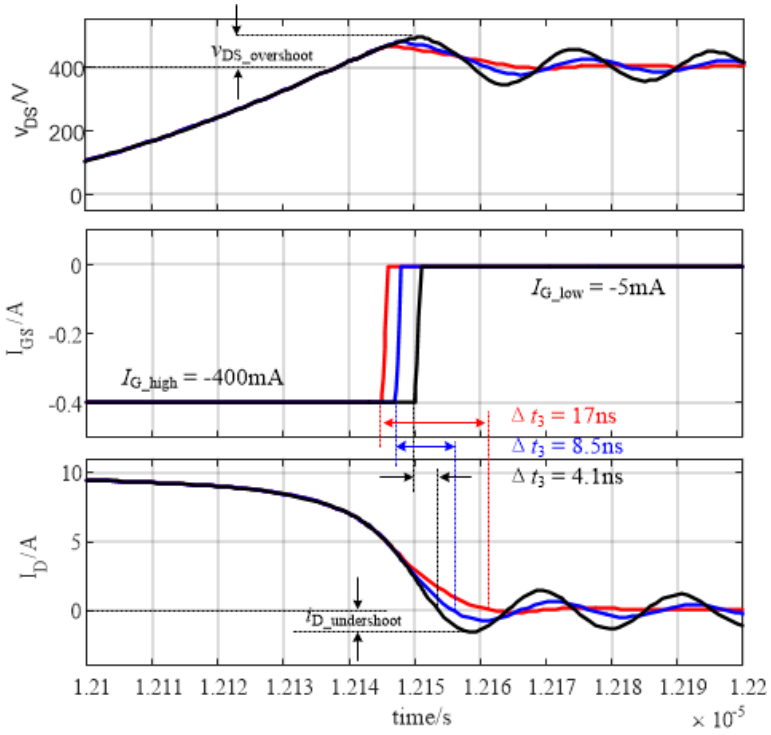


Fig. 4-24 Simulated waveforms of i_D under different Δt_3

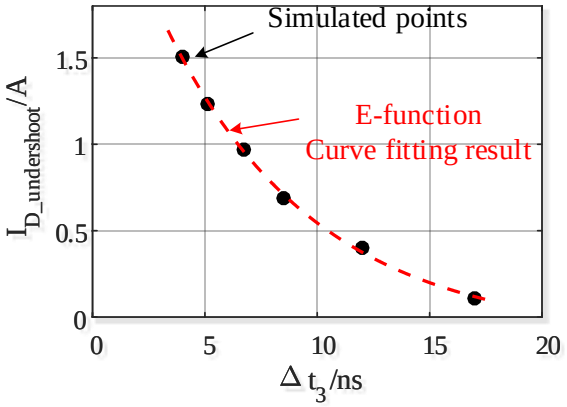


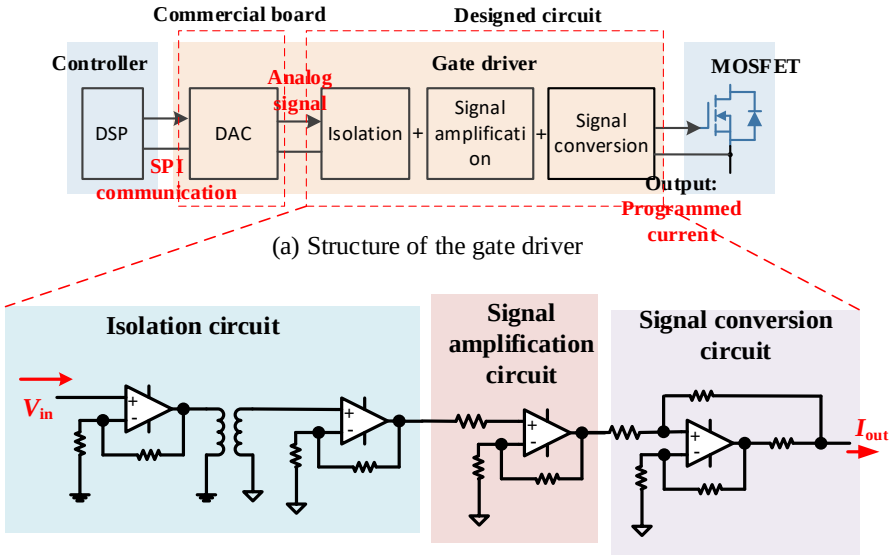
Fig. 4-25 Simulated $i_{D\_undershoot}$ vs Δt_3

Based on the analysis, the position of gate current dip is determined starting from t_n to t_8. The time interval $\Delta t_3 = t_8 - t_n$ has an exponential relation with the oscillation: a larger time interval Δt_3 introduces lower oscillation. Moreover, the voltage overshoot is determined by di_D/dt from t_7 to t_8, therefore, a longer gate current dip covering the period t_7~t_8 can suppress the voltage overshoot.

4.4. Experimental Verification

4.4.1. Active Gate Driver

A current-control active gate driver is designed to evaluate the proposed gate driving signals. The structure of the gate driver structure is illustrated in Fig. 4-26(a), while the schematic of the designed gate driver is demonstrated in Fig. 4-26s (b).



(a) Structure of the gate driver

(b) Schematic of the gate driver

Fig. 4-26. Diagram of the active gate driver

The control signal can be programmed and stored in a DSP controller, then, this signal is transmitted to a DAC (Digital to analog converter) via SPI communication. With the designed gate driver circuit, the analog signal is converted into a corresponding current signal injected into the gate of the MOSFET.

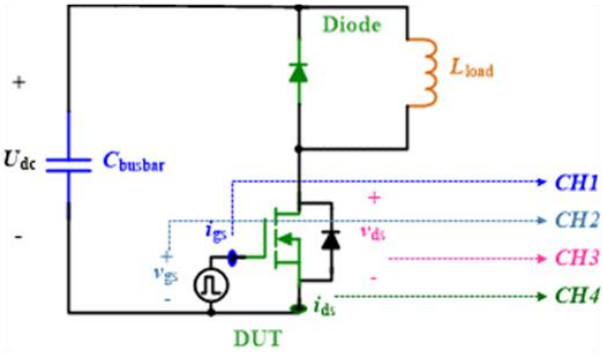
Table 4-1 performance of the active gate driver

Parameters	Value
Output voltage range	-5V~15V
Output current range	0~200mA
Time step	13.3ns ~ 10us

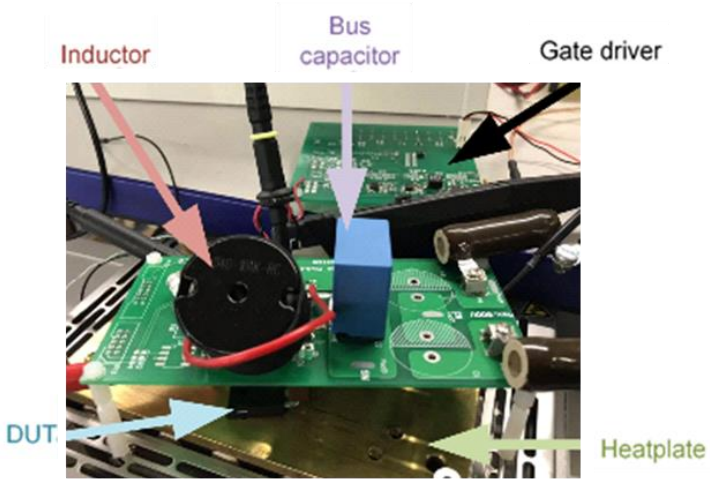
This current-source gate driver has a simple structure with three functional parts: isolation circuit, signal amplification circuit and signal conversion circuit. The input signal V_{in} is signal generated by the DAC. This signal is isolated and amplified before converted into a current signal. A transformer is used to isolate V_{in} while amplifiers are used to convert V_{in} into current signal I_{out}. There are 3 main functions of the proposed gate driver: firstly, the gate driver serves

as the isolator to keep the control system safe from the high voltage of the power circuit; Besides, the small input signal generated by the controller is amplified from less than 1V to the gate voltage level (-5V to 15V); Finally, the voltage signal is converted into the current signal, which means the shape of the output current follows the control of the input voltage signal. The performance of the active gate driver is presented in Table 4-1. The time step is the duration time of each output current value, for example, the duration time of the gate current dip, while the minimum time step can be achieved is 13.3ns.

4.4.2. Construction of Double-Pulse Test



(a) schematic of the platform



(b) picture of the platform

Fig. 4-27. Double pulse test platform, (a) schematic of the platform (b) picture of the platform

A double-pulse test platform is constructed as is shown Fig. 4-27. When the DUT is turned on, the current is conducted through the inductor and increases until it reaches the test current. Then the DUT is turned off and the current path changes from the DUT to the top device; after a short period, the DUT is turned on again, and the switching transient of the device under test is

captured using an oscilloscope. In the experiment, the DUT is the trench SiC MOSFET SCT3060, while the diode is the body diode of power device C3M0065090D. The experiment is conducted under 250V DC voltage and the load current is 10A.

4.4.3. Performance of Gate Driving Signals

As is stated in Chapter 3, the minimum time step the proposed gate driver can achieve is 13.3ns, which means it cannot be used if the switching speed is very fast (<100ns). The experiments presented in this subsection are conducted under low speed switching condition, where the switching time is around 500ns. The influence of low speed is discussed after the presentation of the results.

A. Turn on performance

The U-shape turn-on gate signal is used to evaluate the turn-on performance, compared with the constant gate current signal as shown in Fig. 4-28. The reference signal is a constant gate current signal (blue), which is kept at I_{GS1} for the entire turn-on period. The active gate current signal is the U-shape signal (red), whose value is kept at I_{GS1} for time T_1 and changed to a lower value I_{GS2} for time T_2. From the analysis in 4.3.1, it is expected that a lower current overshoot will be introduced by reducing T_1. Therefore, experiments are conducted to verify the analysis.

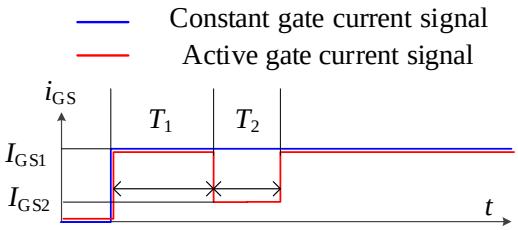


Fig. 4-28 Diagram of the turn-on gate signals used in the experiment

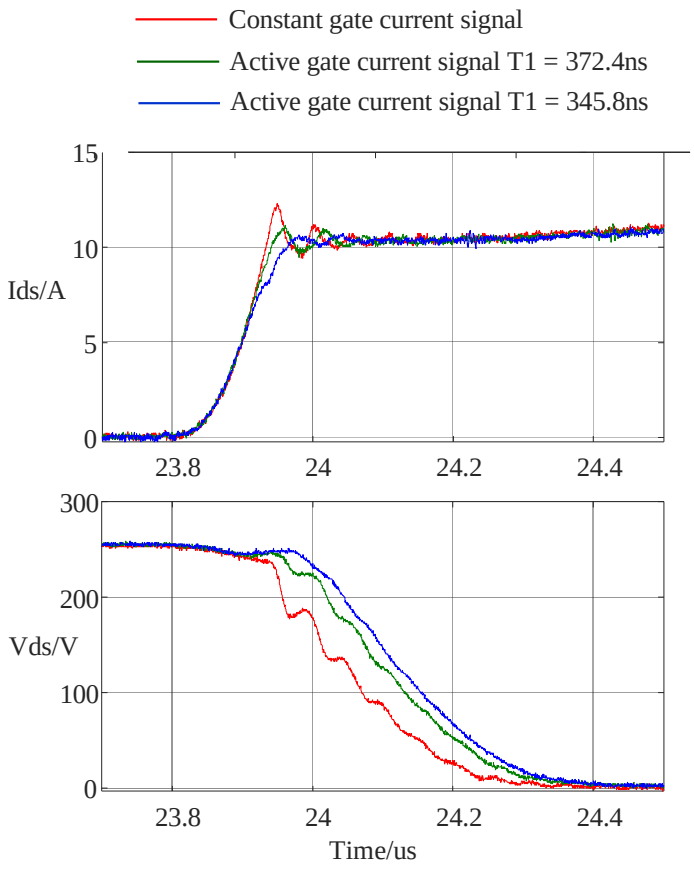


Fig. 4-29 Turn on waveforms of drain current under different gate signals

The turn on waveforms of the drain currents and the drain-source votlages under different gate signals are presented in Fig. 4-29. The experiments are conducted under 25°C, the test voltage is 250V, the test current is 10A, the device under test is SCT3060. The red waveform is the drain current of the MOSFET under a constant gate current signal. The value of the gate current (I_{GS1} in Fig. 4-28) is 50mA. The measured current overshoot is 2.24A. The green waveform is the drain current of the MOSFET under the active gate current signal when T_1 = 372.4ns. The gate current is kept at 50mA for T_1 = 372.4ns, then changed to 14mA (I_{GS2}) at 23.933us for 93.1ns. It is shown in the green waveform that the measured current overshoot is 1.28A, which is reduced by 42.8% compared with the constant gate current signal (2.24A). The drain-source voltage v_{ds} is delayed by 64ns with the same slew rate. T_1 is changed to 345.8ns presented as the blue waveform. The other parameters are the same as the blue waveform (I_{GS1} = 50mA, I_{GS2} = 14mA, T_2 = 93.1ns). The waveform shows that the current overshoot is further reduced to 0.40A(reduced by 82.1%) if T_1 is 2 steps smaller (26.6ns) than it in the green waveform. At the

same time, v_{ds} is delayed by 89ns while its slew rate keeps the same. The results verify the analysis in 4.3.1 that the proposed U-shape gate current signal is effective in reducing the current overshoot during turn on, and smaller T_1 introduces lower current overshoot.

B. Turn off performance

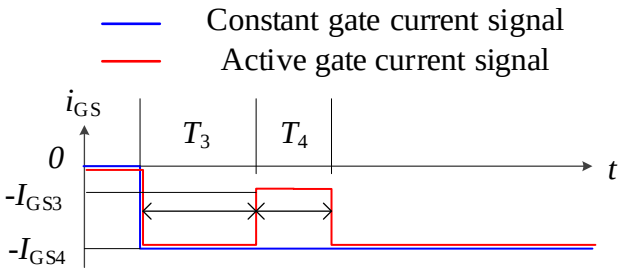


Fig. 4-30 Diagram of the turn-off signals used in the experiment

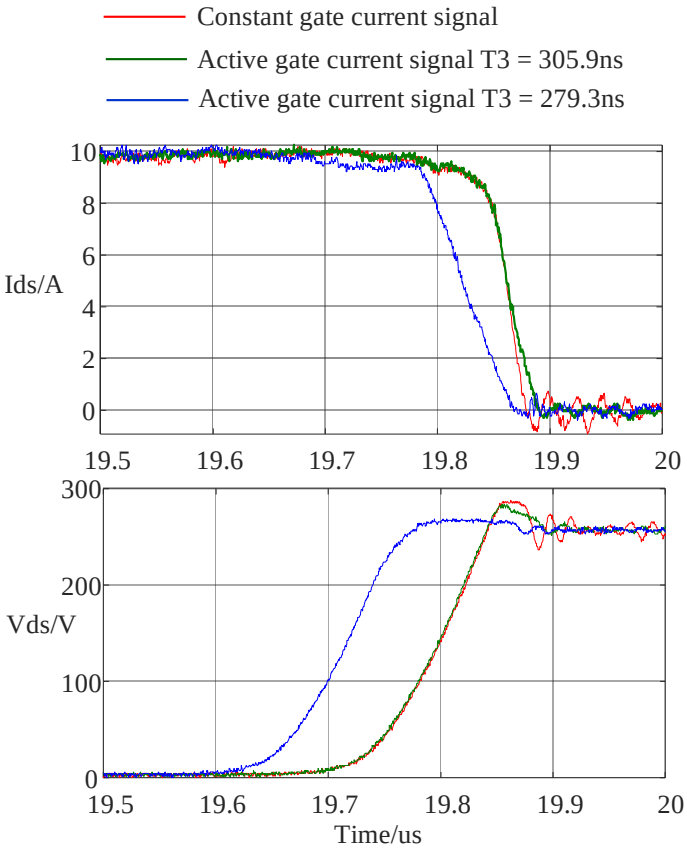


Fig. 4-31 Turn off waveforms of the drain-source voltage under different gate signals

The N-shape turn-on gate signal is used to evaluate the turn-on performance, compared with the constant gate current signal as shown in Fig. 4-30. The reference signal is a constant gate current signal (blue), which is kept at $-I_{GS4}$ for the entire turn-on period. The active gate current

signal is the N-shape signal (red), whose magnitude is kept at I_{GS4} for time T_3 and changed to a lower value I_{GS3} for time T_4. From the analysis in 4.3.2, it is expected that a lower voltage overshoot will be introduced by reducing T_3. Therefore, experiments are conducted to verify the analysis.

The turn off waveforms of the drain-source voltages and the drain curents under different gate signals are presented in Fig. 4-31. The test condition is the same as the turn-on tests. As is shown in Fig. 4-31, the red waveform is the waveform of v_{ds} and i_{ds} under a constant gate current signal. The magnitude of the gate current (I_{GS4} in Fig. 4-30) is 100mA. It is shown that the voltage overshoot is 44V. In order to reduce the voltage overshoot, N-shape gate current signals are used to turn-off the MOSFET. The green waveform is the v_{ds} under the active gate current signal when T_3 = 305.9ns. The magnitude of gate current is kept at 100mA for 305.9ns, then changed to 14mA (I_{GS3}) for 106.4ns (T_4 in Fig. 4-30). It is shown in the green waveform that the measured voltage overshoot is 33V, which is reduced by 25.0% compared with the constant gate current signal (44V). Moreover, the slew rates of V_{ds} and I_{ds} keep the same, which means no extra loss is introduced by using the N-shape gate current. The waveforms of V_{ds} and I_{ds} when T_3 = 279.3ns is presented as the blue waveforms. The other parameters are the same as the blue waveform (I_{GS4} = 100mA, I_{GS3} = 14mA, T_4 = 106.4ns). The waveform shows that the voltage overshoot is further reduced to 11V(reduced by 75.0%) if T_3 is 2 step smaller (26.6ns) than it in green. Although the voltage overshoot is reduced significantly, the decrease of T_3 results in a lower di/dt, which introduces more loss. The results verify the analysis in 4.3.2 that the proposed N-shape gate current signal is effective in reducing the voltage overshoot during turn on, and smaller T_3 introduces lower voltage overshoot.

C. Comparison between the proposed method and the conventional method

The previous results are the performance of the proposed signals on the overshoots. This part presents the comparison between the proposed method and the conventional method. In the conventional method, a voltage-source gate driver is used to control the MOSFET. A higher gate resistor introduces lower overshoots. In this experiment, a gate resistor of 100Ω is used to generate the original switching waveforms as the black waveforms shown in Fig. 4-32. It can

be calculated that the current overshoot in turn on is 1.92A, the voltage overshoot in turn off is 28V, the turn on loss is 0.36mJ, and the turn off loss is 0.24mJ.

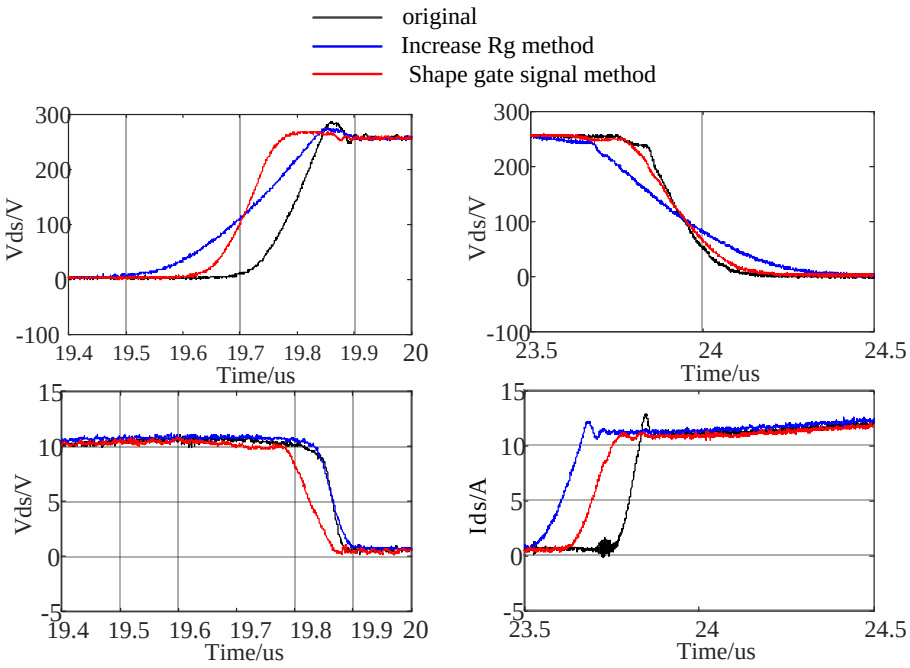


Fig. 4-32 Experiment waveforms of active gate driver compared with conventional gate driver

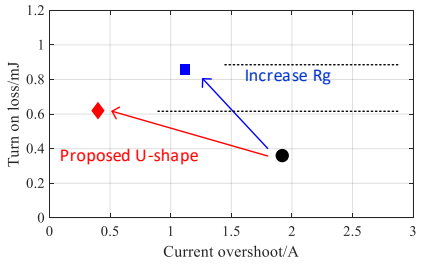
The overshoots of the original waveforms are reduced using two methods. The conventional method is to increase the gate resistor R_g, namely increase R_g method. A larger resistor of 235Ω is used in the test, resulting in a lower switching speed and lower overshoots. The waveforms are shown in blue in Fig. 4-32. It is calculated that the current overshoot in turn on decreases to 1.12A (reduced by 41%), the voltage overshoot in turn off decreases to 19V(reduced by 32.1%), the turn on loss increases to 0.86mJ (increased by 138.9%), and the turn off loss increases to 0.40mJ (increased by 66.7%).

Table 4-2 Comparison of the proposed method and the conventional method

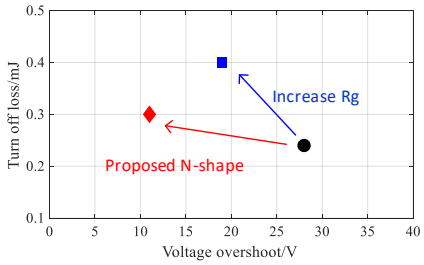
Switching performance	Turn-on loss	Turn-off loss	Current overshoot	Voltage overshoot
No suppression	0.36mJ	0.24mJ	1.92A	28V
Convention suppression method	0.86mJ	0.40mJ	1.12A	19V
Proposed suppression method	0.62mJ	0.30mJ	0.40A	11V

The proposed method is to shape the gate current signal with the proposed signals presented in Fig. 4-28 and Fig. 4-30. The waveforms are shown in red in Fig. 4-32. The active gate signals

used in the test are the turn on signal when T_1 = 345.8ns and T_2 = 93.1ns and the turn off signal when T_3 = 279.3ns and T_4 = 106.4ns. Compared with the conventional method, the proposed method presents better results on the overshoots suppression. The current overshoot in turn on is reduced to 0.40A (reduced by 79.1%), while the voltage overshoot in turn off is reduced to 11V (reduced by 60.7%). In addition, the increase in loss is also less than the conventional method: the turn on loss increases to 0.62mJ (increased by 72.2%), while the turn off loss increases to 0.30mJ (increased by 25%). The performances are summarized in Table 4-2. It is verified that the proposed method presents better performance in both overshoots and losses.



(a) turn-on transient



(b) turn-off transient

Fig. 4-33 Comparison between proposed method and conventional method to reduce switching oscillation (a) turn-on (b) turn-off

The comparison between the proposed method and the conventional method is summarized in Fig. 4-33. The x-axis is the overshoot, while the y-axis is the loss. The positions of the points reflect the performance of the switching condition. Points closer to the original point (0,0) reflects better performance. For the conventional method, the points move from the black to blue, showing lower overshoots but higher losses. Meanwhile, the red points are the performance of the proposed signals. It is shown that the red points are closer to (0,0) than blue points, which means that both the losses and the overshoots are less than the conventional method.

D. Discussion

In the theoretical analysis and simulation, there are quantitative conclusions, including the exponential relationship between current overshoot and t_{U1}, and the sinusoidal relationship between the current overshoot and t_{U2}. Moreover, the optimum signal can be derived using the functions presented in 4.3. However, in the experiment, the active signals are not calculated from the equations. There are two reasons for not using equations to calculate the gate signal shape. Firstly, there is a variable in the equation, R_{MOS}, which is the equivalent resistance of the MOSFET during the switching transient. The value of R_{MOS} keeps changing during the switching transient, which makes it difficult to solve the equations. Secondly, due to the limitation of the proposed gate driver, the minimum time step can be achieved is 13.3ns, which means the time interval of each steps (T_1 and T_2 in Fig. 4-28, T_3 and T_4 in Fig. 4-30) must be a multiple of 13.3ns. It is very likely that the calculated point cannot be achieved by the proposed gate driver.

Although there are difficulties in applying the equations in the proposed gate driver, the analysis provides the guidance to select each time interval (T_1 and T_2 in Fig. 4-28, T_3 and T_4 in Fig. 4-30). For the turn on transient, the analysis shows that the low gate current dip period is supposed to start from the drain current rising period and end at the maximum drain current. For the turn off transient, the low gate current period should cover the drain current decreasing period. The experiment results verify that the U-shape gate driving signal improves the turn-on performance with lower oscillation while the N-shape gate driving signal brings lower voltage overshoot during the turn-off transient. However, due to the limitation of the time resolution of the controller, the analysis about T_2 cannot be verified. Higher resolution can be achieved with high-speed DAC, for example DAC38RF80 from Texas Instruments (TI).. The amplifier should also be changed to amplifiers with higher output current and higher bandwidth, for example THS3491 from Texas Instruments (TI).

4.5. Summary

This section proposes active gate driving methods for SiC MOSFET to reduce overshoots and oscillations. Three active gate driving strategies are compared and it is shown that the gate

current control strategy is more directive and more effective compared to the other two strategies. Moreover, the inherent mechanism of producing switching oscillations is revealed and analyzed using the developed small signal models. In the light of this analysis, the optimized U-shape/N-shape gate current signals are proposed for switching overshoots suppression. The effectiveness of the proposed gate current signals has been verified in the experiments, demonstrating that it outperforms traditional methods for reducing overshoots and oscillations.

Chapter 5 Investigation into Threshold Voltage Shift

As demonstrated in Section 2.2, the threshold voltage shift is important for the health monitoring of power MOSFET. This chapter presents the investigation into threshold voltage shift in the following aspects: 1. An innovative threshold voltage measurement method is proposed, which is easier to be applied to practical converters compared with the traditional V_{th} measurement method; 2. The relation between the threshold voltage shift and the gate stress time is studied using the proposed V_{th} measurement method; 3. The short-time V_{th} shift within 1us is investigated and described with a logarithmic equation, including the double-layer charge trap model proposed to illustrate the V_{th} shift process; 4. The methods are discussed to decouple the influence of temperature on V_{th} shift; 5. The feasibility of the proposed V_{th} measurement method is discussed in different applications.

5.1. V_{th} Measurement Method

The measurement of V_{th} in most of the works are conducted in laboratory condition with complicated equipment[92], which can be difficult to be applied to practical converters. In order to measure V_{th} online, the concepts of "quasi-threshold voltage"[94][89] and "pre-threshold voltage"[93] are proposed. Nevertheless, high-speed circuitry is required to detect the events of gate voltage rise and drain current rise from a zero level[110] in all the aforementioned works. Furthermore, the faster the devices switch, the higher bandwidth of the measurement circuitry is required. Therefore, it is more challenging to apply the conventional V_{th} measurement method to SiC MOSFETs. This section presents a new approach to measure the gate threshold voltage without complicated measurement circuit.

5.1.1. Principle of the Proposed Method

The relationship between the drain current i_D and the gate voltage v_{GS} in saturation region is described in (4.1). It is shown that the gate voltage v_{GS} equals the threshold voltage V_{th} when the MOSFET starts to conduct the drain current. In practice, the gate voltage is regarded as V_{th} when a small drain current is conducted. With the help of the proposed current-controlled gate driver, the required small current can be generated without complicated equipment, enabling

the possibility to measure V_{th} in practical converters.

The principle of the proposed method is illustrated in Fig. 5-1. It is worth noting that Fig. 5-1 only presents the connection with a single MOSFET, the rest of the circuit can be different topologies like a DC/DC converter or a multi-level converter. Detailed discussion is proposed in the application of the proposed method in section 5.5. There are two working modes in the proposed method: operating mode and measuring mode. Operating mode is used for normal operation, while the measuring mode only works when the device is not operating. The threshold voltage is measured in measuring mode, with the help of the proposed current-source gate driver. The current-source gate driver can be programmed to generate normal PWM gate driving signal in operating mode. Meanwhile, it can also be programmed to generate detection gate driving signal in measuring mode. A controlled high voltage switch *S* connects the gate terminal and the drain terminal of the device, introducing the change between the two modes. In operating mode, the switch S is turned off, blocking the high voltage over the drain and the gate. The device works normally to be turned on and off under the PWM gate driving signal. The system can be changed to measuring mode when the switch S is turned on. In this mode, the gate and drain terminals are shorted and a constant gate current is generated by the current-controlled gate driver. The gate current firstly charges the gate-source capacitance of the device and boosts the gate voltage from off-state gate voltage to the gate threshold voltage. When the gate voltage reaches the threshold voltage, a conducting path between the drain and source terminals starts to form. Once the gate current is conducted through drain to source, the gate voltage stops to increase and stays constant at the threshold voltage. The signal sequence of the operating mode and measuring mode are demonstrated in Fig. 5-2. When working under operating mode, the gate voltage of the device varies from off-state gate voltage to on-state gate voltage. In contrast, when working under measuring mode, the gate voltage remains at the gate threshold voltage. Therefore, the gate threshold voltage can be measured.

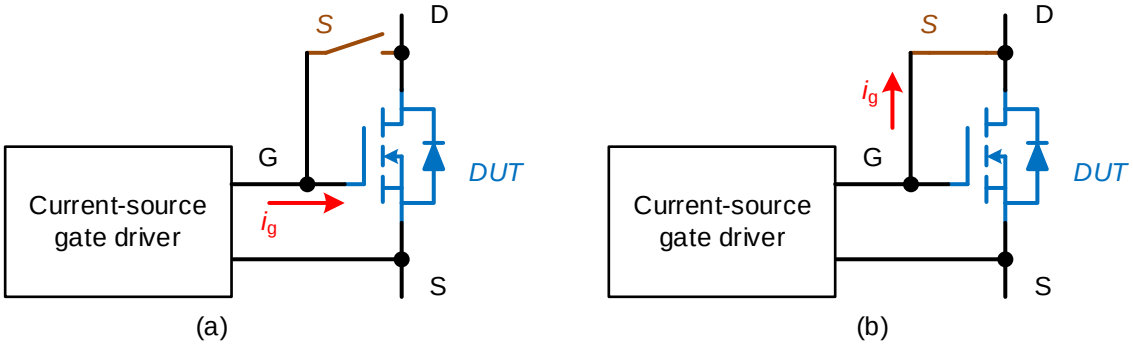


Fig. 5-1 Principle of the proposed Vth measurement method: (a) operating mode (b) measuring mode

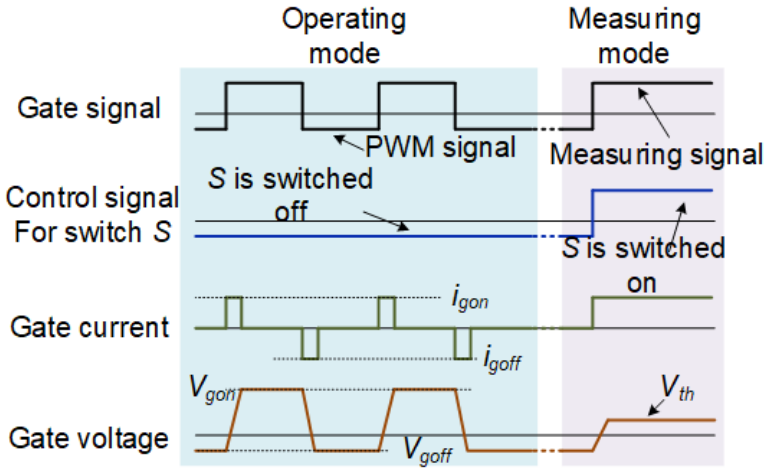


Fig. 5-2 Signal sequence of the proposed V_{th} measurement method

5.1.2. Simulation Verification

From the analysis above, the threshold voltage is obtained when the gate voltage stops increasing and the generated constant gate current flows through drain and source. However, this is different from the widely used process of threshold voltage measurement presented in datasheets. In order to compare the measuring mode of the proposed method and the conventional V_{th} measurement method defined in datasheets, simulation is conducted using a software platform, TINA, from Texas Instruments (TI). The device model used in the simulation comes from ROHM, the spice model of the 3rd generation trench-type SiC MOSFET SCT3060AL. The temperature for the simulation is 25°C. The detailed parameters in the model provide similar performance as a practical device.

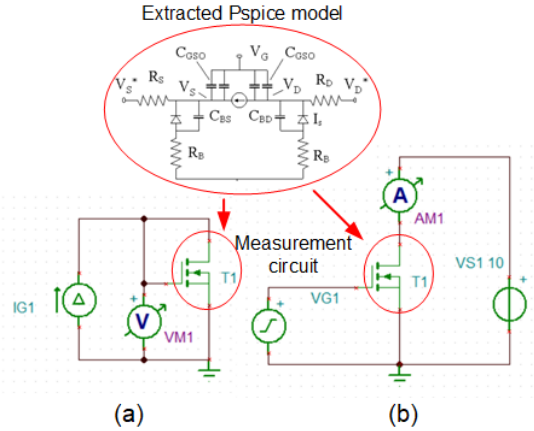


Fig. 5-3 Schematics of the simulation circuits: (a) proposed V_{th} measurement method; (b) V_{th} measurement method from the datasheet of SCT3060AL

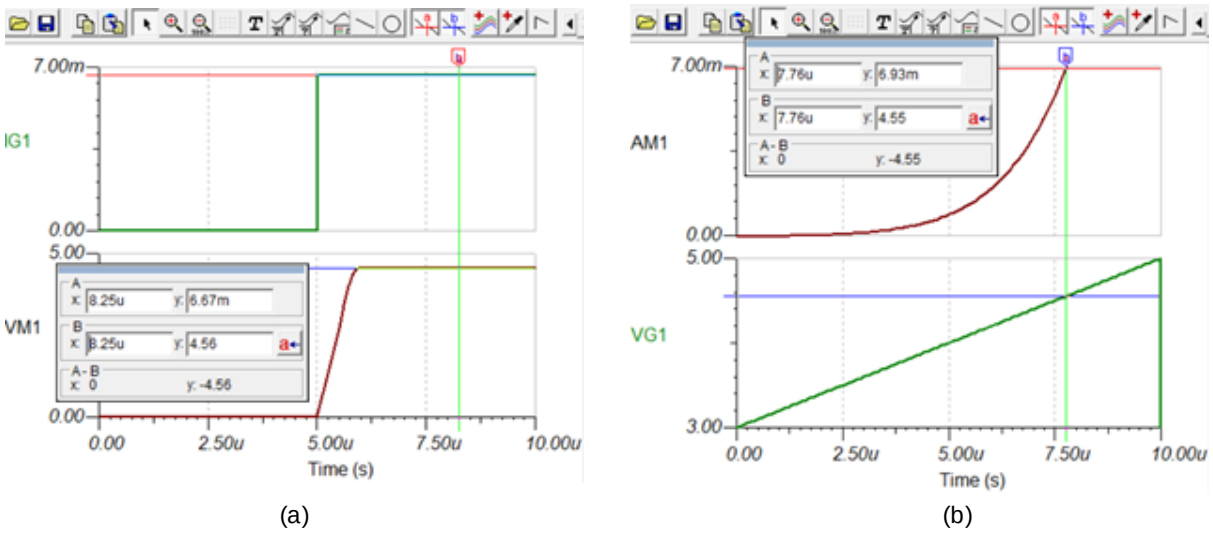


Fig. 5-4 Simulation results: (a) proposed V_{th} measurement method; (b) V_{th} measurement method from the datasheet of SCT3060AL

In the datasheet, the threshold voltage is defined as the gate voltage when drain current reaches 6.67mA under 10V drain-source voltage. In comparison, the proposed measurement method should be the gate voltage when the constant gate current is 6.67mA and the drain terminal is shorted with the gate terminal. The schematics of the simulation circuits are illustrated in Fig. 5-3, and the simulation results are presented in Fig. 5-4. In the proposed V_{th} measurement method, a step current (IG1) with a value of 6.67mA is generated and flows through drain and source while drain and gate terminals are shorted. Fig. 5-4(a) presents the simulation results of the proposed measurement method: the top waveform is the generated current IG1, whose

magnitude jumps at 6.67mA after 5us. The corresponding gate voltage signal is demonstrated in the bottom waveform (VM1), showing that the measured threshold voltage is 4.56V. In the V_{th} measurement method from datasheet shown in Fig. 5-3(b), a slope gate voltage is generated ranging from 3V to 5V after 10us, 10V bias drain-source voltage is applied and the drain current is monitored. When the drain current reaches 6.67mA, the corresponding gate voltage is obtained as the threshold voltage. As shown in Fig. 5-4(b), the top waveform reflects the drain current (AM1), while the bottom waveform (VG1) is the generated slope gate voltage. It is shown that when the drain current reaches 6.93mA, the corresponding gate voltage is 4.55V, which is almost the same as the proposed V_{th} measurement method. Therefore, it is verified that the proposed V_{th} measurement method can be used as it presents nearly the same result for V_{th} when using the conventional measurement method described in datasheet of SCT3060AL. Moreover, the advantage of the proposed V_{th} measurement method is obvious in the simulation: both the gate voltage and drain current stay constant in the proposed measurement method, whereas both the gate voltage and drain current vary in large ranges in the conventional measurement method from datasheet. Even in the simulation, it is hard to capture the accurate time at which the drain current reaches 6.67mA. In practice, the requirement for the bandwidth of sampling circuit is relatively high to improve the accuracy of the measurement. In contrast, the proposed method provides a steady state where both the drain current and gate voltage are constant, making it much easier to extract data.

5.1.3. Experiment Verification

Experiments are conducted to verify the effectiveness of the measuring mode. The diagram of the experiment circuit is illustrated in Fig. 5-5. The drain(D) and gate(G) terminals of the device under test (DUT) are shorted through a wire. A step signal is programmed and stored in the DSP controller. The signal is transferred to the digital to analog converter (DAC) via SPI communication. The signal generated by the DAC is the input to the proposed current-controlled gate driver, producing a step current as the output of the gate driver.

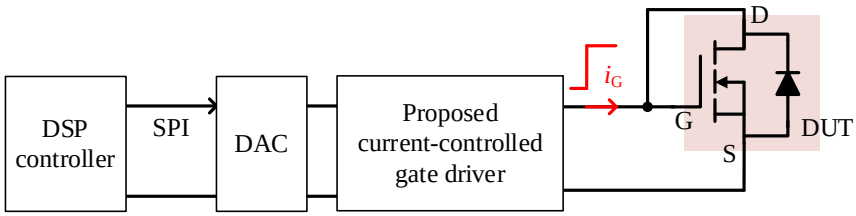


Fig. 5-5 Diagram of the experimental circuit to verify the measuring mode of the proposed V_{th} measurement method

In order to evaluate the measurement results under different drain current, the magnitude of the output step current ranges from 25mA to 200mA. An example of the experimental waveforms is shown in Fig. 5-6. The top waveform is the generated gate current I_{gs}, while the bottom waveform is the corresponding gate voltage V_{gs}. The gate current is a step signal starting at 12us with a magnitude of 25mA. As expected, the gate voltage starts increasing at 12us and stays in a steady state at 4.00V. The gate voltage in the steady state is regarded as the measured V_{th}. The temperature condition of the experiment is 25ºC. The measured V_{th} (4.00V) is different from the simulated V_{th} (4.56V) proposed in Fig. 5-4, both 4.00V and 4.56V are reasonable values as they are within the range at 25ºC (2.7V to 5.6V) proposed in the datasheet of SCT3060.

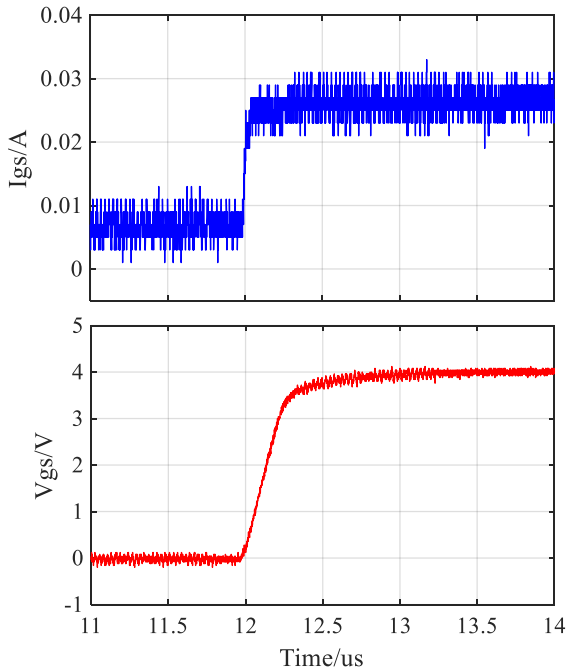


Fig. 5-6 Experimental waveforms of the proposed V_{th} measurement method

Although the value of V_{th} is an inherent parameter of a MOSFET, the measured V_{th} changed if

the test condition is different. The relation between the measured V_{th} and the input I_{gs} at 25°C. is presented in Fig. 5-7. It is verified that in the proposed measurement method, the measured result increases with a higher current. The following of the sections presents that the measured V_{th} shift is not influenced by the input I_{gs}.

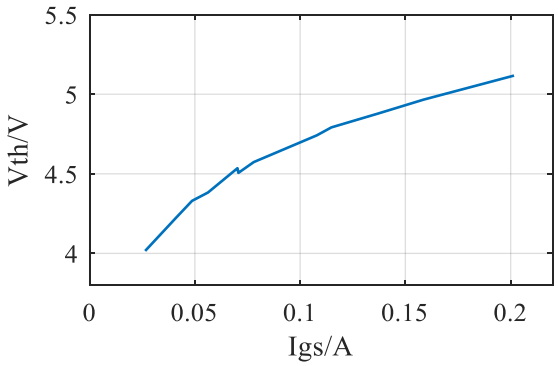


Fig. 5-7 Relation between the measured V_{th} and the input I_{gs}

V_{th} shift introduced due to the gate stress. In this experiment, 30V gate voltage is applied on the gate of the MOSFET for 2 hours to generate the gate stress. 30V is higher than the recommanded operation gate voltage, which helps to accelerate the process, otherwise the shift is very small and is difficult to be observed. After stressed under 30V gate voltage for 2 hours, the MOSFET is measured again with the same method shown in Fig. 5-7. The measured V_{th} after the gate stress is illustrated in Fig. 5-8. It is shown that the measured V_{th} shifts positively after the gate stress. No matter what current value (from 25mA to 200mA) is used for the measurement, it is shown that the measured V_{th} shift is between 0.22V and 0.25V. The increase of the measured V_{th} at different gate current is demonstrated in Fig. 5-9. It is shown that the maximum V_{th} shift is 0.25V when I_{gs} is 0.16A, while the minimum V_{th} shift is 0.22 when I_{gs} is 0.14A. The difference is less than 0.03V, which means V_{th} shift can be regarded as unchanged when different current is used in the experiment. Therefore, it is verified that the proposed V_{th} measurement method can be used for the evaluation of V_{th} shift, and the current used for measuring V_{th} can be any value under 200mA.

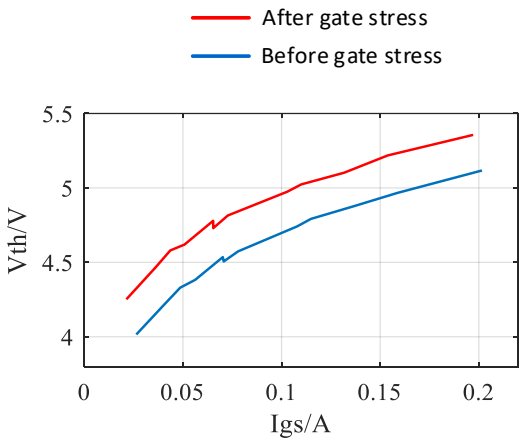


Fig. 5-8 Relation between the measured V_{th} and the input I_{gs} after the gate stress

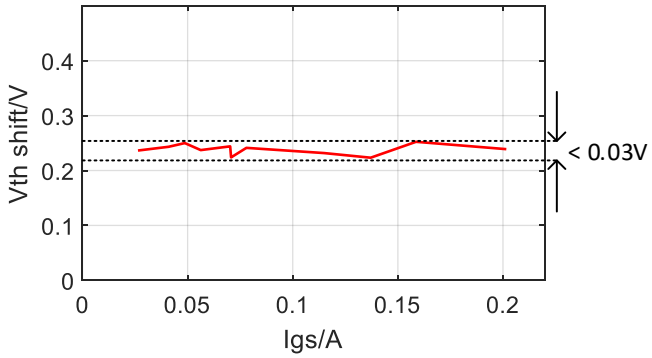


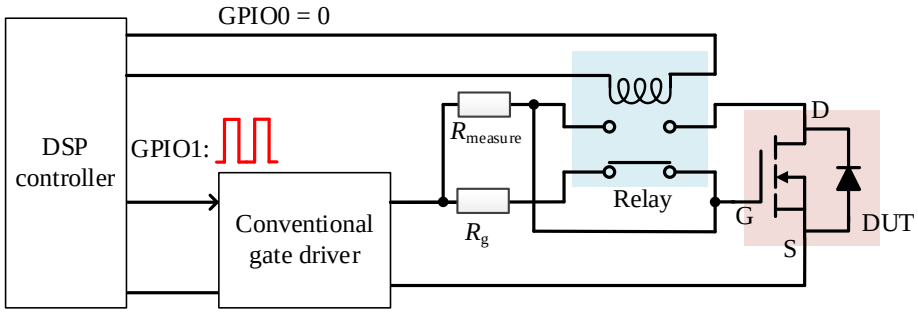
Fig. 5-9 V_{th} shift at different gate current

5.1.4. Application of the Proposed Method on the Conventional Gate Driver

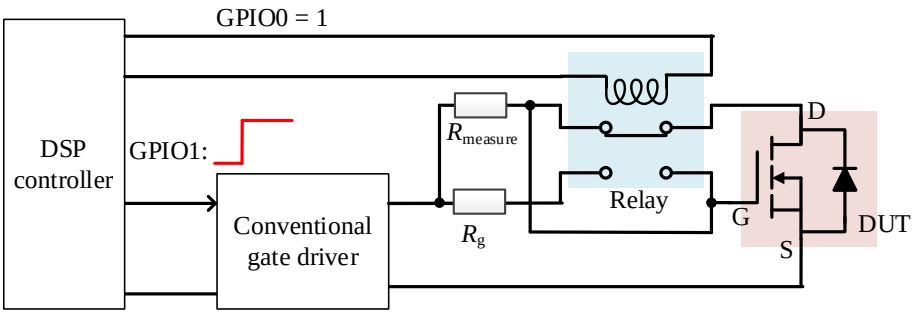
It is demonstrated in section 5.1.3 that the requirement of the proposed V_{th} measurement method is a constant current flowing though the drain and source of the MOSFET. The exact value of the small current is not important for the evaluation of V_{th} shift. Therefore, the proposed V_{th} measurement method can be easily applied to the conventional gate driver.

It is shown in Fig. 5-10 the diagram of the proposed V_{th} measurement method on the conventional gate driver. A relay controlled by the DSP controller is used to switch between the operating mode and the measuring mode. A gate resistor R_g is used to control the switching transient of the DUT, while another resistor $R_{measure}$ is applied for the measurement. It is worth noting that the value of R_g is relatively small, usually less than 20Ω. Meanwhile, the value of $R_{measure}$ is much larger, 10kΩ is used to generate the small drain current for V_{th} measurement.

When the DUT is working in operating mode, the output of GPIO0 is kept at a low voltage (GPIO0 = 0), conducting the path of R_g.



(a) Operating mode



(b) Measuring mode

Fig. 5-10 Diagram of the proposed V_{th} measurement method on the conventional gate driver

The conventional gate driver generates a voltage signal following the GPIO1 of the controller. $R_{measure}$ and R_g are paralleled to conduct the gate current. Considering that $R_{measure} >> R_g$, the influence of $R_{measure}$ can be neglected. In that condition, the DUT can be turned on and off normally following the output of the DSP controller. When the DUT is working in the measuring mode, GPIO0 is pulled up at a high voltage, triggering the relay to conduct the other path connecting the drain and the gate terminals of the DUT. R_g is cut off from the gate in the measuring mode. In that case, GPIO1 outputs a step signal. The gate is slowly charged via $R_{measure}$, introducing the increase of the gate voltage. When the gate voltage reaches the threshold voltage, the current starts to flow through the drain and sources. Therefore, the DUT stays at a steady state, where the gate voltage remains at the threshold voltage while the drain current is limited by $R_{measure}$ at a constant value. According to the analysis in section 5.1.3, the exact value of the drain current has no influence on the results of V_{th} shift. Therefore, the

proposed V_{th} measurement method can be applied to the conventional gate driver. It is worth noting that a large resistor $R_{measure}$ is used due to two reasons. Firstly, the low current can reduce the self-heating effect of the device, in case that the measurement result is influenced by the junction temperature. Moreover, the low current can reduce the influence of V_{th} shift on the generated drain current. For example, the output of the gate driver is 0V to 20V, the threshold voltage of the DUT is 5V. In the condition that $R_{measure}$ =10kΩ, the drain current flowing through the DUT in measuring mode is 1.5mA. When V_{th} shifts to 6V, the corresponding drain current is 1.4mA. There is a difference of 0.1mA in the drain current, which can be neglected. This difference will be enlarged if a lower value resistor is used. Therefore, the resistor used in the measuring mode is required to be large.

5.2. Gate Stress Times on V_{th} Shift

5.2.1. V_{th} Shift Mechanism

V_{th} shift is generally regarded as the results of gate charges trapped in the gate oxide defects. The structure of MOSFET is shown in Fig. 5-11(a) without applying gate bias. When a positive gate bias (V_{gs}) is applied across the gate and source terminals and V_{gs} is higher than V_{th}, the inversion layer is formed beneath the gate oxide as shown in Fig. 5-11(b). The zoomed-in structure of the inversion layer is demonstrated in Fig. 5-11(c). Inversion layer is formed by electrons gathering beneath the gate oxide due to the gate bias voltage. The gate charges can be determined by the gate voltage $Q_g = V_{gs} \cdot C_{OX}$, where C_{OX} is the gate capacitance. After the stress time t_s, some of the electrons are trapped by the defects inside the oxide, as shown in Fig. 5-11(d). These trapped charges can no longer move from source to drain. However, the number of charges to form the inversion layer is not changed. Therefore, more charges are needed to conduct the same current, resulting in the positive shift of V_{th}. The shift of V_{th} represents the number of charges trapped inside the oxide. The negative V_{th} shift is a similar process when the electrons inside the defects of the oxide are dragged out under negative gate bias[91], [92]. The shift of V_{th} may introduce the breakdown of the gate oxide. When more charges are trapped inside the gate oxide, the electrical field in the gate oxide increases as the distance is narrowed between the gate terminal and the electrons. Therefore, the estimation of V_{th} shift is an important

parameter to reflect the health condition of the MOSFET.

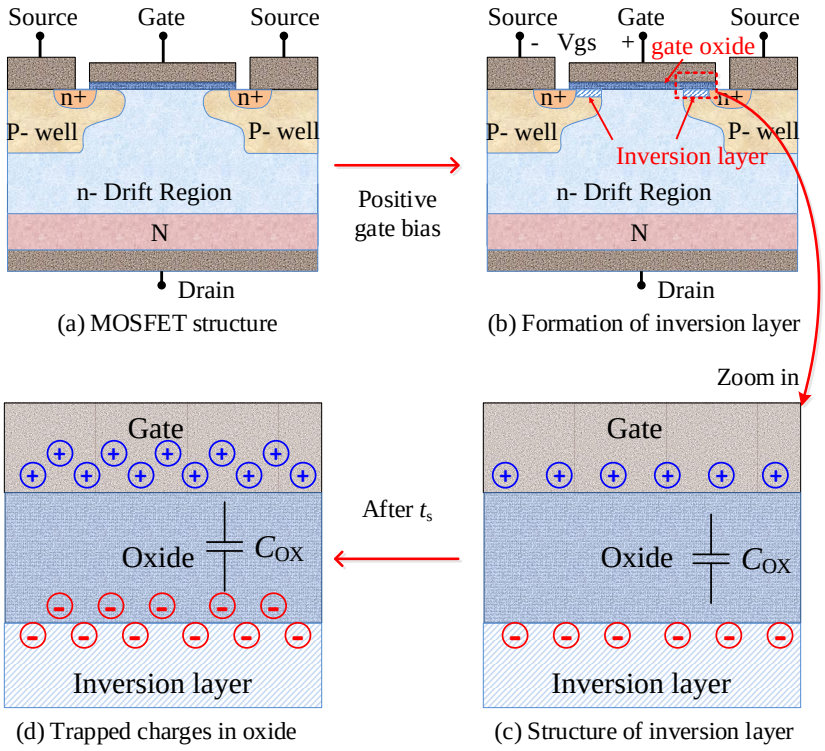


Fig. 5-11 V_{th} shift mechanism: (a) MOSFET structure; (b) Formation of inversion layer; (c) Structure of inversion layer; (d) Trapped charges in oxide

5.2.2. *Experimental Results*

The shift of V_{th} is considered to have the potential to indicate the health condition of the MOSFET. The relation between the V_{th} shift and the gate stress time is investigated using the proposed V_{th} measurement method. The diagram of the experimental circuit is shown in Fig. 5-10. It is worth noting that the constant gate voltage is applied instead of a PWM signal to accelerate the process. The output of the gate driver is maintained at 20V throughout the tests, which is the suggested gate voltage from the datasheet. The value of the resistor is 20kΩ. The diagram of the experimental signal sequence is presented in Fig. 5-33. The 20V gate voltage is applied when GPIO0 = 0 for a certain period, while V_{th} is measured when GPIO0 = 1. Considering that V_{th} shifts faster at the beginning of the gate stress and gets slower thereafter, the gate stress period increases from 5 seconds per sample point to 1 hour per sample point. The total gate stress time is 5 hours 13 minutes (19580 seconds), while V_{th} is measured at the following time: 0.1s, 5s, 10s, 15s, 20s, 30s, 40s, 50s, 60s, 70s, 80s, 140s, 200s, 260s, 320s, 380s,

680s, 980s, 1280s, 1580s, 3380s, 5180s, 6980s, 8780s, 12380s, 15980s and 19580s. The measuring period is 2.2us, which is negligible compared with the gate stress period. An example of the gate voltage waveform in the measuring mode is illustrated in Fig. 5-13.

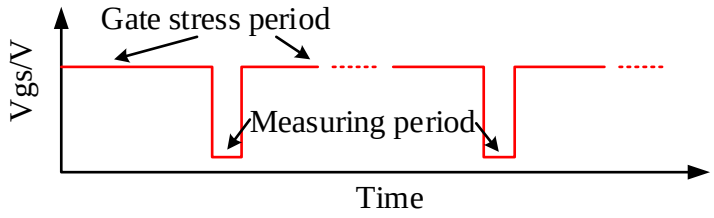


Fig. 5-12 Diagram of the experimental signal sequence

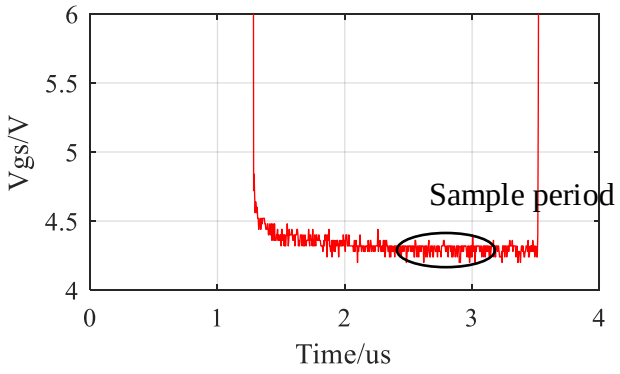


Fig. 5-13 An example of the gate voltage waveform in the measuring mode

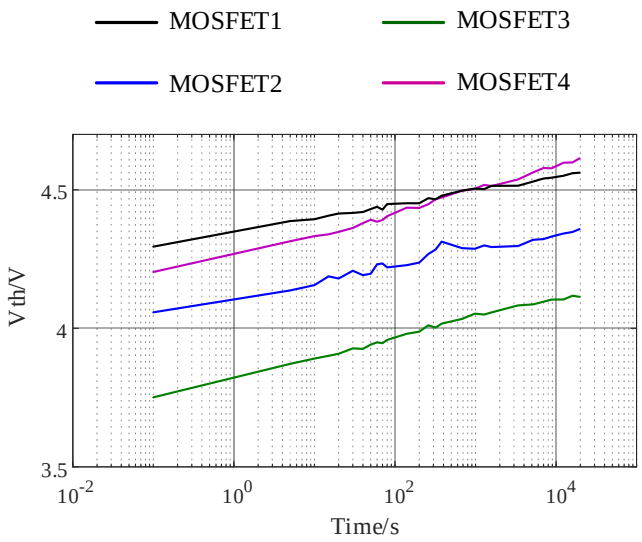


Fig. 5-14 Experimental results of V_{th} shift vs gate stress time under the gate stress of 20V constant gate voltage

As shown in Fig. 5-14, the experimental results of 4 MOSFETs under 20V DC gate stress are illustrated. A linear relationship is demonstrated between V_{th} shift and the logarithm of the gate

stress time for all the devices under tests. The quantitative relationship is generated using the curve fitting tool, as shown below:

$$V_{th1} = 0.056 \cdot \lg t + 4.326 \tag{5.1}$$

$$V_{th2} = 0.046 \cdot \lg t + 4.106 \tag{5.2}$$

$$V_{th3} = 0.074 \cdot \lg t + 3.824 \tag{5.3}$$

$$V_{th4} = 0.080 \cdot \lg t + 4.310 \tag{5.4}$$

where V_{th1} to V_{th4} are the threshold voltages of the 4 devices under tests respectively and t is the gate stress time. It is shown that different MOSFETs present different slope rates ranging from 0.046V/s to 0.080V/s, and different starting points ranging from 3.824V to 4.326V. However, all the devices demonstrate a linear increase of V_{th} with the logarithm of gate stress time. Therefore, it is verified that V_{th} shift can be used to estimate the stressed time of a MOSFET.

In addition to the constant 20V gate stress, switching gate stress between 20V and 0V is also tested. The signal sequence for the switching gate stress test is presented in Fig. 5-15. The switching frequency of the gate voltage is 50kHz in the gate stress period, while the duty cycle is 50%. The measuring period is the same as the constant gate stress test: the measuring period is 2.2us, which is negligible compared with the gate stress period.

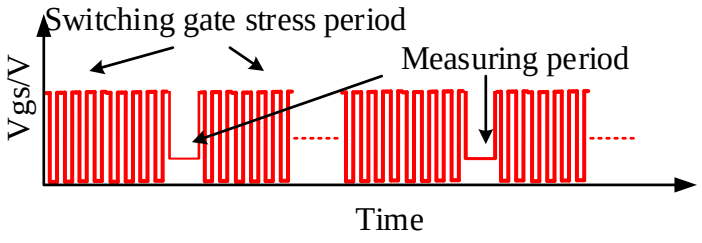


Fig. 5-15 Diagram of the experimental sequence for switching gate stress test

The experimental results of the switching gate stress on 4 MOSFETs are presented in Fig. 5-16. It is shown that the 4 curves have a similar behaviour compared to the previous experiment. However, the absolute value of V_{th} shift under switching gate stress is lower than the results

under constant switching gate stress. In addition, the slope rate is also lower. Curve fitting tool is applied to the results under switching gate stress for quantitative analysis. The fitted V_{th} shift models of the 4 devices are presented below:

$$V_{th1} = 0.018 \cdot \lg t + 4.162 \tag{5.5}$$

$$V_{th2} = 0.036 \cdot \lg t + 3.744 \tag{5.6}$$

$$V_{th3} = 0.032 \cdot \lg t + 3.558 \tag{5.7}$$

$$V_{th4} = 0.044 \cdot \lg t + 4.066 \tag{5.8}$$

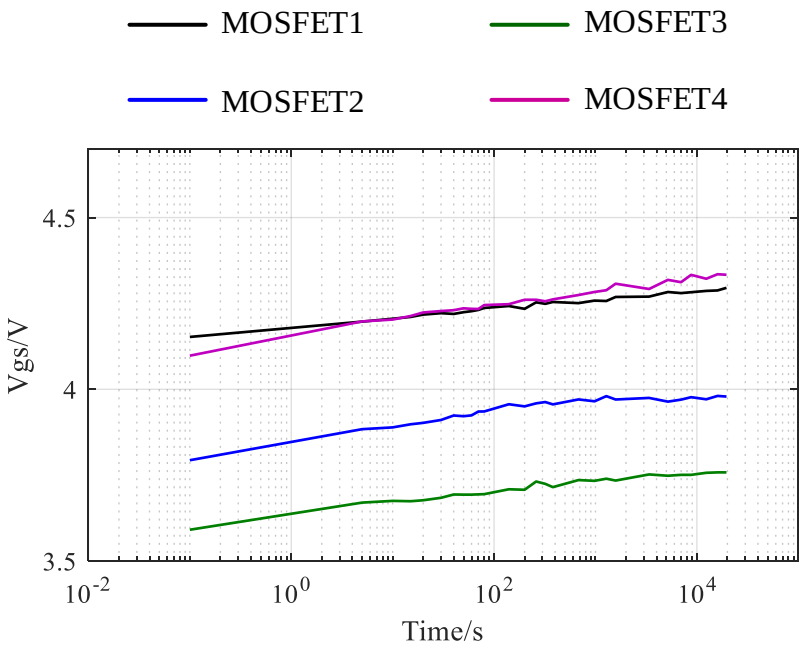


Fig. 5-16 Experimental results of V_{th} shift vs gate stress time under the gate stress of switching gate voltage

It is shown from the equations that the slope rates of all the devices are lower than the corresponding slope rates under constant gate stress. It can be concluded that the V_{th} shift follows a linear relationship with the logarithm of the gate stress time. Furthermore, the value of the slope rate in Fig. 5-16 is around half the value of the slope rate in Fig. 5-14, which means V_{th} shifts faster under constant gate voltage than under switching gate voltage.

5.3. V_{th} Shift in Short Gate Stress Time

5.3.1. *Phenomenon of V_{th} Shift in Short Gate Stress Time*

The experiments presented in section **Error! Reference source not found.** are the V_{th} shifts a fter a period of gate stress, which range from 0.1s to more than 5 hours. For shorter time scale, the method mentioned above cannot be applied, because it requires an actuation time to switch the current path. However, a phenomenon of V_{th} shift can be observed in short gate stress time with the proposed current-controlled gate driver. I look into this phenomenon because it has never been discussed in publications, moreover, this phenomenon can be used for temperature estimation, which is discussed in 5.4.

The proposed current-controlled gate driver is used to generate a constant gate current for the experiment. It is illustrated in section 5.1 that the programmed constant current charges the gate capacitance before V_{gs} reaches V_{th} in the measuring mode. Therefore, it is expected that the waveform of V_{gs} consists of 2 parts in the measuring mode: 1) the gate voltage increases at a constant speed charging the gate capacitance; 2) the gate voltage remains constant at V_{th}. The conceptual V_{gs} waveform in measuring mode is illustrated in Fig. 5-17.

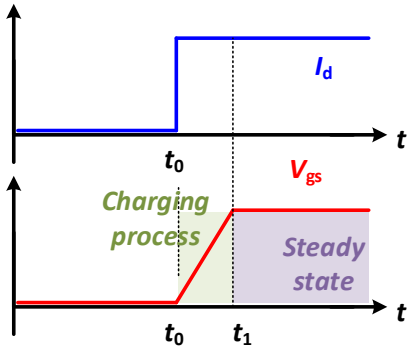


Fig. 5-17 Conceptual V_{gs} waveforms in measuring mode

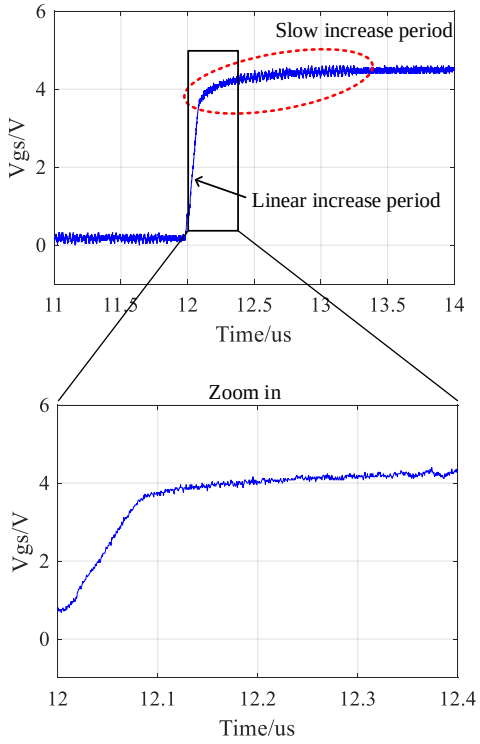


Fig. 5-18 Experimental waveform of V_{gs} in the condition of 25mA drain current and 50°C

The simulation shown in Fig. 5-4(a) verifies the analysis that the constant current stays constant after charging the gate capacitance. However, the experiment waveforms demonstrate differences from the expectation.

Fig. 5-18 illustrates the experimental waveform of V_{gs}, showing an additional slow increase period in addition to the fast linear increase period. This slow increase period is not expected from traditional analysis and the simulation model. Fig. 5-18 shows that the fast linear increase period ends at 12.1us. After this time V_{gs} keeps increasing. It is worth noting that this phenomenon is in the time scale of microseconds. The shift of V_{th} in such a short time scale is not investigated in existing publications[58] [99] [95].

Another phenomenon can also verify that V_{th} shift happens at much faster timescales . Fig. 5-18 shows the turn-on V_{gs} waveform for a conventional gate driver. It is demonstrated that the Miller plateau is not flat but increases slightly. Comparing the practical results with the simulation waveform shown in Fig. 5-20, it is obvious that the Miller plateau in the simulation is flat while the experimental waveform presents an increasing Miller plateau. The increasing Miller plateau is proposed to be introduced by V_{th} shift in short gate stress time, which means

means that the V_{th} shift occurs in every switching transient, but its effect is not considered in traditional analysis and simulations models. The influence of this phenomenon is not clear yet, but this phenomenon can be used as a new TSEP as discussed in 5.4.

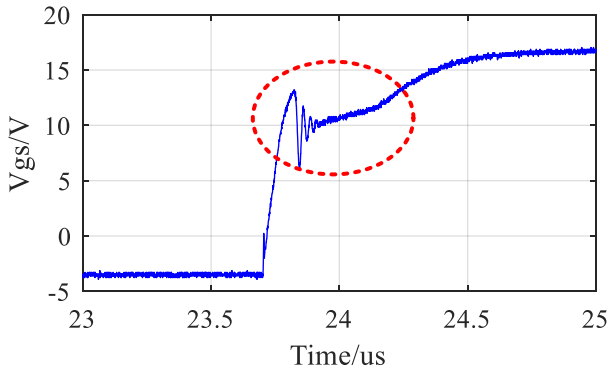


Fig. 5-19 Experiment waveform of V_{gs} during turn-on transient

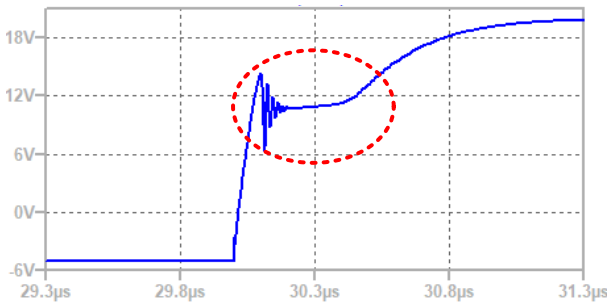
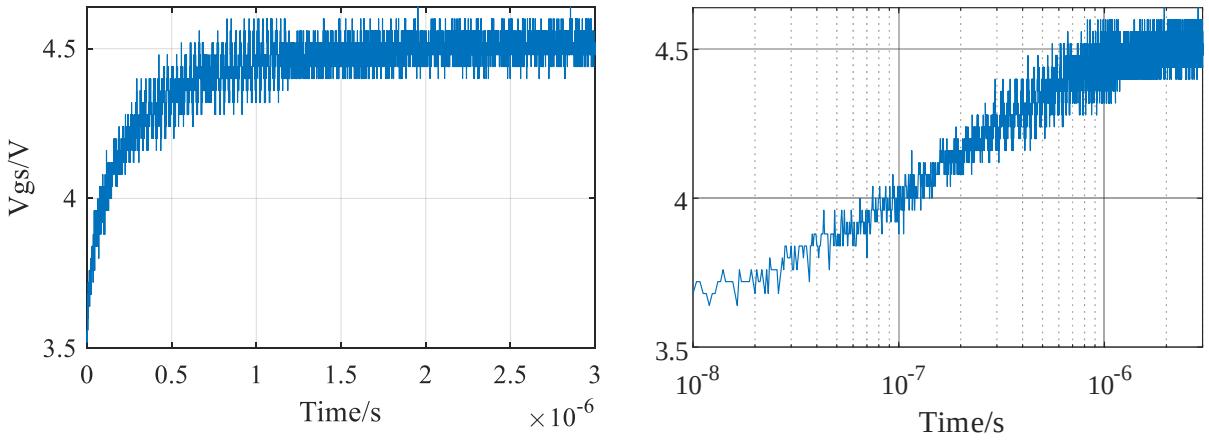


Fig. 5-20 Simulation waveform of V_{gs} during turn-on transient

5.3.2. Modelling of Short Time Vth Shift

The slow increase period in Fig. 5-18 is modelled using curve fitting tool in this subsection. The waveform of V_{gs} in this period is selected and demonstrated in linear time axis and logarithm time axis respectively (Fig. 5-21). A linear relationship can be observed in Fig. 5-21(b) between V_{gs} and the logarithm time axis before 1us.

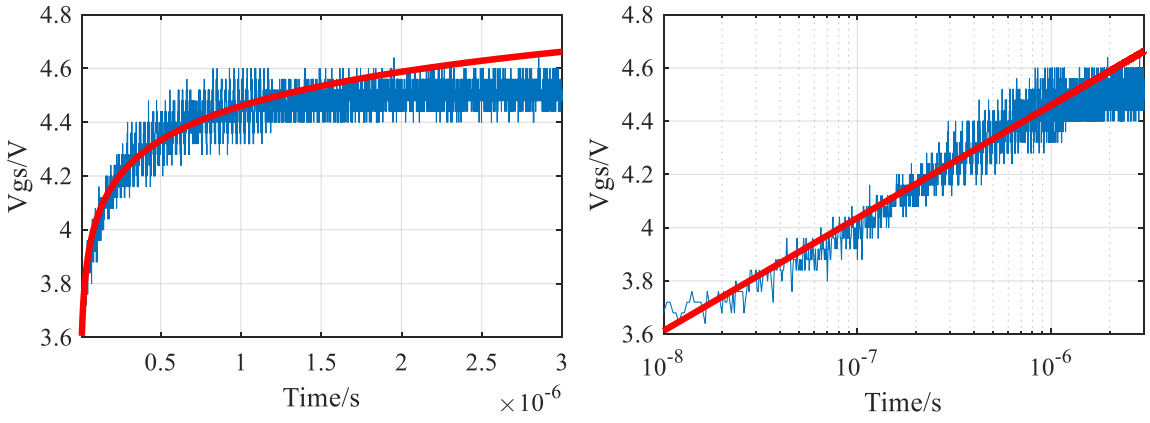


(a) Linear time axis (b) Logarithm time axis

Fig. 5-21 Experiment waveform of V_{gs} in the slow increase period: (a) linear time axis; (b) logarithm time axis

The quantitative relationship can be analyzed using the curve fitting tool. The curve fitting result is illustrated in Fig. 5-22 as the red waveform shows. The mathematical equation is presented as below:

$$V_{th} = 0.184 \cdot \ln t + 7.002 \tag{5.9}$$



(a) Linear time axis (b) Logarithm time axis

Fig. 5-22 Curve fitting result of V_{gs} in the slow increase period: (a) linear time axis; (b) logarithm time axis

Fig. 5-22 demonstrates the curve fitting results of the proposed logarithm model. The blue waveform is the measured V_{gs}, while the red curve is the calculated mathematic relation between V_{th} and the gate stress time. It is shown that in the first 1us V_{th} shifts , the logarithm model can be used to describe the short time shift of V_{th} under the gate stress.

Comparing the short-time V_{th} shift model in (5-9) with the long-time V_{th} shift model in (5-1), it is found that the slope rate of the short-time V_{th} shift is much higher than the long-time V_{th} shift model (0.184 >> 0.056). In addition, the shift of V_{th} in the first 1us is more than 0.6V, while the shift is less than 0.3V in the next 5 hours. It is worth noting that the measured short-time V_{th} shift is under the gate stress of 4.5V, which is much lower than the gate stress applied in the long-time V_{th} shift test.

5.3.3. Modification of MOSFET Pspice Model Considering Short Time Vth Shift

It is stated in section 5.3 that the provided Pspice model of the device under test has not included the effect of V_{th} shift, which introducing the difference in the simulation results, as shown in Fig. 5-19 and Fig. 5-20. In this subsection, the Pspice model of the MOSFET is modified to take the V_{th} shift effect into consideration, showing closer simulation waveforms to the experimental result.

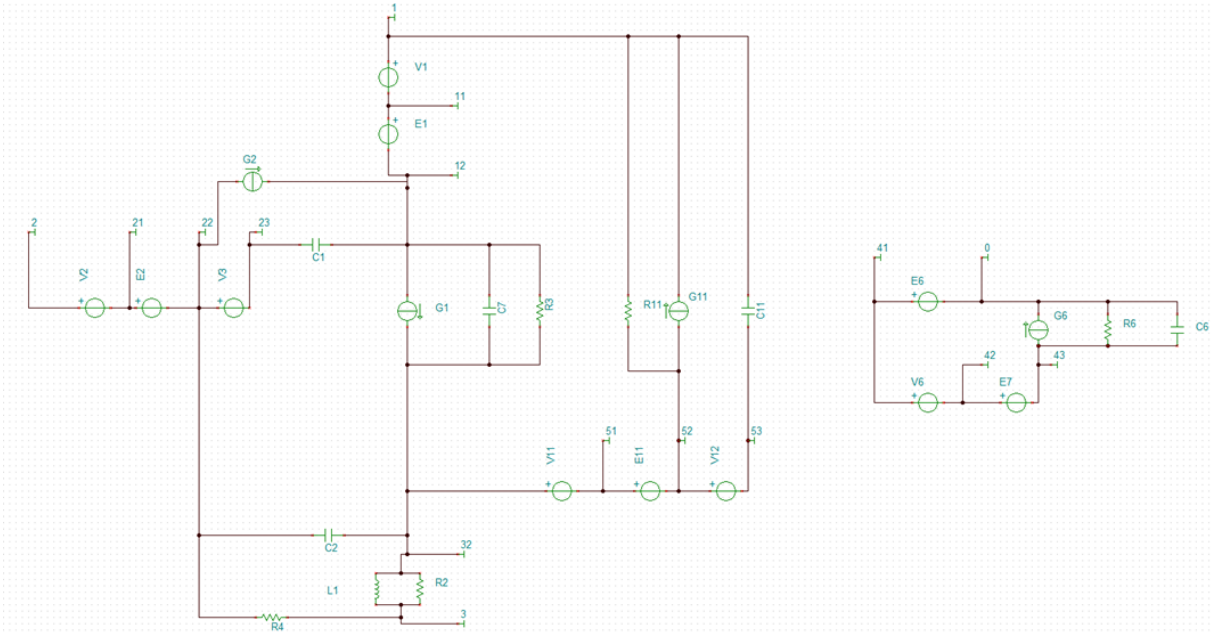


Fig. 5-23 Equivalent circuit of the MOSFET Pspice model

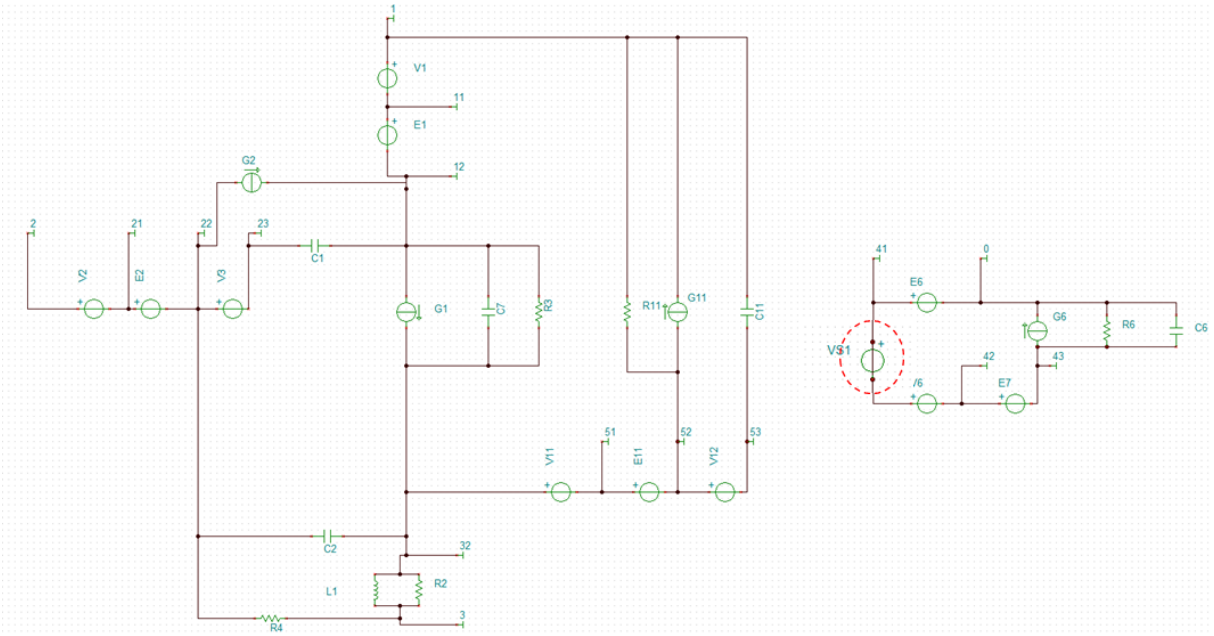


Fig. 5-24 Modified equivalent circuit of the MOSFET Pspice model considering short time V_{th} shift

The equivalent circuit of the MOSFET can be built based on the code of Pspice model. Fig. 5-23 demonstrates the original Pspice model. The left part of the circuit is to simulate the output characteristics of the MOSFET, while the right circuit is to simulate the control of the gate signal. In order to include the short time V_{th} shift effect into the model, an additional controlled voltage source is used to add a logarithm voltage to the existing circuit as shown VS1 in Fig. 5-24. The logarithm increase on gate voltage is therefore presented in the turn on transient. Simulation is conducted under the same condition as in Fig. 5-20. The comparison of the simulation results is presented in Fig. 5-25. It is shown that the modified Pspice model presents the slow increasing Miller plateau as the experimental results. The detailed Pspice code for the original model and the modified model can be found in Appendix II and Appendix III.

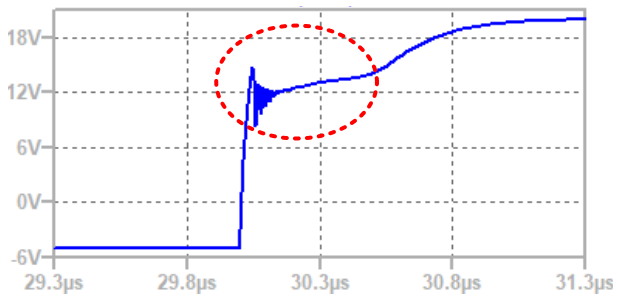


Fig. 5-25 Comparison of the simulation results after the modification of the Pspice model

5.3.4. *Double-layer Trap Model*

A double-layer trap model is proposed in this section to explain the short-time V_{th} shift and long-time V_{th} shift phenomenon shown in Fig. 5-26. The defects inside the gate oxide consists of 2 parts: the interface defects and the deep inside defects. The interface defects distribute near the interface of the inversion layer and the gate oxide; the deep inside defects is further away from the inversion layer. The short-time V_{th} shift occurs within the interface defects, while the long-time V_{th} shift is caused by the deep defects. The higher density of the interface defects and the shorter distance from inversion layer make it easier for the charges in the inversion layer to be trapped by the interface defects. Therefore, the short-time V_{th} shift demonstrates higher speed and larger shifts. In contrast, the density of the deep defects is relatively lower, and the distance of these defects is further away from the charges in the inversion layer. These facts result in the lower slope rate of the long-time V_{th} shift.

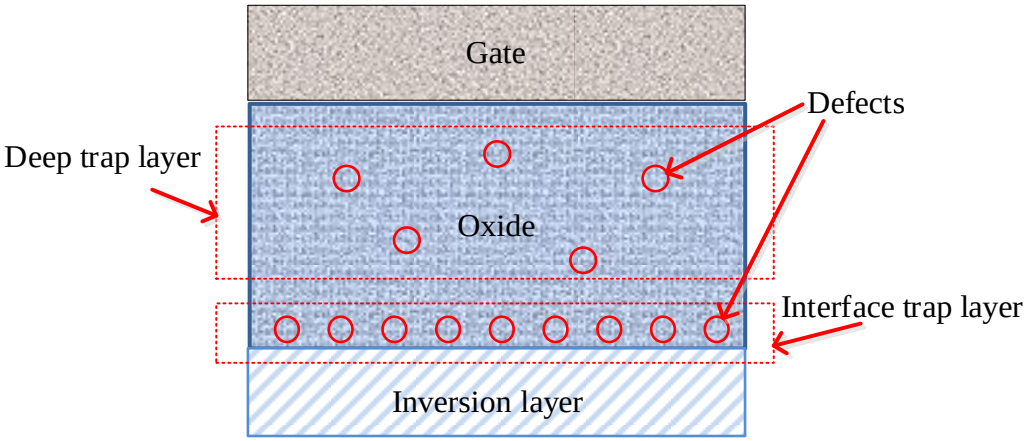


Fig. 5-26 Double-layer trap model for V_{th} shift

Considering that the speed of the interface trap effect is much higher than deep trap, the V_{th} shift process is regarded to be made up of 2 parts: the first process is the interface trap, which happens within the first microsecond. The interface defects are fully occupied before the deep defects start to trap charges from the inversion layer. Both the interface trap and the deep trap follow a linear relationship with the logarithm of the gate stress time. However, the slope rate for the interface trap is much higher than the deep trap, making it easier for the interface defects to trap and release the charges from inversion layer. The interface defects trap the charges in every turn-on period, while they release them in every turn-off period.

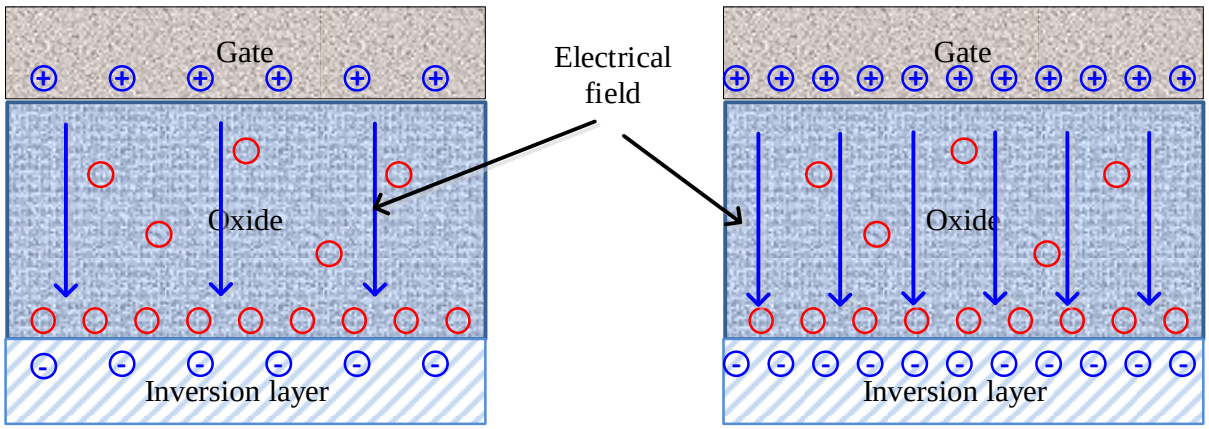
From the double-layer model, the followings are expected: 1. Only the deep trap effect can be used to evaluate the health condition of the gate oxide. The V_{th} shift discussed in all the publications refers to the long-time V_{th} shift. 2. The measurement of V_{th} shift should be conducted after the interface trap period, otherwise the measured V_{th} would be lower if the interface defects are not fully occupied. 3. The interface trap effect is only influenced by the electrical field across the interface, and not influenced by the deep trap effect.

5.3.5. *Impact Factor of the Short-time V_{th} Shift*

Experiments are conducted in this subsection to investigate the impact factor of the short-time V_{th} shift. The logarithm model in section 5.3.2 is used to evaluate the influence of the generated gate current, the temperature and the gate stress.

A. Short-time Vth Shift vs Gate Current

Fig. 5-27 illustrates the influence of the gate current on the electrical filed in the gate oxide. The higher generated gate current results in more electrons gathered in the inversion layer. These extra charges increase both the measured V_{th} and the electrical field. Considering that higher electrical field accelerates the interface trap effect, the slope rate of the short-time V_{th} shift model is expected to increase along with the generated gate current.



(a) low gate current (b) low gate current

Fig. 5-27 Influence of gate current on the electrical field in the gate oxide

The diagram of this experiment is the same as shown in Fig. 5-5. The magnitude of the generated step signal of gate current is increasing from 25mA to 70mA. The process of the

short-time V_{th} shift is evaluated by the slope rate of the V_{th} shift and the logarithm of the gate stress time, as shown in Fig. 5-22(b). The temperature is kept at 25°C in all the measurement. The relation of the slope and the magnitude of the gate current is illustrated in Fig. 5-28. The positive correlation verifies the analysis based on the proposed model. It is worth noting that the measured V_{th} after the short time shift period rises from 4.15V to 4.64V along with the increase of the generated gate current.

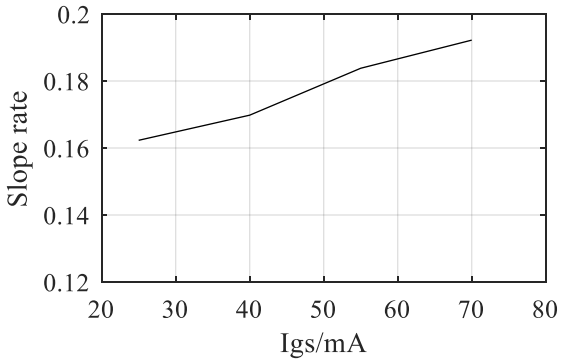
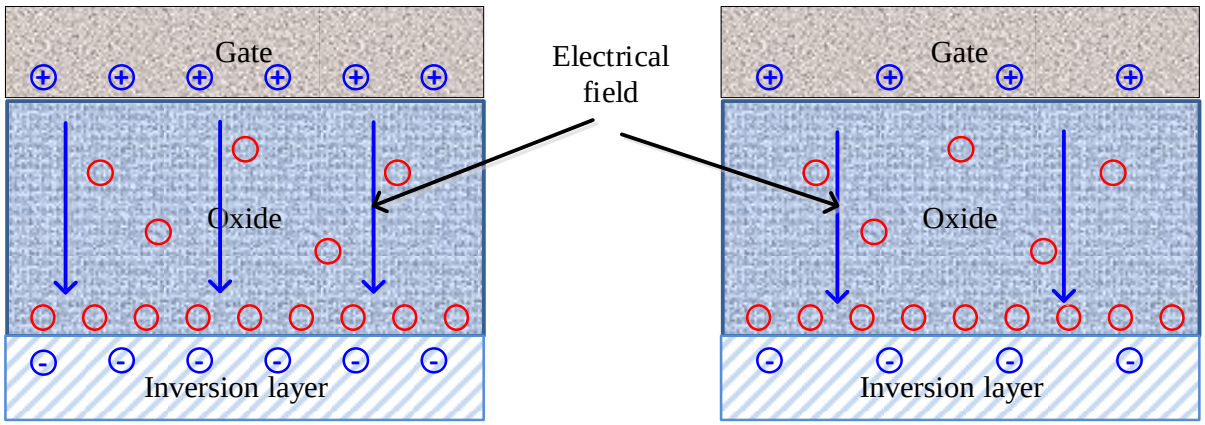


Fig. 5-28 Relation between the slope of the short-time V_{th} shift and the gate current

B. *Short-time Vth Shift vs Temperature*

Fig. 5-29 presents the influence of the temperature on the electrical field in the gate oxide. In the condition of higher temperature, the electrons required for inversion layer are less than lower temperature[111]. The decrease of the charges in the inversion layer reduces the electrical filed. Therefore, it is expected that the slope rate of the short-time V_{th} shift is reduced in higher temperature.



(a) low temperature (b) high temperature

Fig. 5-29 Influence of temperature on the electrical field in the gate oxide

Experiments are conducted under different temperature to verify the above analysis. The gate current used in the measurement is 70mA. The gate voltage waveforms in different temperature of the device under test are captured and evaluated using the logarithm model. It is presented in Fig. 5-30 the relation between the slope of the short-time V_{th} shift and the temperature. The negative correlation verified the analysis based on the proposed model. It is worth noting that the measured V_{th} after short time shift period is reduced from 4.64V to 4.11V along with the increase of temperature.

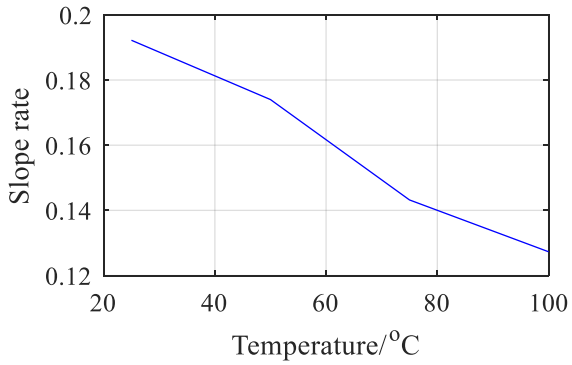
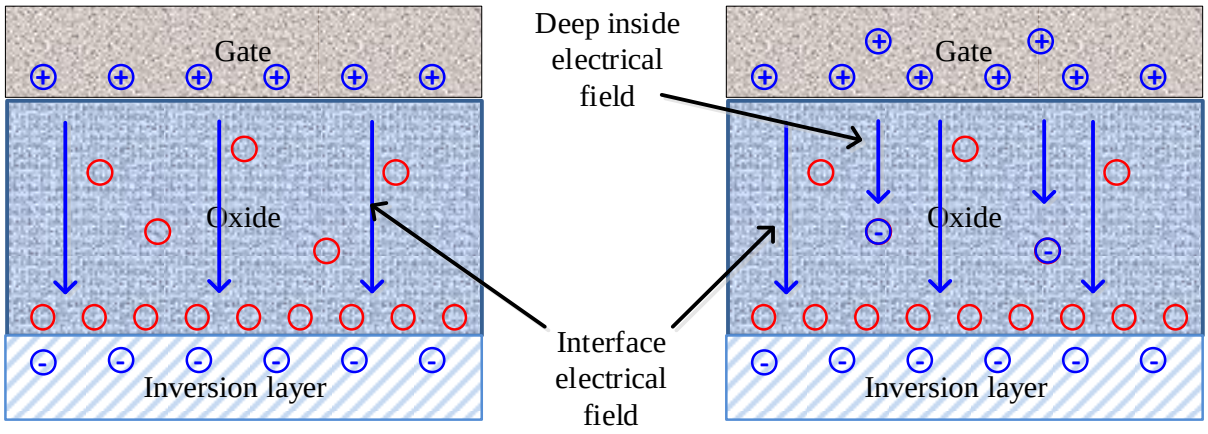


Fig. 5-30 Relation between the slope of the short-time Vth shift and the temperature

C. Short-time Vth Shift vs Gate Stress

Fig. 5-31 presents the influence of gate stress on the electrical field in the gate oxide. The gate stress results in extra charges deep inside the gate oxide, introducing the shift of V_{th} and additional electrical field deep inside the gate oxide. However, this additional electrical field has no influence on the interface trap effect. Therefore, it is expected that the short-time V_{th} shift process is the same after the gate stress.



(a) Before gate stress (b) After gate stress

Fig. 5-31 Influence of gate stress on the electrical field in the gate oxide

Experiments are conducted on the device under tests with three different gate stress condition. Firstly, the gate waveform is captured before the gate stress is applied. Secondly, the device is stressed under 30V for 2 hours before the test is conducted. Finally, an additional 5 hours gate stress is applied. The temperature is maintained at 50°C for all tests, and the gate current is also kept at 70mA. The corresponding slope of the short-time V_{th} shift is calculated and illustrated in Fig. 5-32. The variation of the slope is within 0.01 when the V_{th} increases from 4.45V to 4.70V. It is verified that the gate stress has significant influence on the long-time V_{th} shift, while it has negligible impact on the short-time V_{th} shift.

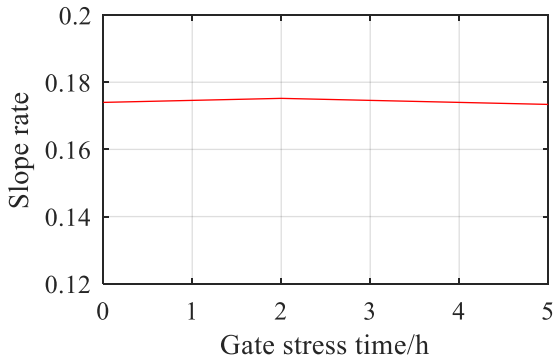


Fig. 5-32 Relation between the slope of the short-time Vth shift and the gate stress time

5.4. Methods to Decouple the Influence of Temperature on V_{th} shift

The section above shows that V_{th} can indicate failures in the gate oxide and can measure the chip temperature. However, both impacts are coupled with each other and is therefore an inevitable hindrance for the evaluation of V_{th} shift or measuring the chip temperature. This

section demonstrates two methods to decouple the influence of temperature on V_{th} shift. It is worth noting that all of the common TSEPs are influenced by V_{th}, including the on-state resistance (R_{on}), the Miller plateau voltage (V_{Miller}), the turn-on delay time (t_{don}), etc. Therefore, the influence of gate stress on V_{th} would results in measurement error in all TSEPs. Considering that a correct TSEP measurement is important for the health monitoring of the MOSFET, the methods to decouple the influence of temperature and the influence of gate stress on V_{th} is highly demanded.

5.4.1. Short-time Vth Shift Slope

According to the experimental results shown in section 5.3.5, the slope of the short-time V_{th} shift has a linear relationship with temperature, presenting the potential to be used as an indicator for temperature. Moreover, the slope is not influenced by the gate stress, making it a perfect candidate for decoupling the influence of temperature and gate stress.

5.4.2. Channel Mobility

According to the working principle of MOSFETs, the relationship between the gate voltage and the drain current in saturation region can be described as below:

$$I_d = K(V_{gs} - V_{th})^2 \tag{5.10}$$

where $K = \frac{\mu_n C_{OX} W}{2L}$, μ_n is the mobility of electrons in the channel, C_{ox} is the capacitance of the gate oxide, W is the channel width, L is the channel length, and V_{th} is the threshold voltage.

Using the proposed V_{th} measurement method in section 5.1, the corresponding V_{gs} under different I_d can be measured. The curve fitting tool can be used to estimate the parameters K and V_{th}. Considering that C_{ox},W and L can all be regarded as constants, parameter K is only influenced by μ_n. Meanwhile, μ_n is only influenced by temperature, independent from the gate stress. Therefore, K can be used as a new TSEP to estimate the temperature.

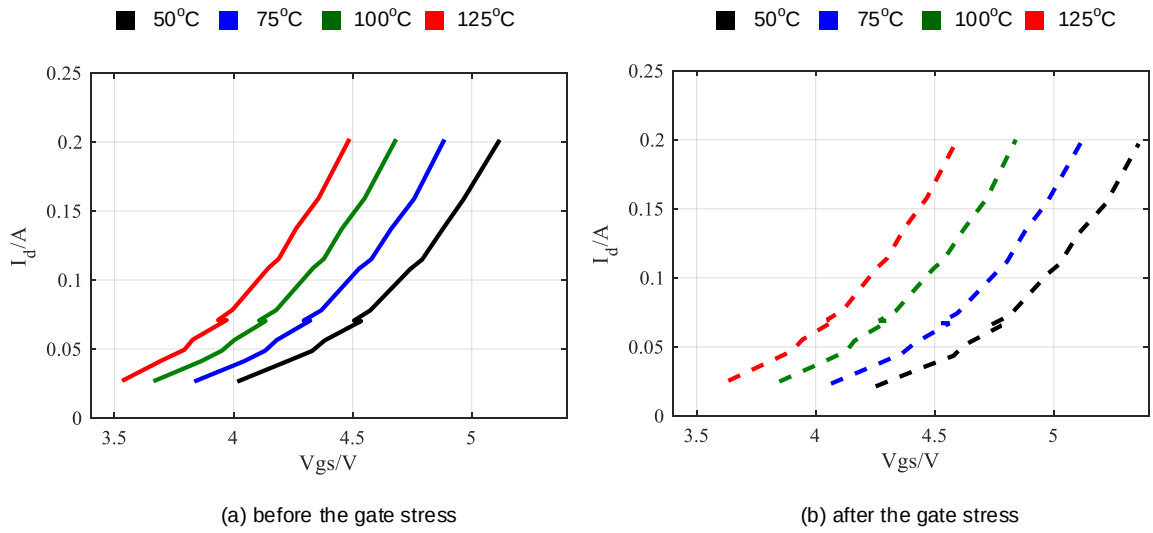
The following steps are conducted to verify the proposed analysis:

1. V_{th} measurement experiments are conducted using the method demonstrated in 5.1,

different constant currents are used ranging from 20mA to 200mA.

2. The relationship between the measured V_{gs} and I_d is plotted.
3. The curve fitting tool is used to describe the mathematic relationship between V_{gs} and I_D with 2nd order polynomial equation.
4. The results of the calculated K and V_{th} are recorded.
5. The steps are repeated under different temperature: 50°C, 75°C, 100°C, 125°C.
6. The steps are repeated after the MOSFET is stressed with 30V gate voltage for 2 hours.

The experiment result of V_{gs} vs I_d is demonstrated in Fig. 5-33, showing that the relation between V_{gs} and I_d follows the 2nd order polynomial equation. Moreover, it is illustrated that the transconductance curve shifts left under increasing temperature, while it shifts right after the gate is biased at 30V for 2 hours. In addition, the parameters K and V_{th} in (5-10) are calculated using the curve fitting tool, whose temperature dependency are plotted as shown in Fig. 5-34. It is illustrated that the gate stress has a negligible effect on the parameter K as the two curves overlap with each other in Fig. 5-34(a). In contrast, a gap of 1.2V~2.1V is presented after the gate is biased under 30V for 2 hours. Therefore, it is verified that K can be used to decouple the influence of temperature and gate stress.



(a) before the gate stress (b) after the gate stress

Fig. 5-33 Measured V_{gs} under different I_d in the test condition: (a)before the gate stress; (b) after the gate stress

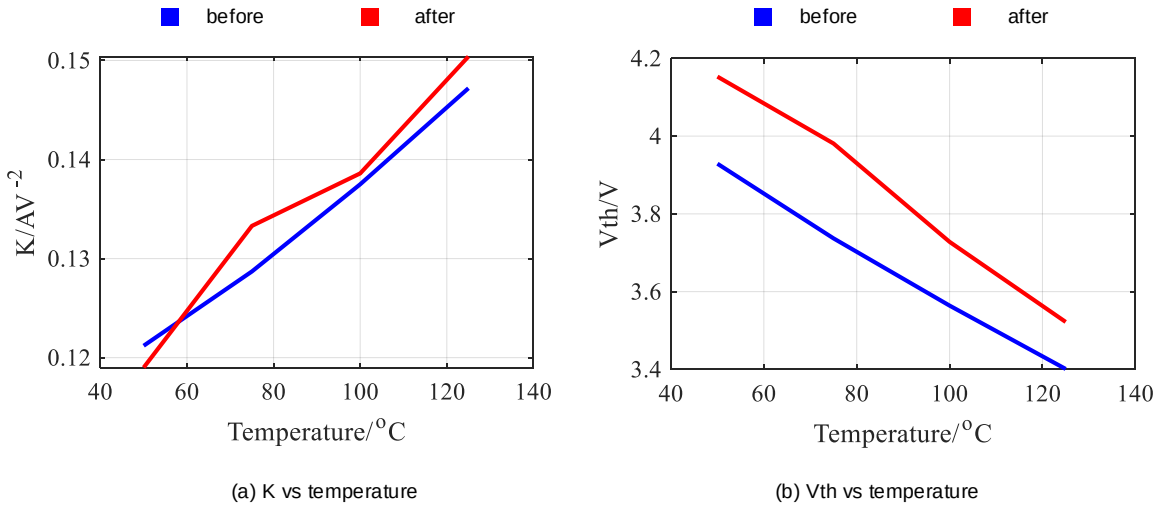


Fig. 5-34 Temperature dependency of the parameters before(blue)/after(red) gate stress: (a) K; (b) Vth

5.5. Applications of the Proposed Method

The basic requirement for the proposed V_{th} measurement method is connecting the drain and the gate terminal of the device under test. Moreover, the drain current is controlled and generated by the gate driver. This means no voltage is applied across the drain and the source, and no current from the power circuit flows through the device. However, this is not the normal operating form of the MOSFET. This section aims to discuss the feasibility of the proposed V_{th} measurement method in different applications.

1. Single-switch Topologies

Typical single-switch topologies include the buck topology and boost topology. During the normal operating period of the circuit, the device either conducts high current or block high voltage. The proposed method cannot be applied to these topologies if the power supply is connected into the circuit. Therefore, the requirement to apply the proposed V_{th} method is to disconnect the power supply and the load to keep off the influence of peripheral circuit.

2. Full-bridge Topologies

Full-bridge topologies are widely used in inverters and motor drives. When all four switches are turned off, no power can flow through the devices. In that condition, the proposed method can be applied. For example, if the device under measurement is S1, S2 will block the high voltage from the input. Also, no current can flow through S1 when all devices are turned off. In

this way, the condition is achieved to short S1 safely. Therefore, the requirement of utilizing the proposed V_{th} measurement method is to switch off all devices during the measurement.

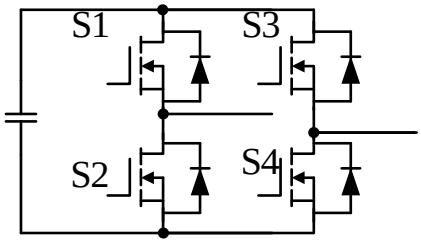


Fig. 5-35 Typical full-bridge topology

3. Natural Point Clamped (NPC) Topology

The typical NPC topology is shown in Fig. 5-36, which is widely used in the multi-level converters to generate high voltage. The proposed method can be applied to S1 and S4 without interrupting the normal operation of the converter. Taking S1 as an example to conduct the measurement, it is safe to turn on S1 when the phase current flows through S3 and S4. In that case, S2 is turned off, blocking the high voltage from the DC bus bar. The measurement introduces no influence on the operation of the converter. Similar measurement can be conducted on S4. However, the proposed method cannot be applied to S2 and S3 during the operation of the converter. The requirement for conducting measurement on S2 and S3 is the same as the full-bridge topology: phase current needs to be zero before this method can be applied.

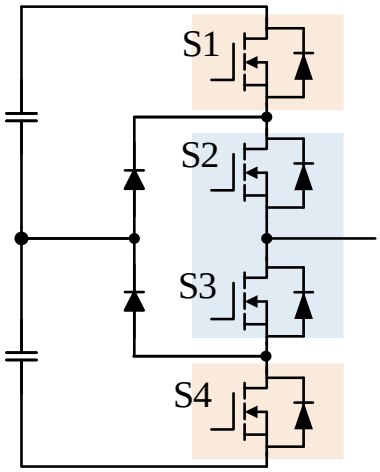


Fig. 5-36 Typical NPC topology

5.6. Discussion on Health Monitoring

This subsection is intended to link the proposed contents with health monitoring. From 5.2, it is presented that V_{th} shift can be used as an indicator for the health condition of the gate oxide of a MOSFET: the longer a MOSFET works under a gate voltage, the more V_{th} will shift. Therefore, a threshold can be set to remind the consumer to replace devices if V_{th} shifts too much. So that the oxide will not break down due to the increasing charges trapped inside. V_{th} can be measured periodically in case it exceeds the threshold. However, V_{th} is not easy to measure with traditional method. To solve the problem, a new method is proposed in 5.1 to measure V_{th} with low cost. Another problem with V_{th} shift is the influence of temperature. A solution to decouple the influence is proposed by using the short-time V_{th} shift slope. Moreover, the channel mobility can also be used to decouple the influence of temperature. These two methods are presented in 5.4. Finally, considering that the device is required to be shorted during the measurement, different topologies are discussed to apply the method.

Chapter 6 Conclusion and Future Work

6.1. Conclusion

SiC MOSFET has witnessed a rapid development with its potential to achieve high-efficiency, high-frequency, high-power-density and high-temperature applications. However, there are many problems when replacing Si device with SiC MOSFET. This thesis focuses on two of the problems: switching transient oscillation and threshold voltage shift, presenting detailed analysis in the switching transient optimization and capturing the threshold voltage shifts.

A unique current-controlled gate driver has been designed and constructed to help with the two above challenges. The proposed gate driver has two key features: 1. The output current of the proposed gate driver is fully controlled; 2. The profile of the output current follows the control of the programmed input signal. With the proposed gate driver, arbitrary gate currents can be generated to achieve switching transient optimization and threshold voltage measurement. The structure of the proposed gate driver is discussed and compared with the structure of the conventional gate driver, illustrating the advantages of the proposed gate driver over the conventional gate driver. The proposed gate driver consists of three functional circuits: isolation circuit, signal amplification circuit and signal conversion circuit. Different topologies for each function are compared and discussed. After the selection of components, two gate driver circuits are constructed. Finally, additional modifications on the topology and the control strategy are presented to improve the stability of the gate driver.

In the analysis of the switching transient optimization, three different gate control strategies are discussed, showing that the current-control strategy is a better way to control the switching transients because switching waveforms are less dependent on the parasitic inductance in the source terminal. Apart from that, detailed analysis on the switching oscillation mechanism is demonstrated. The small signal model in each switching period is presented. The oscillation source and the impact factors of the oscillation are discussed. Based on the analysis, novel gate driving signals are proposed to improve the performance of the turn-on and turn-off transient respectively. Finally, double-pulse tests are conducted using the proposed gate driving signals

and results are compared with the conventional gate driving signal. It is shown that the proposed gate driving signals presents both lower switching loss and lower overshoot in comparison with the conventional gate driving method.

The effect of threshold voltage shift is investigated including long-time V_{th} shift and short-time V_{th} shift. Firstly, an innovative V_{th} measurement method using a current-controlled gate driver is proposed. In addition, it is shown that the measurement method can also easily be embedded in conventional gate drivers. Next, the relationship between V_{th} shift and the gate stress time is investigated using the proposed measurement method. The logarithm model is used to describe the influence of the gate stress time on V_{th}. Specifically, the short-time V_{th} shift phenomenon is investigated. A double-layer trap model is proposed to explain the short-time V_{th} shift phenomenon. Based on the model, the influences of gate current, temperature and gate stress on the short-time V_{th} shift effect are analyzed. It is found out that the gate stress has negligible impact on the short-time V_{th} shift process, making the slope of the short-time V_{th} shift as a good indicator for temperature measurement (Temperature Sensitive Electric Parameter). Finally, the feasibility of conducting the proposed V_{th} measurement method on different topologies is discussed.

6.2. Future Work

6.2.1. Improvement on the Proposed Gate Driver

Limited by the output current of the amplifier and the operating frequency of the controller, the maximum output current of the gate driver is lower than 300mA, and the minimum current step time interval is 13ns. The low output current of the gate driver limits the switching speed of the device, while the large time interval limits the time accuracy of high-speed control. In the future, the proposed gate driver can be improved in two ways: firstly, the output current of the gate driver can be increased; secondly, the time resolution of the controller can be improved.

To increase the output current of the gate driver, amplifiers with higher current capability can be used to replace THS4631. The output current of THS4631 is 150mA, which is not enough to drive a high speed turn on. An example to replace THS4631 is THS3491 from TI. The output current of THS3491 is 420mA, which is around 3 times the value of the current amplifier.

Beside, the parallel structure can be implemented to further increase the output current. For example, the signal conversion circuit (Fig. 3-13) can be duplicated and paralleled to double the output current capability of the gate driver.

To improve the time resolution of the gate driver, higher performance controller and DAC needs to be used. For example, the controller can be changed to faster FPGA instead of DSP; the DAC can be changed to DAC38RF80 instead of AD9104. In principle, the time resolution can be improved from 13ns to 2ns after replacing the control system.

6.2.2. Switching Transient Optimization

It is presented in Chapter 4 that the optimized gate driving signals are closely related to the load current. However, in the proposed method, the shape of the gate driving signals are pre-programmed, which means the gate driving signal needs to be re-programmed if the load current changes. The complicated process limits the application of the proposed gate driver.

To extend the application of the proposed gate driver in a wider load current range, the close-loop control strategy can be implemented. For example, the drain current of the MOSFET is sampled and feedback to the controller. The detected drain current is compared with a reference value. If the drain current is higher than the reference, the gate current is reduced to a low value. Therefore, the time interval of the high gate current can be determined. The gate current signal can be automatically controlled by the detected drain current. Moreover, it is also woth investigating that which signal is the best for the feedback control. There are 3 possible candidates: the drain current (i_D), the diode current (i_{Diode}) and the slope of the drain current (di_D/dt). The effectiveness of the feedback can be compared with the open-loop control method.

Currently, all the tests are based on the double pulse test platform. In the future, the performance of the gate driver can be evaluated in a continuous runing converter, a boost converter for example. In principle, the efficiency of the boost converter can be improved due to the reduced switching loss. Moreover, the EMI of the boost converter can also be reduced as less ringing is introduced if the proposed gate driver is used. The proposed gate driver can also be applied to a DC/AC converter, like a moter driver, if the close-loop control strategy is implemented.

6.2.3. Threshold Voltage Shift

The experiment in Chapter 5 is conducted on a single MOSFET, which is not connected into a converter. In the future, the proposed method can be applied to a continuous runing converter. The discussion presented in Section 5.5 can be verified on the possibility to apply online detection of the threshold voltage shift.

In this work, the MOSFET is stressed under 30V to accelerate the shift process. However, this can be question because 30V is much higher than the recommanded value (20V). Therefore, in the future work, the relationship between the normal shift process (20V) and the accelerated shift process (30V) can be investigated. It is expected that a coefficient K can be derived, which indicates that the shift of a MOSFET under 30V for 1 hour equals to its shift under 20V for K hours. This parameter can be an indicator for the remain useful time of a MOSFET.

The MOSFET studied in this work are only stressed for 5 hours, which is far from the life time. Longer stress time can be applied to explore the limitation of the gate stress. Moreover, the influence of the temperature on the remain useful life of a MOSFET is not investigation in this work. It is expected that high temperature reduces the remain useful life. Therefore, the gate stress under different temperatures can be applied to a MOSFET to study the thermal impact on the gate health condition.

References

[1] M. A. Hannan, M. S. H. Lipu, P. J. Ker, R. A. Begum, V. G. Agelidis, and F. Blaabjerg, "Power electronics contribution to renewable energy conversion addressing emission reduction: Applications, issues, and recommendations," *Appl. Energy*, vol. 251, no. December 2018, p. 113404, 2019.

[2] B. K. Bose, "Global Energy Scenario and Impact of Power Electronics in 21st Century," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2638–2651, Jul. 2013.

[3] F. Blaabjerg, Y. Yang, and K. Ma, "Power electronics - Key technology for renewable energy systems - Status and future," *2013 3rd Int. Conf. Electr. Power Energy Convers. Syst. EPECS 2013*, pp. 0–5, 2013.

[4] I. E. A. OECD, "Energy and Air Pollution: World Energy Outlook Special Report 2016," 2016.

[5] C. Pelletier, Y. Rogaume, L. Dieckhoff, G. Bardeau, M. N. Pons, and A. Dufour, "Effect of combustion technology and biogenic CO2 impact factor on global warming potential of wood-to-heat chains," *Appl. Energy*, vol. 235, no. November 2018, pp. 1381–1388, 2019.

[6] S. K Ghosh, "Fossil Fuel Consumption Trend and Global Warming Scenario: Energy Overview," *Glob. J. Eng. Sci.*, vol. 5, no. 2, pp. 3–8, 2020.

[7] G. Zhang, Z. Li, B. Zhang, and W. A. Halang, "Power electronics converters: Past, present and future," *Renew. Sustain. Energy Rev.*, vol. 81, no. June 2017, pp. 2028–2044, 2018.

[8] T. Kimoto, "Material science and device physics in SiC technology for high-voltage power devices," *Jpn. J. Appl. Phys.*, vol. 54, no. 4, 2015.

[9] K. Shenai, M. Dudley, and R. F. Davis, "Rugged electrical power switching in semiconductors: A systems approach," *Proc. IEEE*, vol. 102, no. 1, pp. 35–52, 2014.

[10] K. Shenai, M. Dudley, and R. F. Davis, “Current Status and Emerging Trends in Wide Bandgap (WBG) Semiconductor Power Switching Devices,” *ECS J. Solid State Sci. Technol.*, vol. 2, no. 8, pp. N3055–N3063, 2013.

[11] F. Roccaforte *et al.*, “Emerging trends in wide band gap semiconductors (SiC and GaN) technology for power devices,” *Microelectron. Eng.*, vol. 187–188, pp. 66–77, Feb. 2018.

[12] H. Amano *et al.*, “The 2018 GaN power electronics roadmap,” *J. Phys. D. Appl. Phys.*, vol. 51, no. 16, p. 163001, Apr. 2018.

[13] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, “Performance and Reliability Review of 650 v and 900 v Silicon and SiC Devices: MOSFETs, Cascode JFETs and IGBTs,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7375–7385, 2020.

[14] H. Li, Y. Ma, R. Ren, and F. Wang, “SiC impact on grid power electronics converters,” *IEEE Power Energy Soc. Gen. Meet.*, vol. 2020–Augus, 2020.

[15] M. F. Yaakub, M. A. M. Radzi, F. H. M. Noh, and M. Azri, “Silicon carbide power device characteristics, applications and challenges: An overview,” *Int. J. Power Electron. Drive Syst.*, vol. 11, no. 4, pp. 2194–2202, 2020.

[16] X. Guo, Q. Xun, Z. Li, and S. Du, “Silicon carbide converters and MEMS devices for high-temperature power electronics: A critical review,” *Micromachines*, vol. 10, no. 6, 2019.

[17] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, “Review of Silicon Carbide Power Devices and Their Applications,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, 2017.

[18] F. Ji S., Zhang Z., Wang, “Overview of High Voltage SiC Power Semiconductor Devices: Development and Application,” *Ces Trans. Electr. Mach. Syst.*, vol. 1, no. 3, pp. 254–264, 2017.

[19] M. Rahimo, “Performance Evaluation and Expected Challenges of Silicon Carbide Power MOSFETs for High Voltage Applications,” *Mater. Sci. Forum*, vol. 897, pp. 649–

654, May 2017.

[20] M. Ostling, R. Ghandi, and C. M. Zetterling, “SiC power devices - Present status, applications and future perspective,” *Proc. Int. Symp. Power Semicond. Devices ICs*, pp. 10–15, 2011.

[21] N. Kondrath and M. Kazimierczuk, “Characteristics and applications of silicon carbide power devices in power electronics,” *Int. J. Electron. Telecommun.*, vol. 56, no. 3, pp. 231–236, 2010.

[22] J. Lutz, “Semiconductor power devices as key technology for a future sustainable society: Power devices - state of the art and future trends,” *Bauelemente der Leistungselektronik und ihre Anwendungen 2017 - 7. ETG-Fachtagung*, pp. 7–21, 2017.

[23] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices*, vol. 2. Cham: Springer International Publishing, 2018.

[24] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, “A Survey of Wide Bandgap Power Semiconductor Devices,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, 2014.

[25] M. Shur, “Wide band gap semiconductor technology: State-of-the-art,” *Solid. State. Electron.*, vol. 155, no. March, pp. 65–75, 2019.

[26] H. Matsunami, “Fundamental research on semiconductor SiC and its applications to power electronics,” *Proc. Japan Acad. Ser. B Phys. Biol. Sci.*, vol. 96, no. 7, pp. 235–254, 2020.

[27] M. Lades, “Modeling and simulation of wide bandgap semiconductor devices: 4H/6H-SiC,” 2000.

[28] Rohm Semiconductors, “SiC Power Devices and Modules,” *Appl. Note*, no. June, 2013.

[29] H. Matsunami and T. Kimoto, “Step-controlled epitaxy of SiC: High-quality homoepitaxial growth,” *Diam. Relat. Mater.*, vol. 7, no. 2–5, pp. 342–347, Feb. 1998.

[30] T. Kimoto, “Progress and future challenges of silicon carbide devices for integrated

circuits," *Proc. IEEE 2014 Cust. Integr. Circuits Conf. CICC 2014*, 2014.

[31] P. Gammon, "Silicon and the wide bandgap semiconductors, shaping the future power electronic device market," *ULIS 2013 14th Int. Conf. Ultim. Integr. Silicon, Inc. "Technology Brief. Day,"* no. March 2013, pp. 9–13, 2013.

[32] K. Madjour, "Silicon Carbide market update : From discrete devices to modules…," *Pcim 2014*, no. May, 2014.

[33] M. Furuhashi, S. Tomohisa, T. Kuroiwa, and S. Yamakawa, "Practical applications of SiC-MOSFETs and further developments," *Semicond. Sci. Technol.*, vol. 31, no. 3, 2016.

[34] M. Pérez-Tarragona, H. Sarnago, Ó. Lucía, and J. M. Burdío, "High performance full-bridge multi-inverter featuring 900-V SiC devices for domestic induction heating applications," *EPE J. (European Power Electron. Drives Journal)*, vol. 27, no. 4, pp. 143–152, 2017.

[35] M. Kitabatake *et al.*, "4H-SiC-DIMOSFET power device for home appliances," *2010 Int. Power Electron. Conf. - ECCE Asia -, IPEC 2010*, pp. 3249–3253, 2010.

[36] H. Sarnago, Ó. Lucía, and J. M. Burdío, "A Comparative Evaluation of SiC Power Devices for High-Performance Domestic Induction Heating," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4795–4804, 2015.

[37] J. Jordan *et al.*, "A Comparative Performance Study of a 1200 V Si and SiC MOSFET Intrinsic Diode on an Induction Heating Inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2550–2562, May 2014.

[38] S. Buschhorn and K. Vogel, "Saving money: SiC in UPS applications," *PCIM Eur. Conf. Proc.*, no. May, pp. 765–771, 2014.

[39] M. Su, C. Chen, S. Sharma, and J. Kikuchi, "Performance and cost considerations for SiC-based HEV traction inverter systems," *WiPDA 2015 - 3rd IEEE Work. Wide Bandgap Power Devices Appl.*, pp. 347–350, 2015.

[40] W. Cai, X. Wu, M. Zhou, Y. Liang, and Y. Wang, "Review and Development of Electric

Motor Systems and Electric Powertrains for New Energy Vehicles," *Automot. Innov.*, no. 0123456789, Feb. 2021.

[41] K. Ishikawa, S. Yukutake, Y. Kono, K. Ogawa, and N. Kameshiro, "Traction inverter that applies compact 3.3 kV / 1200 A SiC hybrid module," *2014 Int. Power Electron. Conf. IPEC-Hiroshima - ECCE Asia 2014*, pp. 2140–2144, 2014.

[42] Q. Xun, B. Xun, Z. Li, P. Wang, and Z. Cai, "Application of SiC power electronic devices in secondary power source for aircraft," *Renew. Sustain. Energy Rev.*, vol. 70, no. November 2015, pp. 1336–1342, 2017.

[43] S. Yin, K. J. Tseng, R. Simanjorang, Y. Liu, and J. Pou, "A 50-kW High-Frequency and High-Efficiency SiC Voltage Source Inverter for More Electric Aircraft," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9124–9134, 2017.

[44] C. Bentheimer, A. Islami, S. Mainusch, F. Hilpert, B. Eckardt, and M. März, "Highly efficient SiC inverter for aircraft application with innovative thermal management," *PCIM Eur. Conf. Proc.*, no. May, pp. 1190–1197, 2019.

[45] T. Miazga, G. Iwański, and M. Nikoniuk, "Energy Conversion System and Control of Fuel-Cell and Battery-Based Hybrid Drive for Light Aircraft," *Energies*, vol. 14, no. 4, p. 1073, Feb. 2021.

[46] M. John, B. Agrawal, and J. Liu, "Efficient and compact 50kW Gen2 SiC device Based PV string inverter," *PCIM Eur. Conf. Proc.*, no. May, pp. 780–786, 2014.

[47] K. Fujii, Y. Noto, and Y. Okuma, "1-MW solar power inverter with boost converter using all SiC power module," *EPE J. (European Power Electron. Drives Journal)*, vol. 26, no. 4, pp. 165–173, 2016.

[48] F. Blaabjerg and K. Ma, "Future on power electronics for wind turbine systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 1, no. 3, pp. 139–152, 2013.

[49] S. Tiwari, T. Undeland, O. M. Midtgard, and R. Nilsen, "SiC MOSFETs for Offshore Wind Applications," *J. Phys. Conf. Ser.*, vol. 1104, no. 1, 2018.

[50] C. Neumann, R. Schmidtke, T. M. Plötz, and H. G. Eckel, “An economic evaluation of sic-mosfet modules in wind turbine converters,” *PCIM Eur. Conf. Proc.*, vol. 1, no. July, pp. 836–843, 2020.

[51] A. Hussein and A. Castellazzi, “Comprehensive design optimization of a wind power converter using SiC technology,” in *2018 International Conference on Smart Grid (icSmartGrid)*, 2018, pp. 34–38.

[52] X. Yuan, I. Laird, and S. Walder, “Opportunities, Challenges, and Potential Solutions in the Application of Fast-Switching SiC Power Devices and Converters,” *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3925–3945, 2021.

[53] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, “Active gate driver for fast switching and cross-talk suppression of SiC devices in a phase-leg configuration,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2015–May, no. May, pp. 774–781, 2015.

[54] S. Zeltner *et al.*, “Advantages and challenges of using sic mosfets in a high power density insulated hv/lv dc/dc converter,” *PCIM Eur. Conf. Proc.*, vol. 1, no. July, pp. 1587–1592, 2020.

[55] D. A. Gajewski, “Challenges and Peculiarities in Developing New Standards for SiC,” *IEEE Int. Reliab. Phys. Symp. Proc.*, vol. 2020–April, 2020.

[56] J. Wang and X. Jiang, “Review and analysis of SiC MOSFETs’ ruggedness and reliability,” *IET Power Electron.*, vol. 13, no. 3, pp. 445–455, 2020.

[57] H. Xu, “Research on Interface State and Reliability of 4H-SiC MOSFETs with Thermal Gate Oxide,” Tokushima University, 2020.

[58] A. J. Lelis, R. Green, and D. B. Habersat, “SiC MOSFET threshold-stability issues,” *Mater. Sci. Semicond. Process.*, vol. 78, no. August 2017, pp. 32–37, 2018.

[59] J. W. McPherson and D. A. Baglee, “Acceleration Factors for Thin Gate Oxide Stressing,” in *23rd International Reliability Physics Symposium*, 1985, vol. 77001, pp. 1–5.

[60] D. A. Gajewski *et al.*, "SiC power device reliability," *Proc. 2016 IEEE Int. Integr. Reliab. Work. IIRW 2016*, pp. 29–34, 2017.

[61] D. J. Lichtenwalner *et al.*, "Reliability studies of SiC vertical power MOSFETs," *IEEE Int. Reliab. Phys. Symp. Proc.*, vol. 2018–March, p. 2B.21-2B.26, 2018.

[62] J. S. Suehle, "Ultrathin gate oxide reliability: Physical models, statistics, and characterization," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 958–971, 2002.

[63] J. J. Sumakeris *et al.*, "Techniques for Minimizing the Basal Plane Dislocation Density in SiC Epilayers to Reduce V_f Drift in SiC Bipolar Power Devices," *Mater. Sci. Forum*, vol. 527–529, pp. 141–146, 2006.

[64] E. Van Brunt *et al.*, "Industrial and body diode qualification of GEN-III medium voltage SIC MOSFETs: Challenges and solutions," *Mater. Sci. Forum*, vol. 963 MSF, pp. 805–810, 2019.

[65] J. Sun, H. Xu, X. Wu, and K. Sheng, "Comparison and analysis of short circuit capability of 1200V single-chip SiC MOSFET and Si IGBT," *2016 Int. Forum Wide Bandgap Semicond. China, IFWS 2016 - Conf. Proc.*, vol. 3, pp. 42–45, 2017.

[66] Z. Wang *et al.*, "Temperature-Dependent Short-Circuit Capability of Silicon Carbide Power MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1555–1566, 2016.

[67] J. W. Palmour, "Silicon carbide power device development for industrial markets," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2015–Febru, no. February, p. 1.1.1-1.1.8, 2015.

[68] Z. Han *et al.*, "A trench/planar SiC MOSFET integrated with SBD (TPSBD) for low reverse recovery charge and low switching loss," *Semicond. Sci. Technol.*, vol. 35, no. 10, 2020.

[69] J. Kim, D. Shin, and S. K. Sul, "A Damping Scheme for Switching Ringing of Full SiC MOSFET by Air Core PCB Circuit," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4605–4615, 2018.

[70] D. P. Sadik, K. Kostov, J. Colmenares, F. Giezendanner, P. Ranstad, and H. P. Nee, "Analysis of Parasitic Elements of SiC Power Modules with Special Emphasis on Reliability Issues," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 988–995, 2016.

[71] Z. Wang, J. Zhang, X. Wu, and K. Sheng, "Analysis of stray inductance's influence on SiC MOSFET switching performance," *2014 IEEE Energy Convers. Congr. Expo. ECCE 2014*, pp. 2838–2843, 2014.

[72] H. Li and S. Munk-nielsen, "Challenges in Switching SiC MOSFET without Ringing," *PCIM Eur.*, no. May, pp. 20–22, 2014.

[73] Toshiba, "Commercialization of new TO-247-4L packaging 600-V Super Junction Power MOSFET (DTMOSIV-H Series)." [Online]. Available: https://toshiba.semicon-storage.com/eu/semiconductor/product/mosfets/400v-900v-mosfets/articles/commercialization-of-new-to-247-4l-packaging-600-v-super-junction-power-mosfet-dtmos4-h-series.html.

[74] B. Zhang and S. Wang, "Parasitic inductance modeling and reduction for a wire bonded half bridge SiC MOSFET multichip power module," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2019–March, pp. 656–663, 2019.

[75] J. Ke *et al.*, "Investigation of Low-Profile, High-Performance 62-mm SiC Power Module Package," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6777, no. c, pp. 1–1, 2020.

[76] T. Liu, R. Ning, T. T. Y. Wong, and Z. J. Shen, "Modeling and Analysis of SiC MOSFET Switching Oscillations," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 747–756, 2016.

[77] T. Liu, Y. Zhou, Y. Feng, T. T. Y. Wong, and Z. John Shen, "Experimental and Modeling Comparison of Different Damping Techniques to Suppress Switching Oscillations of SiC MOSFETs," *2018 IEEE Energy Convers. Congr. Expo. ECCE 2018*, pp. 7024–7031, 2018.

[78] S. Zhao, X. Zhao, Y. Wei, Y. Zhao, and H. A. Mantooth, "A Review on Switching Slew

Rate Control for Silicon Carbide Devices using Active Gate Drivers," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6777, no. c, pp. 1–1, 2020.

[79] Y. Han, H. Lu, Y. Li, and J. Chai, "Open-Loop Gate Control for Optimizing the Turn-On Transition of SiC MOSFETs," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. PP, no. c, p. 1, 2018.

[80] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez, "A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9032–9042, Nov. 2017.

[81] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent Gate Drive for Fast Switching and Crosstalk Suppression of SiC Devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, 2017.

[82] S. Zhao *et al.*, "Adaptive Multi-Level Active Gate Drivers for SiC Power Devices," *IEEE Trans. Power Electron.*, vol. PP, no. c, pp. 1–1, 2019.

[83] B. Lasek, P. Trochimiuk, R. Kopacz, and J. Rąbkowski, "Parasitic-Based Active Gate Driver Improving the Turn-On Process of 1.7 kV SiC Power MOSFET," *Appl. Sci.*, vol. 11, no. 5, p. 2210, Mar. 2021.

[84] Y. Wen, Y. Yang, and Y. Gao, "Active Gate Driver for Improving Current Sharing Performance of Paralleled High-Power SiC MOSFET Modules," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1491–1505, 2021.

[85] Y. Lu and W. Yao, "An Active Gate Driver Design to Reduce Voltage and Current Overshoots for SiC MOSFET Modules," in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, 2020, pp. 915–920.

[86] Y. Jiang, C. Feng, Z. Yang, X. Zhao, and H. Li, "A new active gate driver for MOSFET to suppress turn-off spike and oscillation," *Chinese J. Electr. Eng.*, vol. 4, no. 2, pp. 43–49, Jun. 2018.

[87] J. Chen, Y. Li, M. Liang, R.Kennel, J. Liu, and H. Guo, “A Novel Gate Driver for Suppressing Overcurrent and Overvoltage of SiC MOSFET,” in *10th International Conference on Power Electronics-ECCE Asia*, 2019.

[88] J. O. Gonzalez, O. Alatise, J. Hu, L. Ran, and P. A. Mawby, “An Investigation of Temperature-Sensitive Electrical Parameters for SiC Power MOSFETs,” *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7954–7966, 2017.

[89] A. Griffo, J. Wang, K. Colombage, and T. Kamel, “Real-time measurement of temperature sensitive electrical parameters in SiC power mosfets,” *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2663–2671, 2018.

[90] L. Li, P. Ning, D. Zhang, and X. Wen, “An exploration of thermo-sensitive electrical parameters to estimate the junction temperature of silicon carbide mosfet,” *2017 IEEE Transp. Electrif. Conf. Expo, Asia-Pacific, ITEC Asia-Pacific 2017*, pp. 4–8, 2017.

[91] C. T. Yen *et al.*, “Oxide breakdown reliability of sic mosfet,” *WiPDA Asia 2019 - IEEE Work. Wide Bandgap Power Devices Appl. Asia*, pp. 1–3, 2019.

[92] P. Hofstetter, R. W. Maier, and M.-M. Bakran, “Influence of the Threshold Voltage Hysteresis and the Drain Induced Barrier Lowering on the Dynamic Transfer Characteristic of SiC Power MOSFETs,” in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 944–950.

[93] R. Mandeya, C. Chen, V. Pickert, and R. T. Naayagi, “Prethreshold Voltage as a Low-Component Count Temperature Sensitive Electrical Parameter Without Self-Heating,” *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2787–2791, Apr. 2018.

[94] I. Bakun, N. Čobanov, and Ž. Jakopović, “Real-Time Measurement of IGBT’s Operating Temperature,” *Automatika*, vol. 52, no. 4, pp. 295–305, 2011.

[95] V. Huard, M. Denais, and C. Parthasarathy, “NBTI degradation: From physical mechanisms to modelling,” *Microelectron. Reliab.*, vol. 46, no. 1, pp. 1–23, 2006.

[96] J. Wörle, “Approaching the SiO2/SiC Interface: Novel Concepts for the Characterization

of the Near-Interface Region," 2019.

[97] K. Puschkarsky, H. Reisinger, T. Aichinger, W. Gustin, and T. Grasser, "Threshold voltage hysteresis in SiC MOSFETs and its impact on circuit operation," *IEEE Int. Integr. Reliab. Work. Final Rep.*, vol. 2017–Octob, pp. 1–5, 2018.

[98] M. Miura-Mattausch, H. Kikuchihara, T. K. Maiti, D. Navarro, and H. J. Mattausch, "Modeling of Carrier Trapping and Its Impact on Switching Performance," *IEEE J. Electron Devices Soc.*, vol. 6, no. June, pp. 1056–1063, 2018.

[99] T. Aichinger, G. Rescher, and G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectron. Reliab.*, vol. 80, no. August 2017, pp. 68–78, 2018.

[100] CREE, "SiC MOSFET Isolated Gate Driver." [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/572/product/199/crd_001.pdf.

[101] W. Eberle, Z. Zhang, Y. F. Liu, and P. C. Sen, "A high efficiency synchronous buck VRM with current source gate driver," *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, pp. 21–27, 2007.

[102] L. Shu, J. Zhang, F. Peng, and Z. Chen, "Active Current Source IGBT Gate Drive with Closed-Loop di/dt and dv/dt Control," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3787–3796, 2017.

[103] J. Huntington, *Show networks and control systems: formerly control systems for live entertainment*. John Huntington, 2012.

[104] L. F. S. Alves, P. Lefranc, P. O. Jeannin, and B. Sarrazin, "Review on SiC-MOSFET devices and associated gate drivers," *Proc. IEEE Int. Conf. Ind. Technol.*, vol. 2018–Febru, pp. 824–829, 2018.

[105] B. Sun, Z. Zhang, and M. A. E. Andersen, "Review of Resonant Gate Driver in Power Conversion," *2018 Int. Power Electron. Conf. (IPEC-Niigata 2018 -ECCE Asia)*, pp. 607–613, 2018.

[106] S. Mocevic *et al.*, “Phase current reconstruction based on rogowski coils integrated on gate driver of SiC MOSFET half-bridge module for continuous and discontinuous PWM inverter applications,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2019–March, pp. 1029–1036, 2019.

[107] B. Chen, “Isolated half-bridge gate driver with integrated high-side supply,” *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, pp. 3615–3618, 2008.

[108] X. Wang, H. Wu, and V. Pickert, “Design of an advanced programmable current-source gate driver for dynamic control of SiC device,” *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 2019–March, pp. 1370–1374, 2019.

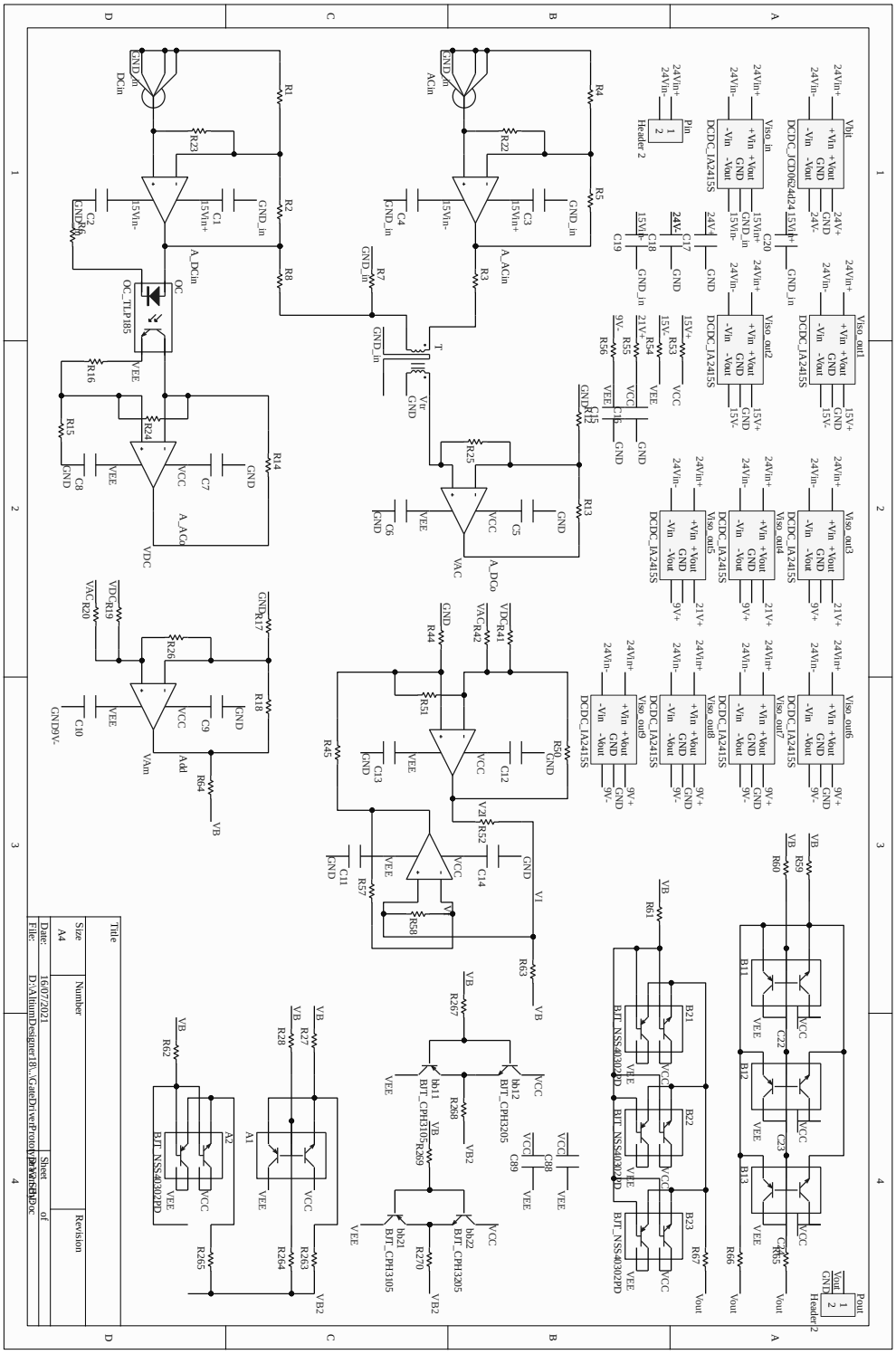
[109] P. Bertemes-Filho, A. Felipe, and V. C. Vincence, “High Accurate Howland Current Source: Output Constraints Analysis,” *Circuits Syst.*, vol. 04, no. 07, pp. 451–458, 2013.

[110] H. Chen, V. Pickert, D. J. Atkinson, and L. S. Pritchard, “On-line monitoring of the MOSFET device junction temperature by computation of the threshold voltage,” in *3rd IET International Conference on Power Electronics, Machines and Drives (PEMD 2006)*, 2006, vol. 2006, no. 0, pp. 440–444.

[111] S. I. Hayashi and K. Wada, “Accelerated aging test for gate-oxide degradation in SiC MOSFETs for condition monitoring,” *Microelectron. Reliab.*, vol. 114, no. May, p. 113777, 2020.

Appendix I

This appendix shows the detailed diagram of the proposed gate driver used in the experiment, including the power supply, signal isolation circuit, signal amplification and signal conversion. The part number of each component can be found in 3.4.1.



Appendix II

This appendix shows the original code of the Pspice model SCT3060. The equivalent circuit in Fig. 5-23 is derived based on the code.

```
* SCT3060AL_LT
* SiC NMOSFET model
* 650V 39A 60mOhm
* Model Generated by ROHM
* All Rights Reserved
* Commercial Use or Resale Restricted
* Date: 2018/07/02
********************D G S
.SUBCKT SCT3060AL_LT 1 2 3
.PARAM T0=25
.PARAM TEMP=50
.FUNC R1(I)      {41.36m*I*EXP((TEMP-
T0)/238.2)+21.52u*I*ABS(I)**1.614*EXP((TEMP-T0)/-2464)}
.FUNC R2(I)      {I*(3.6*(1+TANH(I))/2+2.1*(1-TANH(I))/2)}
.FUNC V1(I)      {216.3m*ASINH(I/0.06749)*EXP((TEMP-T0)/-422.0)+
+                 670.1m*ASINH(I/1.918)*EXP((TEMP-T0)/-
2874)+40.27m*I*EXP((TEMP-T0)/462.8)}
.FUNC V2(V)      {77.46f*V**(16.18*EXP((TEMP-T0)/4501))*EXP((TEMP-
T0)/37.82*EXP((TEMP-T0)/-1787))}
.FUNC V3(V)      {57.62*SINH(V/57.62)}
.FUNC I1(V,W)    {V3(V)*(1+2.993*(TANH((V3(V)-18.71)/23.25)+1)*EXP((TEMP-
T0)/-155.4)/10)*
+                 W/(ABS(W)+2.993*(TANH((V3(V)-18.71)/23.25)+1)*EXP((TEMP-
T0)/-155.4))}
.FUNC C1(U,V,W) {(281.7*V+707.5*(1-W/1.094)**-
0.4356)*(0.1472*TANH((U+7.331)/2.400)+0.8528)}
V1  1 11 0
E1 11 12 VALUE={R1(I(V1))}
V2  2 21 0
E2 21 22 VALUE={R2(I(V2))}
L1  3 32 6.5n
R2  3 32 10
E6 41  0 VALUE={MIN(MAX(V(22,32),0),22)}
V6 41 42 0
E7 42 43 VALUE={V1(I(V6))}
G6 43  0 VALUE={MIN(MAX(V2(MAX(V(43),0)),-300),300)}
C6 43  0 1p
R6 43  0 1T
```

```
G1 12 32 VALUE={MIN(MAX(I1(MAX(I(V6),0),V(12,32)),-200),200)}
C7 12 32 1p
R3 12 32 1T
V3 22 23 0
C1 23 12 1p
G2 22 12
VALUE={I(V3)*C1(V(22,12),MIN(MAX(V(22,12),0),1.84),MIN(V(22,12),0))}
C2 22 32 748.7p
R4 22  3 1G
********* ********* ********* ********* ********* ********* *********
********* ********* ********* *********
.FUNC R11(I)   {80.63m*ASINH(I/0.3144)*EXP((TEMP-
T0)/222.7)+61.10m*I*EXP((TEMP-T0)/714.6)}
.FUNC I11(V)   {50.45n*(EXP(V/0.1059/EXP((TEMP-T0)/-305.0))-1)*EXP((TEMP-
T0)/-67.34*EXP((TEMP-T0)/944.7))-
+               1u*TANH(-V/0.1)*EXP((TEMP-T0)/180.3)-231.9E-21*(EXP(-V/25)-
1)*EXP((TEMP-T0)/-200)}
.FUNC C11(V,W) {382.3*(V-1.127)+602.0*(1-W/2.255)**-0.5046}
V11 32 51 0
E11 51 52 VALUE={R11(I(V11))}
V12 52 53 0
C11 53  1 1p
G11 52  1 VALUE={MIN(MAX(I11(V(52,1)),-
200),200)+I(V12)*C11(MAX(V(52,1),1.127),MIN(V(52,1),1.127))}
R11 52  1 1T

.ENDS SCT3060AL_LT
```

Appendix III

This appendix shows the modified code of the Pspice model SCT3060 to include the influence of short time V_{th} shift. The modification can be found at the comment "original code" and "changes to" below:

```
* SCT3060AL_LT
* SiC NMOSFET model
* 650V 39A 60mOhm
* Model Generated by ROHM
* All Rights Reserved
* Commercial Use or Resale Restricted
* Date: 2018/07/02
********************D G S
.SUBCKT SCT3060AL_LT 1 2 3
.PARAM T0=25
.PARAM TEMP=50
.FUNC R1(I)      {41.36m*I*EXP((TEMP-
T0)/238.2)+21.52u*I*ABS(I)**1.614*EXP((TEMP-T0)/-2464)}
.FUNC R2(I)      {I*(3.6*(1+TANH(I))/2+2.1*(1-TANH(I))/2)}
.FUNC V1(I)      {216.3m*ASINH(I/0.06749)*EXP((TEMP-T0)/-422.0)+
+                 670.1m*ASINH(I/1.918)*EXP((TEMP-T0)/-
2874)+40.27m*I*EXP((TEMP-T0)/462.8)}
.FUNC V2(V)      {77.46f*V**(16.18*EXP((TEMP-T0)/4501))*EXP((TEMP-
T0)/37.82*EXP((TEMP-T0)/-1787))}
.FUNC V3(V)      {57.62*SINH(V/57.62)}
.FUNC I1(V,W)    {V3(V)*(1+2.993*(TANH((V3(V)-18.71)/23.25)+1)*EXP((TEMP-
T0)/-155.4)/10)*
+                 W/(ABS(W)+2.993*(TANH((V3(V)-18.71)/23.25)+1)*EXP((TEMP-
T0)/-155.4))}
.FUNC C1(U,V,W) {(281.7*V+707.5*(1-W/1.094)**-
0.4356)*(0.1472*TANH((U+7.331)/2.400)+0.8528)}
V1  1 11 0
E1 11 12 VALUE={R1(I(V1))}
V2  2 21 0
E2 21 22 VALUE={R2(I(V2))}
L1  3 32 6.5n
R2  3 32 10

* ******************Original codes*********************
* E6 41  0 VALUE={MIN(MAX(V(22,32),0),22)}
* V6 41 42 0
```

```
* changes to

E81 72  0 VALUE = {V(22,32)/5}
C81 72 71 100n
R81 71  0 1

E6 41  0 VALUE={MIN(MAX(V(22,32),0),22)}
E8 41 44 VALUE = {V(72,71)}
V6 44 42 0


* ******************************************************


E7 42 43 VALUE={V1(I(V6))}
G6 43  0 VALUE={MIN(MAX(V2(MAX(V(43),0)),-300),300)}
C6 43  0 1p
R6 43  0 1T
G1 12 32 VALUE={MIN(MAX(I1(MAX(I(V6),0),V(12,32)),-200),200)}
C7 12 32 1p
R3 12 32 1T
V3 22 23 0
C1 23 12 1p
G2 22 12
VALUE={I(V3)*C1(V(22,12),MIN(MAX(V(22,12),0),1.84),MIN(V(22,12),0))}
C2 22 32 748.7p
R4 22  3 1G
********* ********* ********* ********* ********* ********* *********
********* ********* ********* *********
.FUNC R11(I)   {80.63m*ASINH(I/0.3144)*EXP((TEMP-
T0)/222.7)+61.10m*I*EXP((TEMP-T0)/714.6)}
.FUNC I11(V)   {50.45n*(EXP(V/0.1059/EXP((TEMP-T0)/-305.0))-1)*EXP((TEMP-
T0)/-67.34*EXP((TEMP-T0)/944.7))-
+               1u*TANH(-V/0.1)*EXP((TEMP-T0)/180.3)-231.9E-21*(EXP(-V/25)-
1)*EXP((TEMP-T0)/-200)}
.FUNC C11(V,W) {382.3*(V-1.127)+602.0*(1-W/2.255)**-0.5046}
V11 32 51 0
E11 51 52 VALUE={R11(I(V11))}
V12 52 53 0
C11 53  1 1p
G11 52  1 VALUE={MIN(MAX(I11(V(52,1)),-
200),200)+I(V12)*C11(MAX(V(52,1),1.127),MIN(V(52,1),1.127))}
R11 52  1 1T

.ENDS SCT3060AL_LT
```