Research on the topology of switched capacitor multilevel inverter

PHD thesis

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Abstract

With the gradual depletion of fossil energy and the deterioration of the global climate caused by greenhouse gas emissions, renewable energy power generation has become a hot research topic today. Multi-level inverter is an important equipment in renewable energy power generation system. The switched capacitor inverter, which evolved on the basis of the multi-level inverter, has attracted widespread attention in recent years due to its advantages of self-boosting, self-balancing of capacitor voltage, and suitability for medium and high power.

This thesis conducts a comprehensive analysis and research on various multilevel inverters, and then proposes a 13-level switched capacitor inverter topology and a 17-level switched capacitor inverter topology. For the 13-level switched capacitor inverter, there are one DC source input and 3 times voltage gain of the output voltage. The number of the switch is 13 and the number of the diode is 2. The utilization of the t-type structure makes the output voltage step reduced to 1/2Vdc and the utilization of the crossing structure gives the topology the capability of inherent output voltage polarity shift. Redesigned series/parallel switched capacitor unit makes the inverter has the capability of flexible extension to output variable number of output voltage level and output voltage gain. Compared with diode-clamped multilevel inverter, when output the 13-voltage levels, the number of the switches utilize in the circuit is 24 and the number of diodes is 66. So the 13-level switched capacitor inverter proposed in this thesis, the number of the switch is approximately 1.85 times lower than that of the diode clamped multilevel inverter. The number of the diode is 33 times fewer than that of the diode clamped multilevel inverter. The flying capacitor inverter requires relatively more components for the same number of output voltage levels. Compared to the proposed 13-level switched capacitor inverter in this thesis, the flying capacitor inverter has 1.85 times the number of switches and 3 times the number of capacitors. Additionally, the flying capacitor multilevel inverter suffers from capacitor voltage

imbalance, whereas the inverter proposed in this thesis has the capability of self-balancing capacitor voltages.

The 17-level switched capacitor inverter proposed in this thesis is an optimization of the 13-level switched capacitor inverter. By repositioning the DC power sources and adding two necessary switches and one essential diode, the design achieves a higher number of output voltage levels and a 4 times output voltage gain. Based on the switched capacitor inverters with the same number of output levels designed by other scholars in recent years, the typical number of switches used is 20-24, the number of capacitors used is 5-8, and the achieved voltage gain is 2-3 times. Therefore, the 17-level switched capacitor inverter proposed in this thesis reduces the number of switches by 25%, the number of capacitors by 33.3%, and improves the voltage gain by 33.3%. Both of these two proposed topologies are controlled by the phase disposition pulse width modulation (PDPWM) strategy and MATLAB/Simulink is utilized to conduct simulation studies on the two proposed topologies, with a detailed comparative analysis. The results indicate that the device cost of the proposed 17-level switched capacitor inverter is reduced by 34% compared to that of the 13-level switched capacitor inverter, implying a lower component count for the 17-level inverter. Additionally, the Peak Voltage Stress of the 17-level switched capacitor inverter is reduced by 25% compared to the 13-level inverter. In subsequent hardware experiments, the control logic for the 17-level switched capacitor inverter is implemented using FPGA, and detailed experiments are carried out to evaluate its output performance under various load conditions. The results demonstrate the good performance of the proposed 17-level switched capacitor inverter.

ACKNOWLEDGEMENT

I wish to express my profound gratitude to my supervisor, Matthew Armstrong, for his invaluable guidance and unwavering support during my academic pursuits. His expertise, empathy, and patience have greatly enriched my graduate experience. His astute mentorship has been instrumental in the fruition of this research, and his steady encouragement has been the driving force behind my dedication to this project.

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List of abbreviations

DCMLI	Diode-clamped multilevel inverter
FCMLI	Flying-capacitor multilevel inverter
CHBMLI	Cascaded H-bridge multilevel inverter
SCMLI	Switched capacitor multilevel inverter
PV	Photovoltaics
EMI	Electromagnetic interference
PWM	Pulse width modulation
SPWM	Sinusoidal pulse width modulation
PSPWM	Phase shifted carrier pulse width modulation
LSPWM	Level shifted pulse width modulation
PDPWM	Phase disposition pulse width modulation
PODPWM	Phase opposition disposition pulse width modulation
APODPWM	Alternative phase opposition disposition pulse width modulation
THD	Total harmonic distortion
BF	Boost factor
TSV	Total standing voltage
PVS	Peak voltage stress
CF	Cost factor
DSP	Digital signal processor
FPGA	Field programmable logic gate array
RTL	Register-Transfer Level
PLL	Phase-locked loop

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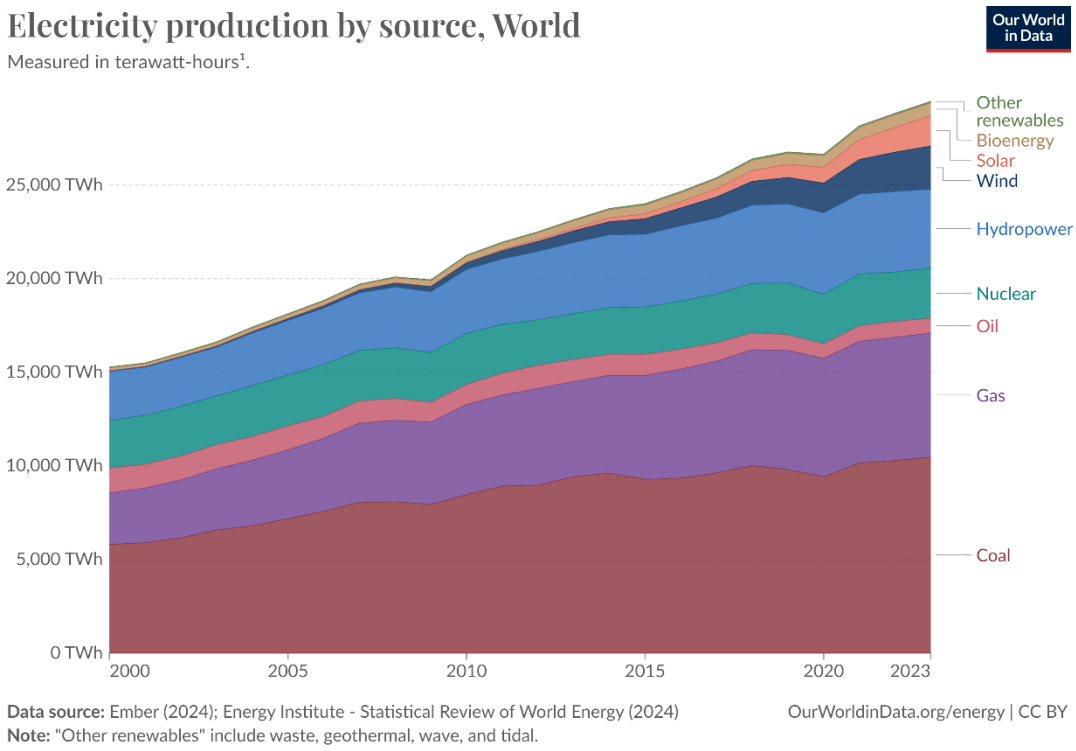
Chapter 1: Introduction

1.1 Background

With the growth of the world's population and the improvement of the overall economic level, industry and technology are developing rapidly. Human beings are increasingly dependent on electrical energy and consume more and more electrical energy. Currently, countries around the world generally rely on traditional fossil energy power generation to meet the growing electricity demand [1]. The long-term heavy reliance on fossil energy has gradually depleted resources, and the greenhouse effect produced by carbon dioxide emissions has increased global temperatures, seriously threatening the living environment of mankind, so energy transformation is imminent [2][3]. In 2024, The United Nations pointed out the renewable energy is the cheapest option to generate electricity power. The cost of electricity generated from solar power dropped by 85% between 2010 and 2020. Affordable electricity from renewable sources could supply 65% of the world's total electricity by 2030. By 2050, it could decarbonize 90% of the power sector, significantly reducing carbon emissions and contributing to the mitigation of climate change. [4]. Figure 1.1 shows the proportion of global electricity generated by different energy sources between 2000 and 2023. It can be seen from the figure that the total global electricity generation has increased year by year from 2000 to 2023. As of 2023, renewable energy accounts for approximately 40% of the total electricity generation. However, the figure also shows that electricity generation from traditional fossil fuels is also rising year by year, indicating that the world has not yet broken its dependence on traditional fossil fuels. Figure 1.2 shows the proportion of electricity generated by different energy sources in Europe from 2000 to 2022. It can be seen that clean energy accounts for about 50% of all energy types used for power generation. However, over the past 20 years, there has been no significant change in the energy structure, and the use of traditional fossil fuels has not decreased noticeably [5]. So, the energy transition is urgent. Using wind power, solar energy and other

renewable energy to replace fossil energy is a common goal of mankind [6]. Although renewable energy generation in Europe has already surpassed that of traditional fossil fuels, it is still insufficient to eliminate reliance on them. While the development of new energy sources offers clear advantages, the initial investment in renewable power projects is often substantial. Projects like wind and solar power are highly dependent on natural conditions, making their energy output intermittent and challenging to predict. Moreover, the collection voltage of photovoltaic arrays is often lower than the grid voltage, complicating the process of integrating photovoltaic power into the grid

In the field of renewable energy power generation, compared with other power generation methods, solar energy has been vigorously developed due to its advantages such as low construction cost, simple laying, and low operating cost [7]. In the past decade, the power generation efficiency of solar power panels has been continuously improved, while the manufacturing cost has been greatly reduced. This has greatly reduced the cost of solar power generation, thus making up for the shortcomings of solar energy's greater dependence on the environment.



1. Watt-hour: A watt-hour is the energy delivered by one watt of power for one hour. Since one watt is equivalent to one joule per second, a watt-hour is equivalent to 3600 joules of energy. Metric prefixes are used for multiples of the unit, usually: - kilowatt-hours (kWh), or a thousand watt-hours. - Megawatt-hours (MWh), or a million watt-hours. - Gigawatt-hours (GWh), or a billion watt-hours. - Terawatt-hours (TWh), or a trillion watt-hours.

Fig 1.1 Distribution diagram of global power generation by different power generation methods from 2000 to 2023[8]

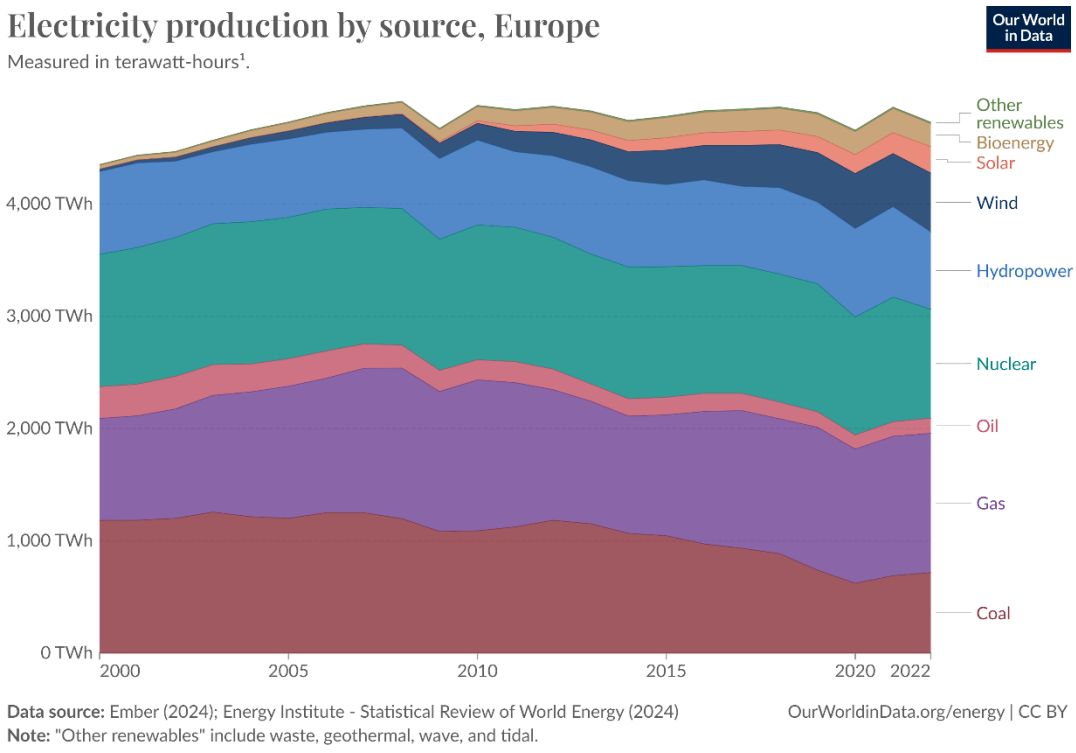


Fig 1.2 Distribution diagram of Europe power generation by different power generation methods from 2000 to 2022 [8]

The inverter is an important component of the photovoltaic grid-connected system, which plays the role of connecting the photovoltaic power generation array and the power grid. Usually, the transformer plays the role of current isolation between the solar power generation panel and the grid, and the DC-DC converter plays the role of balancing the voltage level between the photovoltaic panel and the grid [9][10]. However, due to the access of the transformer and DC-DC converter, the transmission efficiency of the system will be reduced [11]. The above-mentioned problems have been improved with the introduction of transformerless multilevel inverters [12][13][14][15][16].

1.2 Research gap and motivation

In recent years, a large number of scholars have participated in research on multi-level inverters. Research on multi-level inverters includes optimizing topology to obtain high-level output, but more level outputs often increase the use of switching devices [17]. The disadvantages are that it increases the manufacturing cost of the inverter and complicates the control logic of the inverter. In addition, more switching devices will also increase the loss of the inverter and reduce the transmission efficiency. So how to reasonably optimize the inverter topology is a challenge [18][19][20]. Research on inverter topologies with self-boosting capabilities has also received much attention, which helps to abandon the use of DC-DC converters in photovoltaic inverter systems. In addition, the self-boosting topology makes the inverter suitable for high-power applications. But the same disadvantage is that the number of DC supply and switching devices in the inverter will increase as the voltage gain increases [21]. Therefore, how to use fewer devices to obtain higher voltage gain is one of current research challenges. In addition, blindly increasing the voltage gain while ignoring the number of output levels will increase the voltage difference between each step of the output level and increase the harmonics of the output voltage. With the development of semiconductor technology, such as silicon carbide (SiC) and gallium nitride (GaN) devices, further research is needed on how to best utilize these advanced devices in multi-level inverter applications. The control of multi-level inverters is an important part of inverter research. Designing more advanced control strategies and algorithms to improve dynamic performance, reduce harmonics and improve reliability of multi-level inverters is also the main direction of current research. For switched capacitor multilevel inverters, in addition to the above research challenges, it also includes realizing self-balancing of capacitor voltage by designing control strategies and rationalizing the capacity and layout of capacitors.

Traditional multilevel inverter structures face the challenge of a significant increase in the number of components as the number of output voltage levels increases [22].

Additionally, these inverter designs usually lack voltage self-boosting capability. As a result, a boost converter is commonly required at the input side to raise the input voltage to the desired level [23]. However, this additional boost converter introduces extra power losses, which reduces the overall system efficiency.

Designing an inverter with self-boosting capability that can achieve high voltage gain (boost) and generate a higher number of output voltage levels while using fewer switching components would greatly improve energy conversion efficiency and power quality [24]. Switched capacitor inverters meet these requirements by utilizing the charging and discharging processes of capacitors to achieve self-boosting functionality. The structure and control logic of inverters are designed specifically around these capacitor operations, effectively reducing the number of switching components required.

Since the boost converter structure that uses magnetic components (inductors) to boost voltage has been eliminated in practical applications, the overall volume and weight of capacitors are smaller than those of inductors in applications with the same power level. Therefore, SCMLIs are efficient, compact, and modular, making them suitable for microgrids and off-grid power systems, vehicle-mounted inverter systems and motor drives.

1.3 Scope of the project

Based on the research challenges on multilevel inverter described above. This thesis proposed two switched capacitor multilevel inverter. The first one is 13-level switched capacitor inverter, and it has 3 times of voltage gain. The second is 17-level switched capacitor inverter and it has 4 times of voltage gain. They use fewer switching devices and are fully symmetrical structures, which helps simplify the control logic. The benefit of the optimized topology is that the voltage difference of each level in the output voltage of the two proposed topologies is 1/2 of that of others, which significantly improves the waveform quality and reduces the harmonic content. In addition, it is

worth noting that the two topologies proposed use single power supply, which fundamentally avoids the occurrence of voltage imbalance. And through the control logic, the self-balancing of the capacitor is achieved.

The control strategies for the two proposed topologies are designed in this thesis, and using MATLAB/Simulink to conduct simulation experiments, and finally produced a prototype of the 17-level switched capacitor inverter. In the hardware experiment part, FPGA (field-programmable gate array) was used to study the algorithm for controlling the designed inverter prototype. In addition, the gate driving circuit is also studied. After completing these preparatory experiments, all parts were combined into a test bench, experiments were conducted on the performance of the proposed inverter, and the experimental results were collected.

1.4 Contribution

The contributions of this thesis are described following:

(a) A novel 13-level switched capacitor inverter is proposed in this thesis.
(b) A novel 17-level switched capacitor inverter is proposed in this thesis.
(c) A combination idea based on switched capacitor structure and a parallel/series connected switched capacitor unit are proposed. This kind of unit can be used in different switched capacitor inverter topologies to obtain high output voltage gain.
(d) The control strategy based on the multicarrier PWM technology is simplified through the design of topology.

1.5 Thesis summary

This thesis consists of 6 chapters. Chapter 1 explains the background of the research and describes the research challenges of multi-level inverters. Chapter 2 begins with a brief description of the development of multi-level inverters, followed by an introduction to the operating principles, advantages and disadvantages of a series of

traditional multilevel inverters. Finally, a comprehensive review of the topologies proposed in previous papers from different researchers is conducted. Chapter 3 presents the modulation strategies of the multilevel inverter and describes the principle and then using MATLAB/Simulink to build the models to fully understand them. The second part of this chapter is the calculation method of the capacitance of the capacitors utilized in the switched capacitor inverter topology. Chapter 4 proposes two novel switched capacitor inverter topologies and describes the operation principle. Following that, the comparative study of simulation results is analyzed comprehensively. Chapter 5 shows the detailed prototype construction and hardware experiment of the proposed 17-level switched capacitor inverter, and the experiment results are explained at the end. Chapter 6 concludes the research of this thesis and presents the plan of future work.

Chapter 2: Review of Multilevel inverters

2.1 Introduction

With the current technical level, the voltage withstands capability of a single power electronic device is limited. To realize a high-power converter, it is necessary to resort to series connection of switching devices or multi-level technology. Although the inverter using the switch series technology has a simple structure, it will bring about problems such as static voltage equalization and dynamic voltage equalization of the switching device [25]. The multi-level inverter topology is widely used in medium and high-voltage high-power systems because it can output high voltage value and increase the number of the voltage level without increasing the withstand voltage rating of the semiconductor switching devices [26]. As the number of output voltage levels increases, the output voltage is closer to a sinusoidal waveform, which can significantly reduce THD to improve power quality [27]. Common multi-level topologies include NPC, FC, and CHB. The working voltage of each diode in the NPC multi-level inverter topology is half of the DC voltage source, so it can be directly applied to systems with medium and high voltage systems. However, in a three-phase NPC inverter, if the output level of any two phases is 0, the load current will flow into or out of the neutral point, which will increase or decrease the neutral point voltage, causing the voltage of the two capacitors to be different and affecting the quality of the output voltage. Therefore, it is necessary to consider the balance of capacitor voltage when designing NPC inverters [28]. Compared with NPC inverters, FC inverters have no diodes, thus overcoming the shortcomings of NPC, but as the number of output voltage levels increases, the number of flying capacitors will increase, increasing the size of the inverter and cost. In addition, too many capacitors will lead to an increase in the inverter failure rate [29][30]. The CHB inverter is cascaded by H-bridge modules to achieve multi-level output voltage. Each module in the CHB inverter is powered by an independent voltage source, and each H-bridge module can generate voltage values in three states—V, 0, and V. The sum of the output voltage of each module constitutes the multi-level voltage output by the

inverter. Compared with the other two topological structures, CHB inverters do not have the problem of balancing capacitor voltage and have fewer power electronic devices [31]. The modular structure is convenient for manufacturing and maintenance and is beneficial to improve system stability [32]. As mentioned earlier, the higher the number of voltage levels, the more the waveform is close to sinusoidal, and the higher the power quality. Thanks to the modular structure, CHB inverters can more easily obtain higher levels of voltage by stacking H-bridge modules. However, the disadvantage of this topology is that a large number of isolated DC sources are required when outputting voltage with a high number of levels.

In recent years, in order to obtain higher quality power, the number of MLI levels has also increased, which has led to an increase in the number of power switches and dc voltage sources, which has reduced the conversion efficiency of the system, increased costs, and will also affect the power output of the system quality[33].The drawbacks of conventional MLI promote the development of hybrid multi-level inverter[34].
In this chapter, some structure of the multilevel inverters will be presented, and the advantages and disadvantages will be analyzed.

2.2.1 Diode-clamped multilevel inverters

Diode-clamped MLI is one of the earlier researched multilevel topology structures. This type of MLI applies only one DC supply and using the diodes to generate voltage levels and the topology of a standard three-level DCMLI is shown in Figure 2.1. Generally, the basic topology operates three voltage levels and the modulation strategy of this structure is concise, and for the fundamental switching frequency it has relatively high efficiency. For an N-level DCMLI, there will (N-1)*(N-2) diodes and (N-1) capacitors applied in the circuit. The balancing of the capacitor voltage is a challenging and the increased number of diodes used in the circuit make the system complicated [35][36].

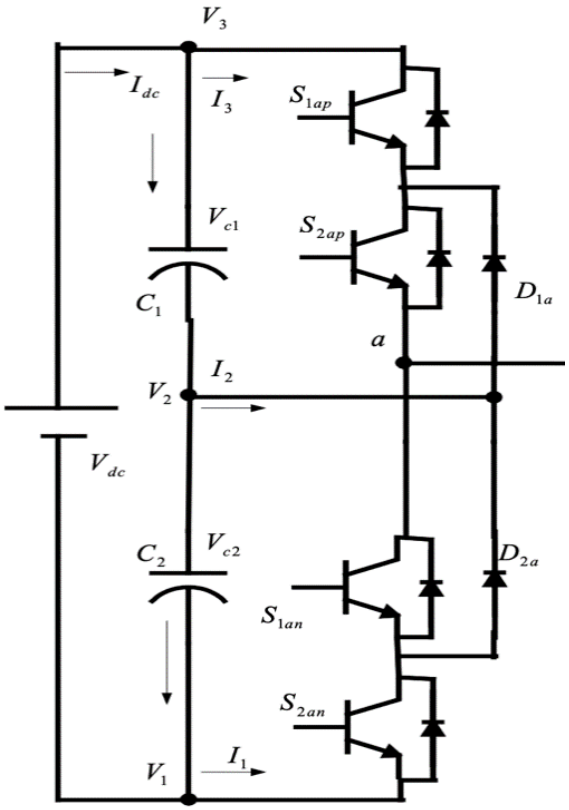


Fig 2.1 Topology of a standard three-level DCMLI

A five-level DCMLI is proposed in [37]. The topology designed in this paper is shown in Figure 2.2 and the standard five-level DCMLI is shown in Figure 2.3. Comparing these two topologies, it can be found the author replaced the three-level converter of the positive bus with the two-level converter to reduce the number of clamping diodes. But the voltage stress on the s_{p1} s_{n1} D_{p2} D_{n2} increased from Vdc to 2Vdc. The proposed topology maintains the same number of switching devices as the traditional topology but slightly increases the total voltage rating of the switching devices. Therefore, this limits the application of this topology in high-voltage, high-power systems. Additionally, the proposed topology may require more complex control strategies to ensure voltage balancing among the levels.

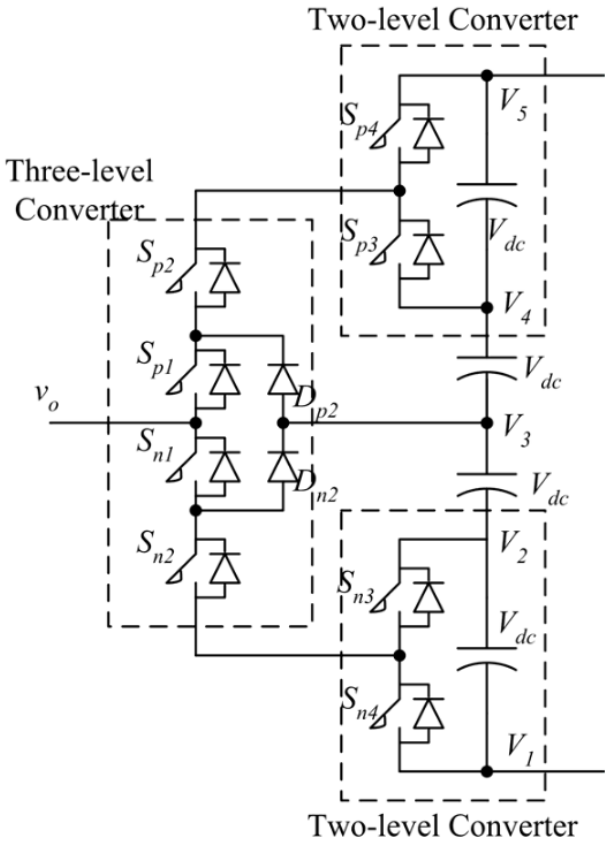


Fig 2.2 Topology of a reduced number of clamping diode five-level DCMLI

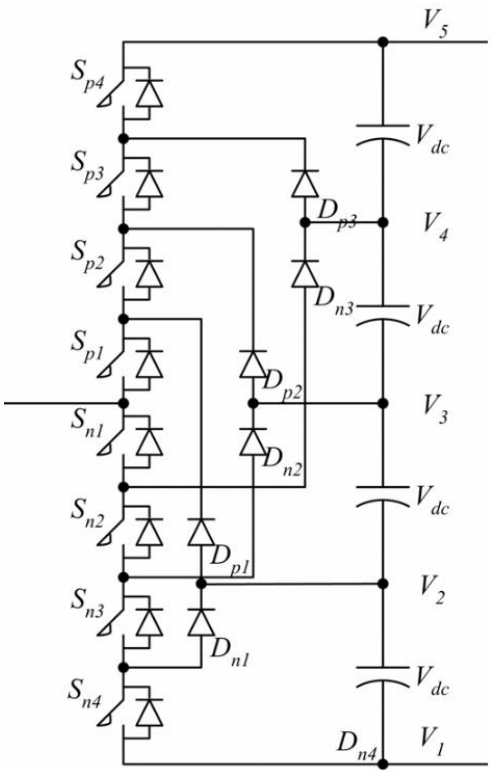


Fig 2.3 Topology of standard five-level DCMLI

In [38], a new DCMLI is proposed to eliminate the imbalance of the capacitor voltage, and it is shown in Figure 2.4. The inductors are inserted between the diodes and the main switches, and the voltage balance of the DC capacitors is guaranteed by controlling the opening time of the corresponding main switches in specific modes. This eliminates the need for parallel circuits on the DC side, resulting in fewer switches, diodes, and capacitors. The proposed topology reduces costs while maintaining suitability and applicability. The document also analyzes the voltage imbalance in conventional diode-clamped multilevel inverters and presents the compensation principle of the proposed topology.

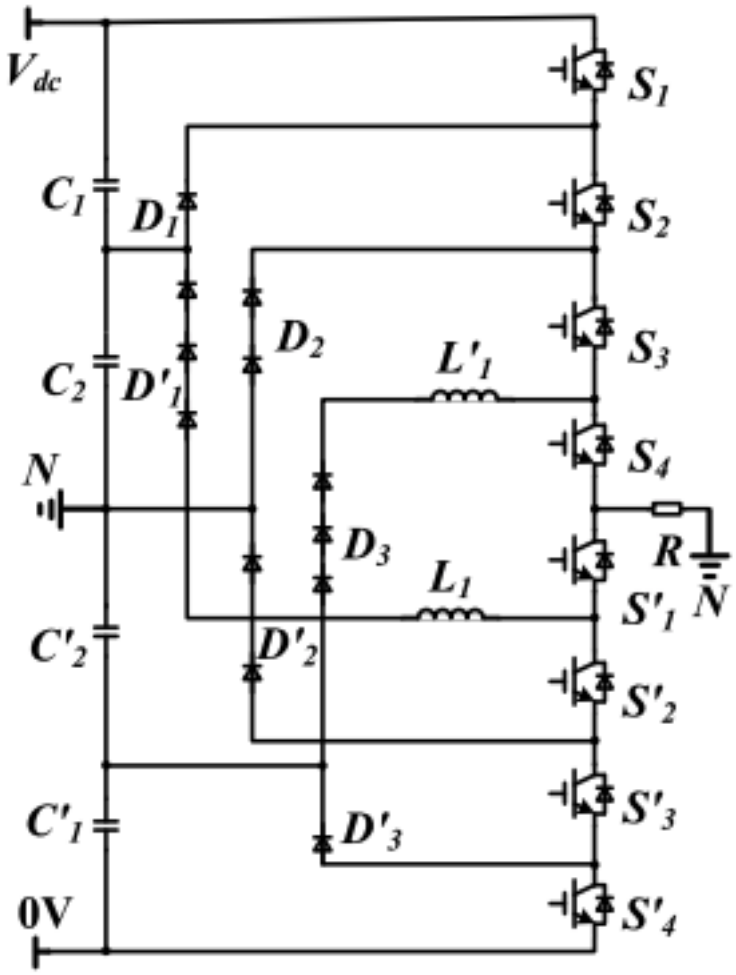


Fig 2.4 Topology of a novel DCMLI to eliminate the capacitor voltage imbalance

2.2.2 Flying-capacitor multilevel inverter

The flying capacitor multilevel inverter was first proposed by Meynard and Foch in 1992 [39]. Compared with the DCMLI, the capacitors were applied to instead the diode and the basic 3-level FCMLI is shown in Figure 2.5. There are three capacitors in the circuit and each capacitor is charged to 1/2Vdc, by different switching states the circuit can generate -1/2Vdc, 0, 1/2Vdc three voltage levels as follows:

When the circuit output -1/2Vdc, the switches S3 and S4 are in the ON state.

When the circuit output 1/2Vdc, the switches S1 and S2 are in the ON state.

There are two switching states to generate 0Vdc, the first one is switches S1 and S3 in the ON state, and the other one is switches S2 and S4 in the ON state.

Table 2.1 shows the switching states of different output voltages. It can be seen from the table, the switches S1 and S4 cannot be conducted at the same time. And the switches S1 and S3, switches S2 and S4 are conducted complementary. Moreover, there are two switching states to generate 0 voltage levels, and the different switch states to generate the same voltage is termed redundant switching states. And the redundant switching states can improve the reliability of the MLI. That is because when one switching state is failure and cannot generate the desired output level redundancy can be used to maintain the output. For FCMLI, the redundant switching state can be used to balance the capacitor voltage to ensure they can operate properly.

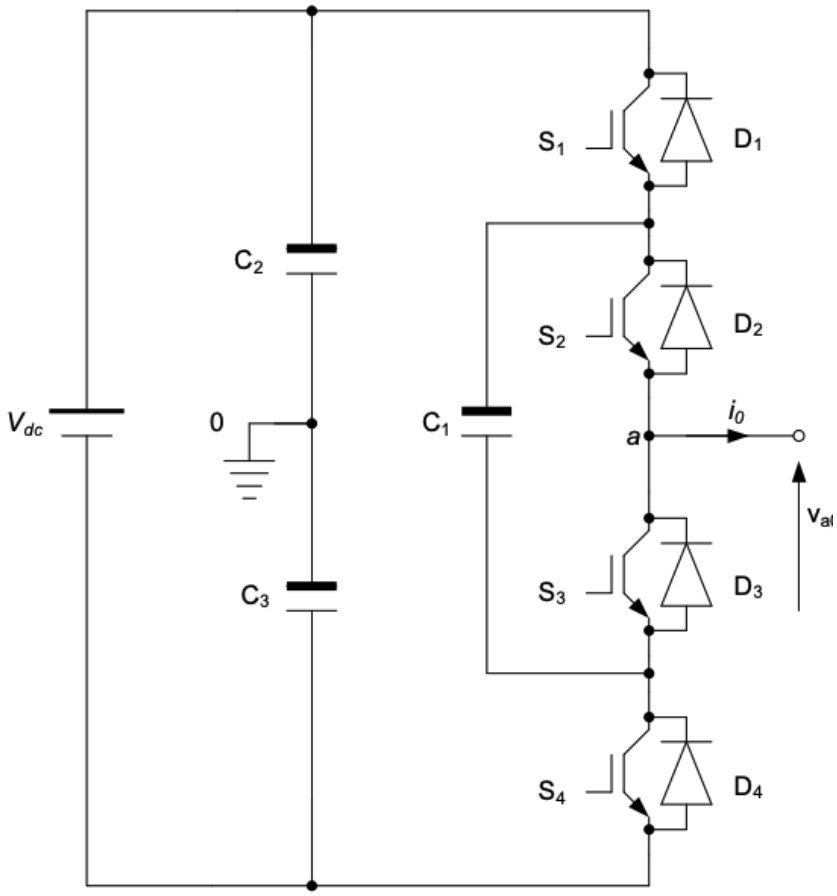


Fig 2.5 Topology of a three-level FCMLI

Vo	S1	S2	S3	S4
+1/2Vdc	1	1	0	0
0	1	0	1	0
0	0	1	0	1
-1/2Vdc	0	0	1	1

Table 2.1 Switching states of a three-level flying capacitor inverter

The redundant switching state will become apparent in FCMLI topologies that output more voltage levels. A standard five-level FCMLI is shown in Figure 2.6, there are 4 dc link capacitors and 6 clamping capacitors, the switching states are followed:

(1) When output 1/4Vdc, switches S1, S2, S3 and S1' are in the ON state, or S2, S3, S4 and S4' are in the ON state, or S1, S2, S4 and S2' are in the ON state.

(2) When output 1/2 Vdc, switches S1 S2 S3 S4 are in the ON state.

(3) When output 0Vdc, switches S1, S2, S1'and S2' are in the ON state, or S3, S4, S3'

and S4’ are in the ON state, or S1, S3, S1’ and S3’ are in the ON state, or S1, S4, S2’, S3’ are in the ON state, or S2, S4, S2’ and S4’ are in the ON state, or S2, S3, S1’and S4’ are in the ON state.

(4) When output -1/2Vdc, switches S1’, S2’, S3’ and S4’ are in the ON state.

(5) When output -1/4Vdc, switches S1, S1’, S2’and S3’ are in the ON state, or switches S2’, S3’, S4’ and S4 are in the ON state, or S1’, S3’, S4 and S3 are in the ON state, or S1’, S2’, S4’ and S2 are in the ON state.

Table 2.2 summarises all the switching states of the 5-level FCMLI, and there are a lot of redundant states when the inverter output 1/4Vdc, 0Vdc and -1/4Vdc. The redundant states make the inverter output voltage and balancing dc link capacitor voltage more flexible. Nevertheless, there still needs a specific method to balance the clamping voltage of capacitors (flying capacitors). And for an N-level topology, the number of clamping capacitors used in the circuit is (N-1)(N-2)/2. Therefore, a large number of capacitors will be applied in high voltage level FCMLI topology. This will undoubtedly complicate the capacitor voltage balancing strategy and reduce the system reliability.

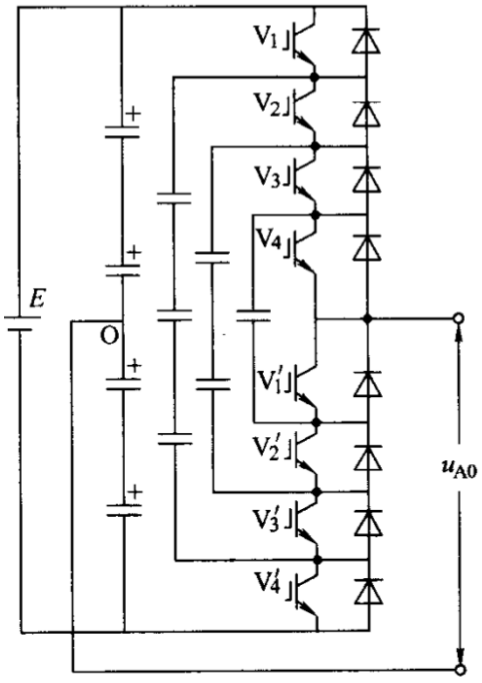


Fig 2.6 Topology of a five-level FCMLI

Vo	S1	S2	S3	S4	S1’	S2’	S3’	S4’
+1/2Vdc	1	1	1	1	0	0	0	0
+1/4Vdc	1	1	1	0	1	0	0	0
+1/4Vdc	0	1	1	1	0	0	0	1
+1/4Vdc	1	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
0	0	0	1	1	0	0	1	1
0	1	0	1	0	1	0	1	0
0	1	0	0	1	0	1	1	0
0	0	1	0	1	0	1	0	1
0	0	1	1	0	1	0	0	1
-1/2Vdc	0	0	0	0	1	1	1	1
-1/4Vdc	1	0	0	0	1	1	1	0
-1/4Vdc	0	0	0	1	0	1	1	1
-1/4Vdc	0	0	1	1	1	0	1	0
-1/4Vdc	0	1	0	0	1	1	0	1

Table 2.2 Switching states of a 5-level FCMLI

There are some new topology and balancing strategy proposed to eliminate the drawbacks referred above. In[40], a carrier-based PWM method is proposed by the author to balance the capacitor voltage. By utilizing the new carriers and the leg voltage redundancy, the average capacitor voltage change can be control to 0 during a specific period. The simulation results from this paper shows the new modulation method have a better harmonics performance than phase shifted PWM and also achieves better capacitor voltage balance. The conventional FCMLI is a kind of step-down inverter, in order to adapt to some circumstances, transformers are necessary. For example, in the grid-connection generation system using the FCMLIs, the generated voltage from the PV panels is usually smaller than the grid voltage, so there is necessary a boost module applied to the system [42][42]. In [43], a novel five-level inverter is proposed, and the topology of the single phase is shown in Figure 2.7. The topology is obtained by cascading two FC module and has an ability to boost the output to two times of the DC source. In addition, the number of capacitors utilized in this topology is fewer than the

conventional FCMLI with the same output voltage level. And the most significant feature is that the proposed topology has the capability to self-balance the capacitor voltage. In addition to the topology discussed above, a 13-level FCMLI proposed in [44] also has the capability to self-balancing and voltage boosting. And it can be seen from Figure 2.8, there are 2 DC voltage source and 4 capacitors applied in the circuit to obtain 3 times voltage boost.

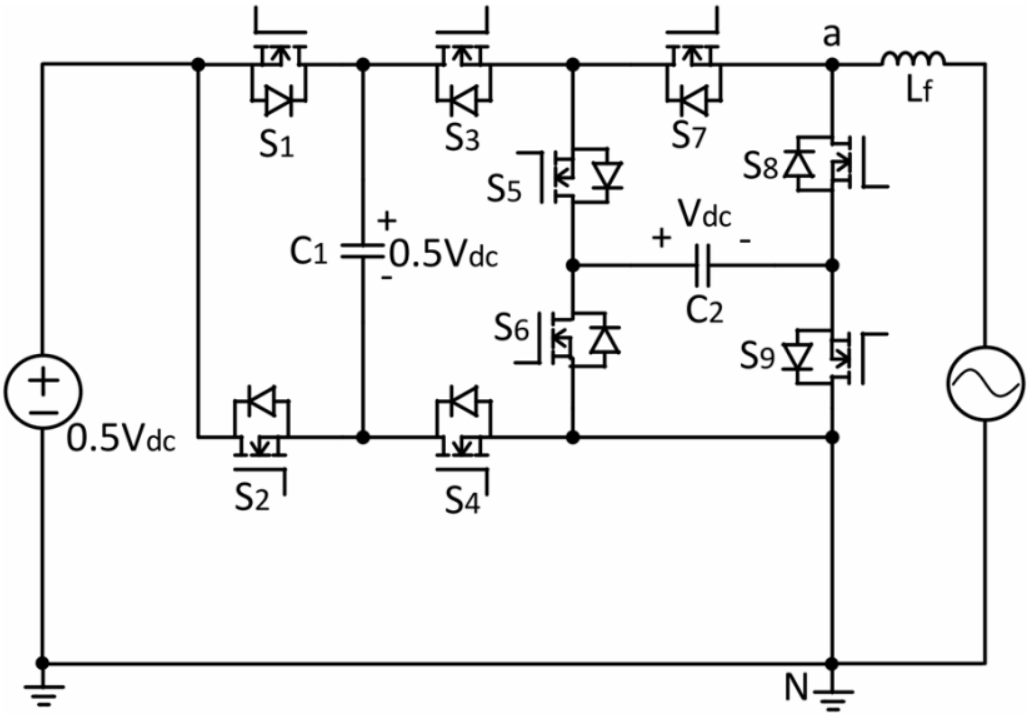


Fig 2.7 Topology of a novel five-level inverter proposed

2.2.3 Cascaded Multilevel inverter

The basic structure of DCMLI and FCMLI have the same feature of utilizing one DC supply and multiple capacitors connected in series to divide the DC voltage. The advantage of that is the voltage stress between the switches are equal to one of the capacitor voltages. This allows the inverter to output a high voltage while ensuring a low voltage stress between the switches [45]. But without any control, the capacitor voltage is hard to be balanced. Cascaded multilevel inverter is formed by cascading multiple modules with independent DC supply, so there is no capacitor balancing issue. The cascaded H-bridge multilevel inverter is the simplest and widely used topology,

especially for high power application [46]. That is because the CHB multilevel inverter can be effectively extended to a high output voltage and a large number of voltage level by cascading a corresponding number of H-bridge [47]. The topology shown in Figure 2.8 is a three-level H-bridge inverter and it is the basic module of the cascaded H-bridge multilevel inverter. When the switches S1 and S2 are conducted the output voltage is E. When the switches S3 and S4 are conducted, the output voltage is -E, when the switches S2 and S3, or S1 and S4 are conducted, the output voltage is 0.

A 5-level CBMLI is derived by cascading two H-bridge modules and the output voltage is from -2E to 2E. The topology is shown in figure 2.9 and the switching states are shown in Table2.3.

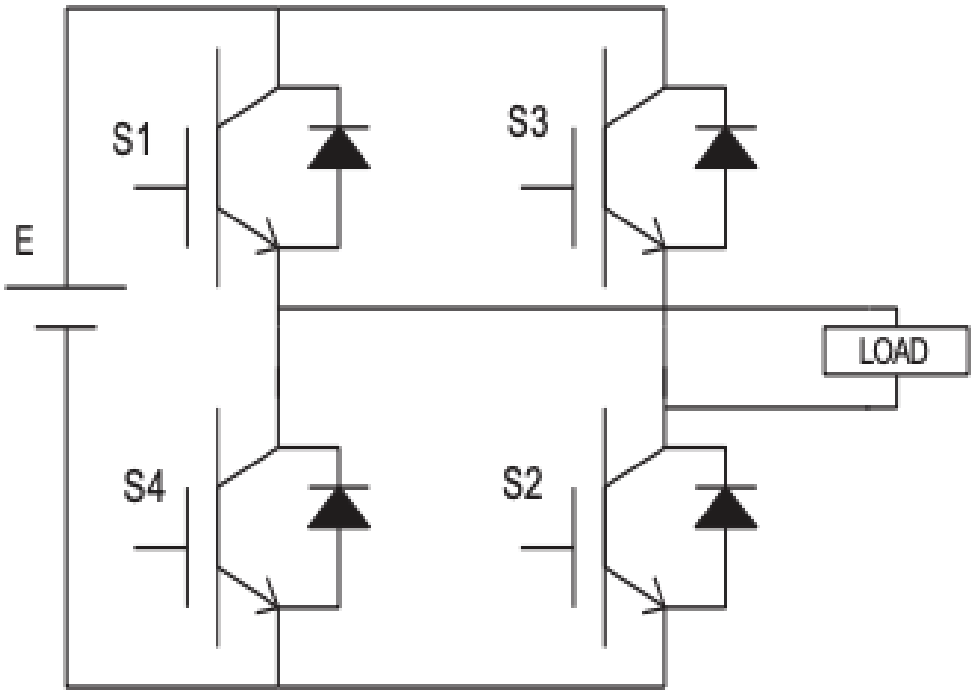


Fig 2.8 topology of a three-level H-bridge inverter

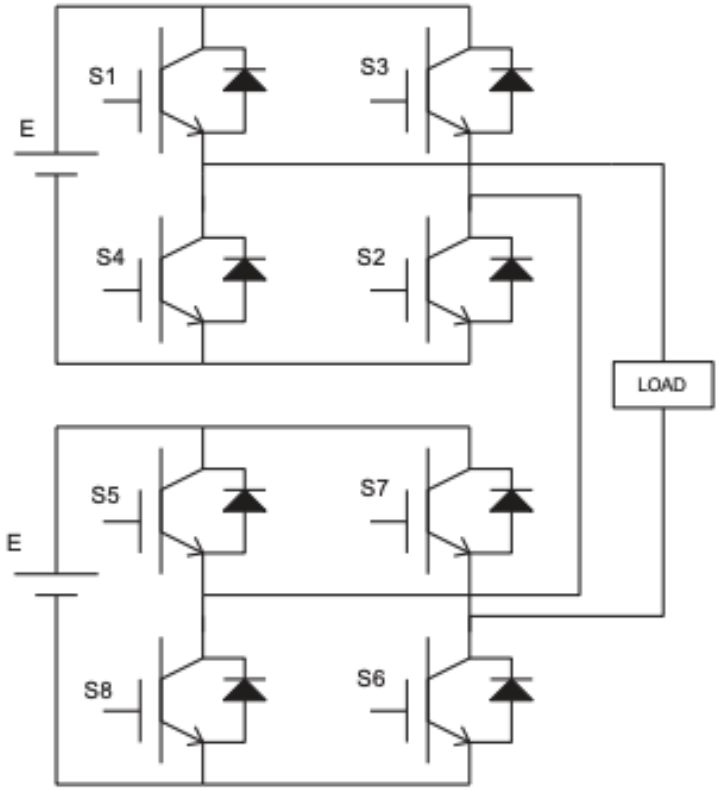


Fig 2.9 Topology of a cascade five-level H-bridge inverter

Output Voltage	S1	S2	S3	S4	S5	S6	S7	S8
+E	1	1	0	0	1	0	1	0
+2E	1	1	0	0	1	1	0	0
0	1	0	1	0	1	0	1	0
-2E	0	0	1	1	0	0	1	1
-E	0	1	0	1	0	0	1	1

Table 2.3 Switching state of the cascaded five-level H-bridge inverter

Each H-bridge module of the 5-level CHB inverter discussed above has the same value of DC supply, so this kind of topology named symmetric cascaded H-bridge inverter. But for the high-power application, it is the trend that the high voltage output of the inverter with minimum number of switches. That is because the fewer number of switches applied in the circuit, the lower switching loss generated and the higher efficiency the inverter obtained.

Therefore, using different value of DC supply is an effective way to increase the output voltage and voltage value. This kind of layout named asymmetric CHBMLI [48][49].

There are two methods to arrange the value of DC supply for different H-bridge modules. For an ACHBMLI with two H-bridge modules, the value of one DC supply is E and the value of the other module is 2E. This kind of DC supply arrangement named binary method. Similarly, if the DC supply of one module is E and the other is 3E, this arrangement names ternary method. For the extension of the ACHBMLI, the ratio of DC supply values of binary method is 1:2:4:..:2^{N-1} and the ratio for the ternary method is 1:3:9:...:3^{N-1}. Therefore, the maximum output voltage and the output voltage level of the binary ACHBMLIs can be expressed by $2^N - 1\ V_{dc}$ and $2^{N+1} - 1$ respectively. In the same way, the maximum output voltage and the output level of the ternary ACHBMLIs can be obtained by $\frac{3^N-1}{2} V_{dc}$ and 3^N respectively [50]. Among them, N represents the number of H-bridge modules in the circuit.

The above is a detailed analysis of the topology of the H-bridge circuit acting as a cascade module. In addition, in order to further reduce the use of switching devices, some scholars have explored the cascaded multilevel inverters applied to other modules. Figure 2.10 is a hybrid 5-level cascaded inverter designed in [51]. Knowing from figure 2.10, the topology is obtained by cascading a H-bridge inverter and one leg of a three-phase two-level inverter. A capacitor replaces the DC voltage source of the h-bridge cell to reduce the number of DC supply utilized in the circuit and operation principle of capacitor is shown in Table2.4. Although the application of the capacitor can reduce the number of DC supply, the discharge of the capacitor is an attenuation process. To maintain the stability of the electric energy, a capacitor with an enormous capacitance value is required which increases the cost. In addition, the lower safety of the capacitor reduces the reliability of the system.

The new module shown in figure 2.11 is discussed in [52]. The module proposed by the author is also intended to use fewer switching devices to obtain higher output voltage and more output levels. And the author simplifies the drive circuit by using a large number of bidirectional MOSFETs. In addition, the author also conducted a detailed study on the DC supply arrangements of the binary method and ternary method of the

proposed module. The 49-level inverter composed of three modules in cascade is shown in figure 2.12, and comparative study with traditional cascaded inverters was conducted, and the results shows that the components utilized by the proposed inverter is the least.

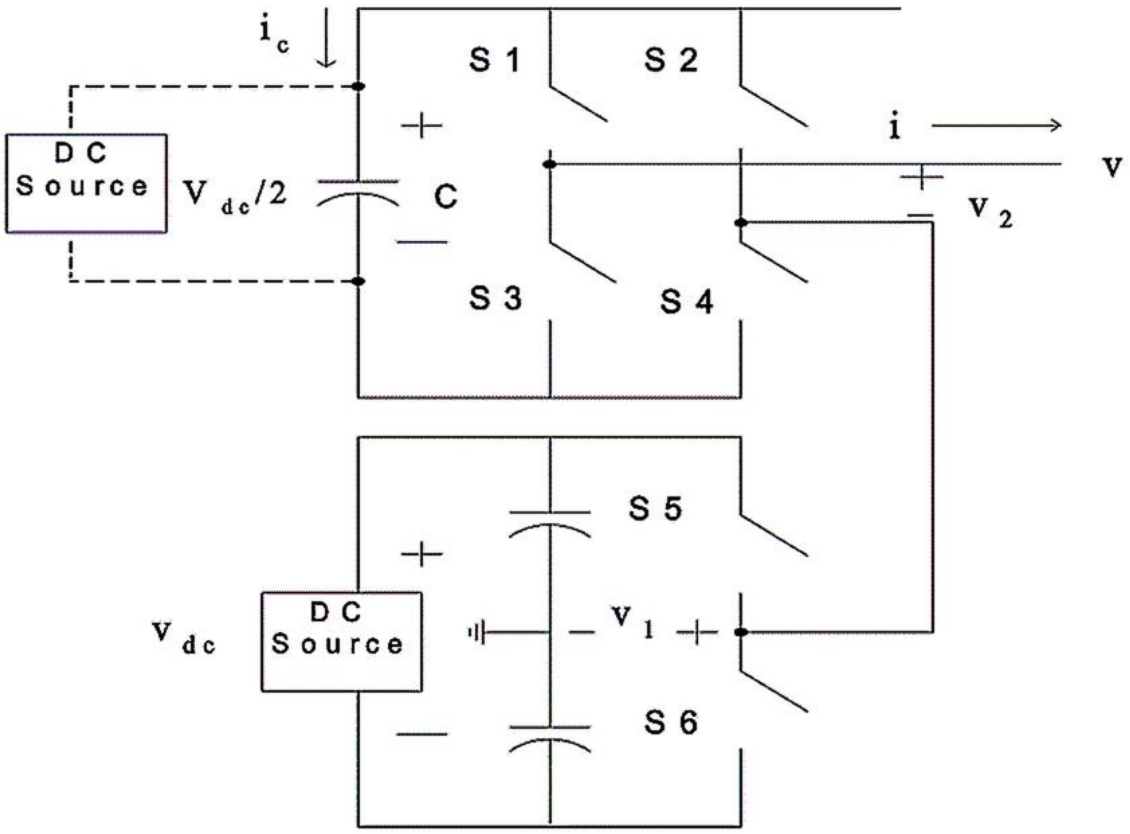


Fig 2.10 Topology of a hybrid 5-level cascaded inverter

Output voltage	V1	V2	C
Vdc	Vdc/2	Vdc/2	Discharging
Vdc/2	Vdc/2	0	Do not work
0	Vdc/2	-Vdc/2	Charging
0	-Vdc/2	Vdc/2	Discharging
-Vdc/2	-Vdc/2	0	Do not work
-Vdc	-Vdc/2	-Vdc/2	Charging
Vdc	Vdc/2	Vdc/2	Charging
Vdc/2	Vdc/2	0	Do not work
0	Vdc/2	-Vdc/2	Discharging
0	-Vdc/2	Vdc/2	Charging
-Vdc/2	-Vdc/2	0	Do not work
-Vdc	-Vdc/2	-Vdc/2	Discharging

Table 2.4 Operation principles of topology proposed in [51]

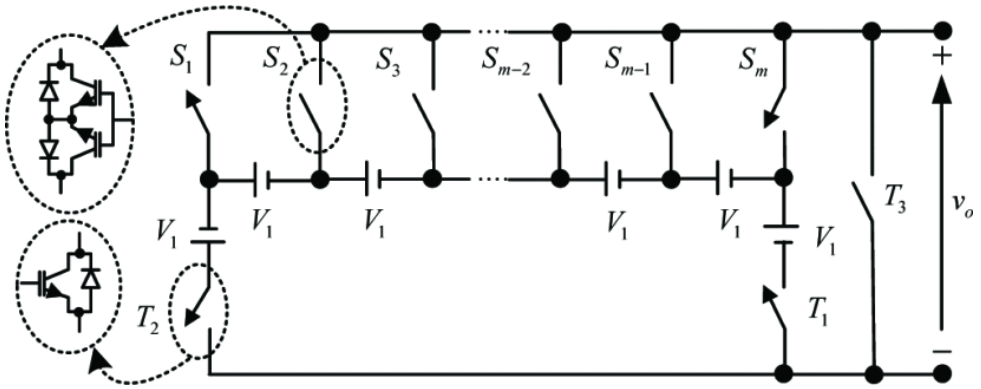


Fig2.11 Basic cascaded unit proposed in [52]

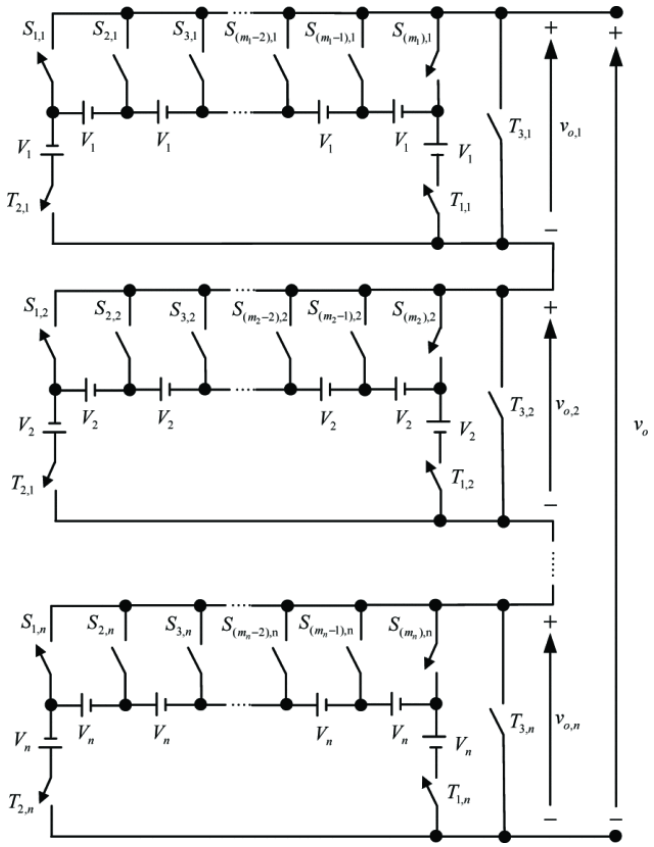


Fig 2.12 Cascaded multilevel inverter proposed in [52]

2.2.4 Switched capacitor multilevel inverter

The cascaded multilevel inverter described above has the capability to output a high power when a number of modules are cascaded. However, the apparent disadvantage is several DC supplies are applied into the circuit [53][54][55]. This will limit its utilization in single power supply applications, such as PV generation, fuel cells, etc. [56][57]. Moreover, traditional multi-level inverters do not have the ability to self-boost, so in the field of power generation, especially in the field of solar power generation, a transformer is required to match the inverter output voltage with the grid-connected voltage [58].

Due to the many disadvantages of conventional multilevel inverters, new MLI topologies have been proposed in recent years. Among them, the switching capacitor MLI has great research values because the features of reduced components numbers, simplified control scheme, self-balanced capacitor voltage and step-up system [59].

The switched capacitor inverter was originally reported by On-cheong Mak and Adrian Ioinovici in 1998 [60] and has been widely studied in the last ten years. The basic principle of the switched capacitor inverter is to use the capacitor in the circuit to reasonably arrange the charge and discharge time and the charge and discharge circuit by controlling the logical conduction of the switch to output the desired voltage value and level. The figure 2.13 below shows the basic unit circuit of a switched capacitor. The circuit highlighted by blue line is the charging circuit and the red line represents the discharging circuit. Therefore, when the isolated voltage source and the capacitor are connected in series, the capacitor is charged, and when the voltage source and the capacitor are connected in parallel, the capacitor is discharged by connecting one or more basic units and designing a polarity shift circuit, a basic switched capacitor inverter structure can be obtained. The topology derived by connecting the basic SC-unit is shown in figure2.14 [61]. It can be seen the topology can be easily extended by connecting more SC-unit and polarity shift is operated by the H-bridge. The topology proposed in [62], after substituting the DC supply with capacitors, can be seen as an optimization of the topology illustrated in figure 2.14. The updated configuration is presented in figure 2.15. By cascading the switched capacitor circuit with a full-bridge circuit, this design achieves a higher output voltage and a greater number of voltage levels, accompanied by a reduced dv/dt. This improvement theoretically results in lower electromagnetic interference (EMI) and reduced harmonic distortion.

Furthermore, the switched capacitor circuit depicted in figure 2.16 has been derived from modifications made to the topology shown in figure 2.13 [63].

The proposed switched circuit uses fewer switches to control the charging and discharging of two capacitors. And the same, the H-bridge is utilized to polarity shift. It can be found from Table 2.5, when there is one SC-unit connected in the circuit, the proposed topology has two times of voltage boost with 9-level output.

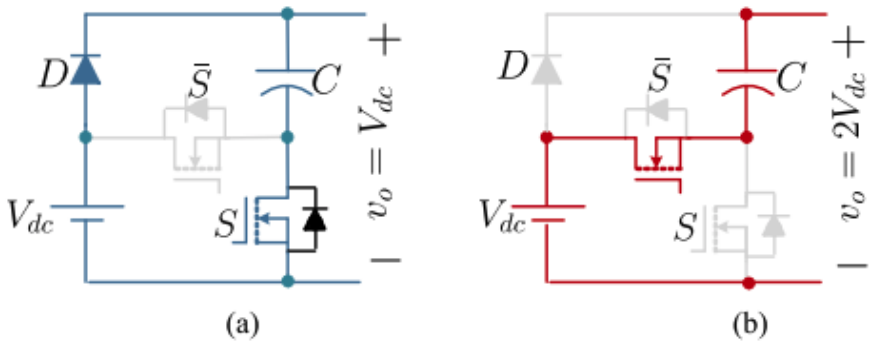


Fig 2.13 Basic unit circuit of a switched capacitor

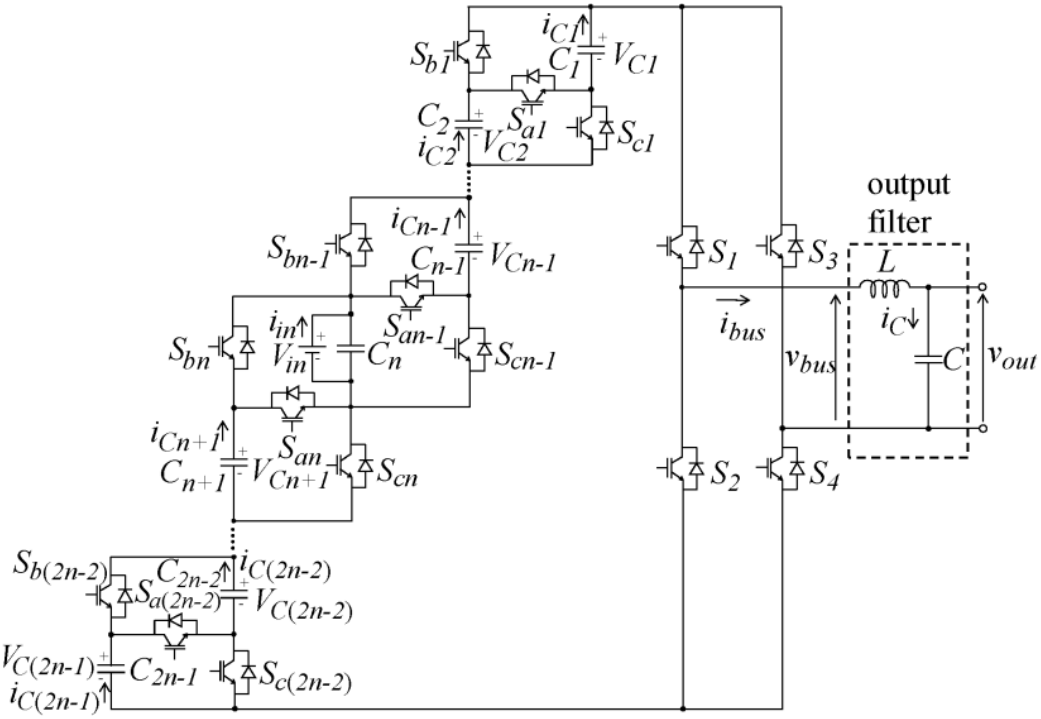


Fig 2.14 Topology by connecting several basic units

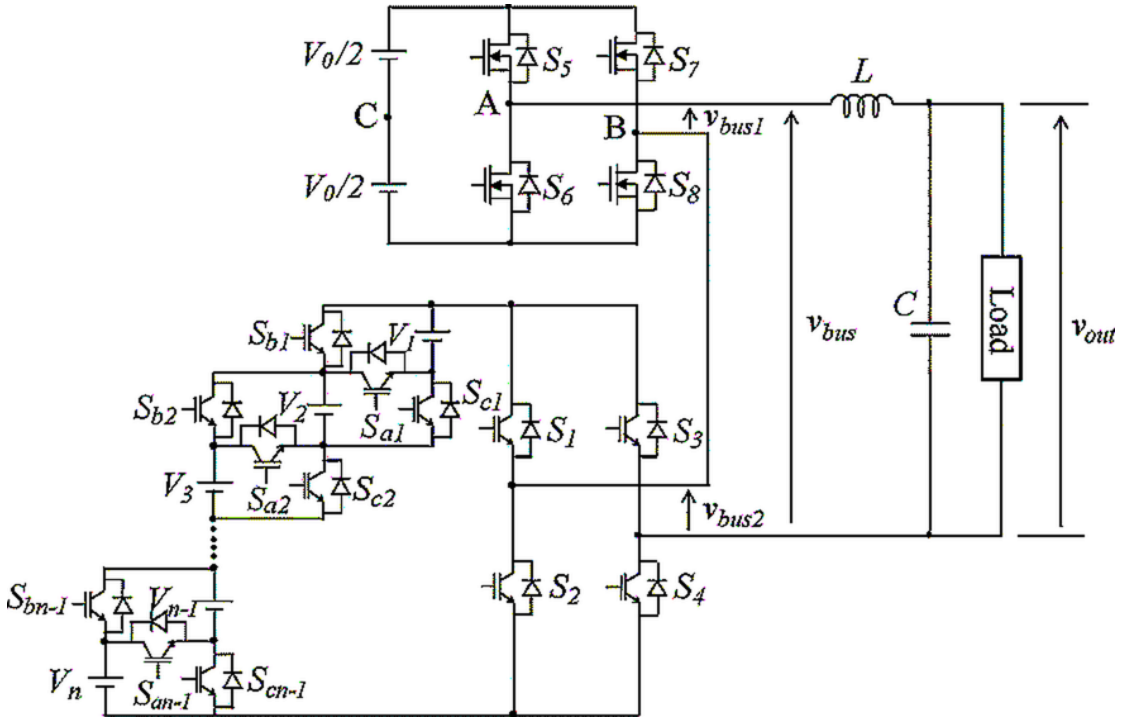


Fig 2.15 Cascaded switched capacitor multilevel inverter with the basic unit

Voltage levels	Switches in HBC				Switches in DSCC					Diodes		Capacitors	
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	D_1	D_2	C_1	C_2
$2V_{dc}$	1	0	0	1	1	1	1	0	0	0	0	D	D
$3V_{dc}/2$	1	0	0	1	1	1	0	0	1	0	1	D	D
V_{dc}	1	0	0	1	1	0	0	1	0	1	0	C	C
$V_{dc}/2$	1	0	0	1	0	0	0	1	1	0	1	D	D
0	0	1	0	1	0	0	0	1	1	0	0	-	-
$-V_{dc}/2$	0	1	1	0	0	0	0	1	1	0	1	D	D
$-V_{dc}$	0	1	1	0	1	0	0	1	0	1	0	C	C
$-3V_{dc}/2$	0	1	1	0	1	1	0	0	1	0	1	D	D
$-2V_{dc}$	0	1	1	0	1	1	1	0	0	0	0	D	D

Table 2.5 Operation principle of the 9-level switched capacitor inverter

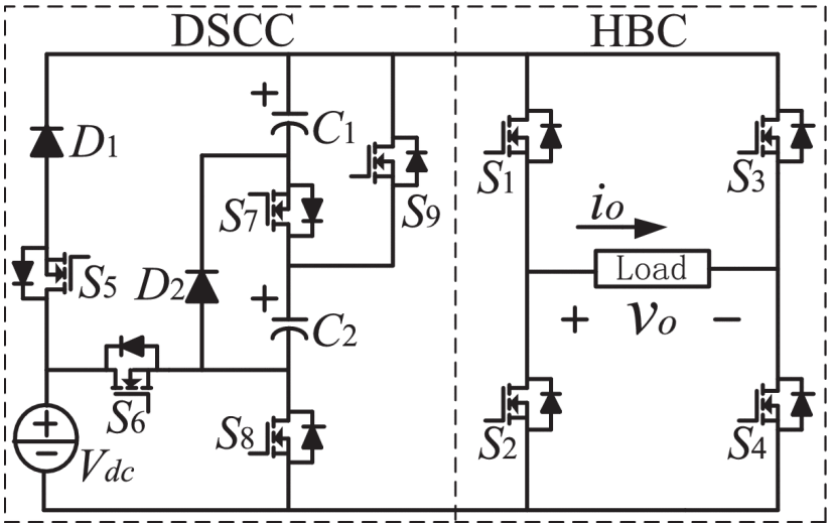


Fig 2.16 Nine-level switched capacitor inverter with H-bridge

However, the switched capacitor MLI mentioned above uses an H-bridge for the polarity shift of the output voltage, and the voltage stress on switches of the H-bridge is several times that of the DC voltage source. So, avoiding using H-bridge can minimize the switching loss and voltage stress across the semiconductor components.

The SCMLI without H-bridge topology proposed in [64] is shown in figure 2.17. The mentioned topology can generate bipolar output voltage without an H-bridge and the amplitude is two times to the DC source.

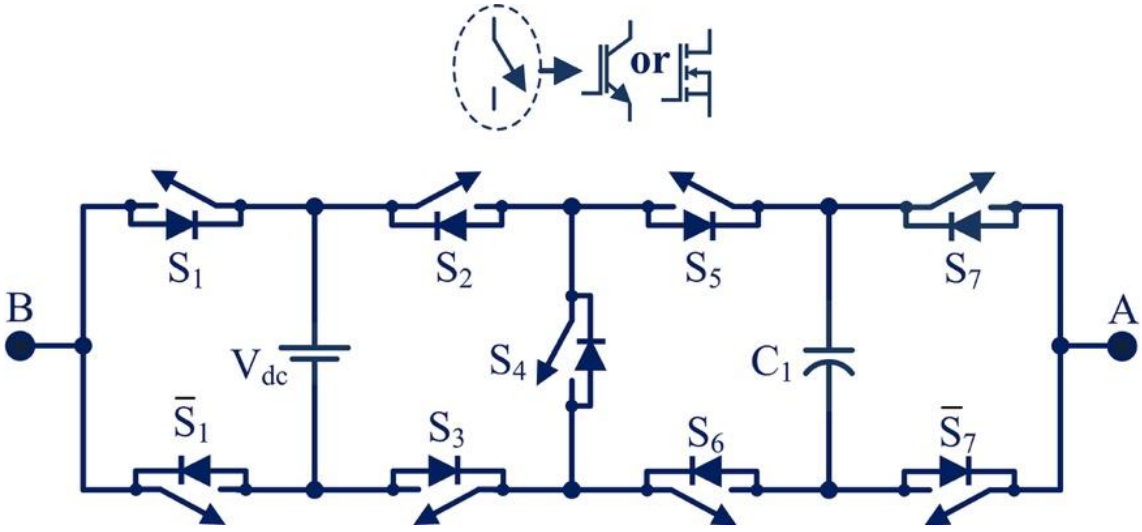


Fig 2.17 Switched capacitor multilevel inverter without H-bridge

2.1 Chapter conclusion

In this chapter, a comprehensive review and discussion of various typical multilevel inverter types are conducted. Traditional structures include the diode-clamped multilevel inverter, flying capacitor multilevel inverter, cascaded inverter, switched capacitor inverter, and several hybrid multilevel inverters optimized for specific characteristics. The diode-clamped multilevel inverter achieves multilevel and sinusoidal outputs by using clamping diodes to clamp the capacitor voltage (connected in parallel with the input power source) to the output. This topology has a high voltage-handling capability since each switch only needs to withstand voltage stress of V_{dc}. However, as the number of output voltage levels increases, the number of diodes and capacitors required grows significantly, increasing the inverter's size and losses. Additionally, the capacitors at the output often face voltage imbalance issues, requiring extra voltage balancing strategies to maintain high-quality voltage outputs. The flying capacitor multilevel inverter generates multilevel outputs by controlling the charge and discharge processes of capacitors through switch combinations. The charge/discharge of flying capacitors effectively balances capacitor voltage, avoiding the imbalance issues seen in diode-clamped inverters. However, as the output voltage levels increase, the number of switches and capacitors in the circuit also rises, leading to larger system size and more complex control algorithms. The cascaded H-bridge multilevel inverter relies on the combination of four switches to achieve voltage level variation at the output. Its main advantage lies in the scalability, as higher voltage levels can be obtained by simply cascading multiple H-bridge units. The control algorithm is simple and logically robust. However, increasing the number of voltage levels also increases the number of switches required. Moreover, cascading multiple H-bridges necessitates the connection of multiple input voltage sources, and without proper balancing mechanisms, the quality of the output waveform may deteriorate significantly. The switched capacitor multilevel inverter achieves voltage boosting and multilevel output by controlling the charge and discharge of capacitors. The switches in the circuit are

designed to facilitate efficient capacitor charge/discharge, ensuring self-balancing of capacitor voltage and stable, high-quality output waveforms. This structure features high voltage levels and a reduced number of switching devices. However, due to the lack of a uniform configuration, designs by different researchers vary significantly. The primary challenges include achieving high voltage gain and a large number of voltage levels using fewer components. Additionally, the self-boosting characteristic of the switched capacitor inverter increases the voltage stress on the switches, necessitating circuit designs that minimize the number of switches operating under high voltage stress. In this chapter, it is observed that most researchers connect an H-bridge at the inverter's output to achieve polarity shifting. However, this approach subjects all four switches in the H-bridge to maximum voltage stress, which increases switching losses and reduces switch reliability. The primary research directions for switched capacitor multilevel inverters are summarized as follows: reducing the number of switching devices, minimizing the voltage stress on switches, increasing the number of output voltage levels, enhancing the voltage gain at the output, and achieving self-balancing of capacitor voltage.

Chapter 3: Methodology

3.1 Chapter introduction

This chapter presents the modulation strategies for multilevel inverters, including conventional sinusoidal pulse width modulation (SPWM) and multicarrier pulse width modulation (PWM). Since multicarrier PWM is a widely used technique for controlling switched capacitor multilevel inverters, the chapter focuses on its principles. MATLAB/Simulink is used to build multicarrier PWM models, demonstrating how to generate switching signals for the inverter by combining sine and triangular wave comparison signals. Additionally, the method of calculating capacitance values in switched capacitor multilevel inverters is also discussed in this chapter

3.2 Pulse-width modulation strategy (PWM)

PWM is a commonly used strategy to control the inverter to output voltages and currents especially the sinusoidal [65][66][67]. In PWM, the desired output waveform of system is the reference signal, and the wave that is modulated is the carrier wave. The reference signal of the SPWM is the sinusoidal wave and the triangle carrier wave is commonly utilized to compare with the reference wave to generate the modulating wave [68]. Furthermore, the SPWM can be classified as unipolar SPWM method and bipolar SPWM method due to the polarity of the output control signal [69]. Figure 3.1 shows a standard h-bridge inverter and the four IGBTs are controlled by the signal generated by SPWM strategy. Both the unipolar and bipolar method can be used to generate the control signal of the H-bridge inverter, and the detailed introduction will be illustrated as follows.

The switches in the same leg of the H-bridge inverter are conducted complementary. The state of Switches S1 and S2 can be controlled with the same gate signal. And similarly, the control signal of S3 and S4 is the same. Therefore, there are only two signals that will be considered when using the SPWM strategy [70]. It can be found in figure 3.2 there are two sinewaves used to be the reference signal and phase difference

of the two sinewaves is 180 degrees. when output the signal V_{g1} (gate signal of S1 and S2),the sinewave V_m will be compared with the carrier wave V_{cr}, and when the $V_m > V_{cr}$, the output signal controls the switches S1 and S2 operating at ON state, and other switches are OFF state. When output the signalV_{g3}(gate signal of S3 and S4), the sinewave V_{m-} will be compared with the carrier wave V_{cr}, and when the $V_{m-} > V_{cr}$, the output signal controls the switches S3 and S4 operating at ON state, and other switches are OFF state. When the Switches S1 and S2 are ON state, the output voltage of the H-bridge inverter is V_{AN}. And when the switches S3 and S4 are ON state, the output voltage of the H-bridge inverter is V_{BN}. The actual output voltage (V_{AB}) of the inverter is the vector superposition of the output voltages of the above two states, so the actual output voltage (V_{AB}) of the inverter is shown in figure 3.2. It can be seen from the output voltage, in the half cycle of the output voltage, there is only one jump from 0 to positive voltage or from 0 to negative voltage. That is to say, the voltage can only jump to one polarity in half a cycle, so this modulation method is called unipolar SPWM [71][72].

Different from the unipolar SPWM, the bipolar SPWM applies only one sinewave compared with carrier wave to generate the control signal of the switches and the waveforms are shown in figure 3.2. And it can be observed from this figure, the output voltage of the inverter has the positive and negative two polarities within the half cycle of the output voltage, so the modulation strategy is called bipolar SPWM [73][74].

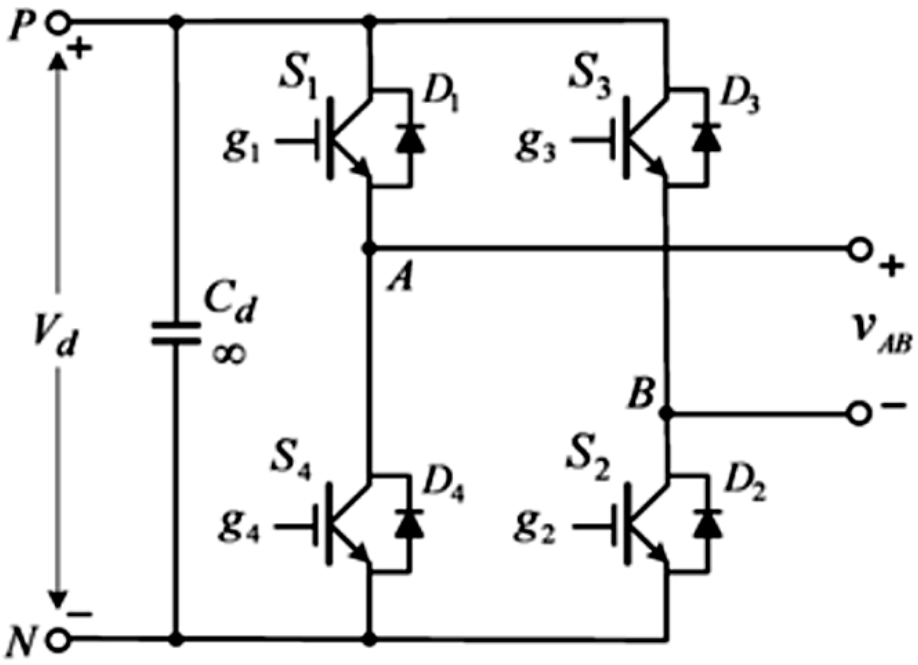


Fig 3.1 Standard H-bridge inverter

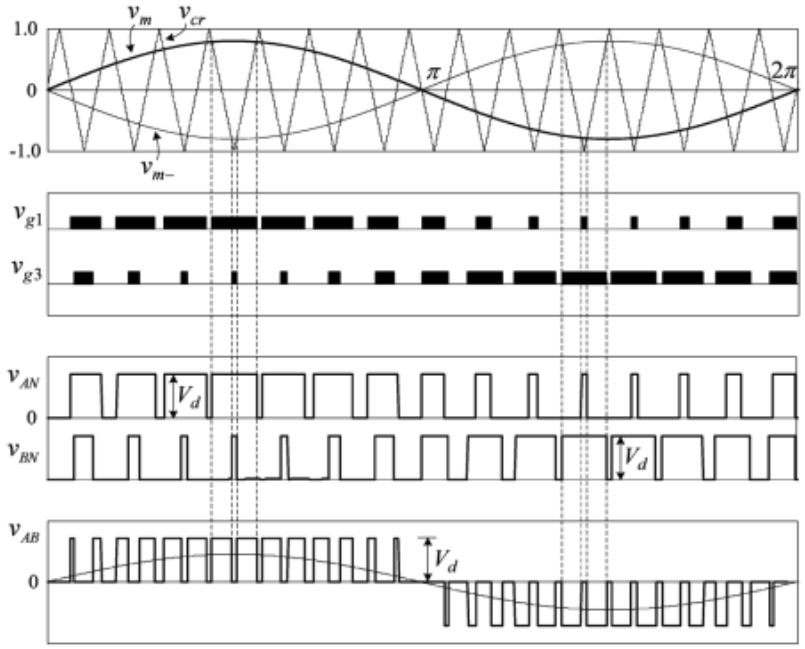


Fig 3.2 Waveforms of unipolar SPWM method

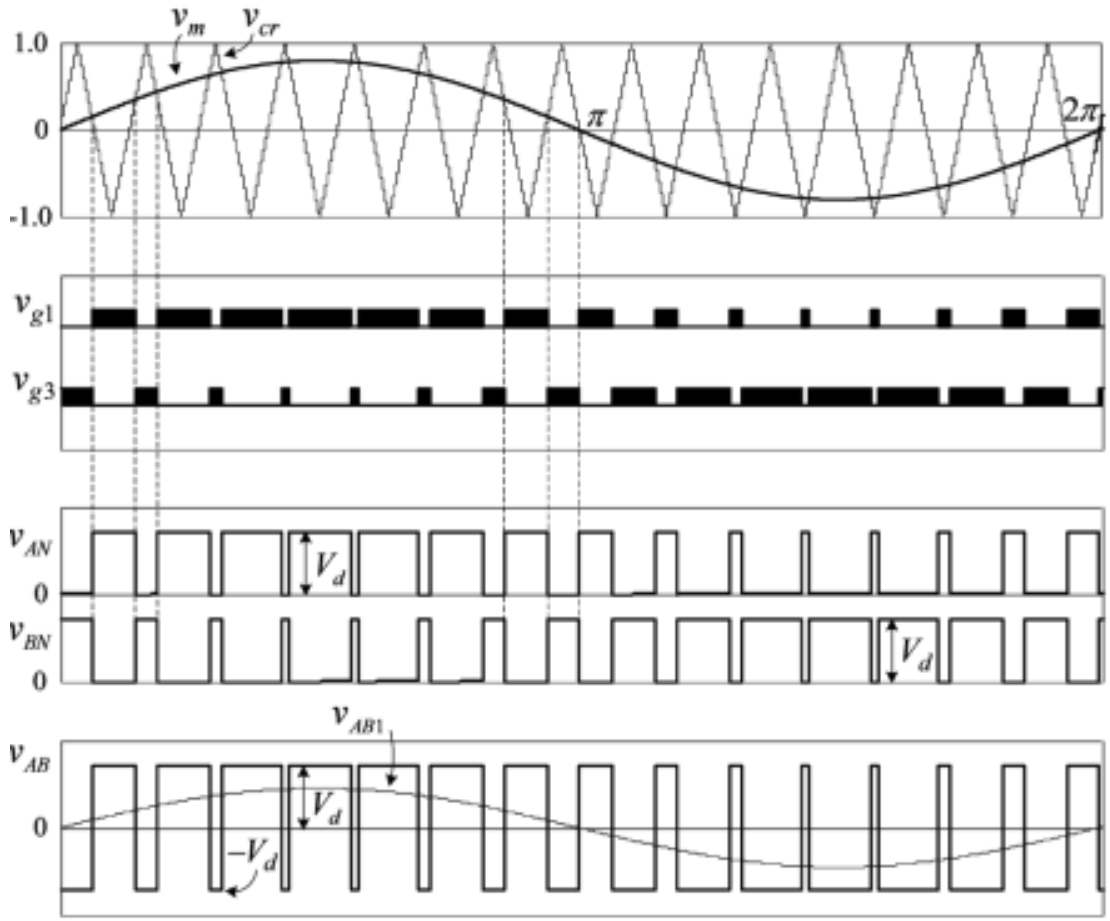


Fig 3.3 Waveforms of bipolar SPWM method

Another way to obtain the control signals using the unipolar SPWM strategy is apply only one sine wave to compare with two triangle carrier waves and the phase difference of the two carrier waves is 180° , the arrangement of waveforms is shown in figure 3.4.

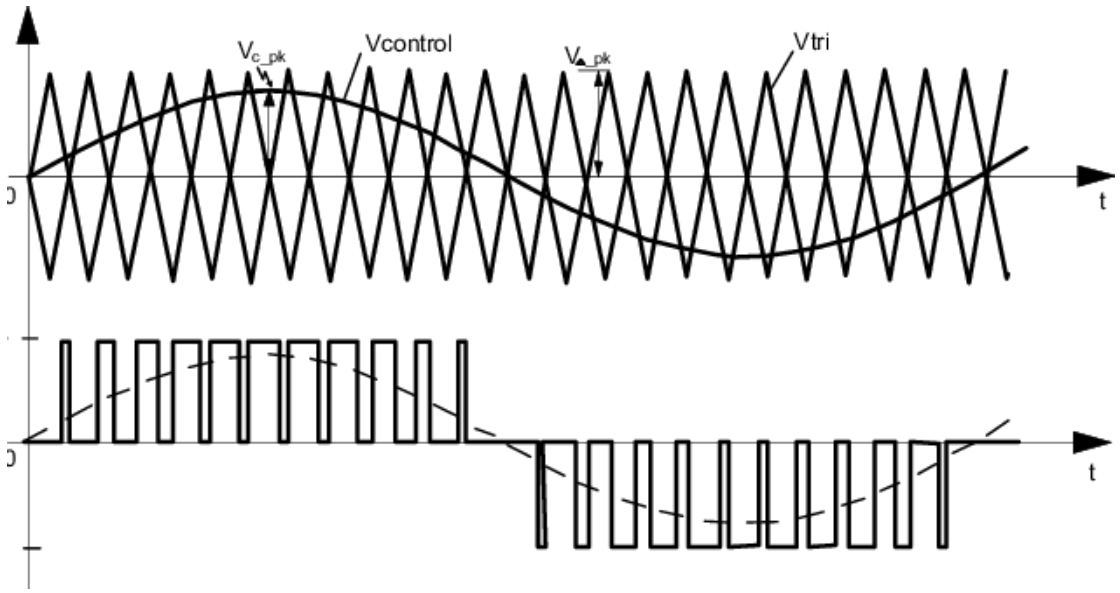


Fig 3.4 Waveforms of unipolar SPWM method

Comparing with the two SPWM modulating methods, the unipolar SPWM using two triangle carrier waves to generate the signal to control the H-bridge inverter output 3-level voltage, while the signal modulated by the bipolar SPWM can only control the inverter output 2-level voltage [75][76]. That is to say, the more carrier wave applied in the PWM the more output voltage levels can be controlled by the PWM modulation signals. So, this idea can be extended to the PWM control of multilevel inverters.

3.3 Multicarrier PWM

The multicarrier PWM strategy is mostly used to control the multilevel inverter. The principle is to use one reference wave to compare with multiple carrier waves to generate the control signal. Usually, the sine wave is used to be the reference wave and the triangle wave used to be a carrier wave. Depending on the different layout of the multiple carrier waves, the multicarrier PWM strategy is divided into phase shifted carrier PWM strategy (PSPWM) and level shifted PWM strategy (LSPWM). And then, the LSPWM can be classified into phase disposition PWM (PDPWM), phase opposition disposition PWM (PODPWM) and alternative phase opposition disposition PWM(APODPWM) [77][78][79][80].

3.3.1 Phase shifted carrier PWM (PSPWM)

The PSPSWM is especially suitable for the cascaded multilevel inverter [81] and the arrangement of the waveforms is shown in figure 3.5. In order to control a 5-level inverter, four triangle carrier waves are applied to compared with the sine wave to generate the control signals. All the triangle waves have the same frequency and amplitude [82][83]. However, each triangle wave is 90° out of phase between the two adjacent triangle waves. And for a N-level inverter, there will be N-1 triangle waves applied in this modulation strategy and the phase angle between each triangle wave is $\frac{360^\circ}{N-1}$.

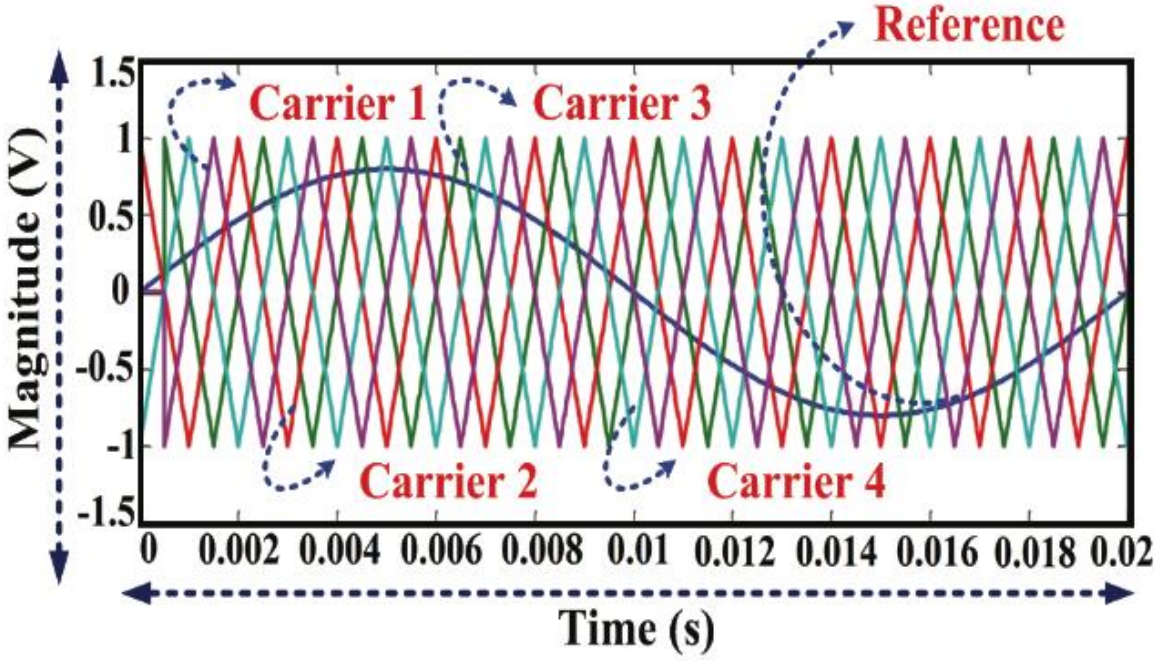


Fig 3.5 Waveform arrangements of the PSPWM

3.3.2 Level shifted PWM (LSPWM)

In the LSPWM strategy, the carrier waves should be arranged by level and all the carrier waves have the same frequency and amplitude. For the LSPWM used to control an N-level inverter, the number of carrier wave is N-1. The amplitude of the reference wave is equal to the sum of the amplitude of all the carrier waves. The signals are generated by comparing the reference wave to the carrier wave separately and when the amplitude

of reference signal is higher than the carrier wave, the output signal pulse is at high level. Otherwise, the signal pulse is at low level [84][85][86].

A. Phase disposition pulse width modulation (PDPWM)

Figure 3.6 shows the waveforms arrangement of the PDPWM strategy used to control a 7-level cascaded H-bridge inverter. It can be seen there are six triangle carrier waves, and they have the same frequency, amplitude range and the same phase. Each carrier wave is compared with the reference sine wave which is during the corresponding amplitude range. The three triangle waves above the x-axis are used to generate the pulse signal to control the inverter to output the positive three voltage levels. And the three triangle waves below the x-axis is used to generate the pulse signal to control the inverter to output the negative three voltage levels.

B. Phase opposition disposition pulse width modulation (PODPWM)

In this strategy, the six triangle waves have the same amplitude and frequency. The three triangle waves above the x-axis are in phase, and the three triangle waves below the x-axis are in phase but they are 180° out of phase with the triangle wave above the x-axis. The three triangle waves above the x-axis are used to generate the pulse signal to control the inverter to output the positive three voltage levels. And the three triangle waves below the x-axis are used to generate the pulse signal to control the inverter to output the negative three voltage levels. The arrangement of the waves is shown in figure 3.7.

C. Alternative phase opposition disposition pulse width modulation (APODWM)

In this strategy, the six triangle waves have the same amplitude and frequency. Each triangle wave is 180° out of phase with the two adjacent triangle waves. The three

triangle waves above the x-axis are used to generate the pulse signal to control the inverter to output the positive three voltage levels. And the three triangle waves below the x-axis are used to generate the pulse signal to control the inverter to output the negative three voltage levels.

The arrangement of the waves is shown in figure 3.8.

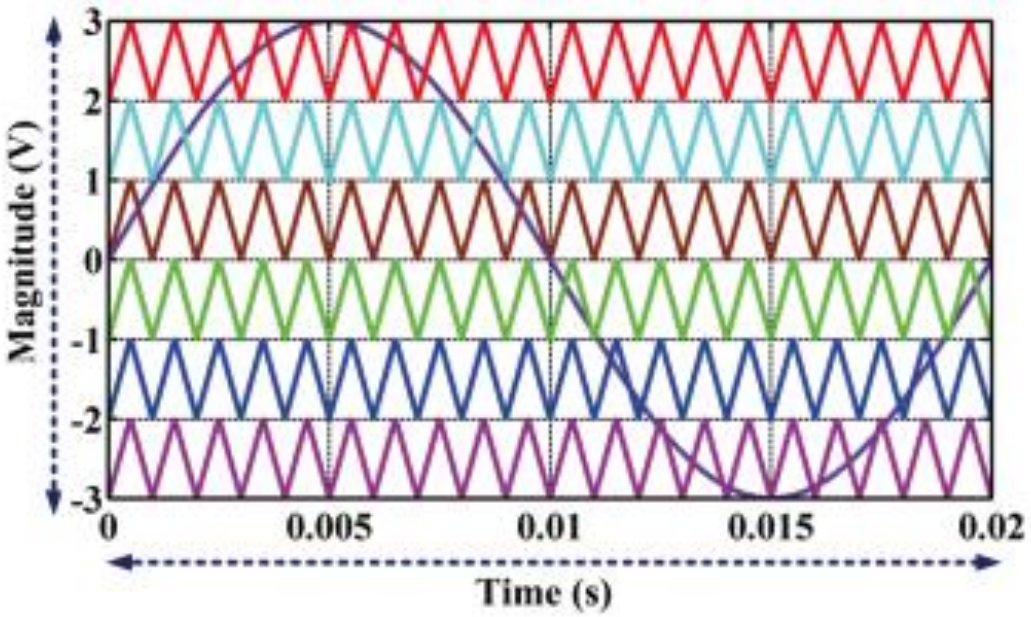


Fig 3.6 Waveform arrangements of the PDPWM

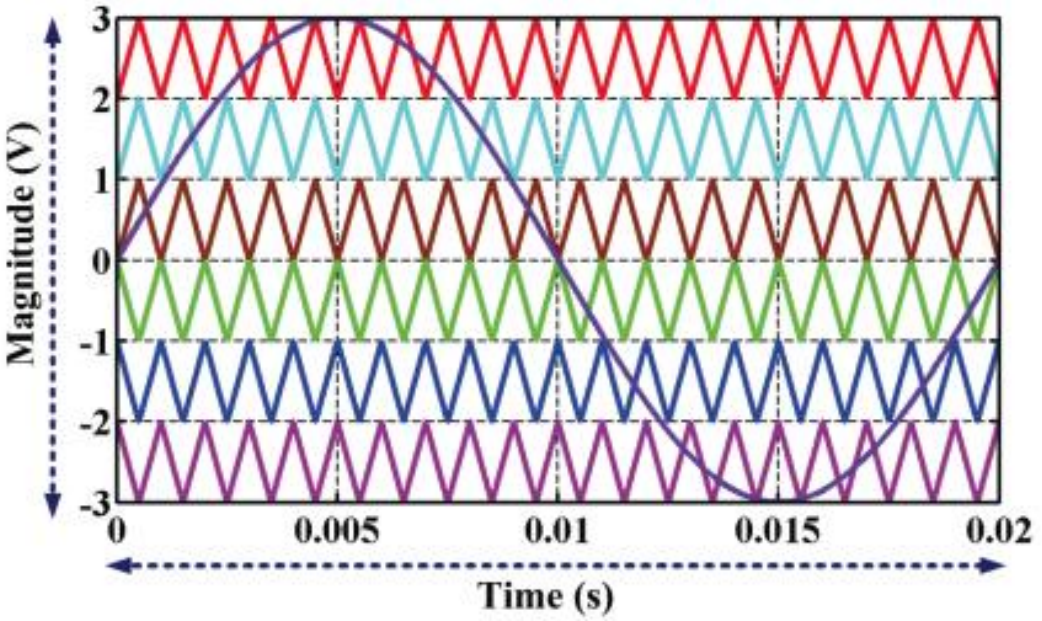


Fig 3.7 Waveform arrangements of the PODPWM

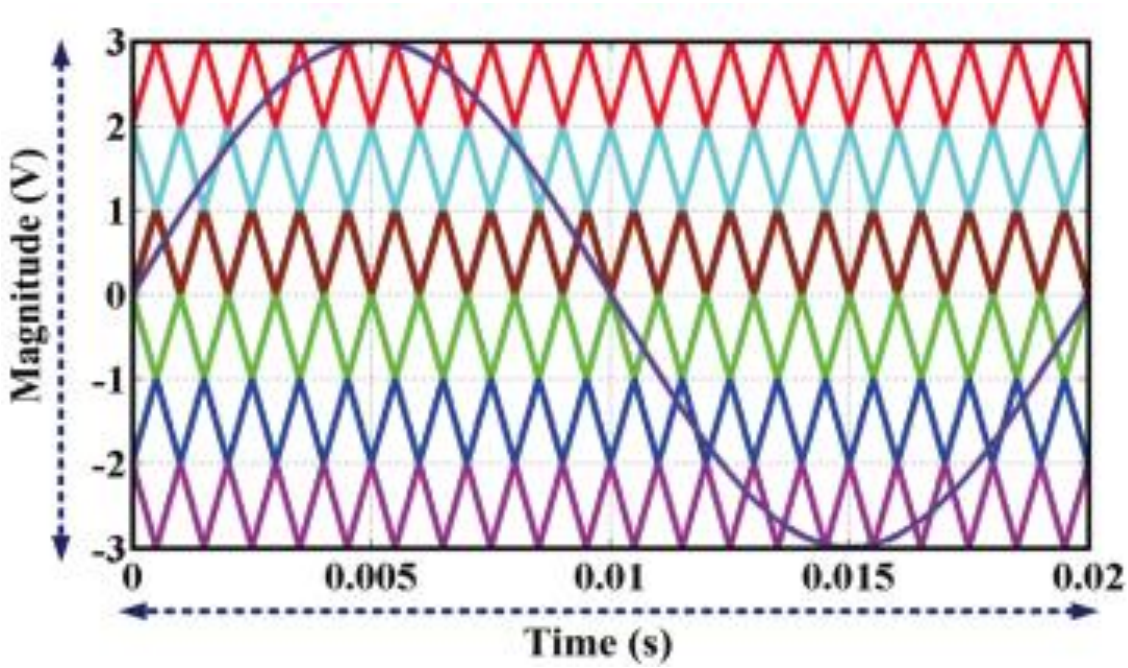


Fig 3.8 Waveform arrangements of the APODPWM

3.4 MATLAB/Simulink model implement

In this section, a 5-level cascaded H-bridge inverter is built in MATLAB/Simulink and different modulation strategies will be built to control the inverter.

The Simulink model of the 5-level cascaded inverter is shown in figure 3.9 and the logic schematic diagrams for the PSPWM, PDPWM, PODPWM and APODPWM are shown in figure 3.10-figure 3.13.

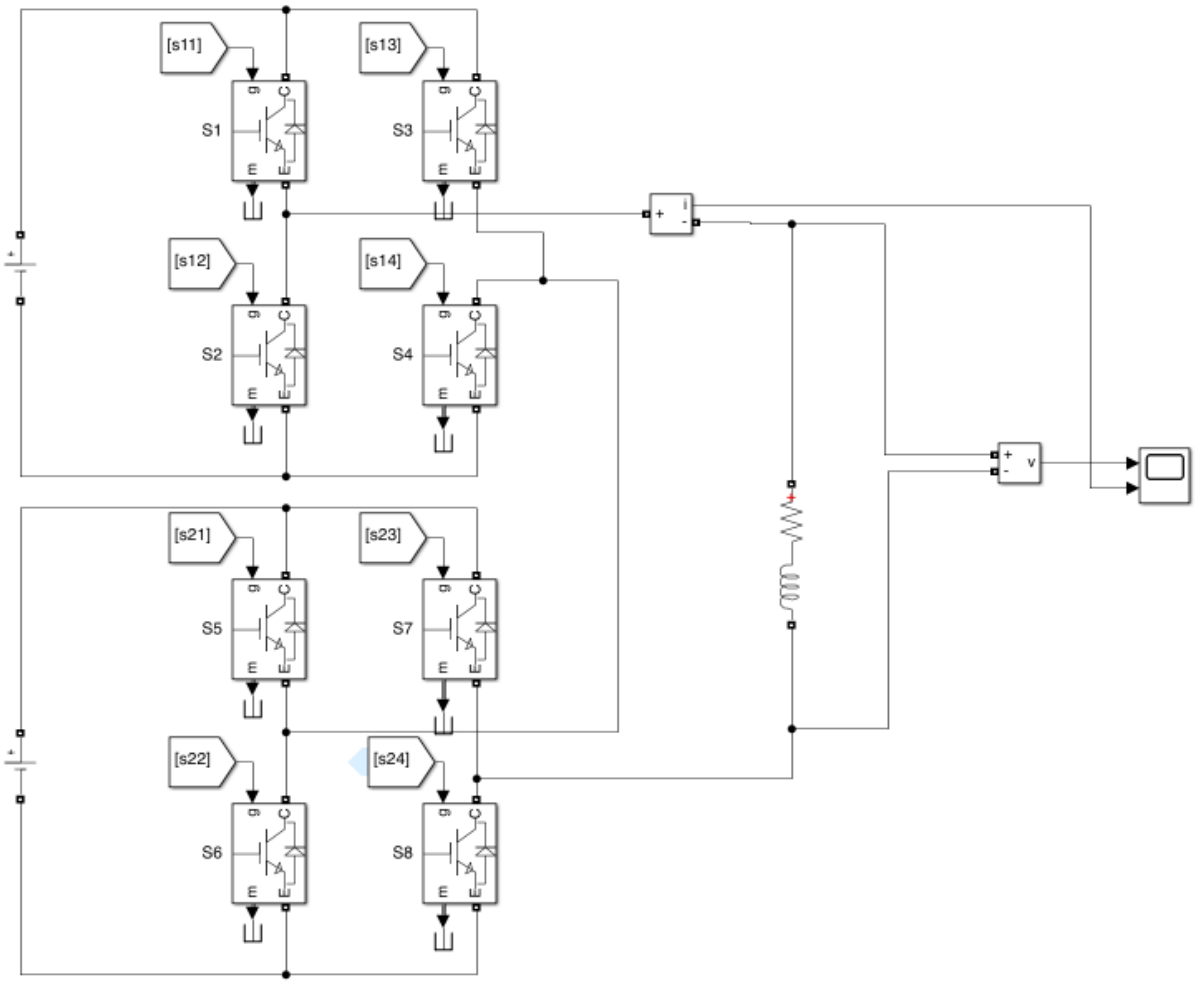


Fig 3.9 Simulink model of 5-level cascaded H-bridge inverter

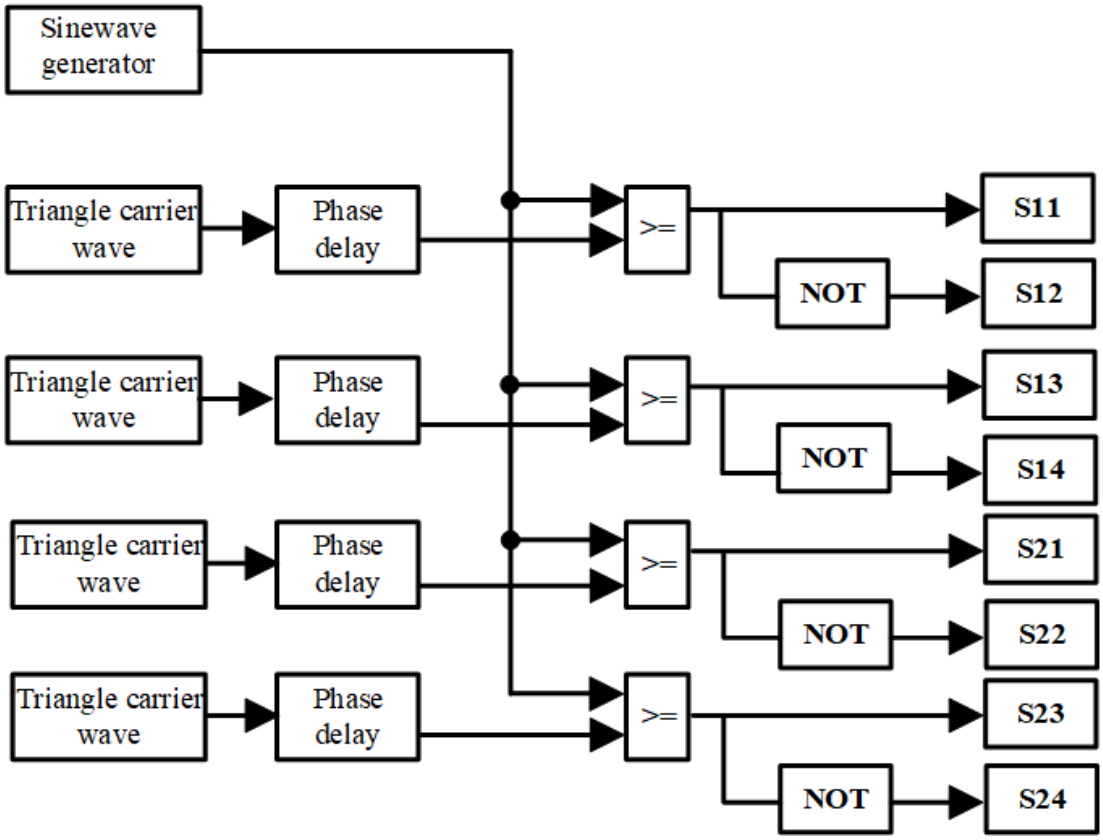


Fig 3.10 Logic schematic of PSPWM

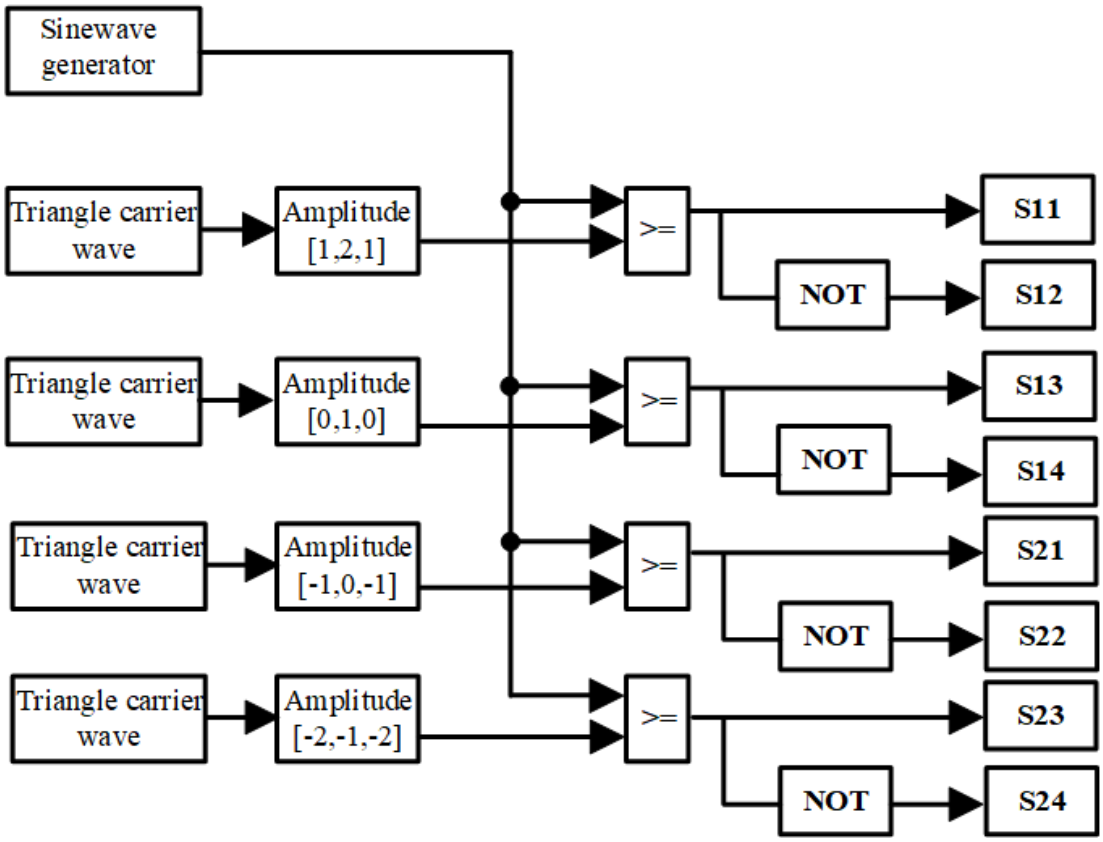


Fig 3.11 Logic schematic of PDPWM

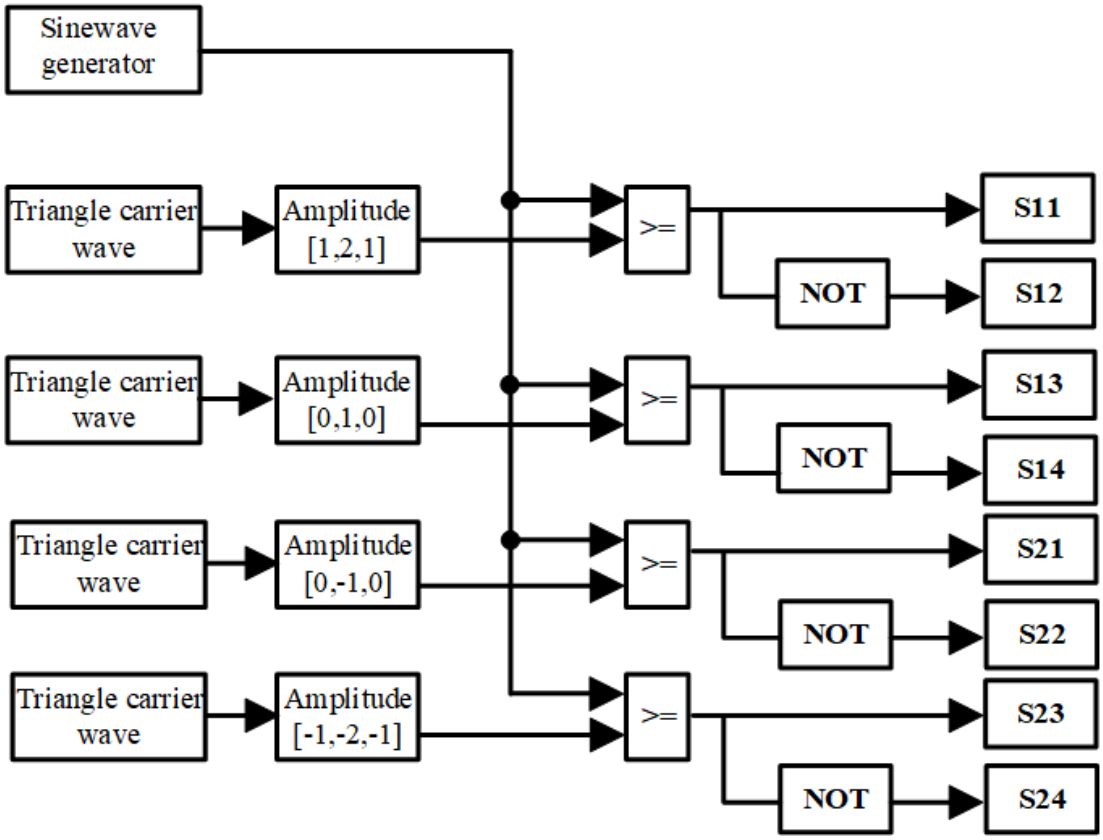


Fig 3.12 Logic schematic of PODPWM

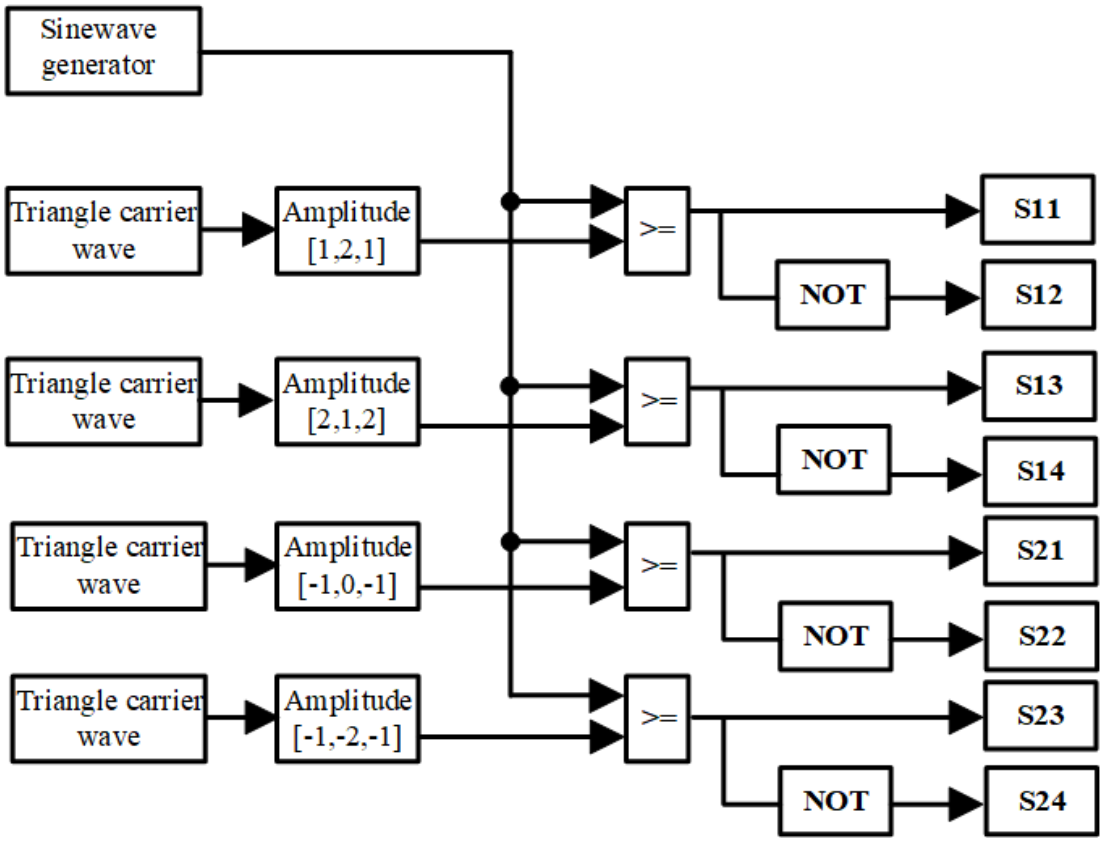


Fig 3.13 Logic schematic of APODPWM

3.5 Capacitance calculation for switched capacitor multilevel inverter

The capacitance of the capacitors applied in the switched capacitor circuit is crucial. In switched capacitor inverters, capacitors are used to generate different voltage levels through charging and discharging processes. These voltage levels are achieved by connecting capacitors in various series and parallel configurations to form the desired output voltage [87][88]. And the capacitors need to maintain stable voltages across different switching states. Incorrect capacitance values can prevent capacitors from reaching or maintaining the required voltage levels during charging and discharging cycles, leading to inaccurate or unstable output voltage levels.

3.5.1 Capacitor voltage ripple

The voltage ripple refers to the variation of fluctuation of voltage across a capacitor over time. It is typically measured as peak-to-peak voltage variation during the charge and discharge cycles of a capacitor. For the switched capacitor multilevel inverters, the capacitor voltage ripple is a critical performance metric. When the inverter operating, the capacitors will undergo several charges and discharges, when the charge and discharge time do not match, or when the switching sequence is unreasonable, can precipitate unbalance charging and discharging of the capacitor. Such unbalancing or over-discharging will increase the capacitor voltage ripple. So the capacitance value directly affects the size of the voltage ripple on the output. A capacitance value that is too small may result in a larger voltage ripple, affecting the accuracy and stability of the voltage levels. A capacitance value that is too big can significantly reduce the voltage ripple. However, the corresponding charging time will be extended, which will be detrimental to the transient response of the inverter. Appropriate capacitance values help reduce voltage ripple and improve the stability of the output voltage [89][90].

3.5.2 Capacitance calculation

In the context of PWPWM, the intersection area between the sine wave and each triangle wave indicates each period of inverter output voltage level. This relationship is exemplified in figure 3.14, where the intersection points of these waveforms are denoted as t_1 to t_{15}. These points are indicative of transitional moments where the output voltage shifts from one level to the next.

Due to different switched capacitor topologies and switching logic, the charging and discharging periods of the capacitor are also different, but the charging and discharging must be within a time range corresponding to one or more levels. However, according to the design, the level corresponding to the charging and discharging of the capacitor is known, so if the above-mentioned t_1 to t_{10} can be calculated, then the charging and discharging time of the capacitor can be known. To this end, equation 3.1 and 3.2 is employed for calculating the specific time instances of t_1 to t_{15}.

$$t_i = \frac{\arcsin(i/8)}{2\pi f_{ref}} \quad i = 1, 2, \dots, 7 \qquad (3.1)$$

$$t_j = \pi - \frac{\arcsin[(15-j)/8]}{2\pi f_{ref}} \quad j = 8, 9, \dots, 15 \qquad (3.2),$$

Where f_{ref} represents the reference signal frequency.

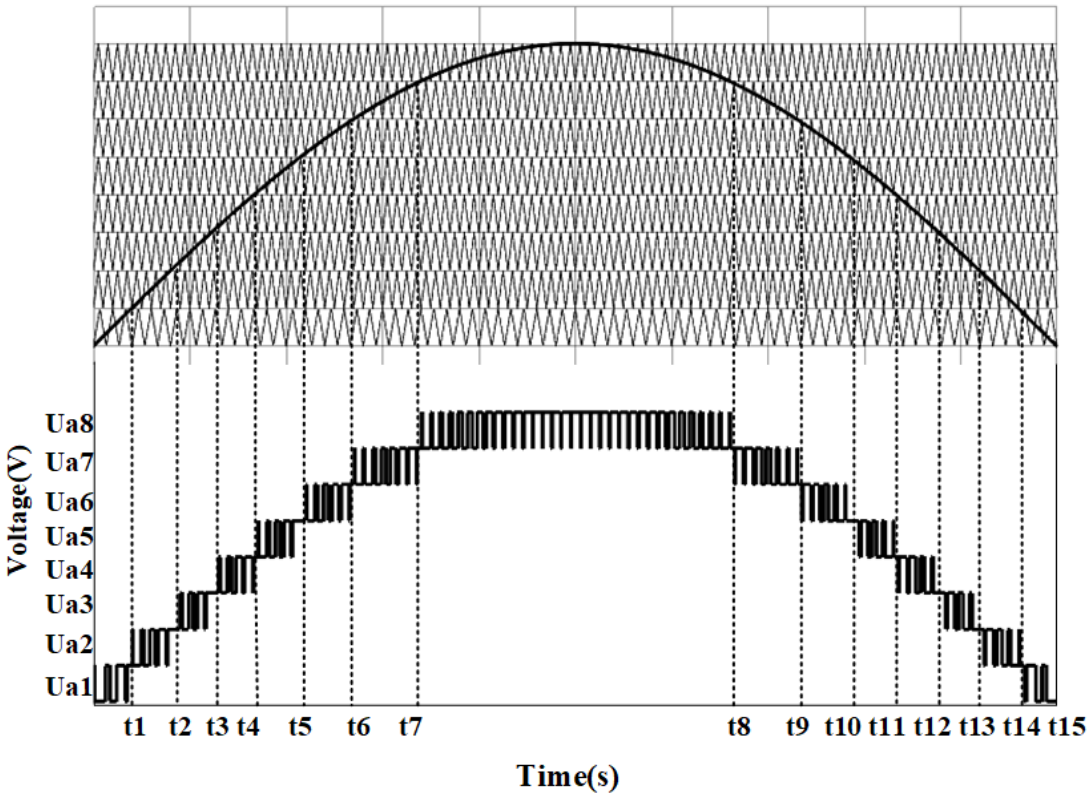


Fig 3.14 The waveforms of the PDPWM

The capacitance is depending on the voltage ripple V_r, and the voltage ripple is determined by the maximum discharging amount Q_c, so the capacitance can be calculated by the equation 3.3 and 3.4.

$$Q_c = \int_{t_b}^{t_a} Isin(2\pi f_{ref}\, t)dt \qquad (3.3),$$

$$C = \frac{Q_c}{V_r} \qquad (3.4),$$

Where t_a represents the capacitor discharge start moment and t_b represents the capacitor discharging finish moment. *I* represent the peak value of the output current.

3.5.3 Chapter conclusion

This chapter introduces the modulation strategies used for multilevel inverters. The basic modulation strategy is sinewave pulse width modulation (SPWM). The principle of SPWM involves comparing a sinusoidal modulation wave with a triangular carrier

wave to generate output signals that control the switches in the inverter. Multicarrier pulse width modulation (PWM) is an evolution of SPWM, where the number of triangular carrier waves is determined by the number of levels in the inverter output voltage. Each carrier wave is compared with the sinusoidal modulation wave to generate signals corresponding to the switching states of the inverter. Based on the arrangement of carrier waves, multicarrier PWM can be divided into Phase Shifted Carrier PWM (PSPWM) and Level Shifted PWM (LSPWM). Level Shifted PWM (LSPWM) is further classified according to the phase relationships of the carrier waves into Phase Disposition Pulse Width Modulation (PDPWM), Phase Opposition Disposition Pulse Width Modulation (PODPWM), and Alternative Phase Opposition Disposition Pulse Width Modulation (APODWM). The logic schematics of these control strategies are presented by using MATLAB/Simulink in this chapter. Furthermore, this chapter discusses methods for calculating capacitance values in switched capacitor inverters.

Chapter 4: Modelling and simulation analysis of a 13-level switched capacitor multilevel inverter.

4.1 Chapter introduction

In this chapter, two novel switched capacitor inverter topologies are proposed, and the corresponding multicarrier PWM-based modulation strategies are also developed. A comprehensive analysis of the operational principles is presented, and the MATLAB/Simulink software was used to simulate the proposed topology. At the end of this chapter, a detailed comparative study was conducted on the simulation results of the two proposed topologies.

4.2 Configuration of a novel 13-level switched capacitor inverter

Switched capacitor inverters are considered capable of achieving self-balancing and self-boosting capabilities with fewer power components, as elaborated in Chapter 2.

Adhering to the abovementioned principles, figure 4.1 presents a newly designed topology that exemplifies a novel self-boosting and capacitor voltage self-balancing structure. This topology is composed of two diodes, four capacitors, and thirteen switches, configured to achieve a 13-level voltage output and three times voltage boost.

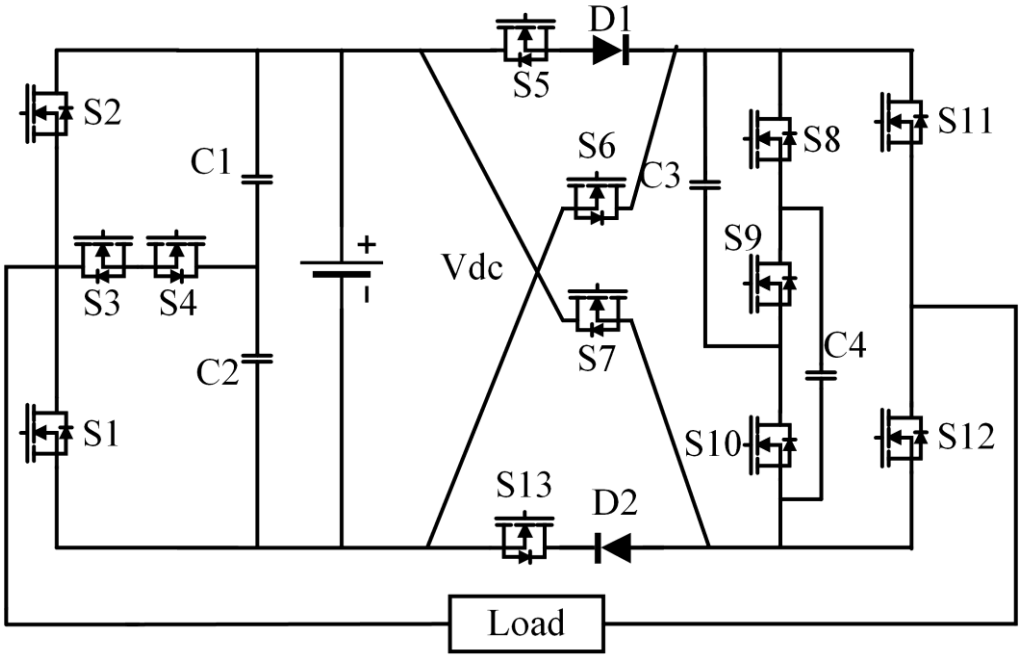


Fig 4.1 Topology of 13-level switched capacitor inverter

As shown in figure 4.1, the topology consists of a t-type, crossing, and series/parallel capacitor structures. Among them, switches S8, S9, and S10 and capacitors C3 and C4 form a series/parallel capacitor structure. The two capacitors can be charged in parallel with the DC supply and then discharged in series or individually. Switches S1, S2, S3, S4, and capacitors C1 and C2 form a T-type structure. Due to the participation of this structure, this topology can output more levels and significantly reduce the voltage step between each level of the output voltage. Correspondingly, the rate of change of voltage ($dv\ /\ dt$) will also become smaller. The benefits of small $dv\ /\ dt$ are low switching stress and low EMI [91][92]. The harmonic content will be lower since the output voltage is closer to sinusoidal. It is worth mentioning that the voltage step between the levels of the proposed topology is $V_{dc}/2$.

In comparison, if the T-type structure is replaced with a DC-link capacitor, the topology will output a 7-level voltage and the voltage step between the levels will grow to V_{dc}. In addition, different from other topologies that apply an H-bridge circuit to realize the voltage polarity change, the proposed topology reasonably arranges the overall circuit and realizes the polarity change of the output voltage through the inherent circuit of the

topology. This will be described in detail in the following topology operating principal part.

Moreover, this topology is an extendable structure that can be extended for different applications to output higher voltage boosts and more levels.

The extension of the proposed topology is shown in figure 4.2. The red box marks the extendable switched capacitor cell. Each cell includes two capacitors, two diodes and seven switches. The two capacitors in each cell can be charged to V_{dc} and the maximum series discharge voltage is $2V_{dc}$. So, the proposed inverter output will increase by $2V_{dc}$ and eight levels with one more cell connected to the circuit. In addition, for a topology with n cells, the output voltage (V_{out}) can be expressed by equation 4.1 and the number of output voltage levels (N_l) can be expressed by equation 4.2.

$$V_{out} = (2n + 1)V_{dc} \qquad (4.1)$$

$$N_l = 8n + 5 \qquad (4.2)$$

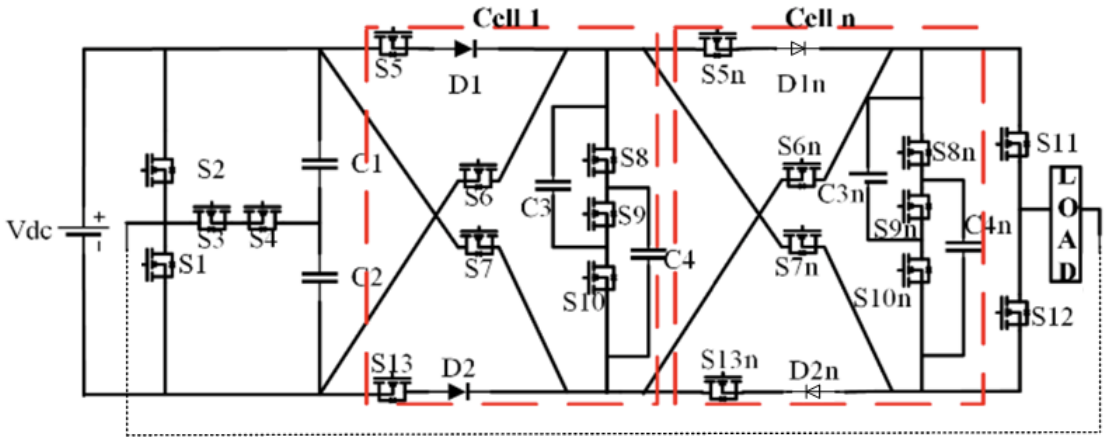


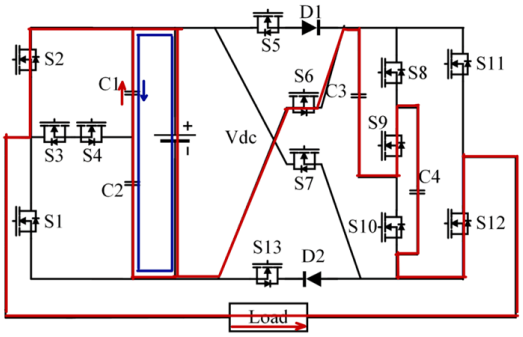
Fig4.2. Extension of the proposed 13-level SCMLI

4.3 Operation principle

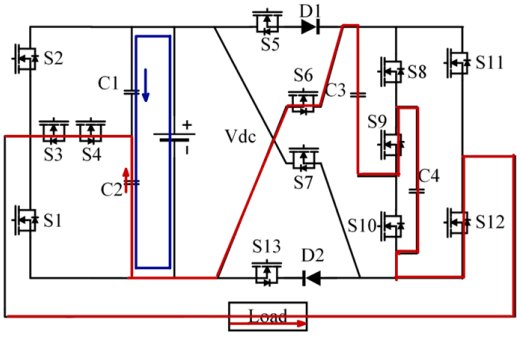
There are 13 switching states of the proposed 13-level SCMLI, and they are shown in Table 4.1. The “C” and “D” in the table indicate the charging state and discharging state of the capacitors, respectively. Correspondingly, according to the switching state, the inverter has 13 operating modes. The inverter operating circuit of each mode is shown in figure 4.3, in which the current path and capacitor discharge path of the corresponding mode are marked with blue lines, and the red line represents the charging path of the capacitors.

Uo	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	C1	C2	C3	C4
+3Vdc	0	1	0	0	0	1	0	0	1	0	0	1	0	D	D	D	D
+5/2Vdc	0	0	1	1	0	1	0	0	1	0	0	1	0	-	D	D	D
+2Vdc	0	1	0	0	0	1	0	1	0	1	0	1	0	D	D	D	D
+3/2Vdc	0	0	1	1	0	1	0	1	0	1	0	1	0	-	D	D	D
+Vdc	0	1	0	0	0	0	0	0	0	0	0	1	1	D	D	-	-
+1/2Vdc	0	0	1	1	1	0	0	1	0	1	0	1	1	-	D	C	C
+0Vdc	1	0	0	0	1	0	0	1	0	1	0	1	1	C	C	C	C
-0Vdc	0	1	0	0	1	0	0	1	0	1	1	0	1	C	C	C	C
-1/2Vdc	0	0	1	1	1	0	0	1	0	1	1	0	1	D	-	C	C
-Vdc	1	0	0	0	1	0	0	0	0	0	1	0	0	D	D	-	-
-3/2Vdc	0	0	1	1	0	0	1	1	0	0	1	0	0	D	-	D	D
-2Vdc	1	0	0	0	0	0	1	1	0	1	1	0	0	D	D	D	D
-5/2Vdc	0	0	1	1	0	0	1	0	1	0	1	0	0	D	-	D	D
-3Vdc	1	0	0	0	0	0	1	0	1	0	1	0	0	D	D	D	D

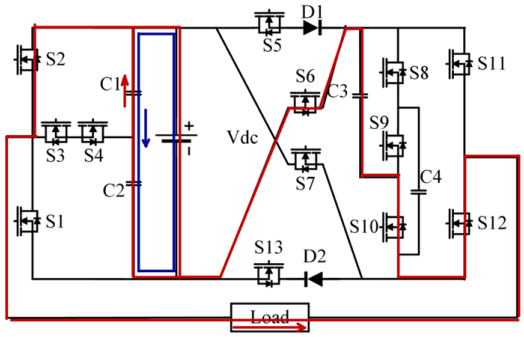
Table 4.1 Switching states of proposed 13-level SCMLI



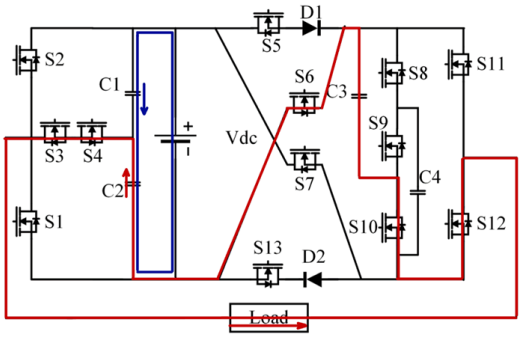
+3Vdc



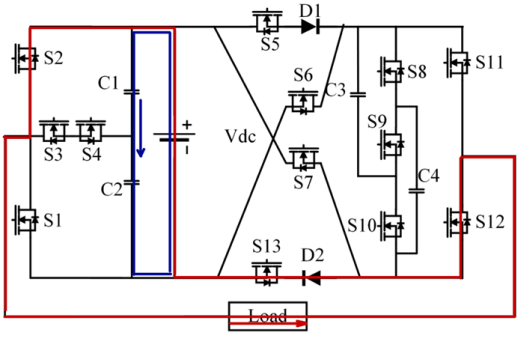
+2.5Vdc



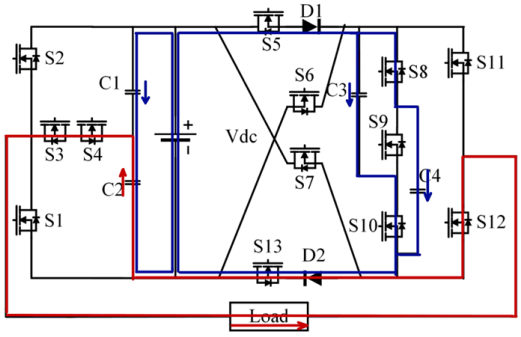
+2Vdc



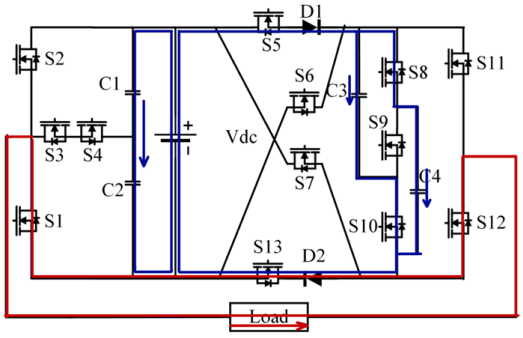
+1.5Vdc



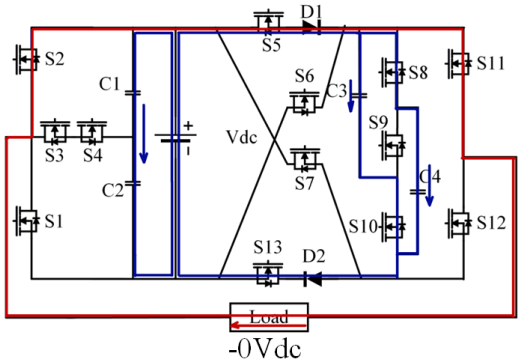
+Vdc



+0.5Vdc



+0Vdc



-0Vdc

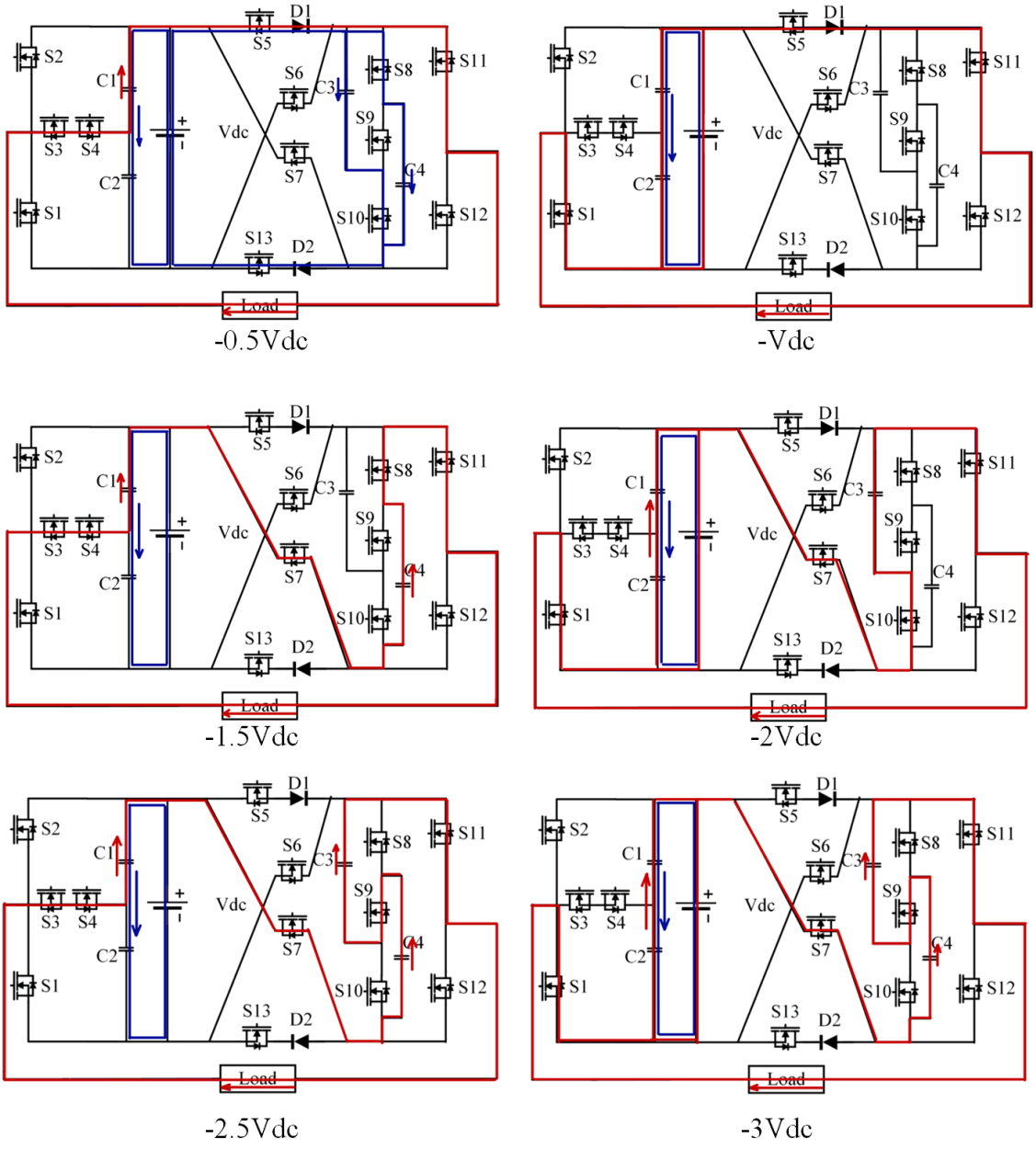


Fig 4.3 Operating circuit of each mode

The operating modes are described below:

Mode1($+3V_{dc}$): Switches S2, S6, S9, and S12 are turned on, and other switches are turned off. Capacitors C1, C2, C3, and C4 are connected in series and discharged via the load.

Mode2($+5/2V_{dc}$): Switches S3, S4, S6, S9 and S12 are turned on, and other switches

are turned off. Capacitors C2, C3, and C4 are connected in series and discharged via the load.

Mode3(+2V_{dc}): Switches S2, S6, S10, and S12 are turned on, capacitor C3 and C4 are connected in parallel and then discharged in series with C1 and C2.

Mode4(+3/2V_{dc}): Switches S3, S4, S6, S10, and S12 are turned on. Capacitors C2 and C3 are connected in series and discharged via the load.

Mode5(+V_{dc}): Switches S2, S12, and S13 are turned on. Capacitors C1 and C2 are connected in series and discharged via the load.

Mode6(+1/2V_{dc}): Capacitor C2 discharges via the load through the switch S3, S4, S12, S13, and diode D2. Simultaneously, capacitors C3 and C4 are connected parallel with the DC power supply and charged to V_{dc} through S5, S8, S10, S13, D1, and D2.

Mode7(0): Because the 0 level spans the positive and negative half cycles of the output voltage, the 0 level can be divided into +0 and -0, which respectively represent the interval where the 0 level is in the positive half cycle of the output voltage and the 0 level is in the interval of the negative half cycle of the output voltage. The +0 interval is achieved by turning on switches S1, S8, S10, S12, and S13. Capacitors C1 and C2 are connected in series and charged to 1/2V_{dc} separately. Capacitors C3 and C4 are connected in parallel and charged to Vdc separately. The -0 interval is achieved by turning on switches S2, S5, S8, S10, S11 and S13. Capacitors C1 and C2 are connected in series and charged to 1/2V_{dc} separately. Capacitors C3 and C4 are connected in parallel and charged to Vdc separately. In this state, diodes D1 and D2 are working in a forward conduction state.

Mode8(-1/2V_{dc}): In this mode, the switches S3, S4, S5, and S11 are ON state, and the capacitor C1 discharges to the load. And the capacitors C3 and C4 are connected

parallel with the DC power supply and charged to V_{dc} through S5, S8, S10, S13, D1, and D2.

Mode9(-V_{dc}): when the switches S1, S5, S11 are on state, capacitors C1 and C2 are connected in series to discharge to the load.

Mode10(-3/2V_{dc}): when the switches S3, S4, S7, S8 and S11 are ON state, capacitor C3 and C4 are connected in parallel and then discharged in series with C1.

Mode11(-2V_{dc}): when the switches S1, S7, S10 and S11 are ON state, capacitor C3 and C4 are connected in parallel and then discharged in series with C1 and C2.

Mode12(-5/2V_{dc}): when the switches S3, S4, S7, S9, S11 are ON state, the capacitors C1, C3 and C4 are series connected to discharge to the load.

Mode13(-3V_{dc}): when the switches S1, S7, S9, S11 are ON state, the capacitors C1, C2, C3 and C4 are series connected to discharge to the load.

Notably, since capacitors C1 and C2 are directly connected to the DC supply, they will quickly recharge through the DC supply after each discharge pulse.

4.4 Modulation strategy

The PDPWM technology is used to generate the control signal, and the principle is shown in figure 4.4. There are twelve triangle waves, which are the carrier wave, and one sine wave, which is the reference wave. All the carrier waves have the same amplitude (A_c) and frequency (f_c). The frequency of the reference wave (f_{ref}) is 50Hz, and the amplitude of the reference wave is represented by A_{ref}. The modulation index (M) is expressed by equation 4.3, and the output level and the voltage value of the proposed inverter are directly related to it. Thus, when the amplitude of the carrier wave

is fixed, the output voltage and level depend on the amplitude of the reference wave.

$$M = \frac{A_{ref}}{6A_c} \qquad (4.3)$$

In figure 4.4, $U_1 - U_{12}$ are the control signals obtained by comparing the sine wave with different triangle waves, respectively. Each signal corresponds to the modulation interval of the corresponding level of the inverter output voltage. By logically combining different signals according to the switching states of the inverter in Table 4.1, the gate signal of each switch in the inverter can be obtained.

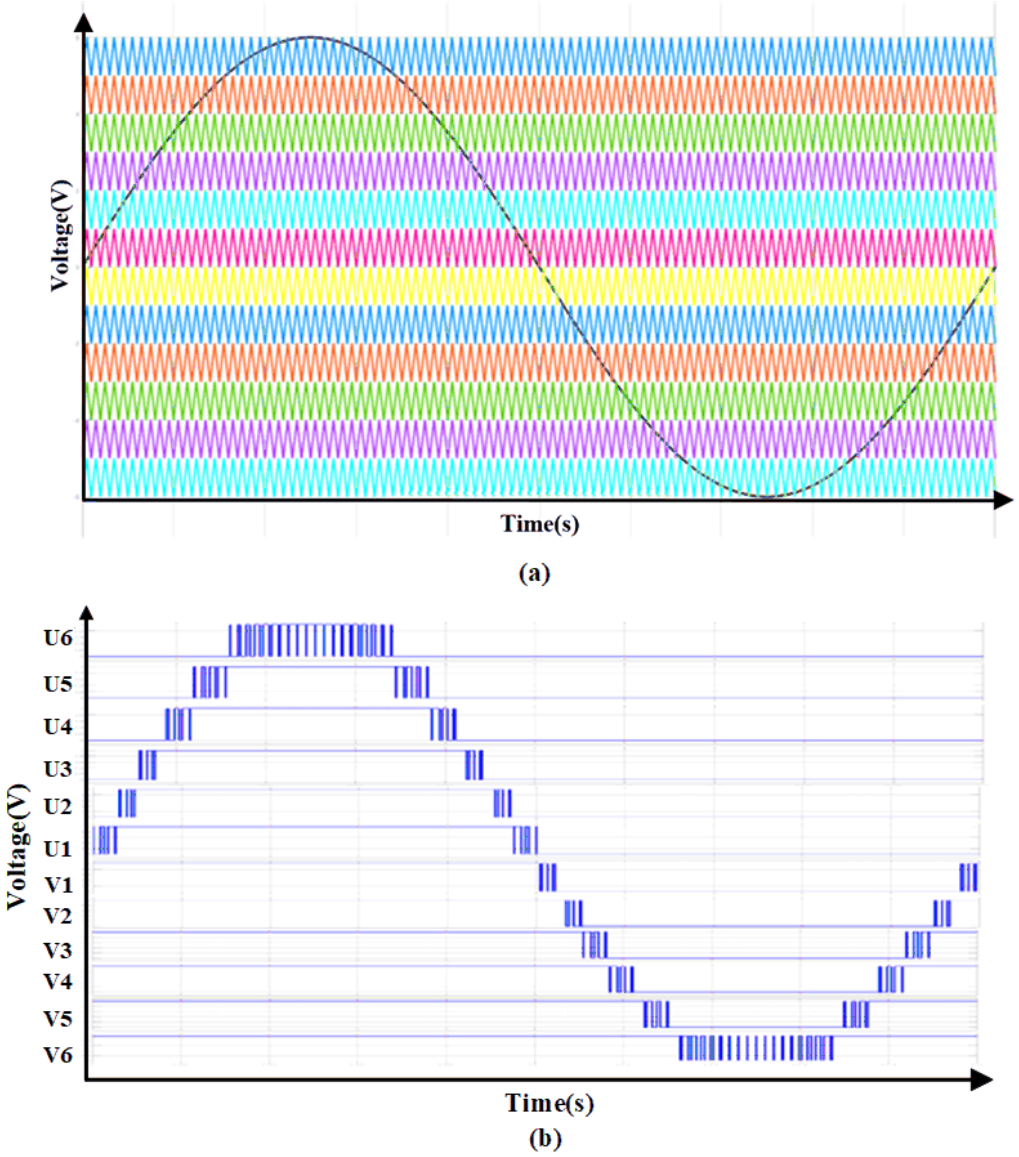


Fig 4.4 Principle of PDPWM (a) Waveform arrangement

(b) Waveform of $U_1 - U_6, V_1 - V_6$

The gate signal of each switch can be expressed by the following equations.

S1=$\bar{V}_3V_2 + \bar{V}_5V_4 + \bar{V}_6$ (4.4)

S2=$U_6 + \bar{U}_4U_5 + \bar{U}_2U_3$ (4.5)

S3=$\bar{U}_5U_6 + \bar{U}_3U_4 + \bar{U}_1U_2 + \bar{V}_2V_1 + \bar{V}_4V_3 + \bar{V}_6V_5$ (4.6)

S4=$\bar{U}_1U_2 + \bar{U}_3U_4 + \bar{U}_5U_6 + \bar{V}_2V_1 + \bar{V}_4V_3 + \bar{V}_6V_5$ (4.7)

S5=$\bar{U}_1U_2 + \bar{V}_2V_1 + \bar{V}_3V_2$ (4.8)

S6=U_3 (4.9)

S7=$\bar{V}_3$ (4.10)

S8=$\bar{U}_3U_4 + \bar{U}_4U_5 + \bar{U}_1U_2 + \bar{V}_2V_1 + \bar{V}_4V_3 + \bar{V}_5V_4$ (4.11)

S9=$U_5 + \bar{V}_5$ (4.12)

S10=$\bar{U}_3U_4 + \bar{U}_4U_5 + \bar{U}_1U_2 + \bar{V}_2V_1 + \bar{V}_5V_4$ (4.13)

S11=$\bar{V}_2$ (4.14)

S12=U_1 (4.15)

S13=$\bar{U}_1U_2 + \bar{U}_2U_3 + \bar{V}_2V_1 + \bar{V}_3V_2$ (4.16)

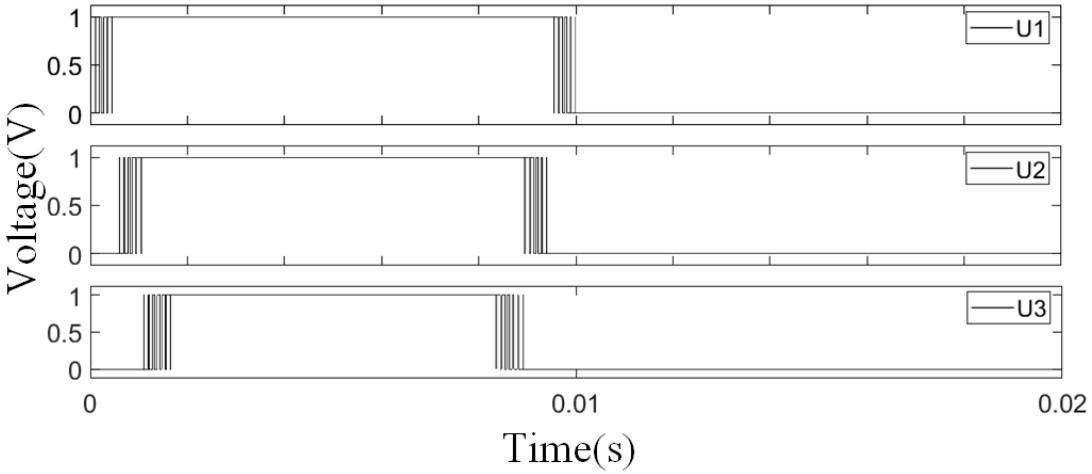


Fig 4.5 Waveforms of signal U1-U3

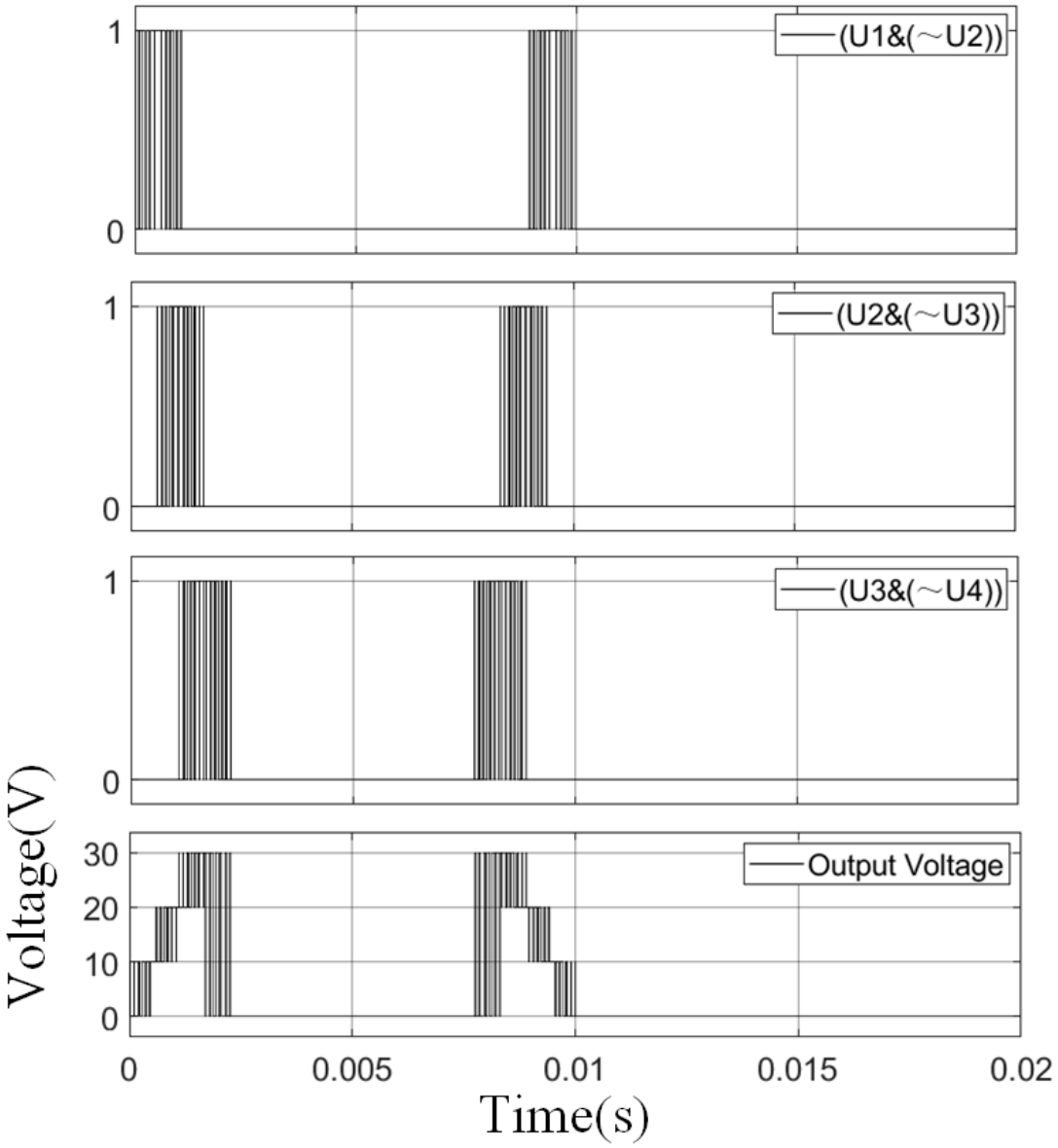


Fig 4.6 Logic signal and corresponding output voltage level

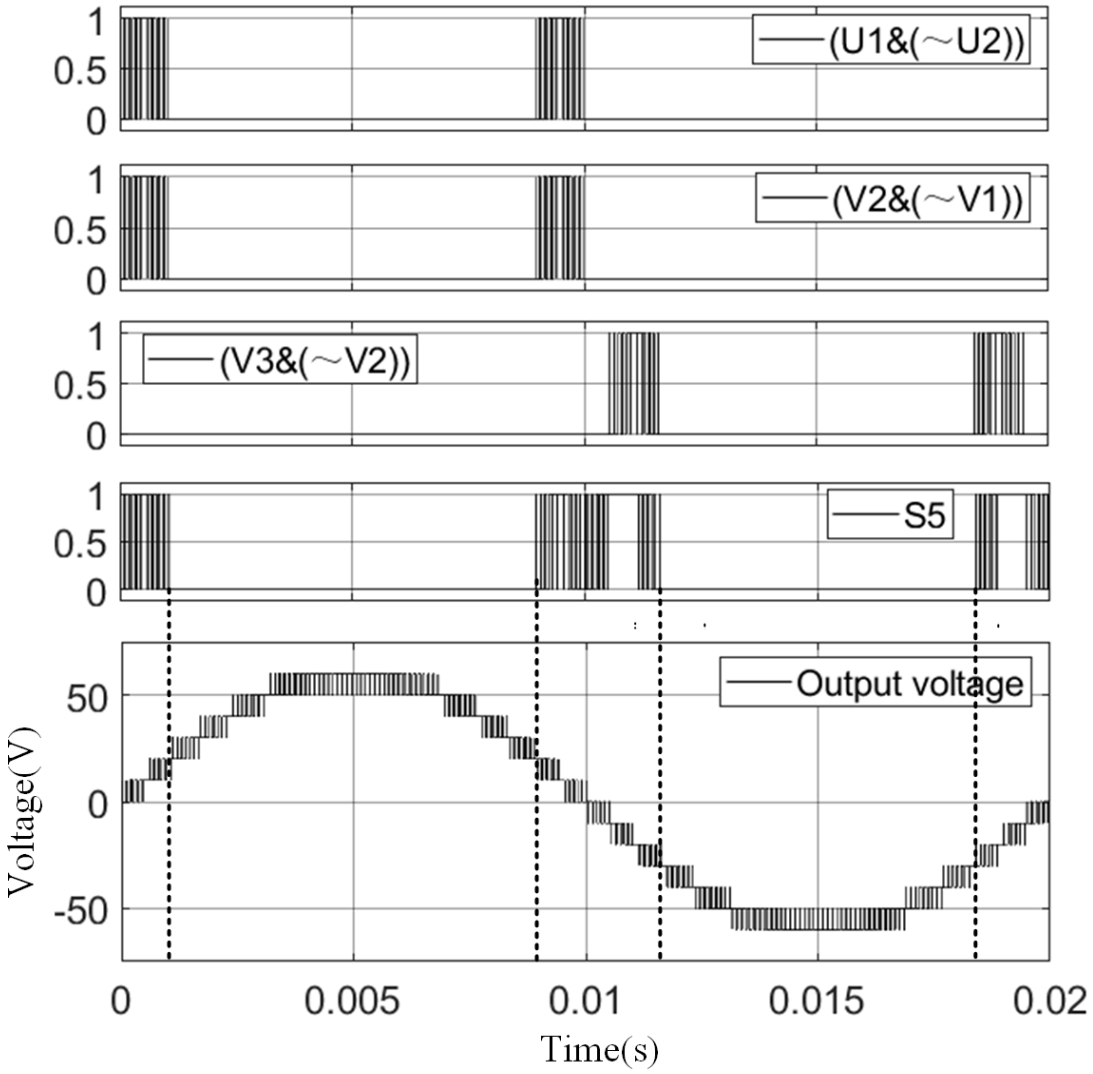


Fig 4.7 Drive signal of switch S5

In figure 4.5, U1, U2, and U3 are the results of comparing the carrier wave with the sinusoidal wave. The pulse signals correspond to the first, second, and third levels of the output voltage, respectively. However, it can be observed from the figure that these comparison signals remain high in the intervals of non-corresponding levels. This implies that if these signals are directly used to control switches, the switches may also turn on during non-corresponding levels, potentially causing a short circuit in the inverter circuit.

To address this issue, the control signals for switches corresponding to each level can be obtained through a logical "AND" operation between the signal for that level and

the inverse signal of the next level. These processed signals are shown in figure 4.6. According to Table 4.1, the conduction interval for switch S5 corresponds to the inverter output voltage ranging from +1/2Vdc to −Vdc. As shown in figure 4.7, by combining the control signals for each level, the switching signal for S5 can be derived.

4.5 Capacitance calculation

Since the proposed topology is symmetrical, capacitors C1 and C2 charge and discharge symmetrically during the positive and negative half-cycles, and capacitors C3 and C4 discharge symmetrically during these cycles as well. Therefore, this section only analyzes the discharge states of C2 and C4 during the positive half-cycle to calculate the capacitance values.

Figure 4.8 shows the positive half-cycle waveform of the inverter's output voltage and the corresponding capacitor discharge current waveform. As illustrated, during the positive half-cycle, capacitor C2 discharges continuously; however, as it is directly connected to the voltage source, the voltage source automatically recharges the capacitor instantly at the end of each discharge pulse. Figure 4.9 is a close-up view of figure 4.8, showing the capacitor's slight charging current. It can be known from figure 4.8, C4, capacitor C4 discharges over the time interval from t2 to t9, with a sinusoidal trend.

As noted above, the discharge current of capacitor C2 does not follow a sinusoidal trend, so it cannot be solved using equation 3.3 and 3.4 from Chapter 3. Here, it is necessary to first calculate the average discharge current of the capacitor and then calculate using equation 4.16 and 4.17. According to simulation results, the capacitance value has minimal impact on the average discharge current, so the average current of the capacitor obtained in MATLAB is 1.5 A.

By substituting this average current value into equation 4.17 and equation 4.18 and setting the capacitor's voltage ripple to 10%, the capacitance of C2 is calculated to be

1500 µF. The capacitance of C4 is calculated using equation 3.3 and 3.4, also with a voltage ripple set to 10%, resulting in a capacitance value of 2600 µF. The capacitor discharge voltages are shown in figure 4.10.

$$Q_c = I_{avg} \times t \qquad (4.17),$$

$$C = \frac{Q_c}{V_r} \qquad (4.18),$$

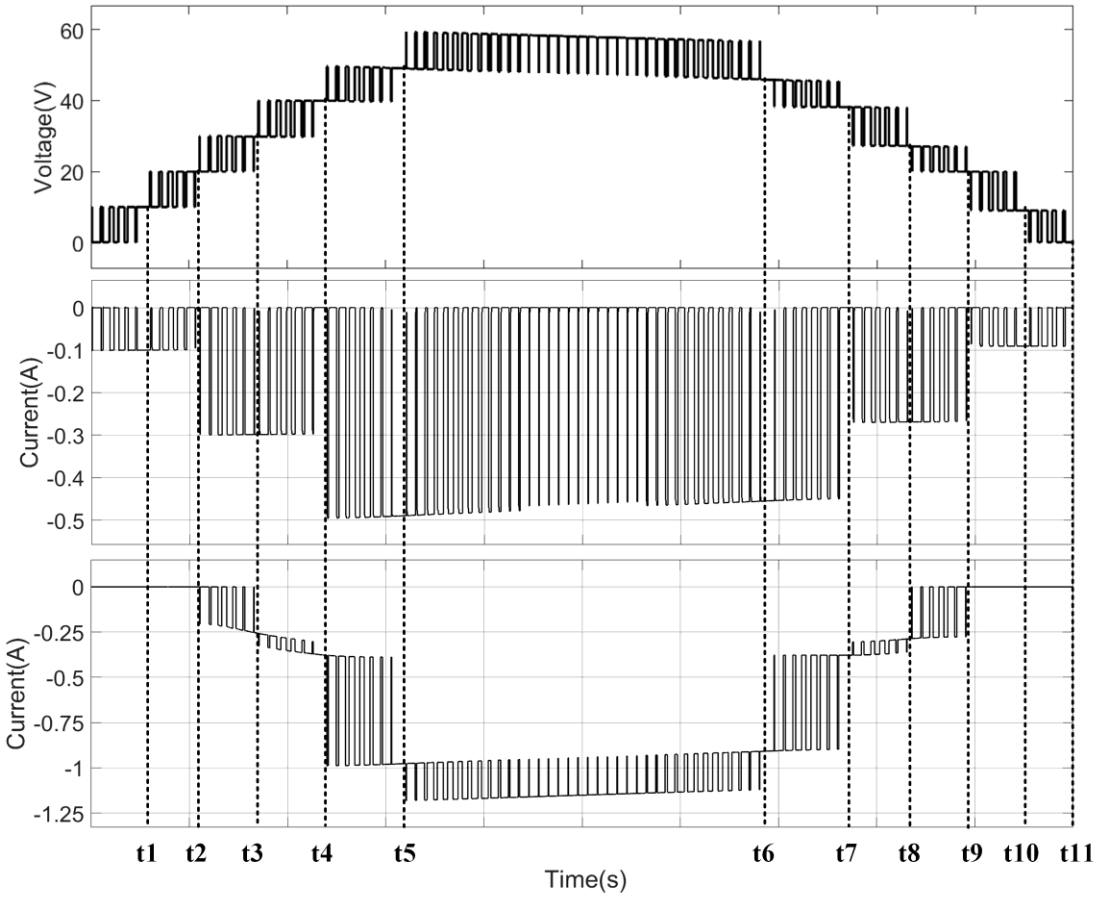


Fig 4.8 Positive half-cycle of the output voltage and discharge current of the capacitor C2 and C3

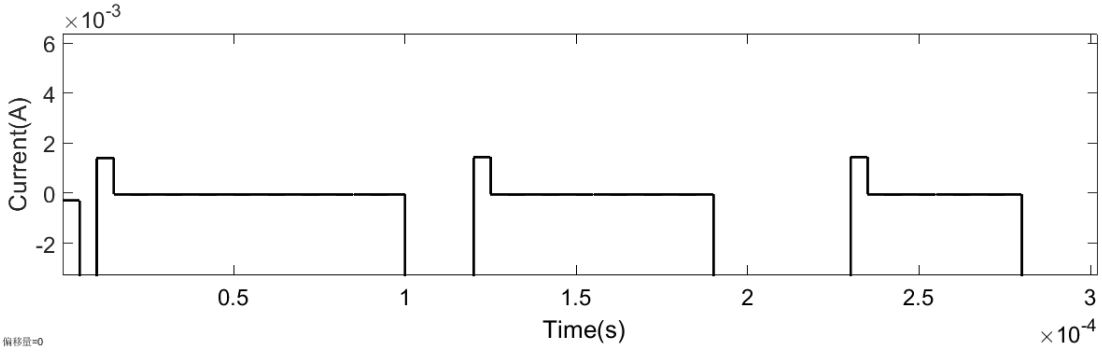


Fig 4.9 Current waveform close-up view of capacitor C2

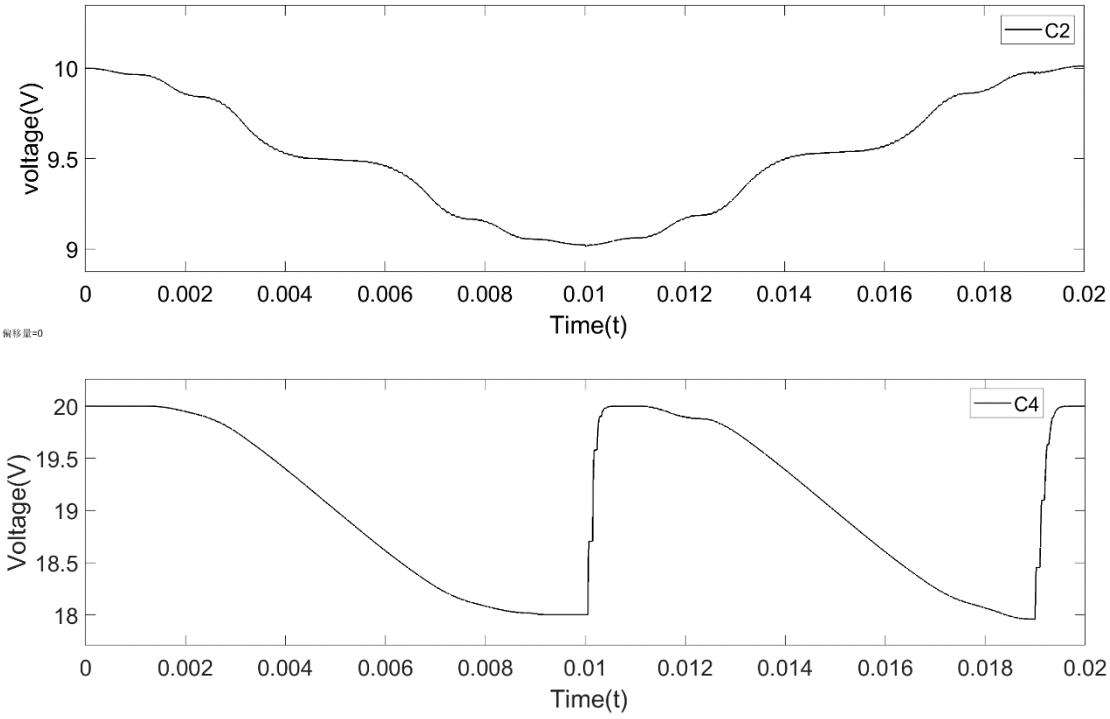


Fig 4.10 Voltage of capacitors C2 and C4

4.6 Simulation setup

The operation principle and the modulation strategy of the proposed topology are described in detail above. So, the circuit of the proposed topology built using MATLAB/Simulink, and the schematic diagram of the control logic is shown in figure 4.11. The simulation parameters of the topology are shown in Table 4.2.

Frequency of the sine wave (f_{ref})	50Hz
Frequency of the carrier wave (f_c).)	20kHz
V_{dc}	20V
Capacitance of capacitor C1	1500uF
Capacitance of capacitor C2	1500uF
Capacitance of capacitor C3	2600uF
Capacitance of capacitor C4	2600uF
Resister load R	50Ω
Inductance load L	5mH

Table 4.2 Simulation model parameters

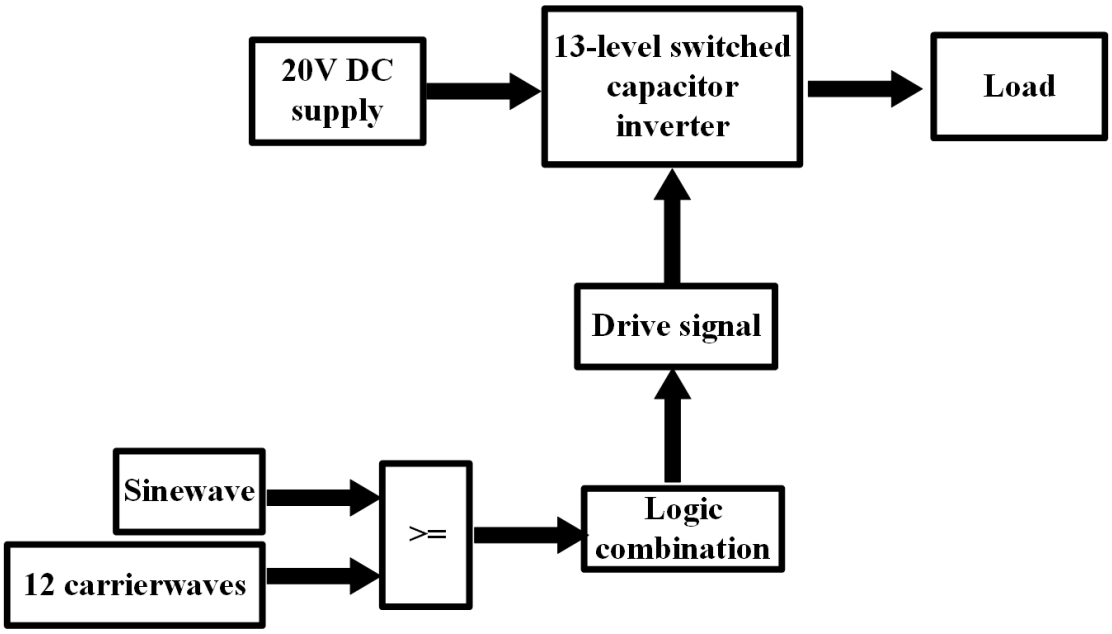


Fig 4.11 Block diagram of the simulation

4.7 Simulation results

The simulation model of the proposed topology has been built above, and detailed parameters have been given. The simulation results will be discussed in this part. The gate signals of the switches generated by the control logic shown in figure 4.12. By comparing it with the operating principle of the proposed topology, it is known that the

gate signals generated by the control logic of the simulation are the same as the principle, proving the accuracy of the control part in the simulation. It also indirectly proves the correctness of the simulation experiment results.

As the proposed topology is a symmetrical structure, when the inverter outputs the positive half-cycle voltage, the voltage stress of the off-state switch corresponds on a one-to-one basis to that of the negative half-cycle. The voltage stress on the switches is shown in figure 4.13. Among them, the maximum voltage stress of switches S1, S2, S5, S8, S9, S10, and S13 is equal to the DC supply. The maximum voltage stress of switches S3 and S4 is $1/2V_{dc}$. The maximum voltage stress of S11 and S12 is $2V_{dc}$. Switches S6 and S7 have the maximum voltage stress in the entire topology. They need to withstand a voltage of $3V_{dc}$. Compared with the topology, using the H-bridge to polarity reverse requires at least four switches to withstand the maximum voltage stress. The proposed topology only needs two switches. This proves that the proposed topology using symmetrical structures can reduce voltage stress.

Figure 4.14 and figure 4.15 show the output voltage, current and total harmonic distortion (THD) of the inverter operating under purely resistive and resistive-inductive loads with the proposed topology, respectively. When the proposed inverter operates with a resistive load, the output voltage has a 3-times boost and 13 levels. This is the same as the design. Further, when the proposed inverter operates with the resistive-inductive load, the output voltage still meets the design requirements, and the output current becomes a smooth sinusoidal waveform, proving that the proposed topology has good inductive load capability. Furthermore, resistive and resistive-inductive loads have little impact on the THD of the inverter output waveform. They are both kept below 10%.

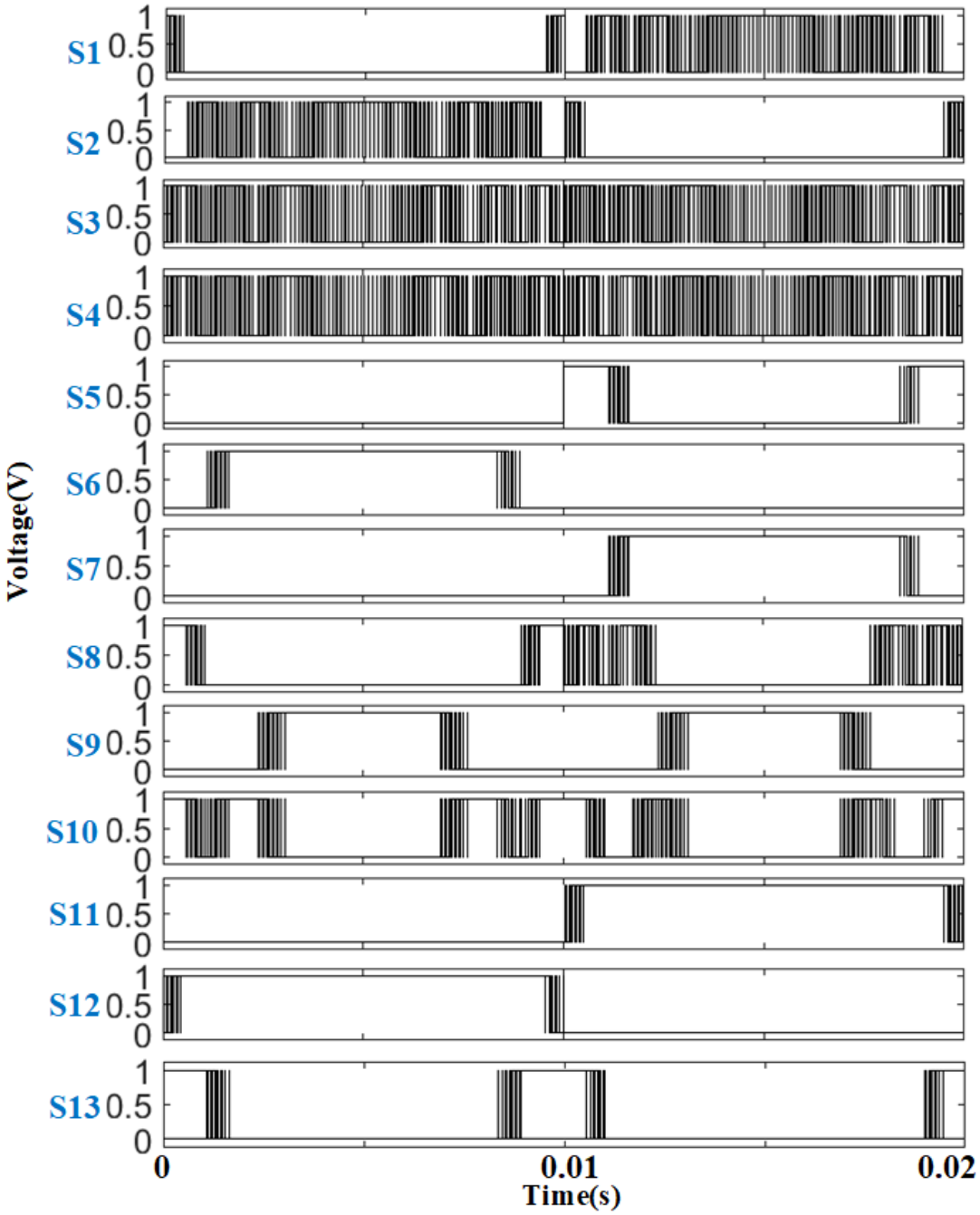


Fig 4.12 Gate signals of switches S1-S13

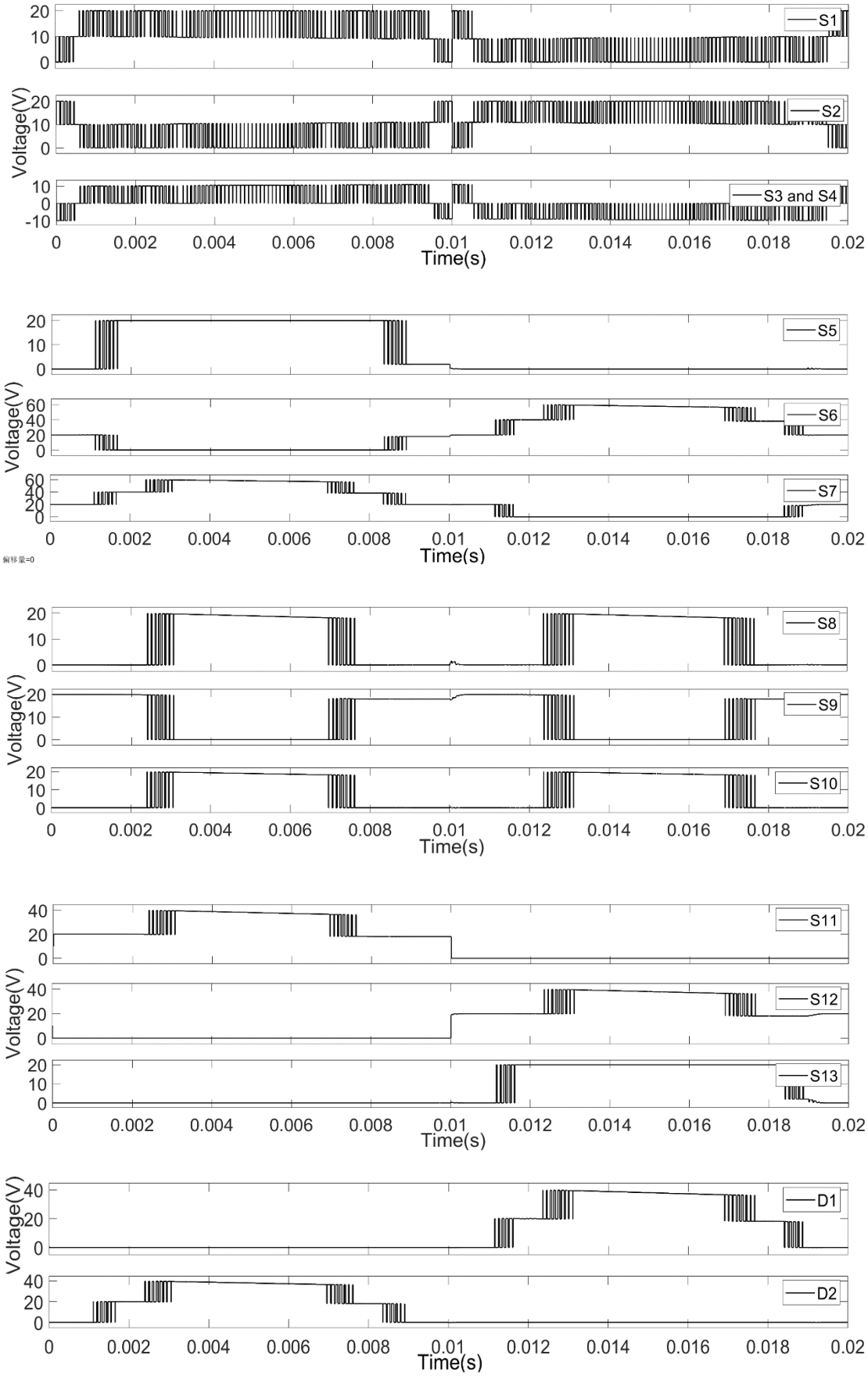
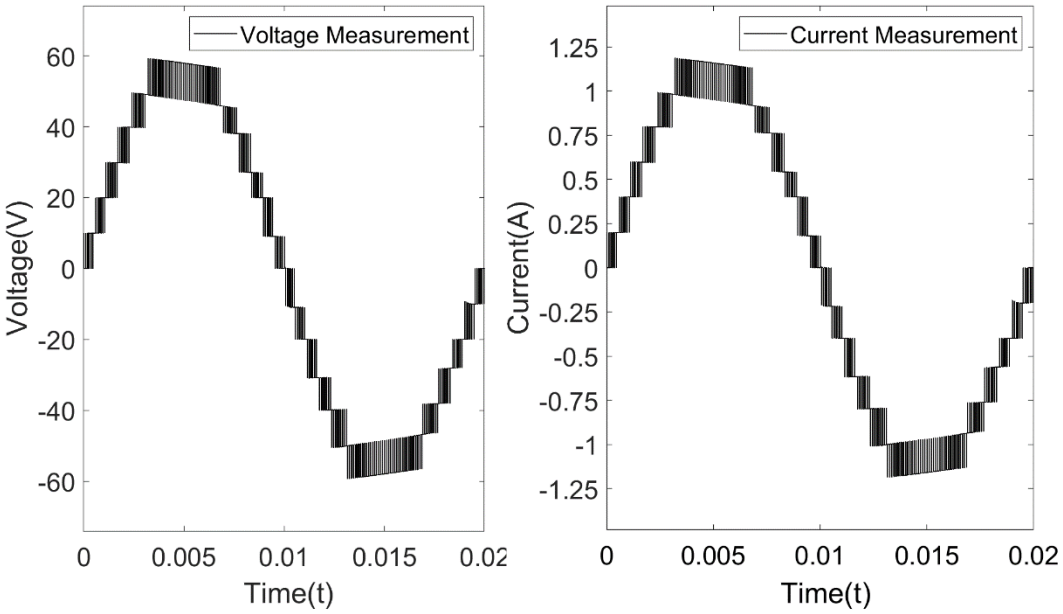
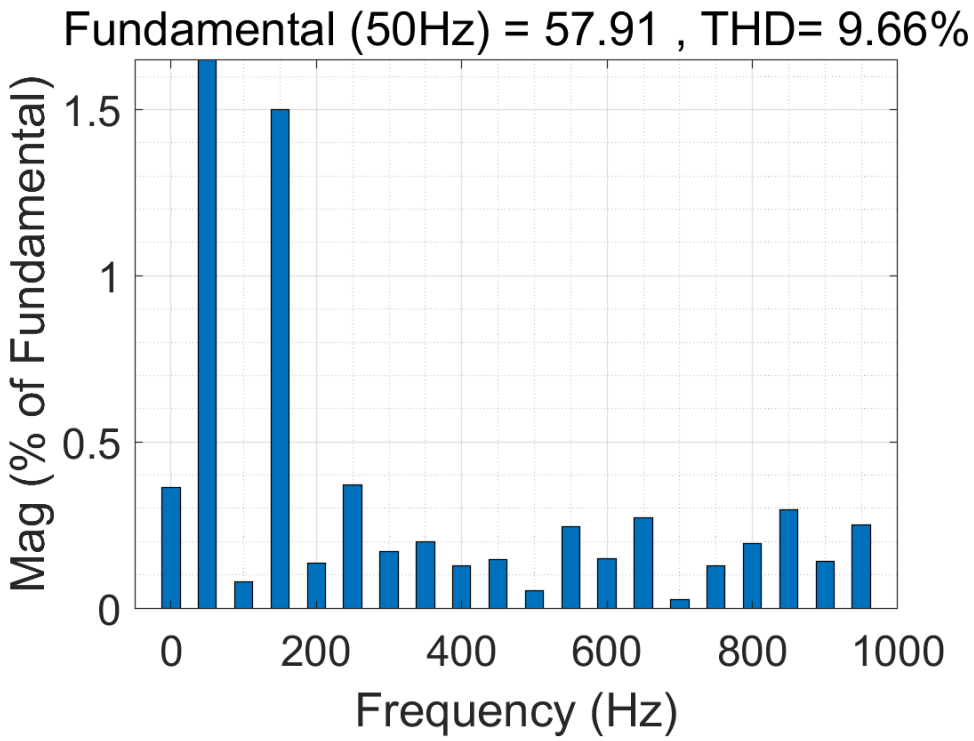


Fig 4.13 Voltage stress of the switches and diodes

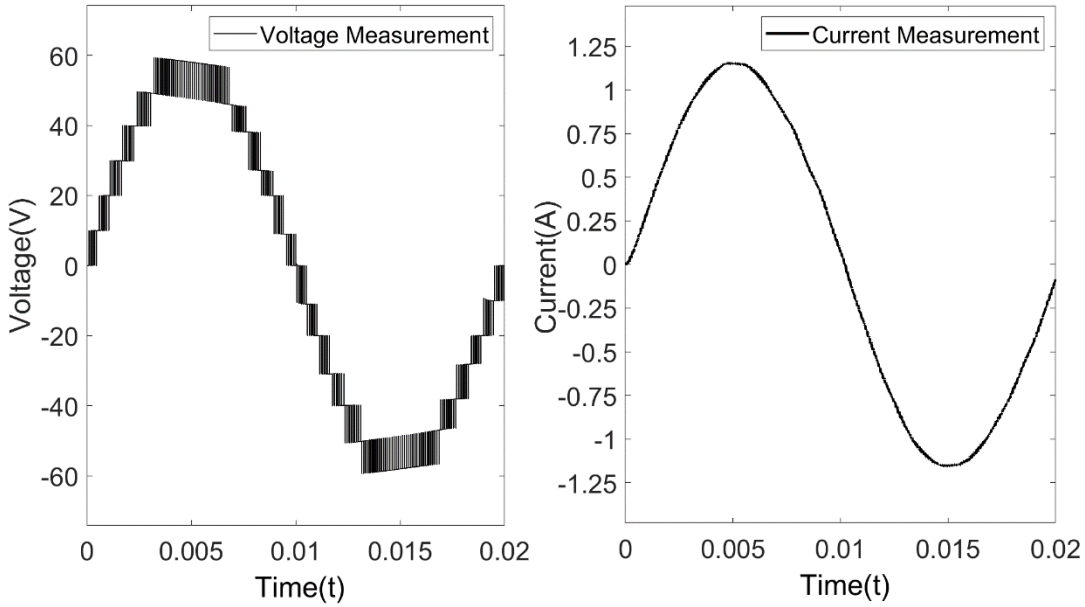


(a)

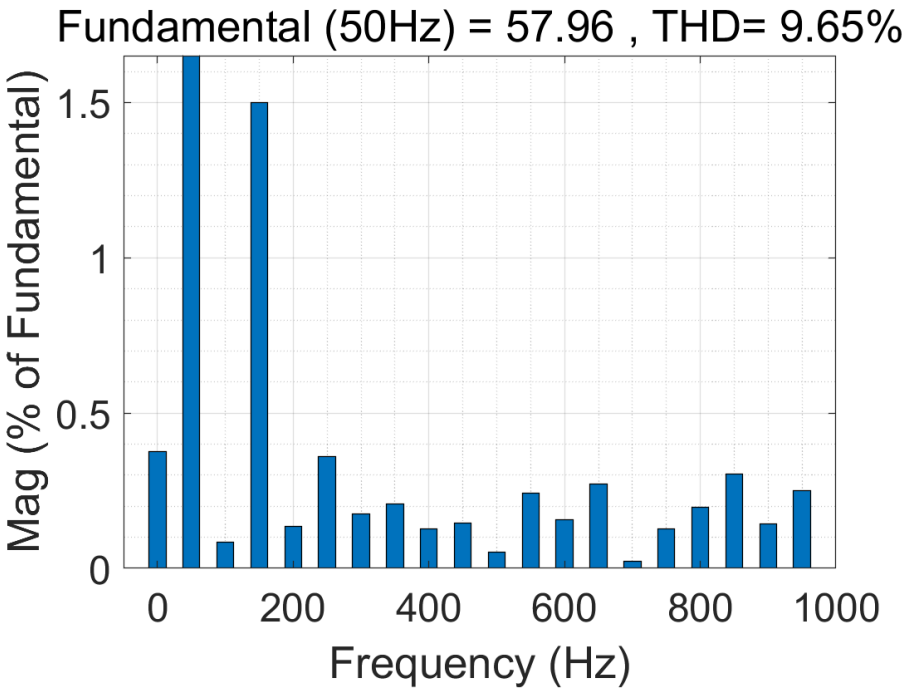


(b)

Fig 4.14 Simulation result for R-load (a) output voltage and current (b) THD



(a)



(b)

Fig 4.15 Simulation result for RL-load (a) output voltage and current (b) THD

4.8 Simulation result of the extension topology

As shown in the figure 4.16, the proposed 13-level topology has been extended by connecting two series/parallel structures to increase the number of output voltage levels and the gain of the inverter. The topology achieves 21 output voltage levels and 5 times

of voltage gain.

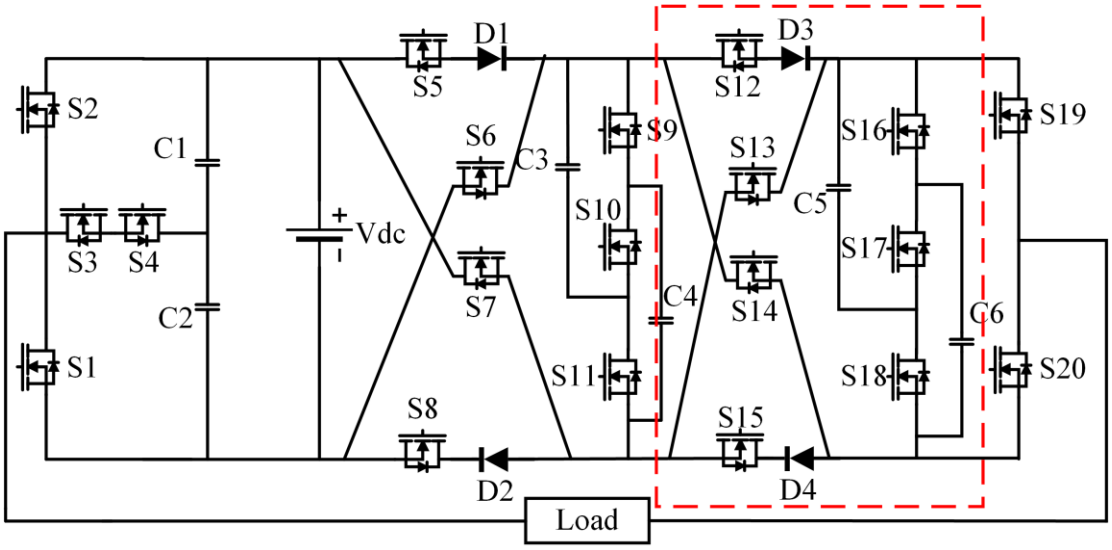
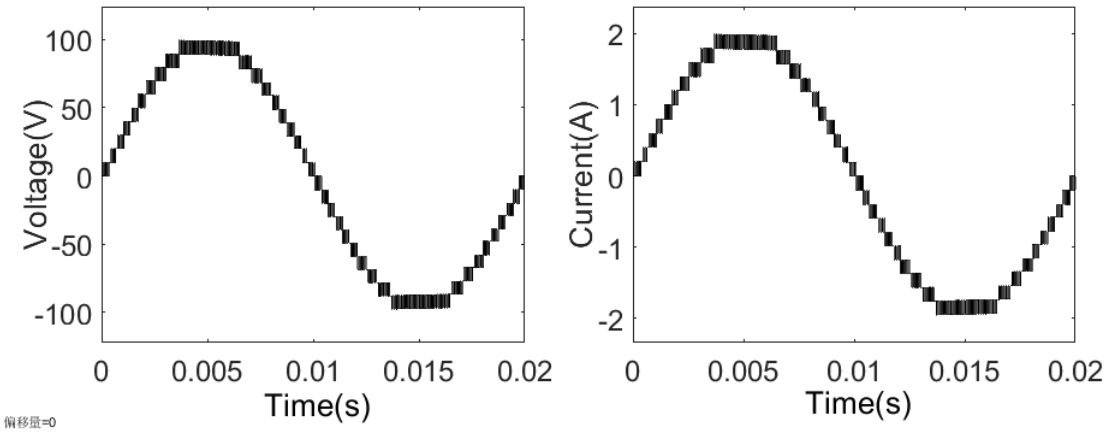


Fig 4.16 Topology of extended 21-level switched capacitor inverter

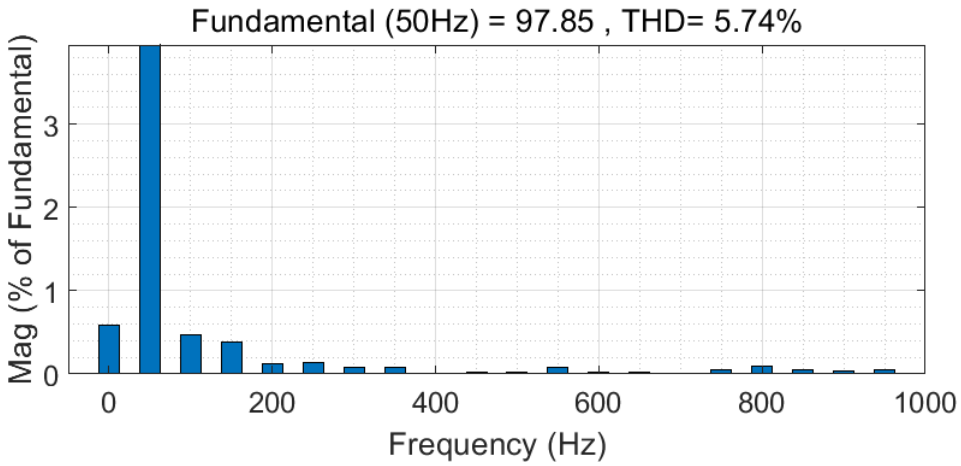
The simulation parameters of proposed 21-level SCMLI is shown in table 4.3 and the simulation result is shown in figure 4.17 and figure 4.18. Simulation results validate that by connecting an additional series/parallel switched capacitor unit into the topology, the output voltage of the inverter increases by 8 levels and voltage gain increases by 2 times.

Frequency of the sine wave (f_{ref})	50Hz
Frequency of the carrier wave (f_c).)	20kHz
V_{dc}	20V
Capacitance of capacitor C1	1500uF
Capacitance of capacitor C2	1500uF
Capacitance of capacitor C3	2600uF
Capacitance of capacitor C4	2600uF
Capacitance of capacitor C5	2600uF
Capacitance of capacitor C6	2600uF
Resister load R	50Ω
Inductance load L	5mH

Table 4.3 Simulation model parameters

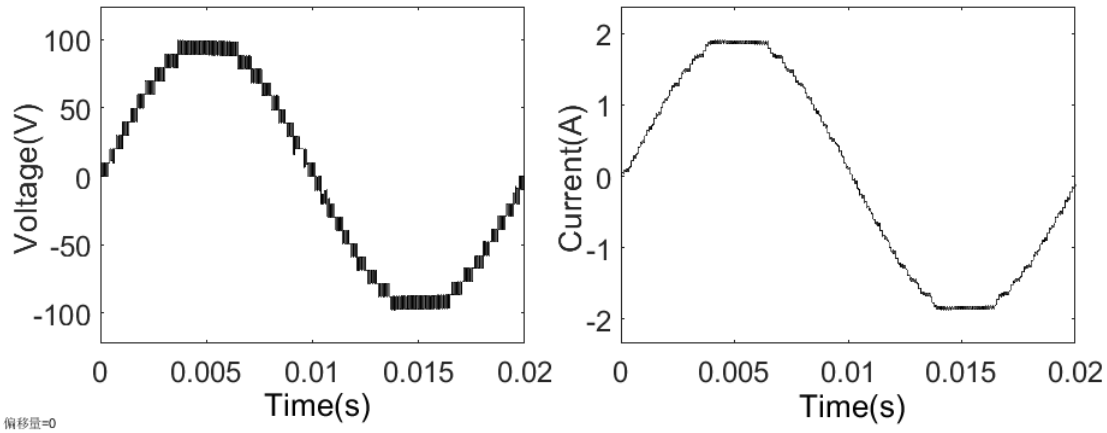


(a)

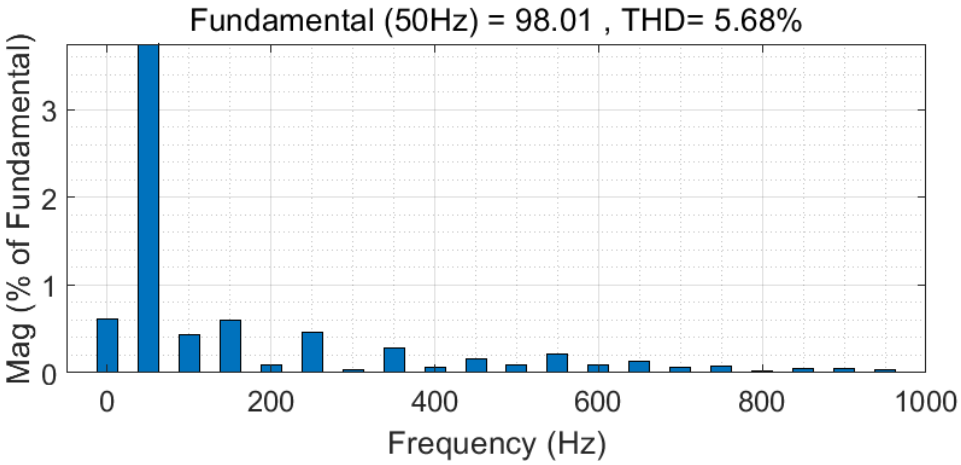


(b)

Fig 4.17 Simulation result of the extended topology under 50 Ω load. (a) Output voltage and current (b) Total harmonic distortion



(a)



(b)

Fig 4.18 Simulation result of the extended topology under 50 Ω and 5mH load. (a) Output voltage and current (b) Total harmonic distortion

4.9 Configuration of a novel 17-level switched capacitor inverter

The above-mentioned 13-level inverter is composed of a T-type structure and a Series/parallel capacitor structure. The advantage of this structure is that it uses fewer switching devices to obtain more levels and higher voltage gain. However, the DC supply only charges the capacitor and does not participate in the inverter circuit. Therefore, the 17-level SCMLI proposed in this section is improved based on the 13-level SCMLI. And the new topology is shown in figure 4.19.

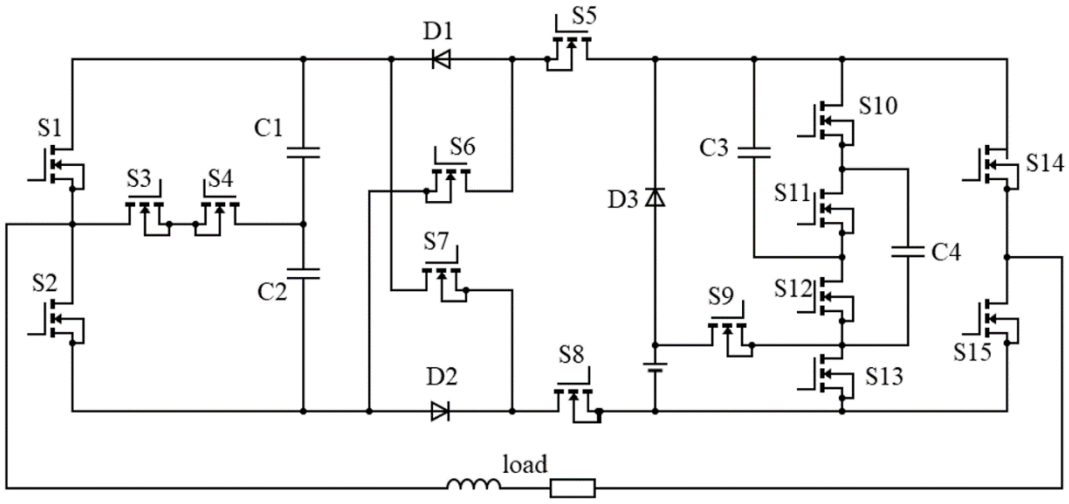


Fig 4.19 Topology of the 17-level SCMLI

The proposed topology uses 15 switches, 3 diodes and 4 capacitors to achieve 17 levels

of output voltage and 4 times voltage boost. The position of the DC supply in the topology is re-planned so that the DC supply participates in the voltage output of the inverter.

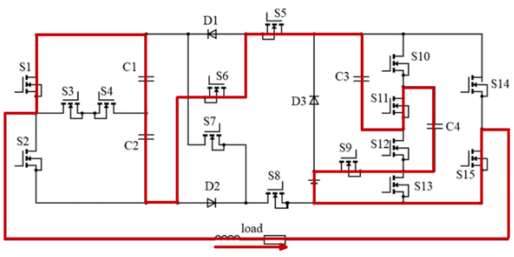
4.10 Operation principle

Different from the previously proposed 13-level SCMLI, the 17-level SCMLI proposed here has five devices that can discharge to the load. They are capacitors C1, C2, C3, C4 and DC supply. Among them, C1 and C2 can be connected in series and then charged in parallel with DC supply. The charging voltage of each capacitor is 1/2Vdc. C3 and C4 are respectively charged in parallel with DC supply. The charging voltage is Vdc. Therefore, the minimum output voltage of the proposed inverter is $1/2V_{dc}$. At this time, only C1 or C2 discharges to the load alone. The maximum output voltage of the inverter is $4V_{dc}$. In this case, four capacitors and the DC supply are connected in series to discharge to the load.

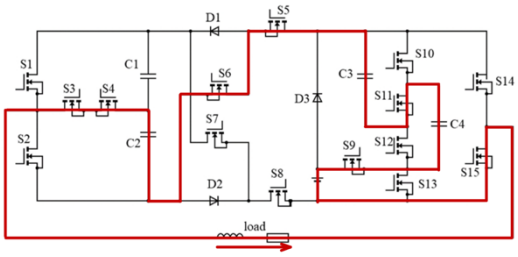
The 17 switching states of the proposed 17-level SCMLI are shown in Table 4.4. The “C” and “D” in the table indicate the charging state and discharging state of the capacitors, respectively. Correspondingly, the inverter has 17 operating modes according to the switching state. The inverter operating circuit of each mode is shown in figure 4.20, in which the current path and capacitor discharge path of the corresponding mode are marked with blue lines, and the red line represents the charging path of the capacitors.

U_o	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	C1	C2	C3	C4
+4Vdc	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	D	D	D	D
+7/2Vdc	0	0	1	1	1	1	0	0	1	0	1	0	0	0	1	-	D	D	D
+3Vdc	1	0	0	0	1	0	0	0	1	0	1	0	0	0	1	-	-	D	D
+5/2Vdc	0	0	1	1	1	0	0	0	1	0	1	0	0	0	1	C	-	D	D
+2Vdc	0	1	0	0	1	0	0	0	1	0	1	0	0	0	1	C	C	D	D
+3/2Vdc	0	0	1	1	1	1	0	0	0	1	0	1	1	0	1	-	D	C	C
+Vdc	1	0	0	0	1	0	0	1	0	1	0	1	1	0	1	C	C	C	C
+1/2Vdc	0	0	1	1	1	0	0	1	0	1	0	1	1	0	1	C	C	C	C
+0Vdc	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	-	-	-	-
-0Vdc	0	1	0	0	0	0	0	1	0	0	0	0	0	0	1	-	-	-	-
-1/2Vdc	0	0	1	1	1	0	0	1	0	1	0	1	1	1	0	C	C	C	C
-Vdc	0	1	0	0	1	0	0	1	0	1	0	1	1	1	0	C	C	C	C
-3/2Vdc	0	0	1	1	0	0	1	1	0	1	0	1	1	1	0	D	-	C	C
-2Vdc	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	C	C	D	D
-5/2Vdc	0	0	1	1	0	0	0	1	1	0	1	0	0	1	0	-	C	D	D
-3Vdc	0	1	0	0	0	0	1	1	1	0	1	0	0	1	0	-	-	D	D
-7/2Vdc	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	D	-	D	D
-4Vdc	0	0	1	0	0	0	1	1	1	0	1	0	0	1	0	D	D	D	D

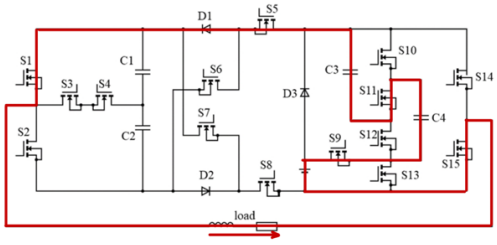
Table 4.4 Switching states of 17-level SCMLI



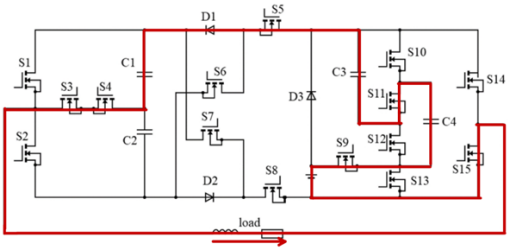
(a) $+4V_{dc}$



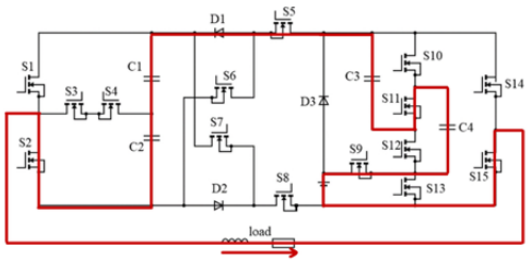
(b) $+3.5V_{dc}$



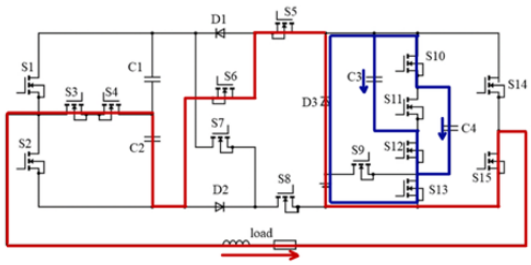
(c) $+3V_{dc}$



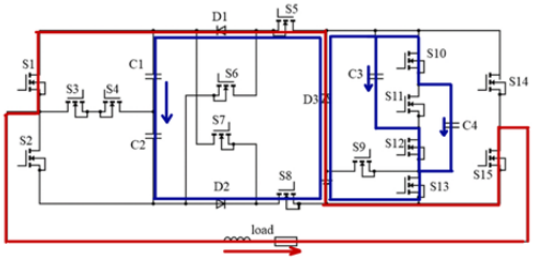
(d) $+2.5V_{dc}$



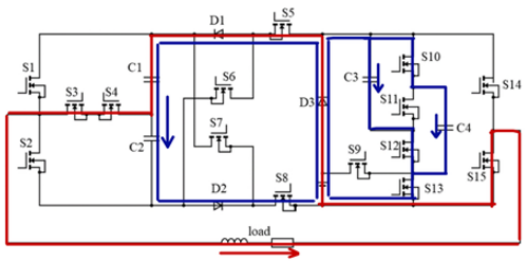
(e) $+2V_{dc}$



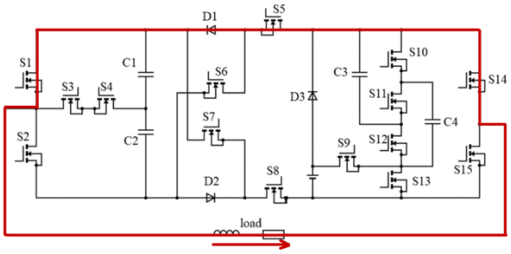
(f) $+1.5V_{dc}$



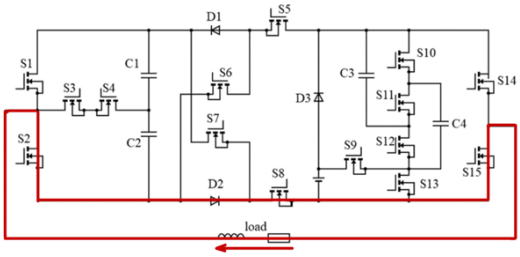
(g) $+V_{dc}$



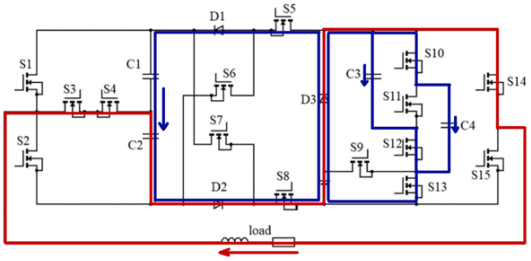
(h) $+0.5V_{dc}$



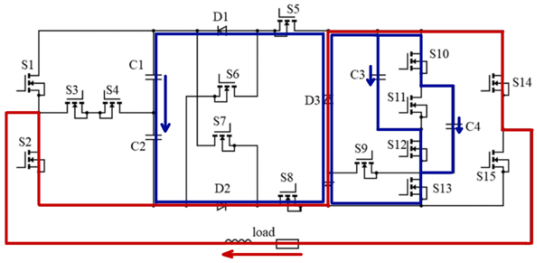
(i) $+0V_{dc}$



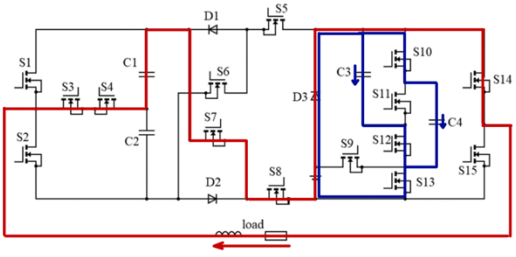
(j) $-0V_{dc}$



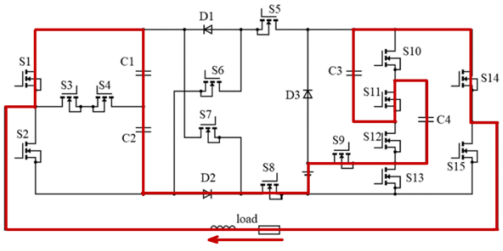
(k) $-0.5V_{dc}$



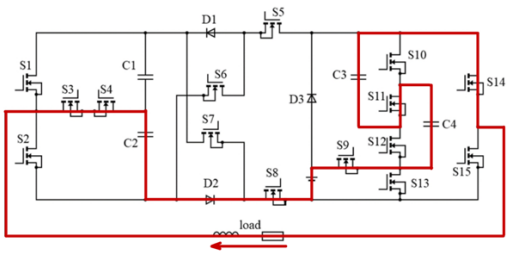
(l) $-V_{dc}$



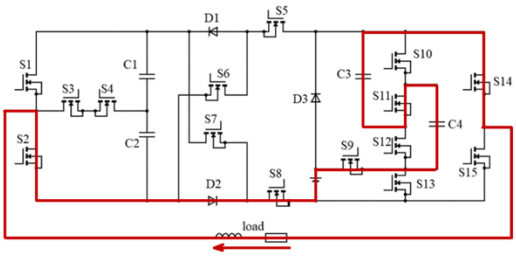
(m) $-1.5V_{dc}$



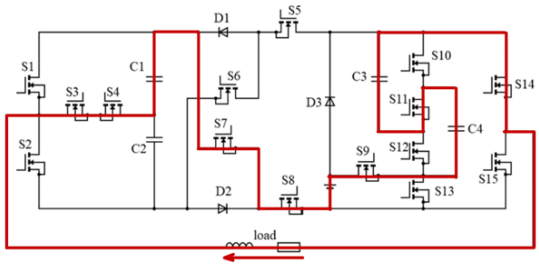
(n) $-2V_{dc}$



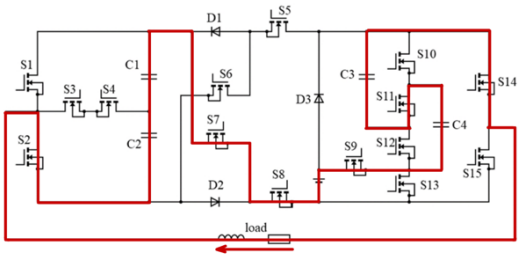
(o) -2.5V_{dc}



(p) -3V_{dc}



(q) -3.5V_{dc}



(r) -4V_{dc}

Fig 4.20 Operating modes of 17-level SCMLI

The operating modes are described below:

Mode1(+4V_{dc}): In this mode, the switches S1, S5, S6, S9, S11, and S15 are ON state, and the capacitors C1, C2, C3, and C4 are series connected with the DC Supply to discharge to the load. In this case, the diode D1 is reverse-biased by the voltage across C1 and C2. Since S9 and S11 are in conduction, the voltage of capacitors C3 and C4 across in reverse on D3, making D3 in a reverse biased state.

Mode2((+7/2V_{dc}): In this mode, the switches S4, S5, S6, S9, S11, and S15 are ON state, and the capacitors C2, C3 and C4 are series connected to discharge to the load. In this case, the diode D1 is reverse-biased. That is because the voltage of C1 appears directly across D1 in a reverse way. And the diode D3 is reverse-biased by the voltage across C3 and C4.

Mode3 (+3V_{dc}): In this mode, the switches S1, S5, S9, S11 and S15 are ON state, and the capacitors C3 and C4 are series connected and discharged to the load. The diode D3

is reverse biased by the voltage across C3 and C4.

Mode4 (+5/2V_{dc}): In this mode, the switches S3, S4, S5, S9, S11, and S15 are ON state, capacitors C3 and C4 are series connected to the DC supply and discharge to the load. In this state, C1 is charged by C3, C4 and DC supply.

Mode5 (+2V_{dc}): In this mode, the switches S2, S5, S9, S11 and S15 are in the ON state, and the capacitors C3 and C4 are series connected to the DC supply and discharge to the load. In this state, capacitors C1 and C2 are series connected and charged by C3, C4 and DC supply.

Mode6 (+3/2V_{dc}): In this mode, the switches S3, S4, S5, S6, S10, S12, S13 and S15 are ON state. The capacitor C2 are series connected with the DC supply and discharge to the load. The capacitors C3 and C4 are parallel connected with the DC supply and charged to V_{dc} respectively. In this case, the diode D1 is reversed biased, and the D3 is in conduction.

Mode7 (+V_{dc}): In this mode, the switches S1, S5, S8, S10, S12, S13, and S15 are ON state, and only the DC supply is connected to the load. Capacitors C1 and C2 are connected in series and charged in parallel with the DC supply and each capacitor is charged to 1/2V_{dc}. Capacitors C3 and C4 are parallel connected with the DC supply and charged to V_{dc} respectively. Moreover, all the diodes are in conduction.

Mode8 (+1/2V_{dc}): In this mode, the switches S3, S4, S5, S8, S10, S12, S13, S15 are ON state. In the current path, the DC supply charges the capacitor C1 to 1/2V_{dc} and then discharges to the load. In the capacitor charging path, capacitors C1 and C2 are connected in series and charged in parallel with the DC supply and each capacitor is charged to 1/2V_{dc}. Capacitors C3 and C4 are parallel connected with the DC supply and charged to V_{dc} respectively. All the three diodes are in conduction.

Mode9 (0): In this mode, the 0 level can be divided into the +0 interval and the -0 interval, depending on whether the 0 level is in the positive or negative half cycle of the output voltage. For the +0 interval, the switches S1, S5, and S14 are in the ON state. For the -0 interval, the switches S2, S8, and S15 are in the ON state.

Mode10 (-1/2V_{dc}): In this mode, the switches S3, S4, S5, S8, S10, S12, S13 and S14 are ON state. All the capacitors are connected to the DC supply to be charged. The DC supply charges the capacitor C2 first and then discharges to the load.

Mode11 (-V_{dc}): In this mode, the switches S2, S5, S8, S10, S12, S13 and S14 are ON state. All the capacitors are connected to the DC supply to be charged. Only the DC supply charges to the load.

Mode12 (-3/2V_{dc}): In this mode, the switches S3, S4, S7, S8, S10, S12, S13 and S14 are ON state. The capacitor C1 and DC supply are connected in series and discharge to the load. The capacitor C3 is parallel connected with the DC supply through switches S12 and S13 and charged to V_{dc}. The capacitor C4 is parallel connected with the DC supply through switches S10 and S13 and charge to V_{dc}. The diode D2 is reverse biased, and the diode D3 is in conduction.

Mode13 (-2V_{dc}): In this mode, the switches S1, S8, S9, S11 and S14 are ON state. The capacitors C3 and C4 are series connected with the DC supply and charge the capacitor C1 and C2 through load.

Mode14 (-5/2V_{dc}): In this mode, the switches S3, S4, S8, S9, S11 and S14 are ON state. The capacitors C3 and C4 are series connected with the DC supply and charge the capacitor C2 through load.

Mode15 (-3V_{dc}): In this mode, the switches S2, S8, S9, S11 and S14 are ON state. The

capacitors C3 and C4 are series connected to the DC supply and discharge to the load. The diode D2 is in conduction, and the diode D3 is reverse biased.

Mode16 (-7/2V_{dc}): In this mode, the switches S3, S7, S8, S9, S11 and S14 are ON state. The capacitors C1, C3 and C4 are series connected to the DC supply and discharge to the load. The diode D2 and D3 are reverse-biased.

Mode17 (-4V_{dc}): In this mode, the switches S2, S7, S8, S9, S1, and S14 are ON state. The capacitors C1, C2, C3, and C4 are connected to the DC supply and discharge to the load. The diode D2 and D3 are reverse-biased.

4.11 Modulation strategy

The PDPWM technology is used to control the proposed 16 triangle waves with the same frequency, phase, and amplitude, which are used to compare with the sine wave. And the arrangement of the waveform is shown in figure 4.21. Among them, U1-U8 and V1-V8 are pulse signals generated by comparing sine waves and triangle waves respectively. Each signal represents the modulation signal of the inverter output voltage within a certain voltage level. Therefore, according to the switching state given in Table 4.3, the gate signal of each switch can be obtained by logically combining the signals U1-U8 and V1-V8.

The gate signal of each switch can be expressed by the following equations:

S1= (U8) | (U6 & (~U7)) | (U2 & (~U3)) | (V5 & (~V4))

S2 = (U4 & (~U5)) | (U3 & (~U4)) | (U1 & (~U2)) | (V3 & (~V2)) | (V7 & (~V6)) | (V8 & (~V7))

S3 = (U7 & (~U8)) | (U5 & (~U6)) | (U3 & (~U4)) | (U1 & (~U2)) | (V2 & (~V1)) | (V4 & (~V3)) | (V6 & (~V5)) | (~V8)

S4 = S3

S5 = (U1) | (V2 & (~V1)) | (V3 & (~V2))

S6= (U8) | (U7 & (~U8)) | (U3 & (~U4))

S7= (V4 & (~V3)) | (V7 & (~V6)) | (~V8)

S8= (U2 & (~U3)) | (U1 & (~U2)) | (~V1)

S9 = (~V4) | (U4)

S10= (U3 & (~U4)) | (U2 & (~U3)) | (V3 & (~V2)) | (V4 & (~V3)) | (V2 & (~V1)) |

S11 = S9

S12 = S10 = S13

S14 = V1

S15 = U1

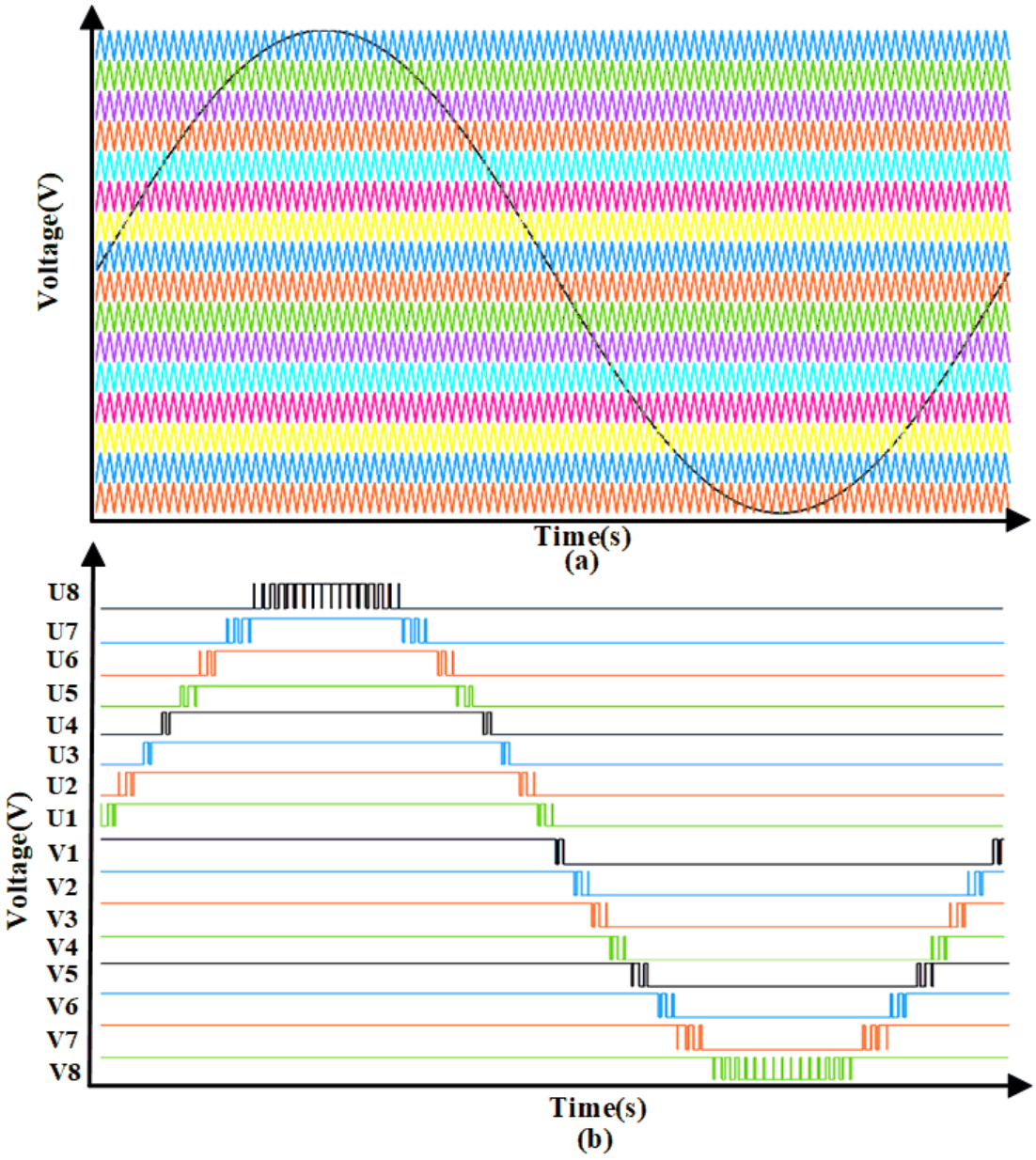


Fig 4.21 Principle of PDPWM (a) Waveform arrangement

(b) Waveform of $U_1 - U_6, V_1 - V_6$

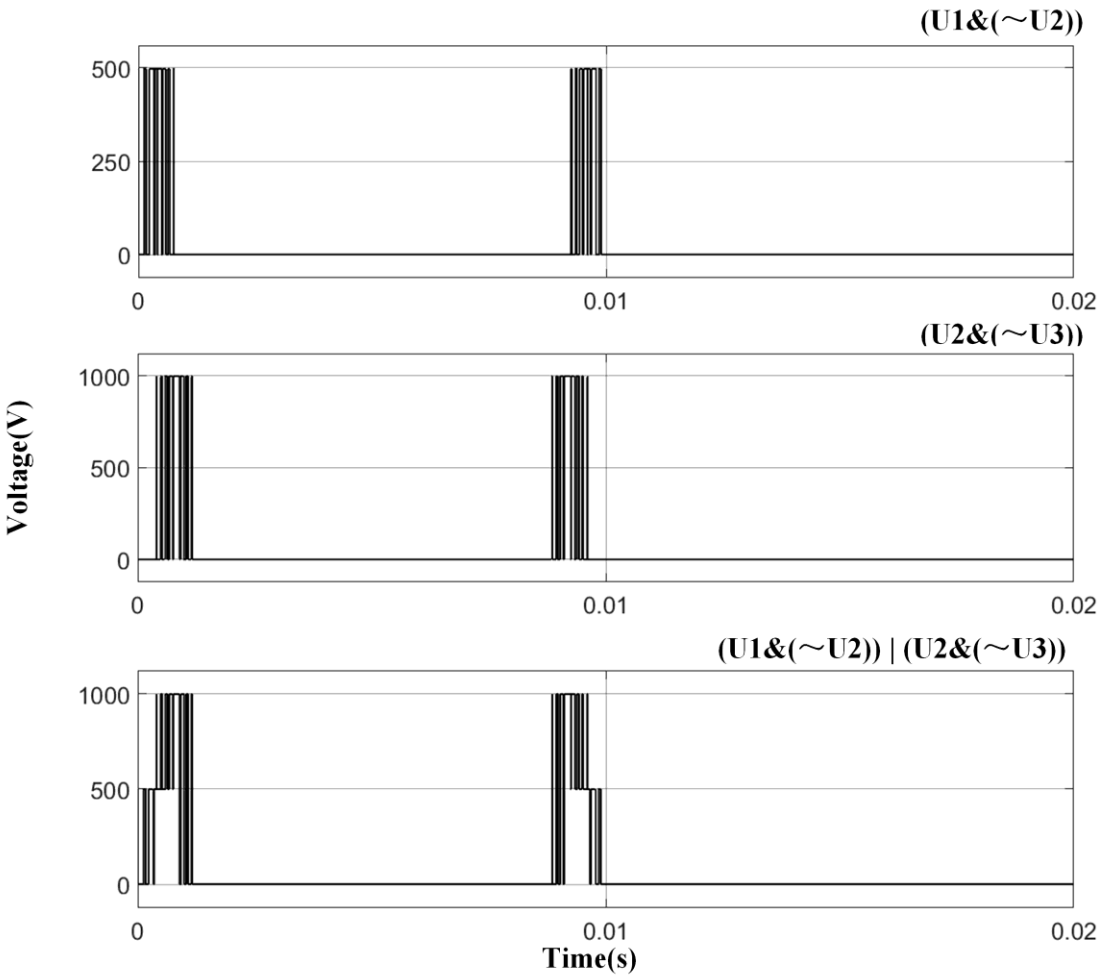


Fig 4.22 Output voltage levels of specific control signal

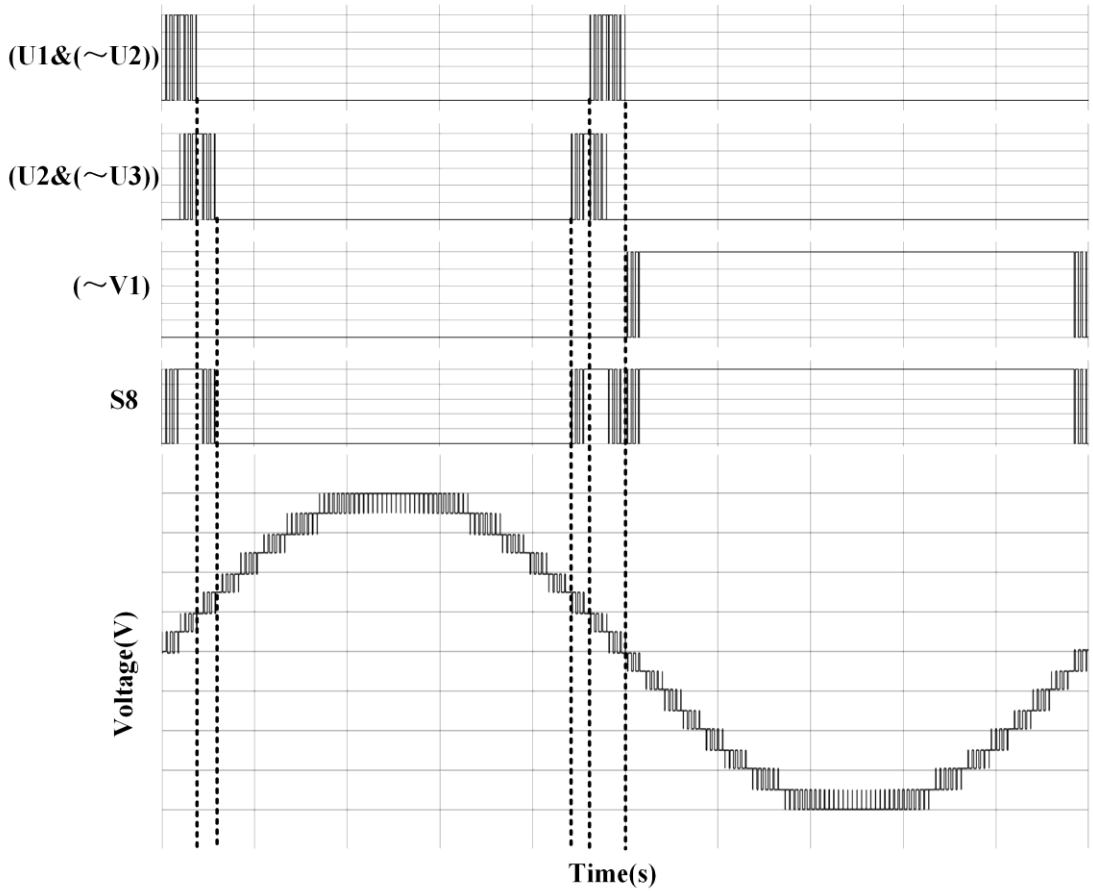


Fig 4.23 Switching signal of S8

The logic signal to control the inverter output corresponding level of voltage is shown in figure 4.22. The inverter output waveform corresponding to (U1 & (~U2)) is the first level. If the DC supply of the inverter is 1000V, the amplitude of the first level is 500V. Similarly, the signal (U2 & (~U3)) in figure 4.22 corresponds to the second level of the inverter output voltage, with an amplitude of 1000V. By combining these two signals, the inverter sequentially outputs first and second voltage levels.

Figure 4.23 illustrates the signal for switch S8. According to Table 4.3, S8 conducts when the inverter outputs are +Vdc, +1/2Vdc, and during the negative half-cycle. Thus, the control signals corresponding to these levels can be combined to generate the control signal for S8.

4.12 Capacitance calculation

Since the proposed topology is symmetrical, capacitors C1 and C2 charge and discharge symmetrically during the positive and negative half-cycles, and capacitors C3 and C4

discharge symmetrically during these cycles as well. Therefore, this section only analyzes the discharge states of C2 and C4 during the positive half-cycle to calculate the capacitance values.

Figure 4.24 shows the positive half-cycle waveform of the output voltage of the proposed 17-level SCMLI, and the corresponding capacitor discharge current waveform. From figure 4.24, it can be seen that the maximum discharge interval of capacitor C2 is from t_6 to t_9, while the maximum discharge interval of capacitor C4 is from t_3 to t_{12}. The maximum discharge current for both capacitors is 80 A. To ensure that the maximum voltage ripple of the capacitors remains below 10%, calculations based on equation 3.1 to equation 3.4 show that the capacitance value of C2 is 6700 µF and that of C4 is 4700 µF. The simulated capacitor voltage waveforms using these calculated values are shown in figure 4.25. From the figure, it can be observed that the voltage ripples of C2 and C4 both remain within 10%, verifying the accuracy of the calculations.

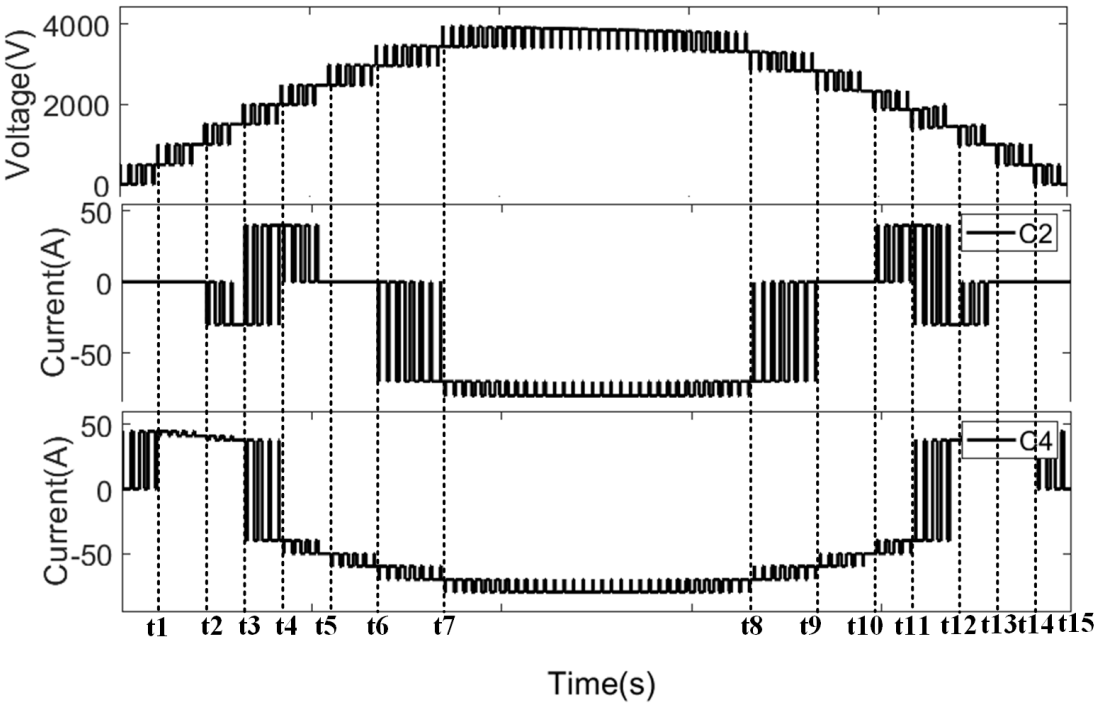


Fig 4.24 Positive half-cycle of the output voltage and discharge current of the capacitor C2 and C3

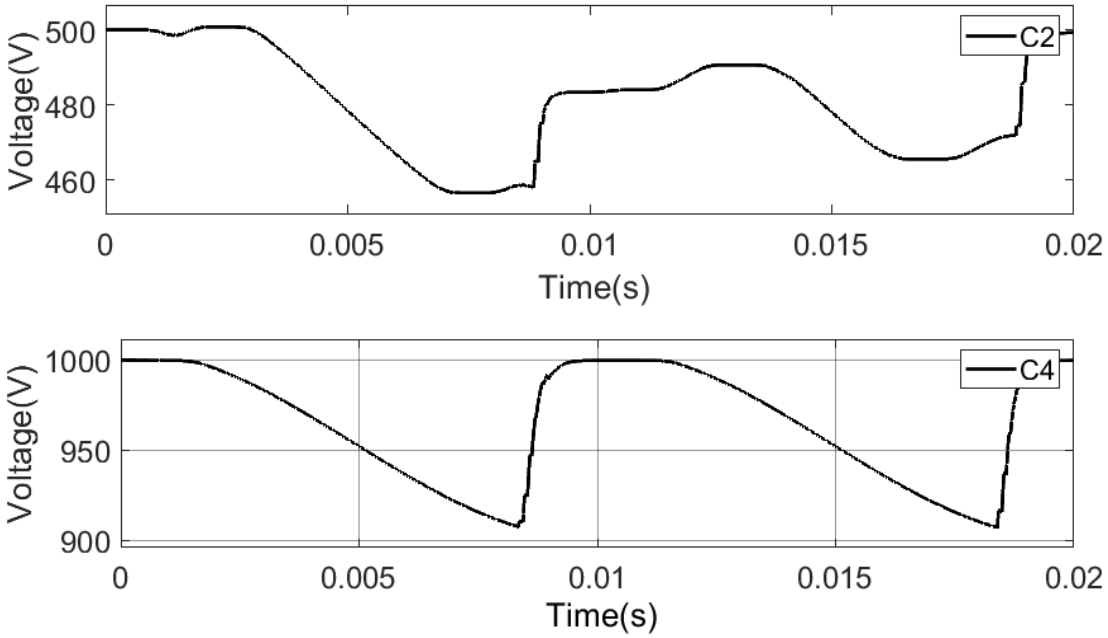


Fig 4.25 Voltage of capacitors C2 and C4

4.13 Simulation Setup

The control logic diagram is shown in figure 4.26. All the parameters are shown in Table 4.5.

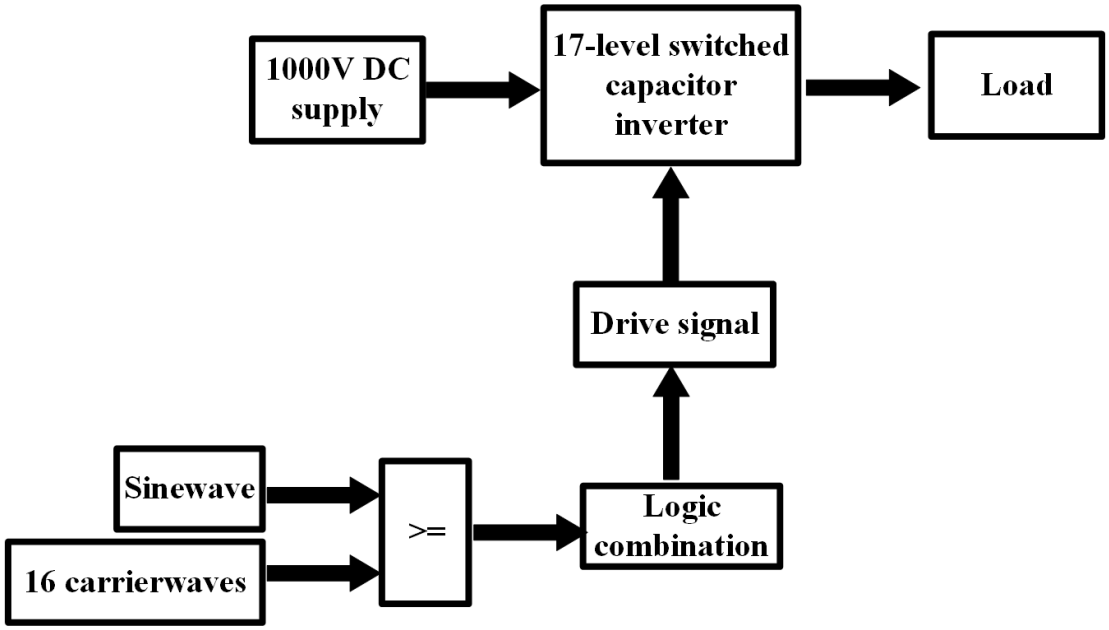


Fig 4.26 Block diagram of simulation

Frequency of the sine wave (f_{ref})	50Hz
Frequency of the carrier wave (f_c).)	20kHz
V_{dc}	1000V
Capacitance of capacitor C1	6700uF
Capacitance of capacitor C2	6700uF
Capacitance of capacitor C3	4700uF
Capacitance of capacitor C4	4700uF
Resister load R	50Ω
Inductance load L	5mH

Table 4.5 Simulation parameters

4.14 Simulation result

The simulation model is built above to verify the theoretical analysis of the proposed 17-level SCMLI. The simulation result will be shown following.

Figure 4.27 shows the gate signals in one cycle of the switches. It can be seen that the interval of the signals is the same as the theoretical principle, as shown in Table 4.3.

The voltage stress that the switch withstands is shown in figure 4.28. The switch voltage stress depends on the voltage of the parallel circuit of the switch when the switch is turned off. Therefore, when the DC supply of the proposed topology is 1000V, the voltage stress of switches S5, S8, S14, and S15 is the highest among all switches. And they will withstand a maximum voltage stress of 3000V. Secondly, the switches S1, S2, S6, S7, S9, S10, S11, S12 and S13in this topology withstands the maximum voltage stress of 1000V, which is equal to the DC supply. The switches with the smallest maximum stress are S3 and S4. The maximum voltage stress is 500V. This is because only capacitors C1 and C2 are connected in parallel with them when they are turned off. This also proves that the T-type structure can effectively reduce the voltage stress of the switches.

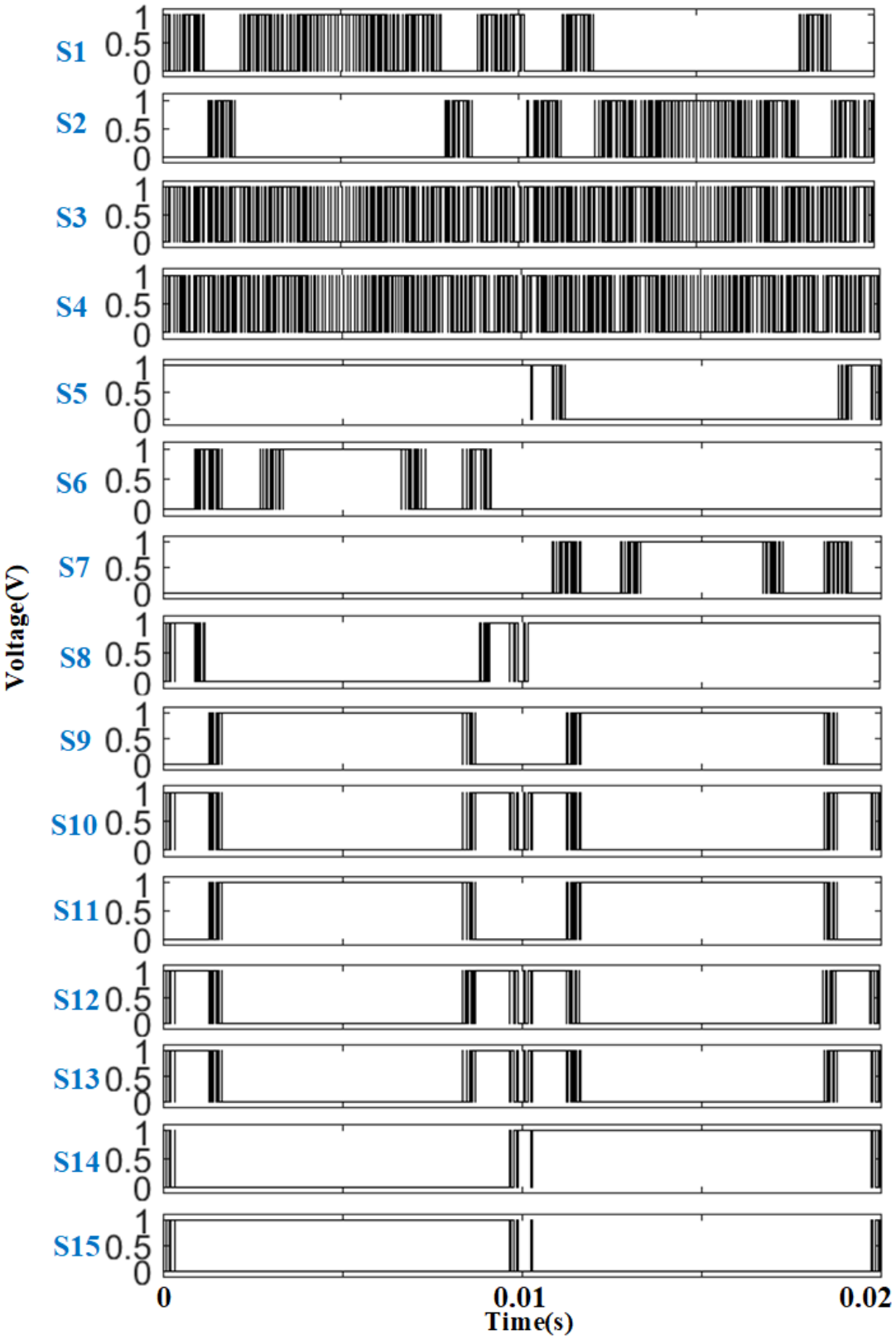


Fig 4.27 Gate signals of switched S1-S15

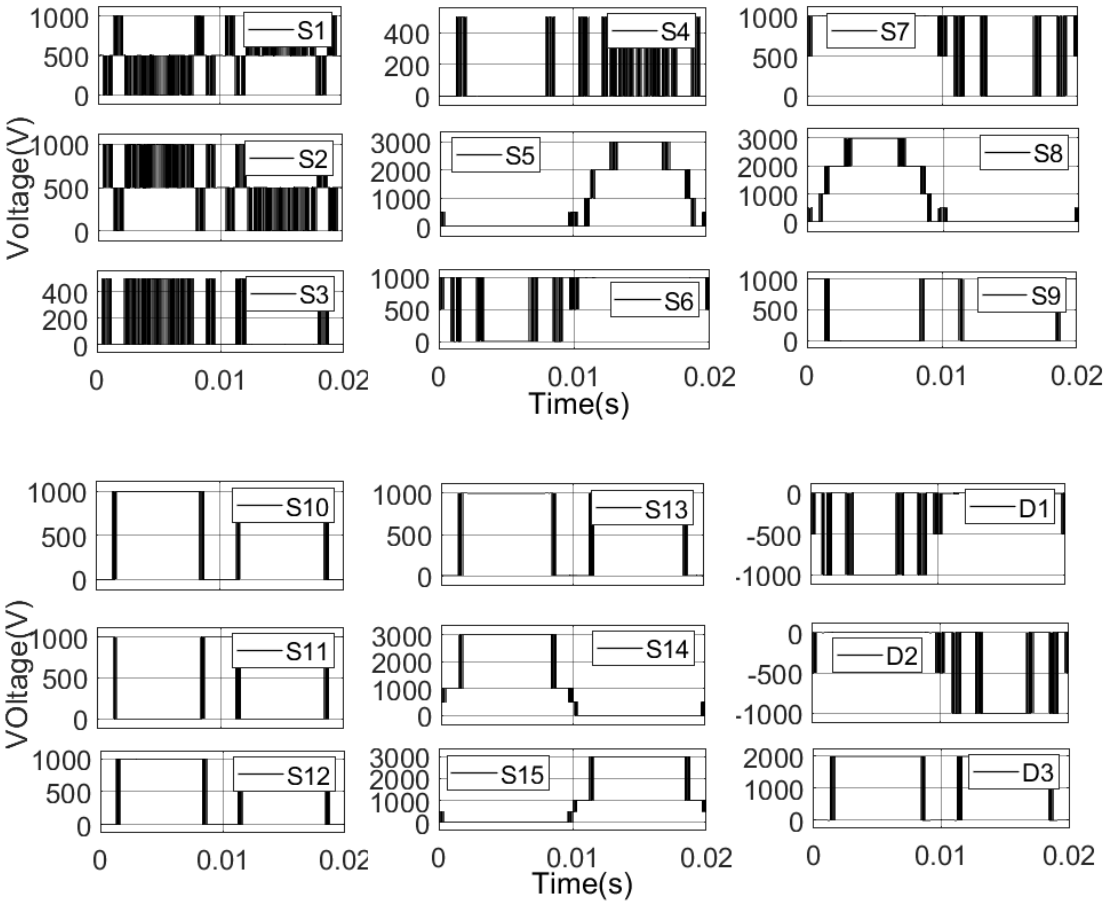
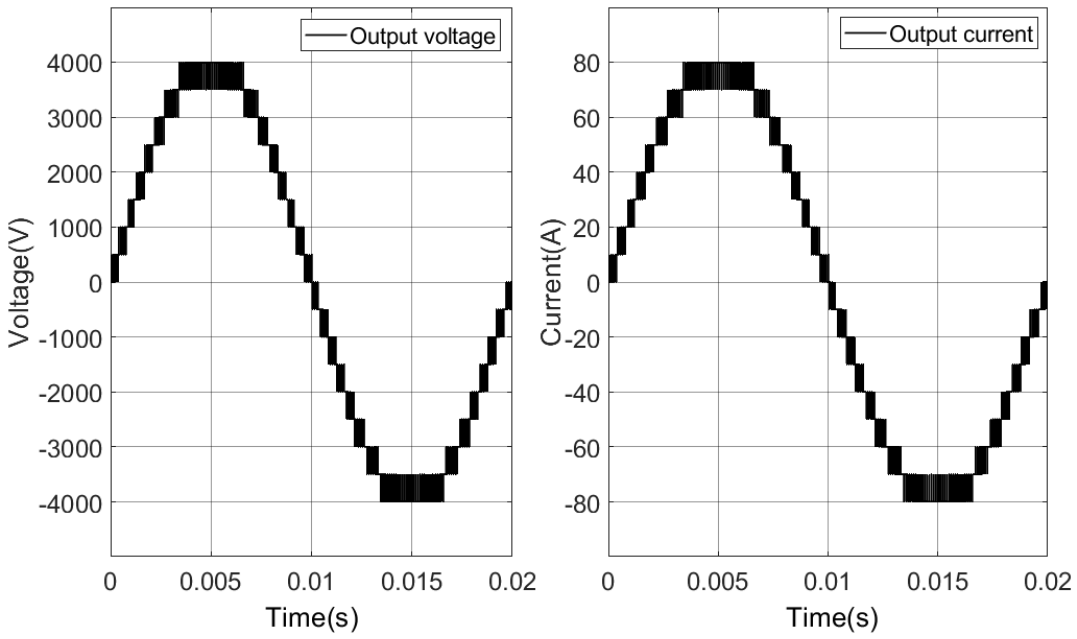


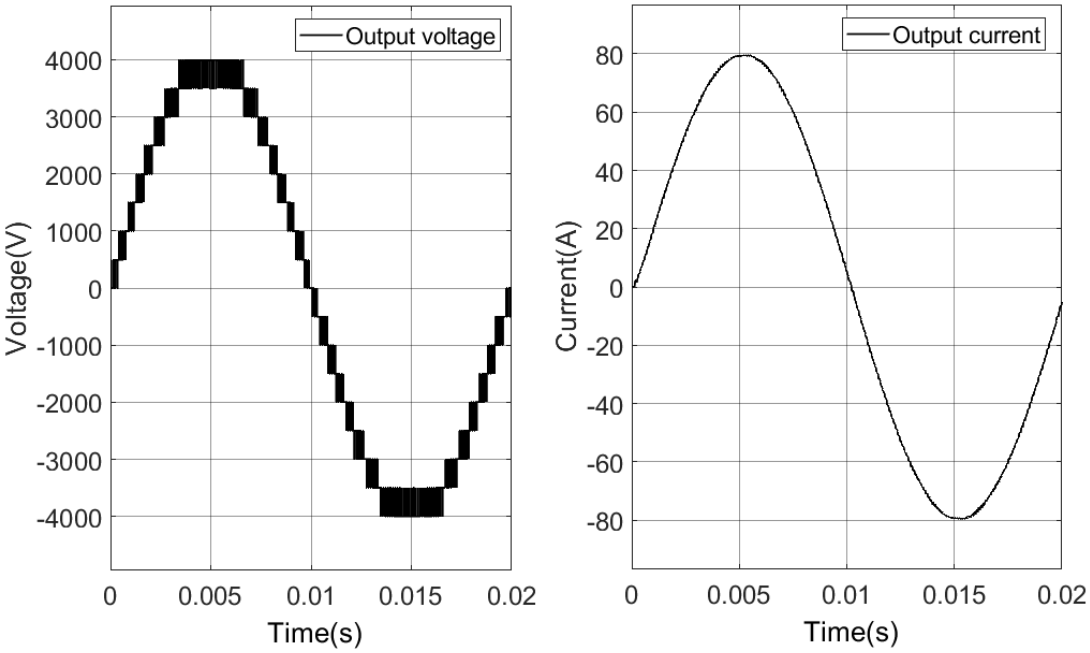
Fig 4.28 Voltage stress of switches and diodes

The proposed topology is tested with the resistive load and inductive-resistive load, and the output voltage and current are shown in figure 4.29.

When the proposed inverter operates with a resistive load, the output voltage has 4 times boost and 17 levels. This is the same as the design. Further, when the proposed inverter operates with the resistive-inductive load, the output voltage still meets the design requirements, and the output current becomes a smooth sinusoidal waveform, proving that the proposed topology has good inductive load capability.



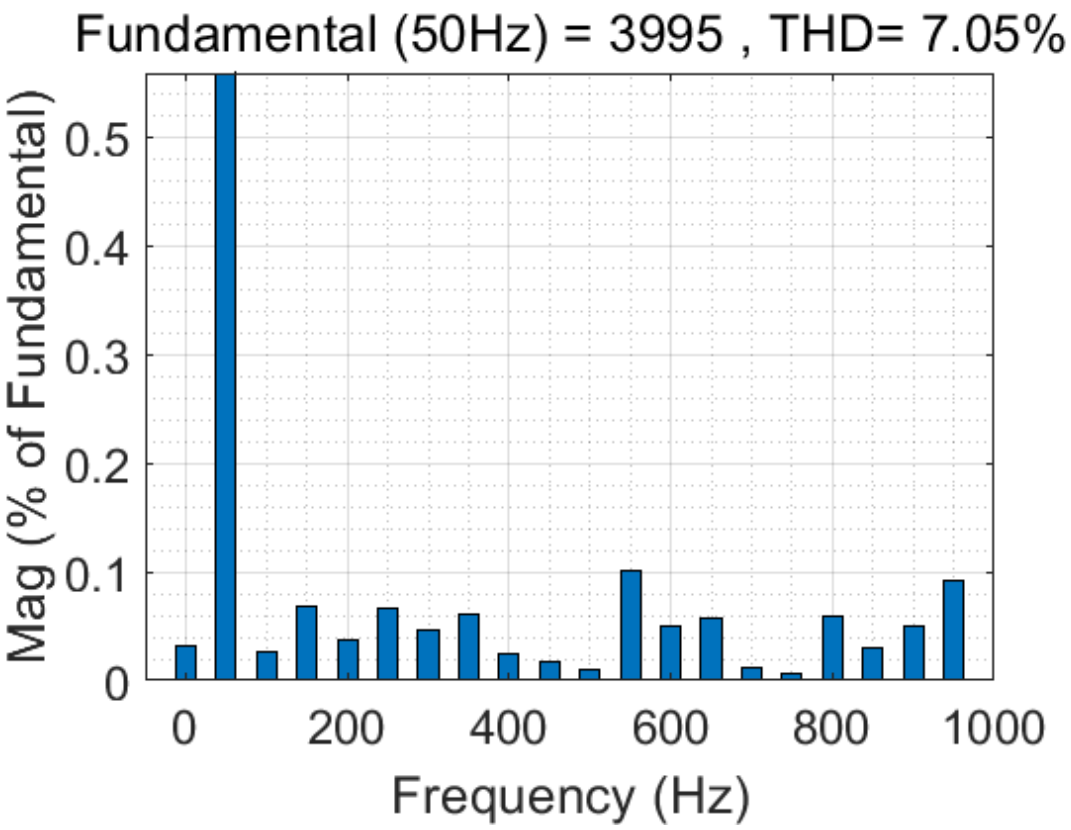
(a)



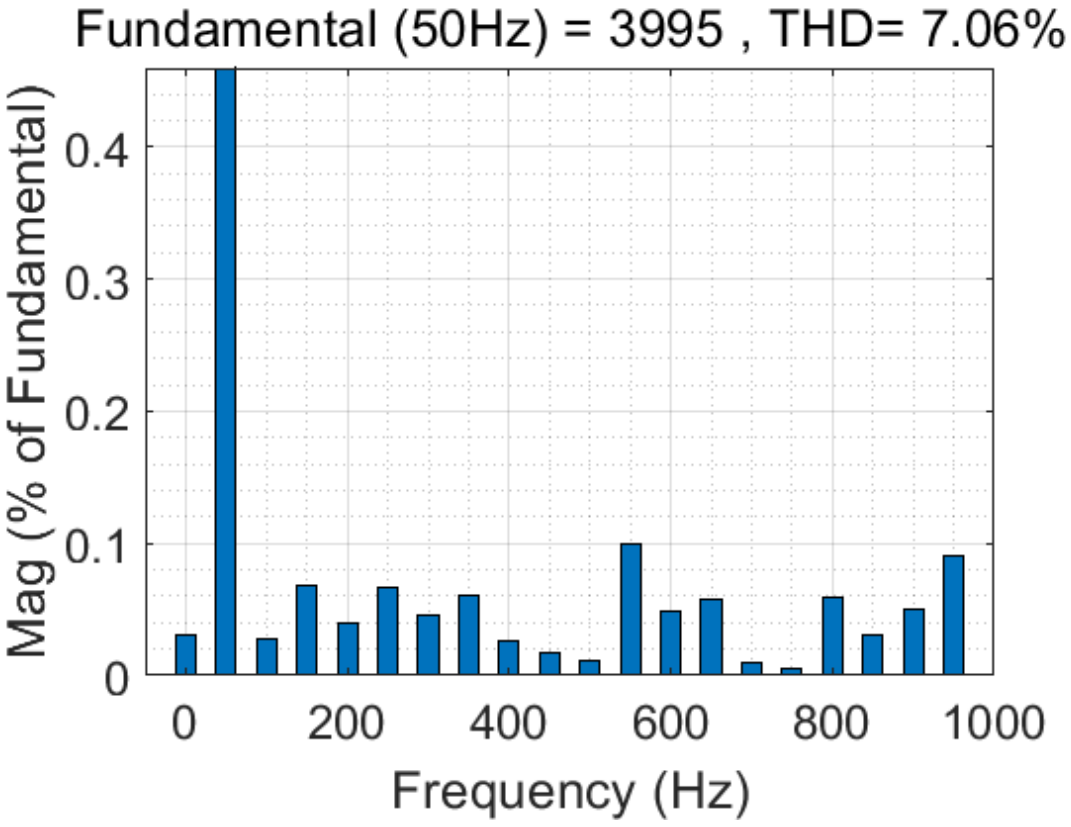
(b)

Fig 4.29 The output voltage and current of the proposed 17-level SCMLI with different load. (a) Resistive load (b) Resistive-inductive load

The total harmonic distortions (THD) of the proposed topology operating with resistive and resistive-inductive loads are shown in figure 4.30. It can be found that the THDs are always around 7%, which is relatively low.



(a)



(b)

Fig 4.30 Total harmonic distortion of output voltage of proposed 17-level SCMLI with different load. (a) Resistive load (b) Resistive-inductive load

4.13 Simulation result of the extended topology

As shown in figure 4.31, the proposed 17-level topology has been extended by cascading two series/parallel structures to increase the number of output voltage levels and the output voltage gain of the inverter. The topology shown in figure 4.31 achieves 25 output voltage levels and 6 times of voltage gain.

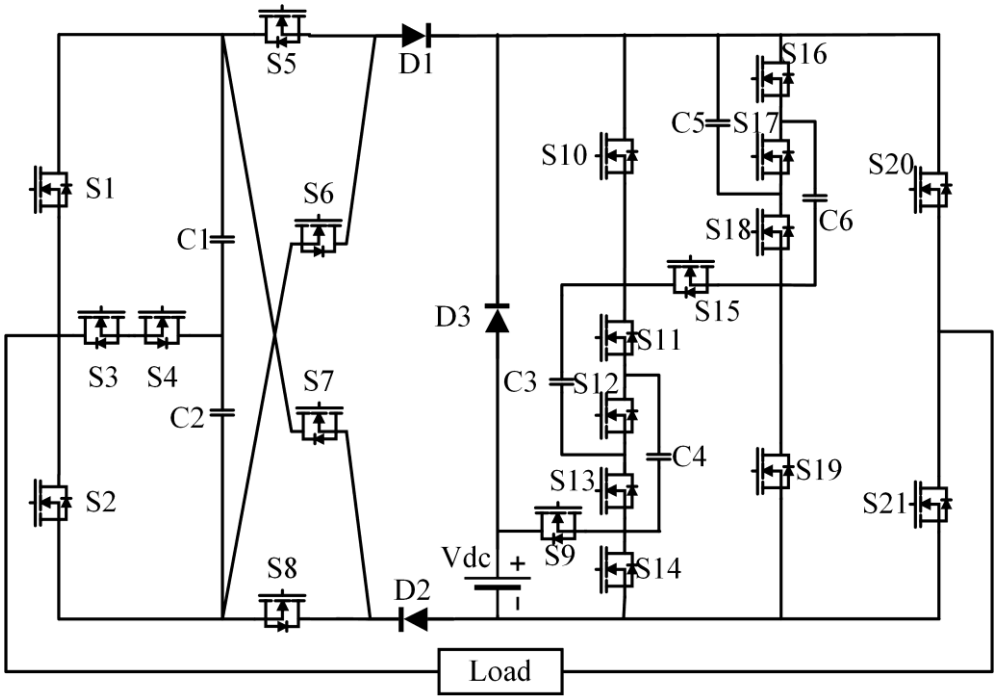
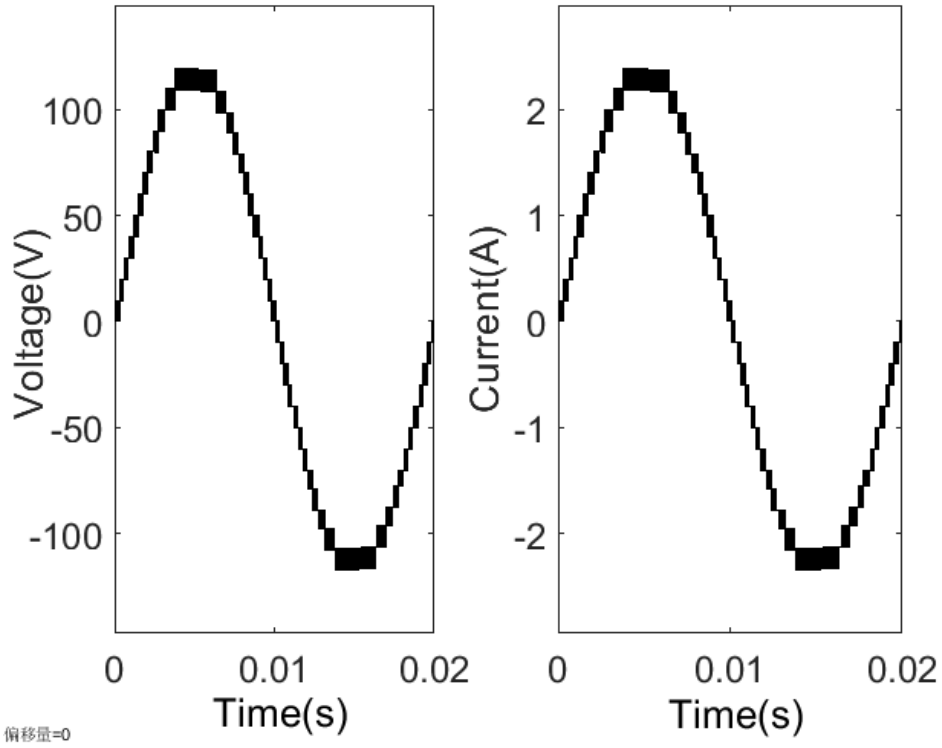


Fig 4.31 Topology of extended 25-level switched capacitor inverter

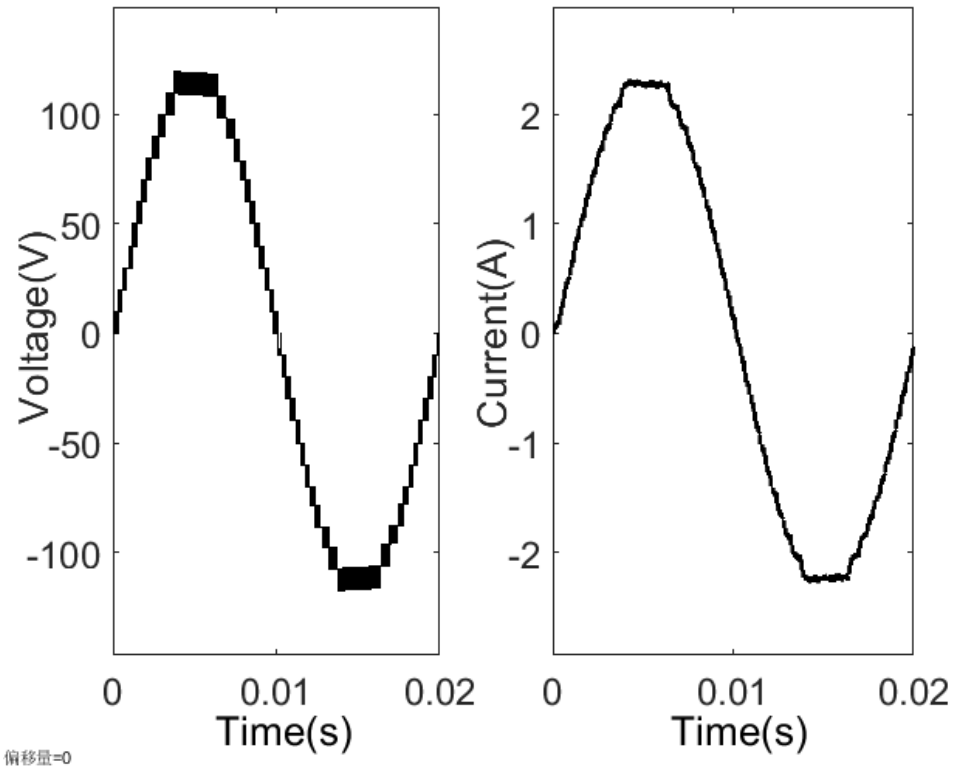
The simulation parameters of proposed 25-level SCMLI are shown in Table 4.6 and the simulation result is shown in figure 4.32 and figure 4.33. Simulation results validate that by connecting an additional series/parallel switched capacitor unit into the topology, the output voltage of the inverter increases by 8 levels and voltage gain increases by 2 times.

Frequency of the sine wave (f_{ref})	50Hz
Frequency of the carrier wave (f_c).)	20kHz
V_{dc}	20V
Capacitance of capacitor C1	6700uF
Capacitance of capacitor C2	6700uF
Capacitance of capacitor C3	4700uF
Capacitance of capacitor C4	4700uF
Capacitance of capacitor C5	4700uF
Capacitance of capacitor C6	4700uF
Resister load R	50Ω
Inductance load L	5mH

Table 4.6 Simulation model parameters

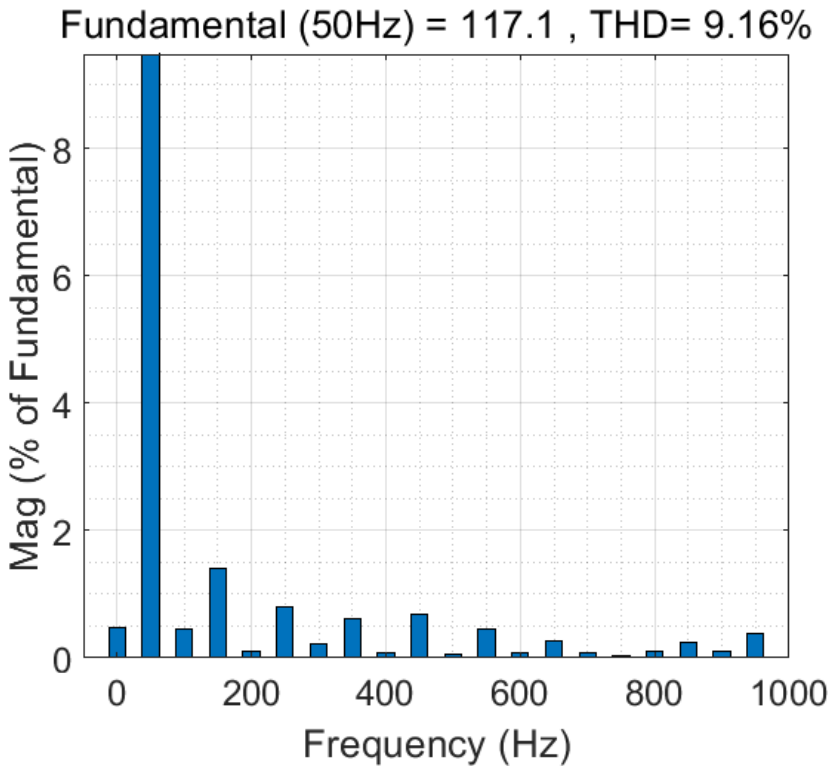


(a)

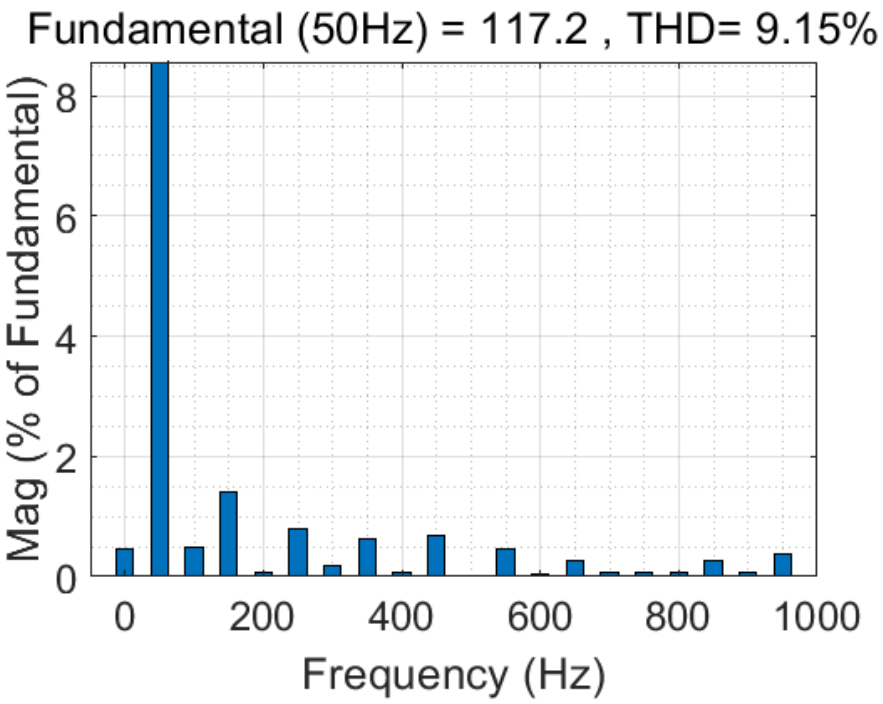


(b)

Fig 4.32 Waveform of output voltage and current of proposed 25-level SCMLI with different load. (a) 50 Ω (b) 50Ω+5mH



(a)



(b)

Fig 4.33 Total harmonic distortion of output voltage of proposed 25-level SCMLI with different load. (a) 50 Ω (b) 50Ω+5mH

4.15 Comparative analysis

In the above, the detailed simulation studies are conducted in the two proposed novel switched capacitor inverters. In this section, a comparative study of the proposed switched capacitor inverter topologies with other topologies will be shown. The factors to be compared include the number of inverter levels(N_l), the number of DC supply(N_{dc}), the number of switches(N_{sw}), the number of capacitors(N_c), the number of diodes(N_d), output voltage boost factor(BF), total standing voltage (TSV), peak voltage stress(PVS) and cost factor (CF)[93][94]. The number of output voltage levels and boost factors of the topologies to be compared are different. Therefore, to facilitate easier comparison and analysis, the TSV and PVS mentioned above are converted to the per unit values using the maximum output voltage magnitude as the base value. Moreover, to evaluate all the SCMLI with different output levels and boost factors, the CF defaults to the value of per boost factor per level. And it can be obtained by the

equation 4.32[95].

$$CF = \frac{N_{sw}+N_c+N_{dr}+N_d+\alpha TSV_{pu}+\gamma PVS_{pu}}{N_l \times BF} \qquad (4.32)$$

Where the α and γ are the weightage factor. If the α and γ <1, the weightage of the switch number is higher than that of TSV and PVS. If the α and γ >1, the weightage of the switch number is lower than that of the TSV and PVS. In the following analysis, the value of the weightage factor is 1.

Topology proposed in	N_{dc}	N_l	N_{sw}	N_{dr}	N_c	N_d	BF	TSV_{pu}	PVS_{pu}	CF
[96]	1	13	23	23	6	4	6	6.67	0.67	0.81
[97]	1	17	39	39	7	0	8	4.88	0.125	0.66
[98]	2	17	24	20	4	0	2	5.5	1	1.6
[99]	1	7	10	9	3	0	1.5	6	0.67	2.73
[100]	1	13	12	11	4	9	1.5	4	1	0.79
[101]	2	13	14	9	2	14	2	5.33	1	1.74
[102]	1	9	10	9	3	3	4	6.38	1	0.9
[103]	2	15	10	10	1	1	1.75	4.85	0.285	1.03
Proposed 13-level SCMLI	1	13	13	12	4	2	3	4.5	1	0.94
Proposed 17-level SCMLI	1	17	15	13	4	3	4	5.5	0.75	0.62

Table 4.7 Comparison of different topologies

Table 4.7 shows the parameters of different topologies. Since the output voltage gains and levels of different topologies are different, comparing the devices used is not intuitive enough. To address this issue, Table 4.8 shows the number of devices used per voltage gain per level of different topologies.

Topology proposed in	N_l	N_{sw}	N_{dr}	N_c	N_d	N_{sum}	BF	TSV_{pu}	PVS_{pu}	CF
[96]	13	0.294	0.294	0.077	0.051	0.716	6	6.67	0.67	0.81
[97]	17	0.286	0.286	0.051	0	0.623	8	4.88	0.125	0.66
[98]	17	0.706	0.714	0.118	0	1.538	2	5.5	1	1.6
[99]	7	0.952	0.857	0.214	0	2.203	1.5	6	0.67	2.73
[100]	13	0.615	0.564	0.205	0.462	1.846	1.5	4	1	0.79
[101]	13	0.538	0.346	0.077	0.538	1.499	2	5.33	1	1.74
[102]	9	0.278	0.25	0.083	0.083	0.694	4	6.38	1	0.9
[103]	15	0.381	0.381	0.038	0.038	0.838	1.75	4.85	0.285	1.03
Proposed 13-level SCMLI	13	0.333	0.308	0.102	0.077	0.82	3	4.5	1	0.94
Proposed 17-level SCMLI	17	0.221	0.206	0.059	0.044	0.53	4	5.5	0.75	0.62

Table 4.8 The number of devices per voltage gain per level of different topologies

The total number of the devices the topology used per level per voltage gain is represent by the N_{sum}. It can be seen from Table 4.8 that with one voltage gain and one level output, the proposed 17-level SCMLI uses the smallest number of devices. Because the inherent circuit is used to replace the H-bridge as the positive and negative polarity conversion of the output voltage, the TSV and PVS of the proposed 17-level SCMLI are maintained at a relatively low level. Moreover, the cost factor of the proposed 17-level SCMLI is the lowest among all the compared topologies.

4.16 Chapter conclusion

In this chapter, two novel switched capacitor inverter topologies are proposed, and their detailed description and simulation modelling are carried out. Subsequently, the simulation results are also explained in detail. Through comparative studies with other switched capacitor topologies, it can be seen that the two proposed switched capacitor topologies have better overall performance, especially 17-level SCMLI is the best.

Chapter 5: Hardware Implement and Experiment Results

5.1 Introduction

In the above, a detailed simulation analysis has been carried out on the proposed two novel switched-capacitor inverters, and a detailed comparative study with other topologies has been carried out. Finally, the comprehensive performance of the proposed 17-level SCMLI was concluded to be better. Therefore, this chapter will conduct detailed prototype model construction and experimental research on the proposed 17-level SCMLI. The control part uses FPGA to implement 17-level switching signals based on PDPWM technology. The driving circuit of the MOSFET is based on optocoupler isolation and current mirror solutions.

5.2 FPGA-based PDPWM implementation

For the control of multi-level inverters, the mainstream methods are DSP (digital signal processor) and FPGA (field programmable logic gate array). DSP and FPGA each have unique characteristics and advantages. First, DSP excels in specialized signal processing capabilities and is particularly suitable for performing efficient mathematical operations and signal processing tasks such as filtering and Fourier transforms [104][105]. This advantage of DSP makes it very useful in signal analysis and processing in power systems [106]. In addition, DSPs are usually designed as low-power devices, which is especially important in inverter systems that require energy saving or battery power [107][108][109]. In terms of cost, DSPs are generally more cost-effective than FPGAs in mass production. However, the functions and processing capabilities of DSPs are relatively fixed, and their flexibility and adaptability are not as good as FPGAs.

In contrast, FPGAs provide greater flexibility and customization capabilities. It can be precisely programmed to suit specific application requirements, such as implementing special control algorithms or logic. The parallel processing capabilities of an FPGA enable it to process multiple operations or signals simultaneously, which is useful when controlling and monitoring various aspects of an inverter in real time. FPGAs also provide speedy and precise response times, which are critical for controlling the switching actions of the inverter. In addition, as design requirements change, FPGA can be easily reprogrammed to adapt to new requirements or standards, making it suitable for implementing complex control logic.

In PDPWM applications, generating multiple signal channels simultaneously or implementing multiple control logic in a single channel is necessary. FPGAs can process these tasks in parallel while maintaining high accuracy and responsiveness for each task [110][111]. Considering the high energy consumption and cost of FPGA, the cyclone series FPGA launched by Altera company was selected in this experiment. This is because the Cyclone family of FPGAs is designed for cost-sensitive applications. They offer an affordable solution while maintaining good performance, which is especially important for projects on a tight budget. In addition, Cyclone series FPGAs pay special attention to low-power design, which is very important for applications that want to reduce overall system energy consumption, especially in portable or battery-powered devices.

The RTL (Register-Transfer Level) diagram is a critical tool in digital circuit design, providing a way to describe the functions and operations of a digital circuit or system. It does not focus on the actual physical implementation of the circuit but rather on how data is transferred between registers and how logical operations are performed on this data. Figure 5.1 shows the RTL diagram of the proposed PDPWM to control the 17-level SCMLI.

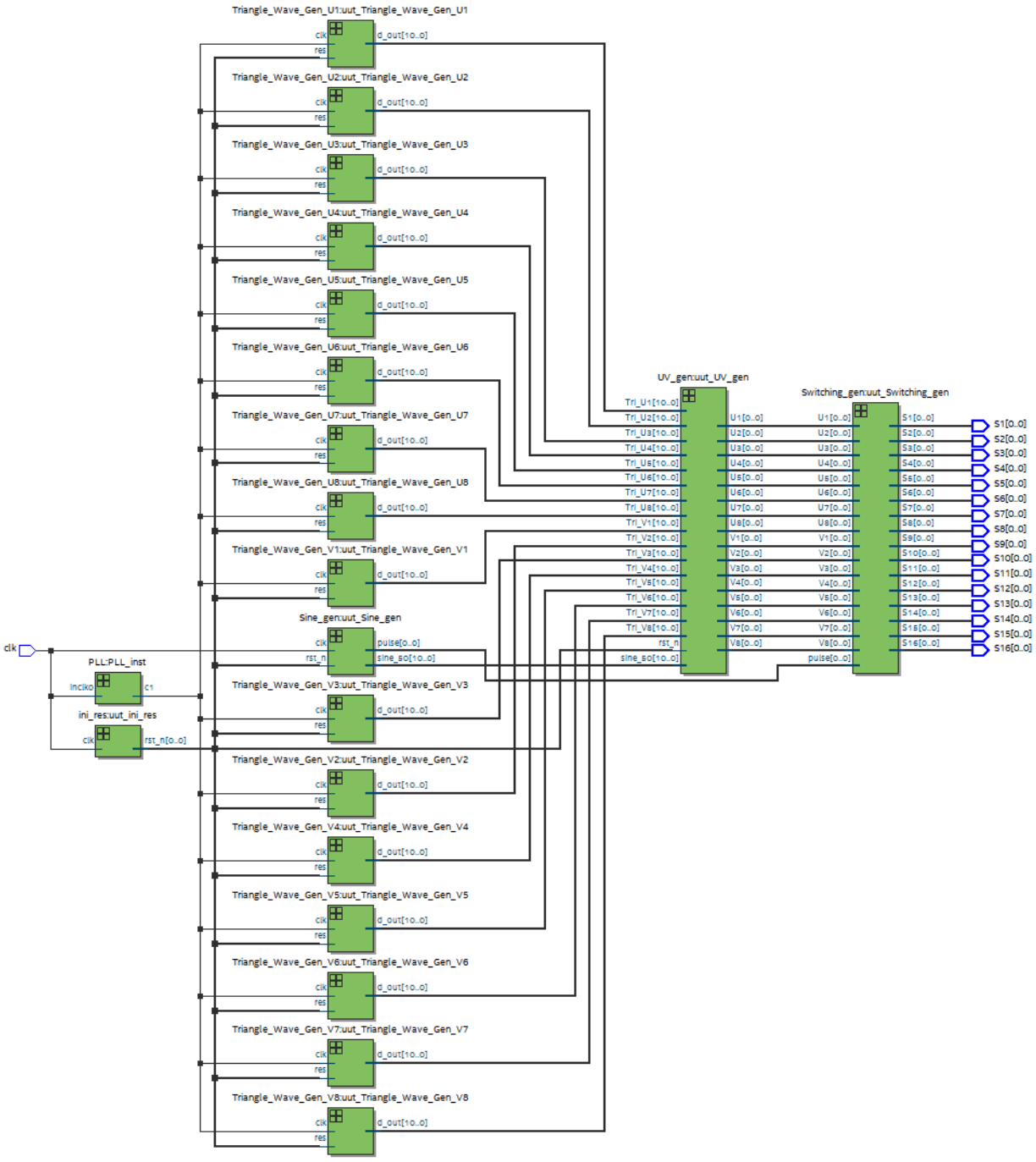


Fig 5.1 RTL diagram of proposed PDPWM

The cyclone IV FPGA chip was chosen, and the clock is 50MHz. As can be seen from figure 5.1, the PLL is used to distribute the system clock to the required clock frequency. The synchronous reset module ensures that all triangle wave phases remain consistent when the system starts working. All clock signals enter the triangle wave generation module in parallel. The sine wave is generated using the MIF maker. The amplitude of the sine wave is 0 to 1024, so on the ordinate, the sine wave has 1024 values. Store all

values in the register to generate 16 triangle waves. The 1024 values are divided into 16 equal parts as the amplitude of the triangle wave. So, each triangle wave counts 128 times in one cycle. The state machine determines whether the triangle wave reaches the peak to trigger the falling state and whether it reaches the lowest point to trigger the rising state. So, the clock frequency can be calculated by applying the following equations

$$T_{trianglewave} = \frac{1}{f_c} \tag{5.1}$$

$$f_{input\ for\ triangle\ wave} = {1}\Big/{\frac{T_{trianglewave}}{128}} \tag{5.2}$$

Where f_c is the desired frequency of the triangle wave.

For example, if the frequency of the triangle wave is 20kHz. The clock frequency of the triangle generation module can be calculated as follows.

$$T_{trianglewave} = \frac{1}{20kHz} = 0.00005$$

$$f_{input\ for\ triangle\ wave} = {1}\Big/{\frac{0.00005}{128}} = 25.6\text{MHz}$$

Therefore, if we want to generate a triangle wave with a frequency of 20kHz, the input clock frequency of the triangle wave generation module is 25.6MHz.

The UV_generation module generates signals by comparing the values of sinewave and triangle waves. The signals here are the modulation signal of each level interval of the output voltage of the controlled inverter. These signals need to be input to the logic combination module and logically combined through the designed inverter switching state to obtain the switching signal of each MOSFET.

By applying a logic analyzer, we can observe the modulation signal generated by the FPGA and the MOSFET switching signal obtained through logic combination. The signals are shown in figure 5.2 and figure 5.3.

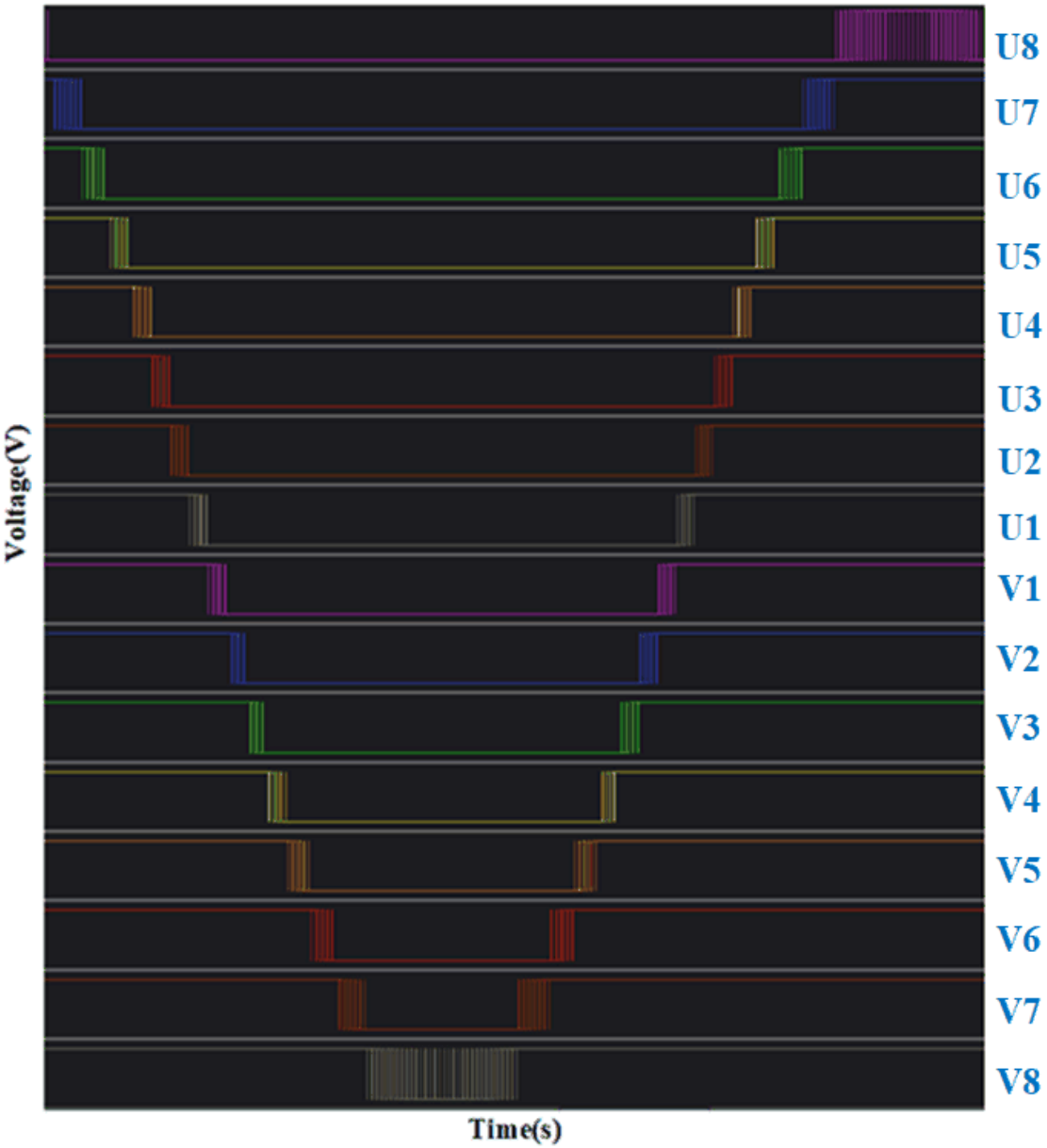


Fig 5.2 The output signal of U1-U8 and V1-V8

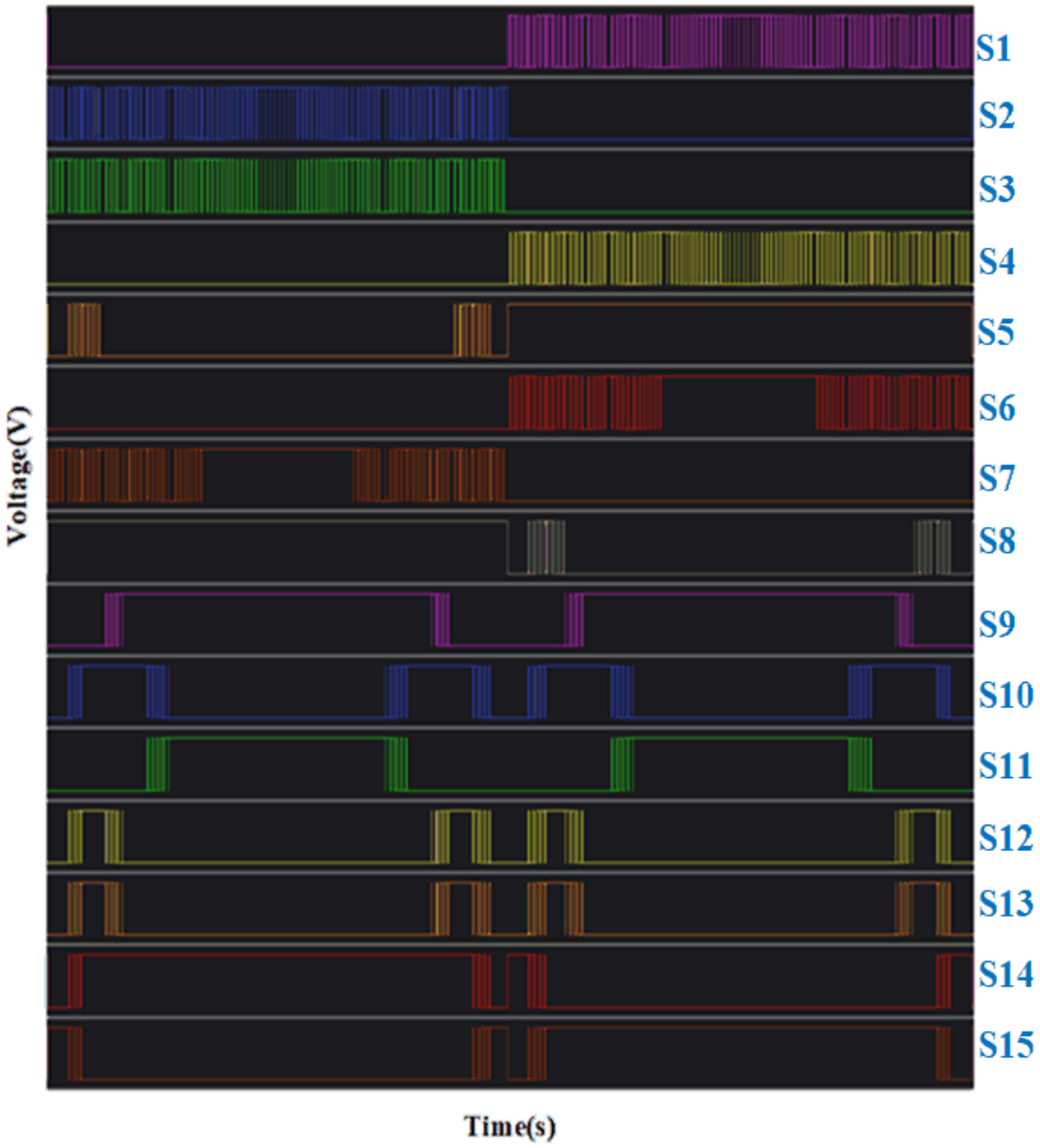


Fig 5.3 Switching signal of S1-S15

5.3 Gate drive of the MOSFETs

In the above research, we have obtained the signals to drive the power MOSFETs through Verilog code by applying FPGA. But these signals cannot directly drive the power MOSFETs. This is because the output of the FPGA can usually only provide a few milliamps of current. Such a small current is insufficient to charge and discharge the gate capacitance in the MOSFET to turn off or turn on the power MOSFET quickly.

Moreover, FPGAs often have low output voltage levels (such as 3.3V or 5V) that may need to be increased to turn on some power switches entirely. Gate drivers can provide higher voltages to ensure adequate conduction of the power MOSFET. The most important thing is that since the 17-level SCMLI in this experiment is designed to be used in high-voltage and high-power situations, direct connection to the FPGA may cause high voltage and enormous current rush into the FPGA and cause damage. Therefore, connecting a gate driver with isolation and protection is necessary to avoid this situation.

Two gate drivers are tested in this experiment, and the PCB prototypes are shown in figure 5.4 and figure 5.5. Both gate driver circuits use optocoupler chips as isolation. The chip model used in the first drive circuit is ACPL-332J, and the chip model used in the second drive circuit is HCPL-3120. Among them, ACPL-332J can provide a higher drive current to drive higher power MOSFET, while the current supplied by the HCPL-3120 is minimal. Therefore, the output voltage of the ACPL-332J in the first gate driver circuit directly drives the MOSFET after being filtered by the capacitor. The output of the transformer in the second gate driver circuit is connected in parallel to the transistor inside the drive circuit through the filter capacitor. HCPL-3120 controls the MOSFET by controlling the opening and closing of the transistor. Moreover, the discharge circuit designs of the two gate driver circuits are different. The first gate driver circuit uses a transient voltage suppressor diode(TVS Diode), and the second gate driver circuit uses a bleeder resistor(R_{gs}). The resistance of the bleeder resistor is 10 kΩ. It is worth noting that the input PWM voltage of the first gate driver circuit is 15V, so an external voltage level shift circuit is necessary, while the input PWM voltage of the second gate driver circuit is 3.3V, which means that it can connect to the FPGA directly.

The output delay of two gate driver circuits is tested, and the test bench is shown in figure 5.6. The voltage level-shifted board is used to step up the 3.3V output voltage from the FPGA to 15V, and the FPGA is used to generate the pulse signal. And a MOSFET is connected to the output of the gate driver board.

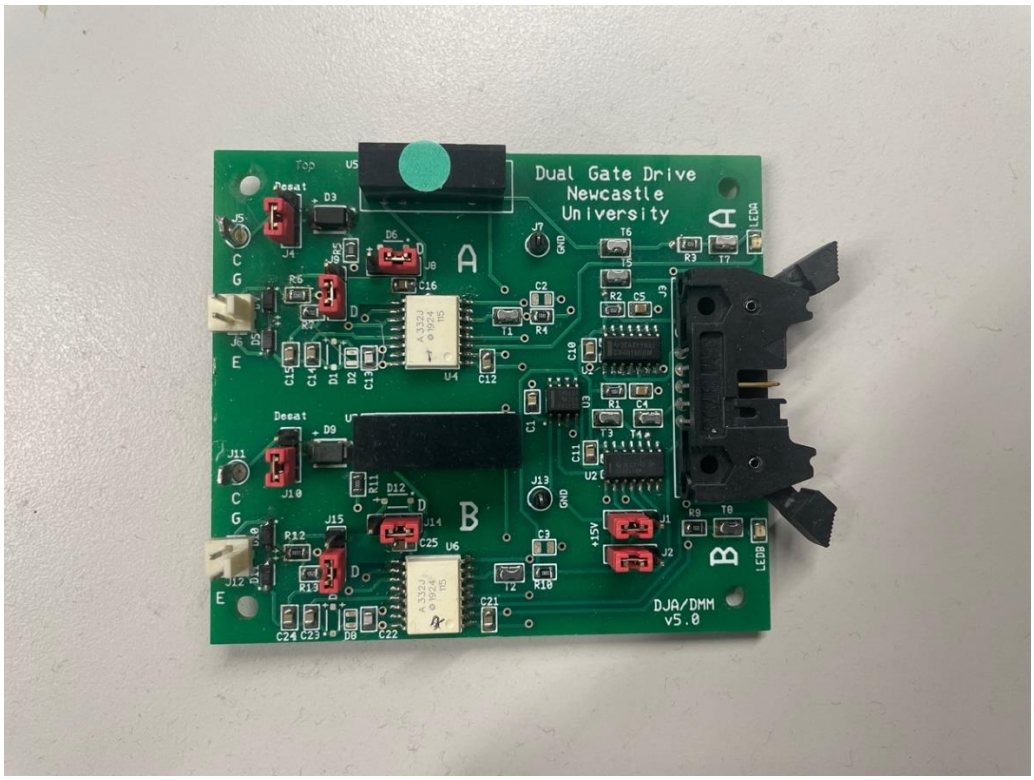


Fig 5.4 PCB prototype of the first gate driver

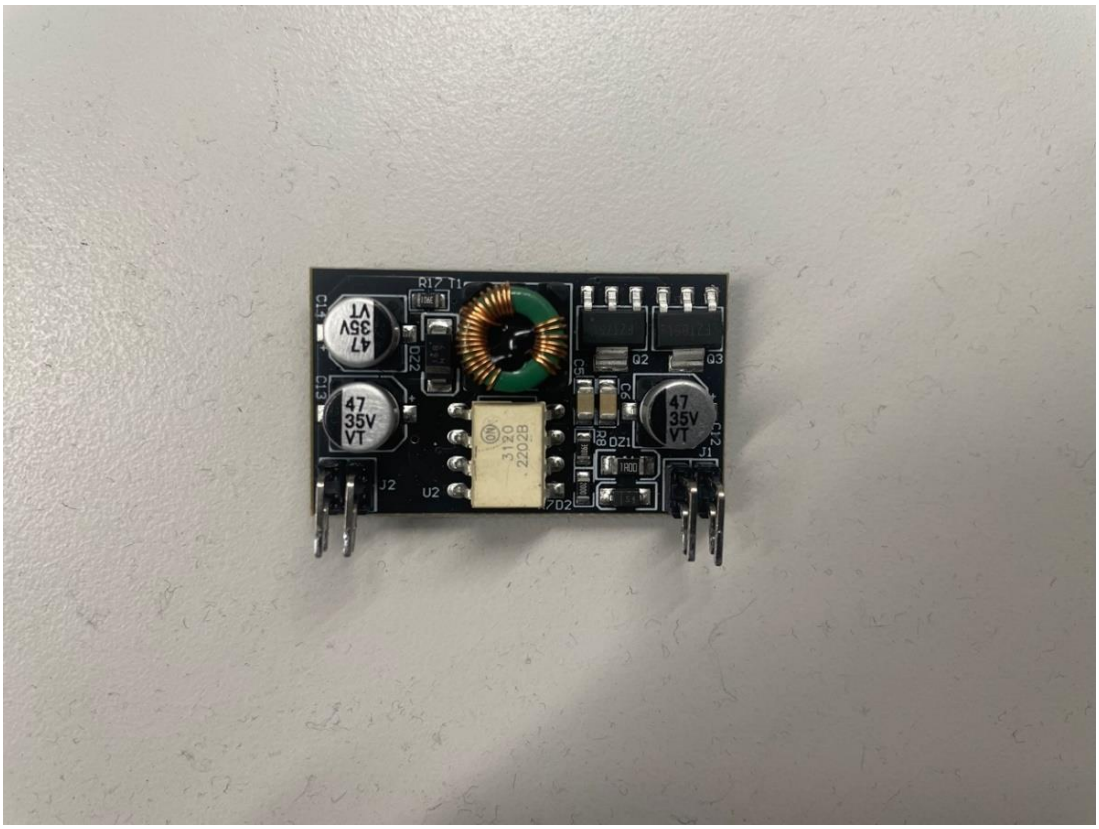


Fig 5.5 PCB prototype of the second gate driver

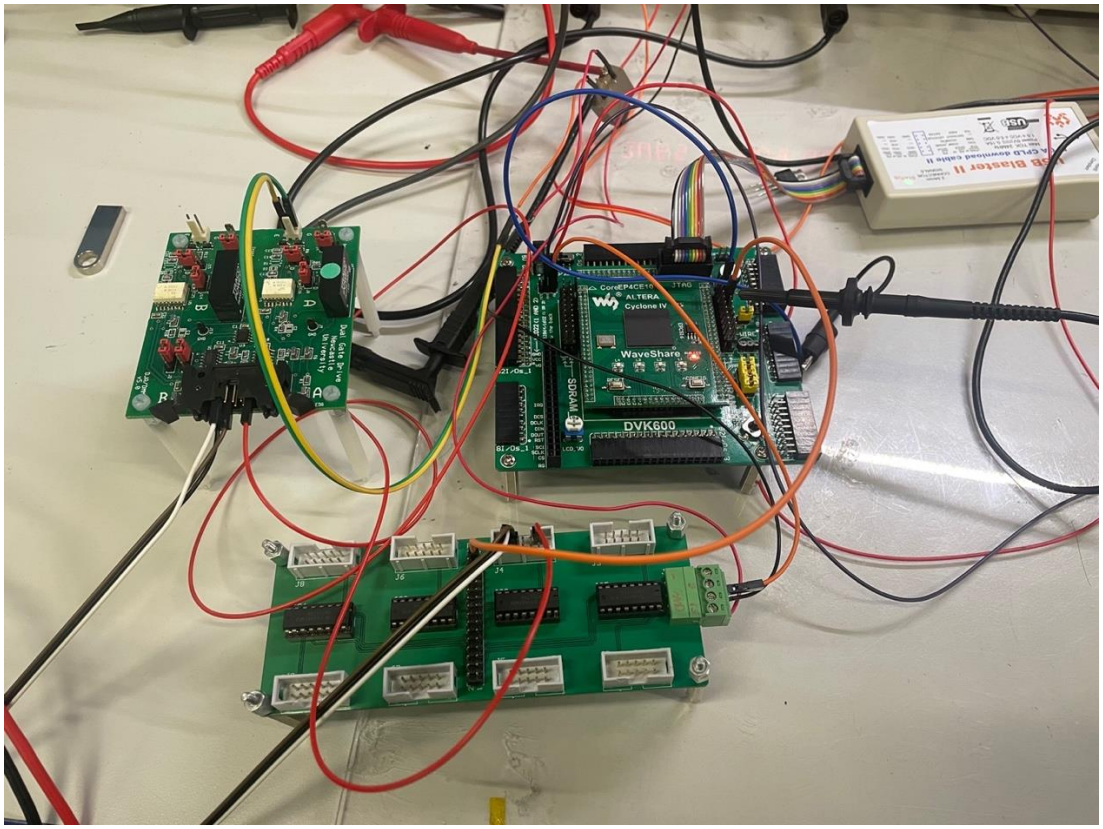
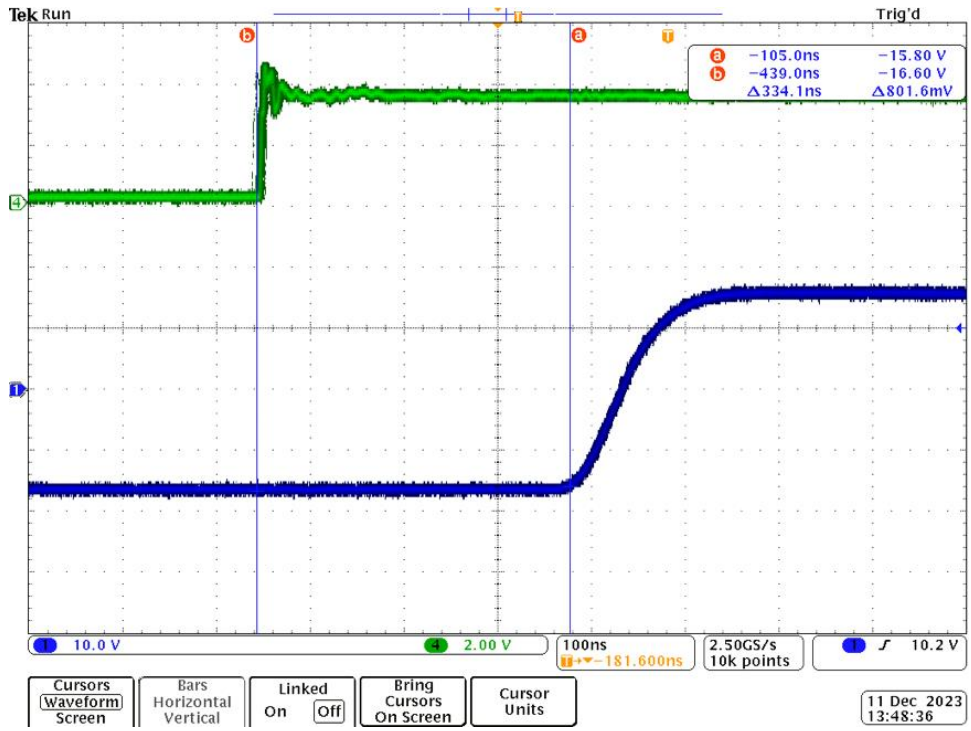


Fig 5.6 Test bench of the gate driver output delay test

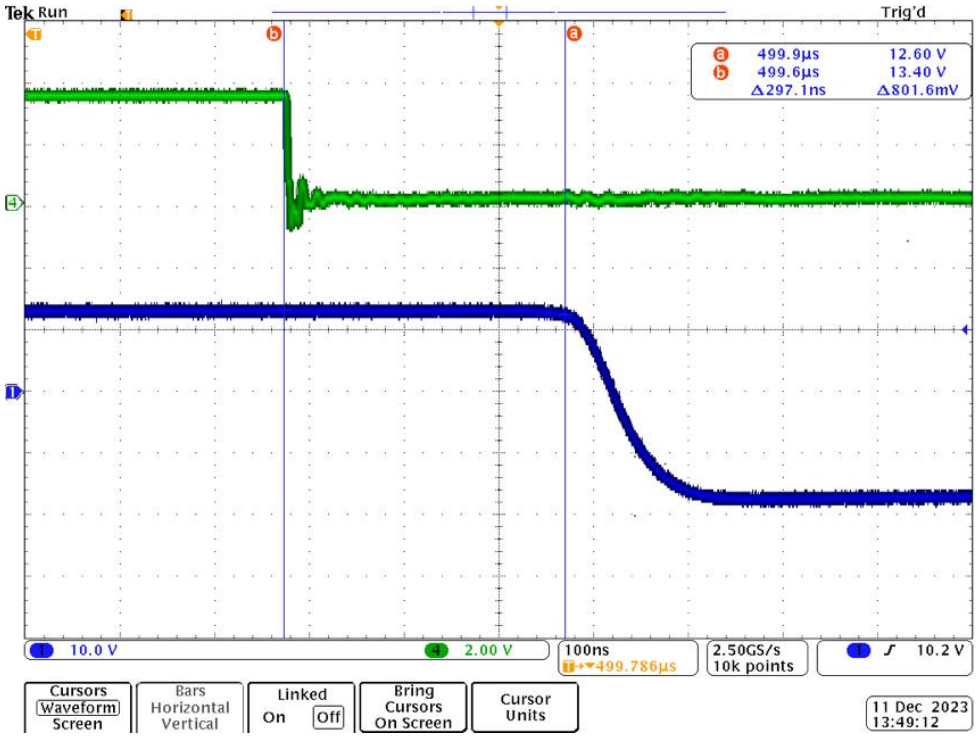
The output delay of the first gate driver board is shown in figure 5.7. The gate ON delay is 334.1ns and the gate OFF delay is 297.1ns.

The output delay of the second gate driver board without the gate ON resistor is shown in figure 5.8. The gate ON delay is 266ns and the gate OFF delay is 260ns. The amplitude of voltage ringing when gate ON is 29V and when gate OFF is 50.2V.

The voltage ringing after connecting a 22Ω resistor is shown in figure 5.9. it can be seen that the ringing is eliminated after connecting the gate ON resistor.

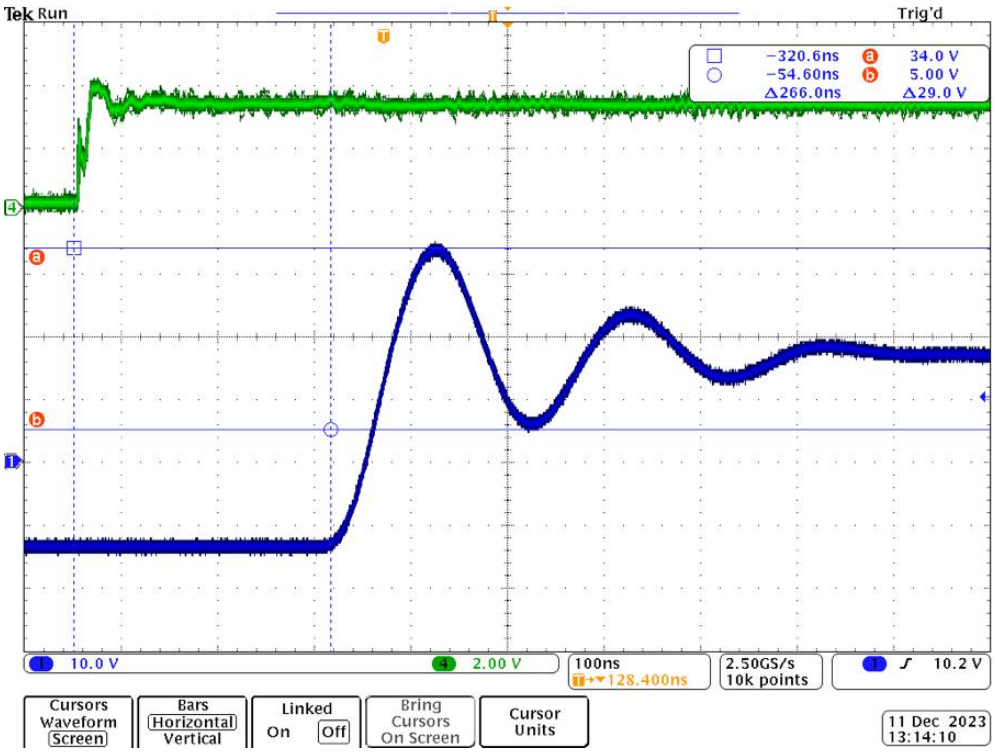


(a)

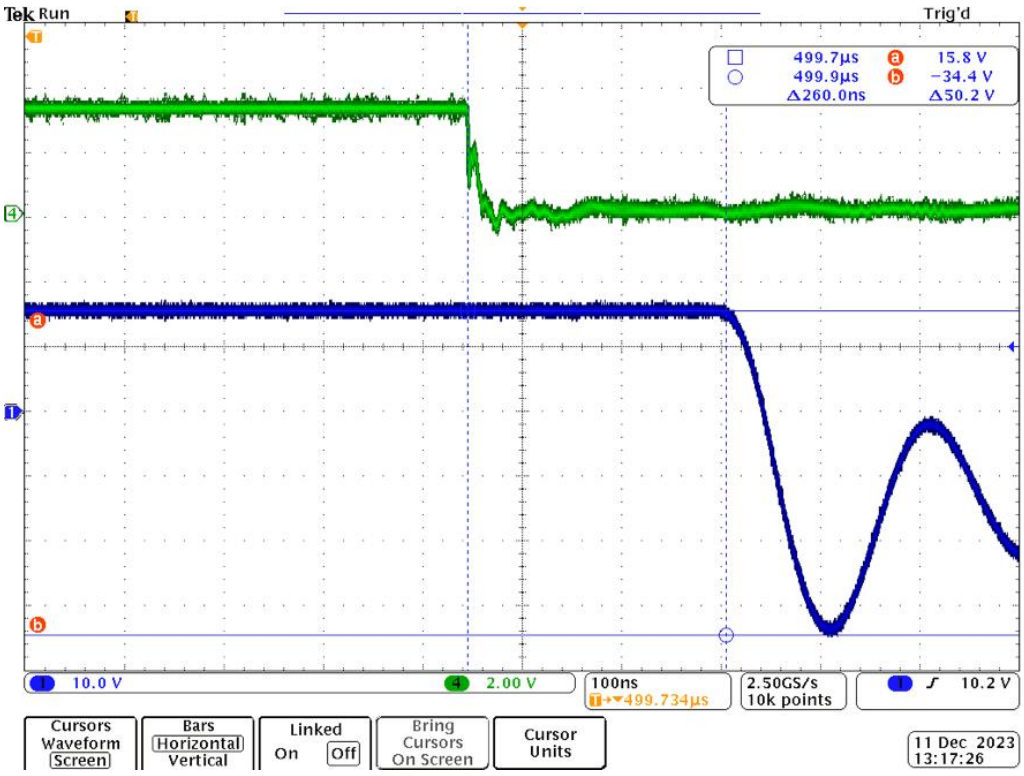


(b)

Fig 5.7 Output delay of the first gate driver board



(a)



(b)

Fig 5.8 Output delay of second gate driver board

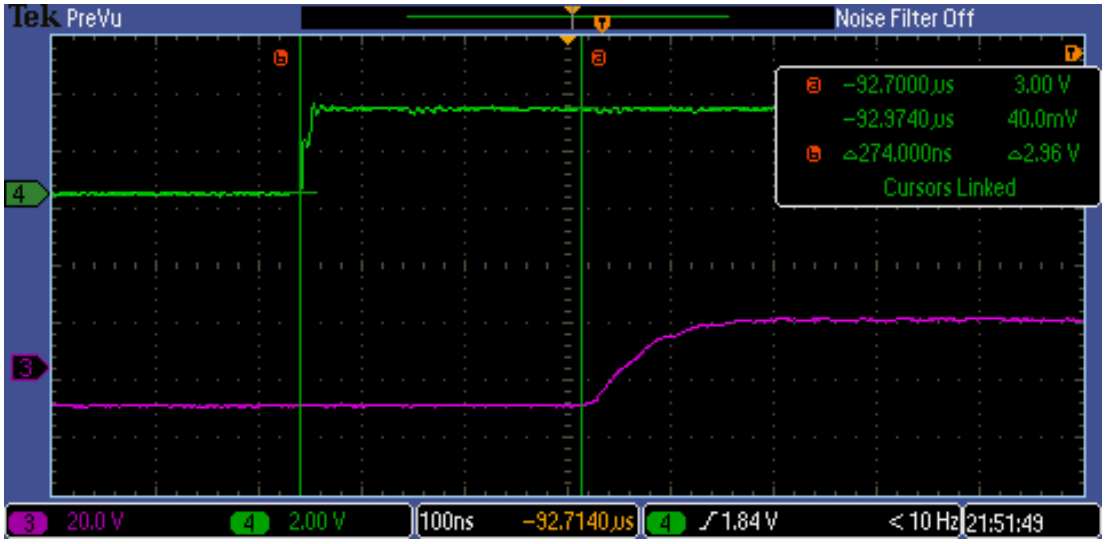


Fig 5.9 Voltage ringing after connecting gate on resistor

5.4 17-level SCMLI prototype implementation and experiment result

The above has been experimentally studied on the FPGA and gate driver used to control the proposed 17-level SCMLI. In this part, the testbench of the proposed 17-level SCMLI will be built and tested. The PCB of the proposed 17-level SCMLI is shown in figure 5.10. Fifteen power MOSFETs of model IRF540 were applied to the inverter circuit for the experiment. The parameters of the prototype used in the experiment are shown in Table 5.1. The full prototype of the system used for the experiment is shown in figure 5.11. In this experiment, the proposed topology was tested in connection with different loads. The self-balancing performance of the capacitor and the harmonic content of the output voltage were verified. Figure 5.12 shows the voltage of the capacitors in the inverter circuits. It can be seen, the capacitors C1 and C2 have the same value and capacitors C3 and C4 have the same value. The maximum voltage of C1 and C2 is 8.8V, and the minimum voltage is 6.6V. Therefore, the voltage ripple of capacitors C1 and C2 is 25%. It can be known that the voltage of the capacitor after charging is slightly lower than the design value of 10V. This is because the threshold voltage of the diodes will lead to a voltage loss in the charging circuit of the capacitors and the MOSFETs in the charging circuit will be in series with the capacitors for voltage division. When the charging current of the capacitor is higher, the voltage division

phenomenon will become obvious. The reason the voltage ripple is larger than the designed value is that the capacitance value selected was smaller due to size and safety considerations in the experiment. The maximum voltage of capacitors C3 and C4 is 19.2V, and the minimum voltage is 16.8V, and the voltage ripple of them is 12.5%. It can be seen that the voltage loss of capacitors C3 and C4 is lower than that of the capacitors C1 and C2. This is because the number of diodes in the charging circuit of C3 and C4 is lower than that of C1 and C2.

The voltage stress of the MOSFETs is shown in figure 5.13. The voltage stress of the MOSFETs in the experimental PCB is the same as that of the simulation.

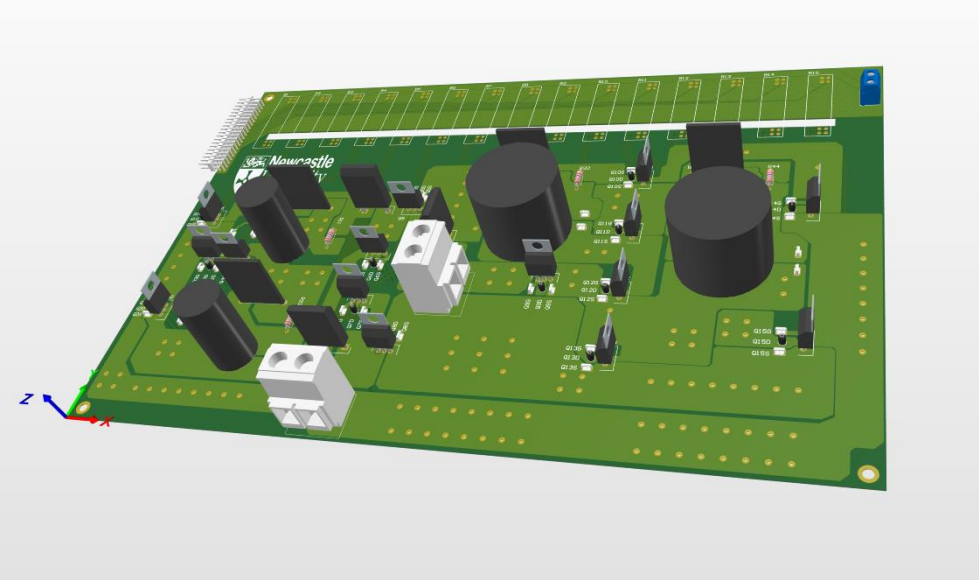


Fig 5.10 PCB layout of the proposed 17-level SCMLI

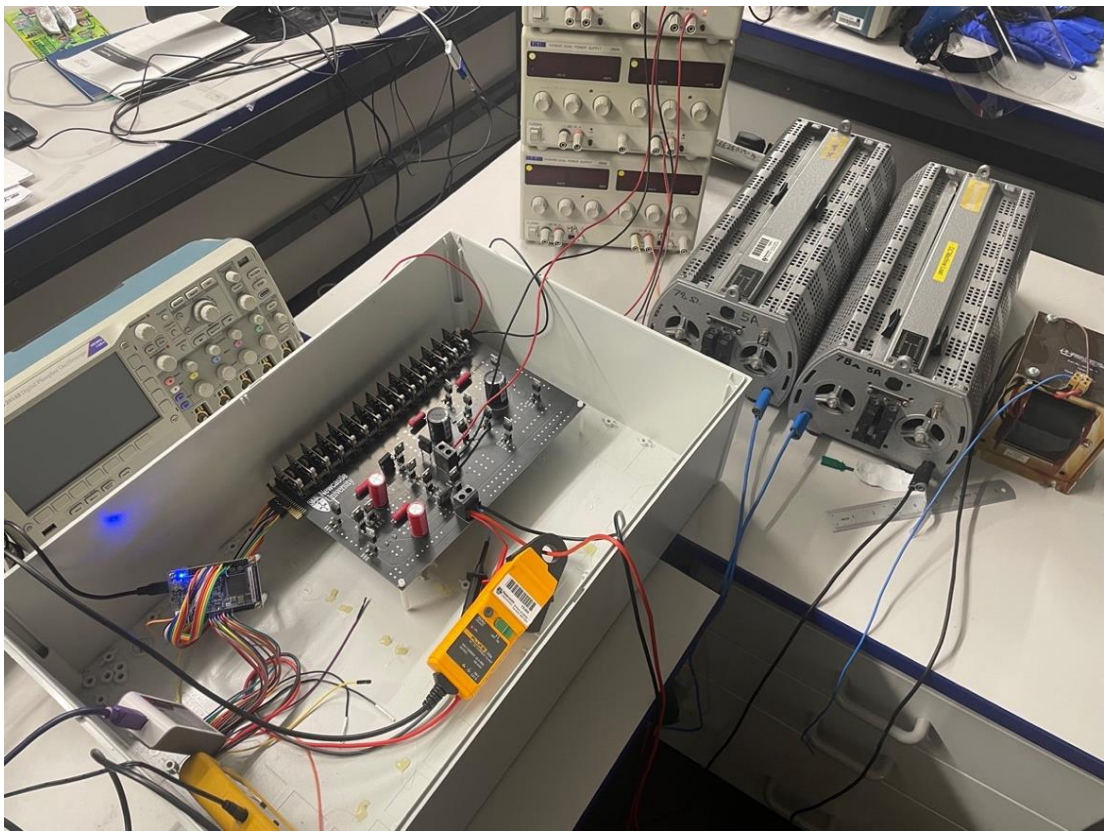
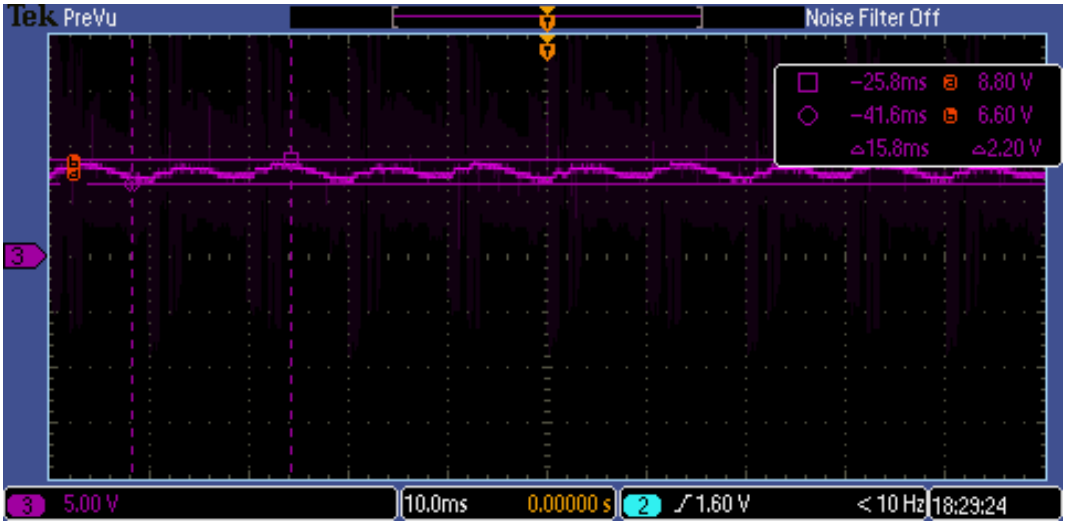
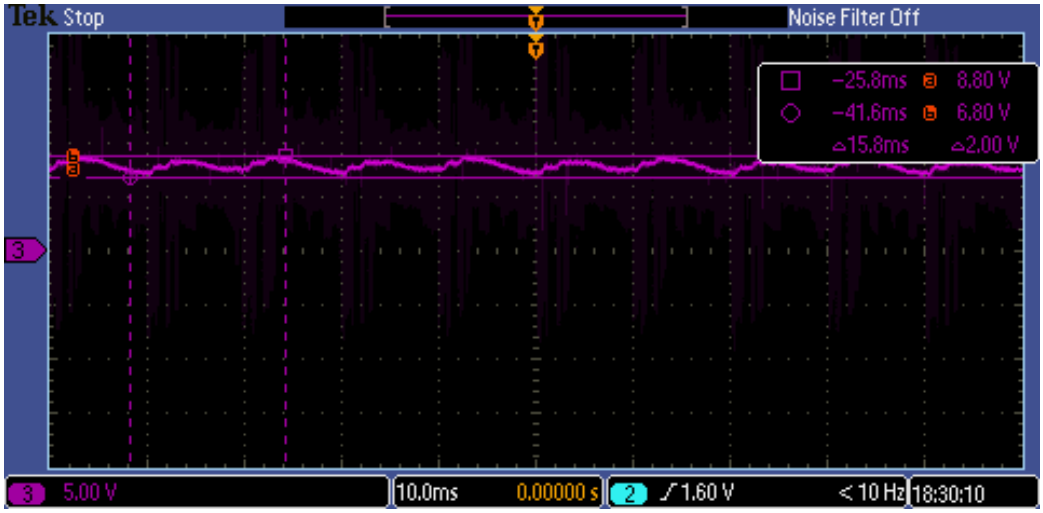


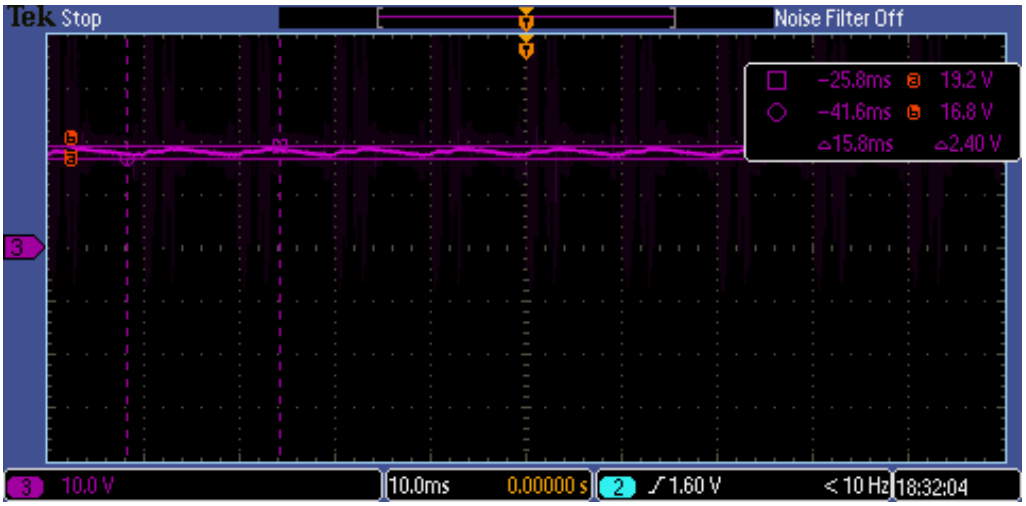
Fig 5.11 Test bench of the inverter system



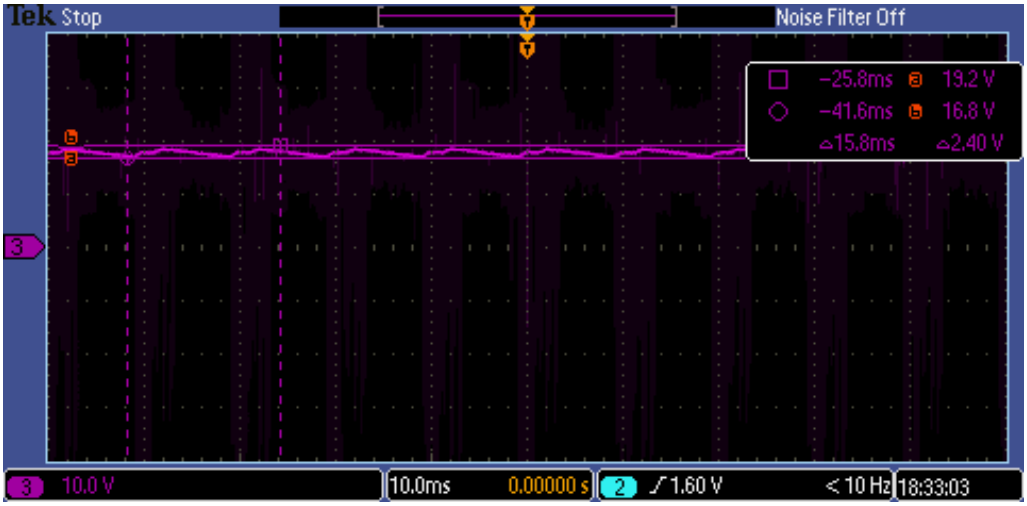
(a)



(b)

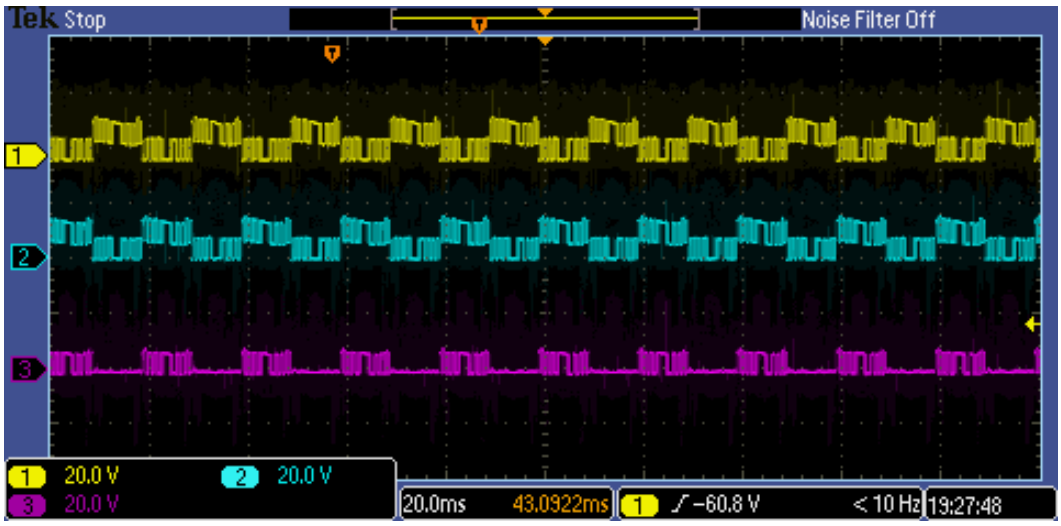


(c)

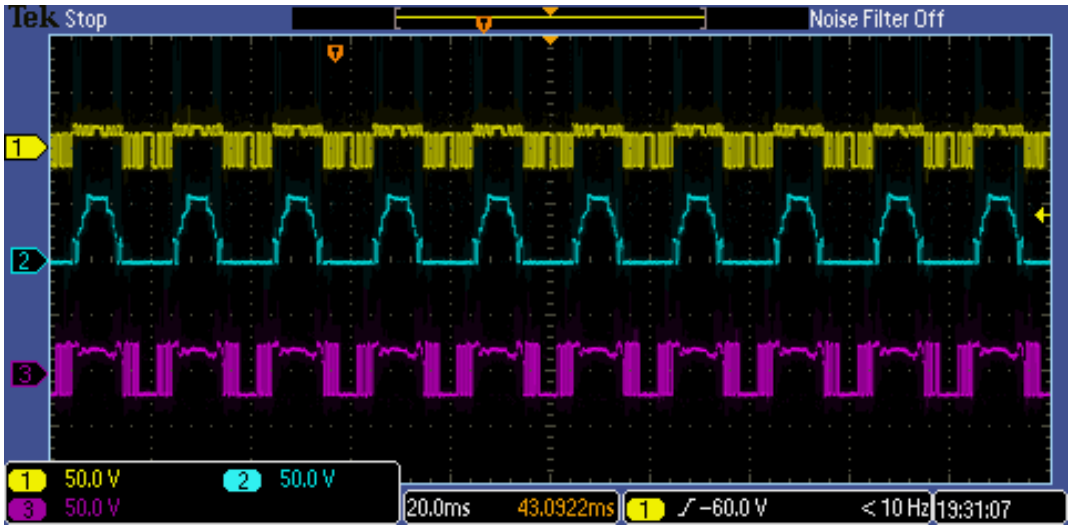


(d)

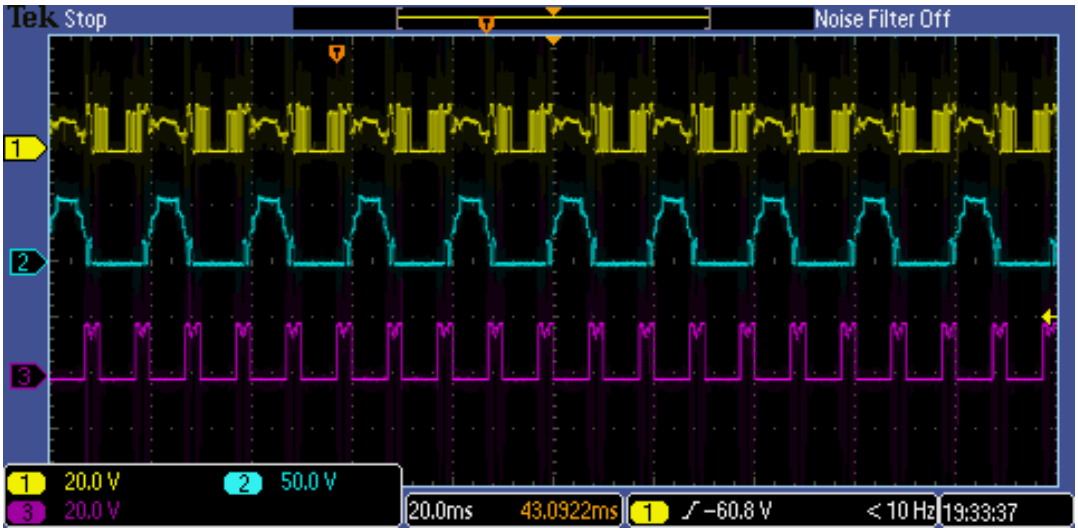
Fig 5.12 Charging and discharging voltage of capacitors(a)capacitor C1(b)capacitor C2(c)Capacitor C3(d)capacitor C4


Tek Stop
Noise Filter Off
1
2
3
1 20.0 V
2 20.0 V
3 20.0 V
20.0ms
43.0922ms
1 ⁄ −60.8 V
< 10 Hz
19:27:48

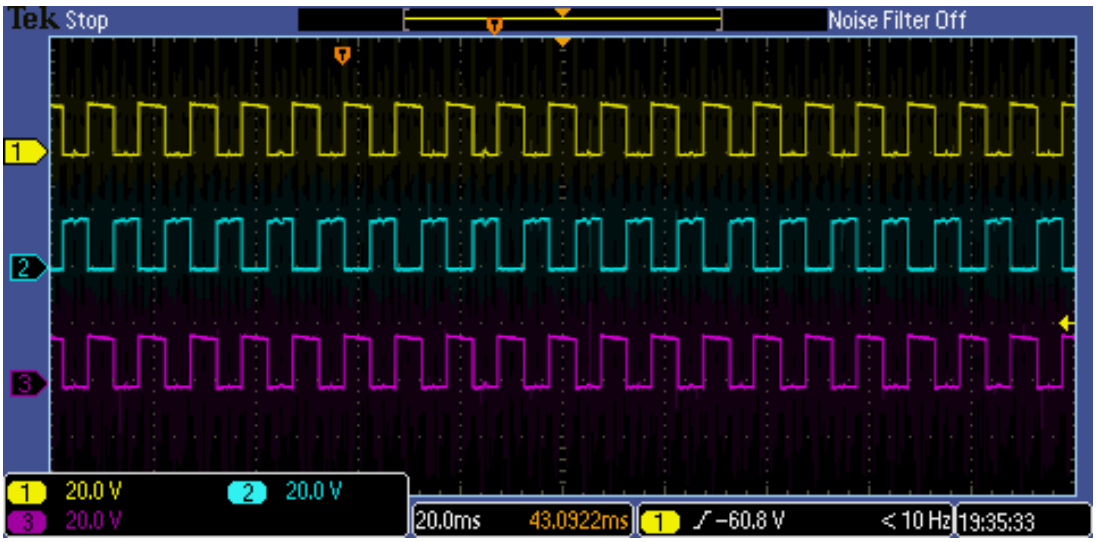
(a)


Tek Stop
Noise Filter Off
1
2
3
1 50.0 V
2 50.0 V
3 50.0 V
20.0ms
43.0922ms
1 ⁄ −60.0 V
< 10 Hz
19:31:07

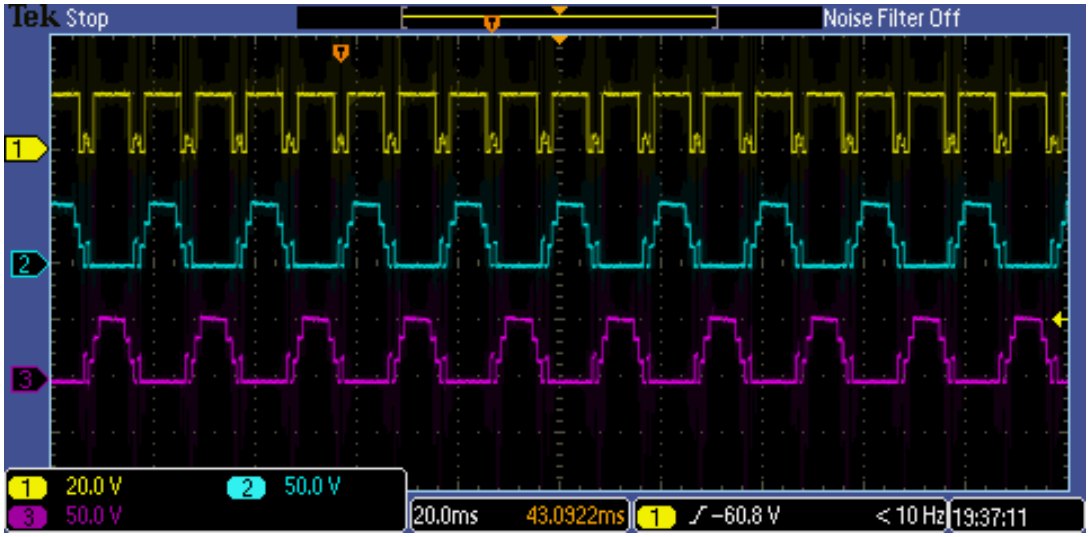
(b)


Tek Stop
Noise Filter Off
1
2
3
1 20.0 V
2 50.0 V
3 20.0 V
20.0ms
43.0922ms
1 ⁄ −60.8 V
< 10 Hz
19:33:37

(c)



(d)



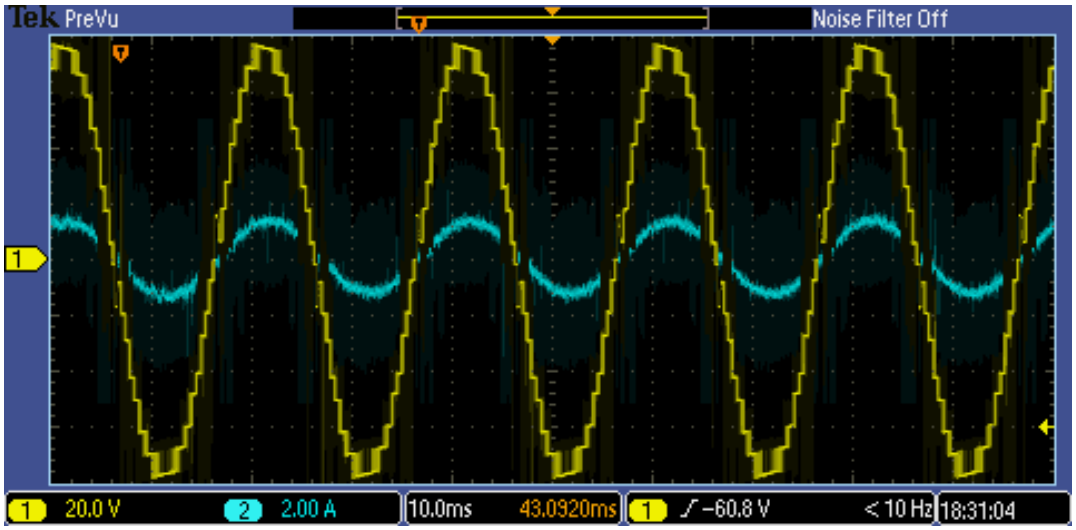
(e)

Fig 5.13 Voltage stress of MOSFETs(a)S1-S3(b)S4-S6(c)S7-S9(d)S10-S12(e)S13-S15

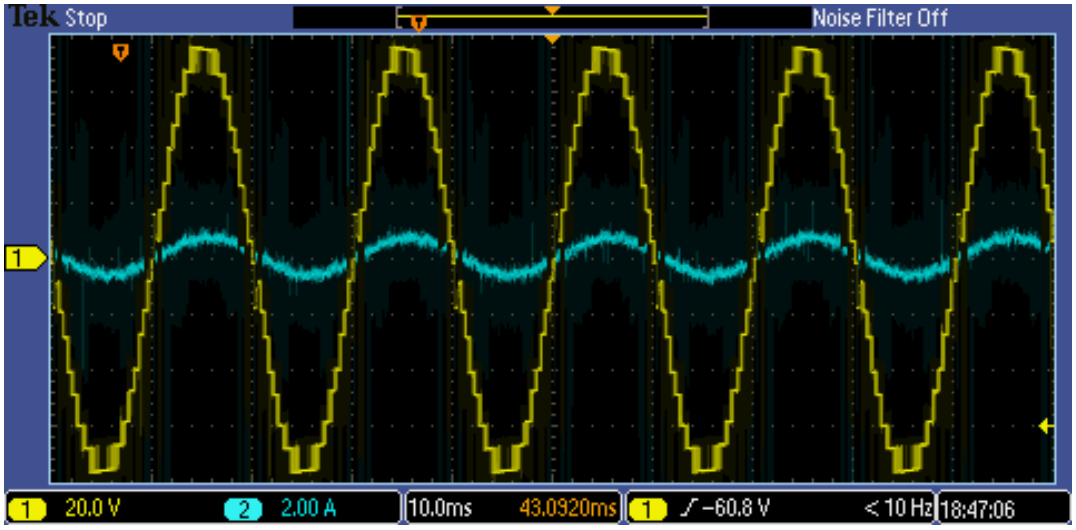
DC supply	20V
Load	(a) 50Ω(b)100Ω(c)50Ω+1.5mH(d)50Ω+10mH
MOSFET model	IRF540
Diode model	RHRG75120
Capacitor C1 and C2 model	WCAP-ATG5 2200uF
Capacitor C3 and C4 model	380LQ682M050H452 6800 uF
FPGA model	Cyclone IV EP4CE22F17C6N

Table 5.1 Parameters of the prototype

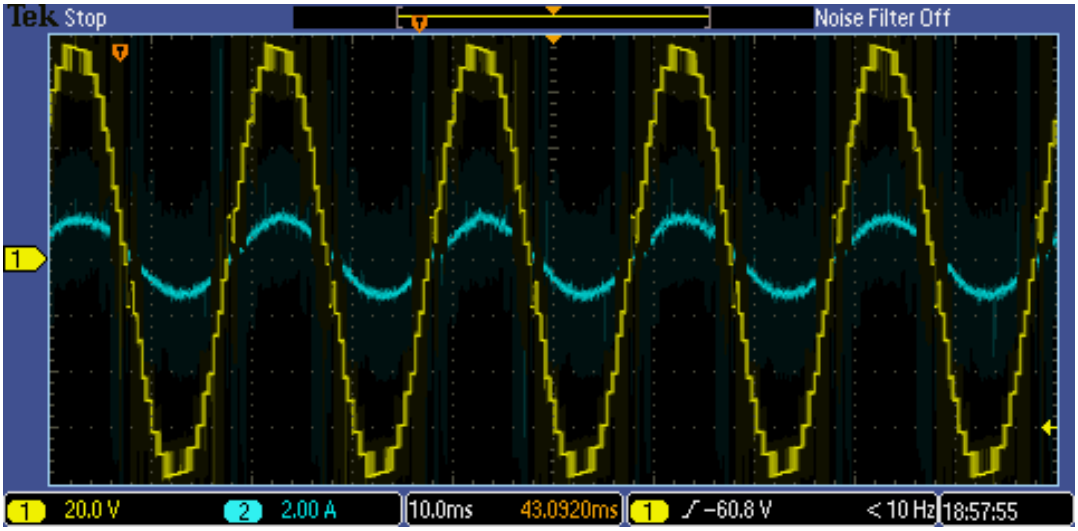
In this experiment, the output of the inverter system was tested with different loads. Figure 5.14(a) is the waveform of the output voltage and current when a 50Ω pure resistive load is connected. (b) is when a 100 Ω pure resistive load is connected. The waveform (c) is the waveform when a resistive-inductive load of 50Ω resistor and 1.5mH inductor is connected. (d) is the waveform when a resistive-inductive load of 50ohm resistor and 10mH inductor is connected. It can be seen from the figure that no matter what kind of load is connected, the inverter can output a voltage waveform of 17 levels and 4 times the voltage gain and a current waveform close to a sine wave.



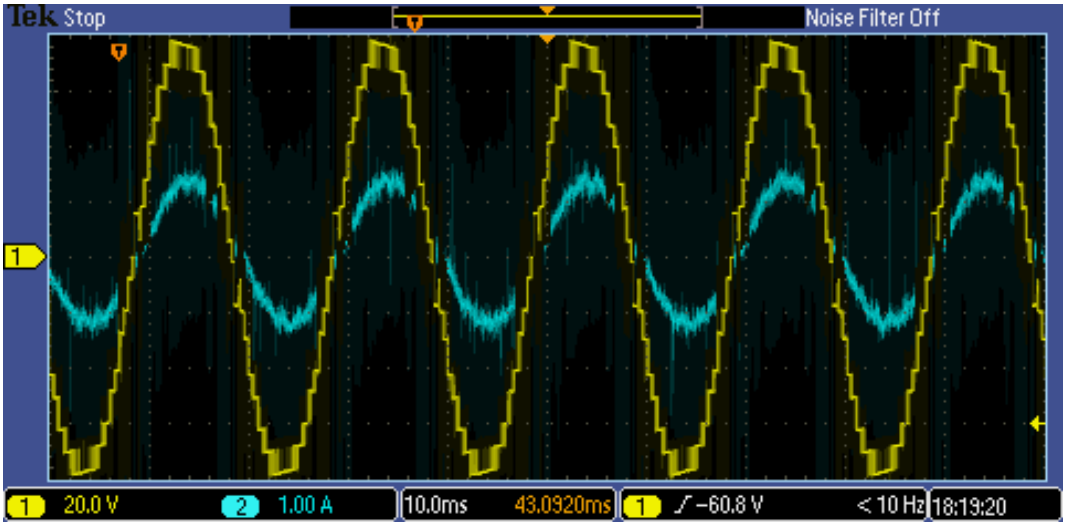
(a)



(b)



(c)



(d)

Fig 5.14 the output voltage and current with different loads(a)50Ω(b)100 Ω(c)50Ω+1.5mH (d)50Ω+10mH

5.5 Chapter conclusion

In this chapter. Hardware experiments and analysis were performed on the proposed 17-level inverter. The PDPWM control strategy for controlling the proposed inverter is implemented using FPGA. Through performance analysis of the two driving circuits, the driving circuit that is more suitable for this experiment was selected. Finally, a prototype of the entire system was built, and the proposed inverter was studied under different load conditions. Finally, it was found that its performance was consistent with the design.

Chapter 6: Conclusion and future work

6.1 Conclusion

In this thesis, the multilevel inverters are discussed in detail. Through the review of topologies proposed by other scholars, it can be found that the current design requirements for multi-level inverter topologies are to use fewer switching devices to achieve more output voltage levels and high voltage gains, and to ensure that the output waveform has low harmonics. In that case, the cost factor is also considered. In addition, the total standing voltage of the switching device is also an important indicator. While increasing the output voltage gain, the voltage stress of the switching device will also increase accordingly. It is necessary to utilize switching devices that can withstand higher voltage to improve their reliability, which will also increase manufacturing costs. Therefore, how to design the topology to apply switching devices with smaller voltage stress to obtain a higher output voltage gain is also a challenge. This thesis proposes two multi-level inverters based on switched capacitor structures, which can use fewer devices to obtain higher output voltage levels and voltage gains, and the total voltage stress of the switching devices is low. At the same time, a parallel/series connected unit based on switched capacitors is proposed. This switched capacitor unit realizes the series and parallel connection of capacitors with fewer switching devices, allowing capacitors to be flexibly combined for charging or discharging. This unit can be combined with other topologies to obtain up to 3 times voltage gain when a parallel/series unit is utilized in the circuit. The 13-level switched capacitor inverter is the first to be proposed. It has a voltage gain of 3 times. The 17-level switched capacitor inverter is obtained by optimizing the position of the DC supply in the 13-level switched capacitor inverter topology. The latter can achieve a voltage gain of 4 times. This thesis conducts a simulation experiment on the proposed topology and makes a detailed comparison of the simulation results. The results show that the 17-level SCMLI proposed in this thesis uses 53% fewer switching devices compared to the 17-level H-bridge cascaded inverter, the 17-level diode-clamped inverter, and the 17-level flying

capacitor inverter. Additionally, compared to the 13-level SCMLI proposed in this thesis, the number of switches used per output level and per unit voltage gain is reduced by 35%. The total harmonic distortion (THD) of the 17-level SCMLI is 27% lower than that of the 13-level SCMLI. It can be found that the performance of the 17-level switched capacitor inverter is significantly better in all aspects. Subsequently, a hardware experimental study is conducted on the 17-level switched capacitor inverter. In the experimental part, FPGA was used to realize the code implementation of the control strategy based on PDPWM technology, and a logic analyzer was used for observation to ensure that the control signal was consistent with the design. A comparative study was also conducted on the gate driver circuit used to drive MOSFET, and a solution more suitable for this experiment was selected. The final experimental results are the same as the simulation results and are highly consistent with theoretical research in various cases.

6.2 Future work

This thesis only investigates the extended topology of 13-level SCMLI and the 17-level SCMLI at the simulation stage, without conducting hardware experiments. This aspect can be addressed in future work. The proposed extension methods for the two topologies are not the only possible approaches, and further exploration of alternative extension methods can be undertaken in the future.

The instantaneous charging current of the capacitor in the switched capacitor inverter is generally large. This feature can also be found in the topology proposed by other scholars. This thesis does not design corresponding measures to limit the charging current for the capacitor. The methods to reduce the capacitor charging current need to be studied in the future work.

The 17-level switched capacitor inverter proposed in this thesis has a lot of redundant circuits to generate the specific level of the output voltage. The redundant circuits can

be utilized to minimize switching transitions between voltage levels, thereby reducing overall losses. Additionally, redundant circuits can be employed to optimize the charging and discharging times of capacitors, enabling a reduction in capacitance. The switching states of the switches can be redesigned using the redundant circuit in the future.

Since the focus of this thesis is on the innovation of the topology for switched capacitor multilevel inverters, it does not focus on closed-loop control. Therefore, the closed-loop control for the two proposed topologies can be addressed in future work.

The experiment in this thesis is conducted by connecting a constant DC voltage source at the input. In the future, the prototype developed in this thesis can be connected to real energy storage devices or photovoltaic panels to validate the dynamic performance of the proposed topology.

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